PhyBOARD-Wega-AM335x Pin Configuration Table

Memory Address	Default Config	Input Enable	Pull Up/Pull Down	Mode	ocessor Pint	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7	Exp 0	Pin 0	Exp 1	Pin 1	Exp 2	Pin 2
0x0800	30	IEN	PU	0	U7	gpmc_ad0	mmc1_dat0_mux2						gpio1[0]						
0x0804	30	IEN	PU	0	V7	gpmc_ad1	mmc1_dat1_mux2						gpio1[1]						
0x0808	30	IEN	PU	0	R8	gpmc_ad2	mmc1_dat2_mux2						gpio1[2]						
0x080C	30	IEN	PU	0	T8	gpmc_ad3	mmc1_dat3_mux2						gpio1[3]						
0x0810	30	IEN	PU	0	U8	gpmc_ad4	mmc1_dat4_mux2						gpio1[4]						
0x0814	30	IEN	PU	0	V8	gpmc_ad5	mmc1_dat5_mux2						gpio1[5]						
0x0818	30	IEN	PU	0	R9	gpmc_ad6	mmc1_dat6_mux2						gpio1[6]						
0x081C	30	IEN	PU	0	T9	gpmc_ad7	mmc1_dat7_mux2						gpio1[7]						
0x0820	30	IEN	PU	0	U10	gpmc_ad8	lcd_data23	mmc1_dat0_mux0	mmc2_dat4_mux1	ehrpwm2A_mux1	pr1_mii_mt0_clk_mux0		gpio0[22]	X70	22				
0x0824	30	IEN	PU	0	T10	gpmc_ad9	lcd_data22	mmc1_dat1_mux0	mmc2_dat5_mux1	ehrpwm2B_mux1	pr1_mii0_col		gpio0[23]	X70	12				
0x0828	30	IEN	PU	0	T11	gpmc_ad10	lcd_data21	mmc1_dat2_mux0	mmc2_dat6_mux1	ehrpwm2_tripzone_input_mux1	pr1_mii0_txen_mux0		gpio0[26]	X70	2				
0x082C	30	IEN	PU	0	U12	gpmc_ad11	lcd_data20	mmc1_dat3_mux0	mmc2_dat7_mux1	ehrpwm0_synco_mux2	pr1_mii0_txd3_mux0		gpio0[27]	X70	23				
0x0830	30	IEN	PU	0	T12	gpmc_ad12	lcd_data19	mmc1_dat4_mux0	mmc2_dat0_mux1	eQEP2A_in_mux1	pr1_mii0_txd2_mux0	pr1_pru0_pru_r30[14]	gpio1[12]	X70	13				
0x0834	30	IEN	PU	0	R12	gpmc_ad13	lcd_data18	mmc1_dat5_mux0	mmc2_dat1_mux1	eQEP2B_in_mux1	pr1_mii0_txd1_mux0	pr1_pru0_pru_r30[15]	gpio1[13]	X70	3				
0x0838	30	IEN	PU	0	V13	gpmc_ad14	lcd_data17	mmc1_dat6_mux0	mmc2_dat2_mux1	eQEP2_index_mux1	pr1_mii0_txd0_mux0	pr1_pru0_pru_r31[14]	gpio1[14]	X70	24				
0x083C	30	IEN	PU	0	U13	gpmc_ad15	lcd_data16	mmc1_dat7_mux0	mmc2_dat3_mux1	eQEP2_strobe_mux1	pr1_ecap0_ecap_capin_apwm_o_mux0	pr1_pru0_pru_r31[15]	gpio1[15]	X70	4				
0x0840	9	IDIS	OFF	1	R13	gpmc_a0_mux0	gmii2_txen	rgmii2_tctl	rmii2_txen	gpmc_a16_mux0	pr1_mii_mt1_clk	ehrpwm1_tripzone_input_mux1	gpio1[16]						
0x0844	21	IEN	PD	1	V14	gpmc_a1_mux0	gmii2_rxdv	rgmii2_rctl	mmc2_dat0_mux0	gpmc_a17_mux0	pr1_mii1_txd3	ehrpwm0_synco_mux3	gpio1[17]						
0x0848	9	IDIS	OFF	1	U14	gpmc_a2_mux0	gmii2_txd3	rgmii2_td3	mmc2_dat1_mux0	gpmc_a18_mux0	pr1_mii1_txd2	ehrpwm1A_mux1	gpio1[18]						
0x084C	9	IDIS	OFF	1	T14	gpmc_a3_mux0	gmii2_txd2	rgmii2_td2	mmc2_dat2_mux0	gpmc_a19_mux0	pr1_mii1_txd1	ehrpwm1B_mux1	gpio1[19]						
0x0850	9	IDIS	OFF	1	R14	gpmc_a4_mux0	gmii2_txd1	rgmii2_td1	rmii2_txd1	gpmc_a20_mux0	pr1_mii1_txd0	eQEP1A_in_mux1	gpio1[20]						
0x0854	9	IDIS	OFF	1	V15	gpmc_a5_mux0	gmii2_txd0	rgmii2_td0	rmii2_txd0	gpmc_a21_mux0	pr1_mii1_rxd3	eQEP1B_in_mux1	gpio1[21]						
0x0858	21	IEN	PD	1	U15	gpmc_a6_mux0	gmii2_txclk	rgmii2_tclk	mmc2_dat4_mux0	gpmc_a22_mux0	pr1_mii1_rxd2	eQEP1_index_mux1	gpio1[22]						
0x085C	21	IEN	PD	1	T15	gpmc_a7_mux0	gmii2_rxclk	rgmii2_rclk	mmc2_dat5_mux0	gpmc_a23_mux0	pr1_mii1_rxd1	eQEP1_strobe_mux1	gpio1[23]						
0x0860	21	IEN	PD	1	V16	gpmc_a8_mux0	gmii2_rxd3	rgmii2_rd3	mmc2_dat6_mux0	gpmc_a24_mux0	pr1_mii1_rxd0	mcasp0_aclkx_mux3	gpio1[24]						
0x0864	21	IEN	PD	1	U16	gpmc_a9_mux0	gmii2_rxd2	rgmii2_rd2	mmc2_dat7_mux0/rmii2_crs_dv_mux2	gpmc_a25_mux0	pr1_mii_mr1_clk	mcasp0_fsx_mux3	gpio1[25]						
0x0868	21	IEN	PD	1	T16	gpmc_a10_mux0	gmii2_rxd1	rgmii2_rd1	rmii2_rxd1	gpmc_a26	pr1_mii1_rxdv	mcasp0_axr0_mux3	gpio1[26]						
0x086C	21	IEN	PD	1	V17	gpmc_a11_mux0	gmii2_rxd0	rgmii2_rd0	rmii2_rxd0	gpmc_a27	pr1_mii1_rxer	mcasp0_axr1_mux3	gpio1[27]						
0x0870	30	IEN	PU	0	T17	gpmc_wait0	gmii2_crs	gpmc_csn4	rmii2_crs_dv_mux0	mmc1_sdcd_mux0	pr1_mii1_col	uart4_rxd_mux2	gpio0[30]						
0x0874	21	IEN	PD	1	U17	gpmc_wpn	gmii2_rxer	gpmc_csn5	rmii2_rxer	mmc2_sdcd_mux0	pr1_mii1_txen	uart4_txd_mux2	gpio0[31]						
0x0878	21	IEN	PD	1	U18	gpmc_be1n_mux0	gmii2_col	gpmc_csn6	mmc2_dat3_mux0	gpmc_dir	pr1_mii1_rxlink	mcasp0_aclkr_mux3	gpio1[28]						
0x087C	8	IDIS	OFF	0	V6	gpmc_csn0							gpio1[29]						
0x0880	37	IEN	PU	7	U9	gpmc_csn1	gpmc_clk_mux1	mmc1_clk_mux0	pr1_edio_data_in6_mux0	pr1_edio_data_out6_mux0	pr1_pru1_pru_r30[12]	pr1_pru1_pru_r31[12]	gpio1[30]	X71	5				
0x0884	37	IEN	PU	7	V9	gpmc_csn2	gpmc_be1n_mux1	mmc1_cmd_mux0	pr1_edio_data_in7_mux0	pr1_edio_data_out7_mux0	pr1_pru1_pru_r30[13]	pr1_pru1_pru_r31[13]	gpio1[31]						
0x0888	37	IEN	PU	7	T13	gpmc_csn3	gpmc_a3_mux2	rmii2_crs_dv_mux1	mmc2_cmd_mux0	pr1_mii0_crs_mux0	pr1_mdio_data	EMU4_mux0	gpio2[0]						
0x088C	30	IEN	PU	0	V12	gpmc_clk_mux0	lcd_memory_clk_mux0	gpmc_wait1	mmc2_clk_mux0	pr1_mii1_crs_mux0	pr1_mdio_mdclk	mcasp0_fsr_mux3	gpio2[1]						
0x0890	8	IDIS	OFF	0	R7	gpmc_advn_ale		timer4_mux3					gpio2[2]						
0x0894	8	IDIS	OFF	0	T7	gpmc_oen_ren		timer7_mux3					gpio2[3]						
0x0898	8	IDIS	OFF	0	U6	gpmc_wen		timer6_mux3					gpio2[4]						
0x089C	8	IDIS	OFF	0	T6	gpmc_be0n_cle		timer5_mux3					gpio2[5]						
0x08A0	2f	IEN	OFF	7	R1	lcd_data0	gpmc_a0_mux1	pr1_mii_mt0_clk_mux1	ehrpwm2A_mux0		pr1_pru1_pru_r30[0]	pr1_pru1_pru_r31[0]	gpio2[6]	X70	5				
0x08A4	2f	IEN	OFF	7	R2	lcd_data1	gpmc_a1_mux1	pr1_mii0_txen_mux1	ehrpwm2B_mux0		pr1_pru1_pru_r30[1]	pr1_pru1_pru_r31[1]	gpio2[7]	X70	7				
0x08A8	2f	IEN	OFF	7	R3	lcd_data2	gpmc_a2_mux1	pr1_mii0_txd3_mux1	ehrpwm2_tripzone_input_mux0		pr1_pru1_pru_r30[2]	pr1_pru1_pru_r31[2]	gpio2[8]	X70	8				
0x08AC	2f	IEN	OFF	7	R4	lcd_data3	gpmc_a3_mux1	pr1_mii0_txd2_mux1	ehrpwm0_synco_mux1		pr1_pru1_pru_r30[3]	pr1_pru1_pru_r31[3]	gpio2[9]	X70	9				
0x08B0	2f	IEN	OFF	7	T1	lcd_data4	gpmc_a4_mux1	pr1_mii0_txd1_mux1	eQEP2A_in_mux0		pr1_pru1_pru_r30[4]	pr1_pru1_pru_r31[4]	gpio2[10]	X70	10				
0x08B4	2f	IEN	OFF	7	T2	lcd_data5	gpmc_a5_mux1	pr1_mii0_txd0_mux1	eQEP2B_in_mux0		pr1_pru1_pru_r30[5]	pr1_pru1_pru_r31[5]	gpio2[11]	X70	14				
0x08B8	2f	IEN	OFF	7	T3	lcd_data6	gpmc_a6_mux1	pr1_edio_data_in6_mux1	eQEP2_index_mux0	pr1_edio_data_out6_mux1	pr1_pru1_pru_r30[6]	pr1_pru1_pru_r31[6]	gpio2[12]	X70	15				
0x08BC	2f	IEN	OFF	7	T4	lcd_data7	gpmc_a7_mux1	pr1_edio_data_in7_mux1	eQEP2_strobe_mux0	pr1_edio_data_out7_mux1	pr1_pru1_pru_r30[7]	pr1_pru1_pru_r31[7]	gpio2[13]	X70	17				
0x08C0	2f	IEN	OFF	7	U1	lcd_data8	gpmc_a12	ehrpwm1_tripzone_input_mux0	mcasp0_aclkx_mux1	uart5_txd_mux2	pr1_mii0_rxd3	uart2_ctsn_mux1	gpio2[14]	X70	18				
0x08C4	2f	IEN	OFF	7	U2	lcd_data9	gpmc_a13	ehrpwm0_synco_mux0	mcasp0_fsx_mux1	uart5_rxd_mux2	pr1_mii0_rxd2	uart2_rtsn_mux1	gpio2[15]	X70	19				
0x08C8	a	IDIS	OFF	2	U3	lcd_data10	gpmc_a14	ehrpwm1A_mux0	mcasp0_axr0_mux1		pr1_mii0_rxd1	uart3_ctsn_mux1	gpio2[16]	X70	20				
0x08CC	a	IDIS	OFF	2	U4	lcd_data11	gpmc_a15	ehrpwm1B_mux0	mcasp0_ahclkr_mux1	mcasp0_axr2_mux2	pr1_mii0_rxd0	uart3_rtsn_mux1	gpio2[17]	X70	25				
0x08D0	2f	IEN	OFF	7	V2	lcd_data12	gpmc_a16_mux1	eQEP1A_in_mux0	mcasp0_aclkr_mux1	mcasp0_axr2_mux3	pr1_mii0_rxlink	uart4_ctsn_mux1	gpio0[8]	X70	27				
0x08D4	2f	IEN	OFF	7	V3	lcd_data13	gpmc_a17_mux1	eQEP1B_in_mux0	mcasp0_fsr_mux1	mcasp0_axr3_mux3	pr1_mii0_rxer	uart4_rtsn_mux1	gpio0[9]	X70	28				
0x08D8	2f	IEN	OFF	7	V4	lcd_data14	gpmc_a18_mux1	eQEP1_index_mux0	mcasp0_axr1_mux1	uart5_rxd_mux1	pr1_mii_mr0_clk	uart5_ctsn_mux1	gpio0[10]	X70	29				
0x08DC	2f	IEN	OFF	7	T5	lcd_data15	gpmc_a19_mux1	eQEP1_strobe_mux0	mcasp0_ahclkx_mux1	mcasp0_axr3_mux2	pr1_mii0_rxdv	uart5_rtsn_mux1	gpio0[11]	X70	30				
0x08E0	27	IEN	PD	7	U5	lcd_vsync	gpmc_a8_mux1	gpmc_a1_mux2	pr1_edio_data_in2	pr1_edio_data_out2	pr1_pru1_pru_r30[8]	pr1_pru1_pru_r31[8]	gpio2[22]	X70	35				
0x08E4	27	IEN	PD	7	R5	lcd_hsync	gpmc_a9_mux1	gpmc_a2_mux2	pr1_edio_data_in3	pr1_edio_data_out3	pr1_pru1_pru_r30[9]	pr1_pru1_pru_r31[9]	gpio2[23]	X70	34				
0x08E8	27	IEN	PD	7	V5	lcd_pclk	gpmc_a10_mux1	pr1_mii0_crs_mux1	pr1_edio_data_in4	pr1_edio_data_out4	pr1_pru1_pru_r30[10]	pr1_pru1_pru_r31[10]	gpio2[24]	X70	32				
0x08EC	27	IEN	PD	7	R6	lcd_ac_bias_en	gpmc_a11_mux1	pr1_mii1_crs_mux1	pr1_edio_data_in5	pr1_edio_data_out5	pr1_pru1_pru_r30[11]	pr1_pru1_pru_r31[11]	gpio2[25]	X70	33				
0x08F0	30	IEN	PU	0	F17	mmc0_dat3	gpmc_a20_mux1	uart4_ctsn_mux0	timer5_mux0	uart1_dcdn_mux1	pr1_pru0_pru_r30[8]	pr1_pru0_pru_r31[8]	gpio2[26]						
0x08F4	30	IEN	PU	0	F18	mmc0_dat2	gpmc_a21_mux1	uart4_rtsn_mux0	timer6_mux0	uart1_dsrn_mux1	pr1_pru0_pru_r30[9]	pr1_pru0_pru_r31[9]	gpio2[27]						
0x08F8	30	IEN	PU	0	G15	mmc0_dat1	gpmc_a22_mux1	uart5_ctsn_mux0	uart3_rxd_mux2	uart1_dtrn_mux1	pr1_pru0_pru_r30[10]	pr1_pru0_pru_r31[10]	gpio2[28]						
0x08FC	30	IEN	PU	0	G16	mmc0_dat0	gpmc_a23_mux1	uart5_rtsn_mux0	uart3_txd_mux2	uart1_rin_mux1	pr1_pru0_pru_r30[11]	pr1_pru0_pru_r31[11]	gpio2[29]						
0x0900	30	IEN	PU	0	G17	mmc0_clk	gpmc_a24_mux1	uart3_ctsn_mux0	uart2_rxd_mux2	dcan1_tx_mux2	pr1_pru0_pru_r30[12]	pr1_pru0_pru_r31[12]	gpio2[30]						
0x0904	30	IEN	PU	0	G18	mmc0_cmd	gpmc_a25_mux1	uart3_rtsn_mux0	uart2_txd_mux2	dcan1_rx_mux2	pr1_pru0_pru_r30[13]	pr1_pru0_pru_r31[13]	gpio2[31]						
0x0908	27	IEN	PD	7	H16	gmii1_col	rmii2_refclk	spi1_sclk_mux1	uart5_rxd_mux0	mcasp1_axr2_mux1	mmc2_dat3_mux2	mcasp0_axr2_mux4	gpio3[0]	X69	32				
0x090C	21	IEN	PD	1	H17	gmii1_crs	rmii1_crs_dv	spi1_d0_mux1	I2C1_SDA_mux0	mcasp1_aclkx_mux1	uart5_ctsn_mux2	uart2_rxd_mux1	gpio3[1]						
0x0910	21	IEN	PD	1	J15	gmii1_rxer	rmii1_rxer	spi1_d1_mux1	I2C1_SCL_mux0	mcasp1_fsx_mux1	uart5_rtsn_mux2	uart2_txd_mux1	gpio3[2]						
0x0914	9	IDIS	OFF	1	J16	gmii1_txen	rmii1_txen	rgmii1_tctl	timer4_mux0	mcasp1_axr0_mux1	eQEP0_index_mux1	mmc2_cmd_mux2	gpio3[3]	X69	25				
0x0918	27	IEN	PD	7	J17	gmii1_rxdv	lcd_memory_clk_mux1	rgmii1_rctl	uart5_txd_mux1	mcasp1_aclkx_mux0	mmc2_dat0_mux2	mcasp0_aclkr_mux2	gpio3[4]	X69	26				
0x091C	27	IEN	PD	7	J18	gmii1_txd3	dcan0_tx_mux0	rgmii1_td3	uart4_rxd_mux0	mcasp1_fsx_mux0	mmc2_dat1_mux2	mcasp0_fsr_mux2	gpio0[16]	X69	28				
0x0920	27	IEN	PD	7	K15	gmii1_txd2	dcan0_rx_mux0	rgmii1_td2	uart4_txd_mux0	mcasp1_axr0_mux0	mmc2_dat2_mux2	mcasp0_ahclkx_mux2	gpio0[17]	X69	30				
0x0924	9	IDIS	OFF	1	K16	gmii1_txd1	rmii1_txd1	rgmii1_td1	mcasp1_fsr_mux1	mcasp1_axr1_mux0	eQEP0A_in_mux1	mmc1_cmd_mux1	gpio0[21]						
0x0928	9	IDIS	OFF	1	K17	gmii1_txd0	rmii1_txd0	rgmii1_td0	mcasp1_axr2_mux0	mcasp1_aclkr_mux0	eQEP0B_in_mux1	mmc1_clk_mux1	gpio0[28]						
0x092C	f	IDIS	OFF	7	K18	gmii1_txclk	uart2_rxd_mux0	rgmii1_tclk	mmc0_dat7	mmc1_dat0_mux1	uart1_dcdn_mux0	mcasp0_aclkx_mux2	gpio3[9]						
0x0930	27	IEN	PD	7	L18	gmii1_rxclk	uart2_txd_mux0	rgmii1_rclk	mmc0_dat6	mmc1_dat1_mux1	uart1_dsrn_mux0	mcasp0_fsx_mux2	gpio3[10]						
0x0934	f	IDIS	OFF	7	L17	gmii1_rxd3	uart3_rxd_mux0	rgmii1_rd3	mmc0_dat5	mmc1_dat2_mux1	uart1_dtrn_mux0	mcasp0_axr0_mux2	gpio2[18]						
0x0938	f	IDIS	OFF	7	L16	gmii1_rxd2	uart3_txd_mux0	rgmii1_rd2	mmc0_dat4	mmc1_dat3_mux1	uart1_rin_mux0	mcasp0_axr1_mux2	gpio2[19]						
0x093C	21	IEN	PD	1	L15	gmii1_rxd1	rmii1_rxd1	rgmii1_rd1	mcasp1_axr3_mux0	mcasp1_fsr_mux0	eQEP0_strobe_mux1	mmc2_clk_mux2	gpio2[20]	X69	27				
0x0940	21	IEN	PD	1	M16	gmii1_rxd0	rmii1_rxd0	rgmii1_rd0	mcasp1_ahclkx_mux0	mcasp1_ahclkr_mux0	mcasp1_aclkr_mux1	mcasp0_axr3_mux4	gpio2[21]						
0x0944	20	IEN	PD	0	H18	rmii1_refclk	xdma_event_intr2_mux0	spi1_cs0_mux1	uart5_txd_mux0	mcasp1_axr3_mux1	mmc0_pow_mux0	mcasp1_ahclkx_mux1	gpio0[29]						
0x0948	70	IEN	PU	0	M17	mdio_data	timer6_mux2	uart5_rxd_mux3	uart3_ctsn_mux2	mmc0_sdcd_mux2	mmc1_cmd_mux2	mmc2_cmd_mux1	gpio0[0]						
0x094C	10	IDIS	PU	0	M18	mdio_clk	timer5_mux2	uart5_txd_mux3	uart3_rtsn_mux2	mmc0_sdwp_mux2	mmc1_clk_mux2	mmc2_clk_mux1	gpio0[1]						
0x0950	20	IEN	PD	0	A17	spi0_sclk	uart2_rxd_mux3	I2C2_SDA_mux2	ehrpwm0A_mux1	pr1_uart0_cts_n_mux0	pr1_edio_sof	EMU2_mux1	gpio0[2]	X69	8	X69	31		
0x0954	20	IEN	PD	0	B17	spi0_d0	uart2_txd_mux3	I2C2_SCL_mux2	ehrpwm0B_mux1	pr1_uart0_rts_n_mux0	pr1_edio_latch_in	EMU3_mux1	gpio0[3]	X69	6	X69	33		

0x0958	30	IEN	PU	0	B16	spi0_d1	mmc1_sdwp_mux0	I2C1_SDA_mux3	ehrpwm0_tripzone_input_mux1	pr1_uart0_rxd_mux0	pr1_edio_data_in0	pr1_edio_data_out0	gpio0[4]	X69	7					
0x095C	30	IEN	PU	0	A16	spi0_cs0	mmc2_sdwp_mux0	I2C1_SCL_mux3	ehrpwm0_synci_mux1	pr1_uart0_txd_mux0	pr1_edio_data_in1	pr1_edio_data_out1	gpio0[5]	X69	5					
0x0960	37	IEN	PU	7	C15	spi0_cs1	uart3_rxd_mux1	eCAP1_in_PWM1_out_mux0	mmc0_pow_mux1	xdma_event_intr2_mux1	mmc0_sdcd_mux0	EMU4_mux1	gpio0[6]	X69	35	X70	38			
0x0964	8	IDIS	OFF	0	C18	eCAP0_in_PWM0_out	uart3_txd_mux1	spi1_cs1_mux1	pr1_ecap0_ecap_capin_apwm_o_mux1	spi1_sclk_mux0	mmc0_sdwp_mux0	xdma_event_intr2_mux2	gpio0[7]	X69	36	X69	38			
0x0968	12	IDIS	PU	2	E18	uart0_ctsn	uart4_rxd_mux1	dcan1_tx_mux0	I2C1_SDA_mux1	spi1_d0_mux0	timer7_mux0	pr1_edc_sync0_out	gpio1[8]							
0x096C	32	IEN	PU	2	E17	uart0_rtsn	uart4_txd_mux1	dcan1_rx_mux0	I2C1_SCL_mux1	spi1_d1_mux0	spi1_cs0_mux2	pr1_edc_sync1_out	gpio1[9]							
0x0970	30	IEN	PU	0	E15	uart0_rxd	spi1_cs0_mux3	dcan0_tx_mux1	I2C2_SDA_mux1	eCAP2_in_PWM2_out_mux0	pr1_pru1_pru_r30[14]	pr1_pru1_pru_r31[14]	gpio1[10]	X69	10					
0x0974	0	IDIS	PD	0	E16	uart0_txd	spi1_cs1_mux3	dcan0_rx_mux1	I2C2_SCL_mux1	eCAP1_in_PWM1_out_mux1	pr1_pru1_pru_r30[15]	pr1_pru1_pru_r31[15]	gpio1[11]	X69	12					
0x0978	28	IEN	OFF	0	D18	uart1_ctsn	timer6_mux1	dcan0_tx_mux2	I2C2_SDA_mux0	spi1_cs0_mux0	pr1_uart0_cts_n_mux1	pr1_edc_latch0_in	gpio0[12]							
0x097C	0	IDIS	PD	0	D17	uart1_rtsn	timer5_mux1	dcan0_rx_mux2	I2C2_SCL_mux0	spi1_cs1_mux0	pr1_uart0_rts_n_mux1	pr1_edc_latch1_in	gpio0[13]							
0x0980	30	IEN	PU	0	D16	uart1_rxd	mmc1_sdwp_mux1	dcan1_tx_mux1	I2C1_SDA_mux2		pr1_uart0_rxd_mux1	pr1_pru1_pru_r31[16]	gpio0[14]							
0x0984	0	IDIS	PD	0	D15	uart1_txd	mmc2_sdwp_mux1	dcan1_rx_mux1	I2C1_SCL_mux2		pr1_uart0_txd_mux1	pr1_pru0_pru_r31[16]	gpio0[15]							
0x0988	30	IEN	PU	0	C17	I2C0_SDA	timer4_mux2	uart2_ctsn_mux0	eCAP2_in_PWM2_out_mux2				gpio3[5]	X69	11	X71	16			
0x098C	30	IEN	PU	0	C16	I2C0_SCL	timer7_mux2	uart2_rtsn_mux0	eCAP1_in_PWM1_out_mux2				gpio3[6]	X69	13	X71	15			
0x0990	20	IEN	PD	0	A13	mcasp0_aclkx_mux0	ehrpwm0A_mux0		spi1_sclk_mux2	mmc0_sdcd_mux1	pr1_pru0_pru_r30[0]	pr1_pru0_pru_r31[0]	gpio3[14]	X71	1					
0x0994	20	IEN	PD	0	B13	mcasp0_fsx_mux0	ehrpwm0B_mux0		spi1_d0_mux2	mmc1_sdcd_mux1	pr1_pru0_pru_r30[1]	pr1_pru0_pru_r31[1]	gpio3[15]	X71	2					
0x0998	20	IEN	PD	0	D12	mcasp0_axr0_mux0	ehrpwm0_tripzone_input_mux0		spi1_d1_mux2	mmc2_sdcd_mux1	pr1_pru0_pru_r30[2]	pr1_pru0_pru_r31[2]	gpio3[16]	X71	3					
0x099C	c	IDIS	OFF	4	C12	mcasp0_ahclkr_mux0	ehrpwm0_synci_mux0	mcasp0_axr2_mux0	spi1_cs0_mux4	eCAP2_in_PWM2_out_mux1	pr1_pru0_pru_r30[3]	pr1_pru0_pru_r31[3]	gpio3[17]							
0x09A0	27	IEN	PD	7	B12	mcasp0_aclkr_mux0	eQEP0A_in_mux0	mcasp0_axr2_mux1	mcasp1_aclkx_mux2	mmc0_sdwp_mux1	pr1_pru0_pru_r30[4]	pr1_pru0_pru_r31[4]	gpio3[18]							
0x09A4	27	IEN	PD	7	C13	mcasp0_fsr_mux0	eQEP0B_in_mux0	mcasp0_axr3_mux1	mcasp1_fsx_mux2	EMU2_mux2	pr1_pru0_pru_r30[5]	pr1_pru0_pru_r31[5]	gpio3[19]							
0x09A8	0	IDIS	PD	0	D13	mcasp0_axr1_mux0	eQEP0_index_mux0		mcasp1_axr0_mux2	EMU3_mux2	pr1_pru0_pru_r30[6]	pr1_pru0_pru_r31[6]	gpio3[20]	X71	4					
0x09AC	0	IDIS	PD	0	A14	mcasp0_ahclkx_mux0	eQEP0_strobe_mux0	mcasp0_axr3_mux0	mcasp1_axr1_mux1	EMU4_mux2	pr1_pru0_pru_r30[7]	pr1_pru0_pru_r31[7]	gpio3[21]	X71	6					
0x09B0	23	IEN	PD	3	A15	xdma_event_intr0		timer4_mux1	clkout1	spi1_cs1_mux2	pr1_pru1_pru_r31[16]	EMU2_mux0	gpio0[19]							
0x09B4	27	IEN	PD	7	D14	xdma_event_intr1		tclkin	clkout2	timer7_mux1	pr1_pru0_pru_r31[16]	EMU3_mux0	gpio0[20]	X69	37					
0x09B8	30	IEN	PU	0	A10	nRESETIN_OUT								X69	23	X69	43	X71	8	
0x09C0	30	IEN	PU	0	B18	nNMI								X69	45					
0x09D0	30	IEN	PU	0	C11	TMS								X69	15					
0x09D4	30	IEN	PU	0	B11	TDI								X69	17					
0x09D8	30	IEN	PU	0	A11	TDO								X69	18					
0x09DC	30	IEN	PU	0	A12	TCK								X69	20					
0x09E0	20	IEN	PD	0	B10	nTRST								X69	16					
0x09E4	30	IEN	PU	0	C14	EMU0							gpio3[7]	X69	42					
0x09E8	30	IEN	PU	0	B14	EMU1							gpio3[8]	X69	44					
0x09F8	30	IEN	PU	0	B5	RTC_porz														
0x09FC	28	IEN	OFF	0	C6	PMIC_POWER_EN														
0x0A00	28	IEN	OFF	0	C5	EXT_WAKEUP								X69	39					
0x0A04	20	IEN	PD	0	B4	ENZ_KALDO_1P8V														
0x0A1C	8	IDIS	OFF	0	F16	USB0_DRVVBUS							gpio0[18]							
0x0A34	8	IDIS	OFF	0	F15	USB1_DRVVBUS							gpio3[13]	X69	52					