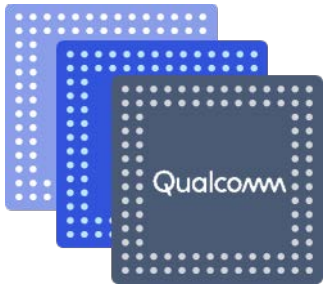
SDM670/SDM710 Linux Android Display Overview

Qualcomm
Qualcomm Technologies, Inc.

80-PD126-13 Rev. B



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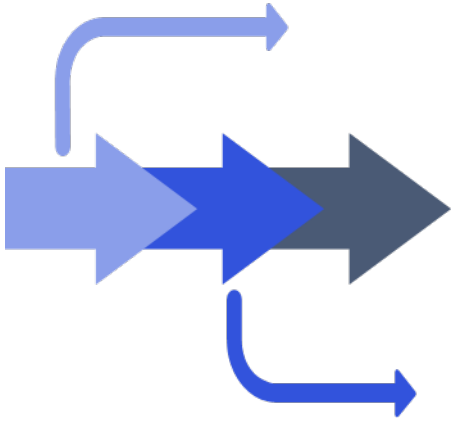
Revision History

Revision	Date	Description
A	August 2017	Initial release
B	April 2018	Updated to align with the SDM710 and SDM670 CS details and configuration; this document should be read in its entirety.

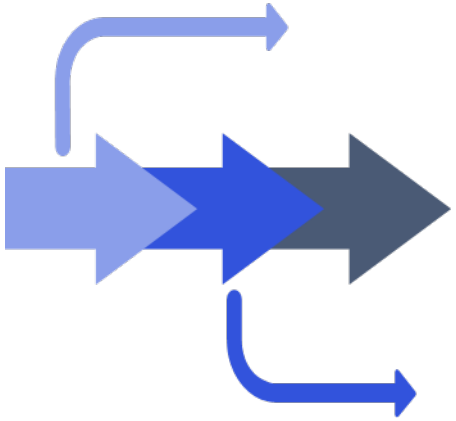
Contents



Objective

Document Objective

- This document serves as an entry point for OEM managers and engineers to understand display architectural and project planning information.
- Use this document to understand the following:
  - New features and product improvements for display in this chipset
  - Chipset and SDM-level hardware architecture
  - Software architecture
  - Key architectural changes compared to the reference chipset
  - Hardware and software migration details to help plan for the development effort
  - New tools and tool versions necessary to support development and commercialization of display on this SDM
  - Debug tools for display high-level software design and directory structure
  - Memory requirements



Product Features

Key Improvements and New Features

- Display serial interface (DSI) 1.2 added 10-bit DSI uncompressed
- DisplayPort (DP) 1.4 supports HBR3 and 2-lane concurrent operation with USB 3.0
- Picture quality improvements
  - QSEED3 scaler alpha scaling improvement
  - New version of Assertive display (AD), improves tone mapping
  - Added Destination surface processor pipes (DSPP) on layer mixers for external Virtual reality (VR) displays
  - VR dual panel skew support
  - 3D gamut LUT on VIG pipe for HDR tone mapping (supported only on SDM710)
- Supports more layers in Layer mixer (LM) for power and performance improvement
- Supports dim layer in LM without using Qualcomm® Adreno™ GPU or Qualcomm® Adreno™ DPU source pipe
- Universal bandwidth compression (UBWC 2.0)
  - E2E 10 bps UBWC support, added UBWC_P010 (10-bit YUV) format in SDM710
- Additional bandwidth reductions and power savings
- Smart direct memory access (SDMA) 2.0
  - Added SDMA 2.0 to VIG pipes, up to two RGB source layer support with single VIG pipe
  - Removed hardware limitations from previous version
  - Added exclusive rectangle support, portion of the rectangle is excluded from the hardware fetch to reduce power consumption
- LUT programming and read via Advanced eXtensible Interface (AXI) for better performance and to reduce CPU/Advanced high-performance bus (AHB) load

Display Features Summary and Software Plan

Feature	Description	Change	Feature type	Software plan
DP 1.4	Added support for ▪ 8.1 Gb data per lane ▪ USB 3.0 concurrency between DP and high-speed USB	Improved hardware block	Performance	Yes (no plan for multiple stream transport (MST))
10-bit DSI uncompressed	Supports uncompressed 30 bpp data over DSI D-PHY/C-PHY	Improved hardware block	Quality improvement	Yes (D-PHY) No (C-PHY)
SDMA 2.0	▪ Improved hardware architecture over SDMA 1.0 block ▪ Added SDMA 2.0 to VIG pipes ▪ Added exclusive rectangle support	Improved hardware block	Power and performance improvement	Yes
UBWC 2.0	Reduced bandwidth requirement and added UBWC_P010 support	Improved hardware block	Power and performance improvement	Yes
Layer mixer	Blends maximum 10 layers	Improved hardware block	Power and performance improvement	Yes
Dim layer	Supports dim layer without Adreno GPU or Adreno DPU resource	Improved hardware block	New feature	Yes

Display Features Summary and Software Plan (cont.)

Feature	Description	Change	Feature type	Software plan
Inline rotation	One-step Inline rotation as compared to two steps	Redesigned hardware block	Power performance improvement	Yes
QSEED3 scaler	Improved alpha scaling	Improved hardware block	Quality improvement	Yes
AD4	New version of assertive display	Improved hardware block	Quality improvement	Yes
3D LUT on VIG (SDM710)	Uses Adreno DPU for source tone mapping instead of Adreno GPU, improved HDR tone mapping	Improved hardware block	Quality improvement	No
LUT DMA	LUT programming and read via AXI port instead of AHB	Added hardware block	Performance	Yes
Dedicated hardware cursor pipes removal	Use of SDMA pipes is a better solution along with eight blending stages for a simplified architecture	Removed hardware	N/A	N/A

KPI Summary – SDM670

- Supports upto two concurrent displays
  - DSI 0
    - FHD+ (10-bit) without Display stream compression (DSC)
    - Supports VESA DSC 1.1
  - DisplayPort
    - 8.1 Gbps/lane
    - Without USB 3.0 concurrency – 4 lanes
      - 1 × 4096 × 2160 30 bpp at 30 Hz
    - With USB 3.0 concurrency – 2 lanes
      - 1 × 3840 × 2160 24 bpp at 30 Hz
- Maximum concurrency configurations
  - FHD+ (10-bit) at 60 Hz primary + 4K at 30 Hz DP or 1080 × 1920 Wi-Fi display (WFD)

Note: For 19:9 and higher resolutions, Adreno DPU may not operate at the lowest voltage corner, and might consume more power compared to the 16:9 resolution. Reducing the panel blanking might help Adreno DPU to operate at a lower voltage corner.

Assumptions for calculation: Video mode panel with 20% panel blanking and 4-lane DSI configuration.

KPI Summary – SDM710

- Supports upto two concurrent displays
  - DSI 0 and DSI 1
    - QHD+ (10-bit) without Display stream compression (DSC)
    - Supports VESA DSC 1.1
  - DisplayPort
    - 8.1 Gbps/lane
    - Without USB 3.0 concurrency – 4 lanes
      - 1 × 4096 × 2160 30 bpp at 30 Hz
    - With USB 3.0 concurrency – 2 lanes
      - 1 × 3840 × 2160 24 bpp at 30 Hz
- Maximum concurrency configurations
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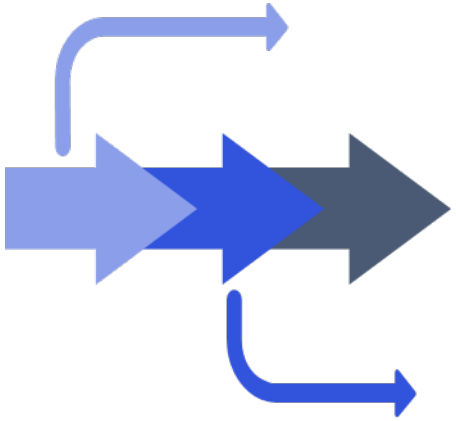
Note: For 19:9 and higher resolutions, Adreno DPU may not operate at the lowest voltage corner, and might consume more power compared to the 16:9 resolution. Reducing the panel blanking might help the Adreno DPU to operate at a lower voltage corner.

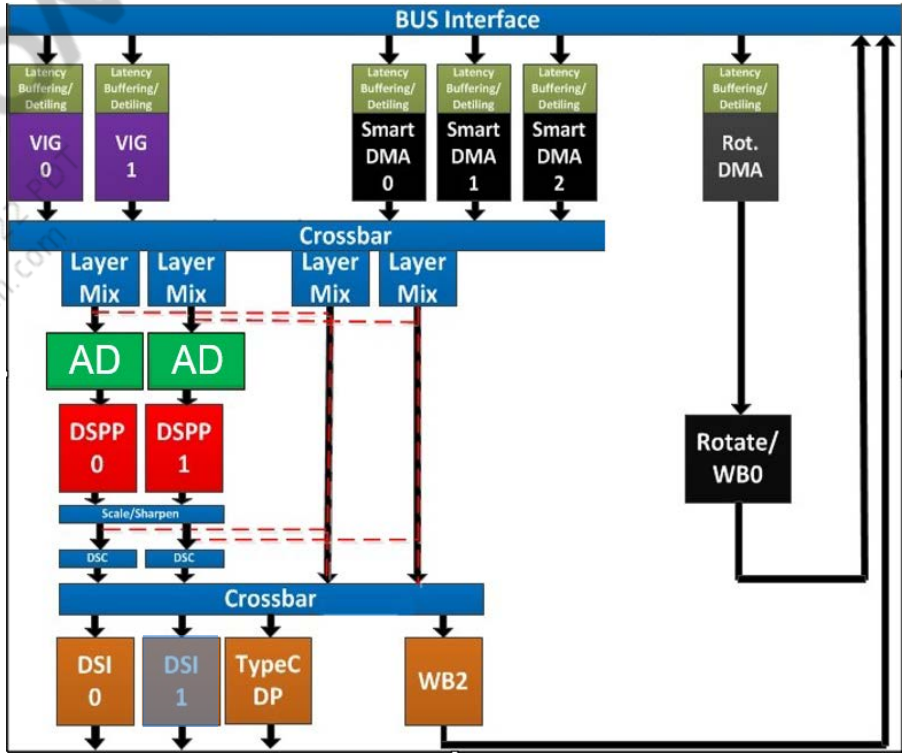
Assumptions for calculation: Video mode panel with 20% panel blanking & 4-lane DSI configuration



System Architecture

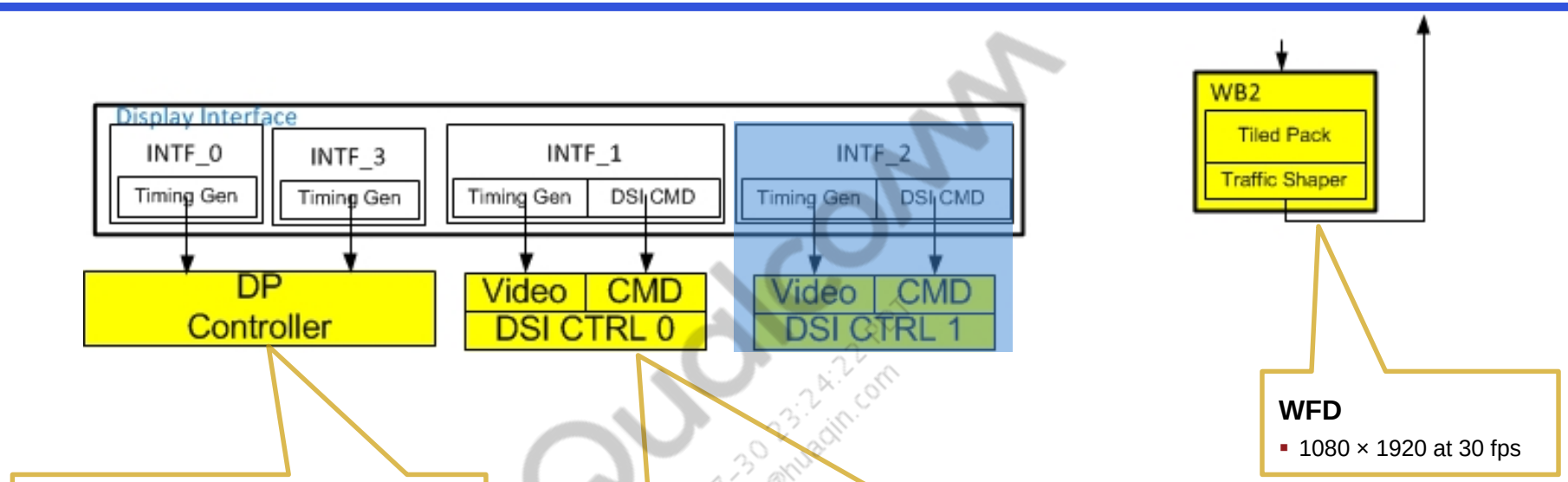
Adreno DPU775 Overview

- Adreno display processing unit (DPU)
  - Provides hardware-accelerated image processing, rapid transfer of image data to display interfaces, and enhanced on-screen image quality.
- Source surface processor (VIG and DMA source surface processor pipes (SSPP))
  - Format conversion and quality improvements for source surfaces. For example, video and graphics.
- Layer mixer (LM)
  - Blends and mixes source surface together
- Destination surface processor pipes (DSPP)
  - Conversion, correction, adjustment based on panel characteristics
- Display stream compression (DSC)
- Write back/rotation
  - Writes back to memory and rotates if needed
- Display interface
  - Timing generator and interface connecting to display peripheral
- Scale/sharpen
  - Scales and sharpens the final composed image that goes to the panel



Note: DSI 1 is available only in SDM710.

Display Peripheral



DisplayPort

- DP 1.4 with 10-bit support
- Supports 30 bpp/24 bpp/18 bpp
- Supports RGB888, YUV422/YUV420
- Supports HDCP 2.2 and HDCP 1.3
- Supports up to HBR3 (8.1 GHz)
- Supports up to 3840 × 2160 at 30 Hz with USB 3.0 concurrency over Type-C
- Supports single display up to 4096 × 2160 at 30 Hz with four data lanes (no USB 3.0)

MIPI DSI

- Two MIPI DSI
- Supports both smart and dumb displays
- One clock lane and up to four data lanes support for each DSI with D-PHY
- Up to 2.5 Gbps per lane with 24 bpp support or 30 bpp with D-PHY
- DATA ± (4 lanes), CLK ± (1 lane)
- Supports compressed or uncompressed 30 bpp (10 bpc) data over D-PHY

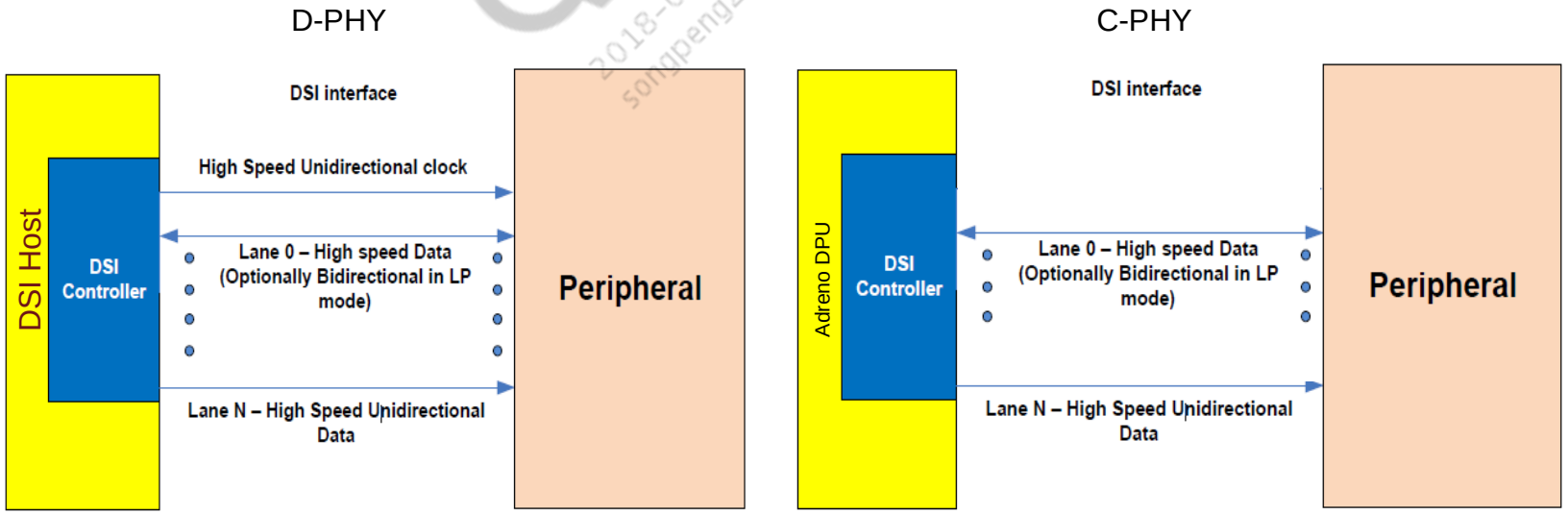
WFD

- 1080 × 1920 at 30 fps

Note: INTF_2 is available only in the SDM710 chipset.

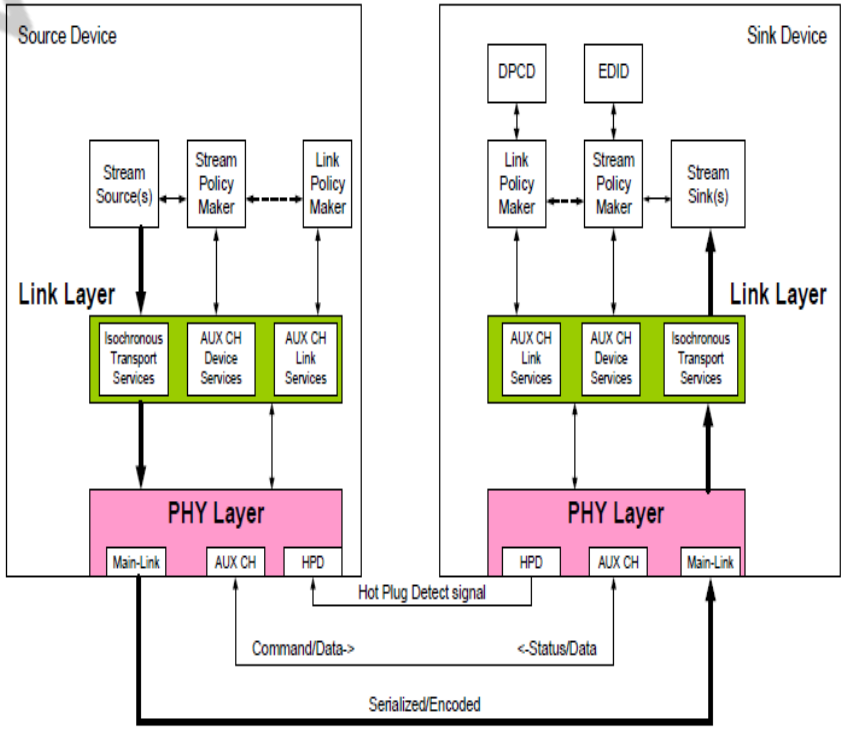
MIPI DSI

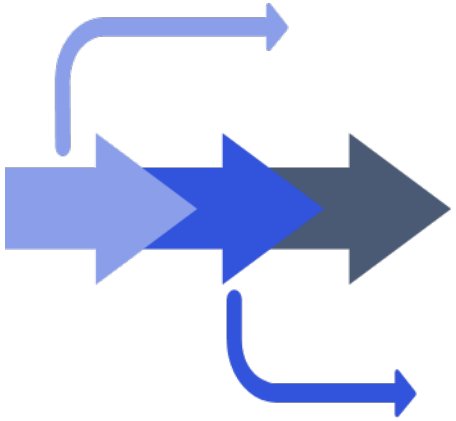
- Two DSI interfaces are implemented to support the MIPI Alliance standard for DSI
  - Supports DSI 1.2 with data rates up to 2.5 Gbps per lane with D-PHY
    - In D-PHY mode, each DSI interface supports one differential clock lane and up to four differential data lanes
  - Supports up to 5.71 Gbps per lane with C-PHY (No software support)
    - In C-PHY mode, each DSI interface supports up to three trios (total six trios)
- DSI-compliant peripherals operate in two modes
  - Command mode
  - Video mode



DisplayPort Tx

- DP 1.4
  - See the DP 1.4 specification at http://www.vesa.org
- HDCP 2.2 and HDCP 1.3
- Supports RGB 30 bpp/24 bpp/18 bpp, YUV420, and YUV422
- 1/2/4 lanes support
  - 8.1/5.4/2.7/1.62 Gbps per lane
- 4K × 2K resolution at 30 fps with USB 3.0 concurrency
- In USB alternate mode, either USB 3.0 or DP 1.4 is supported
- Concurrency with USB 3.0
  - Enables DP (2-lanes) + USB 3.0 (2-lanes) + USB 2.0 all through one USB Type-C connector

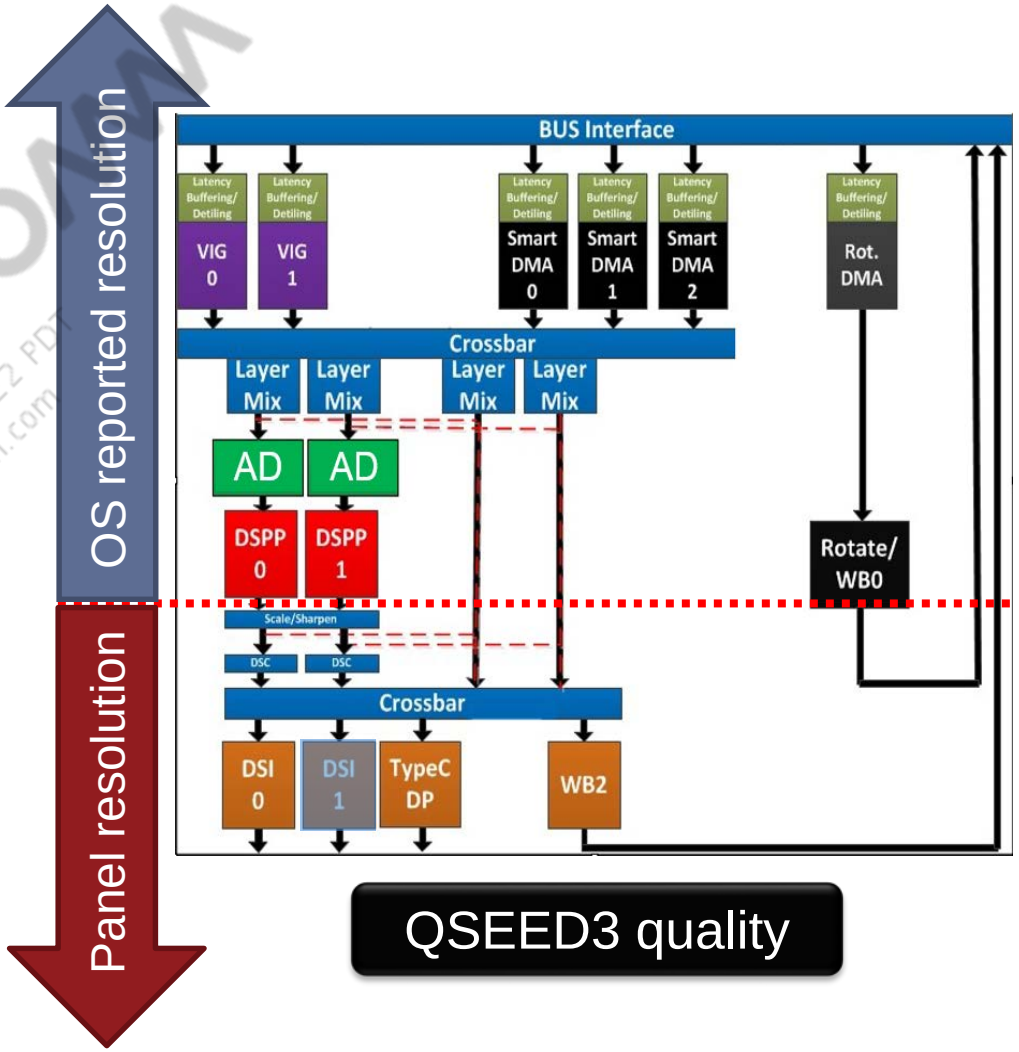




Hardware Features

Destination Scaling/Sharpening

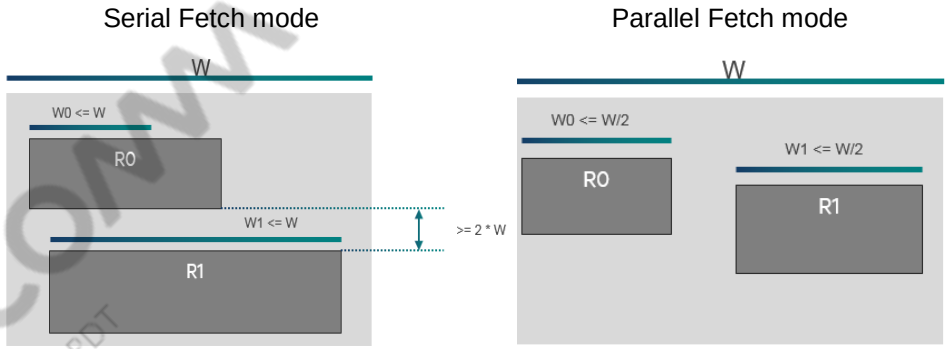
- Composes and blends layers in low resolution and upscales the final composed image to panel resolution
- Separates the physical panel resolution from the resolution that is reported to the operating system
- Saves power as layers are composed and blended in low resolution
- Allows full screen/final image sharpening with QSEED3



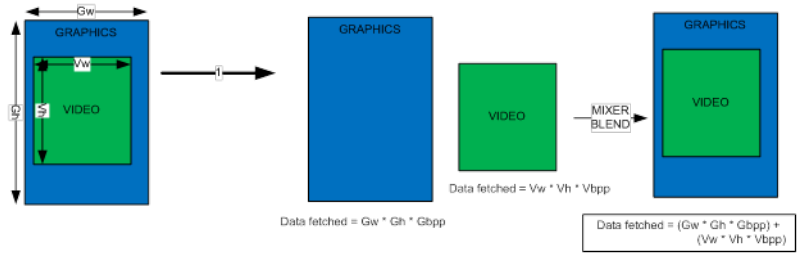
Note: Resolution switch requires reboot of operating system framework.
DSI 1 is available only in SDM710.

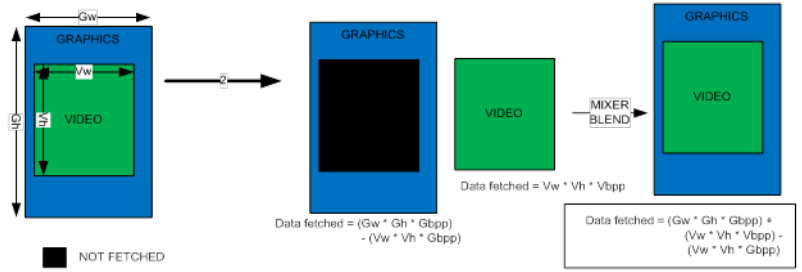
SDMA 2.0

- SDMA allows two RGB source layers with a single pipe
- Available on VIG and DMA pipes
- Supports source split
- Supports both horizontal flip and vertical flip
- Supports overlapping layers, maximum two layers
- Two rectangles can have different formats
- Parallel Fetch mode
  - When the rectangles share a scanline
  - Maximum rectangle width is half of the SSPP width (1280)
- Serial Fetch mode/Time Multiplex mode
  - When one rectangle needs to be processed before the second rectangle
  - Maximum width supported is same as the SSPP width (2560)
  - Rectangle R1 starts at least two linear lines or two UBWC tile rows (eight lines) after Rectangle R0
- Adds an exclusive rectangle
  - Portion of the rectangle is excluded from hardware fetching of the source rectangle
- Restrictions
  - Only ARGB formats are supported
  - No scaling



Video surface on top of an ARGB surface exclusive rectangle comparison





Supported Color Formats

Format						FOURCC/ Common name		IN			Out	
								VIG	DMA	DMA_ROT	WB2 Line	WB0 Block
RGB												
	Bits per component											
	A\X	R\Y	G\U	B\V	Avg per Pixel							
	Linear (Uncompressed)											
Interleaved RGB												
RGB565	0	5	6	5	16	RGB565		✓	✓	✓	✓	✓
RGB888	0	8	8	8	24	RGB888		✓	✓	✓	✓	✓
ARGB8888	8	8	8	8	32	ARGB8888		✓	✓	✓	✓	✓
RGBA8888	8	8	8	8	32	RGBA8888		✓	✓	✓	✓	✓
XRGB8888	8	8	8	8	32	XRGB8888		✓	✓	✓	✓	✓
RGBX8888	8	8	8	8	32	RGBX8888		✓	✓	✓	✓	✓
ARGB1555	1	5	5	5	16	ARGB1555		✓	✓	✓	✓	✓
RGBA5551	1	5	5	5	16	RGBA5551		✓	✓	✓	✓	✓
XRGB1555	1	5	5	5	16	XRGB1555		✓	✓	✓	✓	✓
RGBX5551	1	5	5	5	16	RGBX5551		✓	✓	✓	✓	✓
ARGB4444	4	4	4	4	16	ARGB4444		✓	✓	✓	✓	✓
RGBA4444	4	4	4	4	16	RGBA4444		✓	✓	✓	✓	✓
RGBX4444	4	4	4	4	16	RGBX4444		✓	✓	✓	✓	✓
XRGB4444	4	4	4	4	16	XRGB4444		✓	✓	✓	✓	✓
ARGB2 10 10 10	2	10	10	10	32	ARGB2 10 10 10		✓	✓	✓	✓	✓
XRGB2 10 10 10	2	10	10	10	32	XRGB2 10 10 10		✓	✓	✓	✓	✓
RGBA10 10 10 2	2	10	10	10	32	RGBA10 10 10 2		✓	✓	✓	✓	✓

Supported Color Formats (cont.)

Format						FOURCC/ Common name		IN			Out	
								VIG	DMA	DMA_ROT	WB2 Line	WB0 Block
RGB												
	Bits per component											
	A\X	R\Y	G\U	B\V	Avg per Pixel							
	Linear (Uncompressed)											
Interleaved BGR												
BGR565	0	5	6	5	16	BGR565		✓	✓	✓	✓	✓
BGR888	0	8	8	8	24	BGR888		✓	✓	✓	✓	✓
ABGR8888	8	8	8	8	32	ABGR8888		✓	✓	✓	✓	✓
BGRA8888	8	8	8	8	32	BGRA8888		✓	✓	✓	✓	✓
BGRX8888	8	8	8	8	32	BGRX8888		✓	✓	✓	✓	✓
XBGR8888	8	8	8	8	32	XBGR8888		✓	✓	✓	✓	✓
ABGR1555	1	5	5	5	16	ABGR1555		✓	✓	✓	✓	✓
BGRA5551	1	5	5	5	16	BGRA5551		✓	✓	✓	✓	✓
XBGR1555	1	5	5	5	16	XBGR1555		✓	✓	✓	✓	✓
BGRX5551	1	5	5	5	16	BGRX5551		✓	✓	✓	✓	✓
ABGR4444	4	4	4	4	16	ABGR4444		✓	✓	✓	✓	✓
BGRA4444	4	4	4	4	16	BGRA4444		✓	✓	✓	✓	✓
BGRX4444	4	4	4	4	16	BGRX4444		✓	✓	✓	✓	✓
XBGR4444	4	4	4	4	16	XBGR4444		✓	✓	✓	✓	✓
ABGR2 10 10 10	2	10	10	10	32	ABGR2 10 10 10		✓	✓	✓	✓	✓
XBGR2 10 10 10	2	10	10	10	32	XBGR2 10 10 10		✓	✓	✓	✓	✓
BGRA10 10 10 2	2	10	10	10	32	BGRA10 10 10 2		✓	✓	✓	✓	✓
BGRX10 10 10 2	2	10	10	10	32	BGRX10 10 10 2		✓	✓	✓	✓	✓

Supported Color Formats (cont.)

Format						FOURCC/ Common name		IN			Out	
								VIG	DMA	DMA_ROT	WB2 Line	WB0 Block
RGB												
	Bits per component											
	A\X	R\Y	G\U	B\V	Avg per Pixel							
	Compressed											
UBWC												
RGBX8888	8	8	8	8				✓	✓	✓	✓	✓
RGBA8888	8	8	8	8				✓	✓	✓	✓	✓
RGBA10 10 10 2	2	10	10	10				✓	✓	✓	✓	✓
RGBX 10 10 10 2	2	10	10	10				✓	✓	✓	✓	✓
RGB565	0	5	6	6				✓	✓	✓	✓	✓

Supported Color Formats (cont.)

Format						FOURCC/ Common name		IN			Out	
								VIG	DMA	DMA_ROT	WB2 Line	WB0 Block
YUV												
	Bits per component											
	A\X	R\Y	G\U	B\V	Avg per Pixel							
Linear (Uncompressed)												
YUV420												
YUV Planar	0	8	8	8	12	I420, IYUV, YU12		✓	×	✓	×	×
YVU Planar	0	8	8	8	12	YV12		✓	×	✓	×	×
YUV Semi-Planar	0	8	8	8	12	NV12		✓	×	✓	✓	✓
YVU Semi-Planar	0	8	8	8	12	NV21		✓	×	✓	✓	✓
YUV Semi-Planar 10 Bit	0	10	10	10		P010		✓	×	✓	×	✓
YUV422												
YUV Semi-Planar	0	8	8	8	16			✓	×	✓	✓	✓
YVU Semi-Planar	0	8	8	8	16			✓	×	✓	✓	✓
YUYV Interleaved	0	8	8	8	16	YUYV, YUY2		✓	×	✓	✓	×
YVYU Interleaved	0	8	8	8	16	YVYU		✓	×	✓	✓	×
VYUY Interleaved	0	8	8	8	16	VYUY		✓	×	✓	✓	×
UYVY Interleaved	0	8	8	8	16	UYVY		✓	×	✓	✓	×

Supported Color Formats (cont.)

Format						FOURCC/ Common Name		IN			Out	
								VIG	DMA	DMA_ROT	WB2 Line	WB0 Block
YUV												
	Bits Per Compoent											
	A\X	R\Y	G\U	B\V	Avg per Pixel							
	Compressed											
UBWC												
YUV420 8 Bit	0	8	8	8		UBWC_NV12		✓	×	✓	✓	✓
YUV420 10 Bit	0	10	10	10		UBWC_TP10_420		✓	×	✓	✓	✓
YUV420 Semi-Planar 10 bit	0	10	10	10		UBWC_P010		✓	×	✓	×	✓

Source Surface Processor Pipes (SSPP)

Feature	VIG	SDMA
Predecimation	1/2, 1/4, 1/8, 1/16 (Linear mode only)	No
Scaling ratio	Arbitrary 1/64 - 20x (decimation when <1/4)	No scaling
Sharpening	Yes	No
Chroma up	Yes, any chroma sites	No
Color space conversion (CSC)	Yes	No
Flip	Vertical and horizontal	Vertical and horizontal
Picture adjustment (hue, saturation, contrast, and intensity)	Smooth curve soft clip	No
Memory color (sky, foliage, and skin tone)	Yes	No

Layer Mixer, Background Color, Dim Layer

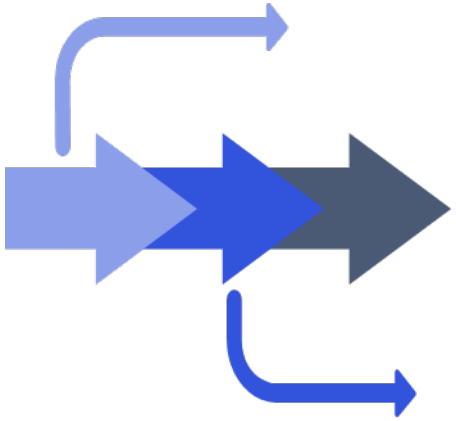
Features	Adreno DPU775 support
Number of layer mixers	4
Maximum number of surfaces blended	10
Total number of pipes for blending	10; 2 × 2 VIG, 3 × 2 DMA (SDMA 2.0 on VIG and SDMA)
Alpha blending	Constant alpha, per-pixel alpha, premultiplied alpha, modulation alpha, and reverse alpha for all
Alpha blending for Background (BG) color	Yes
BG color generation	Yes (no data fetch for BG color)
Arbitrary blending order	Yes
Blending in linear space	No
Dim layer	Supports dim layer without using Adreno GPU or Adreno DPU source pipes
Numbers of hardware cursors	Removed dedicated hardware cursor pipes, uses SDMA pipes, added more layers in layer mixer, and removed restriction in SDMA pipes

Destination Surface Processor Pipes (DSPP)

Feature	Adreno DPU775 support
Assertive display	Yes (new version V4)
Content adaptive backlight control (CABL)	Yes
Panel color correction (PCC)	3 × 11 polynomial
Gamut mapping	3D LUT
Gamma correction	Yes
Picture adjustment (hue, saturation, contrast, and intensity)	Smooth curve soft clip
Dither	Yes
Memory color (sky, foliage, skin tone)	Yes
6-color zone adjustment	Yes

3D Mux, Rotator, and Writeback

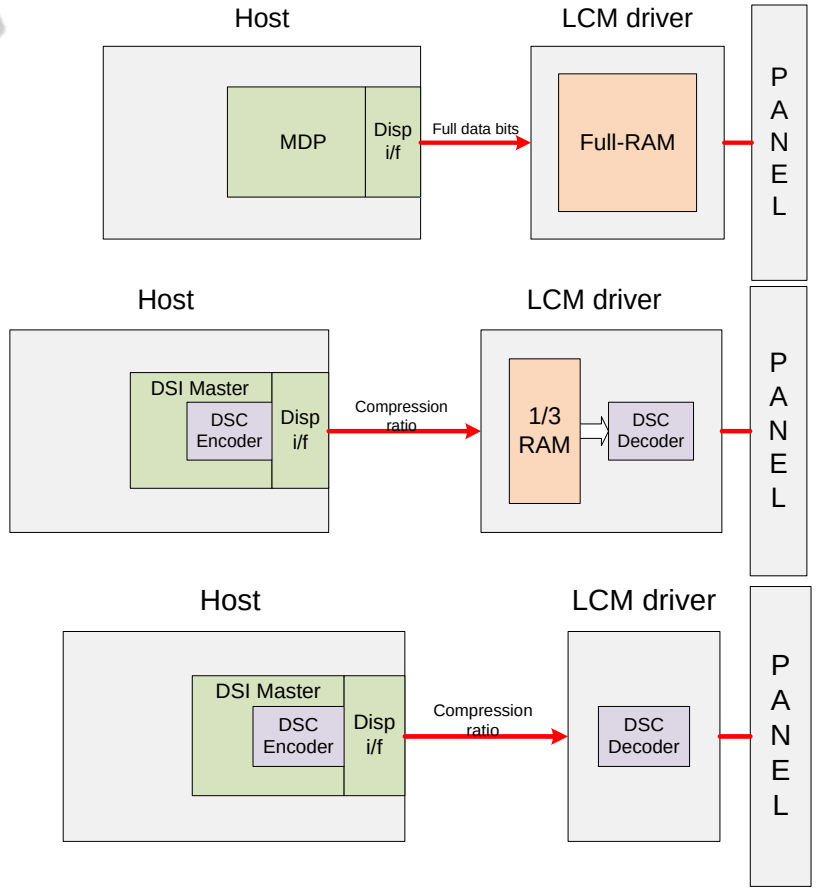
Feature	Adreno DPU775 support
Rotation modes	90º, 180º, 270º
Rotator downscalar	1/2 ~ 1/64 (power of 2) and 1/1.5
Inline rotation	Power optimized inline rotation for single surface
Offline rotation	Two steps offline rotation for more than one surface
3D mux format support	Pixel interleaving, line interleaving, frame packing, side-by-side and top-and-bottom support
Number of writeback paths	1
Writeback performance	1080 × 1920 at 30 Hz



Interface Features

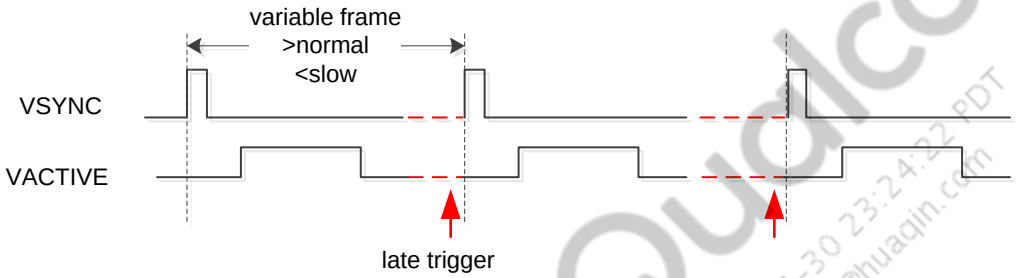
Display Stream Compression (DSC)

- Reduces frame buffer memory size
- Supports VESA DSC 1.1 (3:1 compression ratio)
- Reduces bandwidth and reduces number of lane requirements for display interface and drives higher resolution displays
  - With compression, requires single port 4-lane DSI for resolutions greater than 2560 × 1600
  - Without compression, requires 2-port 8-lane DSI for resolution greater than 2560 × 1600
- Reduces power consumption due to link bandwidth savings
- Alleviates EMI issues
  - Without VESA DSC compression
    - Full link rate
    - Full RAM size
  - Command mode application
    - DSC encoder at host
    - DSC decoder at LCM driver with 1/3 embedded RAM
    - Required DSI link bandwidth reduced by 1/3
    - Compression is applied only on video data payload in DCS commands
    - Memory, bandwidth, and power savings
  - Video mode application
    - DSC encoder at host
    - DSC decoder at LCM driver
    - 1/3 DSI link speed or DSI link at full speed with link in Low-power mode for long time
    - Bandwidth and power savings

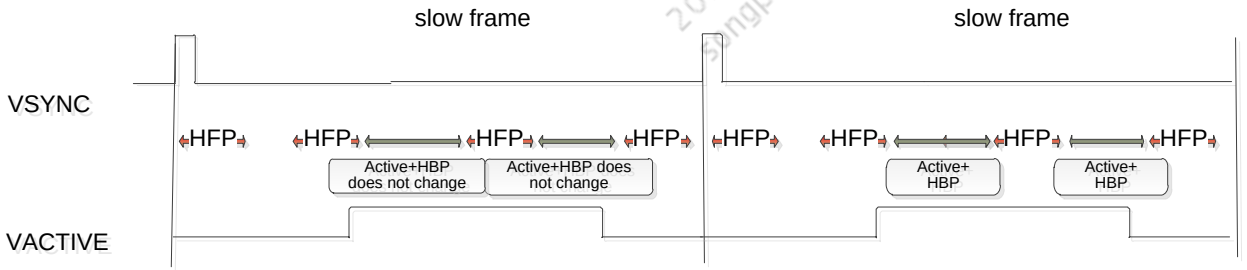


Variable Refresh

- Changes the Video mode operation refresh rate on the fly with variable refresh – change video blanking

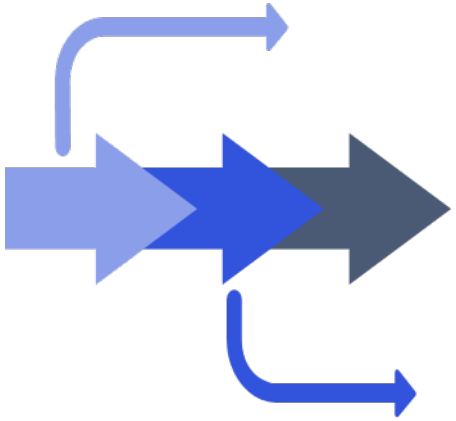


Vertical blanking method



Horizontal blanking method

HFP – Horizontal front porch
HBP – Horizontal back porch



Pixel Processing and Postprocessing

Image and Video Processing

Scaling and sharpening

	VIG pipe	DMA pipe
Scaling ratio	1/64 - 20x (decimation for <1/4)	N/A
Upscaling filter	Yes	N/A
Downscaling filter	Yes	N/A
Sharpening	Yes	N/A
Chroma up	Yes	N/A
Format support	All formats (YUV and RGB)	N/A

QSEED2

4:1 Upscale (Zoomed in)

QSEED3

4:1 Upscale (Zoomed in)

Qualcomm® TruPalette™ Display Feature – Picture Adjustment

Memory color and six color zones

- User-definable memory color zones (sky, foliage, and skin) can be adjusted independently from other regions.
- Additional six color zones can be adjusted independently.

Original

Adjusted

TruPalette Picture Adjustment (Hue, Saturation, Intensity, and Contrast)

- Hue

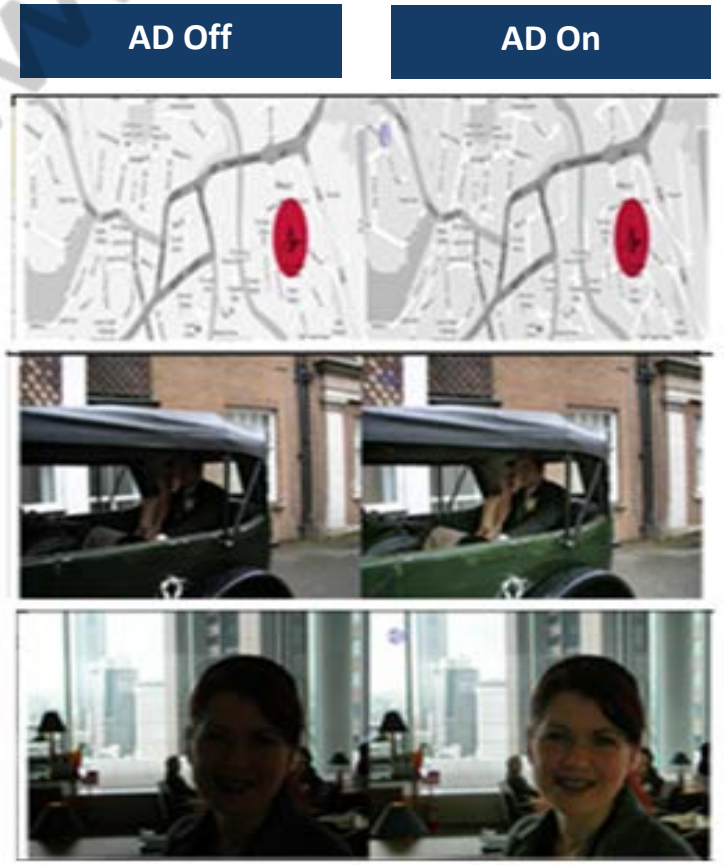
- Saturation

- Brightness

Qualcomm® Low-Power Picture Enhancement – Postprocessing Algorithms

Assertive displays

- Sunlight visibility improvement
- Improved contrast for multimedia content at the same power (backlight) level
- New version to improve tone mapping



Qualcomm Low-Power Picture Enhancement – Postprocessing Algorithms

FOSS

- Achieves an optimal visual experience of the displayed image based on human visual system (HVS) metrics without increase in brightness
- Power saving depends on panel characteristics, display content, and tunable FOSS parameters

Panel power with bright content without FOSS: 222.42 mA

Panel power with bright content with FOSS: 197 mA

Note: These measurements are based on SDM660 device.

Qualcomm Low-Power Picture Enhancement – Postprocessing Algorithms

Global CABL

Feature	Adreno DPU775
Histogram collection	Hardware
LUT	Hardware
Pipeline location	After blending and HSIC adjustment
Core algorithm	Software

Original image

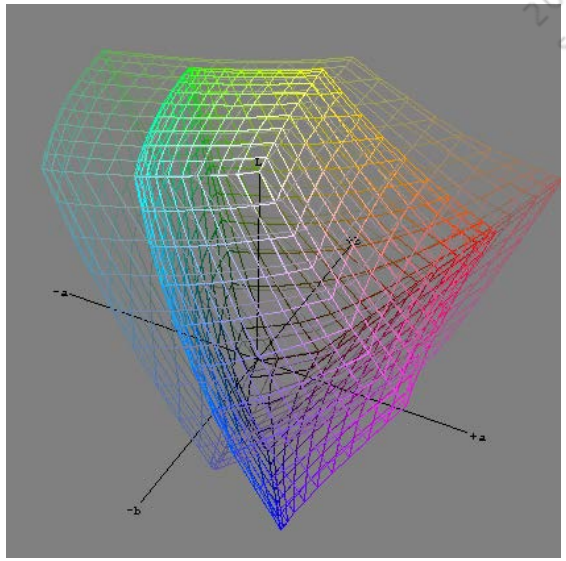
Original image with CABL active

- Reduces LCD backlight power while retaining visual quality
  - No impact to visual quality due to panel characteristic change with backlight variation
- Better visual quality with the separated LUT for gamma correction and ABL
- Less temporal latency
  - Double buffer for histogram collection

Panel Calibration and Correction

	Objective	Correction scope	Block
Gamma correction	To correct tone response resolution of RGB channels to achieve: ▪ Appropriate display tone/gamma response ▪ Solid gray-tracking performance	Full range of grays	3-channel 1D LUT
Color correction	To achieve accurate color rendering on displays and compensate for: ▪ Optical color crosstalk ▪ Electrical color crosstalk ▪ Color shift due to backlight modulation ▪ Color gamut mismatch	Full color gamut	▪ To reduce significant color crosstalk by using 3 × 11 polynomial ▪ Gamut expansion by using 3D LUT

Gamut mapping



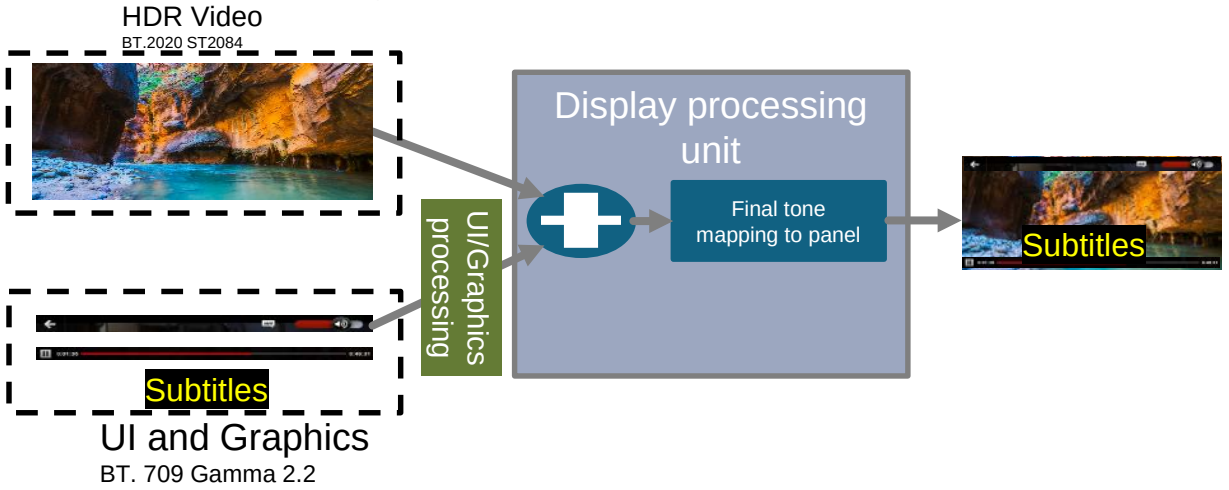
Color crosstalk

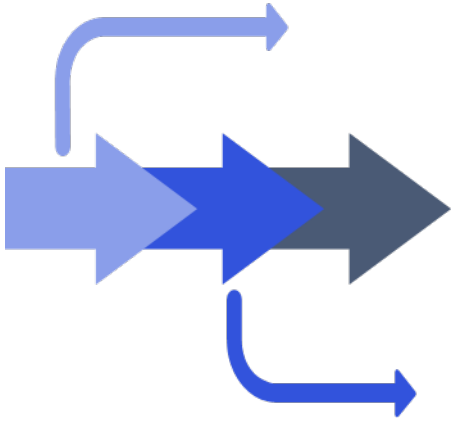
HDR10 Playback Solution for SDM710

- HDR vs. SDR
  - Standard dynamic range (SDR)
    - Studios expect consumers to view content on SDR displays
    - Original source content is mapped to BT.709 color gamut with 100 nits luminance range
  - High dynamic range (HDR)
    - Studios are now grading content to be viewed on new HDR displays available to consumers
    - Original source content is mapped to BT.2020 color gamut with up to 10,000 nits luminance range
  - Low-power solution that leverages Adreno DPU hardware
  - Standardized solution, external component is not required

SDR

HDR





Feature Deltas

Performance

	MSM8976	SDM660	SDM670	SDM710
Panel resolution	1600 × 2560 at 60 fps	1600 × 2560 at 60 fps	1080 × 1920 (10-bit)/ 1080 × 2160 30bpp at 60 fps	1600 × 2560 (10-bit)/ 1440 × 2880 30bpp at 60 fps
Number of displays	2	2	2	2
Maximum concurrency	1600 × 2560 at 60 primary + 1080 × 1920 at 30 WFD	2560 × 1600 at 60 Hz primary + 4096 × 2160 at 30 fps over DP or 1080p at 30 fps for WFD	1920 × 1080 at 60 Hz primary + 4096 × 2160 at 30 fps over DP or 1080 × 1920 at 30 fps for WFD Or 2160 × 1080 at 60 Hz primary + 4096 × 2160 at 30 fps over DP or 1080 × 1920 at 30 fps for WFD	2560 × 1600 at 60 Hz primary + 4096 × 2160 at 30 fps over DP or 1080 × 1920 at 30 fps for WFD Or 2880 × 1440 at 60 Hz primary + 4096 × 2160 at 30 fps over DP or 1080 × 1920 at 30 fps for WFD

Architecture

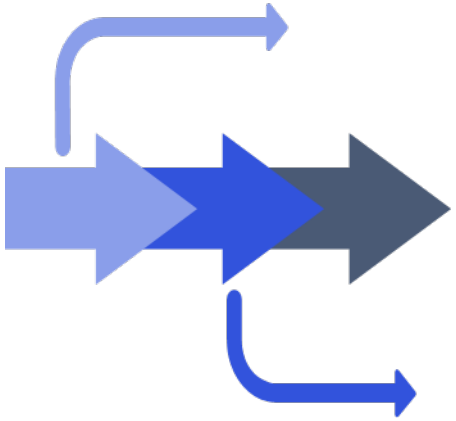
	MSM8976	SDM660	SDM670	SDM710
MDP/SDE/DPU	SDE590	SDE660	Adreno DPU775	Adreno DPU775
RGB pipes	2	0	0	0
VIG pipes	2	2	2 (SDMA 2.0; 1x YUV or 2x ARGB layers)	2 (SDMA 2.0; 1x YUV or 2x ARGB layers)
DMA pipes	1	3 (SDMA 1.0; 2x ARGB layers)	3 (SDMA 2.0; 2x ARGB layers)	3 (SDMA 2.0; 2x ARGB layers)
Writeback/rotator	2	1	1	1
Rotator downscalar	No	Yes	Yes	Yes
Inline rotation	No	Yes	Yes	Yes
Layer mixers	2	4	4	4
Maximum number of surfaces blended	5	8	10	10
DSPP	1	2	2	2
Hardware cursors	1	1	0	0
MDP clock	360 MHz	412 MHz	430 MHz	430 MHz
Support for UBWC	Yes (UBWC 1.0)	Yes (UBWC 1.0)	Yes (UBWC 2.0 + UBWC_P010)	Yes (UBWC 2.0 + UBWC_P010)
Dim layer in layer mixer	No	No	Yes	Yes

Image Processing

Feature	MSM8976	SDM660	SDM670	SDM710
Color management	Yes	Yes	Yes	Yes
CABL	Yes	Yes	Yes	Yes
Frame buffer compression (FBC)	VESA DSC 1.1	VESA DSC 1.1	VESA DSC 1.1	VESA DSC 1.1
Compression ratio	2:1 and 3:1	2:1 and 3:1	2:1 and 3:1	2:1 and 3:1
Memory color (sky, foliage, and skin tone)	Yes	Yes	Yes	Yes
Six color zone adjustment	Yes	Yes	Yes	Yes
Assertive display for split pipe	Yes (V3)	Yes (V3)	Yes (V4)	Yes (V4)

Display Interface

	MSM8976	SDM660	SDM670	SDM710
DSI 0	4 lanes 6 Gbps	4 lanes 8.4 Gbps (D-PHY)	▪ 4 lanes 10 Gbps (D-PHY)/ 3 lanes 17.14 Gbps (C-PHY, No software support) ▪ 10-bit DSI uncompressed or compressed	▪ 4 lanes 10 Gbps (D-PHY)/ 3 lanes 17.14 Gbps (C-PHY, No software support) ▪ 10-bit DSI uncompressed or compressed
DSI 1	4 lanes 6 Gbps	4 lanes 8.4 Gbps (D-PHY)	▪ 4 lanes 10 Gbps (D-PHY)/ 3 lanes 17.14 Gbps (C-PHY, No software support) ▪ 10-bit DSI uncompressed or compressed	▪ 4 lanes 10 Gbps (D-PHY)/ 3 lanes 17.14 Gbps (C-PHY, No software support) ▪ 10-bit DSI uncompressed or compressed
eDP	NA	NA	▪ NA	▪ NA
LVDS	NA	NA	▪ NA	▪ NA
DP (USB Type-C)	NA	4096 × 2160 at 30 Hz	▪ 3840 × 2160 at 30 fps, 24 bpp 2 data lanes with USB 3.0 ▪ 4096 × 2160 at 30 fps, 30 bpp 4 data lanes without USB 3.0	▪ 3840 × 2160 at 30 fps, 24 bpp 2 data lanes with USB 3.0 ▪ 4096 × 2160 at 30 fps, 30 bpp 4 data lanes without USB 3.0
WFD	1080p at 30 Hz	1080p at 30 Hz	1080 × 1920 at 30 Hz	1080 × 1920 at 30 Hz



Linux Android Software Architecture

Android Display Software Subsystem

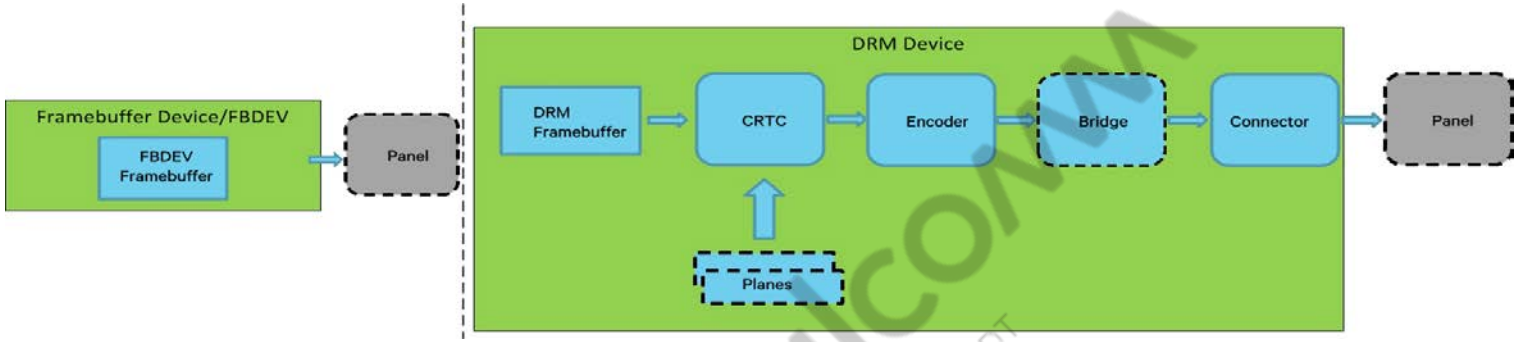
- Android framework components – SurfaceTexture, SurfaceFlinger
- QTI HALs – Graphics allocation, HWC, Snapdragon DM
- Primary panel interfaces – MIPI DSI/DP
- External panel interfaces – DP/HDCP/WFD
- Snapdragon DM core – Adreno DPU drivers, pipe configuration, clocks/power/performance
- Destination postprocessing service (DPPS) – CABL, Assertive display, FOSS, and so on

DRM/KMS Overview

- Direct rendering manager (DRM) is introduced to deal with graphic cards embedding GPUs
- Kernel mode setting (KMS) is a sub part of the DRM API, sets mode on the given display
- Rendering and mode setting are split into two different APIs and are accessible through */dev/dri/renderX* and */dev/dri/controlDX*
- KMS provides a way to configure the display pipeline of a graphic card (or an embedded system)
- KMS is an alternative to frame buffer dev (FBDEV)

Feature	FB Dev	DRM/KMS
Upstream	▪ Less actively maintained ▪ Does not provide all the features like overlays, cursors ▪ Developers are now encouraged to move to DRM/KMS	▪ Actively maintained by open source ▪ Better control on display pipeline ▪ Widely used standardized architecture for Graphics – Display protocol ▪ Full set of advanced features
User/Kernel APIs	▪ Custom overlay/atomic commit APIs	▪ Standard (kernel upstream) APIs
Source pipes management	▪ Managed through enum index and atomic commit IOCTL ▪ Features exposed through DPU driver capabilities	▪ Plane objects managed through properties and atomic mode set commit ▪ Features exposed through plane properties
Layer mixer management	Handled within driver, difficult for user mode to know what is going on	Default allocation in driver. User mode can query and override, virtualization is taken care in CRTC
Panel management	Managed through several sysfs nodes	Managed as connector object with properties

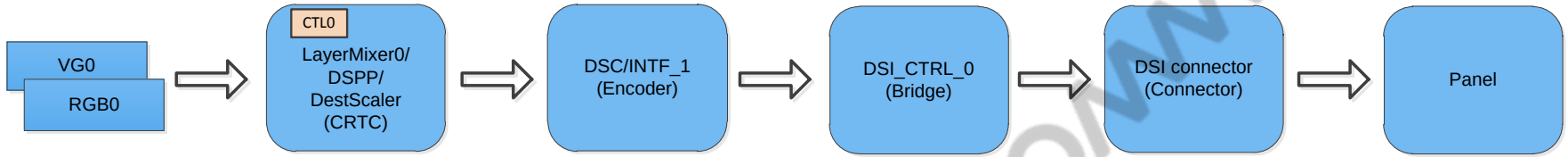
DRM/KMS Overview (cont.)



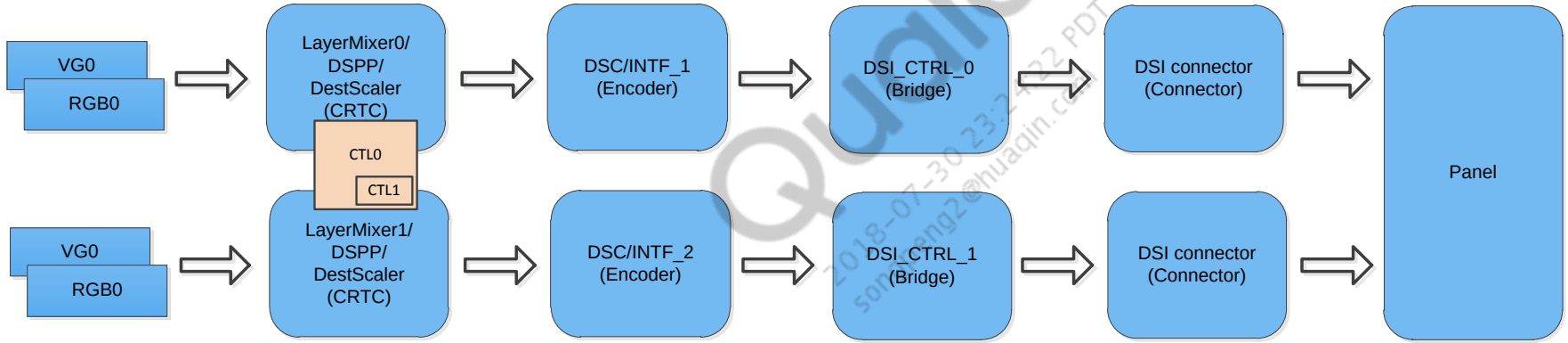
- Frame buffers (struct drm_framebuffer)
  - Frame buffers are abstract memory objects that provide a source of pixels to scan out to a CRTC. Implementation depends on the memory manager used and the IOMMU capabilities
- Planes (struct drm_pane)
  - A plane represents an image source that can be blended with or overlaid on top of a CRTC during the scan out process.
  - Planes are associated with a frame buffer to crop a portion of the image memory (source) and optionally scale it to a destination size. The result is then blended with or overlaid on top of a CRTC.
- CRTC (struct drm_crtc)
  - CRT controller (CRTC) is not related only to CRT displays. It configures the appropriate display settings: Display timings/resolution, scans out frame buffer content to one or more displays, and so on.
- Encoder (struct drm_encoder)
  - Takes pixels data from CRTC and converts it to the format suitable for any attached connectors.
- Connectors (struct drm_connector)
  - Represents display interface (HDMI, DP, DSI, VGA), transmits signal to display, detects display, exposes mode, and so on.
- Bridge
  - Associated with an encoder, participates in mode set, device power management, connection detection, and so on.

DRM/KMS Components/Hardware mapping

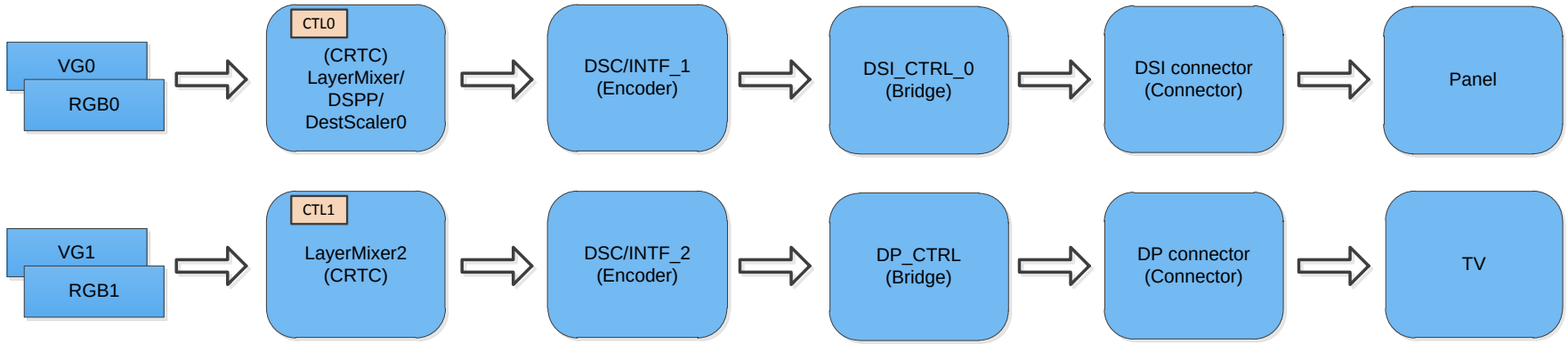
Single DSI single layer mixer single display



Split DSI dual layer mixer single display



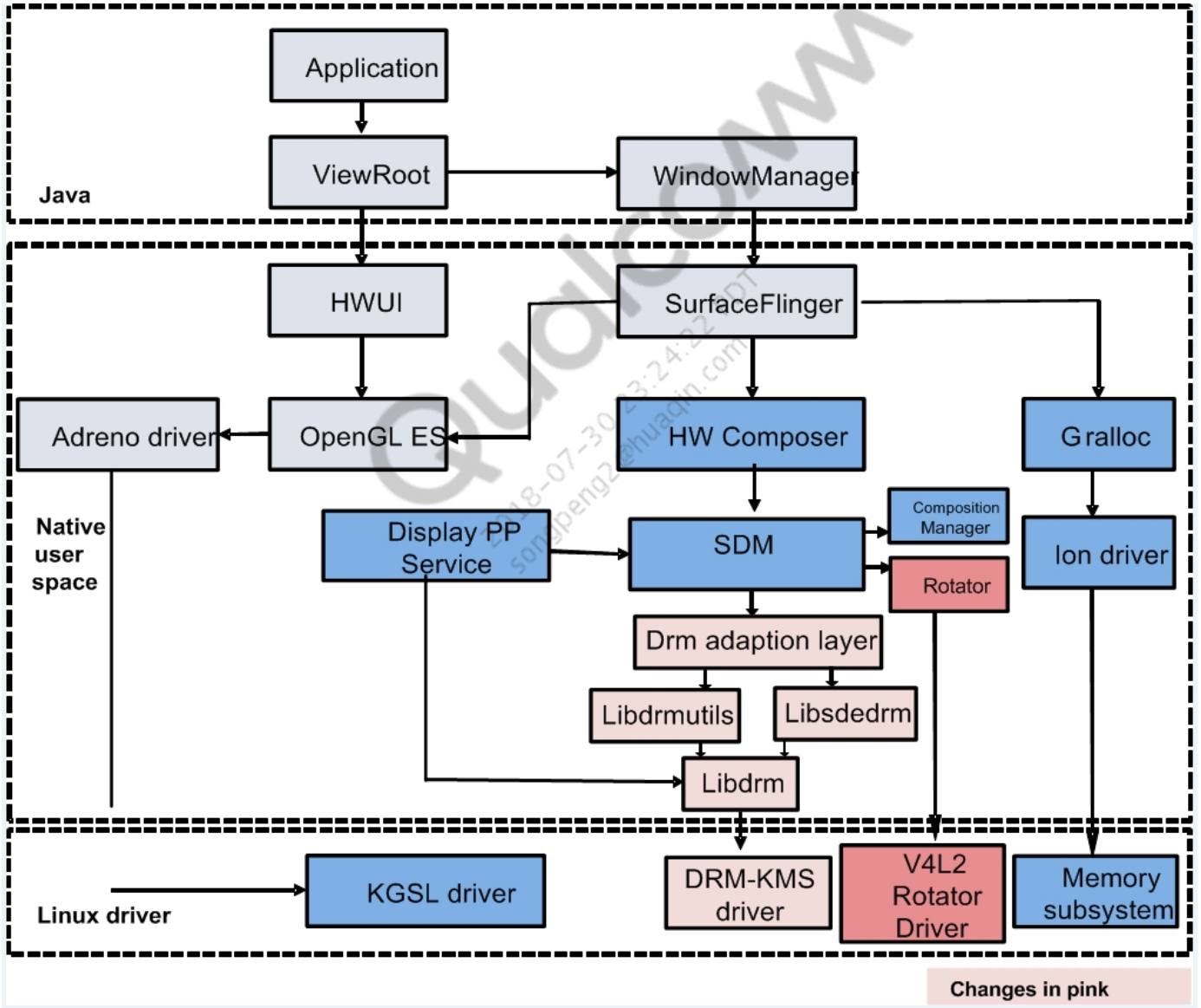
Dual display primary + external



Software Directory Structure

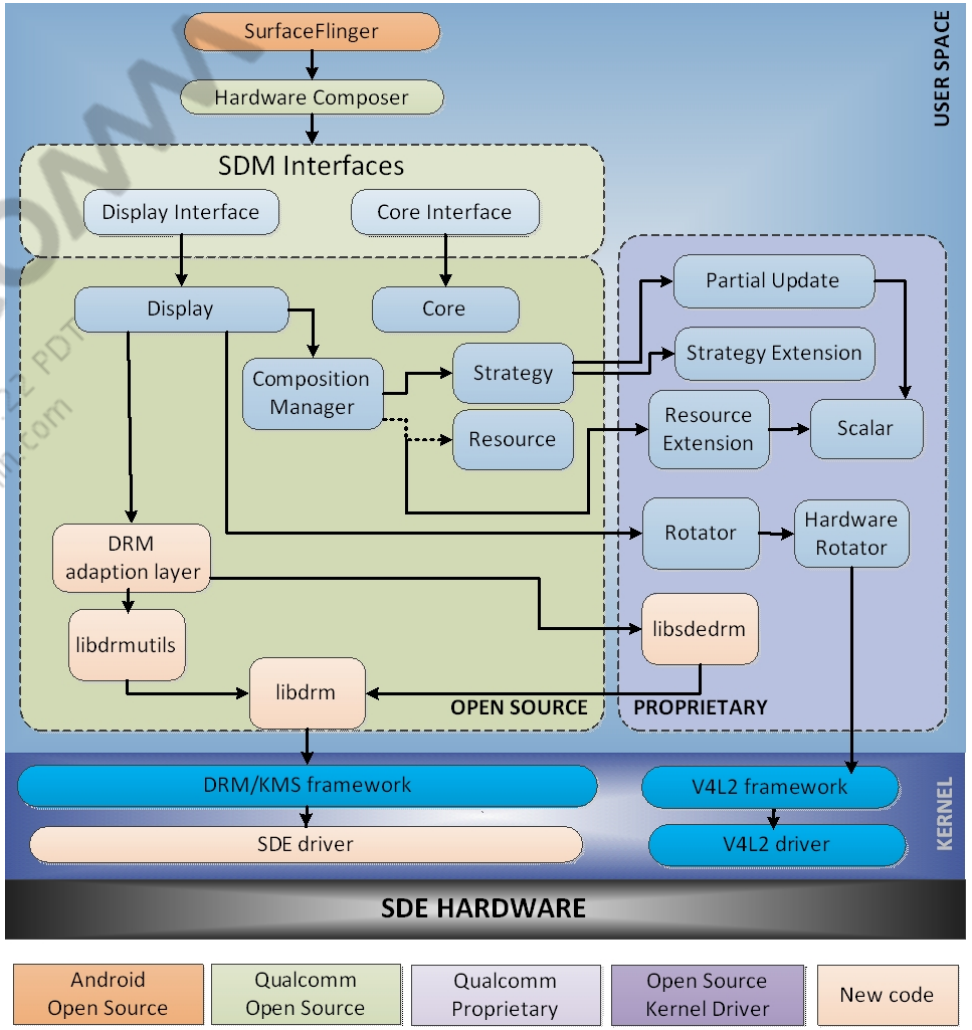
- User space
  - SurfaceTexture – *<build>\frameworks\native\libs\gui*
  - SurfaceFlinger – *<build>\frameworks\native\services\surfaceflinger*
  - Graphics alloc – *<build>\hardware\qcom\display\libgralloc1*
  - HWC – *<build>\hardware\qcom\display\sdm\libs\hwc2*
  - Snapdragon DM – *<build>\hardware\qcom\display\sdm\libs\core*
  - DPPS (postprocessing) – *<build>\vendor\qcom\proprietary\display*
- Driver
  - DRM DPU driver – *<build>\kernel\msm-4.9\drivers\gpu\drm\msm*
  - V4L2 rotator – *<build>\kernel\msm-4.9\drivers\media\platform\msm\sde\rotator*

Display Architecture



SDM DRM Architecture

- **Core** – Manages lifecycle of Snapdragon DM and provides interfaces to create and destroy displays.
- **Display interface** – Manages display lifecycle and interacts with driver for composition operations.
- **Composition manager** – Interacts with strategy and resource modules to determine composition strategy.
- **Strategy** – Analyzes layer stack and selects composition strategy.
- **Partial update** – Identifies updating region and aligns it to hardware bounds.
- **Resource** – Manages pipes, bandwidth, and writes back blocks.
- **Rotator** – Interacts with V4L2 driver for rotation operations.
- **HWC wrapper** – Translates SurfaceFlinger calls to Snapdragon DM.
- **Libdrm** – Upstream standard library as a wrapper over DRM framework provides APIs for accessing DRM IOCTL.

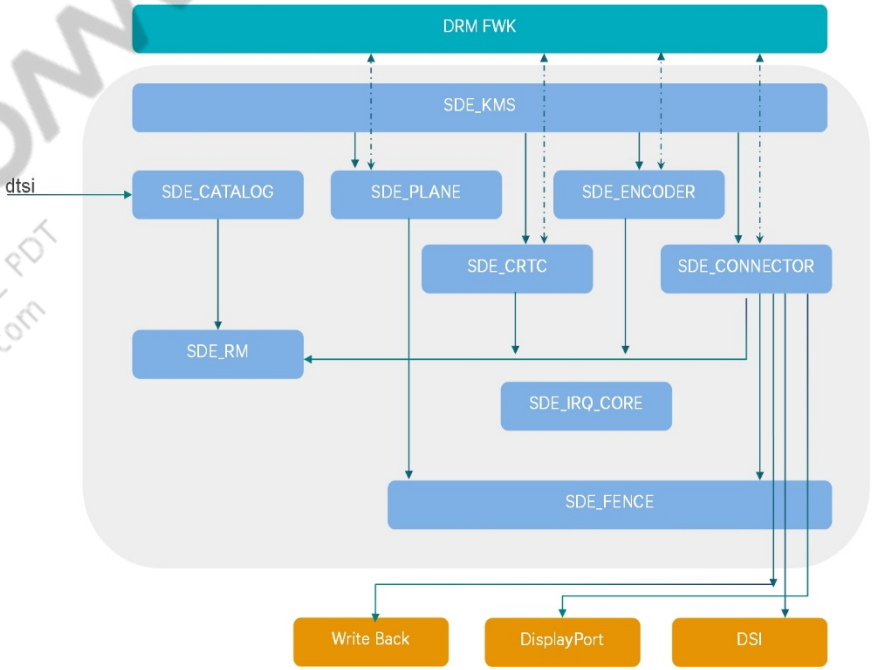


SDM DRM Architecture (cont.)

- **Libdrmutils** – Android and Snapdragon DM independent QTI library provides common master fd for libdrm calls, APIs to convert ION fd to DRM fb_id and logging, and so on.
- **Libsdedrm** – Manages pool of CRTC, connectors, and planes, parses properties, implements DRM manager interface and DRM atomic request interface, such as set plane/crtc/connector properties, validate, and commit.
- **DRM adaption layer** – Translates Snapdragon DM-related parameters to DRM properties, implements hardware APIs for Snapdragon DM to provide DRM definition in parallel to FB HAL. Uses drm_vblank to replace existing Vsync to drive frame updates.
- **DPU driver** – Implements DRM/KMS driver.

DRM/KMS Adreno DPU Driver Architecture

- Adreno DPU driver implements the DRM/KMS kernel mode driver
  - Contains all the KMS components and performs the DRM framework initialization, registration, probe, removes functions and implements the IOCTL interface.
  - Identifies the Adreno DPU hardware version, loads the hardware catalog during initialization. It interacts with the underlying hardware driver to perform all the dependent functionality.
- DRM components implementation
  - Except for DRM planes all the DRM components are virtualized, each DRM component has the SDE_* implementation, which allocates, maintains, and programs the set of hardware blocks it is composed of.
- SDE_CATALOG – Defines the capabilities and I/O region for Adreno DPU hardware, parses the dtsi and maintains common structure accessible by the components.
- SDE_PLANE – Implements the abstraction and hardware configuration for SSPP, plane management is left with user space for Snapdragon DM backward compatibility. Release fence is passed by the user space through a property.



DRM/KMS Adreno DPU Driver Architecture (cont.)

- SDE_CRTC – Manages two atomic commits – TEST_ONLY(validate) and ATOMIC_COMMIT(kickoff), configures blend stages, stream pixels to one or more encoders.
- SDE_ENCODER – Enumerated one per display. Enabled only for active displays, Encoder – Connector one-to-one mapping, used as the primary identifier for display, allocated resources for the display as per the topology through resource manager.
- SDE_CONNECTOR – Represents panel for the DRM, retire fence create/signal.
- SDE_RM – Resource manager for all the hardware blocks except SSPP, reserves the hardware for the display as per the requested topology during TEST (or COMMIT).
- SDE_IRQ_CORE – Interrupt handling
- SDE_FENCE – Android sync fence and timeline are replaced with a new mechanism.

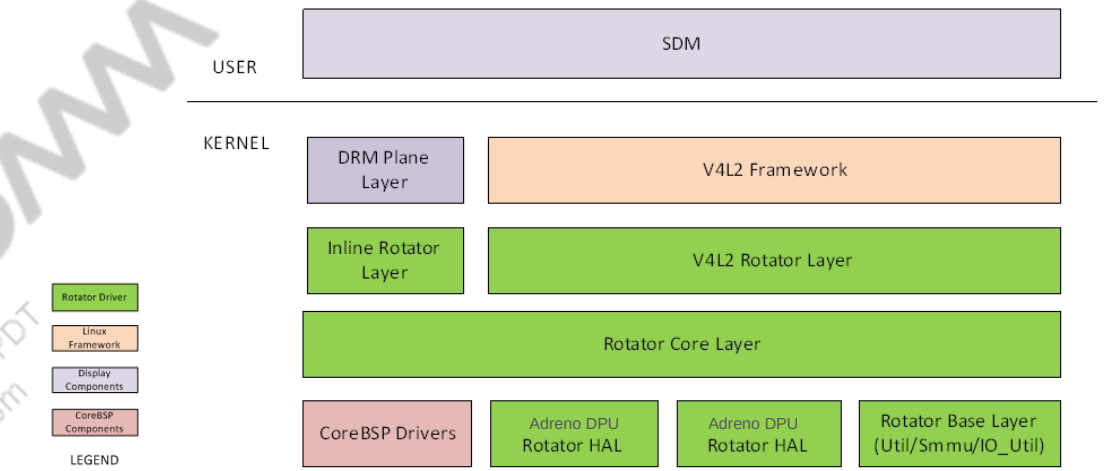
DRM/KMS Adreno DPU Driver Architecture (cont.)

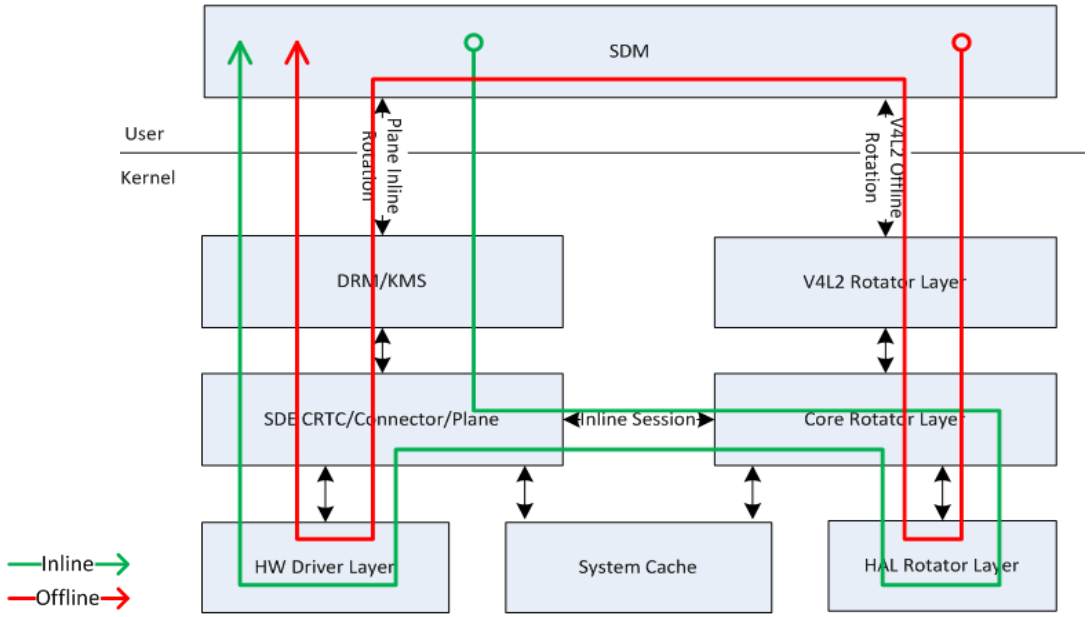
DisplayPort DRM driver

- **DP DRM** – Initializes DP bridge and connector, enumerates DP display and connects it with the DRM framework, defines, and handles the properties and ioctls, called by SDE driver.
- **DP display** – The primary engine that defines the state machine, enumerates all the modules, and connects them.
- **Other modules** – All the modules are independent of each other and perform a dedicated task. Modules do not interact with each other directly. All modules have get/set functions that are called by DP display and provides their functionalities to DP display and other modules to use. All modules have debug implementations, which can be dynamically replaced with actual implementation for debugging purposes.

V4L2 Rotator

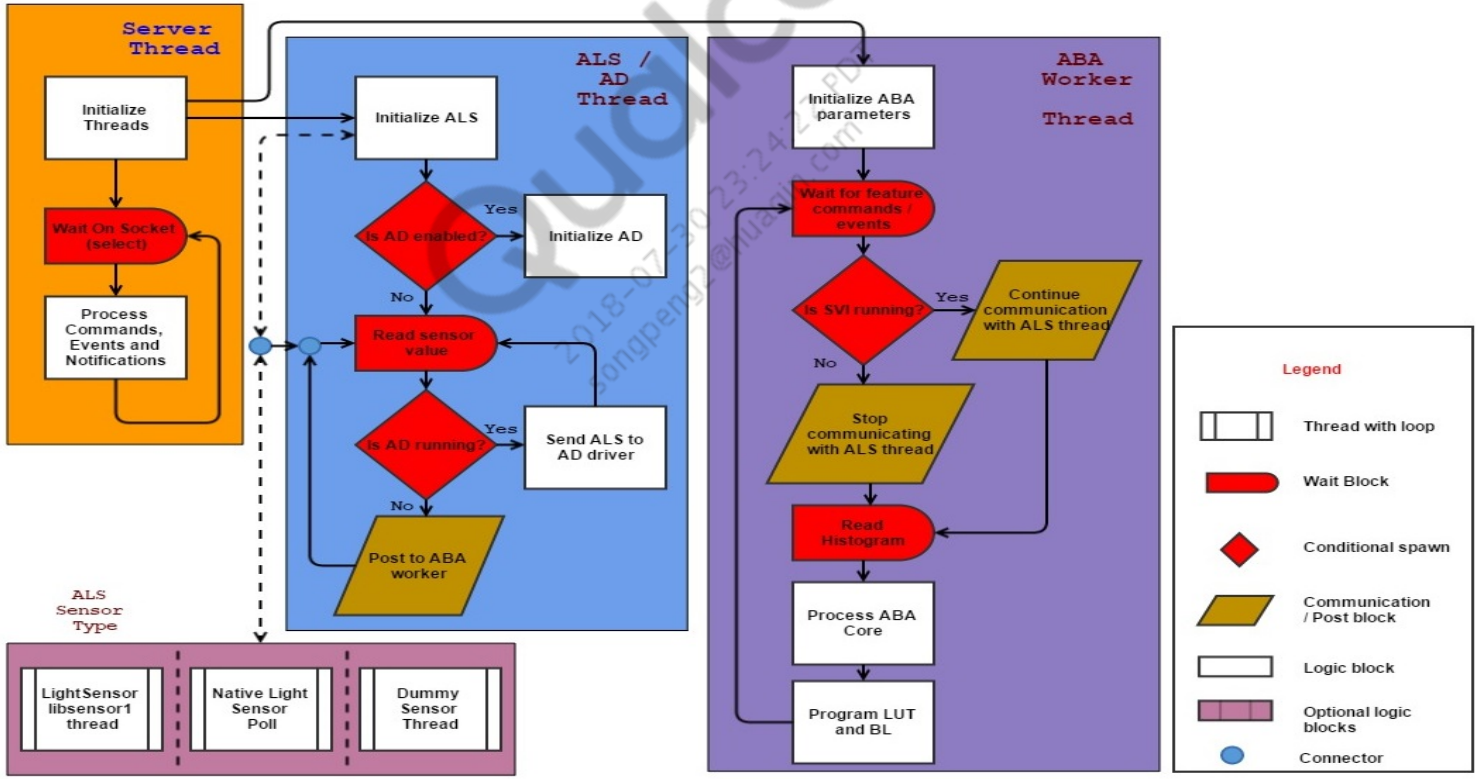
- **Architecture**
  - V4L2 framework – Linux framework for controlling video-related devices
  - V4L2 rotator layer – Adaptation layer between V4L2 and the Adreno DPU rotator driver
  - Adreno DPU rotator core layer – Implements core logic and does I/O operations
  - Adreno DPU – Hardware abstraction layer controlling rotator functionality specific to the Adreno DPU
  - Rotator base layer – Interacts with Adreno DPU, SMMU modules for buffer handling
  - CoreBSP drivers – Configure rotator clock, memory bus, and footswitch configurations
  - DRM plane layer – Adaptation layer between DRM and inline rotator driver
- **Call flow**
  - Offline rotation stays with existing V4L2 call path
  - Inline rotation is invoked via DRM plane call path
  - Both offline and inline rotation share core rotator driver as in existing V4L2 path





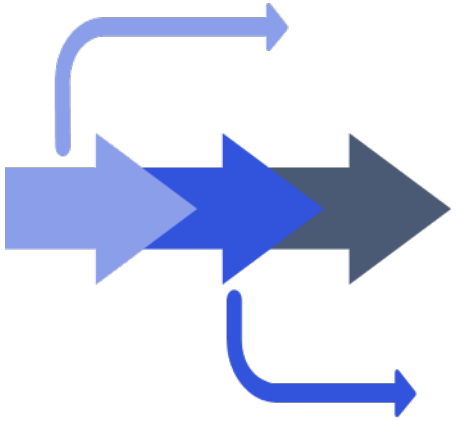
Modules in Display Postprocessing Service

- Clients send commands to display postprocessing service via server thread
- ALS/AD thread implements ambient light sensor and assertive display functionality
- ABA worker thread implements QTI algorithms such as CABL and SVI



Software Feature Comparison

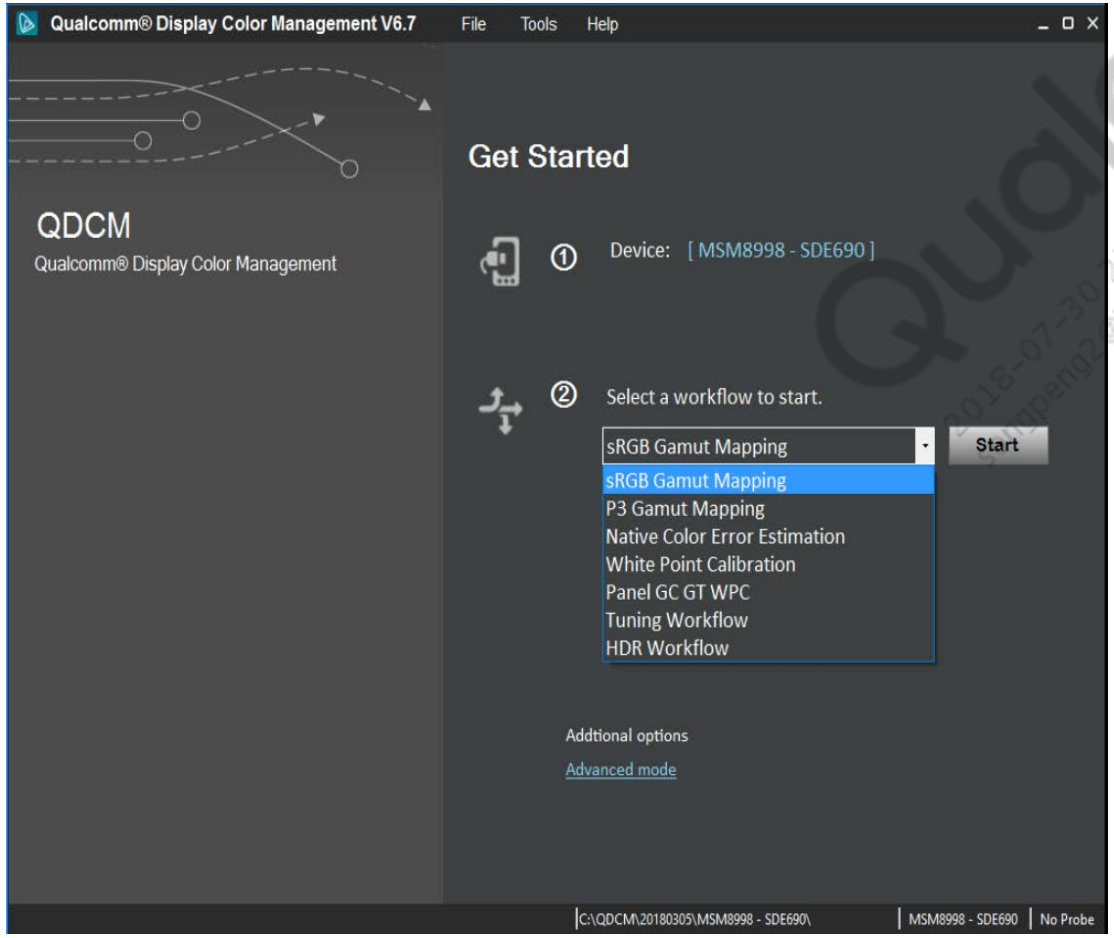
Feature	SDM660	SDM670	SDM710
Partial update (Command mode panel)	Yes	Yes	Yes
ESD	Yes	Yes	Yes
Variable FPS porch method (video mode panel)	Yes	Yes	Yes
Hardware cursor	Yes	Yes	Yes
Command mode/video mode panel switch	Yes	No	No
Dynamic resolution switch	Yes	Yes	Yes
Dynamic clock gating static screen (command mode panel)	Yes	Yes	Yes
DPU DCVS (bus and clock)	Yes	Yes	Yes
DisplayPort	Yes	Yes	Yes
Destination scalar	Yes	Yes	Yes
10-bit, end-to-end support in all pipelines	Yes	Yes	Yes
Inline rotation	No	Yes	Yes
SDMA	1.0	2.0	2.0
Dim layer	Yes (with DPU pipe)	Yes (does not use DPU pipe)	Yes (does not use DPU pipe)
LUT DMA	No	Yes	Yes
UBWC_P010	No	Yes	Yes
HDMI	No	No	No

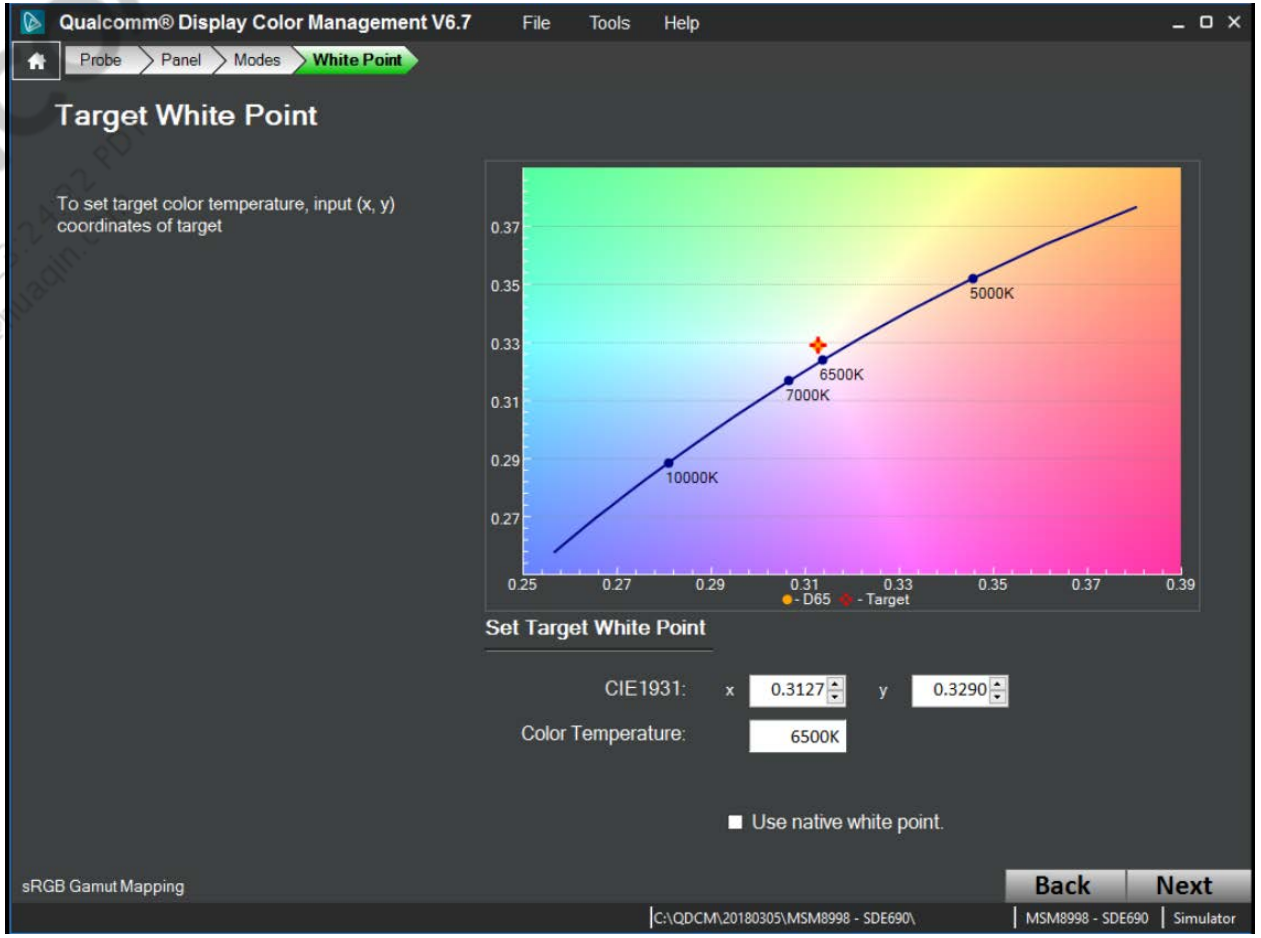


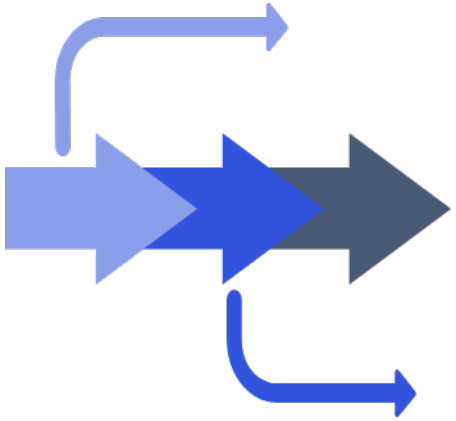
Tools

Qualcomm Display Color Management (QDCM) PC Tool

Use the QDCM PC tool to perform panel calibration and picture adjustment (PA), including HSIC.







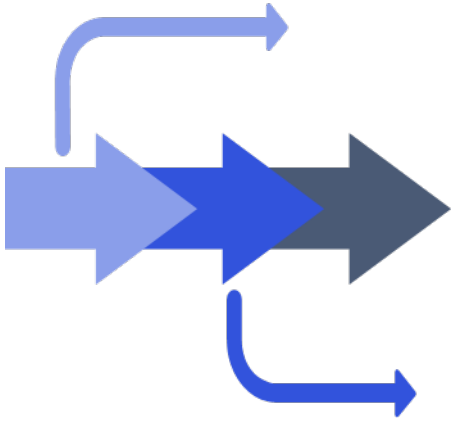
Support

Debugging

- Use Snapdragon Display Triage Tool (SDTT) for debugging display issues, see *Snapdragon Display Triage Tool User Guide* (80-P9417-1)
- For detailed steps to debug display issues, see *Linux Android Display Debug Guide for DRM/KMS* (80-P9301-83)

Design Review and Feature Request Submission

- To raise a new design review or new feature request, refer to *Display Design Review and Feature Request Customer Product Information Form* (80-P4578-1).
- Customer Engineering (CE) support is provided through QTI's Salesforce portal at https://createpoint.qti.qualcomm.com.
- For design review cases, select the following problem areas to direct the case to the display CE team:
  - Problem area 1 – Multimedia
  - Problem area 2 – Display
  - Problem area 3 – Design review



References

References

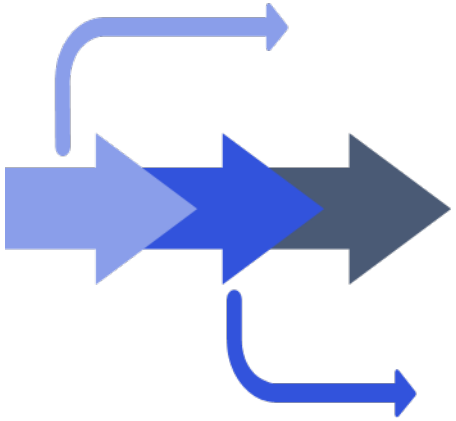
Title	Number
Qualcomm Technologies, Inc.	
Linux Android Display Debug Guide for DRM/KMS	80-P9301-83
SDM670/SDM710 Display Bringup Guide	80-PD126-47
Snapdragon Display Triage Tool User Guide	80-P9417-1
Display Design Review and Feature Request Customer Product Information Form	80-P4578-1
Content Adaptive Backlight Design Guide	80-NP952-1
Qualcomm Display Color Management (QDCM) Tuning Tool	80-NJ550-1
High Dynamic Range (HDR) Feature	80-PA058-1
Open source	
DRM internals	https://01.org/linuxgraphics/gfx-docs/drm/drmInternals.html
Kernel mode setting (KMS)	https://01.org/linuxgraphics/gfx-docs/drm/gpu/drm-kms.html
Standards	
HDMI Specification	www.hdmi.org/
MIPI Alliance Specification for D-PHY	mipi.org
MIPI Alliance Specification for DSI	mipi.org
MIPI Alliance Specification for DCS	mipi.org
VESA Display Stream Compression	www.vesa.org
VESA DisplayPort	www.vesa.org

References (cont.)

Acronym or Term	Definition
ABA	Adaptive backlight algorithm
AD	Assertive display
ALS	Ambient light sensor
ARGB	Alpha Red Green Blue
AHB	Advanced high-performance bus
AXI	Advanced eXtensible Interface
CABL	Content adaptive backlight control
CAF	Content adaptive filter
CEC	Consumer electronic control
DMA	Direct memory access
DM	Display manager
DP	DisplayPort
DPU	Display processing unit
DPPS	Destination postprocessing service
DSC	Display stream compression
DSI	Display serial interface
DSPP	Destination surface processor
DRM	Direct rendering manager
EDID	Extended display identification data
FB	Frame buffer
FBC	Frame buffer compression

References (cont.)

Acronym or Term	Definition
FOSS	Fidelity optimized signal scaling
HDCP	High-bandwidth digital content protection
HSIC	Hue, saturation, intensity, and contrast
HWC	Hardware composer
KMS	Kernel mode setting
LM	Layer mixer
LPCM	Linear pulse-code modulation
LVDS	Low voltage differential signaling
MDP	Mobile display processing
MST	Multiple-stream transport
PCMN	Phase control M/N
PA	Picture adjustment
PP	Postprocessing
QDCM	Qualcomm display color management
SDE	Snapdragon display engine
SDMA	Smart direct memory access
SSPP	Source surface processor pipes
SST	Single stream transport
SVI	Sunlight visibility improvement
UBWC	Universal bandwidth compression
WB	Writeback
WFD	Wi-Fi display



Questions?

https://createpoint.qti.qualcomm.com