SDM670/SDM710/SDM712 Linux Android PMIC Software Drivers Overview

80-PD126-4 Rev. C

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Revision History

Revision	Date	Description
A	August 2017	Initial release
B	April 2018	Updated title and other minor SDM710 updates
C	October 2018	Updated for SDM712

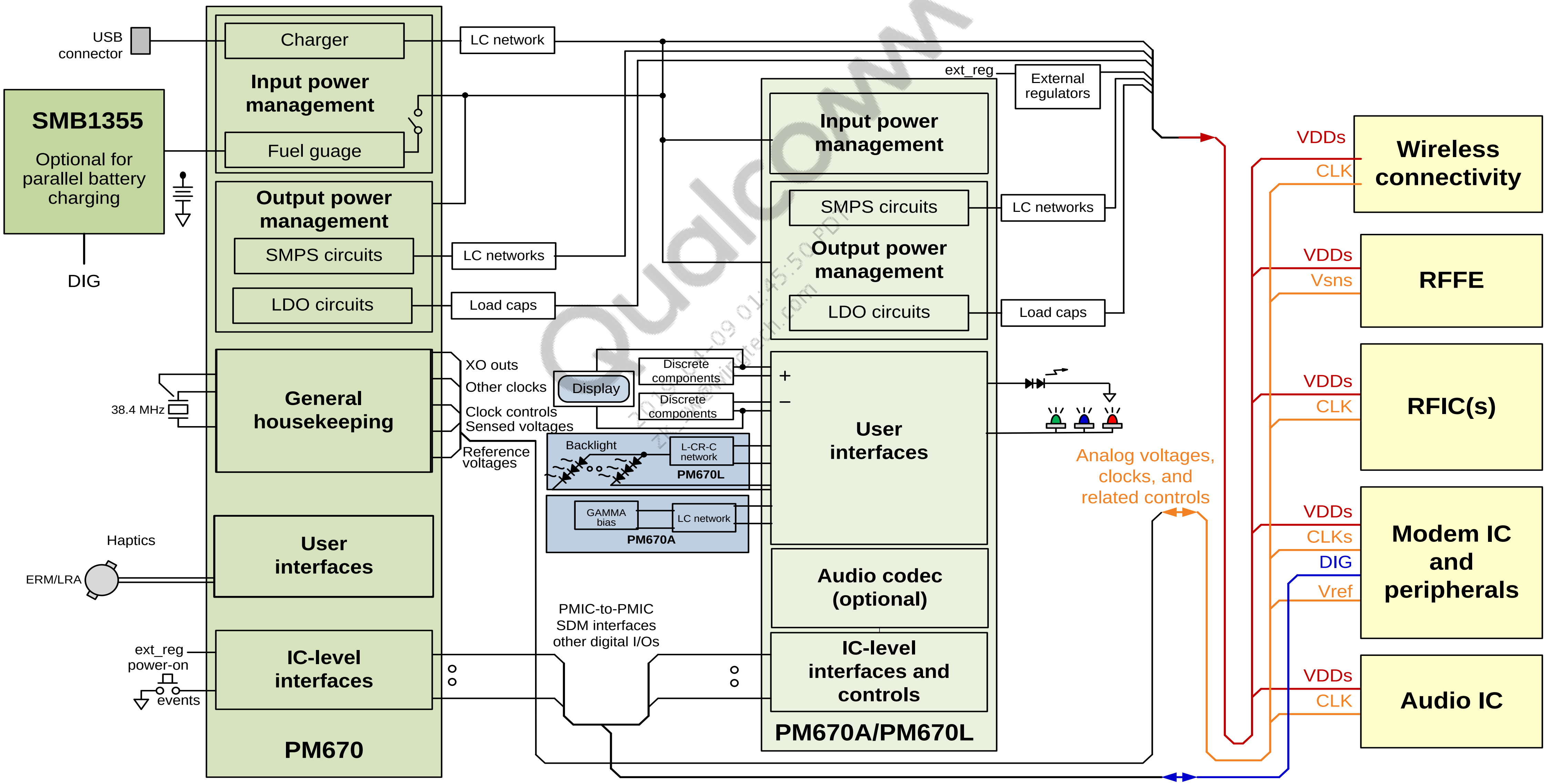
Contents

Introduction

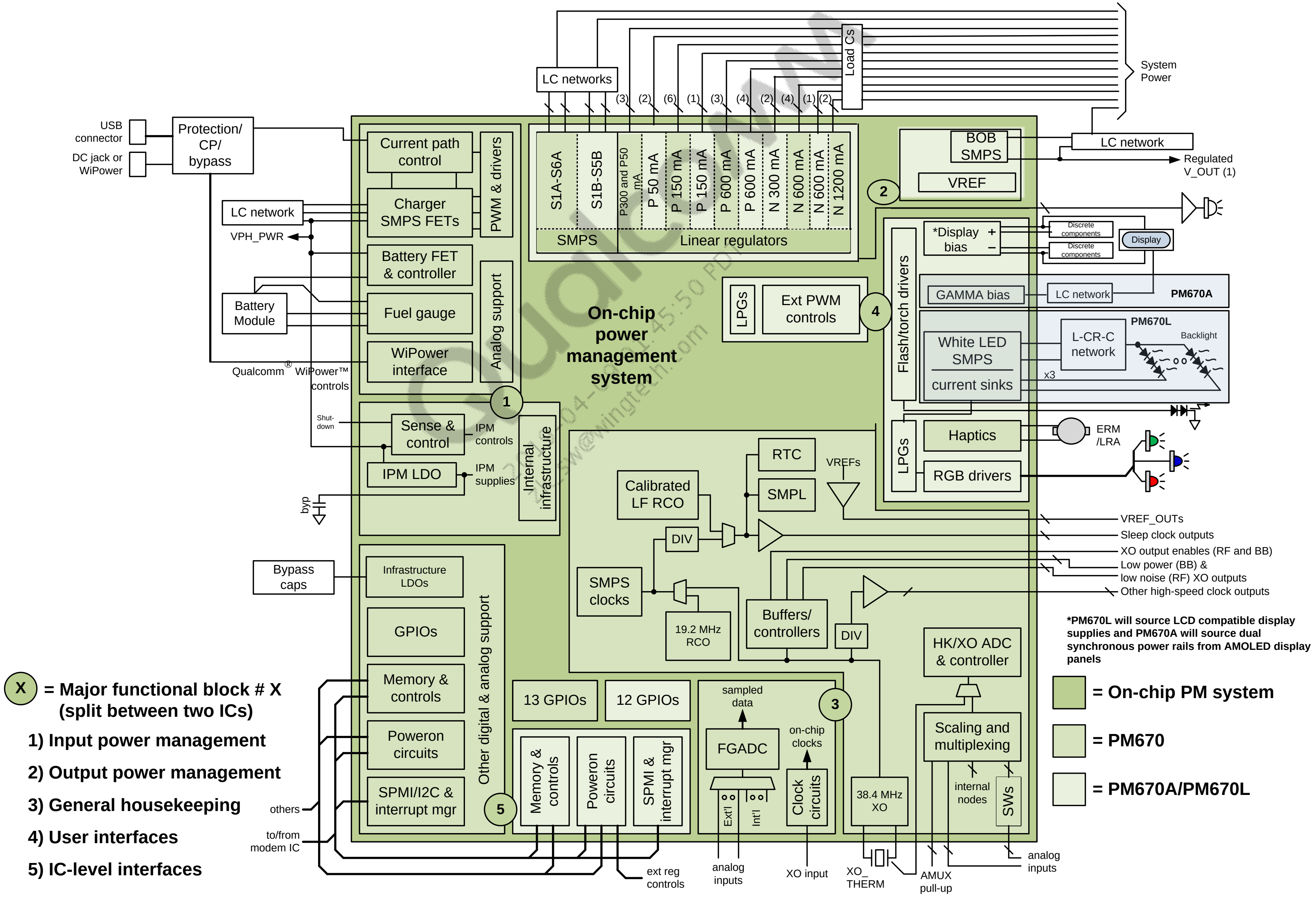
Scope

- At the end of this presentation, you will understand the modules that are controlled by the Linux PMIC software drivers.
- For further details, refer to the module-specific user guides.

SDM670/SDM710/SDM712 PMIC Solution Diagram



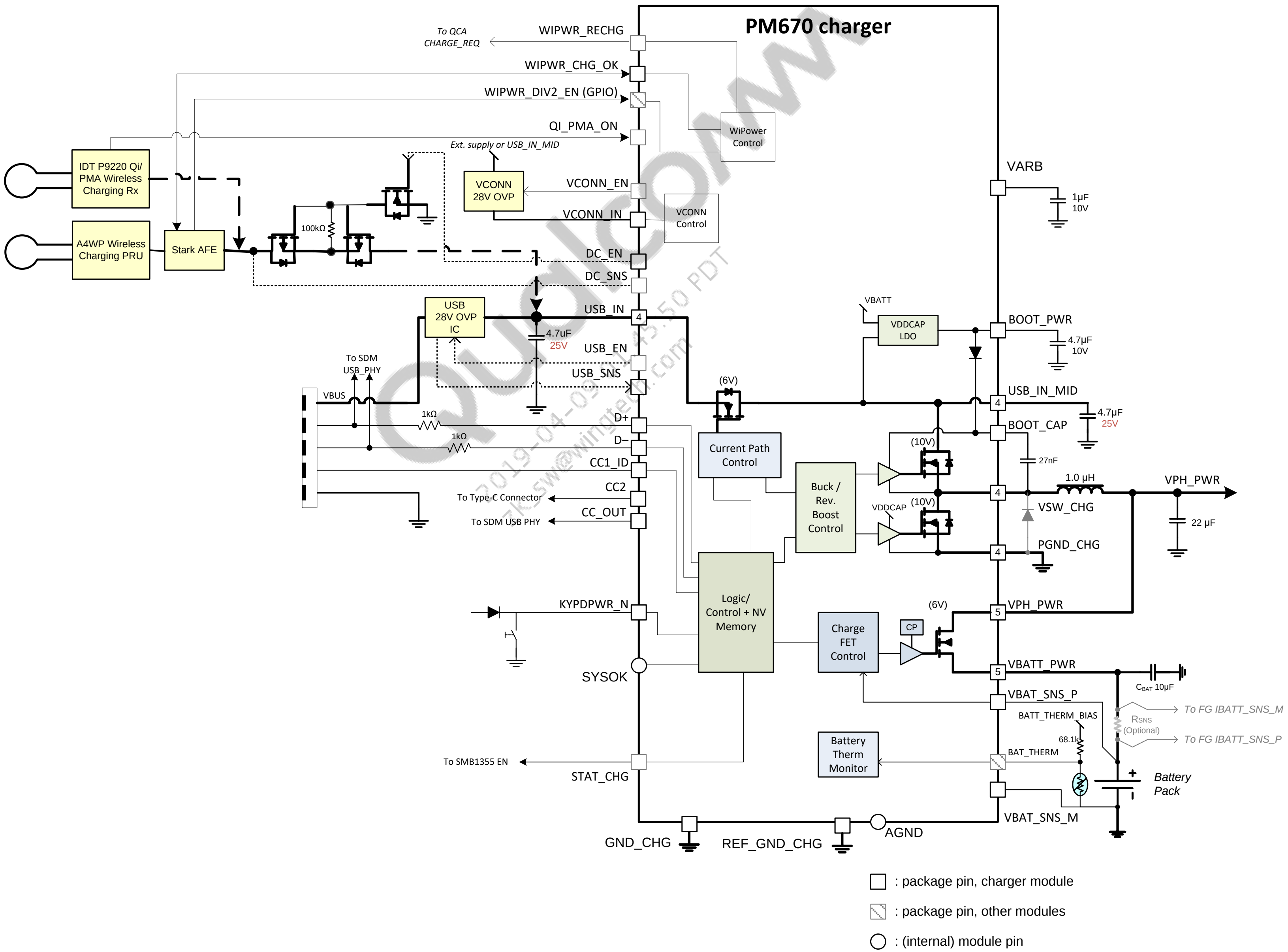
On-chip Power Management System Diagram



Input Power Management

Charging

Hardware Block Diagram



Features of Switching Charger (SCHG)

- Low-power dissipation charger with approximately 1.18 W at 3 A charge current
  - 84 mΩ total charge path resistance designed to take advantage of high duty-cycle (minimum headroom) charging offered by Qualcomm® Quick Charge™ technology v3.0 and v4.0
- Dual source using external OVP + FET control
  - USB_IN – 3.6 V to 10 V input voltage range and 16 V OVP with support for 5 V and 9 V adapters
  - DC_IN – 3.6 V to 10 V input voltage range for wireless charging
- Hardware autonomous Quick Charge v2.0 and v3.0
- Software-based Quick Charge v4.0
- Intelligent negotiation for optimum voltage (INOV) Gen 3 support to find optimal input voltage for the fastest possible charge time while staying within thermal boundaries
  - Internal die temperature and external skin temperature monitoring is performed with ADCs that feed into the hardware thermal INOV algorithm

Features of Switching Charger (SCHG) (cont.)

- Integrated USB Type-C detection, upstream facing port (UFP) or downstream facing port (DFP) mode support, VCONN support, and integrated USB PD PHY
- Differential battery voltage sensing for faster charge time (longer coulomb count duration) and precision EOC accuracy
- Advanced battery cycle-life extension through hardware autonomous step charging and Qnovo software

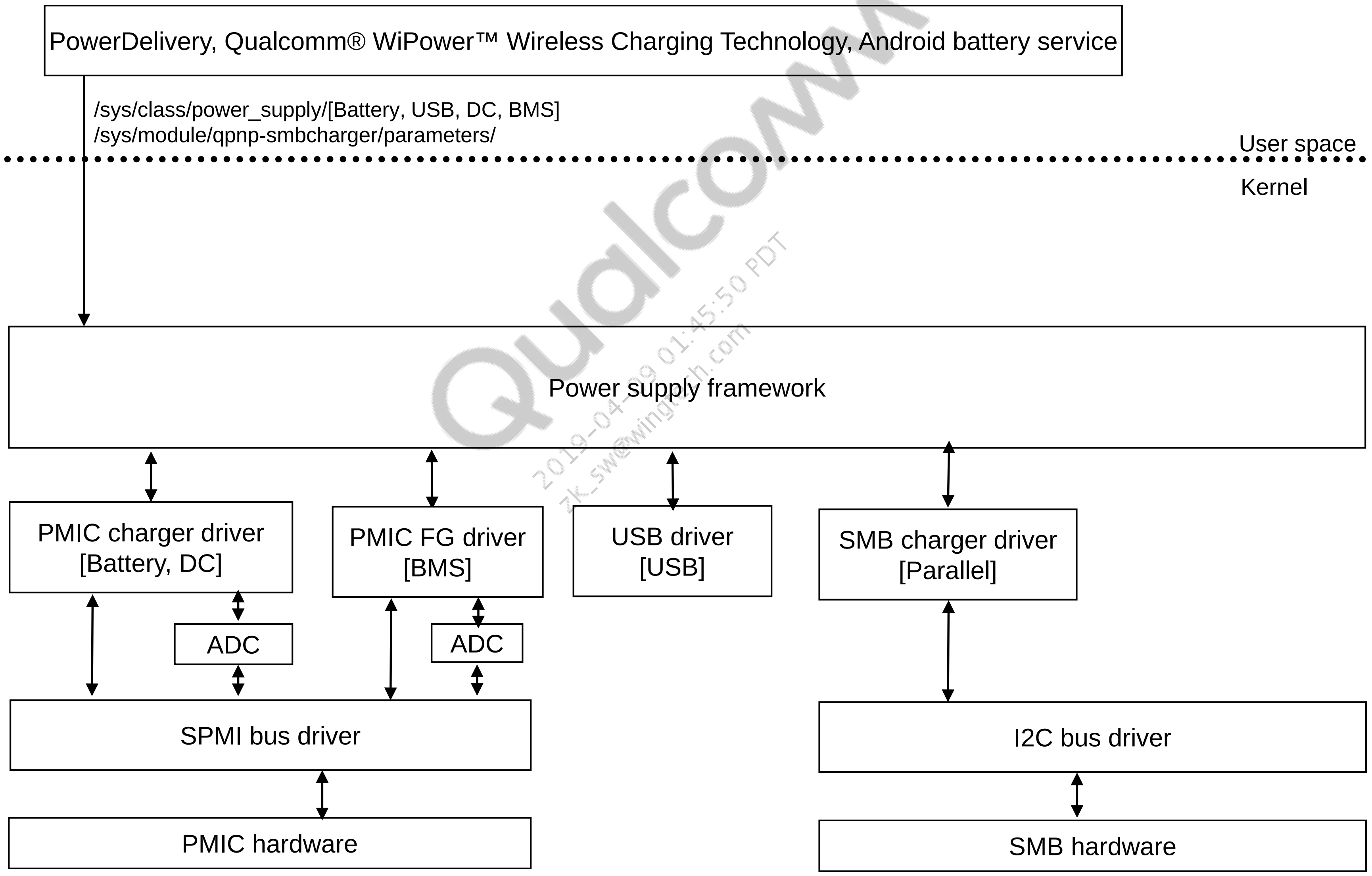
PM670 vs. PMI8952 Features and Performance

Feature	PMI8952	PM670	Comments
USB OVP	28 V	16 V	–
External PMUX support	Yes	Yes	–
USB_IN operating maximum	10 V	10 V	–
ICL range	0 A to 3 A	0 A to 5 A	–
Hardware Quick Charge v2.0	Yes	Yes	5 V and 9 V levels
Hardware Quick Charge v3.0	Yes	Yes	3.6 V to 9 V in 200 mV steps
Quick Charge v4.0	No	Yes	–
Hardware INOV Gen 3	No	Yes	Quick Charge v2.0, v3.0, and v4.0 optimal adapter voltage is selected based on target charge current and skin and die temperature
Hardware USB Type-C detection	No	Yes	Supports DRP, VCONN, try.SRC (Source), and try.SNK (Sink)
Integrated USB PD-PHY	No	Yes	–
Wireless charging hardware support	No	Yes	AirFuel Alliance magnetic resonant specification

PM670 vs. PMI8952 Features and Performance (cont.)

Feature	PMI8952	PM670	Comments
Fast charge current range	25 mA to 3 A	25 mA to 5 A	–
FC step size	25 mA	25 mA	–
VFLT step size	7.5 mV	7.5 mV	–
Differential battery voltage sense	Yes	Yes	Achieves faster charge time and more accurate termination.
FP FET + HS FET + batt FET RDSON	141 mΩ	84 mΩ	Low charge path resistance to optimize around higher duty-cycle and lower voltage operation.
FSW	1 MHz	0.6 MHz to 2 MHz	Accommodates different inductor sizes (optimal IPEAK).
External skin temperature monitoring	No	Yes	Uses external thermistor to monitor skin or connector temperature.
Parallel charging external RSENSE required	Yes	This information will be provided in a future revision of this document	This information will be provided in a future revision of this document
Maximum boost (OTG) current	1.0 A	1.5 A	This information will be provided in a future revision of this document
Boost (OTG) short-circuit hiccup mode	No	Yes	–
Boost output voltage	5 V	5 V to 5.3 V	USB Type-C maximum = 5.5 V
Three-level watchdog timer	No	Yes	Timers are programmable
Telemetry ADC	No	Yes	Measures die temperature, remote temperature, both input voltages, input currents, battery voltage, and charge current

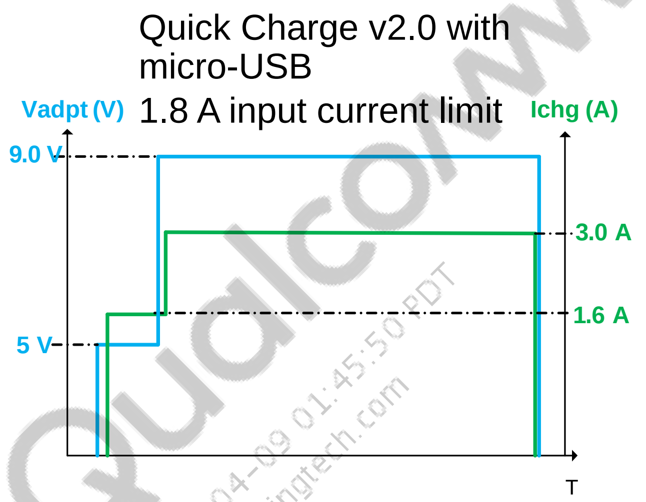
Software Block Diagram

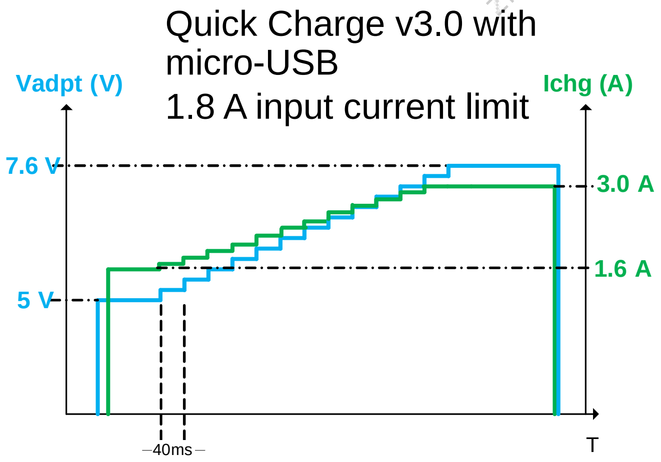


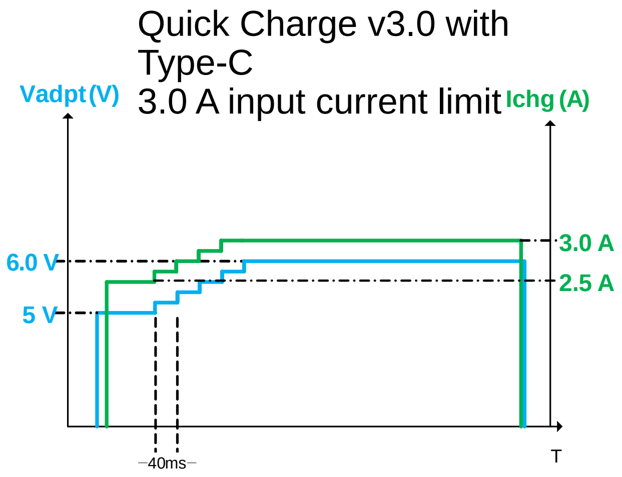
Quick Charge v3.0 with USB Type-C

- Allows 200 mV step adjustments of the adapter voltage from 3.6 V to 10 V vs. 5 V or 9 V, which is used for v2.0
- To optimize charger buck PDISS, operate at the lowest possible V_{in} for a target charge current
  - Buck switching losses, inductor AC core losses, and RMS currents decrease with lower V_{in}
- USB Type-C allows up to 3 A of current from the cable or connector vs. 1.8 A with micro-USB

Quick Charge v3.0 with USB Type-C (cont.)





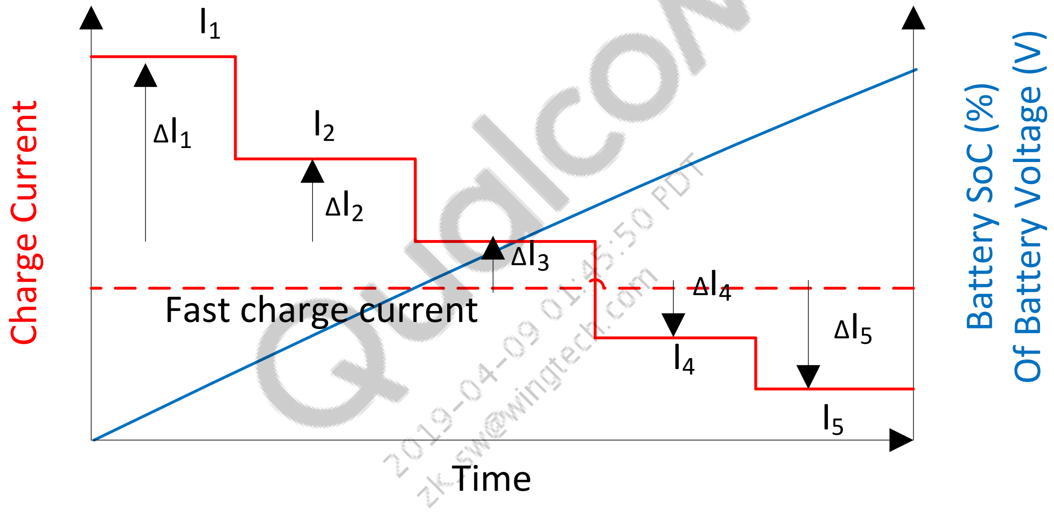


Step Charging

- A hardware autonomous algorithm to enable a staircase charging profile for lithium-ion battery packs
- Allows programmable charge current values based on programmable thresholds on battery voltage or state-of-charge (SoC)
- Industry research has shown that adjusting the battery charge current based on the battery SoC leads to extended battery capacity over a number of charge cycles
- This implementation relies on battery characterization data from battery cell manufacturers to determine the charging profile
- Up to five current steps are implemented, depending on the configuration of PM670. Higher charge currents are momentarily programmed to yield a step charging profile
- This implementation relies on battery characterization data from battery-cell manufacturers to determine the charging profile to be used
- The following are the programmable step charging options:
  - Battery voltage-based
  - Battery-SoC-based
  - Float voltage compensation-based

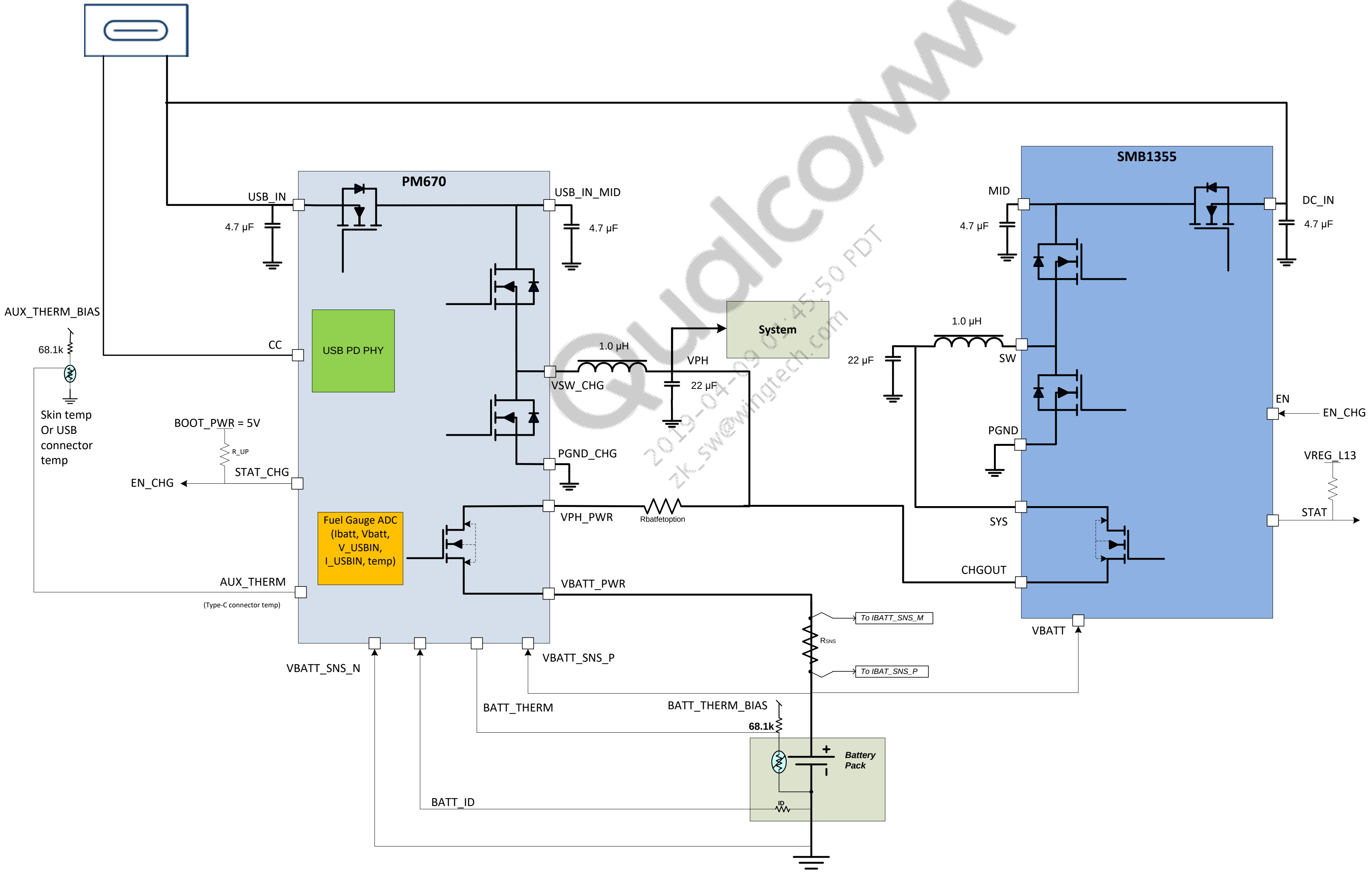
Programmable Current Steps

- Each current step is programmed as a delta from I3, which is the baseline fast charge current



Charge current delta	Current delta minimum	Current delta maximum	Step
$I_{STEP\_DELTA\_1}$	-3.1 A	+3.2 A	0.100 A
$I_{STEP\_DELTA\_2}$	-3.1 A	+3.2 A	0.100 A
$I_{STEP\_DELTA\_3}$	-3.1 A	+3.2 A	0.100 A
$I_{STEP\_DELTA\_4}$	-3.1 A	+3.2 A	0.100 A
$I_{STEP\_DELTA\_5}$	-3.1 A	+3.2 A	0.100 A

PM670 and SMB1355 Parallel Charging



Software Support

eXtensible boot loader (XBL)	XBL UEFI	APSS (HLOS)

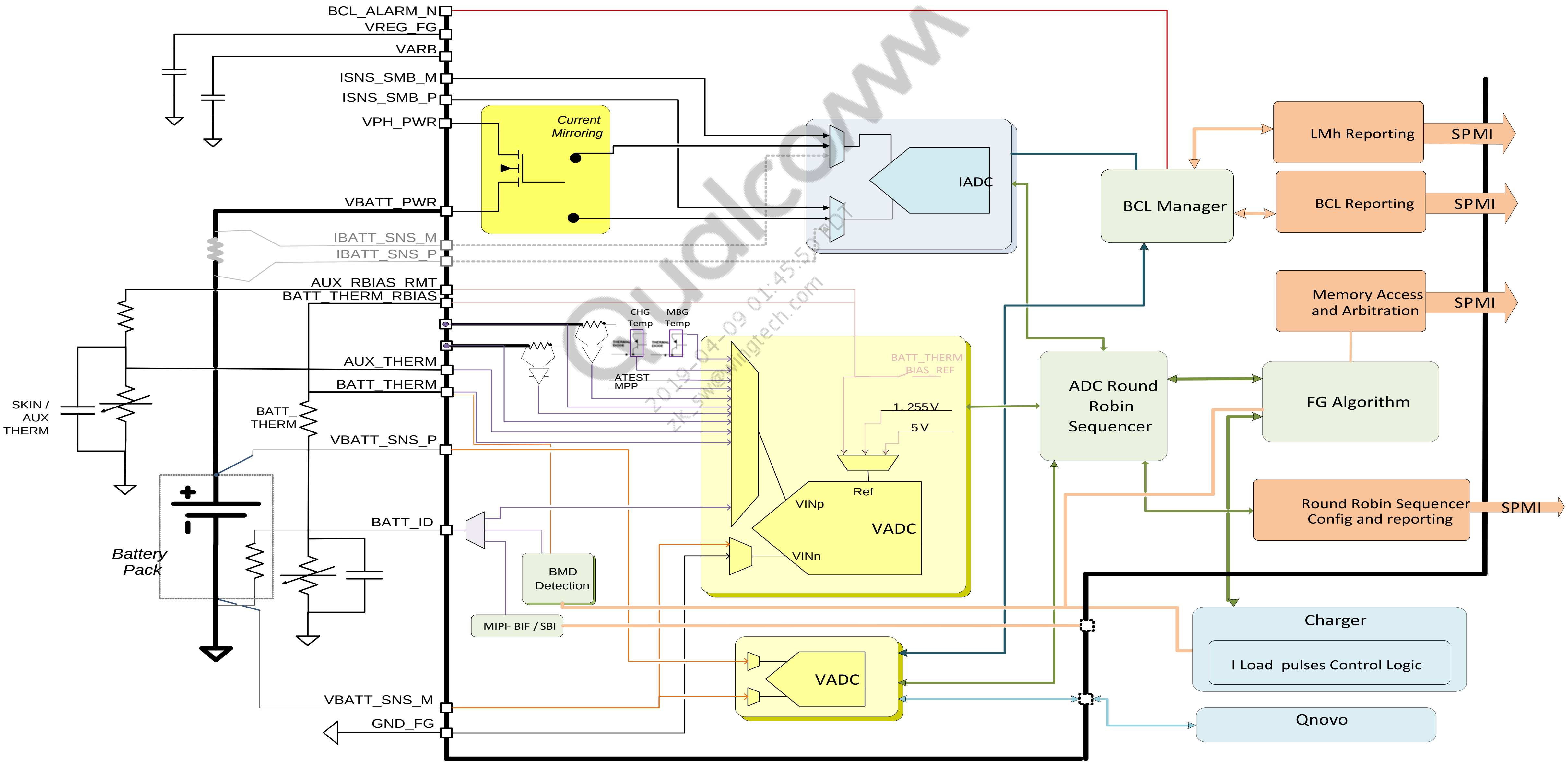
▪ Dead battery charging up to 3.4 V V_{BATT}.
▪ Features
  ▪ Precharging
  ▪ Fastcharging
  ▪ Hardware-controlled Quick Charge v2.0 and v3.0
  ▪ Hardware-controlled parallel charging
  ▪ Hardware-controlled automatic power source detection
  ▪ Hardware-controlled automatic input current limiting
  ▪ Hardware-controlled Type-C detection
	▪ Weak battery charging up to 3.6 V V_{BATT}
	▪ Features
	  ▪ Fastcharging
	  ▪ Hardware-controlled Quick Charge v2.0/v3.0
	  ▪ Hardware-controlled parallel charging
	  ▪ Hardware-controlled automatic power source detection
	  ▪ Hardware-controlled automatic input current limiting
	  ▪ Hardware-controlled Type-C detection
		▪ Features
		  ▪ Fastcharging
		  ▪ Taper charging
		  ▪ Step charging
		  ▪ Qnovo support
		  ▪ USB PowerDelivery software support
		  ▪ Hardware-controlled Quick Charge v2.0/v3.0
		  ▪ Quick Charge v4.0 software Power Delivery based
		  ▪ Hardware-controlled parallel charging
		  ▪ Hardware-controlled automatic power source detection
		  ▪ Hardware-controlled automatic input current limiting
		  ▪ Hardware-controlled Type-C detection

Software Support (cont.)

Feature	Support	Details
APSD	Hardware	Hardware is autonomous with interrupt notification to software
AICL	Hardware	Hardware is autonomous with interrupt notification to software
Pre charging, fast charging, or Taper charging	Hardware	Hardware is autonomous with interrupt notification to software and threshold configuration in charger software
Step charging	Hardware	Hardware is autonomous with interrupt notification to software
JEITA	Hardware	Hardware is autonomous with interrupt notification to software and threshold configuration in FG software
Type-C UFP or DFP detection and negotiation	Hardware	Hardware is autonomous with interrupt notification to software (charger software reports Type-C presence to USB software)
Quick Charge v2.0 and v3.0	Hardware	Hardware controls both versions autonomously without software
USB Power Delivery	Software	USB software daemon handles PD negotiations and instructs the charger driver on VBUS and input current limit settings based on PD profile
Parallel charging (fast charging)	Hardware and software	Hardware controls and enables parallel charging for the fast charging phase. Input current splitting is not required as it is done through PM670. Software conducts FCC (battery current) balancing
Parallel charging (taper charging)	Hardware and software	Charger software steps down the slave charger ICs charging current during taper charging since that is not hardware autonomous
Qnovo	Software	The Qnovo user space daemon uses the PMIC charger driver to drive and shape pulses
USB OTG	Software	USB OTG support remains the same and software enables the reverse boost for OTG support based on the USB driver’s instruction

Fuel Gauge

Hardware Block Diagram

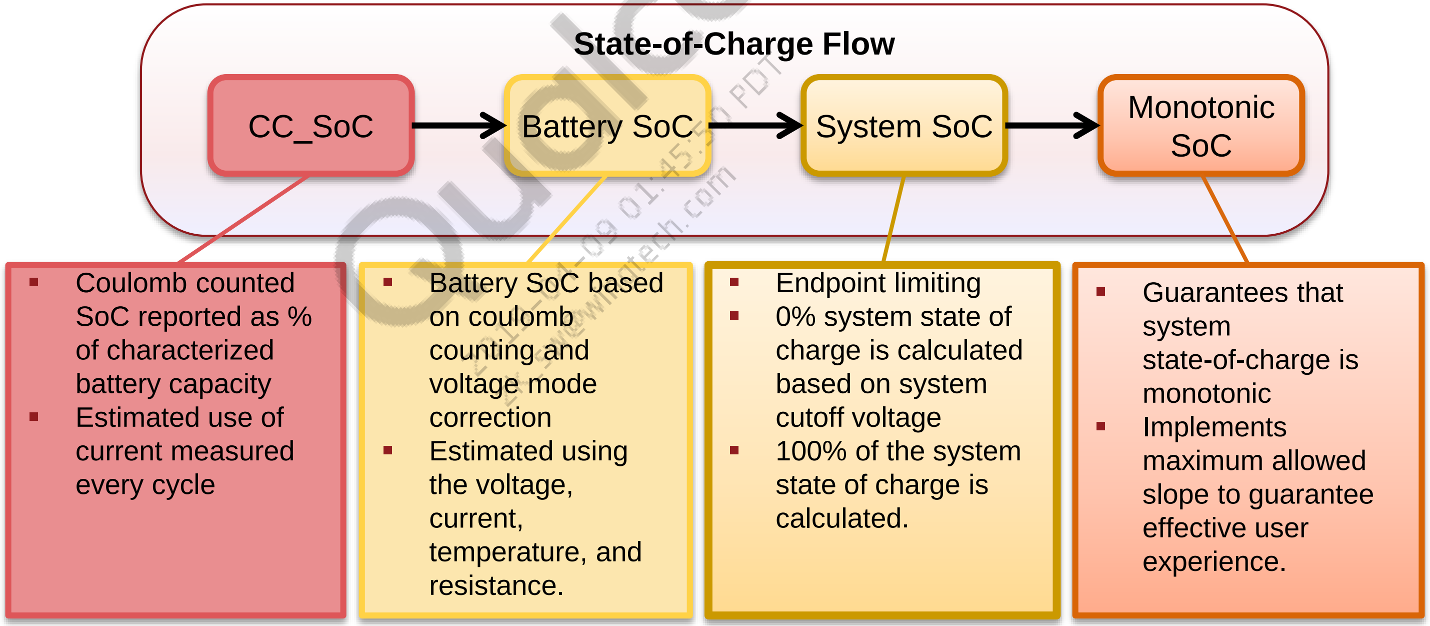


Overview

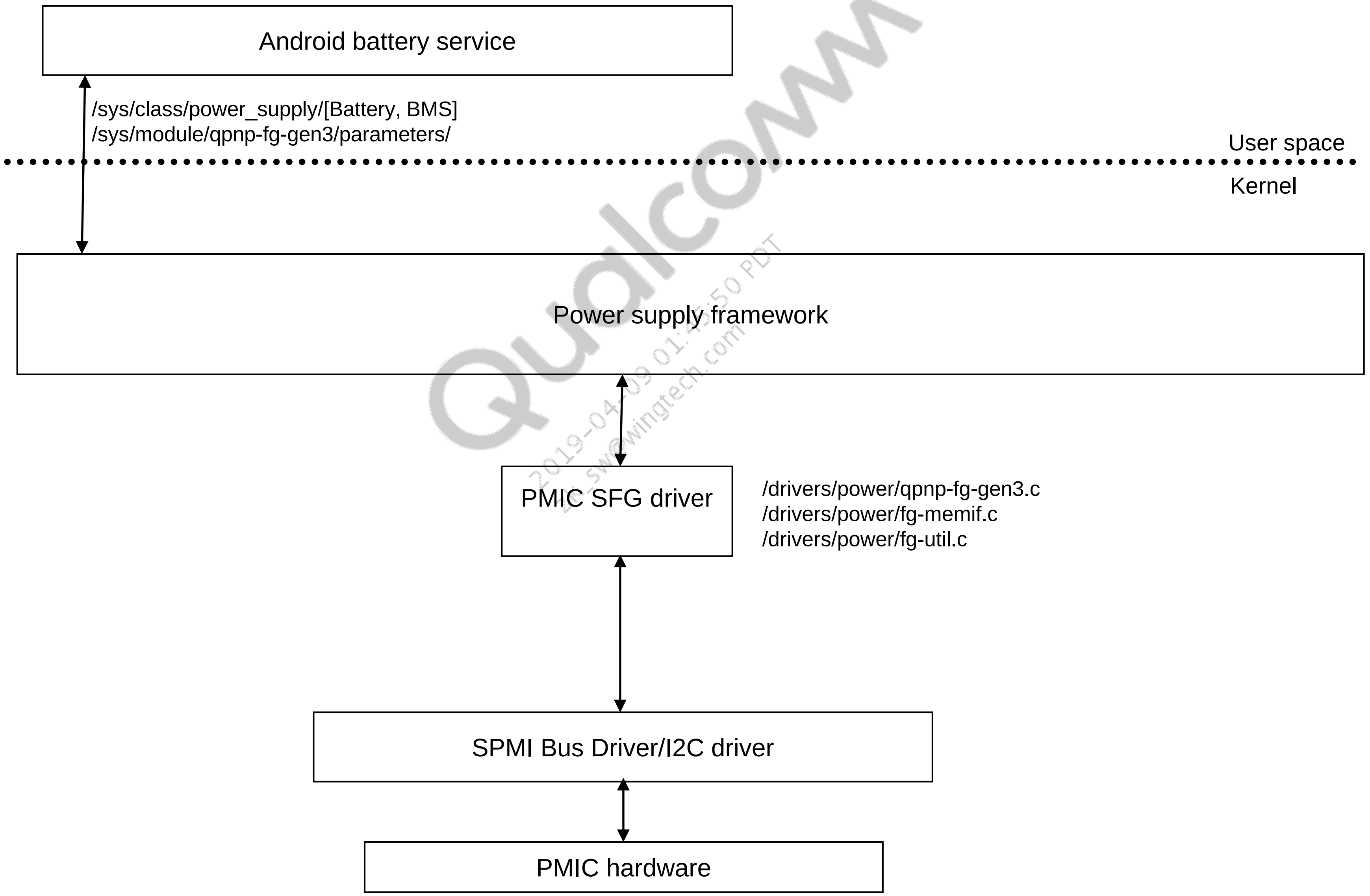
- Supports optimized mixed algorithm with current and voltage monitoring
- Provides a highly accurate battery state-of-charge estimation
- Provides 16-bit dedicated current ADC (15-bit and sign bit)
- Provides 15-bit dedicated voltage ADC for measuring V_{BATT}, BATT_THERM, and BATT_ID
- Operates independently of software and reports state-of-charge without algorithms running on the modem device
- Provides precise voltage, current temperature, and aging compensation
- Supports battery missing detection
- Supports remote thermistor sensing
- Does not require complete battery cycling to maintain accuracy
- Does not require external nonvolatile memory
- Does not require external configuration

Hardware Algorithm – Overview

- Fuel gauge uses four states-of-charge to arrive at the final state-of-charge reported to the end user.
- Each stage of the flow contributes to the final monotonic SoC reported to the end user.



Software Overview

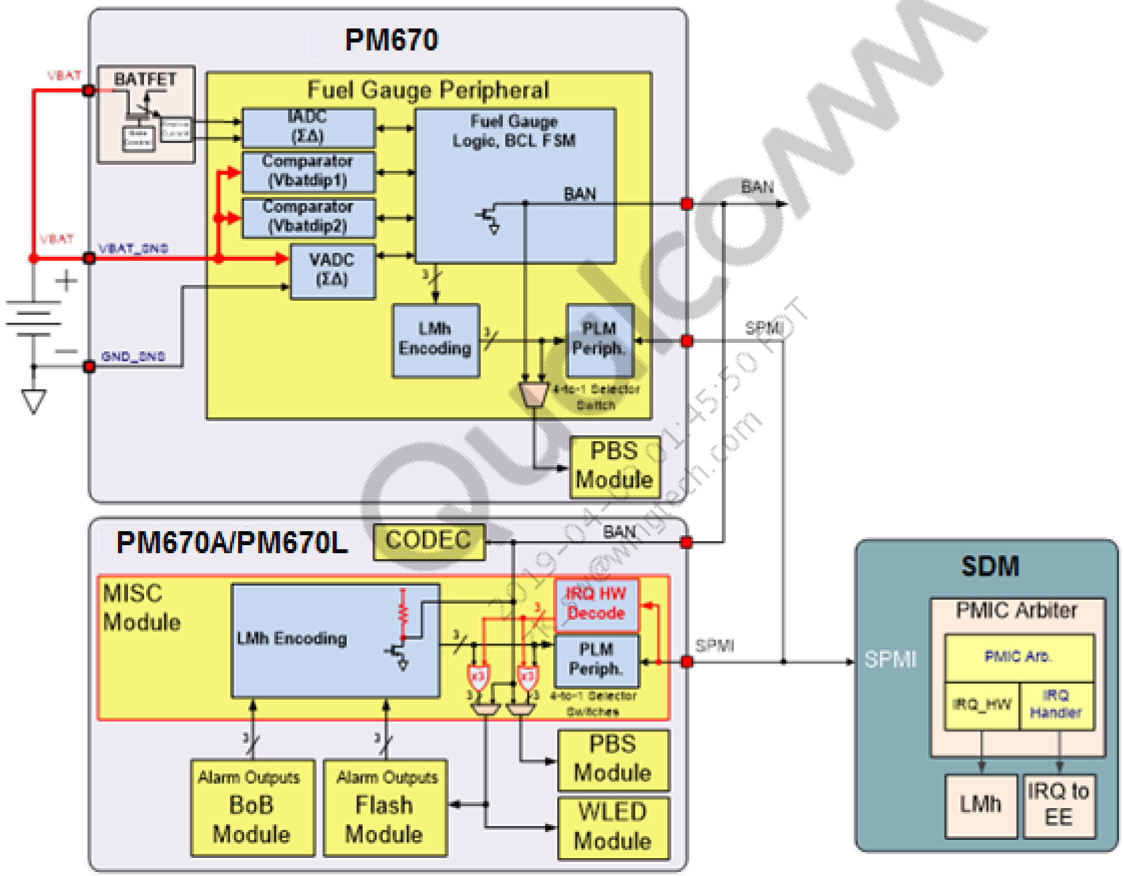


Software Overview (cont.)

- Supports new FG driver modularizing architecture for easy expanding
- Supports abstraction of underlining system bus (SPMI)
- Supports new memory architecture access
- Supports battery profile loading and first SoC detection in LK or UEFI and/or HLOS, battery hotswap and/or new battery insertion
- Provide improved FG notifications upon PON
- Improved SoC reporting with enhance OCV, ESR to Rslow mapping,
- Improved FG status reporting – Cut off, empty, delta SoC, delta ESR
- Advance battery capacity learning and charge cycle count
- Supports battery current limiting (BCL) threshold reporting and settings
- Supports the Trepn requirements
- Supports the new FG ADC peripheral activities (round robin ADC channels sequencing)
- Supports FG battery current sensing
- Supports sleep current monitoring
- Supports integrated charger requirements

BCL

Hardware Block Diagram



Introduction

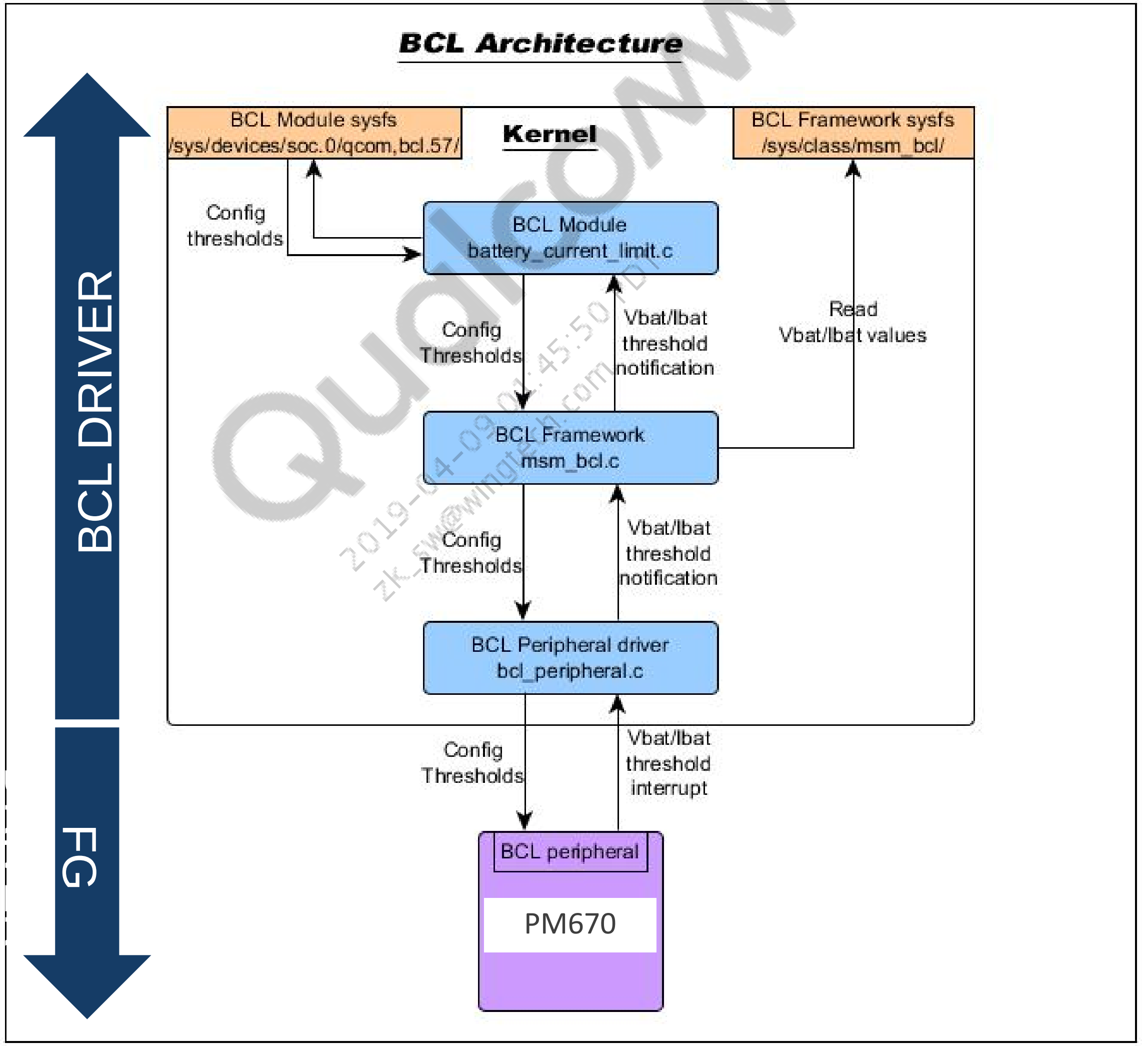
- The BCL hardware is designed to address the following:
  - Prevent battery OCP events
    - Monitors battery current to ensure that the pack protection is not tripped
    - In the event of a trip, warns the relevant subsystems to take appropriate action
    - Mitigates in PMIC and communicates with EEs
  - Protect against OCP events
    - Disconnects the battery cell within the pack
    - Avoids the OCP events through BATFET disconnect
  - Prevent system UVLO
    - Monitors battery voltage to ensure that there is no dip below the UVLO threshold
    - In the event of a dip, warns the relevant subsystems to take appropriate action
    - Mitigates in PMIC and communicates with EEs
  - Permit maximized processor performance
    - Allows aggressive processor frequency scaling and core hot-plug management

PM670 Mitigation Level Actions

Mitigation level	Alarm sources	Alert mechanism		Resulting system action								
		SPMI	BAN	LMh ()	CPU (software)	Graphics (software)	Codec (software or hardware)	RF PA (software or hardware)	Flash (hardware)	Charger OTG	Backlight (hardware)	BATFET (hardware)
A	▪ PMI – Legacy BCL VADC ▪ PM - Vphdip0 ▪ PMI – BOB LMh Level 0 (VCOMP_LOW0)	Int.	No	Level 0 reduces clock by 25% or reduced current limit by 25%	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B	MDM - TX_GTR_THR	Int.	No	N/A	N/A	N/A	-3 dB hardware	N/A	Reduce current	N/A	Reduce current by 50%	N/A
C	▪ PMI - Ibat_high ▪ PMI - Vbat_low ▪ PMI – BOB LMh Level 1 ▪ PM - Vphdip1 (VCOMP_LOW1)	Int.	No	Level 1 (reduce clock by 50% or reduced current limit by 50%)	Unplug 1X sLVT	Some	-3 dB software	-3 dB software	Reduce current	N/A	Reduce current by 50%	N/A
D	▪ PMI - Ibat_too_high ▪ PMI - Vbat_too_low ▪ PMI – BOB LMh Level 2	Int.	No	Level 2 (reduce clock by 75%or reduced current limit by 75%)	Unplug 1X sLVT	More	-3 dB software	-3 dB software	Reduce current	N/A	Reduce current by 50%	N/A
E	▪ PMI – BAN (Ibat_too_high_4ms or Vbat_too_low_4ms) ▪ PM - Vphdip2 (VCOMP_LOW2)	Int.	Yes	Level 2 (reduce clock by 75% or reduced current limit by 75%)	Unplug 2X sLVT	More	- 6 dB hardware	- 6 dB hardware	Reduce current	Disabled	Reduce current by 50%	N/A
F	▪ PMI - Ibat_too_high_8ms ▪ PMI - Vbat_too_low_8ms ▪ PMI or PM - UVLO	Int.*	Yes*	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Open and SMPL

*Interrupt and BAN signal are fired as part of the mitigation level E.

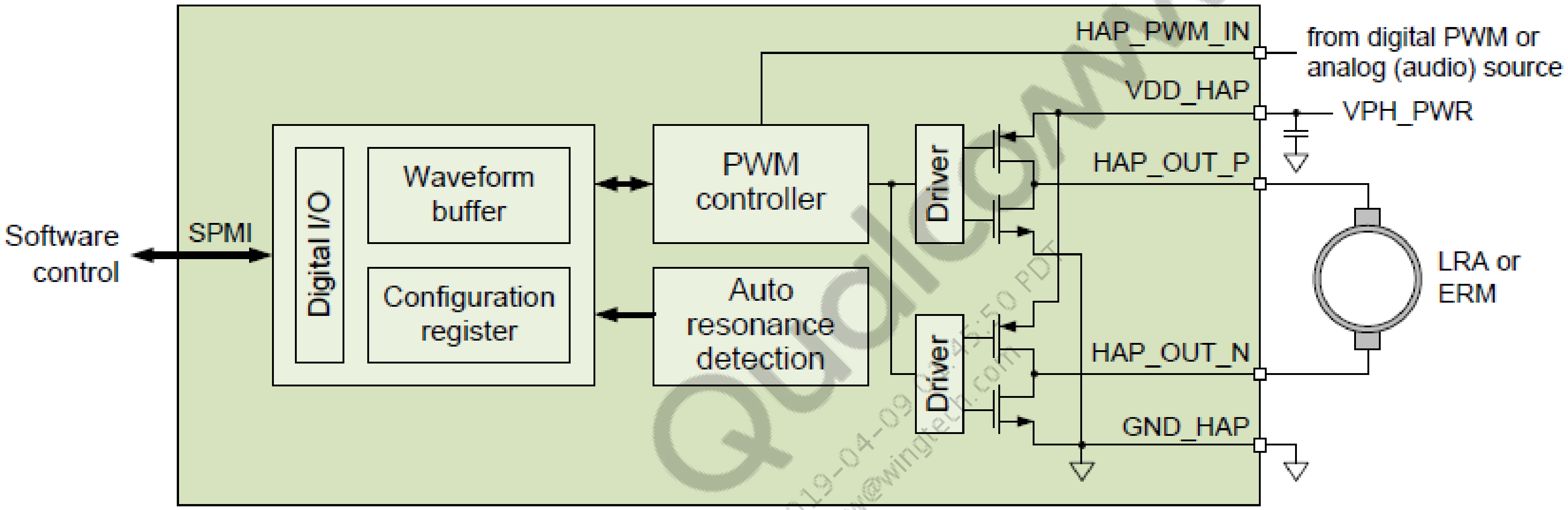
PM670 BCL Software Block Diagram



User Interface

Haptics

Hardware Block Diagram



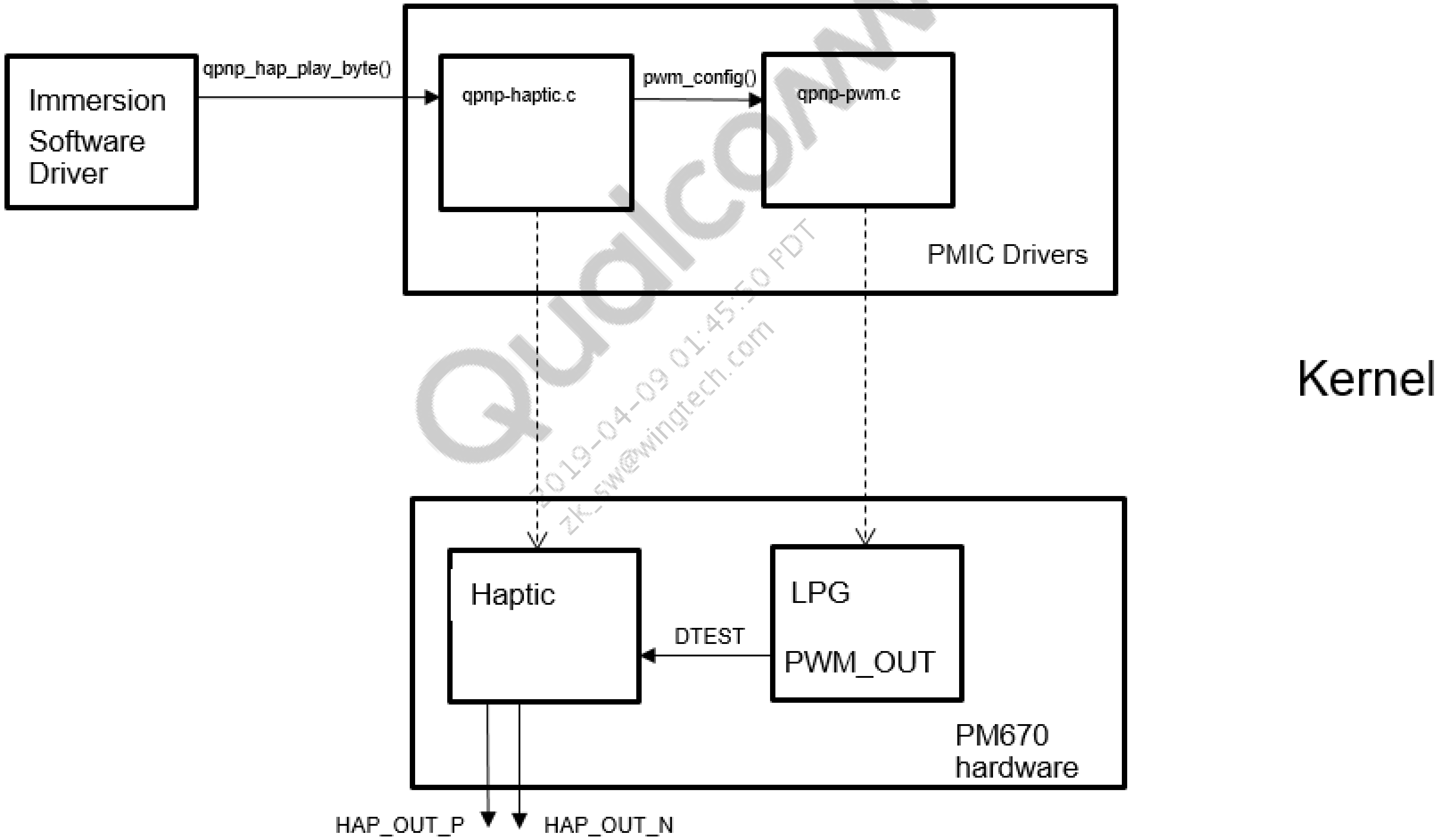
Overview

- Haptics uses vibration to communicate an event or action through human touch. In a mobile phone, haptics is used to simulate the feeling of a real mechanical key by providing tactile feedback to the user as a confirmation of touchscreen contact, or dynamic feedback to enhance the user's gaming experience.
- Key features:
  - Software selectable linear resonant actuator (LRA) or eccentric rotating mass (ERM)
  - Supply voltage correction for direct connect to phone power; wide input voltage range from 2.5 V to 4.75 V
  - Dedicated pin for analog line input from audio codec to drive synchronized haptics waveform
  - PWM H-bridge drive with 500 mΩ (typ) RDS_ON for high efficiency; programmable from 250 kHz to 1000 kHz
  - Programmable maximum output driver voltage from 1.2 V to 3.6 V to cover wide range of ERM or LRA
  - 8 byte internal waveform buffer for storing and playing haptics patterns; loop function for repeating patterns

Overview (cont.)

- Key features:
  - Auto resonance detection for LRA with wide tracking range; programmable range from 50 Hz to 300 Hz
  - Overcurrent or short-circuit protection
  - H-bridge driver can set a PWM output with a configurable amplitude of 1.2 V to 3.6 V. It allows simple vibration and/or complex patterns, depending on the product’s needs
  - Waveform input as digital samples from buffer or as analog signal from line-in, converted to a PWM signal
  - ERM is a DC motor with off-centered mass – requires DC drive signal
  - LRA is a resonator – requires AC drive signal
  - Haptics driver automatically configures signaling based on the software-selected actuator type; enables the selected actuator
  - Software-generated patterns for both LRA and ERM
  - Software controls the haptics waveform pattern; the haptics controller generates the drive signal

Software Block Diagram



Software Support

- Haptics supports immersion control by using the internal light pattern generator (LPG) to generate the PWM.

XBL	UEFI	HLOS
▪ Source-boot_images\QcomPkg\Library\PmicLib\drivers\haptics ▪ API – boot_images\QcomPkg\Include\api\systemdrivers\pmic\pm_haptics.h	Same as XBL	▪ Source –kernel/drivers/soc/Qcom/qpnp-haptic.c ▪ DTSI documentation – kernel/Documentation/devicetree/bindings/soc/Qcom/qpnp-haptic.txt ▪ DTSI files – kernel/arch/arm/boot/dts/Qcom/pm670.dtsi

PM670A/PM670L Display Power and Bias

PM670A/PM670L Display Power and Bias

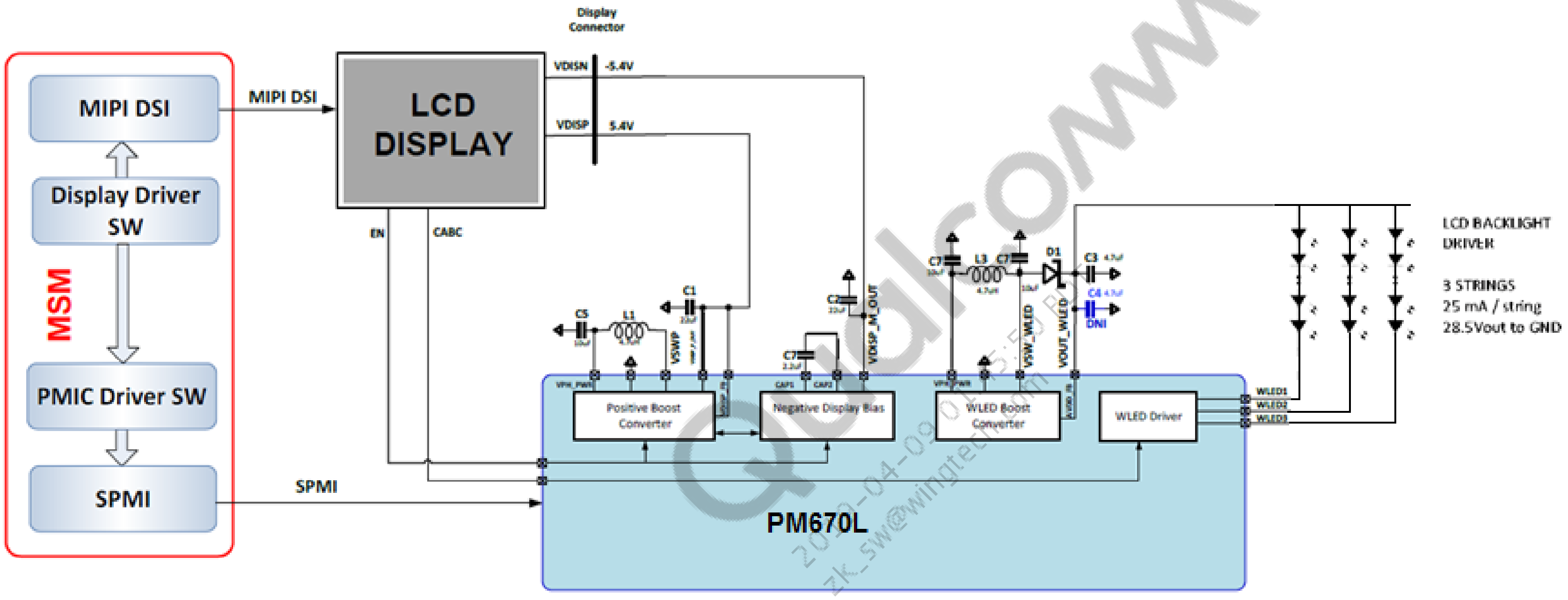
- PMI8952 uses one-chip solution for both the LCD and AMOLED panels. The PM670x solution has dedicated ICs for LED and AMOLED panels
- PM670L is used for LCD display and PM670A for the AMOLED panels
- The PM670x solution is optimized to perform as required for the LCD and AMOLED display panels to remove conflicting requirement of dual IP and reduced BOM requirement

Feature	PMI8952	PM670L
LCD WLED driver	8s4pLED maximum configuration, 30 mA maximum	8s3pLED maximum configuration, 25 mA maximum with improved efficiency
LCD bias power rails	Dual SMPS topology - Boost (LAB) and inverting buck-boost (IBB)	Single inductor double outputs topology optimized for LCD bias supply
	Requires two inductors	Requires single inductor

PM670A/PM670L Display Power and Bias (cont.)

Feature	PMI8952	PM670A
Positive boost supply (LAB) rail	No internal LDO option	Positive boost supply rail (LAB module) includes added series smart LDO to avoid banding
SWIRE	Used for programming only the negative (ELVSS voltage) rail	Used for programming the Gamma bias (OLEDB or AVDD), positive (ELVDD) and negative (ELVSS) rails
AMOLED AVDD programming range	4 default settings → 5.6 V, 5.9 V, 7.46 V, or 7.54 V with software programming for different voltages	5.8 V to 7.9 V in 0.3 V steps with SWIRE control
Gamma bias (OLEDB) supply	▪ Derived from WLED module, thus uses high voltage (30 V) devices ▪ Requires external PFET for input to output isolation when turned Off	▪ AVDD or Gamma bias rail is supplied from dedicated synchronous boost converter. The boost converter uses 10 V devices for better efficiency and smaller size ▪ Does not require external PFET for the input to output isolation since it uses a synchronous converter
	Requires inductor of 10 µH, 2520 × 1.2 mm	Requires smaller inductor of 4.7 µH, 2520 × 0.8 mm

PM670L Hardware Block Diagram



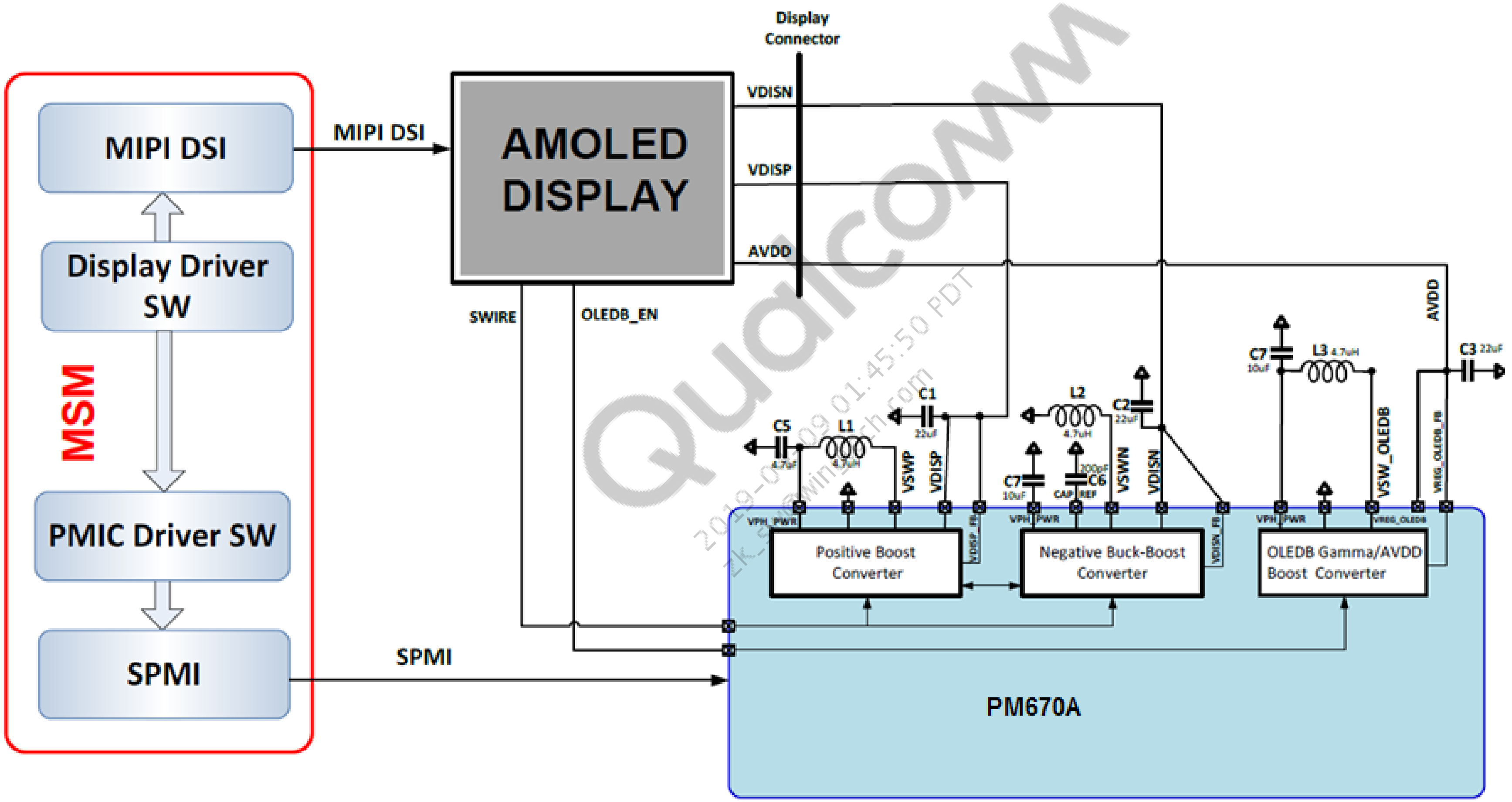
PM670L LCD Bias Features

- Display bias
  - Single inductor double outputs topology optimized for LCD bias supply
  - Integrated front-end DC-DC boost converter for intermediate voltage
  - Integrated LDO for positive bias supply
  - High efficiency negative charge pump for negative bias supply
  - Operating input voltage range 2.5 V – 4.75 V
  - Programmable output voltages (default ± 5.5 V)
  - PFM mode of operation for higher efficiency
  - Touch-to-wake operation
  - Dedicated hardware pin to enable directly from the panel
  - Programmable start-up and shut-down sequence

PM670L LCD Bias Features (cont.)

- White LED (WLED) supply and sinks
  - Support both FHD and QHD screen resolution
  - Design for 3p8s WLED configuration (3 strings – 28 V OVP, 25 mA maximum current)
  - Support PFM mode
  - Design optimized for LCD mode
  - Digital, analog and hybrid dimming capability
  - 12-bit analog dimming resolution
  - 9-bit digital dimming resolution
  - Analog Dimming mode – programmable 12-bit resolution, continuous WLED current
  - Digital Dimming mode – 9-bit resolution, WLED current is pulse width modulated, programmable PWM rate
  - Hybrid Dimming mode – improves auto-optimized dimming efficiency and performance
  - Content adaptive brightness (CABC) capable

PM670A Hardware Block Diagram



PM670A AMOLED Features

Triple supply power solution for AMOLED displays:

- Boost power supply (LAB) at VDISP_P
  - Synchronous boost converter
  - Programmable PWM mode control switching frequency. Programmable output voltage from 4.6 V to 5.0 V
  - 300 mA output current capability
  - ±0.8% DC accuracy over Vbat, temp, and load
  - Soft-start with inrush current limit – short circuit protection (SCP) detection
  - Start-up short detection
- IBB at VDISP_M
  - Synchronous DC-DC converter topology
  - Supports PFM control mode for potential sleep mode-like use cases
  - 2.8 V to 4.75 V input voltage range

PM670A AMOLED Features (cont.)

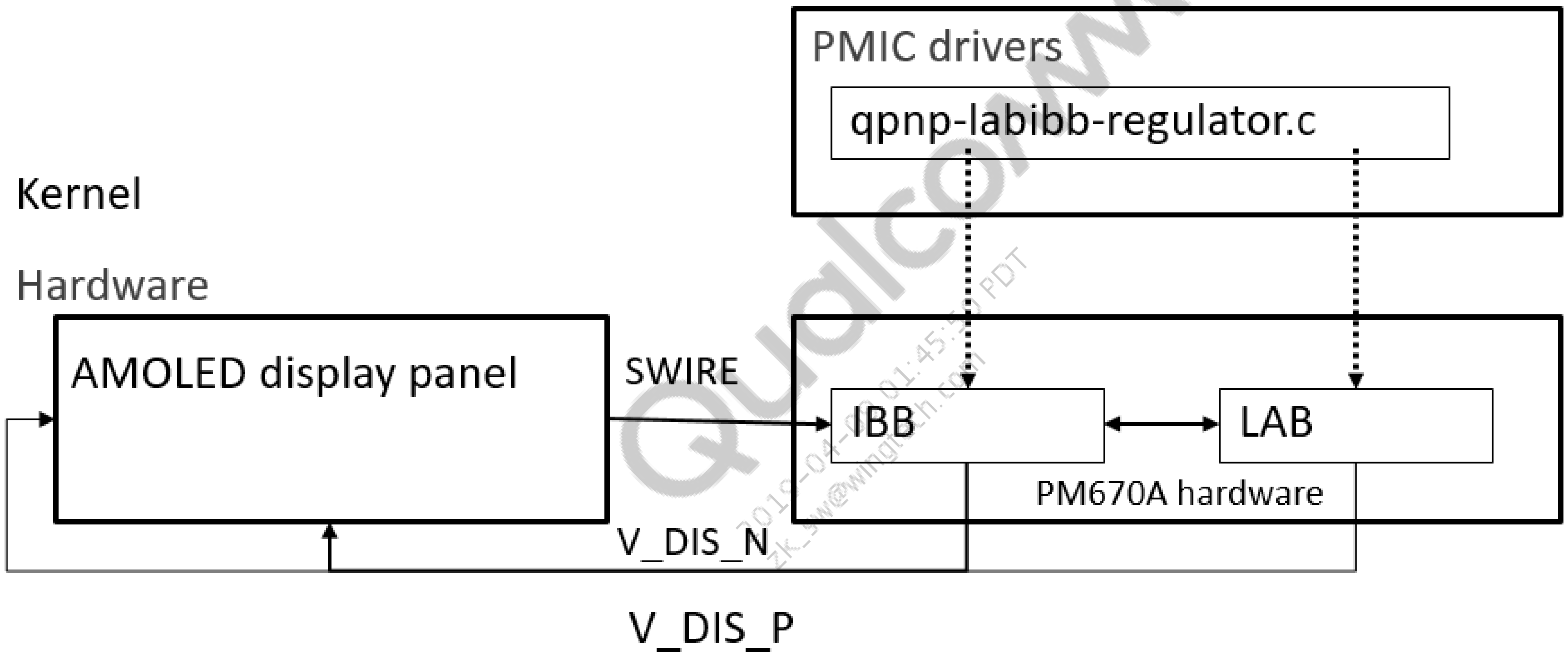
- IBB at VDISP_M
  - Programmable negative output voltages
  - SPMI and SWIRE interface for programming output voltage
  - Programmable output voltage - 0.8 V to - 6.0 V (default value is - 4 V AMOLED)
  - 100 mV resolution
  - +/-20mV Output voltage accuracy
  - 300 mA output current capability
  - Auto output disconnect and active discharge on module shutdown
  - Auto power sequencing on module enable or disable
  - DCM antiringing
  - Pulse Skipping mode for high efficiency at light load
  - Safe power stage disable
  - Low VPH_PWR support

PM670A AMOLED Features (cont.)

- OLEDB boost supply
  - Auxiliary bias rail for all displays greater than FHD
  - Operation across wide range of VPH_PWR (2.5 V to 4.75 V)
  - Fixed bias voltage for a given panel model
  - Adjustable from 5.8 V to 7.9 V in steps of 0.3 V with SWIRE control
  - Output current capability of 60 mA
  - 0.8 MHz to 1.6 MHz switching frequency
  - Pulse Skipping mode for high efficiency under light condition
  - Built-in soft start
  - Ability to power up through both external hardware pin (OLEDB_EN) and SPMI software register
  - Short circuit protection

LAB and IBB

Software Block Diagram

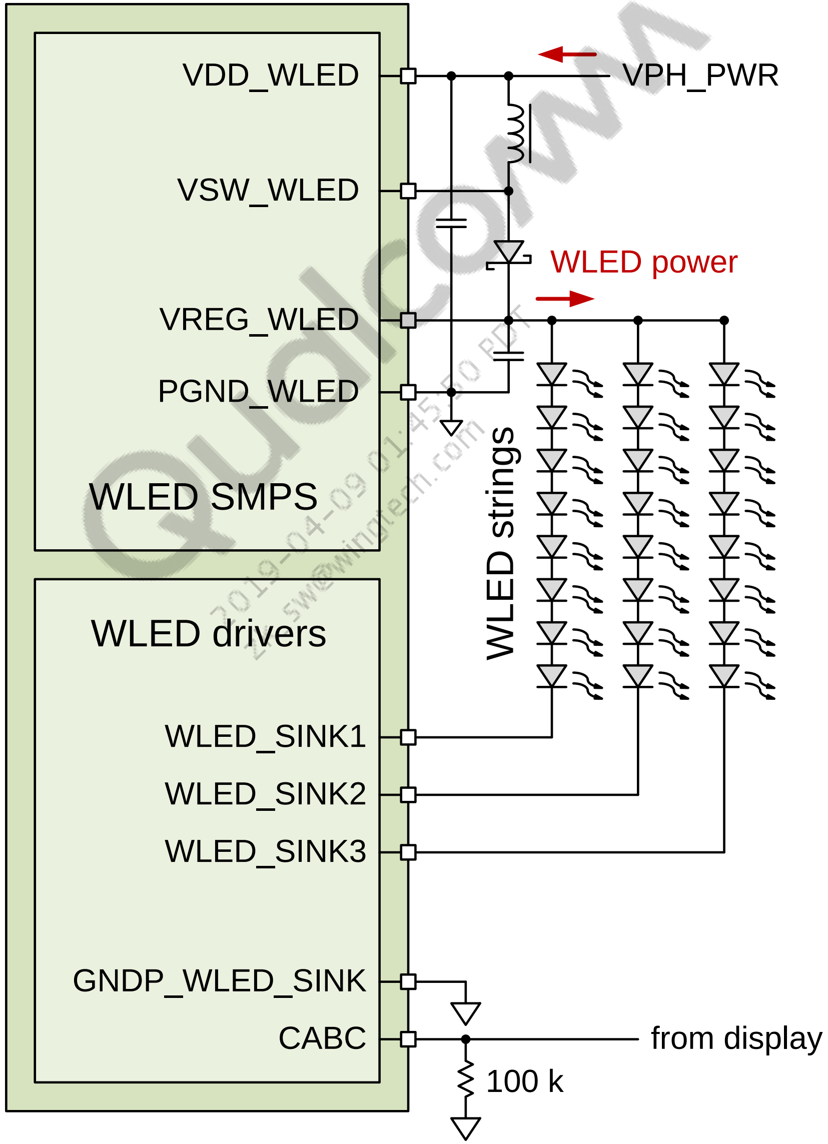


LAB and IBB Software Support

- Software performs one-time-setup configurations for IBBLAB. Hardware controls IBBLAB with the SWIRE pulses for AMOLED.

XBL	UEFI	HLOS
▪ Source –\boot_images\QcomPkg\Library\PmicLib\drivers\ibb ▪ API –\boot_images\QcomPkg\ ▪ Include\api\systemdrivers\pmic\pm_lab.h ▪ \boot_images\QcomPkg\Include\api\systemdrivers\pmic\pm_ibb.h	Same as XBL	▪ Source – kernel/drivers/regulator/qpnp-labibb-regulator.c ▪ DTSI documentation – kernel/Documentation/devicetree/bindings/regulator/ qpnp-labibb-regulator.txt ▪ DTSI files – kernel/arch/arm/boot/dts/Qcom/pm670l.dtsi

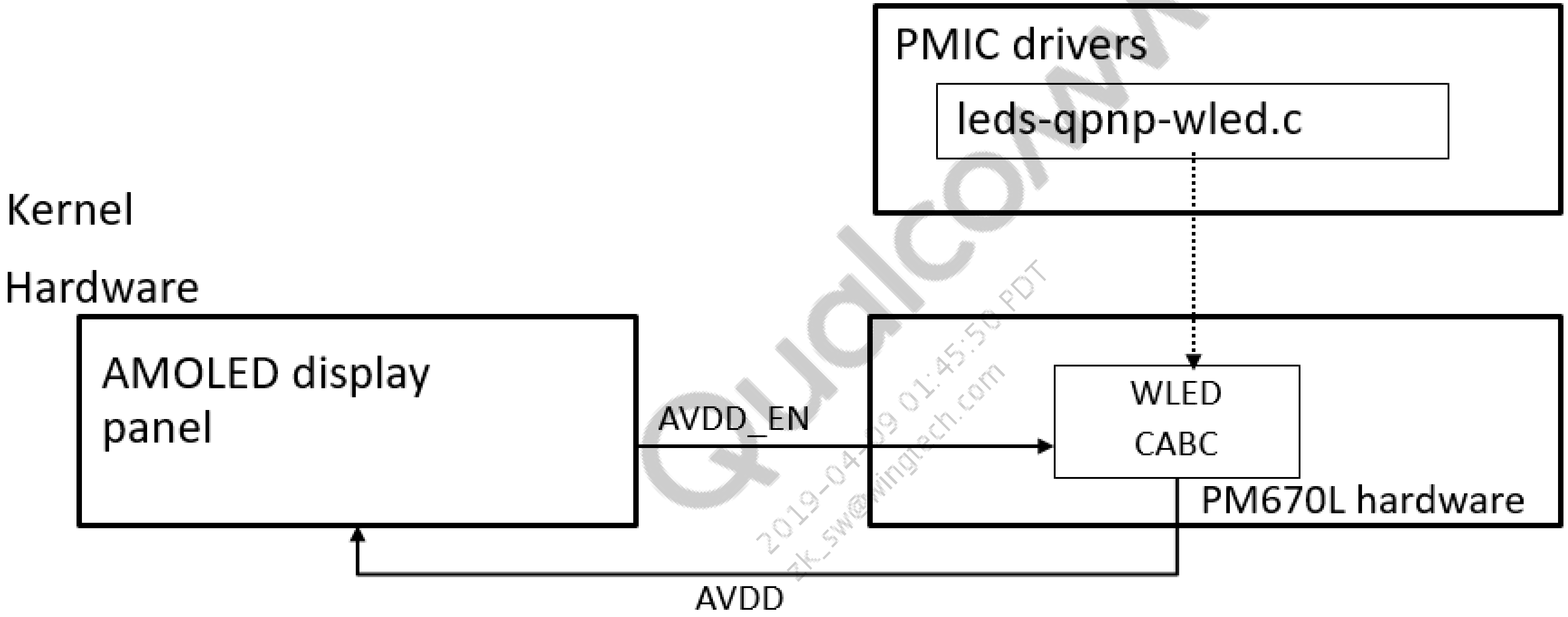
WLED Hardware Block Diagram



Overview

- Integrated boost SMPS generates the high voltage needed for WLED
- High-voltage requirement is eight LEDs in series, VREG_WLED is about +24.5 V (assume 3 V per LED and 0.5 V sink headroom)
- Four ground-referenced current sinks
  - Each supports a string of up to eight LEDs
  - Up to 30 mA each
  - Dedicated ground pin
- WLED CABC is supported
- Switching frequency for the WLED boost is configurable – 600 KHz, 800 KHz, or 1.6 MHz
- The recommended switching frequency for the WLED boost is 800 KHz

Software Block Diagram



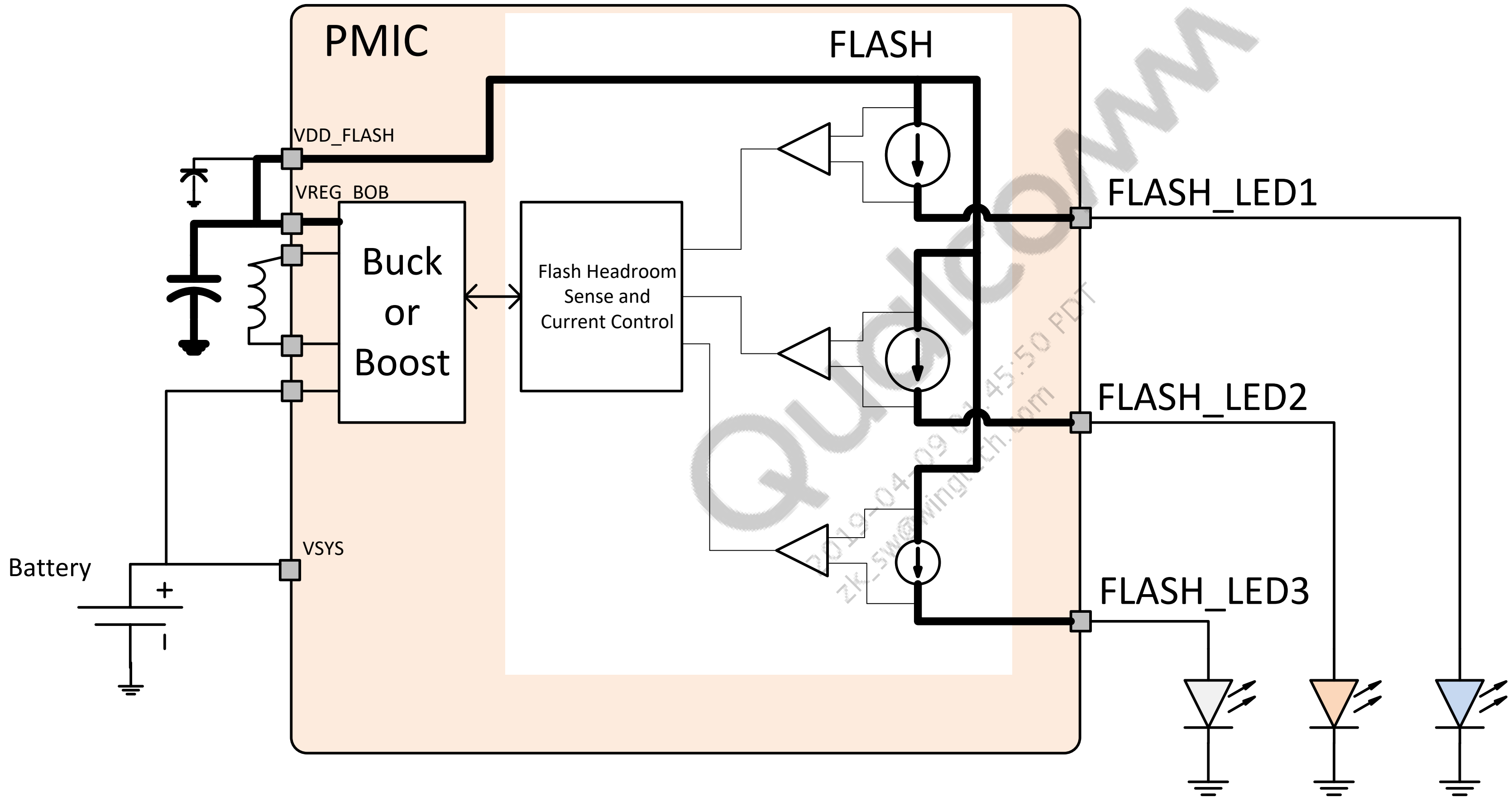
Software Support

- Software mostly performs one-time-setup configurations for WLED-Hardware controls WLED with AVDD_EN.

XBL	UEFI	HLOS
▪ Source –\boot_images\QcomPkg\Library\PmicLib\drivers\ibb\ boot_images\QcomPkg\Library\PmicLib\drivers\lab ▪ API –\boot_images\QcomPkg\Include\api\systemdrivers\pmic\ pm_lab.h\boot_images\QcomPkg\Include\api\systemdrivers\ pmic\pm_ibb.h	▪ Same as XBL ▪ Application files - \boot_images\QcomPkg\ Library\PmicLib\app\wled\src	▪ Source –kernel/drivers/regulator/qpnp-labibb-regulator.c ▪ DTSI documentation –kernel/Documentation/devicetree/ bindings/regulator/qpnp-labibb-regulator.txt ▪ DTSI files – kernel/arch/arm/boot/dts/Qcom/ pm670l.dtsi

Flash

Hardware Block Diagram



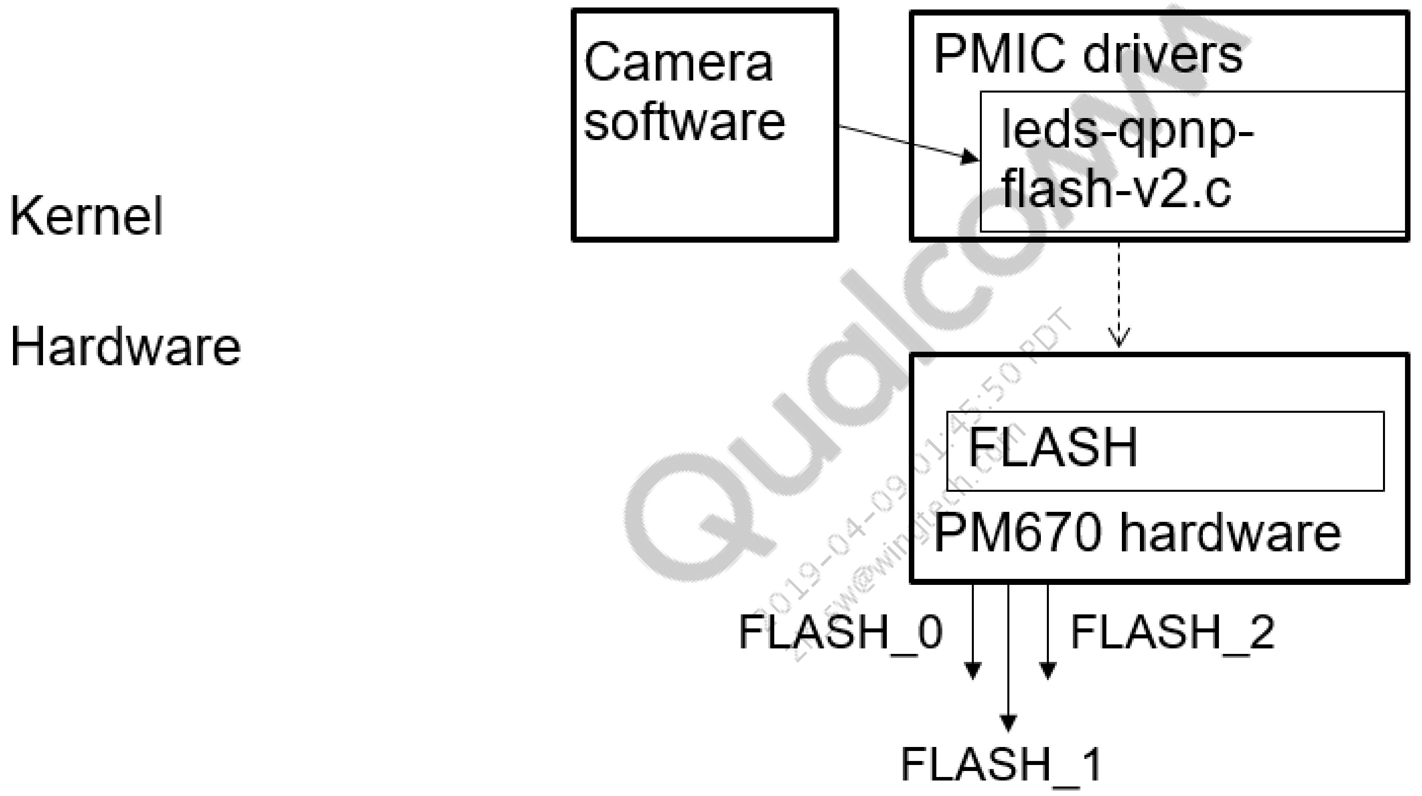
Overview

- Three channels – 2×1.5 A + 1×750 mA
- Independent current control
- 7-bit programmable current
- Configurable current resolution step size – 12.5 mA, 10 mA, 7.5 mA, and 5 mA
- Dynamic driver headroom tracking with PMIC buck-or-boost
- Mitigation features
  - Configurable thermal mitigation
  - Minimum VPH_PWR tracking mitigation
  - Peak buck-or-boost inductor current limit mitigation
  - Battery alarm mitigation
- Hardware or software strobing
  - Options for single or independent strobing of each channel

Overview (cont.)

- IR LED drive support with LPG PWM
- Tight hardware and software solution
  - Predictive maximum flash calculations based on battery
  - Pre-emptive system mitigation
  - Synchronization with camera shutter
- Others
  - Configurable Tx, GPIO mask input
  - Simultaneous charging and flash concurrency

Software Block Diagram

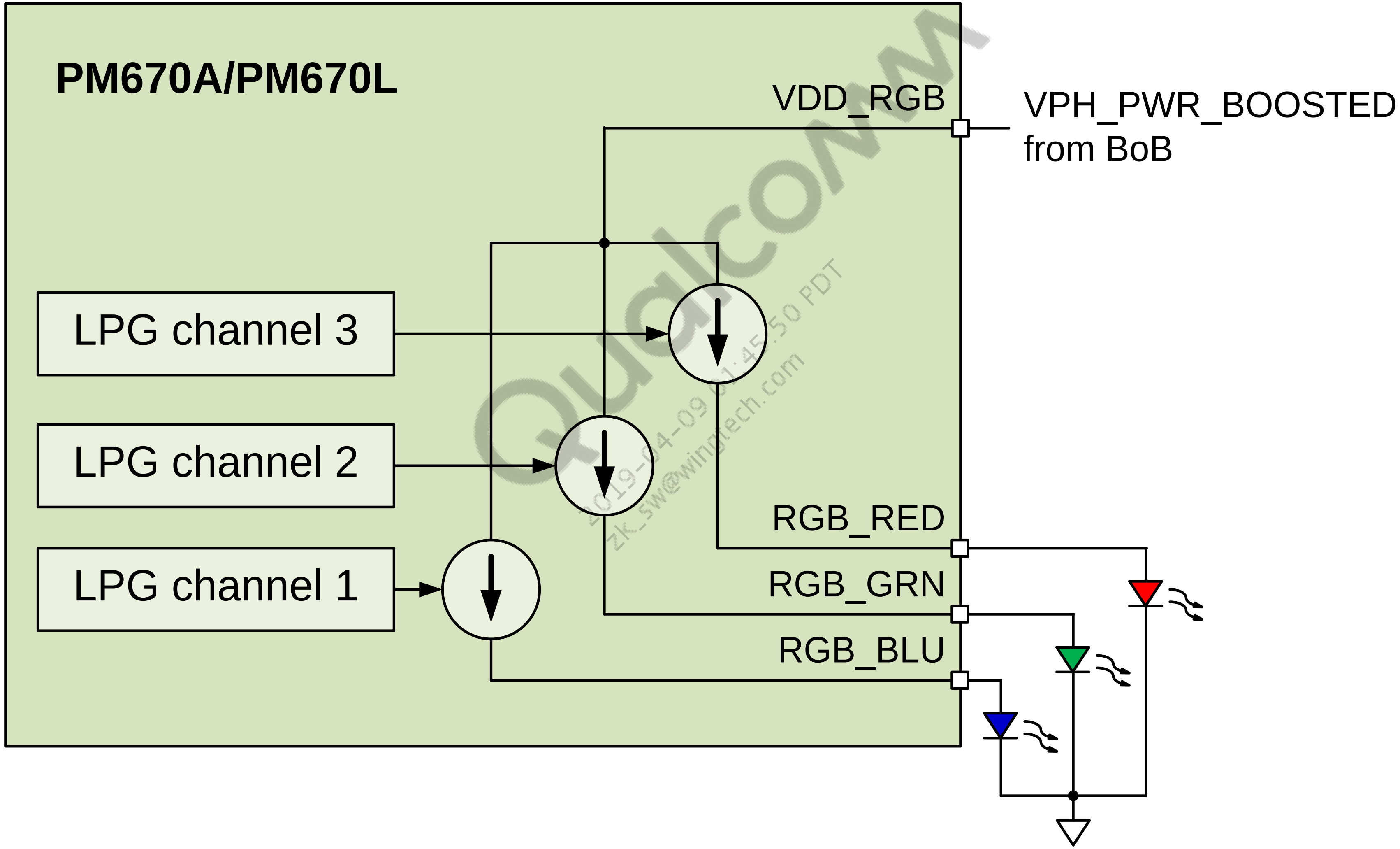


Software Support

XBL	UEFI	HLOS
N/A	N/A	▪ Source – kernel/drivers/leds/leds-qpnp-flash-v2.c ▪ DTSI documentation – kernel/Documentation/devicetree/bindings/leds/leds-qpnp-flash.txt ▪ DTSI files – kernel/arch/arm/boot/dts/Qcom/pm670l.dtsi

RGB LEDs

Hardware Block Diagram



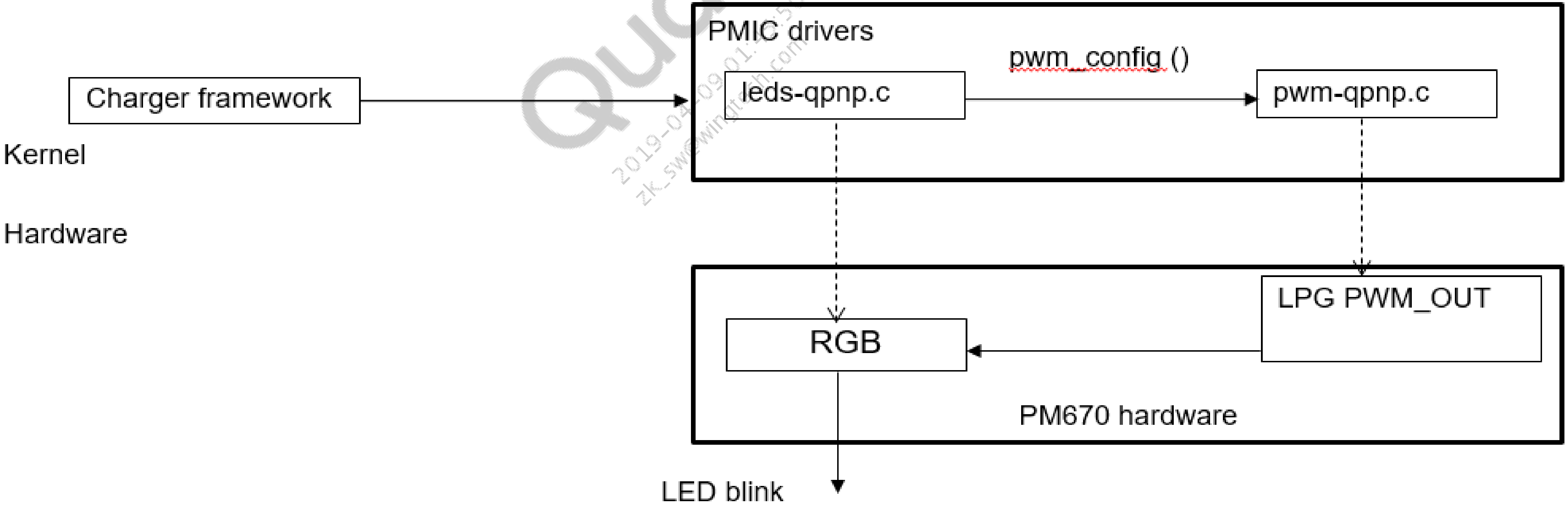
Overview

- Independent brightness control of the red, green, and blue channels
- Power source – External VDD_RGB (from VREG_BOB)
- 8 mA maximum per channel
- Independently programmable duty cycle and period through LPGs (6-bit or 9-bit resolution) for digital dimming
- Flash or blinking with register-selectable durations of on-time from 0 sec to 1 sec in ≤ 0.05 sec steps, and flashing periods from 0 sec to 12 sec in steps of ≤ 0.5 sec (or always on)
- ± 7% accuracy, 300 mV headroom

Software Support

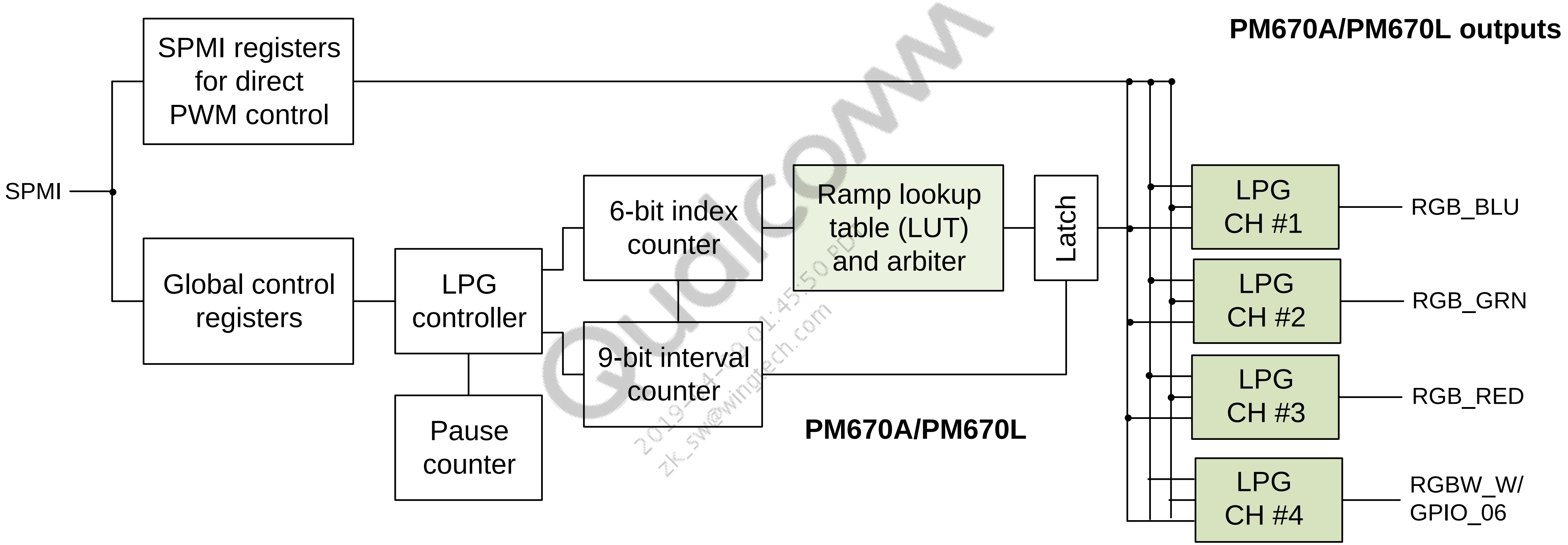
- Linux framework uses RGB LED as a charging indicator.

XBL	UEFI	HLOS
▪ Source – \boot_images\QcomPkg\Library\PmicLib\drivers\rgb ▪ API – \boot_images\QcomPkg\Include\api\systemdrivers\pmic\pm_rgb.h	▪ Same as XBL ▪ Application files –\boot_images\QcomPkg\Library\PmicLib\app\rgb\src	▪ Source – kernel/drivers/leds/leds-qpnp.c ▪ DTSI documentation – kernel/Documentation/devicetree/bindings/leds/leds-qpnp.txt ▪ DTSI files – kernel/arch/arm/boot/dts/Qcom/pm670l.dtsi



LPG

Hardware Block Diagram



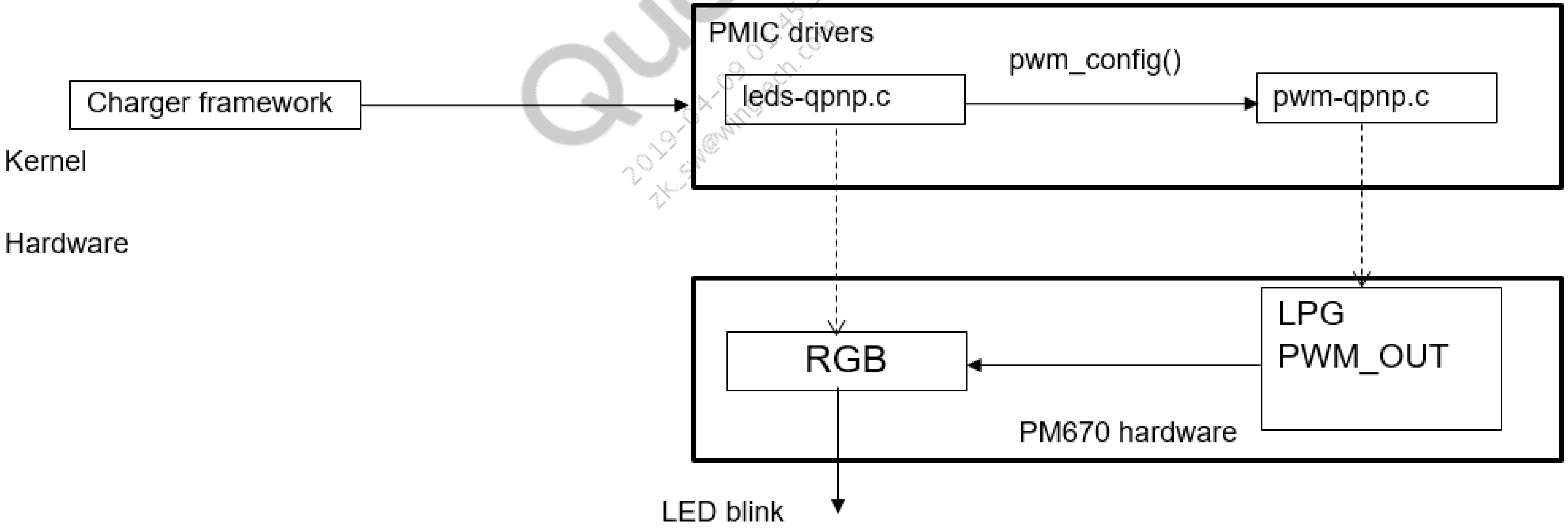
Overview

- LPG is a digital-only module that is used to generate patterns or PWM generation for LED drivers.
- PWM generation is straightforward and PWM frequency is selected based on the resolution, master clock frequency, and predivide options
- A LPG pattern consists of:
  a. Sequence of PWM values arranged in a LUT
  b. A timed pause at either the top or bottom of the sequence
  c. A single instance of the PWM sequence or in a loop
  d. Either repeat the sequence in the same order or reverse the order
  e. Any combination from a to d

Software Support

- LPG is used for MPP, GPIO, RGB LED, and haptics.

XBL	UEFI	HLOS
▪ Source – \boot_images\QcomPkg\Library\PmicLib\drivers\lpg ▪ API –\boot_images\QcomPkg\Include\api\systemdrivers\pmic\pm_lpg.h	Same as XBL	▪ Source – kernel/drivers/pwm/pwm-qpnp.c ▪ DTSI documentation – kernel/Documentation/devicetree/bindings/pwm/pwm-qpnp.txt ▪ DTSI files – kernel/arch/arm/boot/dts/Qcom/pm670l.dtsi



Debug

ADB

```
/sys/kernel/debug/regmap/spmi0-02 # echo 20 > count
/sys/kernel/debug/regmap/spmi0-02 # echo 0x1200 > address
/sys/kernel/debug/regmap/spmi0-02 # cat data
1200: 00
1201: 00
1202: 00
1203: 00
1204: 02
1205: 03
1206: 00
1207: 00
1208: 80
1209: 00
120a: 00
120b: 00
120c: 00
120d: 00
120e: 00
120f: 00
1210: 0c
1211: 6f
1212: 6f
1213: 6f
/sys/kernel/debug/regmap/spmi0-02 #
```

Note: The slave address is highlighted in the directory path. The dumps are single register per line with the address part being only the peripheral number and the register within the peripheral.

References

References

Documents	
Title	**Number**
Qualcomm Technologies, Inc.	
PM670 and PM670A/PM670L Power Management IC Design Guidelines/Training Slides	80-PD119-5A
Linux Android PMIC Charger Software User Guide	80-P2484-77

Acronyms	
Acronym or term	**Definition**
BIF	Battery interface
BCL	Battery current limiting
BLE	Bluetooth low energy
BSI	Battery serial interface
CABC	Content adaptive brightness
DFP	Downstream facing port
ERM	Eccentric rotating mass
IBB	Inverting buck-boost
LPG	Light pattern generator
LRA	Linear resonant actuator

References (cont.)

Acronyms	
Acronym or term	**Definition**
SCP	Short circuit protection
SoC	State-of-charge
UFP	Upstream facing port
WLED	White LED
XBL	eXtensible boot loader

Questions?

https://createpoint.qti.qualcomm.com

