Qualcomm Technologies, Inc.

Device description

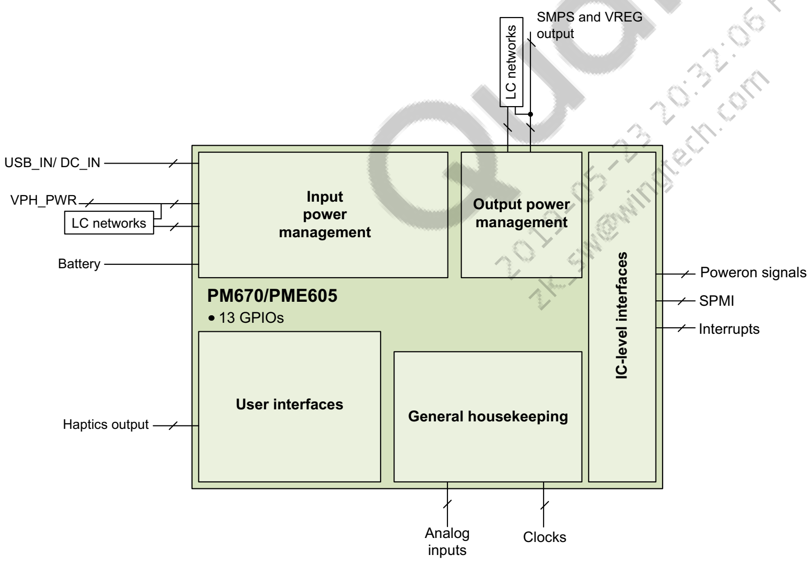
The PM670/PME605 device is part of the dual PMIC solution that integrates wireless product's power management, general housekeeping, user interface, and IC-level interface support functions.

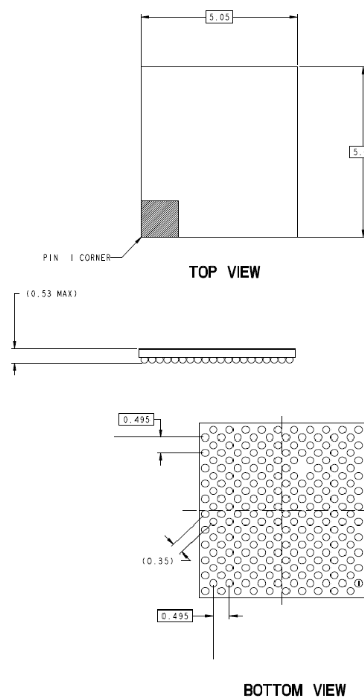
- Parallel charging using the SMB1355/SMB1390 companion IC
- USB Type-C support
- PBS 2.0 support
- System-clock and sleep-clock sources for entire chipset:
  - Two RF (low-noise) outputs
  - Three baseband (low-power) outputs
  - Sleep clock output
- System power management interface (SPMI) interface RCS support for interrupt communication

Key features (see Section 1.2 for details)

- Supports Qualcomm® Quick Charge™ 2.0, Quick Charge 3.0, and Quick Charge 4.0
- Switching charging with Quick Charge 3.0 and Quick Charge 4.0 supports up to 3 A
- Fuel gauge (FG) and housekeeping ADCs
- Six SMPS and 18 low-dropout (LDO) linear regulators
- 38.4 MHz XO controller and XO outputs
- Sleep clock and a real-time clock (RTC) with alarm
- SPMI
- Haptics
- 13 general-purpose input/output (GPIO) pins
- 219-pin wafer-level picoscale package (WLPSP)

PM670/PME605 high-level block diagram and 219 WLPSP package drawing





Contents

1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram

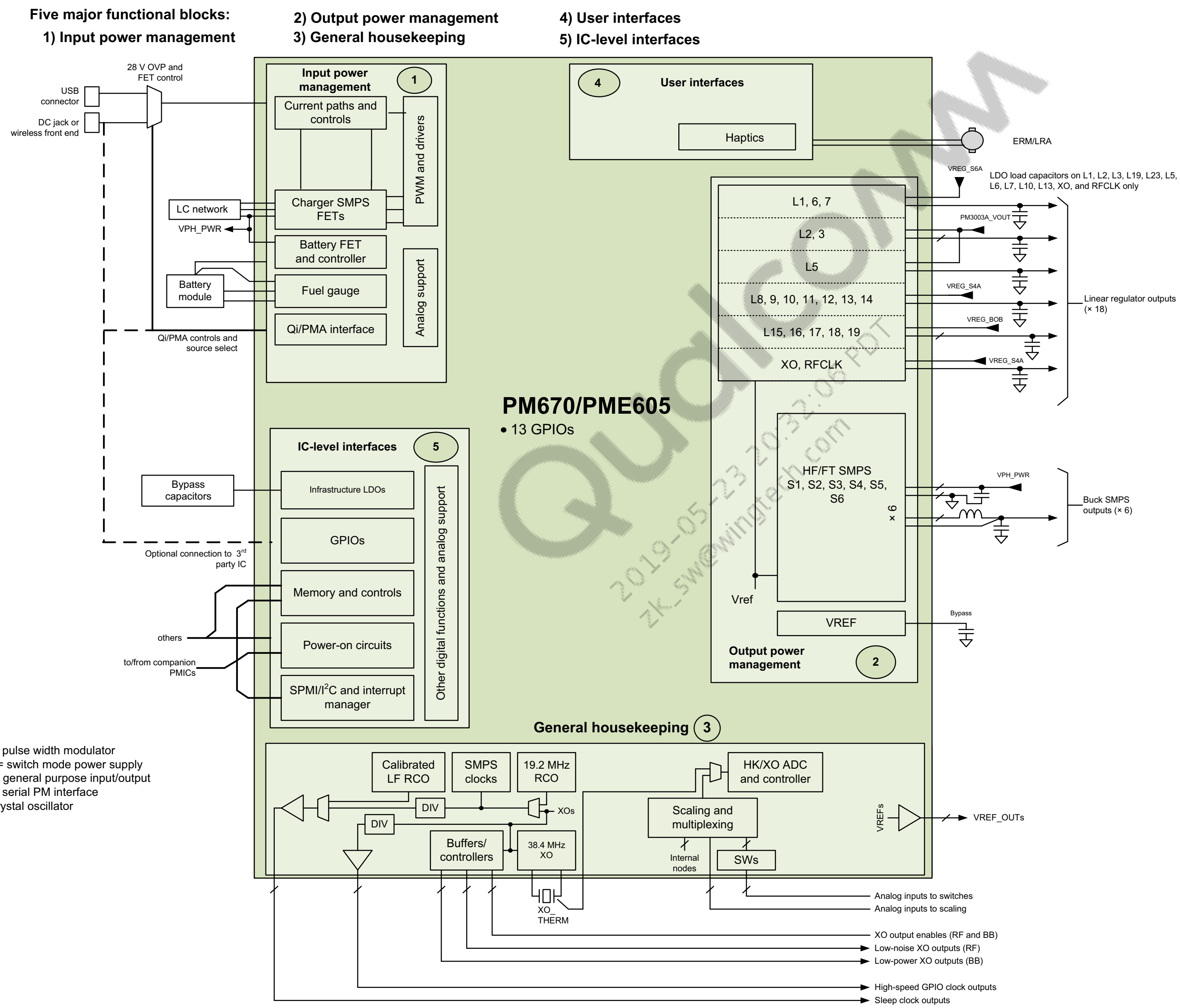


Figure 1-1 PM670/PME605 functional block diagram

1.2 PM670/PME605 features

NOTE: Some hardware features integrated within the PM670/PME605 must be enabled through the SDM IC software. See the latest version of the applicable software release notes to identify the enabled PMIC features.

Table 1-1 PM670/PME605 features

Feature	Capability
Input power management	
Battery charger	Switching charger (SCHG) – switched mode battery charger with reverse boost mode capability ■ Highly efficient (91% peak efficiency) power conversion eliminates heat issues ■ Supports Qualcomm Quick Charge 2.0, Quick Charge 3.0, and Quick Charge 4.0 for fast charging ■ Supports parallel charging using the SMB1355/SMB1390 companion IC for increased efficiency and lower power dissipation at higher charge currents ■ High charging current during Quick Charge 3.0 and Quick Charge 4.0 supports up to 3 A ■ Supports trickle charge, precharge, constant current charging, and constant voltage charging ■ Single input path with automatic and programmable input current limit for universal USB/AC/DC adapter compatibility ■ Automatic power source detection, prioritization, and programmable input current limiting in accordance with the USB 3.1, Type-C, and USB PD specification ■ Up to 750 mA charging output from a 500 mA USB port using TurboCharge™ mode ■ Differential battery voltage sense for decreased charge times ■ Input/output current path control allows system operation with a deeply discharged or missing battery ■ Intelligent Negotiation of Optimal Voltage (INOV) Gen 3 algorithm. Determines the minimum input voltage required to most efficiently charge the battery by dissipating the least amount of power using current and thermal (die/skin) sensors. ■ JEITA and JISC 8714 support ■ Real-time charge and discharge current measurement ■ 3.6 V to 10 V operating input voltage range (USB path) ■ 16 V (USB input) input voltage tolerance (nonoperating) with overvoltage protection (OVP) ■ USB On-The-Go (OTG) supports up to 1.5 A (USB OTG standard compliant and USB-IF ACA specification compliant) ■ Comprehensive protection features ■ Automatic input current limit (AICL) algorithms for wireless and USB charging ■ Hardware-controlled step charging algorithms
Wireless charging support	■ Supports Qi/PMA charging through the DC_IN path

Table 1-1 PM670/PME605 features (cont.)

Feature	Capability
Fuel gauge	■ Advanced mixed algorithm with current and voltage monitoring ■ Highly accurate battery state-of-charge estimation with aging and temperature correction ■ 16-bit dedicated current ADC (15 bits plus sign bit), ± 8.5 A range with internal sensing ■ 15-bit dedicated voltage ADC ■ 10-bit infrastructure ADC for measuring BATT_THERM, AUX_THERM, BATT_ID, USB input current, and voltage ■ Hardware autonomous operation, reporting of the state of charge without algorithms running on the modem device ■ Complete battery cycling not required to maintain accuracy ■ Battery capacity learning and online equivalent series resistance (ESR) tracking ■ Missing battery detection ■ Remote thermistor sensing ■ Battery current limiter (BCL) for platform concurrency management
Output voltage regulation	
Switched-mode power supplies [1] HF-SMPS FT-SMPS	 Three: one at 2 A, two at 3 A Three at 4 A each
LDO linear regulators [2]	18 total: NMOS at 1.2 A (two), 600 mA (four), PMOS at 600 mA (three), 300 mA (two), 150 mA (six), and 50 mA (one)
Pseudocapless LDO designs	10 of 12 LDOs
General housekeeping	
On-chip ADC	Shared housekeeping (HK) and XO support
Analog multiplexing for ADC HK inputs XO input	 Many internal nodes and external inputs Dedicated pin (XO_THERM)
Overtemperature protection	Multistage smart thermal control
38.4 MHz oscillator support	XO (with on-chip ADC)
XO controller and XO output	Five sets: three low-power baseband outputs and two low-noise RF outputs
Special purpose clock outputs	Sleep clock; 19.2, 9.6, 4.8, 2.4, and 1.2 MHz, including low-power mode 2.4 MHz for MP3 (div_clk), through GPIO
RTC	RTC clock circuits and alarms
Internal clocks	Derived from system 38.4 MHz XO
Programmable boot sequence	PBS 2.0 with one-time programmable (OTP) memory and RAM for power-on (PON), power-off (POFF), and reset sequences

Table 1-1 PM670/PME605 features (cont.)

Feature	Capability
User interfaces	
Haptics driver	One full H-bridge power stage for driving haptics ■ Bidirectional drive capability with support for active braking ■ Support for eccentric rotating machines (ERM)/linear resonant actuators (LRA) ■ Programmable PWM frequency from 25 kHz to 250 kHz, in 25 kHz steps ■ Programmable LRA frequency from 50 Hz to 300 Hz, with a 0.5 Hz tuning resolution ■ 6-bit control for output amplitude from 0 V to V_{max}, where V_{max} is configurable from 1.2 V to 3.6 V, in 100 mV steps for different LRAs ■ Support for internal 8-bit LUT to store haptics pattern, repeat, and loop ■ Dual PWM for double the effective switching frequency ■ Automatic resonance tracking ■ External input for audio/PWM mode support ■ Short circuit detection and current limit protection
IC-level interfaces	
Primary status and control	Two-line SPMI
Interrupt managers	Supported by SPMI
Power sequencing	Power on, power off, and soft resets
Battery UICC alarm (BUA)	BUA for effective shutdown to prevent corruption of UICC on a battery disconnection event
Configurable I/Os	
GPIO pins	■ 13 GPIO pins, configurable as digital inputs or outputs ■ Some GPIOs have primary/alternate functions for IC-level interfacing
Package	
Size	5.64 × 5.05 × 0.53 mm
Pin count and package type	219-pin WLPSP (0.35 mm pitch)

1. These are the maximum current ratings of the SMPS regulators. The actual current capability of the SMPS regulators may be less, depending on its configuration, inductor selection, and/or headroom. Overall, the current capability of an SMPS regulator is aligned with system needs based on the power grid.
2. These are the maximum current ratings of the LDO regulators. The actual current capability of the LDO regulators may be less, depending on its configuration and/or headroom. Overall, the current capability of an LDO regulator is aligned with system needs based on the power grid.

1.3 Comparison between PM670 and PME605

	PM670	PME605
Pairs with	SDM670, SDM710, QCS605, SXR1130	QCS603
PON sequence	Differs	
Regulator summary and usage	Differs	
Companion PMIC	PM670A/PM670L/PM3003A	PM8005
Valid configuration	PM670 + PM670A/L + 2x PM3003A, when paired with QCS605/SXR1130/ SDM670/SDM710	PME605 + PM8005 when paired with QCS603

2 Pin definitions

The PM670/PME605 is available in the 219 WLPSP – see Chapter 4 for package details. A high-level view of the pin assignments is shown in Figure 2-1.

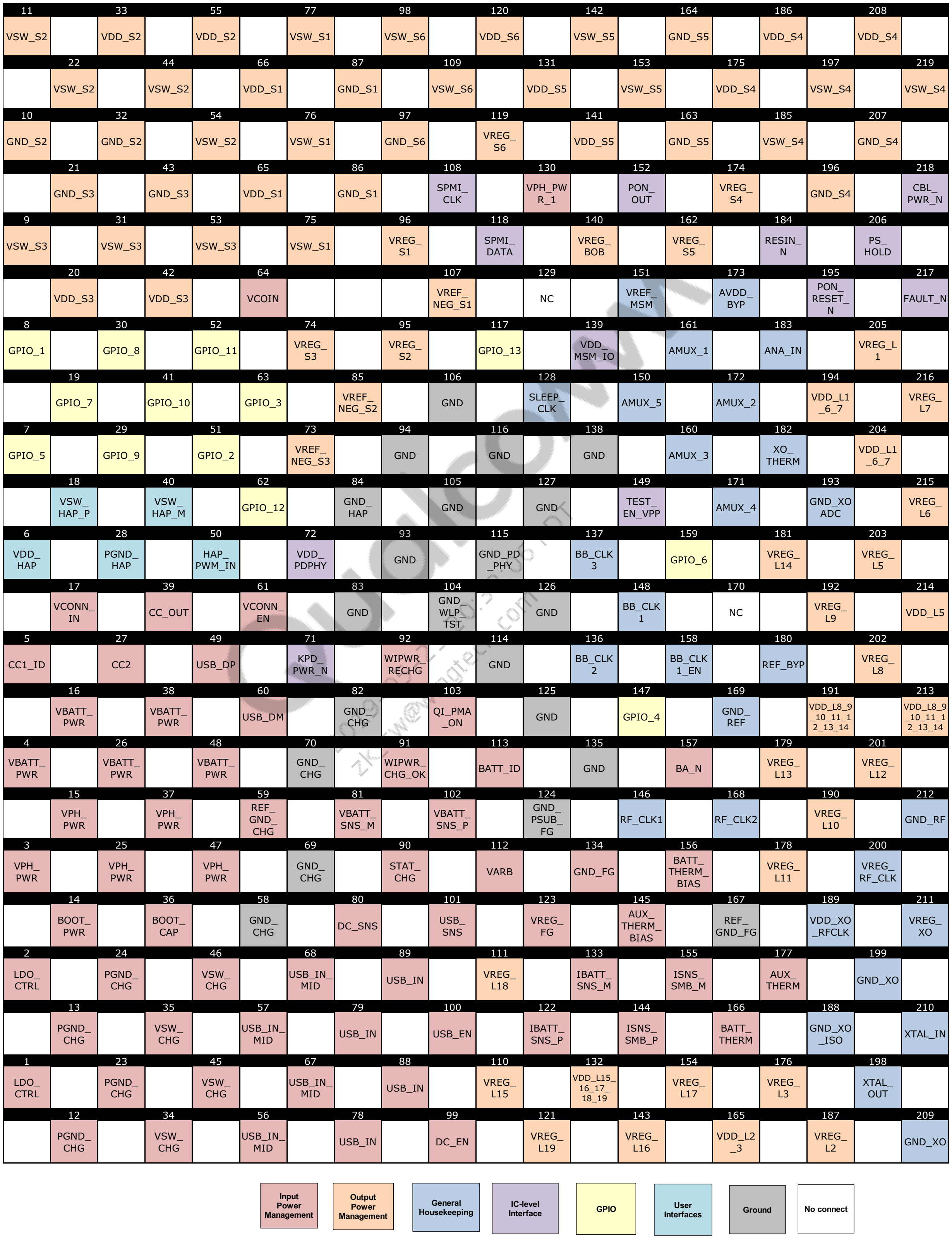


Figure 2-1 PM670/PME605 pin assignments (top view)

2.1 I/O parameter definitions

Table 2-1 I/O parameter (pad type) definitions

Symbol	Description
Pad attribute	
AI	Analog input
AO	Analog output
DI	Digital input (CMOS)
DO	Digital output (CMOS)
PI	Power input; a pin that handles 10 mA or more of current flow into the device
PO	Power output; a pin that handles 10 mA or more of current flow out of the device
Z	High-impedance (Hi-Z) output
MV	Medium voltage
LV	Low voltage
GNDP	Power ground; a pad that handles 10 mA or more of current flow returning to ground. Layout considerations must be made for these pads.
GNDC	Common ground; a pad that does not handle a significant amount of current flow, typically used for grounding digital circuits and substrates.
Pad voltage groupings	
V_INT	Internally generated supply voltage for some power-on circuits
V_PAD	Supply for modem IC interfaces; connected internally to VDD_MSM_IO
V_XBB	Supply for BB_CLKx output buffer; connected internally to VREG_BB_CLK
V_XRF	Supply for RF_CLKx output buffers; connected internally to VREG_RF_CLK
GPIO pin configurations	
When configured as inputs, GPIO pins have configurable pull settings.	
NP	No internal pull enabled
PU	Internal pull-up enabled
PD	Internal pull-down enabled
When configured as outputs, GPIO pins have configurable drive strengths that depend on the GPIO pad's supply voltage.	

2.2 Pin descriptions

Descriptions of all pins are presented in the following tables, organized by functional group:

Table 2-2	Input power management
Table 2-3	Output power management
Table 2-4	General housekeeping
Table 2-5	User interface
Table 2-6	IC-level interfaces
Table 2-7	General-purpose input/output
Table 2-8	No connection pins
Table 2-9	Power-supply pins
Table 2-10	Common ground pins

Table 2-2 Pin descriptions – input power management functions

Pad #	Pad name and/or function	Pad type [1]	Functional description
Charger/OTG interface			
78, 79, 88, 89	USB_IN	PI, PO	Input power from the selected source, or output during USB-OTG. This is a power entry node for the charger and connects to the OVP circuitry.
49	USB_DP	AI/AO	USB data plus for power source detection only; the modem IC handles data transactions.
60	USB_DM	AI/AO	USB data minus for power source detection only; data transactions are handled by the modem device.
SCHG			
36	BOOT_CAP	AO	Charger bootstrap node for bootstrapping the charger start-up bias network with input power before starting the SCHG
14	BOOT_PWR	AO	Auxiliary 4.4 V to 5 V LDO output – 50 mA (minimum) output supply. Also used to supply BOOT_CAP.
103	QI_PMA_ON	DI	Active-high input indicating when a Qi/PMA wireless input is connected
56, 57, 67, 68	USB_IN_MID	AO	Mid-FET capacitor node for accurate current level sensing through OVP FETs of USB_IN; called a mid-FET capacitor due to its placement between the OVP FET and the high-side switching FET.
4, 16, 26, 38, 48	VBATT_PWR	PI, PO	Battery voltage node, connects to BATFET. Output is for charging, and input is for all other operations.
102	VBATT_SNS_P	AI	Battery voltage sense input plus. Connect to the battery positive remote sense node, or connect this directly to the battery positive node.

Table 2-2 Pin descriptions – input power management functions (cont.)

Pad #	Pad name and/or function	Pad type [1]	Functional description
81	VBATT_SNS_M	AI	Battery voltage sense input minus. Connect to the battery negative remote sense node or connect this directly to the battery negative node.
3, 15, 25, 37, 47	VPH_PWR	PI, PO	Primary system supply node; SCHG regulated node
34, 35, 45, 46	VSW_CHG	PO	Charger SMPS switching node
12, 13, 23, 24	PGND_CHG	GNDP	Specific ground for the SCHG. Layout considerations must be made for this pad.
59	REF_GND_CHG	GNDP	Dedicated ground for the charger-specific master bandgap. Special considerations must be made to ensure that this ground is properly connected on the PCB.
61	VCONN_EN	DO	Digital output to toggle the external FET gate drive.
17	VCONN_IN	AI	An external 5 V supply is applied to this pin to support Type-C powered cables.
144	ISNS_SMB_P	AI	Current sense plus from the external parallel charger.
155	ISNS_SMB_M	AI	Current sense minus from the external parallel charger.
5	CC1_ID	AI	OTG mode enable or CC1 pin for the USB Type-C connector (user programmable). This requires IEC protection.
27	CC2	AI	CC2 pin for the USB Type-C connector. This requires IEC protection.
39	CC_OUT	AO	1.8 V push-pull tri-state output indicating CC1 or CC2 connection (orientation)
SCHG digital signals			
90	STAT_CHG	DO	Status/fault/interrupt indicator. Indicates charging, fault status, or enable for parallel charging. Multiplexed static (fault) or pulsed output (IRQ). Programmable polarity.
1, 2	LDO_CTRL	AO	No connect (NC)
Fuel gauge/battery interface			
133	IBATT_SNS_M	AI	Connect to VBATT_PWR
122	IBATT_SNS_P	AI	Connect to VBATT_PWR
123	VREG_FG	AO	Bypass capacitor for the internal fuel gauge LDO. It is only used by the fuel gauge and must not be used as a general LDO output.
112	VARB	AO	Internal LDO pin out for use with the fuel gauge only
134	GND_FG	GNDP	Analog ground for the fuel gauge. LDO bypass capacitors connect here.

Table 2-2 Pin descriptions – input power management functions (cont.)

Pad #	Pad name and/or function	Pad type [1]	Functional description
113	BATT_ID	AI	Battery ID input to the ADC and MIPI BIF interface. It can be used for missing battery detection.
166	BATT_THERM	AI	Battery temperature input to ADC for measuring the pack temperature. It is used for charger safe operation and BMS/FG.
156	BATT_THERM_BIAS	AO	Dedicated voltage source for BATT_THERM resistor network biasing.
177	AUX_THERM	AI	Temperature input to the ADC for the skin/remote thermistor.
145	AUX_THERM_BIAS	AO	Dedicated voltage source for AUX_THERM resistor network biasing.
157	BA_N	DO	Battery alarm open drain output. Part of the BCL system.
Wireless power interface			
91	WIPWR_CHG_OK	DO	Connect to GND
92	WIPWR_RECHG	DO	No connect
80	DC_SNS	AI	Voltage sense for DC_IN path
99	DC_EN	DO	Enable the DC_IN path from the external power multiplexer or external FET control
100	USB_EN	DO	Enable the USB path from the external 28 V OVP
101	USB_SNS	AI	USB input voltage sense pin from the external 28 V OVP
Input power sources			
130	VPH_PWR_1	PI	System input power node generated by either the charger or battery
Coin cell or keep-alive battery			
64	VCOIN	AI, AO	Coin-cell battery/capacitor or backup battery charger supply and input. Last remaining available source to maintain xVdd backed registers.

1. See Table 2-1 for pad voltage and type definitions.

Table 2-3 Pin descriptions – output power management functions

Pad #	Pad name and/or function	Pad type [1]	Functional description
High-frequency buck SMPS circuits			
185, 197, 219	VSW_S4	PO	S4 SMPS switch node

Table 2-3 Pin descriptions – output power management functions (cont.)

Pad #	Pad name and/or function	Pad type [1]	Functional description
174	VREG_S4	AI	S4 SMPS sense input
175, 186, 208	VDD_S4	PI	S4 SMPS supply power input
196, 207	GND_S4	GNDP	S4 SMPS power ground
142, 153	VSW_S5	PO	S5 SMPS switch node
162	VREG_S5	AI	S5 SMPS sense input
131, 141	VDD_S5	PI	S5 SMPS supply power input
163, 164	GND_S5	GNDP	S5 SMPS power ground
98, 109	VSW_S6	PO	S6 SMPS switch node
119	VREG_S6	AI	S6 SMPS sense input
120	VDD_S6	PI	S6 SMPS supply power input
97	GND_S6	GNDP	S6 SMPS power ground
Fast-transient buck SMPS circuits			
75, 76, 77	VSW_S1	PO	S1 SMPS switch node
96	VREG_S1	AI	S1 SMPS sense input
65, 66	VDD_S1	PI	S1 SMPS supply power input
86, 87	GND_S1	GNDP	S1 SMPS power ground
107	VREF_NEG_S1	AI	S1 SMPS ground sense; route as differential pair with VREG_S1.
11, 22, 44, 54	VSW_S2	PO	S2 SMPS switch node
95	VREG_S2	AI	S2 SMPS sense input
33, 55	VDD_S2	PI	S2 SMPS supply power input
10, 32	GND_S2	GNDP	S2 SMPS power ground
85	VREF_NEG_S2	AI	S2 SMPS ground sense; route as differential pair with VREG_S2.
9, 31, 53	VSW_S3	PO	S3 SMPS switch node
74	VREG_S3	AI	S3 SMPS sense input
20, 42	VDD_S3	PI	S3 SMPS supply power input
21, 43	GND_S3	GNDP	S3 SMPS power ground
73	VREF_NEG_S3	AI	S3 SMPS ground sense; route as differential pair with VREG_S3.
LDO circuits			
205	VREG_L1	PO	L1 LDO regulated output
187	VREG_L2	PO	L2 LDO regulated output
176	VREG_L3	PO	L3 LDO regulated output
203	VREG_L5	PO	L5 LDO regulated output
215	VREG_L6	PO	L6 LDO regulated output

Table 2-3 Pin descriptions – output power management functions (cont.)

Pad #	Pad name and/or function	Pad type [1]	Functional description
216	VREG_L7	PO	L7 LDO regulated output
202	VREG_L8	PO	L8 LDO regulated output
192	VREG_L9	PO	L9 LDO regulated output
190	VREG_L10	PO	L10 LDO regulated output
178	VREG_L11	PO	L11 LDO regulated output
201	VREG_L12	PO	L12 LDO regulated output
179	VREG_L13	PO	L13 LDO regulated output
181	VREG_L14	PO	L14 LDO regulated output
110	VREG_L15	PO	L15 LDO regulated output
143	VREG_L16	PO	L16 LDO regulated output
154	VREG_L17	PO	L17 LDO regulated output
111	VREG_L18	PO	L18 LDO regulated output
121	VREG_L19	PO	L19 LDO regulated output
132	VDD_L15_16_17_18_19	PI	Power supply for L15, L16, L17, L18, and L19 LDOs
165	VDD_L2_3	PI	Power supply for L2 and L3 LDOs
191, 213	VDD_L8_9_10_11_12_13_14	PI	Power supply for L8, L9, L10, L11, L12, L13, and L14 LDOs
194, 204	VDD_L1_6_7	PI	Power supply for L1, L6, and L7 LDOs
214	VDD_L5	PI	Power supply for L5 LDO
BOB circuits			
140	VREG_BOB	PI	Power supply from BOB

1. See Table 2-1 for pad voltage and type definitions.

Table 2-4 Pin descriptions – general housekeeping functions

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
HK/XO ADC and analog multiplexer circuits				
182	XO_THERM	–	AI	XO thermistor resistor divider input
161	AMUX_1	–	AI	Analog multiplexer (AMUX) input 13 connected to AMUX channel 51; typically used for MSM™ thermistor readings
172	AMUX_2	–	AI	AMUX input 2 connected to AMUX channel 14; typically used for UFS thermistor readings
160	AMUX_3	–	AI	AMUX input 3 connected with AMUX channel 15; typically used for PA thermistor 1 readings
171	AMUX_4	–	AI	AMUX input 4 connected with AMUX channel 16; typically used for PA thermistor 2 readings

Table 2-4 Pin descriptions – general housekeeping functions (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
150	AMUX_5	–	AI	AMUX input 5 connected with AMUX channel 17; typically used for quiet thermistor readings
193	GND_XOADC	–	GNDP	XO ADC reference ground, which should be routed as a thin trace to the XO ground island along with a connection to the main ground plane, where there are minimal temperature transients
183	ANA_IN	–	AI	PM670A/PM670L die temperature input
Sleep clock circuits				
128	SLEEP_CLK	V_PAD	DO	32 kHz sleep clock output to the modem IC
XO and clock buffer circuits				
210	XTAL_IN	–	AI	19.2/38.4 MHz XO input
198	XTAL_OUT	–	AO	19.2/38.4 MHz XO output
211	VREG_XO	–	AO	Linear regulator for XTAL circuits (internal use only)
199, 209	GND_XO	–	GNDP	Exclusive ground for XTAL circuits, which connects directly to the main ground plane through a single dedicated via; this ground pad should not be shared with any other ground pads.
146	RF_CLK1	V_XRF	DO	38.4 MHz RF (low-noise) XO clock buffer output (1 of 2)
168	RF_CLK2	V_XRF	DO	38.4 MHz RF (low-noise) XO clock buffer output (2 of 2)
200	VREG_RF_CLK	–	AO	Linear regulator for RF_CLK circuits (internal use only)
148	BB_CLK1	V_XBB	DO	19.2 MHz baseband (low-power) XO clock buffer output (1 of 3)
136	BB_CLK2	V_XBB	DO	19.2 MHz baseband (low-power) XO clock buffer output (2 of 3)
137	BB_CLK3	V_XBB	DO	19.2 MHz baseband (low-power) XO clock buffer output (3 of 3)
158	BB_CLK1_EN	V_PAD	DI	Hardware control enable for the BB_CLK1 buffer when this pad is driven high by the modem IC for the CXO
189	VDD_XO_RFCLK	–	PI	Power supply for XO and RF clock buffer LDOs, powered from the S4 SMPS.
212	GND_RF	–	GNDP	Exclusive ground for all clock buffers, which connects directly to the main ground plane through a single dedicated via; this ground pad should not be shared with any other ground pads.
188	GND_XO_ISO	–	GNDP	XO clock circuit ground for shielding; use a single via directly to the main ground plane; this ground pad should not be shared with any other ground pads.
PMIC power infrastructure				
173	AVDD_BYP	–	AO	Bypass capacitor connection for the internal aVdd regulator (1.875 V); used to power internal analog infrastructures.
180	REF_BYP	–	AO	Bypass capacitor for the dedicated master bandgap regulator; this reference must only be used for the master bandgap and must not be used as a general reference output.

Table 2-4 Pin descriptions – general housekeeping functions (cont.)

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
169	GND_REF	–	GNDP	Dedicated master bandgap ground reference connection; should be isolated from all other grounds – the pad should be connected directly to the main ground plane (with a via at the pin) and to the REF_BYP capacitor negative terminal.
Vref outputs				
151	VREF_MSM	–	AO	1.25 V reference for HV PADC on the modem IC
GPIOs can be configured for general housekeeping functions not listed here. [2]				

1. See Table 2-1 for pad voltage and type definitions.
2. Other housekeeping GPIO functions are possible. To assign a GPIO a particular function, identify all of the application's requirements and map each GPIO to its function, carefully avoiding assignment conflicts. All GPIOs are listed in Table 2-7.

Table 2-5 Pin descriptions – user interface functions

Pad #	Pad name	Pad type [2]	Functional description
Haptics			
18	VSW_HAP_P	AO	Haptics H-bridge driver output plus
40	VSW_HAP_M	AO	Haptics H-bridge driver output minus
50	HAP_PWM_IN	DI	PWM input for haptic control
6	VDD_HAP	PI	Haptics supply power input
28	PGND_HAP	GNDP	Haptics power ground
GPIOs may be configured for user interface functions. [1]			

1. GPIOs may be configured for user interface functions. To assign a GPIO a particular function, identify all of the application's requirements and map each GPIO to its function, carefully avoiding assignment conflicts. All GPIOs are listed in Table 2-7.
2. See Table 2-1 for parameter and acronym definitions.

Table 2-6 Pin descriptions – IC-level interface functions

Pad #	Pad name and/or function	Pad characteristics [1]		Functional description
		Voltage	Type	
IC-level interfacing power supply				
139	VDD_MSM_IO	–	PI	Input supply power for digital I/O signals to/from the modem device
Power-on, power-off, and reset control				
71	KPD_PWR_N	–	DI	Input pad generally connected to a keypad power-on button and when grounded; initiates the power-on sequence. Can also be configured for generating a Stage 2 and/or Stage 3 reset if held at a logic low for longer durations. Pulled up internally to 1.8 V via the dVdd regulator.
217	FAULT_N	–	DI, DO	PMIC fault signal (bidirectional) that initiates shutdown or S3 reset to all PMICs.
152	PON_OUT	–	DO	Output to control power-on, reset, and shutdown to other PMICs.
184	RESIN_N	–	DI	Input pad used for generating a Stage 2 and/or Stage 3 reset when held at a logic low.
195	PON_RESET_N	–	DO	Power-on reset output signal (active low), which is deasserted to take the modem device out of reset after the PMIC power-on sequence has completed, and is asserted when a reset or shutdown commences.
206	PS_HOLD	–	DI	Power supply hold control input. This signal's main purpose is to tell the master PMIC device to keep its power supplies on, and it can initiate a reset or power-down when asserted low; this signal comes from the modem device's PS_HOLD output.
218	CBL_PWR_N	–	DI	Alternate input pad, which can be used to initiate the power-on sequence when grounded; pulled up internally to 1.8 V via the dVdd regulator.
USB PD-PHY interface				
72	VDD_PDPHY		PI	Power input for the USB PD-PHY. Connects to the 3.075 V USB LDO on the core PMIC.
SPMI signals				
108	SPMI_CLK	V_PAD	DI	SPMI communication bus clock signal
118	SPMI_DATA	V_PAD	DI, DO	SPMI communication bus data signal
Miscellaneous IC functions				
149	TEST_EN_VPP	–	GNDC	Pin must be grounded externally
GPIOs can be configured for IC-level interface functions not listed here. [2]				

1. See Table 2-1 for pad voltage and type definitions.
2. Other IC-level interface GPIO functions are possible. To assign a GPIO a particular function, identify all of your application's requirements and map each GPIO to its function, carefully avoiding assignment conflicts. All GPIOs are listed in Table 2-7.

Table 2-7 Pin descriptions – general-purpose input/output functions

Pad #	Pad name	Configurable function	Pad type [1]	Functional description
Predefined GPIO functions – available only at the assigned GPIOs				
8	GPIO_1	OPT_1	MV	Configurable; default digital input with 10 μA pull-down. Optional hardware configuration control bit (1 of 2), depending on its voltage level (VDD/GND/Hi-Z); defines specific characteristics for the PMIC such as its power-on sequence.
51	GPIO_2	Spare	LV	Configurable; default digital input with 10 μA pull-down. GPIO_2 is configured as SLEEP_CLK out during PON.
63	GPIO_3	9.6MHZ_CLK	LV	Configurable; default digital input with 10 μA pull-down. WCD9340 clock (9.6 MHz)
147	GPIO_4	NFC_CLK_EN	MV	Configurable; default digital input with 10 μA pull-down. NFC clock enable
7	GPIO_5	WLANRF_VCTRL	LV	Configurable; default digital input with 10 μA pull-down. WCN WLAN RF voltage control
159	GPIO_6	Spare	LV	Configurable; default digital input with 10 μA pull-down.
19	GPIO_7	BUA	LV	Configurable; default digital input with 10 μA pull-down. BUA
30	GPIO_8	SLB	MV	Configurable; default digital input with 10 μA pull-down. SLB (used for power-on sequencing) PM670 GPIO_8 is connected to PM670A/PM670L GPIO_10 in the system.
29	GPIO_9	TYPEC_UUSB_SEL	MV	Configurable; default digital input with 10 μA pull-down. Used for Type-C and Micro USB select
41	GPIO_10	WCSS_VCTRL	LV	Configurable; default digital input with 30 μA pull-up. WCSS voltage control
52	GPIO_11	HOME_KEY	LV	Configurable; default digital input with 10 μA pull-down. Home key
62	GPIO_12	Spare	LV	Configurable; default digital input with 10 μA pull-down.
117	GPIO_13	Spare	LV	Configurable; default digital input with 10 μA pull-down.
Other available GPIO functions [2]				

1. See Table 2-1 for pad voltage and type definitions.
2. Each GPIO pair can be used as a level translator by using different rail voltages.

Fixed supply for GPIO_2, GPIO_3, GPIO_5, GPIO_6, GPIO_7, GPIO_10, GPIO_11, GPIO_12, and GPIO_13:

- 0 and 1 = VDD_MSM_IO (1.8 V)

For GPIO_1, GPIO_4, GPIO_8, and GPIO_9, options include the following:

- 0 = VPH_PWR (3.6 V nominal)
- 1 = VDD_MSM_IO (1.8 V)

Table 2-8 Pin descriptions – no connection pins

Pad #	Pad name	Functional description
129, 170	NC	No connect; not connected internally

Table 2-9 Pin descriptions – input DC power

Power inputs
Note: Power inputs are grouped with their respective modules. These can be found in the previous tables.

Table 2-10 Pin descriptions – common grounds

Pad #	Pad name	Pad type [1]	Functional description
Note: This table only includes common ground pins. Power ground pins are grouped with their respective modules and can be found in the previous tables.			
58, 69, 70, 82	GND_CHG	GNDC	SMBC controller ground
83, 93, 94, 105, 106, 114, 116, 125, 126, 127, 135, 138	GND	GNDC	Ground for all nonspecialized circuits
167	REF_GND_FG	GNDC	Reference ground for fuel gauge controller
124	GND_PSUB_FG	GNDC	FG substrate ground
84	GND_HAP	GNDC	Haptics controller ground
115	GND_PD_PHY	GNDC	Pull-down PHY ground
104	GND_WLP_TST	GNDC	Test pin; connect directly to ground

1. See Table 2-1 for pad voltage and type definitions.

3 Electrical specifications

3.1 Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Units
Input power management functions				
USB_IN, USB_SNS	Input power from USB source and USB input voltage sense [1]	-0.3	16	V
DC_SNS	Power from wireless front end or external DC voltage sense [1]	-0.3	16	V
USB_IN_MID	Input power from USB source (unprotected connection to USB_IN, not for general use) [1]	-0.3	16	V
VSW_CHG	Switching node of charger buck Steady state Transient (< 20 ns)	 -0.3 -2.5	 15.0 15.0	 V V
VBATT_PWR, VBATT_SNS_x	Main-battery voltage Steady state Transient (< 10 ms)	 -0.5 -0.5	 6 7	 V V
VPH_PWR	Handset power-supply voltage	-0.5	7	V
Power supply pads				
VDD_xx	PMIC power-supply voltages not listed elsewhere (steady state) Transient (< 10 ms)	-0.5 -0.5	6 7	V V
Signal pins				
V_IN	Voltage on any nonpower supply pin [2]	-0.5	$V_{xx} + 0.5$	V

1. Battery voltage of at least 2.5 V present on VBATT_PWR
2. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage and thermal conditions (Table 3-2). The PM670 meets all performance specifications listed in Section 3.3 through Section 3.10, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions

Parameter		Min	Typ	Max	Units
Input power management functions					
DC_SNS	Wireless power or DC input voltage sense	3.6	–	10	V
USB_SNS	USB input voltage sense	3.6	–	10	V
USB_IN	Input power from USB source	3.6	–	10	V
VPH_PWR	Handset power-supply voltage	2.8	3.8	4.75	V
VBATT_PWR, VBATT_SNS_x	Main battery voltage	2.8	3.8	4.75	V
Power supply pads					
VDD_MSM_IO	Pad voltage for digital I/Os to/from the IC	1.75	1.8	1.85	V
VDD_xx	All power supply pads not listed elsewhere [1]	2.8	3.8	4.75	V
VCOIN [2]	Coin-cell voltage	2.1	3.0	3.25	V
Signal pins					
V_IN	Voltage on any nonpower-supply pin [3]	0	–	V_{XX} + 0.5	V
Thermal conditions					
T_A	Ambient temperature	-30	25	85	°C
T_J	Junction temperature	-30	25	125	°C

1. Specified range accommodates low-voltage lithium batteries on the low end, and high-voltage lithium batteries on the high end.
2. The VCOIN feature is supported from PM670 Rev. 2.0 CS onwards. See Issue 4-4, *VCOIN feature may prevent phones from powering on* of the *PM670 Device Revision Guide* (80-PD119-4) for more information.
3. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.3 DC power consumption

This section specifies DC power supply currents for the various IC operating modes (Table 3-3). Typical currents are based on IC operation at room temperature (+25°C) using default settings.

Table 3-3 DC power supply currents

Parameter		Comments	Min	Typ	Max	Units
I_ACTIVE	Supply current, active mode [1]		–	4.3	–	mA
I_SLEEP	Supply current, sleep mode [2]		–	490	–	μA
I_OFF	Supply current, off mode [3]		–	38	80	μA
I_SHIP	Supply current, ship mode [4]		–	14	37	μA
I_USB	USB charger current in suspend mode [5]		–	0.8	1.4	mA
I_COIN	Coin-cell supply current, off mode [6]	Average current				
	XTAL off		–	8	19	μA
	RC calibration		–	9	20	μA

1. I_ACTIVE is the total supply current from the battery with the PMIC on after its primary power-on sequence. In this state, the charger module is enabled, the crystal oscillator is on, the fuel gauge module is enabled, the temperature alarm is active, the internal infrastructure is enabled, BCL, and the following voltage regulators and signals are enabled: S1A, S2A-S3A, S4A, S5A, L1A, L3A, L6A, L8A, L9A, L10A, L11A, L13A, L14A, L19A, and VREF_MSM. All enabled SMPS regulators mentioned are also in auto mode.
2. I_SLEEP is the total supply current from the main battery with the PMIC on, the XO oscillator on, internal infrastructure enabled, and the following voltage regulators on with no load and low-power mode enabled: S4A, S5A, L5A, and L13A.
3. I_OFF is the total supply current from the battery with PM670 off. This only applies when the temperature is between -30°C and +60°C.
4. I_SHIP is the total supply current from the battery with PM670 in ship mode. This only applies when the temperature is between -30°C and +60°C.
5. I_USB is the total supply current from a USB charger when the phone has a good battery (VBATT_PWR > 3.2 V and not being charged). During USB suspend, current from a PC is limited to 2.5 mA. The specified I_USB value allows 1.1 mA for external components connected to VBUS during suspend.
6. I_COIN is the total supply current from a 3.0 V coin cell with the PMIC off and the following conditions:
   – 32 kHz crystal oscillator off (applies from -30°C to +85°C).
   – 32 kHz crystal oscillator off and RC calibration enabled with nominal settings (applies from -30°C to +85°C, and does not include the peak currents when RC calibration is performed).

3.4 Digital logic characteristics

The charger has unique digital signaling characteristics as listed within Section 3.5.3; all other PM670/PME605 digital I/O characteristics are specified in Table 3-4.

Table 3-4 Digital I/O characteristics

Parameter		Comments [1]	Min	Typ	Max	Units
V_{IH}	High-level input voltage		0.65 × V_{IO}	–	V_{IO} + 0.3	V
V_{IL}	Low-level input voltage		-0.3	–	0.35 × V_{IO}	V
V_{SHYS}	Schmitt hysteresis voltage		15	–	–	mV
I_L	Input leakage current [2]	V_{IO} = max, V_{IN} = 0 V to V_{IO}	-0.2	–	0.2	µA
V_{OH}	High-level output voltage	$I_{out} = I_{OH}$	V_{IO} - 0.45	–	V_{IO}	V
V_{OL}	Low-level output voltage	$I_{out} = I_{OL}$	0	–	0.45	V
I_{OH}	High-level output current [3]	$V_{out} = V_{OH}$	3	–	–	mA
I_{OL}	Low-level output current [3]	$V_{out} = V_{OL}$	–	–	-3	mA
I_{OH_XO}	High-level output current	XO digital clock outputs only	6	–	–	mA
I_{OL_XO}	Low-level output current	XO digital clock outputs only	–	–	-6	mA
C_{IN}	Input capacitance [4]		–	–	5	pF

1. V_{IO} is the supply voltage for the modem IC/PMIC interface (most PMIC digital I/Os).
2. GPIO pins comply with the input leakage specification only when configured as a digital input or set to the tri-state mode.
3. Output current specifications apply to all digital outputs unless specified otherwise, and are superseded by specifications for specific pins (such as GPIO pins).
4. Input capacitance is guaranteed by design but is not 100% tested.

3.5 Input power management

Input power management performance specifications are split into two functional categories as defined within its block diagram (Figure 3-1).

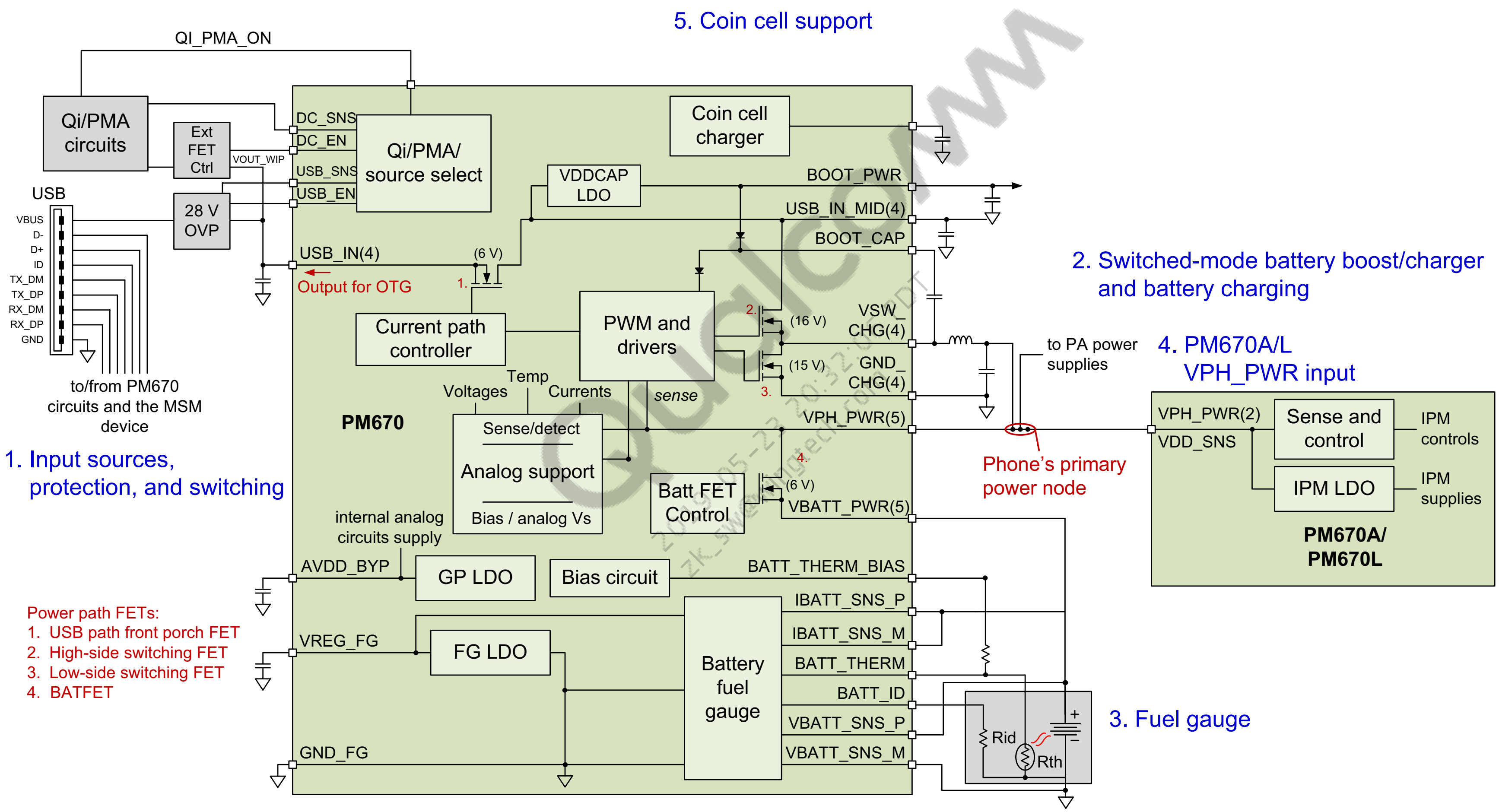


Figure 3-1 PM670 input power management functional block diagram

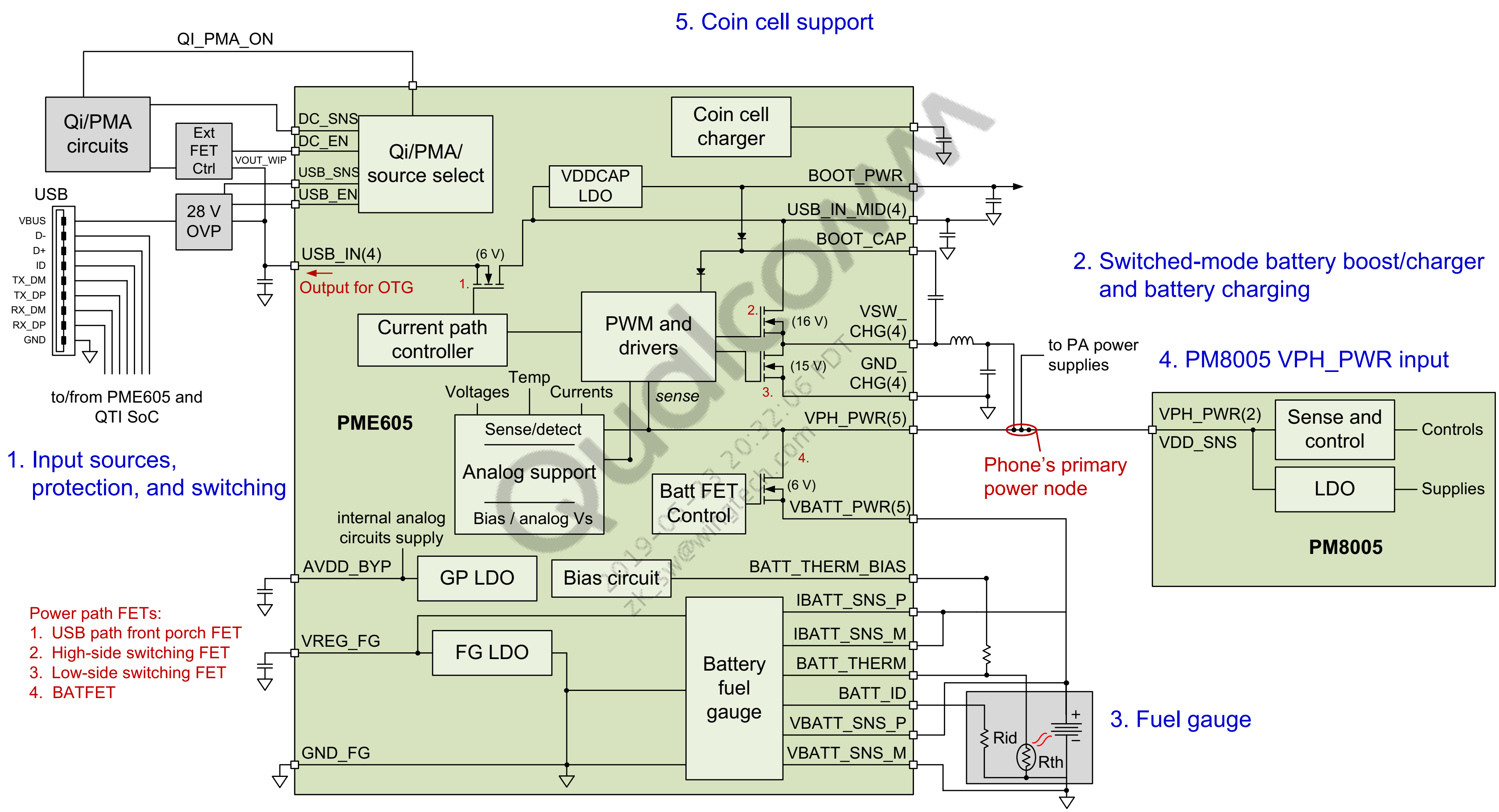


Figure 3-2 PME605 input power management functional block diagram

3.5.1 Coin-cell charging

Coin-cell charging is enabled through software control and powered from VBAT. The on-chip charger is implemented using a programmable voltage source and a programmable series resistor. The modem IC reads the coin-cell voltage through the PMIC's analog multiplexer to monitor charging. Coin-cell charging performance is specified in Table 3-5.

Table 3-5 Coin-cell charging performance specifications

Parameter	Comments	Min	Typ	Max	Units
Target regulator voltage [1]	V_{in} > 3.3 V, I_{CHG} = 100 µA	2.5	–	3.2	V
Target series resistance [2]		800	–	2100	Ω
Coin-cell charger voltage error	I_{CHG} = 0 µA	-5	–	5	%
Coin-cell charger resistor error		-20	–	20	%
Dropout voltage [3]	I_{CHG} = 2 mA	–	–	200	mV
Ground current, charger enabled	PMIC = off; VCOIN = open				
VBAT = 3.6 V, T = 27ºC		–	4.5	–	µA
VBAT = 2.5–5.5 V		–	–	8	µA

1. Valid regulator voltage settings are 2.5, 3.0, 3.1, and 3.2 V.
2. Valid series resistor settings are 800, 1200, 1700, and 2100 Ω.
3. Set the input voltage (VBAT) to 3.5 V. Note the charger output voltage; call this value V_0. Decrease the input voltage until the regulated output voltage (V_1) drops 100 mV ($V_1 = V_0 - 0.1$ V). The voltage drop across the regulator under this condition is the dropout voltage ($V_{dropout}$ = VBAT - V_1).

Table 3-6 Qualified coin-cell/super capacitor specifications [1]

Parameter	Comments	Min	Typ	Max	Units
Operating temperature		-30	25	60	°C
Storage range		-30	–	85	°C
Rated voltage		3.1	3.2	3.3	V
Effective series resistance (ESR) [2]		–	–	2000	Ω
Effective capacitance of super capacitor [3]	0.5 hour runtime	12	–	–	mF
	1 hour runtime	24	–	–	mF

1. 47 µF on VCOIN must be used to support the 2 sec SMPL timer.
2. Effective series resistance (ESR) is the worst-case ESR of the unit tested at the worst-case temperature after four years of typical usage. A typical use case is a unit biased constantly with 3.2 V DC voltage at 25°C.
3. With shorter run time expectancy, the effective capacitance requirement can be scaled.

3.5.2 Battery charger

The PM670/PME605 features a fully programmable switched-mode Li-ion battery charger, input power, and output power controller for portable devices. The device is designed to be used in conjunction with systems using single-cell Li-ion and Li-polymer battery packs. The PM670 provides three major functions to the end-system: input selection and arbitration, system output supply and control, and battery charging. The device is fully programmable via the SPMI interface.

DC operating characteristics (unless otherwise noted)

All voltages are relative to ground.

- T_A = -30°C to +85°C
- V_{USB_IN} = +5.0 V, +9.0 V
- V_{FLT} = 4.4
- V_{BATT} = 3.9
- F_{SW} = 1.05 MHz

Table 3-7 Battery charger specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input-power source control and protection						
V_{USB_SNS}	USB_IN voltage	UVLO is defined as the higher of V_{UVLO} or battery voltage + V_{ASHDN}	3.6	–	10	V
V_{DC_SNS}	DC_SNS input voltage	UVLO is defined as the higher of V_{UVLO} or battery voltage + V_{ASHDN}	3.6	–	10	V
V_{ASHDN}	Autoshutdown lockout	V_{IN} minus (-) V_{SYS}, V_{IN} falling	70	130	190	mV
		Hysteresis	–	80	–	mV
		Glitch filter time, rising and falling	–	20	–	ms
V_{UNPLUG}	Input coarse detection threshold	V_{IN} falling	–	1	–	V
		Glitch filter time, rising and falling	–	10	–	µs
V_{UVLO}	Input undervoltage lockout	V_{USB_IN} falling, 5 V only, 5 V to 9 V, or continuous	3.5	3.6	3.7	V
		V_{USB_IN} falling, 9 V	6.9	7.2	7.5	V
		Hysteresis	–	0.2	–	V
		V_{USB_IN} glitch filter time, rising and falling	–	20	–	ms

Table 3-7 Battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OVLO}	Input overvoltage lockout	V_{USB_IN} rising, 5 V only	6.2	6.4	6.5	V
		V_{USB_IN} rising, 9 V only, or 5 V to 9 V	10	10.3	10.6	V
		Hysteresis	–	0.2	–	V
		Response time, V_{IN} rising, all ranges	–	10	–	ms
		Glitch filter time, V_{IN} falling	–	100	–	ms
$I_{PULL\_DOWN\_OV}$	USB_IN pull-down current source strength	USB_IN overvoltage	–	10	–	mA
$I_{PULL\_DOWN\_UV}$	USB_IN and USB_IN_MID pull-down current source strength	USB_IN undervoltage	–	20	–	mA
$I_{USB\_IN\text{-}SUSP}$	USB_IN suspend mode current	USB_IN power path in suspend mode, $V_{UVLO} < V_{USB\_IN} < V_{OVLO}$	–	0.8	1.4	mA
$I_{LIM\text{-}USB\_IN\_ACC}$	USB_IN maximum input current limit [1]	USB 2.0 option: 500 mA mode, T = 0°C to +70°C (475 mA setting)	451	475	500	mA
		USB 2.0 option: 100 mA mode, T = 0°C to +70°C (75 mA setting)	50	75	100	mA
		USB 3.0 option: 900 mA mode, T = 0°C to +70°C (850 mA setting)	807	850	900	mA
		USB 3.0 option: 150 mA mode, T = 0°C to +70°C (125 mA setting)	100	125	150	mA
		Type-C medium-current mode, T = 0°C to +70°C (1425 mA setting)	1353	1425	1500	mA
		Type-C high-current mode, T = 0°C to +70°C (2850 mA setting) USB_SNS = 5.0 V	2707	2850	3000	mA
		USB high-current mode (programmable 0 mA to 5000 mA, in 25 mA steps), $I_{LIM\text{-}USB\_IN} \geq$ 500 mA, T = 0°C to +70°C, USB_IN = 5 V	0.90 × $I_{LIM\text{-}USB\_IN}$	0.95 × $I_{LIM\text{-}USB\_IN}$	$I_{LIM\text{-}USB\_IN}$	mA

Table 3-7 Battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Automatic input current limiting (AICL)						
V_{AICL_RANGE}	AICL voltage-collapse threshold range	Programmable (44 settings with 100 mV steps from 4 V to 5.6 V, and 200 mV steps from 5.6 V to 8.6 V)	4	–	8.6	V
$V_{AICL\_5V\_RANGE}$	5 V AICL voltage-collapse threshold range	Programmable (eight settings with 100 mV steps)	4	–	4.7	V
$V_{AICL\_9V\_RANGE}$	9 V AICL voltage-collapse threshold range	Programmable (eight settings with 200 mV steps)	7.2	–	8.6	V
V_{AICL_HYST}	AICL voltage-collapse threshold hysteresis	Hysteresis	–	0.2	–	V
V_{AICL_GF}	AICL voltage-collapse threshold deglitch time	Glitch filter time, rising and falling (option 3)	–	5	–	ms
V_{CL_ACC}	AICL voltage-collapse threshold accuracy		-3.5	–	3.5	%
$t_{AICL\text{-}RERUN}$	AICL automatic rerun timer	Four programmable settings (0.2 sec, 0.4 sec, 0.8 sec, and 1.6 sec)	-15	–	15	%
$t_{AICL\text{-}STEP}$	AICL discrete method step duration	AICL discrete method selected and input current rising, or AICL ADC disabled and input current falling	–	10	–	ms
Automatic power source detection (APSD) for BC 1.2						
V_{DP_SRC}	D+ source voltage	$I_{DP\_SRC} \leq 250\ \mu A$	0.6	0.65	0.7	V
V_{DAT_REF}	Data detect voltage		0.25	0.325	0.4	V
V_{DP_UP}	D+ pull-up voltage		3	–	3.6	V
I_{DM_SINK}	D- sink current		25	50	75	μA
I_{DP_SRC}	Data contact detect current source		7	–	10	μA
$t_{DP\_SRC\_ON}$	D+ source on time		100	–	–	ms
$t_{DCD\_TIMEOUT}$	DCD timeout	Option 1	321	328	335	ms
		Option 2	642	656	670	ms
$t_{ENUM\_TIMEOUT}$	SDP enumeration timeout		–	–	2	min
t_{DPSRC_HICRNT}	D+ source off to high current		40	–	–	ms
t_{DPSRC_CON}	D+ source off to connect		40	–	–	ms
$t_{CHGR\_DET\_DBNC}$	Charger detect debounce		10	–	–	ms

Table 3-7 Battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{DP/DM}$	D+/D- capacitance	D+/D- Hi-Z	–	4	–	pF
R_{ID_GND}	ID resistance ground detection	Micro-USB mode	–	–	1.3	kΩ
R_{ID_FLOAT}	ID resistance float detection	V_{USB_IN} absent, only battery present, micro-USB mode	210	–	–	kΩ
		V_{USB_IN} present, micro-USB mode	210	–	238	kΩ
		V_{USB_IN} present, micro-USB mode	777	–	–	kΩ
USB Type-C interface and detection						
CC_{CAP}	Maximum CC pin capacitance		–	–	600	pF
$DFP_{I\_SRC\_STDUSB}$	Standard USB current source	In DFP mode	64	80	96	µA
$DFP_{I\_SRC\_STDUSB}$	Medium-current USB current source	In DFP mode	166	180	194	µA
$R_{CC\_FMB\_1}$	USB Type-C factory-mode boot resistance 1	V_{USB_IN} present, Type-C mode, UFP mode	–	255	–	kΩ
$R_{CC\_FMB\_2}$	USB Type-C factory-mode boot resistance 2	V_{USB_IN} present, Type-C mode, UFP mode	–	301	–	kΩ
$R_{CC\_FMB\_3}$	USB Type-C factory-mode boot resistance 3	V_{USB_IN} present, Type-C mode, UFP mode	–	532	–	kΩ
$R_{CC\_FMB\_4}$	USB Type-C factory-mode boot resistance 4	V_{USB_IN} present, Type-C mode, UFP mode	–	619	–	kΩ
Z_{OPEN}	Minimum open-circuit CC impedance to ground		126	–	242	kΩ
R_d	R_d pull-down resistor to ground	In UFP mode	4.59	5.1	5.61	kΩ
R_a	R_a pull-down resistor to ground	Audio adapter or powered cable attached	800	–	1200	Ω
V_{CLAMP}	CC UFP mode clamping threshold	Power-off, $V_{BATT} < V_{UVLO}$ or battery missing	–	1.1	–	V
V_{CLAMP_HV}	CC pin always enabled high-voltage clamp	$V_{BATT} \geq 3.5$ V	–	3.5	–	V
V_{CLAMP_HV}	CC pin always enabled high-voltage clamp	$V_{BATT} < 3.5$ V	–	V_{BATT}	–	V

Table 3-7 Battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC_SINK}	Voltage on CC pins when PMIC is in sink role (initially UFP)	V_{Ra} detected	0.025	–	0.25	V
		V_{Rd} - connect detected	0.25	–	2.04	V
		V_{Rd} - USB detected	0.25	–	0.61	V
		V_{Rd} - 1.5 A detected	0.7	–	1.16	V
		V_{Rd} - 3.0 A detected	1.31	–	2.04	V
$VCC_{SOURCE\_DEFAULT\_USB}$	Voltage on CC pins when PMIC is in source role (initially UFP) and advertising default USB current	V_{Ra} (powered cable/adapter) detected	0	–	0.15	V
		V_{Rd} (sink) detected	0.25	–	1.5	V
		No connect (V_{OPEN})	1.65	–	–	V
$VCC_{SOURCE\_1.5}$	Voltage on CC pins when PMIC is in source role (initially UFP) and advertising 1.5 A Type-C current	V_{Ra} (powered cable/adapter) detected	0	–	0.35	V
		V_{Rd} (sink) detected	0.45	–	1.5	V
		No connect (V_{OPEN})	1.65	–	–	V
$tCC_{DEBOUNCE}$	Time a port waits before it can determine it is attached	Transitioning between the attached wait state and the attached source or attached sink states	–	120	–	ms
$tPD_{DEBOUNCE}$	Time a port waits before it can determine it is either detached or there has been a change in the Type-C current advertisement	Transitioning between the attached wait state and the attached source or attached sink states	–	12	–	ms
VCONN	VCONN voltage range	VCONN enabled	3.0	–	5.5	V
I_{LIM_VCONN}	VCONN current limit	VCONN enabled and powered from 4.75 V - 5.5 V supply, maximum output power $\geq$ 1.67 W VCONN enabled and powered from 3.0 V - 5.5 V supply, maximum output power $\geq$ 1.0 W	333	375	464	mA
$t_{VCONN\_DISCHARGE}$	Maximum time from when cable is detached until $V_{VCONN\_Discharge}$ is met	VCONN powering off	–	–	250	ms
t_{VCONN_ON}	Maximum time from when PMI supplies V_{BUS} in the attached source state to when VCONN reaches 5 V	DFP mode, $V_{BUS} \geq 5$ V, VCONN powering on	–	–	2	ms

Table 3-7 Battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VCONN_OFF}	Maximum time from when the sink is detached or as commanded until VCONN supply is disabled and the bulk capacitance is removed	VCONN powering off	–	–	35	ms
$V_{VCONN\_DISCHARGE}$	Maximum VCONN voltage following cable detach	VCONN disabled	–	–	150	mV
t_{VBUS_ON}	Maximum time from entry of attached source state until V_{BUS} reaches 5 V	DFP mode, charger boost enabled	–	–	275	ms
t_{VBUS_OFF}	Maximum time from when the sink is detached until V_{BUS} is powered off and reaches 0 V	DFP mode, charger boost powering off	–	–	650	ms
t_{SINK_ADJ}	Response time for the PMI to decrease its input current limit to be within the specified range due to a change in Type-C current advertisement	Sink mode, charger buck enabled	$t_{PD\_Debounce}$	–	60	ms
Thermal control and protection						
T_{TEMP_LB}	IC die temperature regulation window lower threshold	$T_{DIE} \geq T_{TEMP\_LB}$ (programmable 60˚C to 130˚C in 1˚C steps), die temperature rising, FG digital comparator	-3	–	3	°C
T_{TEMP_UB}	IC die temperature regulation window upper threshold	$T_{DIE} \geq T_{TEMP\_UB}$ (programmable, $T_{DIEREGL}$ + 1 to 10˚C with 1˚C steps), die temperature rising, FG digital comparator	-3	–	3	°C
T_{TEMP_RST}	Rapid increase die temperature threshold	$T_{DIE} \geq T_{TEMP\_UB}$, T_{DIE} rising, four programmable settings: 101°C, 110°C, 119°C, and 128°C	-3	134	3	°C
$T_{SKINREGL}$	Skin temperature regulation window lower threshold	$T_{SKIN} \geq T_{SKINREGL}$ (programmable 10˚C to 60˚C in 0.5˚C steps), skin temperature rising, FG digital comparator	-1	–	1	°C
$T_{SKINREGH}$	Skin temperature regulation window upper threshold		-1	–	1	°C

Table 3-7 Battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{SD}	IC thermal shutdown temp		–	155	–	°C
T_{HYST}	IC thermal shutdown hysteresis		–	20	–	°C
BOOT_PWR output						
V_{BOOT_PWR}	BOOT_PWR regulated output voltage	I_{OUT} = 20 mA, V_{USB_IN}/V_{DC_SNS} > 5.0 V, 5 V setting	4.7	5	5.3	V
		I_{OUT} = 20 mA, V_{USB_IN}/V_{DC_SNS} > 4.4 V, 4.4 V setting	4.136	4.4	4.664	V
$V_{BOOT\_PWRULVO}$	BOOT_PWR undervoltage lockout	V_{USB_IN}/V_{DC_SNS} falling	2.9	3.0	3.1	V
$I_{BOOT\_PWR\_LIM}$	BOOT_PWR output current limit	$V_{USB\_IN}/V_{DC\_SNS} \geq 5.0$ V	20	–	–	mA
PWM buck regulator and CurrentPath controller						
R_{DSON}	MOSFET on-resistance	USB_IN input FET (6 V)	–	25	–	mΩ
		USB_IN high-side FET (16 V)	–	50	–	mΩ
		Low-side FET (15 V)	–	65	–	mΩ
I_{BUCK_PK}	Buck peak switch current limit		-20	–	20	%
		V_{IN} = 9 V, V_{SYS} = 3.6 V to 4.6 V, all F_{SW}	–	5.25	–	A
I_{BUCK_DC}	Buck DC maximum output current	V_{IN} = 9 V, V_{SYS} = 3.6 V to 4.6 V, all F_{SW}	–	3	–	A
t_{MIN_WIDTH}	Minimum low-side pulse width	1-in-8 mode, option 1	–	100	–	ns
		1-in-8 mode, option 2	–	150	–	ns
		First pulse during start up	80	100	–	ns
V_{BOOT_UVLO}	Boot capacitor UVLO threshold	Boot UVLO enabled, 1-in-8 mode, V_{USB_IN}/V_{DC_IN} = 5 V	–	2.45	–	V
$f_{SW\_BUCK\_RANGE}$	Buck switching frequency range	Programmable (eight settings with 200 kHz steps)	600	–	1600	kHz
$f_{SW\_BUCK\_ACC}$	Buck switching frequency accuracy	T = 0°C to +70°C	-15	–	15	%
DC_{BUCK}	Buck duty cycle	Maximum, FSW = 1.05 MHz, 1-in-4 mode	–	96.25	–	%
		Maximum, FSW = 1.05 MHz, 1-in-8 mode	–	98.125	–	%
		Minimum	–	0	–	%

Table 3-7 Battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SYSMIN_RANGE}	Minimum regulated output voltage range	Programmable (four settings with 200 mV steps), $V_{BATT} < V_{SYSMIN}$, $I_{IN} < I_{LIM}$	3.2	–	3.8	V
		Programmable (four settings with 200 mV steps), $V_{BATT} < V_{SYSMIN}$, $I_{IN} = I_{LIM}$	3.1	–	3.7	V
V_{SYSMIN_ACC}	Minimum regulated output voltage accuracy	$V_{BATT} < V_{SYSMIN}$, $I_{IN} \leq I_{LIM}$	-3	–	3	%
V_{SYS}	Regulated output voltage	USB_IN present, charging enabled in full-on mode, $V_{SYSMIN} < V_{SYS} < V_{SYSMAX}$	–	V_{BATT} + (I_{CHG} x R_{DSON})	–	V
		USB_IN present, charging disabled, two programmable options, $V_{SYSMIN} < V_{SYS} < V_{SYSMAX}$	VBATT + 50 mV	VBATT + 100 mV	VBATT + 150 mV	V
$I_{DD\text{-}BUCK}$	Boot UVLO	Switcher enabled, no load, USB_IN = 5 V, $V_{SYS} = V_{SYSMIN}$, PFM, BOOT_UVLO mode	–	2	7	mA
	Buck active supply current	Switcher enabled, no load, USB_IN = 5 V, $V_{SYS} = V_{SYSMIN}$, PFM, 1-in-8 mode	–	6	9	mA
		Switcher enabled, no load, USB_IN = 5 V, V_{SYS} = 4.5 V, PWM mode	–	15	24	mA
V_{SYSOV}	System overvoltage protection threshold	Two programmable options, also disable bit	4.7	–	–	V
			4.8	–	–	
V_{SYSOV_HYST}	System overvoltage threshold hysteresis	V_{SYS} falling	–	100	–	mV
t_{SYSOV}	System overvoltage glitch filter	$V_{SYS} > V_{SYSOV}$	–	10	–	us
$\Delta V_{SYSLOAD}$	Output-voltage load regulation	I_{SYS} = 0.1 A to 4 A in 10 μs, C_{SYS} = 22 μF, C_{USB_IN} = 4.7 μF, C_{MID} = 4.7 μF, V_{BATT} = 3.9 V, PWM mode, F_{SW} = 1.05 MHz, charging disabled	V_{BATT} - 0.2	V_{BATT} - 0.1	–	V
V_{SOFT_LIMIT}	Soft-limit regulation voltage	Regulated system voltage, V_{SYS} falling, $V_{BATT} < V_{SYSMIN}$, $I_{IN} = I_{INLIM}$	–	V_{SYSMIN} - 100	–	mV
V_{IDEAL_DIODE}	Ideal diode regulation voltage	Regulated system voltage, V_{SYS} falling, $V_{BATT} > V_{SYS}$, $I_{IN} = I_{INLIM}$	–	V_{BATT} - 50	V_{BATT} - 90	mV

Table 3-7 Battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{BUCK\_PFM\_P-P}$	PFM buck output ripple	C_{SYS} = 22 μF, C_{USB_IN} = 4.7 μF, C_{MID} = 4.7 μF, no load, V_{BATT} = 3.0 V, PFM mode	–	50	–	mV
$V_{BUCK\_PWM\_P-P}$	PWM buck output ripple	C_{SYS} = 22 μF, C_{USB_IN} = 4.7 μF, C_{MID} = 4.7 μF, no load, V_{BATT} = 3.9 V, PWM mode, F_{SW} = 1.05 MHz	–	25	–	mV
PWM boost regulator-source/OTG/MyDP/MHL mode						
V_{BOOST_RANGE}	Boost regulated output voltage range	Four programmable options, in 100 mV steps	4.9	–	5.3	V
V_{BOOST_ACC}	Boost regulated output voltage accuracy	All settings	-3	–	3	%
$V_{BOOST\_PFM\_P-P}$	PFM boost output ripple	C_{SYS} = 22 μF, C_{USB_IN} = 4.7 μF, C_{MID} = 4.7 μF, no load, V_{BATT} = 4.4 V, PFM mode	–	100	–	mV
$V_{BOOST\_PWM\_P-P}$	PWM boost output ripple	C_{SYS} = 22 μF, C_{USB_IN} = 4.7 μF, C_{MID} = 4.7 μF, 500 mA load, V_{BATT} = 3.8 V, PWM mode, F_{SW} = 1.05 MHz	–	50	–	mV
$I_{DD-BOOST}$	Boost supply current	OTG mode, no load, PFM, F_{SW} = 800 kHz	–	12	–	mA
$V_{BATUVLO}$	Battery undervoltage lockout	Programmable 2.7 V to 3.30 V, V_{BATT} falling, $V_{BATUVLO}$ = 3.3 V	-4	–	4	%
$t_{BATUVLO}$	Battery undervoltage lockout glitch filter	Programmable 2.5 V to 3.30 V, V_{BATT} falling	–	20	–	ms
$V_{BATUVLOHY}$	UVLO hysteresis	OTG operation, T = 0°C to +70°C	–	65	–	mV
$I_{BOOST\_LIM\_RANGE}$	Steady-state boost output current limit range	Eight programmable options with 250 mA steps	250	–	1500	mA
$I_{BOOST\_LIM\_ACC}$	Steady-state boost output current limit accuracy	V_{BATT} = 3.9 V, F_{SW} = 1.0 MHz, V_{BUS} = 5.0 V, I_{BOOST_LIM} = 1.5 A	0	5	10	%
V_{BOOST_OCP}	Boost overcurrent shutdown threshold	I_{BOOST} > I_{BOOST_LIM}, V_{USB_IN} falling	–	V_{SYS} + V_{ASHDN}	–	V
t_{BOOST_OCP}	Boost short-current shutdown glitch filter	V_{USB_IN} > V_{BOOST_OCP}, V_{USB_IN} falling	–	20	–	ms

Table 3-7 Battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{BOOST\_OCP\_RETRY}$	Number of boost restart attempts	$I_{BOOST} > I_{OCP}$	–	–	3	
V_{BOOST_SC}	Boost short-current protection threshold	$I_{BOOST} > I_{BOOST\_LIM}$, $V_{USB\_IN} < V_{BOOST\_OCP}$, V_{USB_IN} falling	–	1	–	V
$F_{SW\_BOOST\_RANGE}$	Boost-switching frequency range	Programmable (eight settings with 200 kHz steps)	600	–	1600	kHz
$F_{SW\_BOOST\_ACC}$	Boost-switching frequency accuracy	T = 0°C to +70°C	-20	–	20	%
DC_{BOOST}	Boost duty cycle	Maximum, F_{sw} = 1.05 MHz	–	75	–	%
		Minimum	–	0	–	%
Battery FET						
R_{DSON}	BATT-to-SYS MOSFET on resistance	Battery FET (5 V)	–	9	–	mΩ
I_{BF_DC}	Maximum continuous DC battery FET current	Battery discharging	–	–	5	A
I_{BF_PEAK}	Peak battery FET current	Battery discharging, max 10 ms	–	–	10	A
$I_{BF\_OCP\_RANGE}$	Overcurrent threshold range	Programmable (56 settings with 80 mA steps)	4	–	8.4	A
$I_{BF\_OCP\_ACC}$	Overcurrent threshold accuracy	Internal sense	-2	–	2	%
$t_{BF\_OCP\_RANGE}$	Overcurrent threshold deglitch time range	Programmable (eight settings with 2 ms steps), $I_{BATT} > I_{OCP}$	1	–	17	ms
$t_{BF\_OCP\_ACC}$	Overcurrent threshold deglitch time accuracy	$I_{BATT} > I_{OCP}$	-5	–	5	%
$t_{BF\_OCP\_RETRY}$	Overcurrent battery FET reconnect time duration	$I_{BATT} > I_{OCP}$, battery FET open to closed	–	10	–	ms
Battery charger						
V_{BOV}	Battery overvoltage lockout	V_{BATT} rising	V_{FLT} + 0.05	V_{FLT} + 0.1	V_{FLT} + 0.150	V
$V_{TRICKLECHG}$	Trickle-charge to precharge voltage threshold		2	2.1	2.2	V
$I_{TRICKLECHG}$	Nominal trickle-charge current	V_{BATT} =1.7 V	–	45	–	mA
$I_{TRICKLEWEAR}$	Nominal wearables trickle-charge current	V_{BATT} < P2F Thresh ENG_WEAR_TRICK_EN =1	–	25	–	mA

Table 3-7 Battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PRECHG_RANGE}	Precharge to fast-charge voltage threshold range	Programmable, (four settings with 200 mV steps)	2.4	–	3	V
V_{PRECHG_ACC}	Precharge to fast-charge voltage threshold accuracy	T = 0°C to +70°C, V_{PRECHG} = 2.8 V	-4	–	4	%
I_{PRECHG_RANGE}	Precharge current range	Programmable, (with 25 mA steps)	0	–	1500	mA
I_{PRECHG_ACC}	Precharge current accuracy	T = 0°C to +70°C, I_{PRECHG} = 100 mA	-20	–	20	mA
I_{FCHG_RANGE}	Fast-charge current range	Programmable, (201 settings with 25 mA steps) [2]	0	–	5000	mA
I_{FCHG_ACC}	Fast-charge current accuracy	T = 0°C to +70°C, $I_{FCH} \geq$ 1000 mA 50 mA < IFCH < 300 mA 300 mA < IFCH < 1000 mA	-5 -40 -10	– – –	5 40 10	% mA %
V_{FLT_RANGE}	Float voltage range	Programmable (120 settings with 10 mV steps), T = 0°C to +70°C	3.6	–	4.79	V
V_{FLT_ACC}	Float voltage accuracy	V_{FLT} < 4.2 V, T = 0°C to +70°C	-1	–	1	%
		$V_{FLT} \geq$ 4.2 V, T = 0°C to +70°C	-0.5	–	0.5	%
I_{TERM_RANGE}	Charge-termination current range	FG setting, programmable (40 mA steps)	60	–	760	mA
t_{TERM}	Charge-termination glitch filter time	FG controlled	164	–	1500	ms
V_{RECHG_RANGE}	Automatic recharge threshold range	FG setting, programmable (25 mV steps)	4	–	4.75	V
V_{RECHG_ACC}	Automatic recharge threshold accuracy	FG V_ADC accuracy over temp	-0.2	–	0.2	%
t_{RECHG}	Glitch filter time for recharge	FG controlled	164	–	1500	ms
$V_{INHIBIT\_RANGE}$	Charge-inhibit threshold voltage range	FG setting; four steps, after power applied	50	–	300	mV
$V_{INHIBIT\_ACC}$	Charge-inhibit threshold voltage accuracy		–	V_{FLT}-85	–	mV
$t_{INHIBIT}$	Glitch filter time for inhibit	FG controlled	164	–	1500	ms
t_{GLITCH_BATT}	Battery voltage glitch filter		–	175	–	ms

Table 3-7 Battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input missing poller						
Conditions	Input missing poller algorithm active conditions	I_{in} < 100 mA, battery = present, maximum duty-cycle = true	–	–	–	–
I_{PULL_DOWN}	USB_IN/DC_IN and USB_IN_MID/ pull-down combined current source strength	Input missing poller active	–	20	–	mA
t_{IMP}	Input missing poller active timing	Charger buck disabled, 20 mA current sink enabled (option 1)	–	3	–	ms
		Charger buck disabled, 20 mA current sink enabled (option 2)	–	75	–	ms
V_{IMP}	Input missing detection voltage threshold	Input missing poller active, charger buck disabled, 20 mA current sink enabled	–	V_{REVI}	–	V
Logic inputs/outputs						
V_{IL}	Input logic-low threshold	QI_PMA_ON	–	–	0.6	V
V_{IH}	Input logic-high threshold	QI_PMA_ON	1.4	–	–	V
V_{OL}	CC_OUT/ VCONN_EN/ output low level	I_{SINK} = 2 mA	–	–	0.3	V
V_{OH1_8}	CC_OUT/ VCONN_EN/ output high level		–	1.8	–	V
R_{PULL}	Push-pull output pull-up resistance	Output configured as push-pull, V_{DD} = 1.8 V	–	1.27	–	kΩ
I_{LEAK}	STAT leakage current	V_{IN} = 5.0 V	–	–	1	µA
Missing-battery detection						
I_{BMDDIS}	Missing-battery detection discharge current	For the first 100 ms	–	10	–	mA
V_{BMDDIS}	Missing-battery detection voltage		–	V_{FLT} - V_{RECH}	–	V
t_{BMDDIS}	Missing-battery detection timer		–	85	–	ms
Low-battery/SYS_OK voltage detector						
$V_{LOWBATT\_RANGE}$	Low-battery voltage detection threshold range (triggers PON to SBL)	Programmable (16 settings with 50 mV steps), V_{BATT} falling	2.5	–	3.25	V

Table 3-7 Battery charger specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{LOWBATT\_ACC}$	Low-battery voltage detection threshold accuracy (triggers PON to SBL)	$V_{LOWBATT}$ = 2.8 V	-2	–	2	%
$T_{LOWBATT}$	Low battery voltage glitch filter	V_{BATT} rising or falling	–	175	–	ms
$V_{LOWBATTHYS}$	Low-battery voltage/HLOS detection threshold hysteresis	V_{BATT} rising	–	200	–	mV
Oscillator						
f_{OSC_MAIN}	Main oscillator frequency	Same as buck/boost switching frequency specifications	–	1.05	–	MHz
f_{OSC_STBY}	Standby oscillator frequency		198	200	202	kHz
CurrentPath controller						
t_{START}	Start-up time	USB_IN or DC_IN connected to VSYS start-up	200	–	–	ms
$t_{ID\text{-}ON}$	Ideal diode turn-on time	Falling	–	10	–	µs
$t_{ID\text{-}OFF}$	Ideal diode turn-off time	Rising	–	10	–	µs
Watchdog and safety timers						
t_{CTOPC}	Precharge safety timer	Programmable (48 min to 191 min)	-20	–	20	%
t_{CTOFC}	Complete charge safety timer	Programmable (382 min to 1527 min)	-20	–	20	%
t_{SYS_HO}	Buck start-up holdoff timer	USB_IN	200	–	–	ms
		DC_IN	5	10	15	ms
t_{CHG_HO}	Charger start-up holdoff timer	Enabled	250	–	–	ms
		Disabled	–	1	–	ms
t_{SNARL_WD}	Snarl watchdog timer	Programmable (eight settings, 1/16 sec to 8 sec), snarl timer enabled	-20	–	20	%
t_{BARK_WD}	Bark watchdog timer	Programmable (four settings, 16 sec to 128 sec), bark timer enabled and expired	-20	–	20	%
t_{BITE_WD}	Bite watchdog timer	Programmable (four settings, 1/16 sec to 8 sec), bark timer expired, bite timer enabled and expired	-20	–	20	%

1. I_{CHG} is overridden by the input current limit (I_{LIM})
2. Recommended to use minimum setting of 50 mA or above

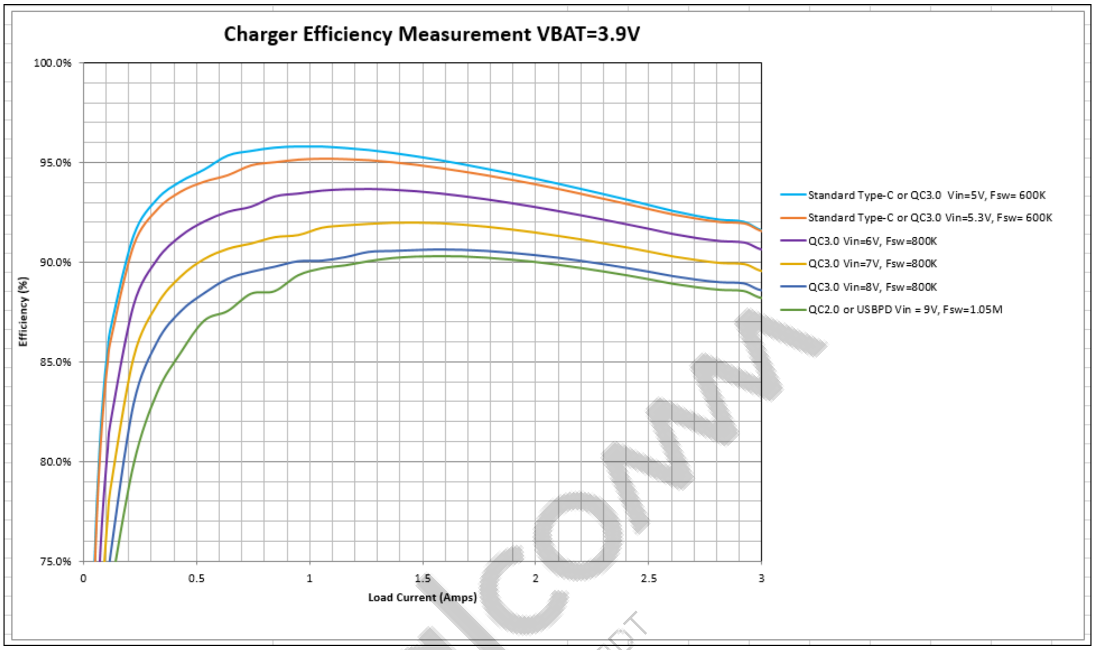


Figure 3-3 Charger efficiency measurement

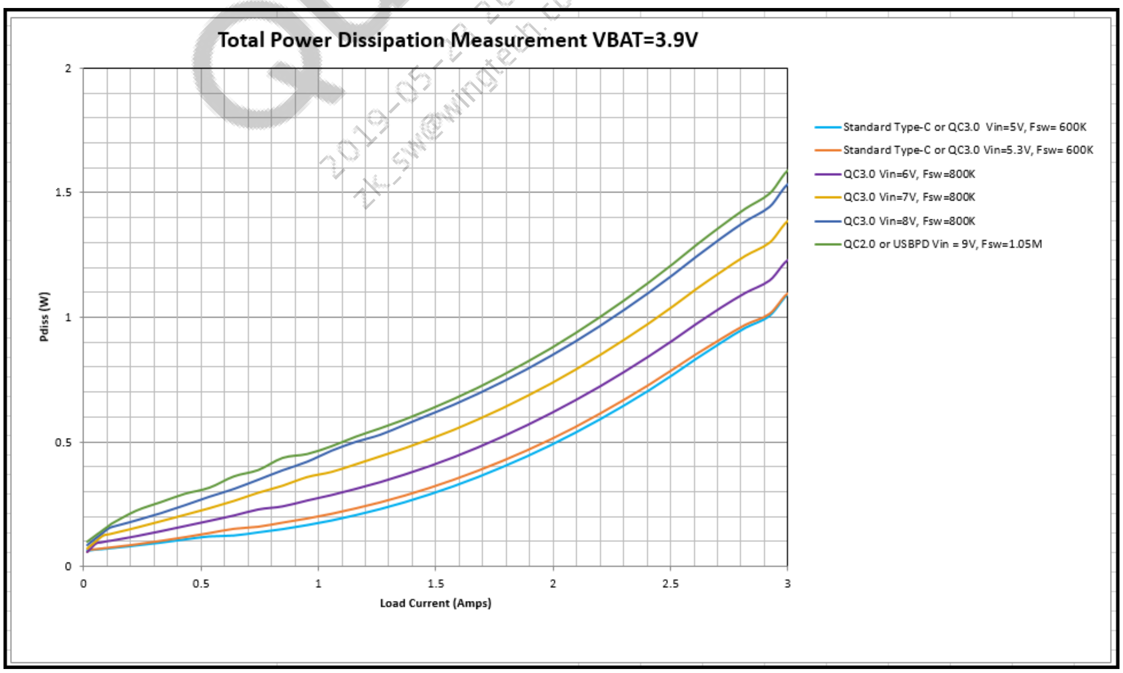


Figure 3-4 Total power dissipation measurement

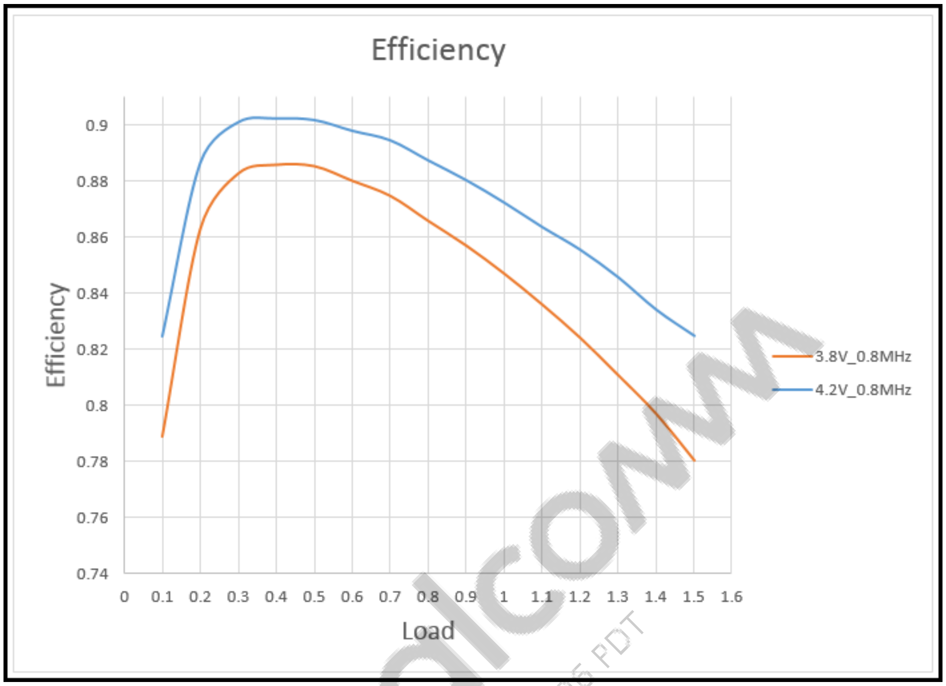


Figure 3-5 OTG efficiency across battery voltage and output current

The data is measured under the following conditions: Vbatt = 3.8 V and 4.2 V (measured at the Vbatt node), 800 kHz switching frequency

3.5.3 Fuel gauge

The fuel gauge module offers a hardware-based algorithm that is able to accurately estimate the battery's state of charge by using current monitoring and voltage-based techniques. This hybrid approach ensures both excellent short-term linearity and long-term accuracy. Furthermore, neither full battery charge cycling, nor zero-current-load conditions, are required to maintain the accuracy.

The fuel gauge measures the battery pack temperature by sensing the voltage across an external thermistor. Missing battery detection is also incorporated to accurately monitor battery insertion and removal scenarios, while properly updating the state of charge when a battery is reconnected.

Using precise measurements of battery voltage, current, and temperature, the fuel gauging algorithm compensates for the variation in battery characteristics across temperature changes and aging effects. This provides a dependable state of charge estimate throughout the entire life of the battery and across a broad range of operating conditions.

A low level of interaction with the system is required. A broad range of configuration registers are provided to fit the requirements of various applications.

Performance specifications for the PM670/PME605 fuel gauge are presented in Table 3-8.

Test conditions (unless otherwise noted); all voltages are relative to GND.

- T_A = -30°C to +85°C
- V_{USBIN} = 5.0 V, 9.0 V, or missing
- V_{FLT} = 4.4 V
- 2.7 V < V_{BATT} < 4.75 V

Table 3-8 PM670/PME605 FG performance specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Battery voltage ADC						
$NBIT_{VBATT}$	Battery voltage resolution	UVLO is defined as the higher of V_{UVLO} or battery voltage + V_{ASHDN}.	–	15	–	bits
LSB_{VBATT}	Battery voltage LSB		–	152.6	–	µV
$VBATT_{TCONV}$	Battery voltage conversion time	15 bit	–	163.84	–	ms
$VBATT_{GRNG}$	Battery voltage guaranteed input range		0	–	4.75	V
$VBATT_{ACC}$	Battery voltage absolute accuracy	(VBATT_SNS_P - VBATT_SNS_M); T_A = 25°C; V_{BATT} = 3.0 V to 4.4 V	-0.15	–	0.15	%
		(VBATT_SNS_P - VBATT_SNS_M); T_A = 0°C to +70°C; V_{BATT} = 3.0 V to 4.4 V	-0.3	–	0.3	%
Battery ID: ADC and battery missing						
$NBIT_{VBID}$	Battery ID voltage reading bit number		–	10	–	bits
LSB_{VBID}	Battery ID voltage reading LSB		–	2.441	–	mV
$VBID_{RNG}$	Battery ID voltage nominal input range		0	–	2.5	V
$VBID_{GRNG}$	Battery ID voltage guaranteed input range	V_{AA} = 2.7 V	0	–	2.35	V

Table 3-8 PM670/PME605 FG performance specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$VBID_{ACC}$	Battery ID voltage reading gain accuracy, room temperature	T_A = 25°C; V_{BATT_ID} > 1 V	-0.75	–	0.75	%
	Battery ID voltage reading gain accuracy, over temperature	T_A = 0°C to +70°C; V_{BATT_ID} > 1 V	-1	–	1	%
	Battery ID voltage reading offset, room temperature	T_A = 25°C; V_{BATT_ID} < 1 V	-7.5	–	7.5	mV
	Battery ID voltage reading offset, over temperature	T_A = 0°C to +70°C; V_{BATT_ID} < 1 V	-10	–	10	mV
$IBID_{I1}$	Bias current 1 value	T_A = 25°C	–	150	–	μA
	Bias current 1 tolerance		-5	–	5	%
$IBID_{I2}$	Bias current 2 value	T_A = 25°C	–	15	–	μA
	Bias current 2 tolerance		-5	–	5	%
$IBID_{I3}$	Bias current 3 value	T_A = 25°C	–	5	–	μA
	Bias current 3 tolerance		-5	–	5	%
$BID_{MISSING}$	Battery guaranteed to be detected as missing		750	–	–	kΩ
Battery thermistor: ADC and battery missing						
$NBIT_{BTHERM}$	Thermistor voltage reading bit number		–	10	–	bits
LSB_{BTHERM}	Thermistor voltage reading LSB	BATT_THERM_BIAS = 2.7 V; 10 bits	–	2636	–	μV
$BTHERM_{RNG}$	Thermistor voltage nominal input range	BATT_THERM_BIAS = 2.7 V	–	0 to 2.7	–	V
$BTHERM_{GRNG}$	Thermistor voltage guaranteed input range	THERM pin; referenced to battery thermistor bias	0	–	94%	[FSR]
$VBTHERM_{ACC}$	Thermistor voltage reading gain accuracy, room temperature	T_A = 25°C; BATT_THERM_BIAS = 2.7 V; V_{THERM} > 1 V	-1	–	1	%
	Thermistor voltage reading gain accuracy, over temperature	T_A = -20°C to +70°C; BATT_THERM_BIAS = 2.7 V; V_{THERM} > 1 V	-1.5	–	1.5	%
	Thermistor voltage reading offset, room temperature	T_A = 25°C; BATT_THERM_BIAS = 2.7 V; V_{THERM} < 1 V	-7.5	–	7.5	mV
	Thermistor voltage reading offset, over temperature	T_A = -20°C to +70°C; BATT_THERM_BIAS = 2.7 V; V_{THERM} < 1 V	-10	–	10	mV

Table 3-8 PM670/PME605 FG performance specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$TBTEMP_{ACC}$	Battery temperature measurement and mapping accuracy	T_{Batt}: 0°C to +50°C; I_{BATT} < 50 mA; thermistor β= 3450; thermistor value = 68 K; ideal passives	-1	–	2	°C
	Battery temperature measurement and mapping accuracy	T_{Batt}: -10°C to +60°C; I_{BATT} < 50 mA; Thermistor β= 3450; Thermistor value = 68 K; ideal passives	-3.25	–	3.25	°C
$V_{BATT\_THERM\_BIAS}$	Biasing voltage value	T_A = 0°C to +70°C; V_{AA} = 2.7 V	2.43	–	2.97	V
		T_A = 0°C to +70°C; V_{AA} = 2.57 V	2.31	–	2.76	V
		T_A = 0°C to +70°C; V_{AA} = 3.0 V	2.7	–	3.3	V
$TPREBIAS_{STEPS}$	Prebiasing length for thermistor conversion	Steps: 1, 2, 4, 8, 12, 16, 24, 32, and 40	1	–	40	ms
BAT_THERM_{RES}	Supported thermistor value range		10	–	100	kΩ
	Supported thermistor accuracy		–	0.5	–	%
	Supported thermistor beta value range		3200	–	4400	–
BAT_THERM_{CAP}	Supported thermistor capacitor value	$BATT\_THERM_{RES}$ = 10 kΩ to 100 kΩ	0	5	100	nF
$THERM_{MISSING}$	Battery guaranteed to be detected as missing	Value expressed as a $V_{THERM}/V_{BATT\_THERM\_BIAS}$ ratio; BATT_THERM_BIAS > 0.5 V	96	–	–	%
$THERM_{PRESENT}$	Battery guaranteed to be detected as present	Value expressed as a $V_{THERM}/V_{BATT\_THERM\_BIAS}$ ratio; BATT_THERM_BIAS > 0.5 V	–	–	94	%
Skin/external thermistor: ADC						
$NBIT_{SETHERM}$	Skin/external voltage bit number		–	10	–	bits
$LSB_{SETHERM}$	Skin/external thermistor voltage reading LSB	BATT_THERM_BIAS_EXT = 2.7 V, 10 bits	–	2636	–	μV
$SETHERM_{RNG}$	Skin/external thermistor voltage nominal input range	BATT_THERM_BIAS_EXT = 2.7 V	–	0 to 2.7	–	V

Table 3-8 PM670/PME605 FG performance specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$SETHERM_{GRNG}$	Skin/external thermistor voltage guaranteed input range	THERM pin; referenced to auxiliary thermistor bias	0	–	94%	[FSR]
$SEVTHERM_{ACC}$	Skin/external thermistor voltage reading gain accuracy, over temperature	T_A = -20°C to +70°C; V_{THERM} > 1 V	-0.5	–	2	%
	Skin/external thermistor voltage reading offset, over temperature	T_A =-20°C to +70°C; V_{THERM} < 1 V	5	–	25	mV
$TSTEMP_{ACC}$	Skin thermistor measurement and mapping accuracy for skin temperature regulation	T_{SKIN_CENTER} = 45°C; T_{SKIN}: 35°C to 60°C; I_{BATT} < 50 mA; skin/external thermistor β = 3450; skin/external thermistor value = 68 K; ideal passives	-0.5	–	1	°C
		T_{SKIN_CENTER} = 45°C; T_{SKIN}: 25°C to 70°C; I_{BATT} < 50 mA; skin/external thermistor β = 3450; skin/external thermistor value = 68 K; ideal passives	-0.5	–	2	°C
USB input voltage: ADC specifications						
$USB\_IN\_V_{NBIT}$	USB_IN voltage bit number		–	10	–	bits
$LSB_{USB\_IN\_V}$	USB_IN voltage LSB		–	15.6	–	mV
$USB\_IN\_V_{TCONV}$	USB_IN voltage conversion time		–	5.1	–	ms
$USB\_IN\_V_{RNG}$	USB_IN voltage input nominal range		0	–	16 - LSB	V
$USB\_IN\_V_{GRNG}$	USB_IN voltage guaranteed input range		0	–	15.25	V
$USB\_IN\_V_{ACC}$	USB_IN voltage accuracy	T_A = 0°C to +70°C; 4 V < V_{USB_IN} < 15.25 V	-1	–	0.65	%
USB input current: ADC specifications						
$USB\_IN\_I_{NBIT}$	USB_IN current bit number		–	10	–	bits
$LSB_{USB\_IN\_I}$	USB_IN current LSB		–	4.9	–	mA
$USB\_IN\_I_{TCONV}$	USB_IN current conversion time		–	5.1	–	ms
$USB\_IN\_I_{RNG}$	USB_IN current input nominal range		0	–	5-LSB	A

Table 3-8 PM670/PME605 FG performance specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$USB\_IN\_I_{GRNG}$	USB_IN current guaranteed input range		0	–	4.5	A
$USB\_IN\_I_{ACC}$	USB_IN current accuracy	T_A = 0°C to +70°C; 3.4 V < V_{BATT} < 4.4 V; 4 V < V_{USB_IN} < 5.5 V; input current = 1 A to 5 A; voltage-to-current scaling factor: 0.536	-7.5	–	7.5	%
		T_A = 0°C to +70°C; 4 V < V_{USB_IN} < 15.25 V; input current < 1 A	-80	–	60	mA
Charger die temperature: ADC specifications						
$VDIECHG_{NBIT}$	Charger die temperature voltage bit number		–	10	–	bits
$LSB_{DIECHG\_TEMP\_V}$	Charger die temperature voltage LSB		–	1.63	–	mV
$VDIECHG_{TCONV}$	Charger die temperature voltage conversion time		–	5.1	–	ms
$VDIECHG_{RNG}$	Charger die temperature voltage input nominal range		0	–	1.85	V
$VDIECHG_{GRNG}$	Charger die temperature voltage guaranteed input range		0	–	1.666	V
$VDIECHG_{ACC}$	Charger die temperature channel accuracy	T_A = -20°C to +70°C	-10	–	10	mV
PMIC die temperature: ADC specifications						
$VDIEPMI_{NBIT}$	PMIC die temperature voltage bit number		–	10	–	bits
$LSB_{DIEPMI\_TEMP\_V}$	PMIC die temperature voltage LSB		–	1.63	–	mV
$VDIEPMI_{TCONV}$	PMIC die temperature voltage conversion time		–	5.1	–	ms
$VDIEPMI_{RNG}$	PMIC die temperature voltage input nominal range		0	–	1.85	V
$VDIEPMI_{GRNG}$	PMIC die temperature voltage guaranteed input range		0	–	1.66	V
$VDIEPMI_{ACC}$	PMIC die temperature channel accuracy	T_A = -20°C to +70°C	-8	–	8	mV

Table 3-8 PM670/PME605 FG performance specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Internal sensing without external reporting: ADC specifications						
$IBATTIS_{NBIT}$	Internal sensing without external reporting bit number		–	15	–	bits
$LSB_{IBATTIS}$	Internal sensing without external reporting LSB		–	305	–	µA
$IBATTIS_{TCONV}$	Internal sensing without external reporting conversion time		–	163	–	ms
$IBATTIS_{GRNG}$	Internal sensing without external reporting guaranteed input range		-8.5	–	8.5	A
$IBATTIS_{ACC}$	Internal sensing without external reporting current accuracy	T_A = 25°C; V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = 1 A to 8 A; discharge	-5	–	5	%
		T_A = 25°C; V_{BATT} = 3.4 V to 4.4 V; I_{BATT} = -1 A to -4.5 A; V_{BATT} > V_{SYSMIN}; charging	-3	–	3	%
		T_A = 0°C to +70°C; V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = 1 A to 8 A; V_{BATT} > V_{SYSMIN}; discharge	-6.5	–	6.5	%
		T_A = 0°C to +70°C; V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = -1 A to -4.5 A; V_{BATT} > V_{SYSMIN}; charging	-6.5	–	6.5	%
		T_A = 25°C; V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = 0 to -1 A; charging	-35	–	40	mA
		T_A = 0°C to +70°C; V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = 0 to -1 A; V_{BATT} > V_{SYSMIN} charging	-70	–	70	mA
		T_A = 25°C; V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = 0 A to 1 A; discharge	-40	–	40	mA
		T_A = 0°C to +70°C; V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = 0 A to 1 A; discharge	-70	–	70	mA
		T_A = 25°C V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = 1 A to 8 A; discharge	-5	–	5	%

Table 3-8 PM670/PME605 FG performance specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$IBATTIS_{TERM\_ACC}$	Internal sensing without external reporting charge termination current accuracy	T_A = 0°C to +70°C; V_{BATT} = 4.4 V; V_{USB_IN} = 5 V; I_{BATT} = -100 mA	-60	-100	-140	mA
Internal sensing with external reporting: ADC specifications						
$IBATTISWR_{NBIT}$	Internal sensing with external reporting bit number		–	15	–	bits
$LSB_{IBATTISWR}$	Internal sensing with external reporting LSB		–	305	–	µA
$IBATTISWR_{TCONV}$	Internal sensing with external reporting conversion time		–	163	–	ms
$IBATTISWR_{GRNG}$	Internal sensing with external reporting guaranteed input range		-8.5	–	8.5	A

Table 3-8 PM670/PME605 FG performance specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$IBATTISWR_{ACC}$	Internal sensing with external reporting current accuracy (charging only)	T_A = 25°C; V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = -1 A to -8.5 A; $V_{BATT} > V_{SYSMIN}$; 5 V charging	-2	–	3.5	%
		T_A = 0°C to +70°C; V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = -1 A to -8.5 A; $V_{BATT} > V_{SYSMIN}$; 5 V charging	-4	–	5.5	%
		T_A = 25°C; V_{BATT} = 3.4 V to 4.4 V; I_{BATT} = -2.5 A to -8.5 A; $V_{BATT} > V_{SYSMIN}$; 9 V charging	-2	–	4.5	%
		T_A = 0°C to +70°C; V_{BATT} = 3.4 V to 4.4 V I_{BATT} = -2.5 A to -8.5 A; $V_{BATT} > V_{SYSMIN}$; 9 V charging	-4	–	6	%
		T_A = 25°C; V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = 0 to -1 A; $V_{BATT} > V_{SYSMIN}$; 5 V charging	-35	–	45	mA
		T_A = 0°C to +70°C; V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = 0 to -1 A; $V_{BATT} > V_{SYSMIN}$; 5 V charging	-35	–	60	mA
		T_A = 25°C; V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = -0.3 A to -1 A; $V_{BATT} > V_{SYSMIN}$; 9 V charging	-10	–	55	mA
		T_A = 0°C to +70°C; V_{BATT} = 3.0 V to 4.4 V; I_{BATT} = -0.3 A to -1 A; $V_{BATT} > V_{SYSMIN}$; 9 V charging	-35	–	65	mA
$IBATTISWR_{TERM\_ACC}$	Internal sensing with external reporting termination current accuracy	T_A = 0°C to +70°C; V_{BATT} = 4.2 V to 4.55 V; V_{USB_IN} = 5 V; I_{BATT} = -100 mA	-85	-100	-140	mA

Table 3-8 PM670/PME605 FG performance specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BCL/LMh reporting: battery current ADC and threshold specifications						
$BCLIADC_{RES}$	Resolution of BCL battery current reading	7 bit + sign	–	80	–	mA
$BCLIADC_{SAMPLETIME}$	BCL sample interval	LPM	–	–	1.47	sec
		HPM	–	–	1	ms
$BCLIADC_{GRNG}$	BCL current guaranteed range		-8.42	–	8.42	A
$BCLIADC_{ACC}$	Accuracy of BCL battery current reading	Internal sensing; T_A = 0°C to +70°C; V_{BATT} = 2.5 V to 4.75 V; I_{BATT} = 0 A to +8.5 A	-540	–	540	mA
BCL/LMh reporting: battery voltage ADC specifications						
$BCLVADC_{RES}$	Resolution of BCL battery voltage reading	7 bit + sign	–	80	–	mA
$BCLVADC_{SAMPLETIME}$	BCL sample interval	LPM	–	–	1.47	sec
		HPM	–	1	50	ms
$BCLVADC_{RNG}$	BCL voltage nominal range		2	–	5	V
$BCLVADC_{GRNG}$	BCL voltage guaranteed range		2	–	4.75	V
$BCLVADC_{ACC}$	Accuracy of BCL battery voltage reading	Internal sensing, without external reporting; T_A = 25°C; V_{BATT} = 2.0 V to 4.75 V; I_{BATT} < 4 A; time = 80 ms	-120	–	120	mV
BCL/LMh reporting: battery voltage comparator						
$VBATT\_L_{ACC}$	V_{BATT} low comparator accuracy		-30	–	30	mV
$VBATT\_TL_{ACC}$	V_{BATT} too-low comparator accuracy		-30	–	30	mV
Standby oscillator specification						
$STBOSC_{ACC}$	ADC clock time base accuracy	T_A= 25°C	198	200	202	kHz
		T_A= 0°C to +70°C	196	200	204	kHz
FG reference specifications						
VREG_FG	Regulator for ADC		2.5	–	3.0	V
SRAM _RETENTION	Minimum input supply voltage for memory volatile content retention		–	2.5	–	V

Table 3-8 PM670/PME605 FG performance specifications (cont.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR detection						
ESR_{PDOWN}	ESR pull-down current	T_A = 0°C to +70°C	–	150	–	mA

NOTE: Relevant FG SoC accuracy plots will be provided in a future revision of this document.

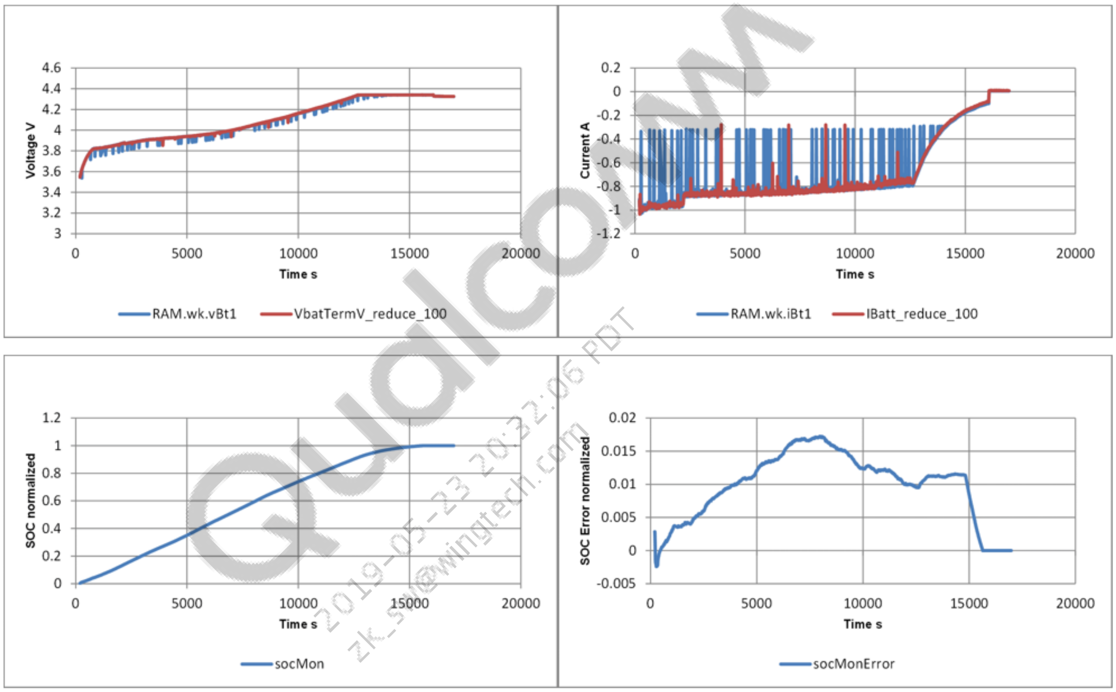


Figure 3-6 Typical charge

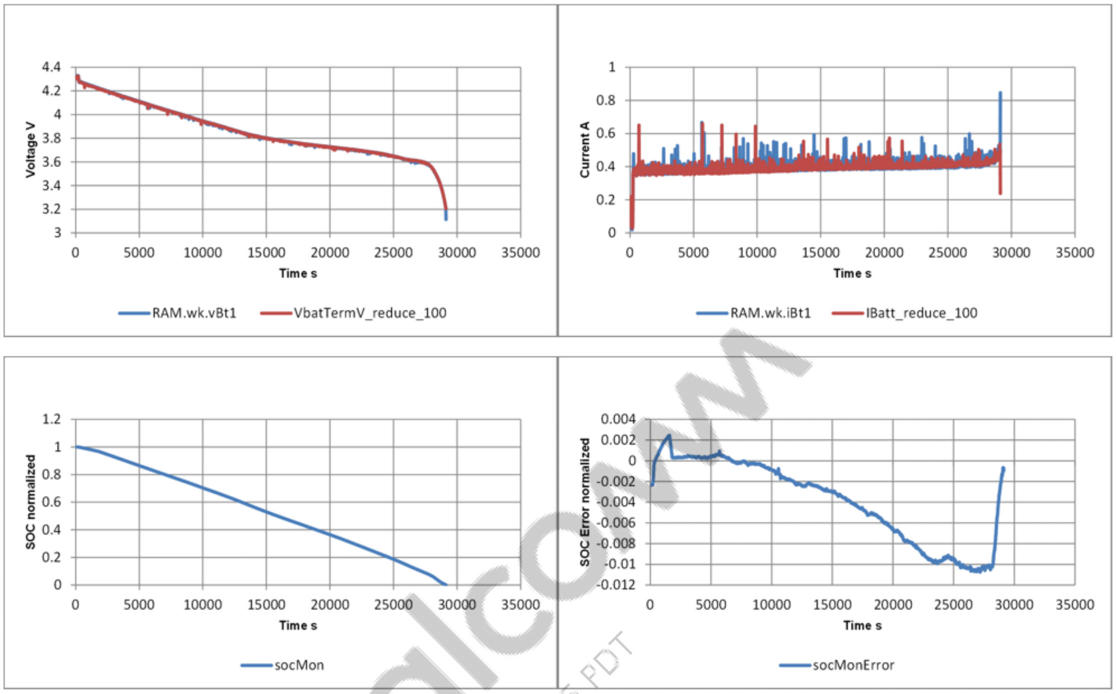


Figure 3-7 Typical discharge

3.5.3.1 Battery serial interface

Battery serial interface (BSI) implements the physical layer of the MIPI battery interface (BIF) to connect either a low cost or smart battery pack. When interfaced with a smart battery, BSI enables a single-wire serial interface that allows digital communication between a mobile device (host) and battery (slave) over a battery communication line (BCL) or battery ID (BATT_ID) line. The purpose of BIF is to provide a method for communicating battery characteristics information to ensure safe and efficient charging control under all operating conditions. The software detects if a smart battery is connected and enables digital communication over BCL. BIF also provides battery authentication through a digital unique ID (UID) so that the host device can take appropriate action when an unauthorized battery is connected to the phone.

Table 3-9 BSI performance specifications

Parameter	Comments [1]	Min	Typ	Max	Unit
MIPI-BIF I/O electrical specifications					
BCL logic high or idle voltage	R_ID = 240 kΩ–450 kΩ I_PU = 5 µA	1.2	–	2.25	V
BCL logic low voltage	R_ID = 450 Ω	–	–	0.1	V
Internal ID pull-up current source. See Table 3-8 for battery ID specifications.					
Internal fast pull-up resistor		7	9	11	kΩ
BCL idle DC voltage for low-cost battery Programmable range Accuracy	R_ID = 19.6 kΩ–140 kΩ	 0.294 -4	 – –	 2.1 4	 V %
MIPI-BIF I/O timing specifications for smart battery					
BIF time base range	Based on software programming	2	–	150	µs
Rise time	0 V to 1.1 V R_ID = 240 kΩ C_BCL = 50 pF	–	–	500	ns
Fall time	VOH_BCL (max) to 0.1 R_ID = 450 kΩ C_BCL = 50 pF	–	–	50	ns
MIPI-BIF timing specifications for battery removal detection					
Battery removal debounce filter time Programmable range Accuracy	Software programmable with step of 31 µs (32 kHz sleep clock)	 0 -16	 – –	 1 16	 ms %

1. T = -30°C to +85°C, +2.7 V < V_{BATT} < +4.5 V, unless otherwise noted. All voltages are relative to GND.

3.6 Output power management

Output power management circuits include:

- Bandgap voltage reference circuit
- Internal voltage regulator connections
- High-frequency switched-mode power supply (HF-SMPS) circuits
- Fast-transient SMPS (FT-SMPS) circuits
- LDO linear regulators

The PM670 device is supplemented by the PM670A/PM670L device to provide all the regulated voltages needed for most wireless handset applications. Similarly, PME605 is supplemented by PM8005 to provide power to target applications.

Independent regulated power sources are required for various electronic functions to avoid signal corruption between diverse circuits, to support power management sequencing, and to meet different voltage-level requirements.

A total of 24 programmable voltage regulators are provided by the PMIC, with all outputs derived from a common bandgap reference circuit. Each regulator can be set to a low-power mode for power savings.

A high-level summary of all regulators is listed in Table 3-10 and Table 3-11.

Table 3-10 SMPS regulator summary for PM670

Regulator name	Circuit type	I_{RATED} (mA) [1]	PON sequence	Default state or on boot voltage (V) [2]	Nominal voltage (V)	Sleep state	Specified/ programmable range [3]	Expected use
S1A	FTS426 SMPS	4000	28	0.828	0.752	Off	0.344 V to 0.952 V	Qualcomm® Kryo™ Silver APC
S2A–S3A	FTS426 SMPS	8000	–	Off	0.752	Off	0.348 V to 1.056 V	Kryo Gold APC
S4A	HFS3 SMPS	3000	3	2.04	2.04	On	1.808 V to 2.04 V	HV subregulation LDOs
S5A	HFS3 SMPS	3000	27	0.828	0.752	Off	0.348 V to 1 V	Modem SS–Modem Q6–Boot memory
S6A	HFS3 SMPS	2000	12	1.352	1.352	On	1.224 V to 1.4 V	MV subregulation LDOs
S2A	FTS426 SMPS	4000	–	Off	0.752	Off	0.348 V to 1.056 V	APPS1–Single phase alternate
S3A	FTS426 SMPS	4000	16 (for single phase APPS1)	1.128	1.128	On	1 V to 1.2 V	LPDDR4X VDD2 alternate

1. Rated current is the maximum current for which specification compliance is guaranteed, unless otherwise stated.
   The current capability on SMPS regulators (S1 through S6) may be less than the I_{RATED} values to optimize external electrical bill of materials. However, configurations are designed for necessary robustness in the chipset application.
2. All regulators have default voltage settings, whether they default on or not; the voltage and state depends on the programmable boot sequencer (PBS) configuration.
3. The specified voltage range is the programmed range for which performance is guaranteed to meet all specifications. For usage outside this range, submit a case to QTI for approval.

Table 3-11 Linear/low-voltage regulator summary for PM670

Regulator name	Circuit type	I_{RATED} (mA)	PON sequence	Default state/ on boot voltage (V)	Nominal voltage Vout (V)	Sleep state	Specified/ programmable range (V)	Expected use
LDO1A	N600-MT	600	19	1.2	1.2	On	1.096 V to 1.296 V	PHY 1.2 V–UFS VCCQ
LDO2A	N1200-HT	1200	–	Off	1.0	Off	0.896 V to 1.096 V	SDR 1.0 V analog
LDO3A	N600-MT	600	4	1.0	1.0	Off	0.896 V to 1.096 V	SDR 1.0 V digital
LDO5A	N600-HT	600	9	0.8	0.8	Lowered	0.488 V to 0.8 V	WCSS
LDO6A	N600-HT	600	14	1.304	1.304	Off	1.248 V to 1.352 V	WCN RF, GPS, Metis
LDO7A	N1200-HT	1200	–	Off	1.2	Off	1.096 V to 1.304 V	SDR 1.2
LDO8A	P600-LV-MT	800	17	1.8	1.8	Off	1.696 V to 1.904 V	EMMC/UFS 1.8 V
LDO9A	P150-LV-HT	150	13	1.8	1.8	Off	1.696 V to 1.904 V	WCN_XO
LDO10A	P300-LV-HT	300	22	1.8	1.8	Off	1.696 V to 1.904 V	PHY - PLL - BB_CLK - USB
LDO11A	P150-LV-MT	150	18	1.8	1.8	Off	1.696 V to 1.904 V	Display touchscreen
LDO12A	P300-LV-HT	300	–	Off	1.8	Off	1.696 V to 1.904 V	SDR 1.8 V BBRX_HV, DAC
LDO13A	P600-LV-MT	600	10	1.8	1.8	On	1.696 V to 1.904 V	P3 pad, general IO (1.8 V)
LDO14A	P150-LV-MT	150	–	Off	1.8	Off	1.696 V to 1.904 V	Sensors (1.8 V)
LDO15A	P150-MT	150	–	Off	1.808	Off	1.696 V to 3 V	UICC1. NFC
LDO16A	P150-MT	150	–	Off	2.704	Off	2.6 V to 2.8 V	QFE
LDO17A	P150-MT	150	–	Off	1.808	Off	1.696 V to 3 V	UICC2
LDO18A	P50-MT	50	–	Off	2.704	Off	2.6 V to 2.8 V	WLAN, WWAN antenna sharing
LDO19A	P600-MT	600	15	3.104	3.312	Off	3 V to 3.4 V	WCN CHAIN0
LDO_XO	P50	50	–	Off	1.8	Off	1.7 V to 1.9 V	Internal LDO for clock

NOTE:

- All regulators have default voltage settings, whether or not they default on; the voltage and state depends upon the programmable boot sequencer (PBS) configuration.
- The specified voltage range is the programmed range for which performance is guaranteed to meet all specifications.
  For usage outside this range, submit a case to QTI for approval.
  LDO-rated current specifications are only valid while maintaining their specified headroom.
- Regulators with suffix "A" are from PM670 and suffix "B" are from PM670A/PM670L

Table 3-12 SMPS regulator summary for PME605

Regulator name	Circuit type	I_{RATED} (mA)	Regulator source	PON sequence	Default state or on boot voltage (V)	Nominal voltage (V)	Sleep state	Specified/ programmable range	Expected use
S1A	FTS426 SMPS	4000	VPH	22	0.752	0.752	Off	0.348 to 0.952	Kryo cores
S2A	FTS426 SMPS	4000	VPH	3	0.8	0.8	Lowered	0.488 to 0.952	VDDMX - LPI_MX
S3A	FTS426 SMPS	4000	VPH	15	0.6	0.6	Off	0.570 to 0.648	LP-DDR4X VDDQ + EBI VDDIO
S4A	HFS3 SMPS	3000	VPH	1	2.04	2.04	On	1.64 to 2.04	HV SUB-REG LDO
S5A	HFS3 SMPS	3000	VPH	2	1	1	On	0.376-1.000	LV SUB-REG LDO
S6A	HFS3 SMPS	2000	VPH	10	1.352	1.352	Off	1.168-1.392	MV SUB-REG LDO

Table 3-13 Linear/low-voltage regulator summary for PME605

Regulator name	Circuit type	I_{RATED} (mA)	Regulator source	PON sequence	Default state/ on boot voltage (V)	Nominal voltage Vout (V)	Sleep state	Specified/ programmable range (V)	Expected use
L1A	N600-MT	600	S5A	6	0.8	0.8	Off	0.8 to 0.8	WLAN digital core
L2A	N1200-HT	1200	S6A	14	1.2	1.2	Off	1.15 to 1.25	PHY 1.2 V UFS VCCQ
L3A	N600-MT	138	S6A		Off	1.304	Off	1.15 to 1.35	WCN 1P3 RF
L5A	N600-HT	600	S6A		Off	1.2	Off	1.1 to 1.3	Camera 1.2 V digital
L6A	N600-HT	600	S5A	16	0.88	0.88	Off	0.88 to 0.88	PHY 0.88 V
L7A	N1200-HT	1200	S5A	4	0.8	0.8	On	0.352 to 0.952	LPI_CX
L8A	P600-LV-MT	600	S4A	13	1.8	1.8	On	1.7 to 1.95	UFS_EMMC VDDQ
L9A	P150-LV-HT	150	S4A		Off	1.8	Off	1.62 to 1.98	WCN XO
L10A	P300-LV-HT	300	S4A	17	1.8	1.8	Off	1.7 to 1.95	PLL - BBCLK - PHY_ USB
L11A	P150-LV_MT	150	S4A		Off	1.8	Off	1.7 to 1.9	CAMERA 1.8 V
L12A	P300-LV-HT	300	S4A		Off	1.8	Off	1.62 to 1.98	HDMI bridge chip
L13A	P600-LV-MT	600	S4A	7	1.8	1.8	On	1.7 to 1.9	GEN 1.8 V IO_LP-DDR4X VDD1
L14A	P150-LV-MT	150	S4A		Off	1.8	Off	1.7 to 1.9	Sensors
L15A	P150-MT	150	VPH		Off	2.8	Off	2.7 to 2.9	Rear camera 2.8 V auto focus
L16A	P150-MT	150	VPH		Off	3	Off	2.9 to 3.1	ALPS sensor
L17A	P150-MT	150	VPH	18	3.088	3.088	Off	2.921 to 3.23	USB
L18A	P50-MT	50	VPH	20	2.96	2.96	Off	2.7 to 3.6	SDCard IO
L19A	P600-MT	600	VPH	19	2.96	2.96	Off	2.95 to 3.3	UFS_EMMC VCC
LDO_XO	P50-LV-MT	50	S4A		Off	1.8	Off	1.7 to 1.95	Internal LDO for clock

3.6.1 Reference circuit

All PMIC regulator circuits, and some other internal circuits, are driven by a common, on-chip voltage reference circuit.

Applicable voltage reference performance specifications are given in Table 3-14.

Table 3-14 Voltage reference performance specifications

Parameter	Comments	Min	Typ	Max	Units
Nominal internal VREF		–	1.250	–	V
Output voltage deviations					
Normal operation	Over temperature only, -20ºC to +120ºC	-0.32	–	0.32	%
Normal operation	All operating conditions	-0.50	–	0.5	%
Sleep mode	All operating conditions	-1.00	–	1.00	%

3.6.2 Internal voltage-regulator connections

Some regulator supply voltages and/or outputs are connected internally to power other PMIC circuits. These circuits will not operate properly unless their source voltage regulators are enabled and set to their proper voltages. These requirements are summarized in Table 3-15.

Table 3-15 Internal voltage regulator connections

Voltage supply or regulator output	Default	Supported circuits
VDD_MSM_IO	1.8 V	GPIOs; SPMI
VPH_PWR	3.6 V	GPIOs
VREG_L10A	1.8 V	BB_CLK
VREG_L7B	3.125 V	USB PD PHY

3.6.3 HF-SMPS

The PM670 device includes three high-frequency switched-mode power supply (HF-SMPS) circuits. They support PWM and PFM modes, and the automatic transition between PWM and PFM modes, depending on the load current. They also support a retention mode, which is an ultralow power state allowing significant efficient improvements in sleep. Pertinent performance specifications are given in the following tables.

Table 3-16 HF buck generic specification (all modes)

Parameter	Comments	Min	Typ	Max	Units
Output voltage operating range		0.32	–	2.04	V
Enable overshoot (voltage upon buck enabling)		–	–	80	mV
Enable settling time (turning on and off regulator)	From enable to within 1% of the final value, no load	–	–	500	µs

Table 3-16 HF buck generic specification (all modes) (cont.)

Parameter	Comments	Min	Typ	Max	Units
Ground current, no load [1]	PWM mode PFM mode Retention mode	– – –	550 50 1	– – –	μA
Power supply ripple rejection ratio (PSRR) [2]	50 Hz 1 kHz 100 kHz	– – –	60 45 20	– – –	dB
Discharge time to 10% of output voltage [3]	Nominal load cap 10 μF (effective), initial voltage = 2.04 V. Strong pull-down enabled.	–	0.5	3	ms
Peak inductor current limit (via SPMI)		0.85 × Ilim	Ilim	1.15 × Ilim	mA

1. Quiescent current (no switching). Auto mode selects the PFM/PWM mode, depending on the load current.
2. The specification will be updated after the characterization is completed.
3. A higher value of capacitance takes longer to discharge and requires lower pull-down strength.

Table 3-17 HF buck specifications (PWM)

Parameter	Test condition	Min	Typ	Max	Units
DC accuracy (over voltage, normal mode, over process, load, temperature, and line regulation) [1]	$V_{out} \geq 0.8$ V $0.32 \leq V_{out} < 0.8$ V	-2 -16	0 0	2 16	% mV
Load transient response [2]	PWM mode, 400 mA load attack, or release	-50	–	80	–
Ripple voltage in PWM, continuous switching	Tested using 20 MHz BW limit	–	10	20	mVpp
Ripple voltage in PWM, light-load pulse skipping	Tested using 20 MHz BW limit at 40 mA load	–	20	50	mVpp

1. Buck in DCM/CCM, continuous switching
2. Applies to any 0.4 A step from 10 mA to I_{RATED} in > 1 μs steps

Table 3-18 HF buck specification PFM and retention mode (RM)

Parameter	Test condition	Min	Typ	Max	Units
Rated load current	PFM Retention mode	200 200 [1]	– –	– –	 mA
DC accuracy PFM mode (over voltage, over process, load, temperature, and line regulation) [2]	$V_{out} \geq 0.8$ V, $I_{RATED}/2$ $0.32 \leq V_{out} < 0.8$ V, 100 mA	-2 -16	– –	4 40	% mV
Ripple voltage in PFM mode	PFM low current mode, measured using 20 MHz bandwidth	–	–	50	mVpp
Ripple voltage in retention mode	Regulator maintains -50 mV to +80 mV from the programmed voltage	–	55	–	mVpp

Table 3-18 HF buck specification PFM and retention mode (RM) (cont.)

Parameter	Test condition	Min	Typ	Max	Units
Mode transition voltage regulation window PWM to/from PFM/retention [3]		-50	–	80	mV
Retention mode load current slew rate		–	–	1	mA/ms

1. Retention mode can only handle 1 mA/ms transient
2. Relates to the valley of the PFM waveform
3. Manual mode transition

Table 3-19 HF buck specifications auto mode

Parameter	Test condition	Min	Typical	Max	Units
Load transient response [1]	400 mA load step	-50	–	80	mV

1. Applies to any 0.4 A steps from 10 mA to I_{RATED} in > 1 µs steps

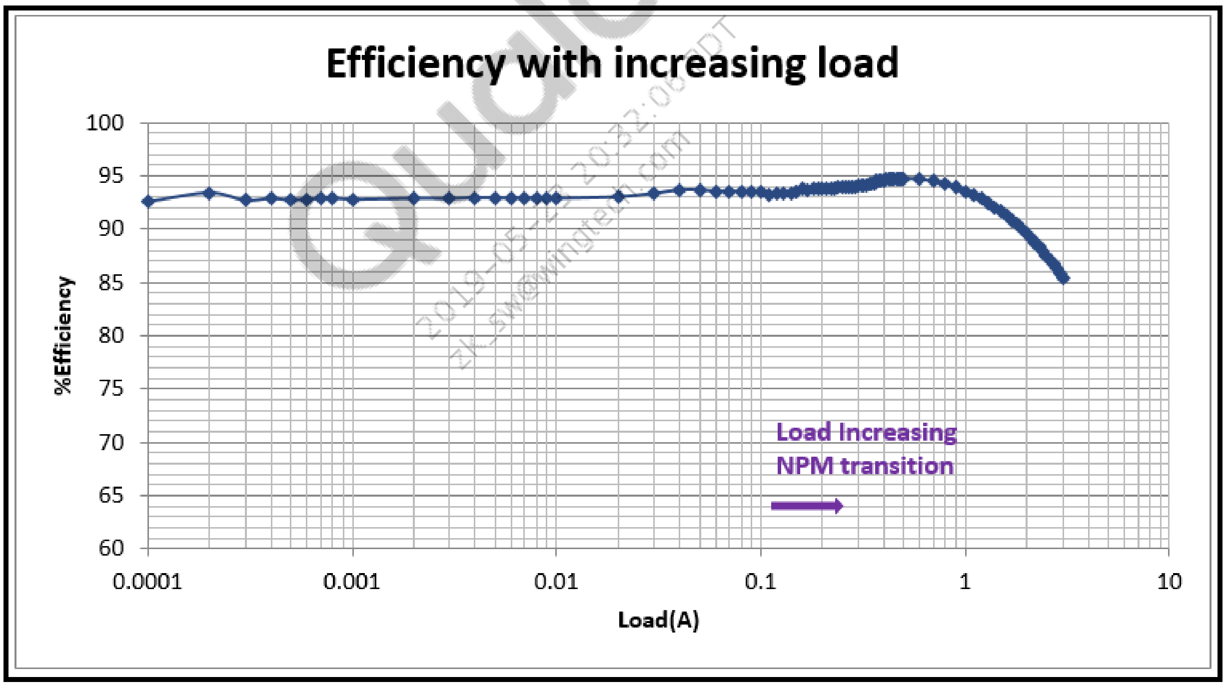


Figure 3-8 S4A efficiency: V_{in} = 3.8 V, V_{out} = 2.04 V (increasing load) auto mode

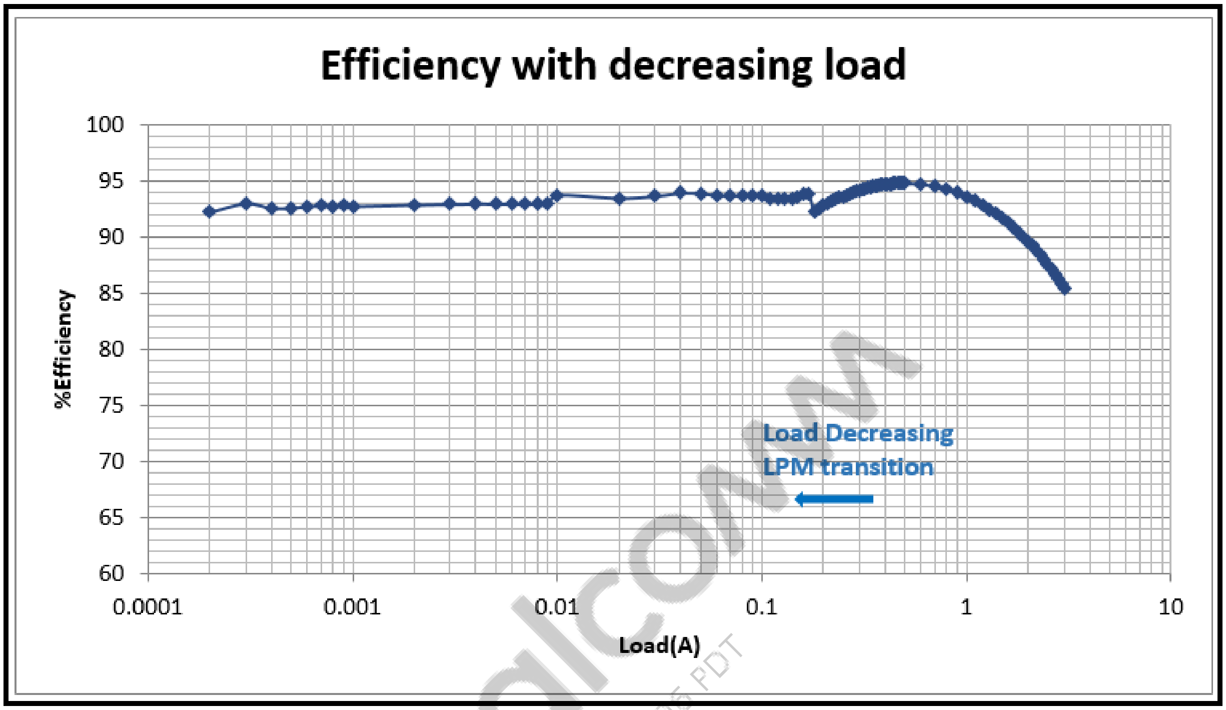


Figure 3-9 S4A efficiency: V_{in} = 3.8 V, V_{out} = 2.04 V (decreasing load) auto mode

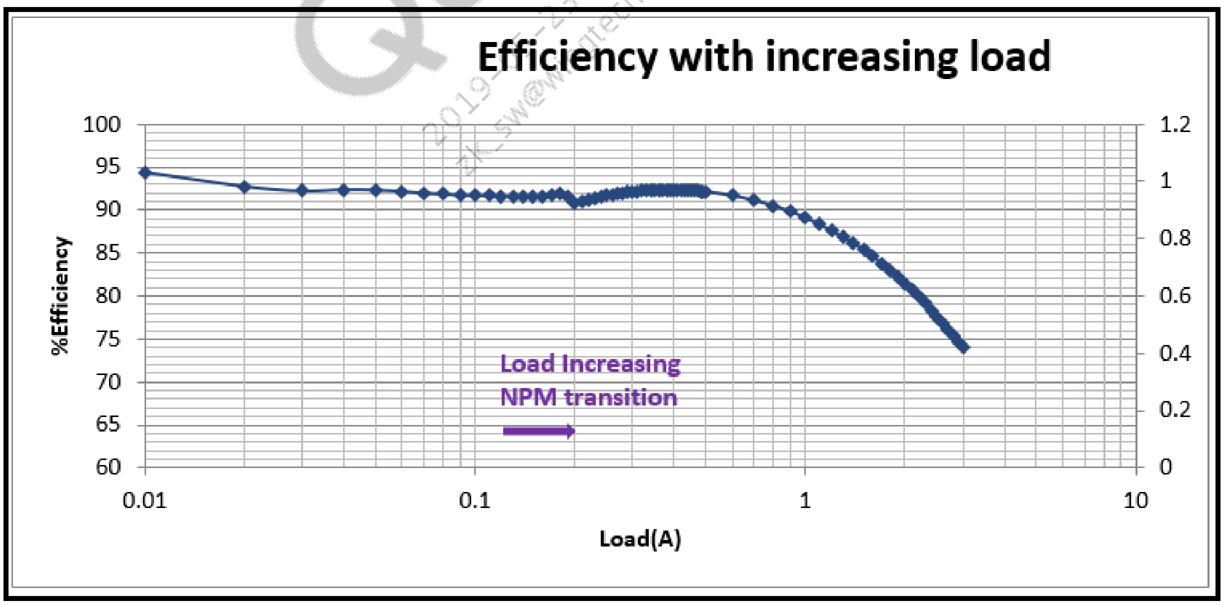


Figure 3-10 S5A efficiency: V_{in} = 3.8 V, V_{out} = 1.35 V (increasing load) auto mode

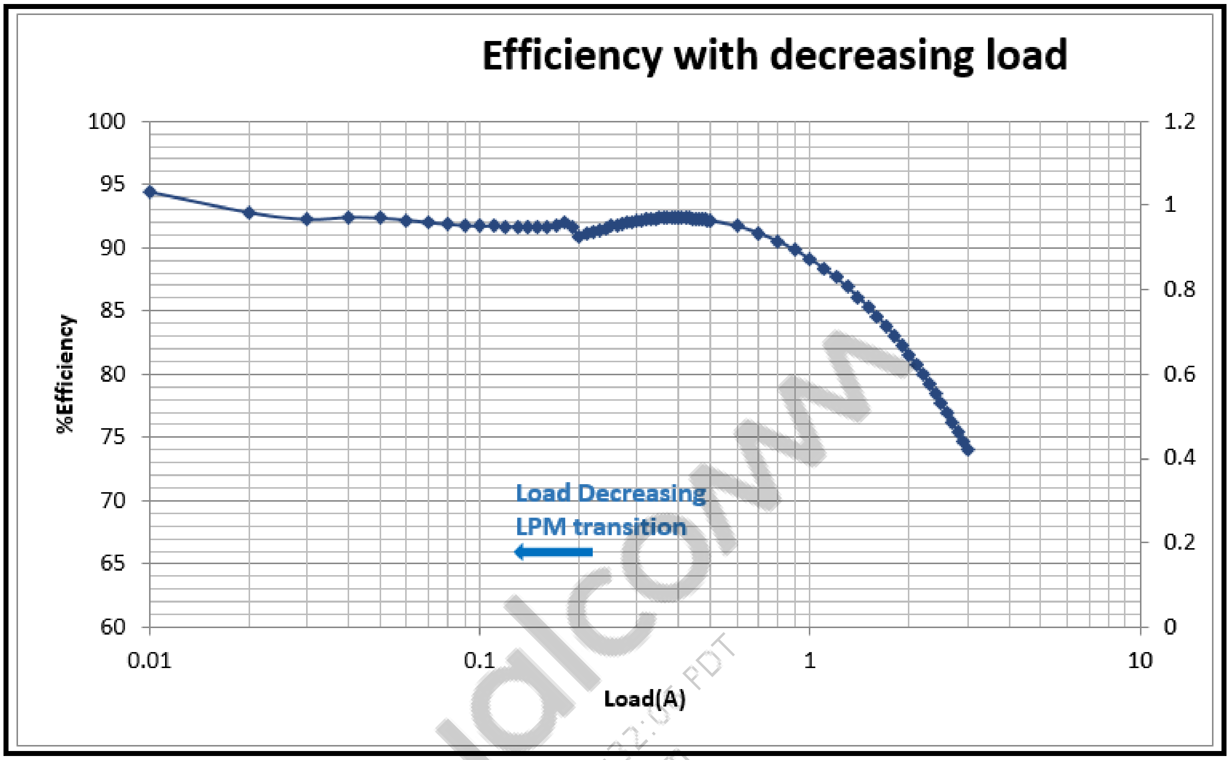


Figure 3-11 S5A efficiency: V_{in} = 3.8 V, V_{out} = 1.35 V (decreasing load) auto mode

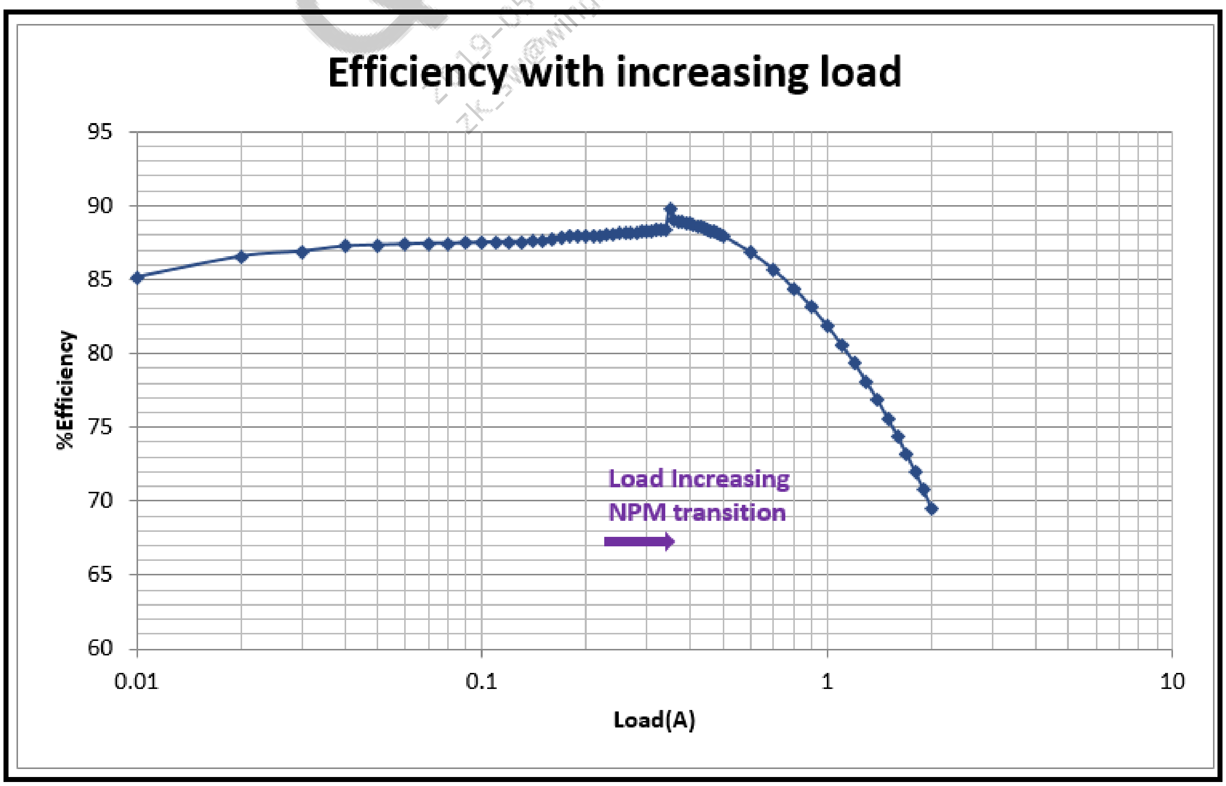


Figure 3-12 S6A efficiency: V_{in} = 3.8 V, V_{out} = 0.87 V (increasing load) auto mode

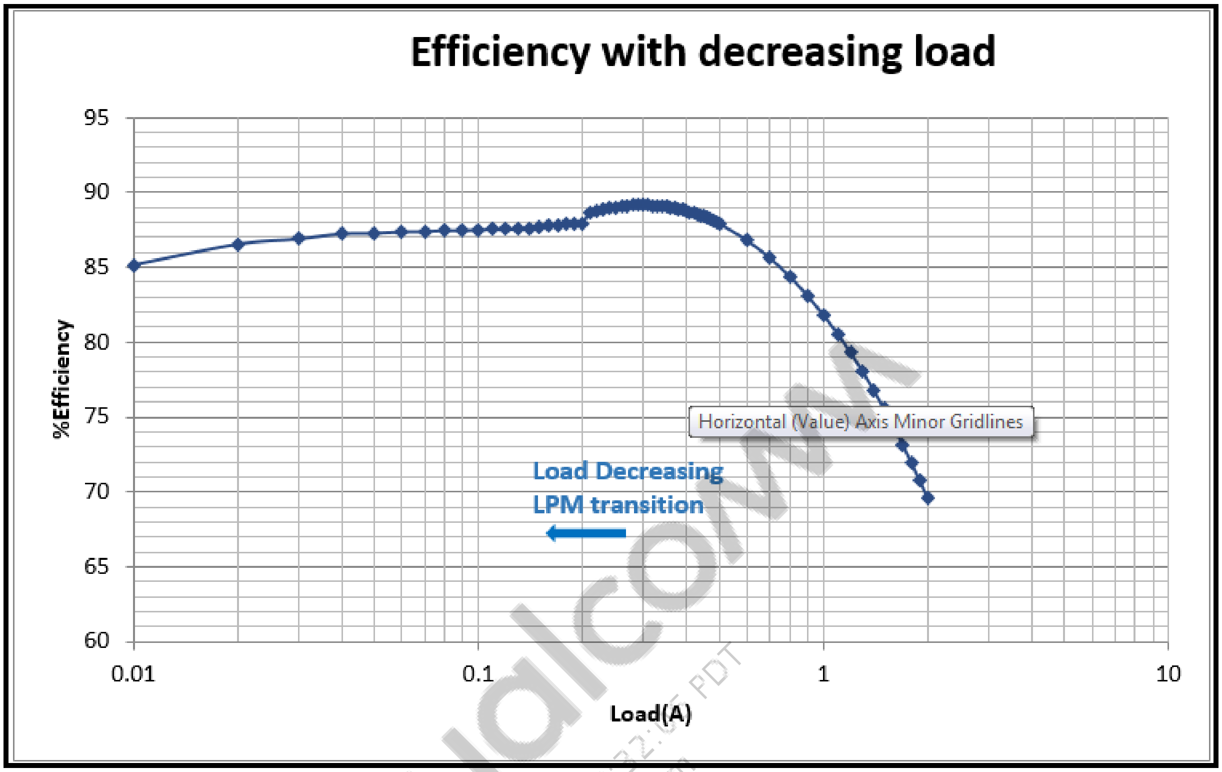


Figure 3-13 S6A efficiency: V_{in} = 3.8 V, V_{out} = 0.87 V (decreasing load) auto mode

3.6.4 FT-SMPS

The PM670 device includes 3 FT-SMPS circuits. All FT-SMPS circuits can be combined for multiphase operation. PWM, PFM, and pulse-skipping modes are supported. New features introduced in the FT-SMPS are autonomous phase control (APC) and autonomous mode control (AMC). APC is where in multiphase operation, the phase count is autonomously managed in the hardware to select the appropriate number of phases for optimal efficiency based on the operative load current. AMC is where hardware manages the selection of PWM or PFM mode based on the operative load current in which the transitions are hardware autonomous. Pertinent **target** performance specifications are given in Table 3-20.

Table 3-20 FT-SMPS generic performance specifications [1]

Parameter	Comments	Min	Typ	Max	Units
General characteristics					
Output voltage range		0.352	–	1.352	V
CMC NPM or AMC NPM, any number of phases					
Rated steady-state load current per phase	Full-sized power stage	4.0	–	–	A
DC output voltage accuracy in CMC NPM or AMC NPM	VREG ≥ 0.8 VREG < 0.8 -30°C to 125°C	-2.0 -16.0	– –	2.0 16.0	% mV

Table 3-20 FT-SMPS generic performance specifications [1] (cont.)

Parameter	Comments	Min	Typ	Max	Units
Ripple voltage CMC NPM or AMC NPM		–	5.0	15.0	mVpp
Line transient response	GSM burst induced line transient represented by: R_{BAT} = 350 mΩ, I_{STEP} = 2 A with 10 µs slew. VPH_PWR capacitance = 100 µF.	–	–	20.0	mVpp
CMC NPM or AMC NPM, multiphase					
Phase current mismatch in multiphase operation	Steady state loading, two or more phases; all active phases in CCM	-25.0	–	25.0	%
Phase current mismatch in multiphase operation at max rated current	Steady state loading, two or more phases; all active phases in CCM	-10.0	–	10.0	%
PWM current limit accuracy	Dynamic current limit as measured by maximum IL during PWM operation	-10.0	–	10.0	%
Ground current					
Ground current CMC NPM	Preliminary projection No load Single phase	–	0.55	0.80	mA
Ground current per phase CMC NPM (multiphase) or AMC NPM	Any number of phases	–	1.9	2.3	mA
Ground current CMC LPM	No load Sleep configuration Any number of phases	–	55.0	90.0	µA
Ground current per phase AMC LPM	No load Nonsleep configuration Any number of phases	–	80.0	110.0	µA
Ground current Retention mode	No load Single phase only	–	1.0	2.0	µA
CMC NPM or AMC load transient, single phase					
Load transient dip/bump voltage disturbance, including any associated mode changes [2]	1 A load step Transient step ~100 ns 1 V output	-40.0	–	70	mV
CMC NPM or AMC load transient, multiphase					
Load transient dip/bump voltage disturbance, including any associated mode or phase-count changes [2]	1.75 A load step per phase Transient step ~100 ns 1 V output	-40.0	–	70	mV

Table 3-20 FT-SMPS generic performance specifications [1] (cont.)

Parameter	Comments	Min	Typ	Max	Units
AMC, any number of phases					
HCPFM ripple voltage	HCPFM transition mode	–	–	70.0	mVpp
CMC LPM or AMC LPM, CPC or APC, any number of phases					
DC output accuracy in CMC LPM or AMC LPM	V_{SET} ≥ 0.8 V V_{SET} < 0.8 V -30°C to 125°C	-2.0 -16.0	– –	4.0 32.0	% mV
DC output voltage accuracy at trimmed set point in CMC LPM or AMC LPM	VREG = trimmed set point -30°C to 125°C	-1.8 -14.4	– –	3.8 30.4	%
PFM ripple voltage CMC LPM or AMC LPM		–	25.0	50.0	mVpp
Transition specifications					
Phase adding warm-up time	NPM CPC change in the phase count	–	25.0	–	µs
Phase current settling time (CMC NPM, CPC)	Steady state loading; all active phases in CCM; change in the phase count	–	–	200	µs
Other general characteristics					
Enable settling time	V_{OUT} slewing to within 1% of final value (includes enable warmup of 40 µs); 40 µs warmup plus V_{SET} slewed at 4.8 mV per µs	–	196.0 at V_{SET} of 0.752 V	–	µs
Voltage stepper dip/bump	One LSB step slewing	-5.0	–	5.0	mV
Discharge impedance	Active strong pull-down enabled	–	32.0	–	Ω

1. Performance is tuned on a domain-by-domain basis for alignment with chipset application requirements. All the specifications are valid for minimum VDD of 3 V
2. Some performance relaxations are possible at VDD < 3 V.

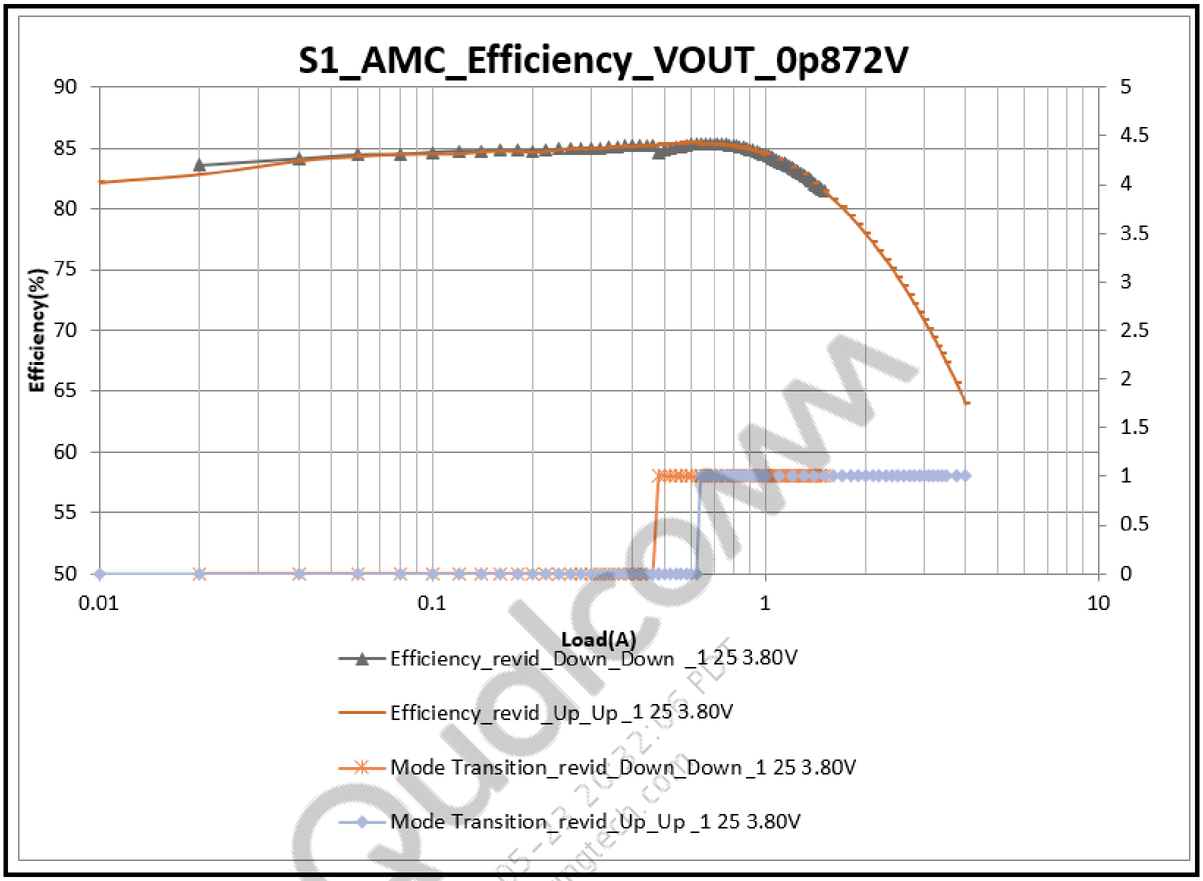


Figure 3-14 S1A efficiency: V_{in} = 3.8 V, V_{out} = 0.872 V

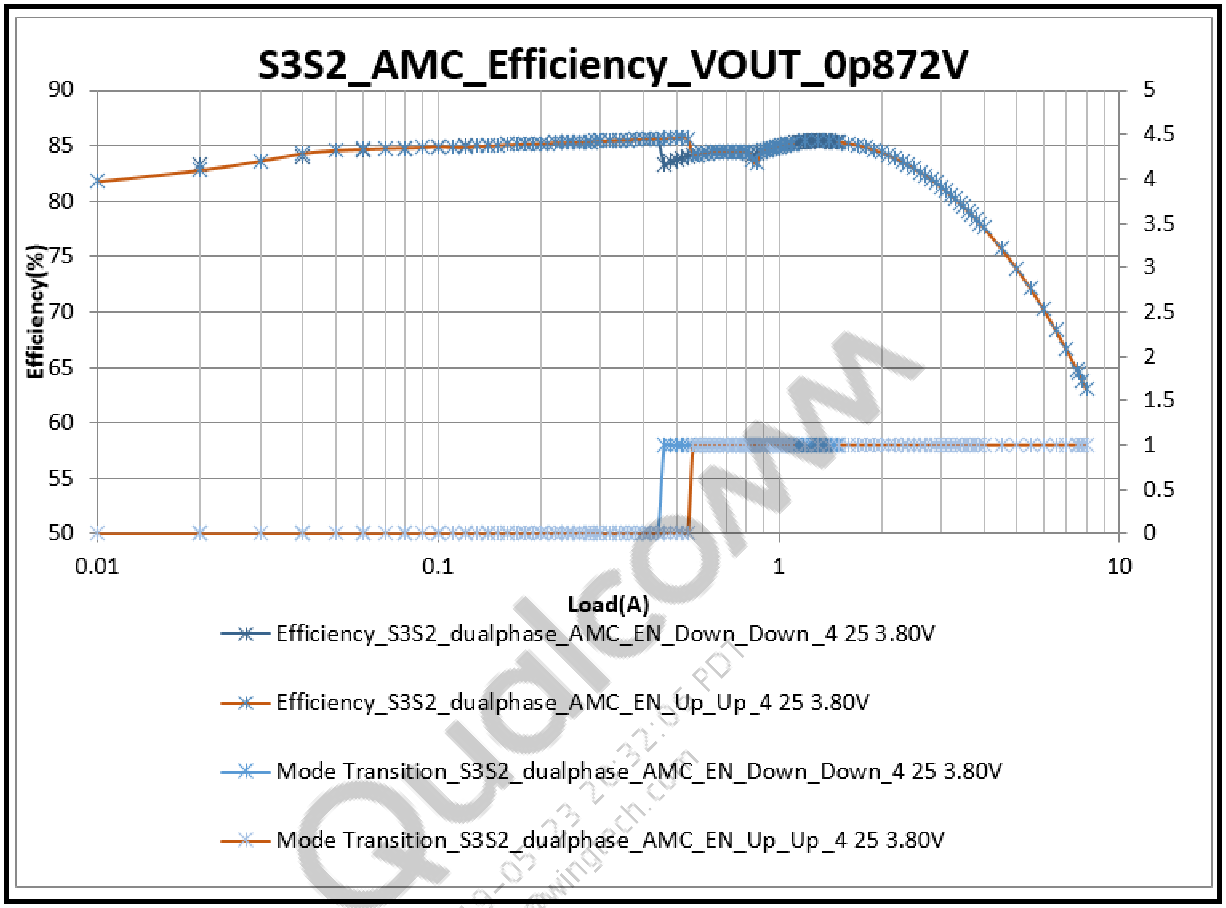


Figure 3-15 S2A/S3A efficiency: V_{in} = 3.8 V, V_{out} = 0.872 V

3.6.5 Linear regulators

19 low dropout (LDO) linear regulator designs are implemented within the PM670/PME605:

- NMOS rated for 600 mA (N600) – four
- NMOS rated for 1200 mA (N1200) – two
- PMOS rated for 50 mA (P50) – one
- PMOS rated for 150 mA (P150) – three
- PMOS rated for 600 mA (P600) – one
- LV-PMOS rated for 600 mA (LVP600) – two
- LV-PMOS rated for 150 mA (LVP150) – three
- LV-PMOS rated for 300 mA (LVP300) – two
- LV-PMOS rated for 50 mA (LVP50) – one

LDO performance specifications are presented in the following tables.

NOTE: The specifications in Table 3-21 for LVPMOS, PMOS, and NMOS LDOS require that the external component and PCB routing parasitics be in compliance with the targeted values listed in the *Understanding Low-Dropout (LDO) Regulators Application Note* (80-VT310-125).

NOTE: All specifications are defined with 100 mV headroom for LVPMOS and NMOS, 500 mV for PMOS (battery connected), and measured at C_{OUT} , unless stated otherwise (an example for the exception would be dropout voltage).

The headroom for subregulated LDOs is defined as V_{SET_BUCK} - V_{SET_LDO}.

For specifications that have multiple contributors, like overall DC error and dropout voltage, refer to the diagrams in the *Understanding Low-Dropout (LDO) Regulators Application Note* (80-VT310-125).

Table 3-21 LVPMOS (subregulated) LDO regulator specifications

Parameter	Comments	Min	Typ	Max	Units
Input voltage range	V_{IN} > 2.1 V degrade device reliability	1.8	–	2.04	V
Output voltage range	Programmable from 1.504 V to 3.544 V	1.504	–	2.0	V
V_{OUT} step size	–	–	8	–	mV
Normal power mode					
Rated load current [1] LV P150 LV P300 LV P600	Maximum load current at which all specifications are met. HR = 160 mV. Higher load current is possible at increased headroom.	 150 300 600	 – – –	 – – –	 mA mA mA
Overall DC error at default voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error) [2]	Measured at C_{OUT}. HR = 160 mV Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (1.2% + 6 mV + 15 mV)	–	+1.2%	–
Overall DC error at nondefault voltage (includes load and line regulation, temperature, VBAT, MBG, variation, and trim error) [2]	Measured at C_{OUT} HR = 160 mV Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (2% + 6 mV + 15 mV)	–	+2%	–
Load transient, undershoot, overshoot [3] [4]	Load step of 0.5 × I_{RATED} in 1 µs, with baseline current of 0.1 × I_{RATED} to 0.5 × I_{RATED}. HR = 160 mV. Compared to the final settled value.	-40	–	70	mV
Start-up settling time [5]	To within 1% of the final value	90	200	300	µs
Start-up in-rush current	During start-up. V_{SET} = 1.8 V LV P150 LV P300 LV P600	 – – –	 50 50 170	 250 400 700	 mA mA mA
Dropout voltage [6]	From parent buck C_{OUT} to LDO sense point; load at I_{RATED}	–	–	85	mV
Load regulation	I_{LOAD} = I_{RATED}/100 to I_{RATED}. HR = 160 mV, measured at C_{OUT}. Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	–	–	0.3% + 6 mV + 15 mV	–
Line regulation	Based on VBAT from 3 V to 5 V. HR = 160 mV. For V_{OUT} ≥ 0.5 V	–	–	0.1	%/V

Table 3-21 LVPMOS (subregulated) LDO regulator specifications

Parameter	Comments	Min	Typ	Max	Units
Over current protection detection threshold (I_{OCP})	Threshold for OCP detection. OCP interrupt and self-shutdown are based on tripping this threshold. LVP150 LVP300 LVP600	 350 700 1100	 400 800 1500	 450 900 1850	 mA mA mA
Short circuit current limit	Maximum current LDO will output when shorted to ground.	2x	2x	2x	I_{OCP}
Short circuit current limit test mode	Maximum current LDO will output when shorted to ground in test mode.	0.12x	0.12x	0.12x	I_{OCP}
Output noise density	HR = 160 mV; measured at C_{OUT} LDO contribution only, assumes clean V_{IN} 100 Hz ≤ f 1 kHz 1 kHz ≤ f ≤ 10 kHz 10 kHz ≤ f ≤ 100 kHz 100 kHz ≤ f 1 MHz	 – – – –	 5 1.7 0.65 0.25	 – – – –	$\mu V/\sqrt{Hz}$
PSRR	From V_{IN} to V_{OUT}; measured at C_{OUT} (HR = 160 mV, I_{LOAD} = I_{RATED}) 50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	 40 25 20 5	 50 30 25 15	 – – – –	 dB dB dB dB
	From V_{IN} to V_{OUT}; measured at C_{OUT} (HR = 80 mV, I_{LOAD} = I_{RATED}/2) 50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	 35 20 15 0	 40 25 20 10	 – – – –	 dB dB dB dB
	From V_{IN} to V_{OUT}; measured at C_{OUT} (HR = 40 mV, I_{LOAD} = I_{RATED}/4) 50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	 30 15 10 0	 35 20 15 5	 – – – –	 dB dB dB dB
Ground current, no load	Measured at the battery. I_Q may be much higher if LDO is operated in drop-out condition.	–	80	100	μA
Low-power mode					
Rated load current [1]	–	10	–	–	mA

Table 3-21 LVPMOS (subregulated) LDO regulator specifications

Parameter	Comments	Min	Typ	Max	Units
Overall DC error at default voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error) [2]	Measured at C_{OUT} Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (2.7% + 0.1 mV + 0.25 mV)	–	+2.7%	–
Overall DC error at non default voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error) [2]	Measured at C_{OUT} Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (3.7% + 0.1 mV + 0.25 mV)	–	+3.7%	–
Load transient, undershoot, overshoot	Load step of 0.5 × I_{RATED} in 1 µs, with baseline current of 0.01 × I_{RATED} to 0.5 × I_{RATED}. HR = 160 mV. Compared to the final settled value.	-40	–	70	mV
Dropout voltage	From parent buck C_{OUT} to LDO sense point. Load at I_{RATED}.	–	–	15	mV
Load regulation	I_{LOAD} = I_{RATED}/100 to I_{RATED}. HR = 160 mV, measured at C_{OUT}. Format: X + Y + Z X = Performance at LDO sense point Y = On-die routing DCR contribution Z = PCB routing DCR contribution	–	–	1.5% + 0.1 mV + 0.25 mV	–
Line regulation	Based on VBAT from 3.4 V to 4.75 V.	–	–	0.5	%/V
Over current protection detection threshold (I_{OCP})	Threshold for OCP detection. OCP interrupt and self-shutdown are based on tripping this threshold.	30	50	90	mA
Short-circuit current limit	Max current LDO outputs when shorted to ground.	1.3x	1.3x	1.3x	I_{OCP}
Power supply ripple rejection ratio (PSRR)	From V_{IN} to V_{OUT}; measured at C_{OUT} (HR = 160 mV, I_{LOAD} = LPM I_{RATED} 50 Hz to 100 kHz	30	35	–	dB
Ground current, no load [7]	Measured at the battery. I_Q may much be higher if LDO is operated in drop-out condition. Excludes FF/125 corner (20 µA).	–	6.5	8	µA
Normal and low-power mode					
NPM: LPM overshoot and undershoot	HR = 160 mV, Measured at C_{OUT}. Iload = LPM I_{RATED}	-40	–	70	mV
NPM: Bypass overshoot and undershoot	Measured at C_{OUT}. Iload = NPM I_{RATED}. Bypass entry: V_{IN} lowered to LDO V_{SET} Bypass exit: V_{IN} increased to LDO V_{SET} + 160 mV	-40	–	70	mV

Table 3-21 LVPMOS (subregulated) LDO regulator specifications

Parameter	Comments	Min	Typ	Max	Units
LPM: Bypass overshoot and undershoot	Measured at C_{OUT}. Iload = LPM I_{RATED}. Bypass entry: V_{IN} lowered to LDO V_{SET} Bypass exit: V_{IN} increased to LDO V_{SET} + 160 mV	-40	–	70	mV
Analog auto bypass entry/exit overshoot and undershoot	Starting HR = 40 mV, HR = 0, HR = 110 mV. Ramp rate=100 mV/µs during transition. I_{LOAD} = I_{RATED}. Compared to final settled value.	-40	–	70	mV
Ground current, with load	% of the load current. Closer to UL during light load and low HR condition.	–	0.4	0.8	% I_{LOAD}
LDO discharge time to below 100 mV	Strong pull-down enabled. UL is with maximum C_{OUT}. LVP600 LVP300 and LVP150	– 	 0.3 0.07	 2.5 0.5	 ms ms
VREG_OK threshold		85%	90%	95%	V_{OUT}
Bypass mode					
Ground current [8]		–	0.25	1	µA
LVP150 on resistance	From input capacitor (buck C_{OUT}) to LDO output cap. Format: X + Y + Z X = LDO contribution Y = on-die routing DCR, top level Z = PCB routing DCR	–	–	480 + 80 + 140 = 700	mΩ
LVP300 on resistance		–	–	240 + 40 + 70 = 350	mΩ
LVP600 on resistance		–	–	120 + 20 + 35 = 175	mΩ

1. The rated current is the current at which the regulator meets all specifications. Higher currents can be allowed, but the regulator may need more headroom (the difference between V_{IN} and V_{OUT}. For low-power mode, the user should switch the LDO to normal power mode if the load current is expected to be above the rated current.
2. At high temperature and some process corners, the pass device leakage causes the output voltage to float up under no-load conditions. The leakage pull-down may need to be enabled to meet the specification.
3. Overshoot and undershoot (load transient) scale linearly with load step. For example, PMOS LDO in normal power mode will have an overshoot/undershoot of 35 mV/-25 mV for a 0.01 × I_{RATED} to 0.5 × I_{RATED} load step with 100 ns rise/fall time.
4. Overshoot and undershoot (load transient) specifications can be met with the recommended load capacitance and as the output voltage changes under the following conditions:
   - $V_{IN} > V_{OUT}$ + 0.5 V
   - Load changes from I_{RATED}/100 to I_{RATED} within 1 µs rise/fall time

   Overshoot and undershoot (other conditions) specifications can be met with the recommended load capacitance and when $V_{IN} > V_{OUT}$ + 0.5 V under the following conditions:
   - Line change by 1 V
   - LPM to NPM transitions
   - LDO start-ups
5. The settling time is for start-up and any upward voltage change with the rated load capacitance. Time is increased with larger load capacitance. Settling time of a downward voltage change depends on the load current.

6. Dropout voltage is defined as follows:
   a. Apply the specified load current.
   b. Set $V_{IN} = V_{OUT} + 0.5$ V.
   c. Measure the output voltage.
   d. Reduce V_{IN} until V_{OUT} is reduced by 100 mV.
   e. Calculate dropout voltage as $V_{IN} - V_{OUT}$ in this condition.
7. The low-power mode no-load ground current may be higher due to the current limiting mistrigger in the low-headroom configuration. Disabling the current limiting feature or giving enough headroom as of the dropout requirement can prevent mistriggering and reduce the ground current
8. In bypass mode, there is an active gate to source clamp to protect the LV PMOS.

Table 3-22 PMOS (battery connected) LDO regulator specifications

Parameter	Comments	Min	Typ	Max	Units
Input voltage range		2.5	–	5.5	V
Output voltage range		1.504	–	3.544	V
V_{OUT} step size		–	8	–	mV
Normal power mode					
Rated load current [1]	Max load current at which all specifications are met. Higher load current is possible at increased headroom.				
P50		50	–	–	mA
P150		150	–	–	mA
P300		300	–	–	mA
P600		600	–	–	mA
Maximum PASSFET power dissipation	–	–	–	600	mW
Overall DC error at default voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error) [2]	Measured at C_{OUT} Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (1% + 6 mV + 15 mV)	–	+1%	–
Overall DC error at non default voltages (includes load and line regulation, temperature, VBAT, MBG variation, and trim error) [2]	Measured at C_{OUT} Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (2% + 6 mV + 15 mV)	–	+2%	–
Load transient, undershoot, overshoot [3, 4]	Load step of 0.5 × I_{RATED} in 1 µs, with baseline current of 0.01 x I_{RATED} to 0.5 × I_{RATED}. HR = 500 mV. Compared to final settled value.	-50	–	70	mV
Start-up settling time [5]	To within 1% of final value V_{OUT} = 3.3 V. UL is with max C_{OUT}.	150	–	500	µs

Table 3-22 PMOS (battery connected) LDO regulator specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Start-up in-rush current	During start-up. V_{SET} = 3.3 V.				
	P50	–	30	250	mA
	P150	–	25	300	mA
	P300	–	40	400	mA
	P600	–	150	800	mA
Dropout voltage [6]	From parent buck C_{OUT} to LDO sense point. Load at I_{RATED}.	–	–	300	mV
Load regulation	I_{LOAD} = I_{RATED}/100 to I_{RATED}. HR = 500 mV, measured at C_{OUT}. Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	–	–	0.3% + 6 mV + 15 mV	–
Line regulation	Based on V_{BAT} from 3 V to 5 V. HR = 500 mV	–	–	0.1	%/V
Over current protection detection threshold (I_{OCP})	Threshold for OCP detection. OCP interrupt and self-shutdown are based on tripping this threshold.				
	P50	75	100	150	mA
	P150	225	325	425	mA
	P300	450	650	700	mA
	P600	900	1200	1400	mA
Short-circuit current limit	Maximum current LDO will output when shorted to ground.	2x	2x	2x	I_{OCP}
Short circuit current limit test mode	Max current LDO will output when shorted to ground in test mode.	–	0.12x	–	I_{OCP}
Output noise density	HR = 500 mV. Measured at C_{OUT} LDO contribution only, assumes clean V_{IN}				$\mu V/\sqrt{Hz}$
	100 Hz ≤ f ≤ 1 kHz	–	11	–	
	1 kHz ≤ f ≤ 10 kHz	–	3.5	–	
	10 kHz ≤ f ≤ 100 kHz	–	1.2	–	
	100 kHz ≤ f ≤ 1 MHz	–	0.7	–	

Table 3-22 PMOS (battery connected) LDO regulator specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
PSRR	From V_{IN} to V_{OUT}; measured at C_{OUT} (HR = 500 mV, $I_{LOAD} = I_{RATED}$) 50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	 40 30 25 10	 45 35 30 20	 – – – –	 dB dB dB dB
	From V_{IN} to V_{OUT}; measured at C_{OUT} (HR = 300 mV, $I_{LOAD} = I_{RATED}$) 50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	 30 20 20 5	 35 25 25 15	 – – – –	 dB dB dB dB
Ground current, no load	Measured at the battery. I_Q may be much higher if LDO is operated in a dropout condition.	–	85	120	µA
Low-power mode					
Rated load current		10	–	–	mA
Overall DC error at default voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error) [2]	Measured at C_{OUT} Format: X + Y + Z X = performance at LDO sense point Y= on-die routing DCR contribution Z= PCB routing DCR contribution	- (2.7% + 0.1 mV + 0.25 mV)	–	+2.7%	–
Overall DC error at non default voltages (includes load and line regulation, temperature, VBAT, MBG variation, and trim error) [2]	Measured at C_{OUT} Format: X + Y + Z X = performance at LDO sense point Y= on-die routing DCR contribution Z= PCB routing DCR contribution	- (3.7% + 0.1 mV + 0.25 mV)	–	+3.7%	–
Load transient undershoot, overshoot [3, 4]	Load step of 0.5 × I_{RATED} in 1 µs, with baseline current of 0.01 x I_{RATED} to 0.5 × I_{RATED}. HR = 500 mV. Compared to final settled value.	-40	–	70	mV
Dropout voltage	From parent buck C_{OUT} to LDO sense point. Load at I_{RATED}	–	35	80	mV
Load regulation	$I_{LOAD} = I_{RATED}/100$ to I_{RATED}. HR = 500 mV, measured at C_{OUT}. Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	–	–	1.5% + 0.1 mV + 0.25 mV	–
Line regulation	Based on V_{BAT} from 3.4 V to 4.75 V.	–	–	0.5	%/V
Overcurrent protection detection threshold	Threshold for OCP detection. OCP interrupt and self-shutdown are based on tripping this threshold.	20	30	50	mA

Table 3-22 PMOS (battery connected) LDO regulator specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Short-circuit current limit	Maximum current LDO will output when shorted to ground.	1.3x	1.3x	1.3x	I_{OCP}
PSRR	From V_{IN} to V_{OUT}. Measured at C_{OUT}. (HR = 500 mV, I_{LOAD} = I_{RATED}).				
	50 Hz to 1 kHz	35	40	–	–
	1 kHz to 10 kHz	30	30	–	–
	10 kHz to 100 kHz	30	30	–	–
	100 kHz to 1 MHz	20	30	–	–
Ground current, no load [7]	Measured at the battery. I_Q may much be higher if LDO is operated in the dropout condition. Excludes FF/125 corner (20 µA)	–	6.5	8	µA
Normal and low-power mode					
NPM: LPM overshoot and undershoot	HR = 500 mV, measured at C_{OUT}. Iload = LPM I_{RATED}	-40	–	70	mV
Analog auto bypass entry/exit overshoot and undershoot	Starting HR = 500 mV, HR = 0 (for 500 µs), HR = 500 mV. Ramp rate=100 mV/µs during transition. I_{LOAD} = I_{RATED}. Compared to the final settled value.	-40	–	70	mV
Ground current, with load	% of the load current. Closer to UL during light load and low HR condition.	–	0.4	0.8	% I_{LOAD}
LDO discharge time to below 100 mV	Strong pull down enabled. UL is with max C_{OUT}.				
	P600	–	–	3	ms
	P300, P150, P50	–	–	1.3	ms
VREG_OK threshold	–	85%	90%	95%	V_{OUT}
Bypass mode					
Ground current [8]	–	–	0.5	1	µA
P50 on resistance	From input capacitor (BBYP or BoB C_{OUT}) to LDO output capacitor. Format: X + Y + Z X = LDO contribution Y = on-die routing DCR, top level Z = PCB routing DCR	–	–	5.04 + 0.24 + 0.6 = 5.88	Ω
P150 on resistance		–	–	1.68 + 0.08 + 0.2 = 1.96	Ω
P300 on resistance		–	–	0.84 + 0.04 + 0.1 = 0.98	Ω
P600 on resistance		–	–	0.42 + 0.02 + 0.05 = 0.49	Ω

1. The rated current is the current at which the regulator meets all specifications. Higher currents can be allowed, but the regulator may need more headroom (the difference between V_{IN} and V_{OUT}). For low-power mode, the user should switch the LDO to normal power mode if the load current is expected to be above the rated current.

2. At high temperature and some process corners, the pass device leakage causes the output voltage to float up under no-load conditions. The leakage pull-down may need to be enabled to meet the specification.
3. Overshoot and undershoot (load transient) scale linearly with load step. For example, PMOS LDO in normal power mode will have an overshoot/undershoot of 35 mV/-25 mV for a 0.01 × I_{RATED} to 0.5 × I_{RATED} load step with 100 ns rise/fall time.
4. Overshoot and undershoot (load transient) specifications can be met with the recommended load capacitance and as the output voltage changes under the following conditions:
   - $V_{IN} > V_{OUT} + 0.5$ V
   - Load changes from $I_{RATED}/100$ to I_{RATED} within 1 µs rise/fall time

   Overshoot and undershoot (other conditions) specifications can be met with the recommended load capacitance and when $V_{IN} > V_{OUT} + 0.5$ V under the following conditions:
   - Line change by 1 V
   - LPM to NPM transitions
   - LDO start-ups
5. The settling time is for start-up and any upward voltage change with the rated load capacitance. Time is increased with larger load capacitance. Settling time of a downward voltage change depends on the load current.
6. Dropout voltage is defined as follows:
   a. Apply the specified load current.
   b. Set $V_{IN} = V_{OUT} + 0.5$ V.
   c. Measure the output voltage.
   d. Reduce V_{IN} until V_{OUT} is reduced by 100 mV.
   e. Calculate dropout voltage as $V_{IN} - V_{OUT}$ in this condition.
7. The low-power mode no-load ground current may be higher due to the current limiting mistrigger in the low-headroom configuration. Disabling the current limiting feature or giving enough headroom as of the dropout requirement can prevent mistriggering and reduce the ground current.
8. In bypass mode, there is an active gate to source clamp to protect the LV PMOS.

Table 3-23 NMOS LDO regulator specifications

Parameter	Comments	Min	Typ	Max	Units
Input voltage range		0.32	–	1.4	V
Output voltage range	Programmable from 0.312 V to 1.328 V	0.32	–	1.304	V
V_{OUT} step size		–	8	–	mV
Normal power mode					
Rated load current [1] N300 N600 N1200	Maximum load current at which all specifications are met. HR = 160 mV. Higher load current is possible at increased headroom.	 300 600 1200	 – – –	 – – –	 mA mA mA
Overall DC error at default voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error) [2]	Assume default voltage ≥ 0.8 V; measured at C_{OUT} HR = 160 mV Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (1.3% + 12 mV + 30 mV)	–	+1.3%	–
Overall DC error at non default voltages (includes load and line regulation, temperature, VBAT, MBG variation, and trim error) [2]	For V_{OUT} ≥ 0.5 V, up to I_{RATED}; measured at C_{OUT} HR = 160 mV Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (2% + 12 mV + 30 mV)	–	+2%	
	For V_{OUT} < 0.5 V, up to $I_{RATED}/4$. Measured at C_{OUT} HR = 160 mV Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (10 + 3 + 8)	–	10	mV
Load transient undershoot, overshoot [3, 4]	Load step of 0.5 × I_{RATED} in 1 µs, with baseline current of 0.01 × I_{RATED} or higher. HR = 160 mV. Compared to final settled value.	-40	–	70	mV
Start-up settling time [5]	To within 1% of the final value	80	140	200	µs
Start-up in-rush current	During start up. Variation due to the bulk capacitor size. N300 N600 N1200	 – – –	 40 80 160	 400 800 900	 mA mA mA
Dropout voltage [6]	From parent buck C_{OUT} to LDO sense point. Load at I_{RATED} For V_{PH} ≥ 3 V For V_{PH} < 3 V	 – –	 – –	 85 95	 mV mV

Table 3-23 NMOS LDO regulator specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Load regulation	$I_{LOAD} = I_{RATED}/100$ to I_{RATED}. HR = 160 mV, Measured at C_{OUT}. Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	–	–	0.3% + 12 mV + 30 mV	–
Line regulation	Based on VBAT from 3 V to 5 V. HR = 160 mV. For V_{OUT} >=0.5 V	–	–	0.1	%/V
Short circuit current limit and OCP detection threshold N300	The maximum current LDO will output when shorted to ground.	400	550	900	mA
Short-circuit current limit and OCP detection threshold N600	The maximum current LDO will output when shorted to ground.	800	1100	1800	mA
Short-circuit current limit and OCP detection threshold N1200	The maximum current LDO will output when shorted to ground.	1800	2400	3300	mA
Short circuit current limit test mode	The maximum current LDO will output when shorted to ground in test mode.	–	110	–	mA
Output noise density	HR = 160 mV; measured at C_{OUT} LDO contribution only, assumes clean V_{IN}. 100 Hz ≤ f 1 kHz 1 kHz ≤ f ≤ 10 kHz 10 kHz ≤ f ≤ 100 kHz 100 kHz ≤ f 1 MHz	 – – – –	 3 1.5 1.2 0.5	 – – – –	$\mu V/\sqrt{Hz}$
PSRR	From V_{IN} to V_{OUT}. Measured at C_{OUT} (HR = 160 mV, $I_{LOAD} = I_{RATED}$). 50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	 50 35 30 15	 70 55 45 30	 – – – –	 dB dB dB dB
	From V_{IN} to V_{OUT}. Measured at C_{OUT} (HR = 80 mV, $I_{LOAD} = I_{RATED}/2$). 50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	 40 25 20 10	 50 35 30 25	 – – – –	 dB dB dB dB
	From V_{IN} to V_{OUT}. Measured at C_{OUT} (HR = 40 mV, $I_{LOAD} = I_{RATED}/4$). 50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	 30 15 15 5	 40 25 20 20	 – – – –	 dB dB dB dB
Ground current, no load	Measured at the battery. I_Q may be much higher if LDO is operated in drop-out condition.	–	95	110	µA

Table 3-23 NMOS LDO regulator specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Low-power mode					
Rated load current [1]	Maximum load current at which all specifications are met. Higher load current is possible at increased headroom	30	–	–	mA
Overall DC error at default voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error) [2]	Assume default voltage ≥ 0.8 V; measured at C_{OUT} Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (2.5% + 1.2 mV + 3 mV)	–	+2.5%	–
Overall DC error at non default voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error) [2]	For V_{OUT} ≥ 0.5 V, up to I_{RATED}; Measured at C_{OUT} Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (3% + 1.2 mV + 3 mV)	–	+3%	–
	For V_{OUT} < 0.5 V, up to I_{RATED}/4; measured at C_{OUT}	-20	–	20	mV
Load transient, undershoot, overshoot [3, 4]	Load step of 0.5 × I_{RATED} in 1 µs, with baseline current of 0.1 × I_{RATED} or higher. HR = 160 mV. Compared to the final settled value.	-40	–	70	mV
Dropout voltage	From package V_{IN} pin to V_{OUT} pin. Load at I_{RATED}	–	–	85	mV
Load regulation	I_{LOAD} = I_{RATED}/100 to I_{RATED}. HR = 160 mV, Measured at C_{OUT}. Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	–	–	1% + 1.2 mV + 3 mV	–
Line regulation	Based on V_{BAT} from 3.4 V to 4.75 V.	–	–	0.5	%/V
Short circuit current limit and OCP detection threshold	Maximum current LDO will output when shorted to ground.	75	–	250	mA
Ground current, no load [7]	Measured at the battery. I_Q may much be higher if LDO is operated in drop-out condition.	–	20	23	µA
Normal and low-power mode					
NPM: LPM overshoot and undershoot	HR = 160 mV, measured at C_{OUT}. Iload = LPM I_{RATED} Vph > 3 V Vph > 3 V	 -40 -40	 – –	 70 100	 mV mV

Table 3-23 NMOS LDO regulator specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
NPM: Bypass overshoot and undershoot	Measured at C_{OUT}. Iload = NPM I_{RATED}. Bypass entry: V_{IN} lowered to LDO V_{SET} Bypass exit: V_{IN} increased to LDO V_{SET} +160 mV	-40	–	70	mV
LPM: Bypass overshoot and undershoot	Measured at C_{OUT}. Iload = LPM I_{RATED}. Bypass entry: V_{IN} lowered to LDO V_{SET} Bypass exit: V_{IN} increased to LDO V_{SET} + 160 mV	-40	–	70	mV
Analog auto bypass entry/exit overshoot and undershoot	Starting HR = 40 mV, HR = 0, HR = 110 mV. Ramp rate=100 mV/µs during transition. I_{LOAD} = I_{RATED}. Compared to final settled value.	-40	–	70	mV
Ground current, with load	% of the load current	–	–	0.5	% I_{LOAD}
LDO discharge time to below 100 mV	Nominal load capacitor and strong pull-down enabled	–	0.1	2	ms
VREG_OK threshold		85%	90%	95%	V_{OUT}
Bypass mode					
Ground current [8]		–	2	5	µA
N300 on resistance	From input cap (buck C_{OUT}) to LDO output cap. Format: X+Y+Z X = LDO contribution Y = on-die routing DCR, top level Z = PCB routing DCR	–	–	280 + 80 + 140 = 500	mΩ
N600 On resistance		–	–	140 + 40 + 70 =250	
N1200 on resistance		–	–	70 + 20 + 35 =125	

1. The rated current is the current at which the regulator meets all specifications. Higher currents can be allowed, but the regulator may need more headroom (the difference between V_{IN} and V_{OUT}). For low-power mode, the user should switch the LDO to normal power mode if the load current is expected to be above the rated current.
2. At high temperature and some process corners, the pass device leakage causes the output voltage to float up under no-load conditions. The leakage pull-down may need to be enabled to meet the specification.
3. Overshoot and undershoot (load transient) scale linearly with load step. For example, PMOS LDO in normal power mode will have an overshoot/undershoot of 35 mV/-25 mV for a 0.01 × I_{RATED} to 0.5 × I_{RATED} load step with 100 ns rise/fall time.
4. Overshoot and undershoot (load transient) specifications can be met with the recommended load capacitance and as the output voltage changes under the following conditions:
   - $V_{IN} > V_{OUT} + 0.5$ V
   - Load changes from I_{RATED}/100 to I_{RATED} within 1 µs rise/fall time

   Overshoot and undershoot (other conditions) specifications can be met with the recommended load capacitance and when $V_{IN} > V_{OUT} + 0.5$ V under the following conditions:
   - Line change by 1 V
   - LPM to NPM transitions
   - LDO start-ups
5. The settling time is for start-up and any upward voltage change with the rated load capacitance. Time is increased with larger load capacitance. Settling time of a downward voltage change depends on the load current.

6. Dropout voltage is defined as follows:
   a. Apply the specified load current.
   b. Set $V_{IN} = V_{OUT} + 0.5$ V.
   c. Measure the output voltage.
   d. Reduce V_{IN} until V_{OUT} is reduced by 100 mV.
   e. Calculate dropout voltage as $V_{IN} - V_{OUT}$ in this condition.
7. The low-power mode no-load ground current may be higher due to the current limiting mistrigger in the low-headroom configuration. Disabling the current limiting feature or giving enough headroom as of the dropout requirement can prevent mistriggering and reduce the ground current
8. In bypass mode, there is an active gate to source clamp to protect the LV PMOS.

Table 3-24 LDO2A, LDO5A, LDO6A, and LDO7A NMOS regulator specifications

Parameter	Test condition or comment	Min	Typ	Max	Units
Input voltage range		0.312	–	1.4	V
Output voltage range	Programmable from 0.312 to 1.328	0.312	–	1.304	V
V_{out} step size		–	8	–	mV
Normal power mode					
Rated load current [1] N300 N600 N1200	Max load current at which all specifications are met. HR = 100 mV. Higher load current is possible at increased headroom	300 600 1200	– – –	– – –	mA mA mA
Overall DC error at default voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error) [2]	Assume default voltage ≥ 0.8 V. Measured at C_{out}. HR = 100 mV. Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (1.3% + 12 mV + 30 mV)	–	1.3%	–
Overall DC error at non-default voltage (includes load and line regulation, temperature, VBAT, MBG variation, and trim error) [2]	For V_{out} ≥ 0.5 V, up to I_{RATED}. Measured at C_{out}. HR = 100 mV. Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (2% + 12 mV + 30 mV)	–	2%	–
	For V_{out} < 0.5 V, up to I_{RATED}/4. Measured at C_{out}. HR = 100 mV. Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (10 + 3 + 8)	–	10	mV
Load transient undershoot, overshoot	Load step of 0.5 × I_{RATED} in 1 µs, with baseline current of 0.1 × I_{RATED} or higher. HR = 100mV. Compared to the final settled value.	-40	–	70	mV
Startup settling time [3]	To within 1% of final value	40	140	200	µs

Table 3-24 LDO2A, LDO5A, LDO6A, and LDO7A NMOS regulator specifications (cont.)

Parameter	Test condition or comment	Min	Typ	Max	Units
Startup in-rush current	During start-up. Variation due to bulk cap size N300 N600 N1200	 – – –	 40 80 160	 400 800 900	mA
Dropout voltage [4]	From parent buck C_{OUT} to LDO sense point. Load at I_{rated} For Vph ≥ 3 V For Vph < 3 V	 – –	 – –	 54 65	mV
Load regulation	$I_{LOAD} = I_{RATED}/100$ to I_{RATED}. HR = 100 mV. Measured at C_{OUT}. Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	–	–	0.3% + 12 mV + 30 mV	
Line regulation	Based on V_{BAT} from 3 V to 5 V. HR = 100 mV. For Vout ≥ 0.5 V	–	–	0.1	%/V
Short circuit current limit and OCP detection threshold N300	Max current LDO will output when shorted to ground	400	550	900	mA
Short circuit current limit and OCP detection threshold N600	Max current LDO will output when shorted to ground	800	1100	1800	mA
Short circuit current limit and OCP detection threshold N1200	Max current LDO will output when shorted to ground	1800	2400	3300	mA
Short circuit current limit test mode [5]	Max current LDO will output when shorted to ground in test mode	–	110	–	mA
Output noise density	HR = 100 mV. Measured at Cout. LDO contribution only, assumes clean Vin. 100 Hz ≤ f ≤ 1 kHz 1 kHz ≤ f ≤ 10 kHz 10 kHz ≤ f ≤ 100 kHz 100 kHz ≤ f ≤ 1 MHz	 2 1 0.5 0.35	 – – – –	 – – – –	$\mu V/\sqrt{Hz}$ $\mu V/\sqrt{Hz}$

Table 3-24 LDO2A, LDO5A, LDO6A, and LDO7A NMOS regulator specifications (cont.)

Parameter	Test condition or comment	Min	Typ	Max	Units
PSRR	From V_{IN} to V_{OUT}. Measured at Cout. (HR = 100 mV, $I_{LOAD} = I_{RATED}$). 50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	 40 30 15 5	 55 35 25 10	 – – – –	dB
	From V_{IN} to V_{OUT}. Measured at Cout. (HR = 50 mV, $I_{LOAD} = I_{RATED}/2$). 50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	 15 15 10 –	 50 30 15 10	 – – – –	dB
	From V_{IN} to V_{OUT}. Measured at Cout. (HR = 25 mV, $I_{LOAD} = I_{RATED}/4$). 50 Hz to 1 kHz 1 kHz to 10 kHz 10 kHz to 100 kHz 100 kHz to 1 MHz	 10 10 5 –	 40 20 10 5	 – – – –	dB
Ground current, no load	Measured at the battery. I_Q may be much higher if LDO is operated in drop-out condition.		95	110	µA
Low-power mode					
Rated load current [1] N300 N600 N1200	Max load current at which all specifications are met. Higher load current is possible at increased headroom	 30 30 30	–	 – – –	mA
Overall DC error at default voltage (includes load and line regulation, temperature, VBAT, MBG variation and trim error) [2]	Assume default voltage ≥ 0.8 V. Measured at Cout Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (2.5% + 1.2 mV + 3 mV)	–	2.5%	–

Table 3-24 LDO2A, LDO5A, LDO6A, and LDO7A NMOS regulator specifications (cont.)

Parameter	Test condition or comment	Min	Typ	Max	Units
Overall DC error at non-default voltage (includes load and line regulation, temperature, VBAT, MBG variation and trim error) [2]	For Vout ≥ 0.5 V, up to I_{RATED} Measured at Cout. Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	- (3% + 1.2 mV + 3 mV)	–	3%	
	For Vout < 0.5 V, up to $I_{RATED}/4$ Measured at Cout	-20	–	20	mV
Load transient undershoot, overshoot	Load step of 0.5 × I_{RATED} in 1 µs, with baseline current of 0.1 × I_{RATED} or higher. HR = 100mV. Compared to final settled value.	-40	–	70	mV
Dropout voltage	From package V_{IN} pin to V_{OUT} pin. Load at I_{RATED}	–	–	7.5	mV
Load regulation	I_{LOAD} = $I_{RATED}/100$ to I_{RATED}. HR = 100 mV. Measured at Cout. Format: X + Y + Z X = performance at LDO sense point Y = on-die routing DCR contribution Z = PCB routing DCR contribution	–	–	1% + 1.2 mV + 3 mV	
Line regulation	Based on V_{BAT} from 3.4 V to 4.75 V	–	–	0.5	%/V
Ground current, no load [6]	Measured at the battery. IQ may much be higher if LDO is operated in drop-out condition.	–	17	23	µA
Normal and low power mode					
NPM to LPM overshoot and undershoot	HR = 100 mV, Measured at Cout. I_{LOAD} = LPM I_{RATED}	-50	–	90	mV
Analog auto-bypass entry/exit overshoot and undershoot	Starting HR = 40 mV, HR = 0, HR = 110 mV. Ramp rate = 100 mV/µs during transition. I_{LOAD} = I_{RATED}. Compared to final settled value.	-40	–	70	mV
Ground current, with load	% of the load current	–	–	0.5	% I_{LOAD}
LDO discharge time to below 100 mV	Nominal load cap and strong pull-down enabled	–	0.1	2	ms

Table 3-24 LDO2A, LDO5A, LDO6A, and LDO7A NMOS regulator specifications (cont.)

Parameter	Test condition or comment	Min	Typ	Max	Units
VREG_OK threshold		85%	90%	95%	V_{out}
Bypass mode					
Ground current [7]		–	2	5	μA
N300 on resistance	From input cap (buck C_{out}) to LDO output cap. Format: X + Y + Z X = LDO contribution Y = on-die routing DCR, top level Z = PCB routing DCR	–	–	140 + 80 + 140 = 360	mΩ
N600 on resistance		–	–	70 + 40 + 70 = 180	mΩ
N1200 on resistance		–	–	35 + 20 + 35 = 90	mΩ

1. The rated current is the current at which the regulator meets all specifications. Higher currents can be allowed, but the regulator may need more headroom, that is, the difference between V_{IN} and V_{OUT}. For low-power mode, the user should switch the LDO to normal power mode if the load current is expected to be above the rated current.
2. At high temperature and some process corners, the pass device leakage causes the output voltage to float up under no-load conditions. The leakage pull down may need to be enabled to meet the specification.
3. The settling time is for start-up and any upward voltage change with the rated load capacitance. Time is increased with larger load capacitance. Settling time of a downward voltage change depends on the load current.
4. Dropout voltage is defined as follows:
   a. Apply the specified load current.
   b. Set $V_{IN} = V_{OUT} + 0.5$ V.
   c. Measure the output voltage.
   d. Reduce V_{IN} until V_{OUT} is reduced by 100 mV.
   e. Calculate dropout voltage as $V_{IN} - V_{OUT}$ in this condition.
5. The current limit test mode in NPM is used to evaluate the actual current limit threshold in normal mode. The threshold of test mode is designed to allow ATE to test the current limit functionality without having to use test resource that can support more than 200 mA of DC current.
6. The low-power mode no-load ground current may be higher due to the current limiting mistrigger in low headroom configuration. Disabling the current limiting feature or giving enough headroom as of the dropout requirement can prevent mistriggering and reduce the ground current.
7. In bypass mode, there is an active gate to source clamp to protect the LV NMOS.

Table 3-25 VREG_XO specifications

Parameter	Comments	Min	Typ	Max	Units
Rated load current		–	–	3	mA
V_{in} range		1.8	–	2.15	V
V_{out}		–	1.8	–	V
Settling time	To within 1% of final voltage, with 1 µF output capacitor	–	–	250	µs

Table 3-26 VREG_RF specifications

Parameter	Comments	Min	Typ	Max	Units
Rated load current		–	–	10	mA
V_{in} range		1.8	–	2.15	V
V_{out}		1.0	1.2	1.7	V
Settling time	To within 1% of final voltage, with 1 µF output capacitor	–	–	250	µs

3.7 General housekeeping

The PMIC includes many circuits that support handset-level housekeeping functions – various tasks that must be performed to keep the handset in order. Integration of these functions reduces the external parts count and the associated size and cost. Housekeeping functions include an analog switch matrix, multiplexers, and voltage scaling; an HK/XO ADC circuit; system clock circuits; a real-time clock for time and alarm functions; and overtemperature protection.

3.7.1 Analog multiplexer and scaling circuits

A set of analog switches, analog multiplexers, and voltage-scaling circuits select and condition a single analog signal for routing to the on-chip HK/XO ADC. The multiplexer and scaling functions are summarized in Table 3-27.

Table 3-27 Analog multiplexer and scaling functions

Channel number (hexadecimal)	Channel number (dec.)	Description	Source	Scaling	Internal pull-up	Input range (V)
0	0	REF_GND	Pin: GND_REF	1/1	Open	0 to 1.875
1	1	1.25VREF	Internal: MBG	1/1	Open	0 to 1.875
2	2	VREF_VADC	Internal: VADC LDO	1/1	Open	0 to 1.875
83	131	VPH_PWR	Pin: VPH_PWR	1/3	Open	0 to 4.75
85	133	VCOIN	Pin: VCOIN	1/3	Open	0 to 4.75
6	6	DIE_TEMP	Internal: TEMP_ALARM	1/1	Open	0 to 1.875
C	12	XO_THERM	Pin: XO_THERM	1/1	Open	0 to 1.875
D	13	AMUX_THM1	Pin: AMUX_1	1/1	Open	0 to 1.875
E	14	AMUX_THM2	Pin: AMUX_2	1/1	Open	0 to 1.875
F	15	AMUX_THM3	Pin: AMUX_3	1/1	Open	0 to 1.875
10	16	AMUX_THM4	Pin: AMUX_4	1/1	Open	0 to 1.875
11	17	AMUX_THM5	Pin: AMUX_5	1/1	Open	0 to 1.875
12	18	AMUX1_GPIO	Pin: GPIO_02	1/1	Open	0 to 1.875
13	19	AMUX2_GPIO	Pin: GPIO_03	1/1	Open	0 to 1.875
14	20	AMUX3_GPIO	Pin: GPIO_04	1/1	Open	0 to 1.875
15	21	AMUX4_GPIO	Pin: GPIO_05	1/1	Open	0 to 1.875
16	22	AMUX5_GPIO	Pin: GPIO_07	1/1	Open	0 to 1.875
17	23	AMUX6_GPIO	Pin: GPIO_09	1/1	Open	0 to 1.875
18	24	AMUX7_GPIO	Pin: GPIO_10	1/1	Open	0 to 1.875
19	25	AMUX8_GPIO	Pin: GPIO_12	1/1	Open	0 to 1.875
1D	29	ANA_IN	Pin: ANA_IN	1/1	Open	0 to 1.875
2C	44	XO_THERM	Pin: XO_THERM	1/1	30 k	0 to 1.875
2D	45	AMUX_THM1	Pin: AMUX_1	1/1	30 k	0 to 1.875

Table 3-27 Analog multiplexer and scaling functions (cont.)

Channel number (hexadecimal)	Channel number (dec.)	Description	Source	Scaling	Internal pull-up	Input range (V)
2E	46	AMUX_THM2	Pin: AMUX_2	1/1	30 k	0 to 1.875
2F	47	AMUX_THM3	Pin: AMUX_3	1/1	30 k	0 to 1.875
30	48	AMUX_THM4	Pin: AMUX_4	1/1	30 k	0 to 1.875
31	49	AMUX_THM5	Pin: AMUX_5	1/1	30 k	0 to 1.875
32	50	AMUX1_GPIO	Pin: GPIO_02	1/1	30 k	0 to 1.875
33	51	AMUX2_GPIO	Pin: GPIO_03	1/1	30 k	0 to 1.875
34	52	AMUX3_GPIO	Pin: GPIO_04	1/1	30 k	0 to 1.875
35	53	AMUX4_GPIO	Pin: GPIO_05	1/1	30 k	0 to 1.875
36	54	AMUX5_GPIO	Pin: GPIO_07	1/1	30 k	0 to 1.875
37	55	AMUX6_GPIO	Pin: GPIO_09	1/1	30 k	0 to 1.875
38	56	AMUX7_GPIO	Pin: GPIO_10	1/1	30 k	0 to 1.875
39	57	AMUX8_GPIO	Pin: GPIO_12	1/1	30 k	0 to 1.875
4C	76	XO_THERM	Pin: XO_THERM	1/1	100 k	0 to 1.875
4D	77	AMUX_THM1	Pin: AMUX_1	1/1	100 k	0 to 1.875
4E	78	AMUX_THM2	Pin: AMUX_2	1/1	100 k	0 to 1.875
4F	79	AMUX_THM3	Pin: AMUX_3	1/1	100 k	0 to 1.875
50	80	AMUX_THM4	Pin: AMUX_4	1/1	100 k	0 to 1.875
51	81	AMUX_THM5	Pin: AMUX_5	1/1	100 k	0 to 1.875
52	82	AMUX1_GPIO	Pin: GPIO_02	1/1	100 k	0 to 1.875
53	83	AMUX2_GPIO	Pin: GPIO_03	1/1	100 k	0 to 1.875
54	84	AMUX3_GPIO	Pin: GPIO_04	1/1	100 k	0 to 1.875
55	85	AMUX4_GPIO	Pin: GPIO_05	1/1	100 k	0 to 1.875
56	86	AMUX5_GPIO	Pin: GPIO_07	1/1	100 k	0 to 1.875
57	87	AMUX6_GPIO	Pin: GPIO_09	1/1	100 k	0 to 1.875
58	88	AMUX7_GPIO	Pin: GPIO_10	1/1	100 k	0 to 1.875
59	89	AMUX8_GPIO	Pin: GPIO_12	1/1	100 k	0 to 1.875
6C	108	XO_THERM	Pin: XO_THERM	1/1	400 k	0 to 1.875
6D	109	AMUX_THM1	Pin: AMUX_1	1/1	400 k	0 to 1.875
6E	110	AMUX_THM2	Pin: AMUX_2	1/1	400 k	0 to 1.875
6F	111	AMUX_THM3	Pin: AMUX_3	1/1	400 k	0 to 1.875
70	112	AMUX_THM4	Pin: AMUX_4	1/1	400 k	0 to 1.875
71	113	AMUX_THM5	Pin: AMUX_5	1/1	400 k	0 to 1.875
72	114	AMUX1_GPIO	Pin: GPIO_02	1/1	400 k	0 to 1.875
73	115	AMUX2_GPIO	Pin: GPIO_03	1/1	400 k	0 to 1.875

Table 3-27 Analog multiplexer and scaling functions (cont.)

Channel number (hexadecimal)	Channel number (dec.)	Description	Source	Scaling	Internal pull-up	Input range (V)
74	116	AMUX3_GPIO	Pin: GPIO_04	1/1	400 k	0 to 1.875
75	117	AMUX4_GPIO	Pin: GPIO_05	1/1	400 k	0 to 1.875
76	118	AMUX5_GPIO	Pin: GPIO_07	1/1	400 k	0 to 1.875
77	119	AMUX6_GPIO	Pin: GPIO_09	1/1	400 k	0 to 1.875
78	120	AMUX7_GPIO	Pin: GPIO_10	1/1	400 k	0 to 1.875
79	121	AMUX8_GPIO	Pin: GPIO_12	1/1	400 k	0 to 1.875
94	148	AMUX3_GPIO	Pin: GPIO_04	1/3	Open	0 to 4.75
97	151	AMUX6_GPIO	Pin: GPIO_09	1/3	Open	0 to 4.75
FF	255	All channels off	–	–	–	–

3.7.2 HK/XO ADC circuit

The analog-to-digital converter circuit is shared by the housekeeping (HK) and 38.4 MHz crystal oscillator (XO) functions.

HK/XO ADC performance specifications are listed in Table 3-28.

Table 3-28 VADC electrical specification

Specification	Test condition	Min	Typ	Max	Units
1/1 channel end-to-end accuracy	Calibrated data result	-11	6	11	mV
1/1 channel end-to-end accuracy with internal pull-up	Calibrated data result	-12.5	7	12.5	mV
1/3 channel end-to-end accuracy	Calibrated data result	-20	10	20	mV
ADC resolution (LSB)		–	114.441	–	μV
Analog bandwidth (anti-alias filter)		–	500	–	kHz
ADC LDO voltage		1.828	1.875	1.910	V
ADC sample clock		–	4.8	–	MHz
ADC conversion time	1 K decimation ratio, 4.8 MHz sample clock	–	515	550	μs
Current consumption	VADC active	–	450	500	μA
100 K pull-up	Trimmed value	99.5	100	100.5	kΩ
400 K pull-up	Trimmed value	398	400	402	kΩ
30 K pull-up	Trimmed value	29.7	30	30.3	kΩ
Pull-up temperature coefficient		-100	–	100	ppm/°C
1/1 channel AMUX input resistance		10	–	–	MΩ
1/3 channel AMUX input resistance		1	–	–	MΩ

3.7.3 System clocks

The PMIC includes several clock circuits whose outputs are used for general housekeeping functions and elsewhere within the handset system. These circuits include a 19.2 MHz XO with multiple controllers and buffers, an MP3 clock output, an RC oscillator, and sleep-clock outputs. Performance specifications for these functions are presented in the following subsections.

3.7.3.1 38.4 MHz XO circuits

An external crystal is supplemented by on-chip circuits to generate the intended 38.4 MHz reference signal. Using an external thermistor network, the on-chip ADC, and advanced temperature compensation software, the PMIC eliminates the large and expensive VCTCXO module required by previous-generation chipsets. The XO circuits initialize and maintain valid pulse waveforms and measure time intervals for higher-level handset functions.

Multiple controllers manage the XO and signal buffering and generate the intended clock outputs (all derived from one source):

- RF_CLKx and BB_CLKx low-noise outputs – enabled internally, or can be enabled via properly configured GPIOs (RF_CLKx is 38.4 MHz while BB_CLKx is 19.2 MHz).
- BB_CLK1_EN low-noise output – enabled by the dedicated control pin; this output is used as the modem IC's clock signal.

Since the different controllers and outputs are independent, circuits other than those needed for the WAN can operate even while the modem IC is asleep and its RF circuits are powered down.

The XTAL_IN and XTAL_OUT pins are incapable of driving a load—the oscillator will be significantly disrupted if either pin is externally loaded.

The 38.4 MHz XO circuit and related performance specifications are listed in the following tables.

Table 3-29 RF_CLKx specification

Parameter	Comments	Min	Typ	Max	Unit
Frequency	Set by external crystal	–	38.4	–	MHz
Duty cycle		48	50	52	%
Output voltage swing		1.164	1.2	1.236	V
Output buffer impedance	1x	–	45	–	Ω
	2x	–	35	–	Ω
	3x	–	25	–	Ω
	4x	–	13	–	Ω
Phase noise	At 1 kHz	–	-130	–	dBc/Hz
	At 10 kHz	–	-142	–	dBc/Hz
	At 100 kHz	–	-154	–	dBc/Hz
	At 1 MHz	–	-154	–	dBc/Hz
AM noise	At 1 kHz	–	–	-87	dBc/Hz
	At 10 kHz	–	–	-122	dBc/Hz
	At 100 kHz	–	–	-137	dBc/Hz
	At 1 MHz	–	–	-137	dBc/Hz

Table 3-30 BB_CLKx specification

Parameter	Comments	Min	Typ	Max	Unit
Frequency	Set by the external crystal	–	19.2	–	MHz
Duty cycle		48	50	52	%
Output voltage swing		1.746	1.8	1.854	V

Table 3-30 BB_CLKx specification (cont.)

Parameter	Comments	Min	Typ	Max	Unit
Output buffer impedance	1x	–	38	–	Ω
	2x	–	28	–	Ω
	3x	–	19	–	Ω
	4x	–	10	–	Ω
Phase noise	At 10 Hz	–	-86	–	dBc/Hz
	At 100 Hz	–	-110	–	dBc/Hz
	At 1 kHz	–	-136	–	dBc/Hz
	At 10 kHz	–	-144	–	dBc/Hz
	At 100 kHz	–	-144	–	dBc/Hz
	At 1 MHz	–	-144	–	dBc/Hz
Period jitter	RMS	–	3	–	ps
Period jitter (peak to peak)	500 kHz–2.2 MHz	–	50	–	ps
	2.2 MHz–9.6 MHz	–	100	–	ps

Table 3-31 Divided-down XO clock output specifications

Parameter	Min	Typ	Max	Units
Buffer output impedance				
at low GPIO drive strength	–	42	–	Ω
at medium GPIO drive strength	–	30	–	Ω
at high GPIO drive strength	–	22	–	Ω
Phase noise				
at 100 Hz	–	-85	–	dBc/Hz
at 1 kHz	–	-95	–	dBc/Hz
at 10 kHz	–	-100	–	dBc/Hz
at 100 kHz	–	-105	–	dBc/Hz
at 250 kHz	–	-105	–	dBc/Hz
at 500 kHz	–	-105	–	dBc/Hz

3.7.3.2 38.4 MHz XO crystal requirements

Crystal performance is critical to a wireless product's overall performance. Guidance is available within the *38.4 MHz Modem Crystal Qualification Requirements and Approved Suppliers* (80-NJ458-19) document. This document includes:

- Data needed from crystal suppliers to demonstrate compliance
- Approved suppliers for different crystal configurations
- Description of various schematic options

3.7.3.3 MP3 clock

GPIOs can be configured as a 2.4 MHz clock output to support MP3 in a low-power mode. This clock is a divided-down version of the 38.4 MHz XO signal, so its most critical performance features are defined within the XO table (Table 3-31). Output characteristics (voltage levels, drive strength, and so on) are defined in Section 3.4.

3.7.3.4 Sleep clock

The sleep clock is generated one of three ways:

- Using the 38.4 MHz XO circuit and dividing its output by 1172 to create a 32.768 kHz signal.
- Using an internal 100 KHz RC oscillator divide by 3 or Cal-RC

The PMIC sleep-clock output is routed to the modem IC via SLEEP_CLK. It is also available for other applications using properly configured GPIOs. Table 3-32 shows the sleep clock performance specifications.

Table 3-32 Sleep clock performance specifications

Parameter	Comments	Min	Typ	Max	Units
Period jitter (RMS)	XO/1172 source; as defined in JDSE6	–	10	–	ns
Duty cycle	XO/1172 source	–	50	–	%
Tolerance	XO/1172 source	-20	–	20	ppm

Related specifications presented elsewhere include:

- 38.4 MHz XO circuits (Section 3.7.5)
- Output characteristics (voltage levels, drive strength, and so on), as defined in Section 3.4

3.7.4 RTC

The RTC functions are implemented by a 32-bit real-time counter and one 32-bit alarm; both are configurable in one-second increments. The primary input to the RTC circuits is the selected sleep-clock source (calibrated low-frequency oscillator, or divided-down 38.4 MHz XO). Even when the phone is off, the selected oscillator and RTC continue to run off the main battery.

If only the main battery is present and an SMPL event occurs, then RTC contents are corrupted. The phone must re-acquire system time from the network to resume the usual RTC accuracy. Similarly, if the main battery is not present and the voltage at VCOIN drops too much, RTC contents are again corrupted. In either case, the RTC reset interrupt is generated. A different interrupt is generated if the oscillator stops, also causing RTC errors.

If RTC support is needed when the battery is removed, a qualified coin-cell or super capacitor is required on the VCOIN pin of the PMIC. If only SMPL support is needed when battery is removed, a 47 µF capacitor with at least 10 µF effective capacitance at 3 V is required on the VCOIN pin of the PMIC.

Pertinent RTC specifications are listed in Table 3-33.

Table 3-33 RTC performance specifications

Parameter	Comments	Min	Typ	Max	Units
Tuning resolution	With known calibrated source	–	3.05	–	ppm
Tuning range		-192	–	+192	ppm
Accuracy					
XO/1172 as RTC source	Phone on	–	–	24	ppm
CalRC as RTC source	Phone off, valid battery present	–	–	50	ppm
	Phone off, valid coin-cell present [1]	–	–	200	ppm

1. Assumes a maximum ESR of coin cell/super capacitor is 1 kΩ. For a maximum ESR of 2 kΩ, the accuracy is 500 ppm.

3.7.5 Overtemperature protection (smart thermal control)

The PMIC includes Overtemperature protection in stages, depending on the level of urgency as the die temperature rises:

- Stage 0 – normal operating conditions.
- Stage 1 – 90°C to 100°C (configurable threshold); an interrupt is sent to the MSM device without shutting down any PMIC circuits.
- Stage 2 – 100°C to 130°C (configurable threshold); an interrupt is sent to the modem IC and unnecessary high-current circuits are shut down. The charger reduces the charging current.
- Stage 3 – greater than 150°C; an interrupt is sent to the modem IC, and the PMIC is completely shut down.

Temperature hysteresis is incorporated, such that the die temperature must cool significantly before the device can be powered on again. If any start signals are present while at Stage 3, they are ignored until Stage 0 is reached. When the device cools enough to reach Stage 0 and a start signal is present, the PMIC powers up immediately.

3.8 User interfaces

User interfaces performance specifications are split into six functional categories as defined within its block diagram (Figure 3-16).

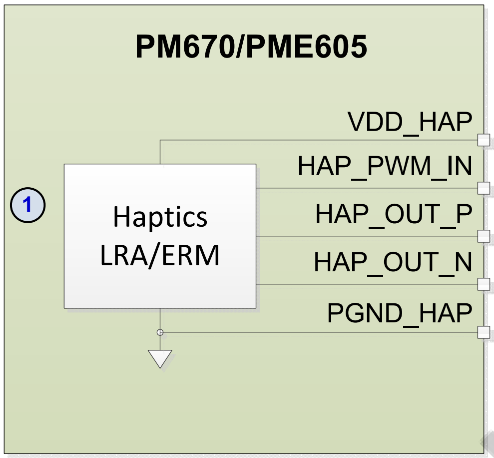


Figure 3-16 User interfaces functional block diagram

3.8.1 Haptics

Haptics uses vibration to communicate an event or action through human touch. In a mobile phone, haptics is used to simulate the feeling of a real mechanical key by providing tactile feedback to the user as confirmation of touchscreen contact, or dynamic feedback to enhance the user's gaming experience. Pertinent performance specifications are listed in Table 3-34.

Table 3-34 Haptics performance specifications

Parameter	Comments [1]	Min	Typ	Max	Units
Operational input voltage	Connected at VDD_HAP	2.50	3.6	4.75	V
Output voltage [2]					
Peak, no load	At VSW_HAP_P and VSW_HAP_M	–	–	VH	V
Average (V_HA)	Differential, over one PWM cycle	0	–	3.6	V
Maximum drive [3]	Differential, over one PWM cycle	1.2	–	3.6	V
Accuracy	Duty cycle ≤ 95%	–	50	–	mV
Output current limit	Cycle-to-cycle limit				
R_ERM or R_LOAD = 20 Ω		300	400	500	mA
R_ERM or R_LOAD = 10 Ω		600	800	1000	mA
On resistance					
R_ON_P	High-side switch	0.25	0.5	1.25	Ω
R_ON_N	Low-side switch	0.25	0.5	1.25	Ω
Internal PWM frequency					
Programmable options	253 kHz, 505 kHz, 739 kHz, and 1076 kHz	253	503	1076	kHz
Accuracy		–	–	±16	%
LRA resonance					
Programmable period	5 µs (±16% due to internal oscillator) steps	3.33	–	20	ms
Accuracy	Auto resonance detection	–	5	10	µs
LRA self-resonance capture		–	±20	–	Hz
HAP_PWM_IN voltage		0	–	1.8	V
Start-up time	Enable to full output drive voltage	–	–	100	µs
Ground current					
Active		–	3.0	–	mA
Shutdown		–	–	1.0	µA

1. All specifications apply at VDD_HAP = 3.6 V, T = -30ºC to +85ºC, and F_pwm = 500 kHz unless noted otherwise.
2. Output voltage is programmable in steps of 116 mV. "VH" = VDD_HAP (3.6 V typical).
3. VDD_HAP > V_HA + I_out x (R_ON_P + R_ON_N).

3.9 IC-level interfaces

3.9.1 Power-on circuits and power sequences

Dedicated circuits continuously monitor several events that might trigger a power-on sequence. If any of these events occur, the PMIC circuits are powered on, the handset's available power sources are determined, the correct source is enabled, and the modem IC is taken out of reset. The PM670A/PM670L device complements the PM670 device to meet the system's power management needs. Power sequencing details are shared between the two ICs, so this topic is addressed in the *PM670 and PM670A/PM670L Power Management ICs Design Guidelines/Training Slides* (80-PD119-5A), including:

- Power-on circuit block diagrams and descriptions
- Pin assignment descriptions and schematic details showing PMIC interconnections
- Types of triggers and turn on and off trigger events
- Power sequencing and detailed descriptions

The regulators that are included during the initial power-on sequence are determined by the hardware configuration control option pins, as defined in Section 3.9.4. The sequence of signals are detailed below.

Table 3-35 Power-on sequence: Dual phase APPS1 for PM670

Power-on sequence	Device location	Regulator name	Vout primary (V)	Notes
1	PM670A/PM670L	BOB	3.3 V	LV battery support
2	PM3003A-4	DBU1	1.1125 V	External SMPS–LV subreg LDO
3	PM670	S4A	2.04 V	HV subreg LDO
4	PM670A	L3A	1 V	SDR 1.0 V digital
5	PM670A/PM670L	S1B	0.884 V	VDDMX
6	PM670A/PM670L	LDO10B	0.88 V	LPI_MX
7	PM670A/PM670L	S3B_S4B	0.828 V	VDDCX
8	PM670A/PM670L	LDO9B	0.824 V	LPI_CX
9	PM670	LDO5A	0.8 V	WCSS
10	PM670	LDO13A	1.8 V	P3, general IO (1.8 V)
11	PM670	VREF_MSM	1.25 V	HV PAD REF
12	PM670	S6A	1.352 V	MV subreg LDO
13	PM670	LDO9A	1.8 V	WCN XO
14	PM670	LDO6A	1.304 V	WCN 1P3
15	PM670	LDO19A	3.104 V	WCN CHAIN0
16	PM3003A-3	DBU2	1.1125 V	LPDDR4X VDD2
17	PM670	LDO8A	1.8 V	EMMC/UFS 1.8 V
18	PM670	LDO11A	1.8 V	Display touchscreen
19	PM670	LDO1A	1.2 V	PHY1.2 V UFS VCCQ

Table 3-35 Power-on sequence: Dual phase APPS1 for PM670

Power-on sequence	Device location	Regulator name	Vout primary (V)	Notes
20	PM670A/PM670L	S5B	0.6 V	LPDDR4X VDDQ + EBI VDDIO
21	PM670A/PM670L	LDO1B	0.88 V	PHY:USB, QLink, DSI, UFS
22	PM670	LDO10A	1.8 V	PHY - PLL - BB_CLK -USB
23	PM670A/PM670L	LDO7B	3.088 V	USB
24	PM670A/PM670L	LDO4B	2.96 V	EMMC
25	PM670A/PM670L	LDO2B	2.96 V	SD card IO
26	PM670A/PM670L	LDO5B	2.96 V	SD/MMC card
27	PM670	S5A	0.828 V	MODEM SS - Modem Q6 - Boot memory
28	PM670	S1A	0.828 V	Kryo silver APC

For single phase APPS1, the power-on sequence is similar to dual phase APPS1, except for the following differences:

Table 3-36 Power-on sequence: Single phase APPS1 for PM670

Power-on sequence	Device location	Regulator name	Vout primary (V)	Notes
16	PM670	S3A	1.128 V	LPDDR4X VDD2 alternate

The I/Os to/from the power-on circuits are basic digital control signals that must meet the voltage-level requirements stated in Section 3.4. The KPD_PWR_N and CBL_PWR_N inputs are pulled up to an internal voltage (dVdd). More complete definitions for time intervals included in the table are provided in the *PM670 and PM670A/PM670L Power Management ICs Design Guidelines/Training Slides* (80-PD119-5A).

Table 3-37 PME605 power-on sequence

Device location	Regulator name	PON sequence	V_{out} primary (V)	Notes
PME605	S4A	1	2.04	HV SUB-REG LDO
PME605	S5A	2	1	LV SUB-REG LDO
PME605	S2A	3	0.8	VDDMX - LPI_MX
PME605	L7A	4	0.8	LPI_CX
PM8005	S1C_4C	5	0.752	VDDCX
PM8005	S1C_4C	5	0.752	VDDCX
PME605	L1A	6	0.8	On chip WLAN
PME605	L13A	7	1.8	General purpose 1.8 V IO and LPDDR4X VDD1
PM8005	S2C	8	1.128	LPDDR4X VDD2
PME605	VREF_MSM	9	1.25	HV PAD REF
PME605	S6A	10	1.352	MV SUB-REG LDO
PME605	L8A	13	1.8	UFS_EMMC VDDQ
PME605	L2A	14	1.2	PHY 1.2 V UFS VCCQ
PME605	S3A	15	0.6	LPDDR4X VDDQ + EBI VDDIO
PME605	L6A	16	0.88	PHY 0.88 V
PME605	L10A	17	1.8	PLL - BBCLK - PHY_USB
PME605	L17A	18	3.088	USB
PME605	L19A	19	2.96	UFS_EMMC VCC
PME605	L18A	20	2.96	SDCard IO
PME605	S1A	22	0.752	Kryo Silver, Kryo Gold

3.9.2 Undervoltage lockout

The handset supply voltage (VDD) is monitored continuously by a circuit that automatically turns off the device at severely low VDD conditions.

To power on successfully, VPH must be between the UVLO rising threshold and the OVLO falling threshold. These thresholds are not used after P_{ON}. However, in order to stay on, VPH must remain between the UVLO falling threshold and the OVLO rising threshold. If these thresholds are exceeded, a fault occurs and the chip will immediately shut down.

Other than the programmable threshold, software is not involved in UVLO/OVLO detection. Hysteresis and time delays are not programmable, and UVLO/OVLO events do not generate interrupts. They are reported to the modem IC via the PON_RESET_N signal. UVLO/OVLO-related voltage and timing specifications are listed in Table 3-38.

Table 3-38 UVLO and OVLO thresholds

Parameter	Comments	Min	Typ	Max	Units
UVLO falling threshold voltage [1]		1.50	2.4 V ± 50 mV	3.05	V
UVLO rising threshold voltage [1]		1.95	2.85 V ± 50 mV	3.50	V
UVLO interval detection		–	3	–	µs
OVLO rising threshold voltage [2]		4.20	5.9 V ± 100 mV	7.30	V
OVLO falling threshold voltage [2]		3.70	5.4 V ± 100 mV	6.80	V
OVLO detection interval		–	6	–	µs

1. UVLO falling threshold is programmable. The UVLO rising threshold = UVLO falling threshold + hysteresis. In software, the falling threshold is set to 1.85 V ± 50 mV, with hysteresis (600 mV). The UVLO falling threshold for PM670A/PM670L is configured well below the PM670 UVLO falling threshold. This allows the PM670 to be the dominating factor for executing a UVLO.
2. OVLO rising threshold is programmable. The OVLO rising threshold = OVLO falling threshold + hysteresis.

3.9.3 SPMI and the interrupt managers

The SPMI is a bidirectional, two-line digital interface that meets the voltage and current level requirements stated in Section 3.4. PMIC interrupt managers support the chipset modem and its processors and communicate with the modem IC via SPMI. Since the interrupt managers are entirely embedded functions, additional performance specifications are not required.

3.9.4 OPT hardwired controls

Two pins must be hardwired to ground or VDD, or be left open (high-impedance state or Hi-Z).

Table 3-39 lists the parameters that option pins decide.

Table 3-39 Hardware configuration options for PM670

Option pin	Parameter	Configuration
PM670 GPIO_01 GND Hi-Z VDD	Chipset power-on/off sequence	 Reserved Dual phase APPS1 Single phase APPS1
PM670 GPIO_09 GND Hi-Z VDD	Micro USB charger presence	 Micro USB Type-C NA

Each chipset that uses the PM670 and PM670A/L device must set the OPT pins correctly for their particular application.

However, stuffing options should be made available for all three options of VDD, Hi-Z, and GND to ensure flexibility in reconfiguring the option pins if needed.

Table 3-40 Hardware configuration options for PME605

Option pin	Parameter	Configuration
TBD	TBD	TBD

3.10 GPIO specifications

The 13 GPIO ports are digital I/Os that can be programmed for a variety of configurations (Table 3-41). General digital I/O performance specifications for the different configurations are included in Section 3.4.

NOTE: Unused GPIO pins should be configured as inputs with 10 µA pull-down (their default state).

NOTE: GPIO_2 is configured as sleep_clk out during PON

Table 3-41 Programmable GPIO configurations

Configuration type	Configuration description
Input	■ No pull-up ■ Pull-up (1.5 µA, 30 µA, or 31.5 µA) ■ Pull-down (10 µA) ■ Keeper
Output	Open-drain or CMOS Inverted or noninverted Programmable drive current

All GPIOs, except for GPIO_1, default to digital input with 10 µA pull-down at power-on. The GPIOs must be configured properly for their intended purposes after power-on.

GPIOs are designed to run at a 4 MHz rate to support high-speed applications. The supported rate depends on the load capacitance and IR drop requirements. If the application specifies load capacitance, then the maximum rate is determined by the IR drop. If the application does not require a specific IR drop, then the maximum rate can be increased by increasing the supply voltage and adjusting the drive strength according to the actual load capacitance.

4 Mechanical information

4.1 Device physical dimensions

The PM670 is available in the 219 WLPSP that includes ground pins for improved grounding, mechanical strength, and thermal continuity. The 219 WLPSP has a 5.05 mm × 5.64 mm body with a maximum height of 0.53 mm. Pin 1 is located by an indicator mark on the top of the package and by the ball pattern when viewed from below. A simplified version of the 219 WLPSP outline drawing is shown in Figure 4-1.

NOTE: Click the following link to download *Package Outline Drawing, 219 WLPSP, 5.05 x 5.64 x 0.53 mm, D280, B25* (NT90-P6338-1) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-P6338-1

After successfully logging on, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

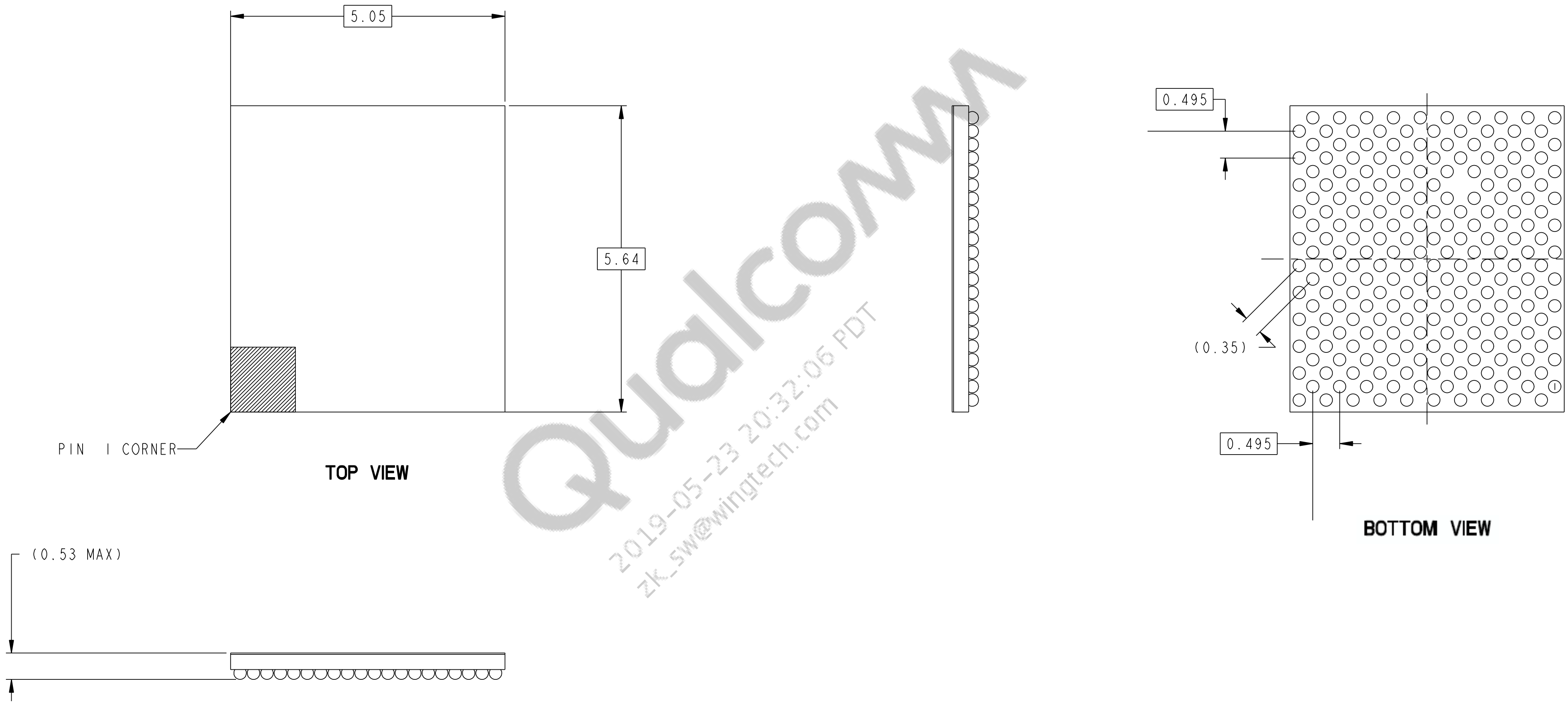


Figure 4-1 219 WLPSP (5.05 x 5.64 x 0.53 mm) outline drawing

NOTE: This is a simplified outline drawing. Click the following link to download the complete, up-to-date package outline drawing:

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-P6338-1

4.2 Part marking

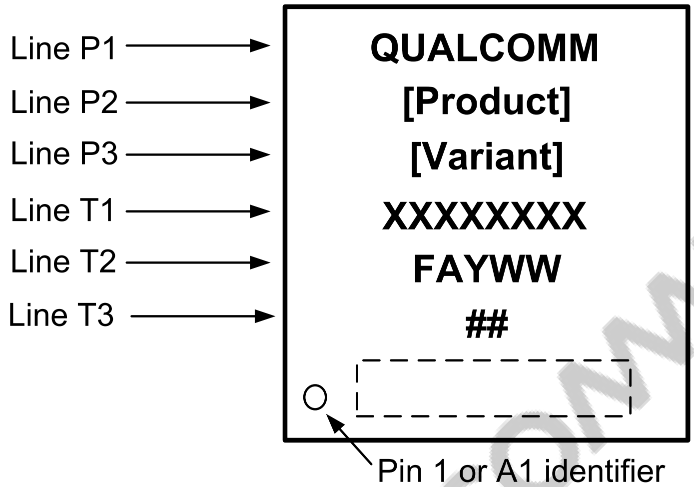


Figure 4-2 PM670/PME605 device marking (top view, not to scale)

Table 4-1 PM670/PME605 device marking line definitions

Line	Marking	Description
P1	QUALCOMM	Qualcomm name or logo
P2	[Product]	Qualcomm Technologies, Inc. (QTI) product name □ PM670 □ PME605
P3	[Variant] PRR-BB	Device variant information P = product configuration code ■ See Table 4-2 for the assigned values. RR = product revision ■ See Table 4-2 for the assigned values. BB = feature code ■ See Table 4-2 for the assigned values.
T1	XXXXXXXX	XXXXXXXX = traceability number
T2	FAYWW	F = supply source code ■ F = F for TSMC ■ F = H for GLOBALFOUNDRIES ■ F = E for MagnaChip A = assembly site code ■ A = U for Amkor, China ■ A = M for STATS ChipPAC, Singapore ■ A = E for ASE, Taiwan Y = single-digit year WW = work week (based on calendar year)

Table 4-1 PM670/PME605 device marking line definitions (cont.)

Line	Marking	Description
T3	##	## = Two-digit wafer number
E	Blank or variable	Additional content as necessary

4.3 Device ordering information

4.3.1 Specification-compliant devices for PM670

This device can be ordered using the identification code shown in Figure 4-3.

Device ID code ►	AAA-AAAA	— P	— CCC	DDDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product revision	Source code	Feature code
Example ►	PM670	— 0	— 219	WLPSP	— MT	— 01	— 1	— NA

Figure 4-3 Example: device identification code for PM670

Device identification details for all samples available to date are summarized in Table 4-2.

Table 4-2 Device identification details for PM670

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code (if applicable) [1]	Hardware revision number	S value [2]	Comments
PM670	ES	000	1.1	0	–
PM670 [3]	CS	001	2.0	1	–

1. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
2. S is the source configuration code that identifies all of the qualified die fabrication-source combinations available when the particular sample type was shipped. S values are defined in Table 4-3.
3. The PM670 2.0 samples are sourced from the TSMC and GLOBALFOUNDRIES fab sources.

Table 4-3 Source configuration code for PM670

S value	Die	F value = F	F value = H	F value = E
0	Digital	TSMC	GLOBALFOUNDRIES	MagnaChip
1	Digital	TSMC	GLOBALFOUNDRIES	
Other columns and rows will be added in future revisions of this document, if needed.				

4.3.2 Specification-compliant devices for PME605

This device can be ordered using the identification code shown in Figure 4-3.

Device ID code ►	AAA-AAAA	— P	— CCC	DDDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product revision	Source code	Feature code
Example ►	PME-605	— 0	— 219	WLPSP	— MT	— 01	— 1	— NA

Figure 4-4 Example: device identification code for PME605

Device identification details for all samples available to date are summarized in Table 4-2.

Table 4-4 Device identification details for PME605

Device	Sample type	Variant (PRR-BB) P = product configuration code RR = product revision code BB = feature code (if applicable) [1]	Hardware revision number	S value [2]	Comments
PME605	ES1	001	2.0	0	–
PME605	ES2	001-00	2.0	0	See the *PME605 and PM8005 devices fail to power on occasionally* issue details in the *PM670/PME605 Device Revision Guide* (80-PD119-4)

1. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.
2. S is the source configuration code that identifies all of the qualified die fabrication-source combinations available when the particular sample type was shipped. S values are defined in Table 4-3.

Table 4-5 Source configuration code for PME605

S value	Die	F value = F	F value = H
1	Digital	TSMC	GLOBALFOUNDRIES
Other columns and rows will be added in future revisions of this document, if needed.			

4.3.3 Daisy chain devices

The PM670 daisy chain ordering part number is DS90-P6338-1.

The PME605 daisy chain ordering part number is TBD.

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-6.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH; PM670A/PM670L rating
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hrs	≤ 30°C/60% RH
4	72 hrs	≤ 30°C/60% RH
5	48 hrs	≤ 30°C/60% RH
5a	24 hrs	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The PM670 devices are classified as MSL1; the qualification temperature was 260°C +0°/-5°C***. This qualification temperature (260°C +0°/-5°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CreatePoint website. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE: Click the following link below to download the *PM670 219 WLPSP Package Thermal Model Icepak* (HS11-P7905-5AHW) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-P7905-5AHW

Click the following link to download the *PM670 219 WLPSP Package Thermal Model Flotherm* (HS11-P7905-6AHW) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-P7905-6AHW

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

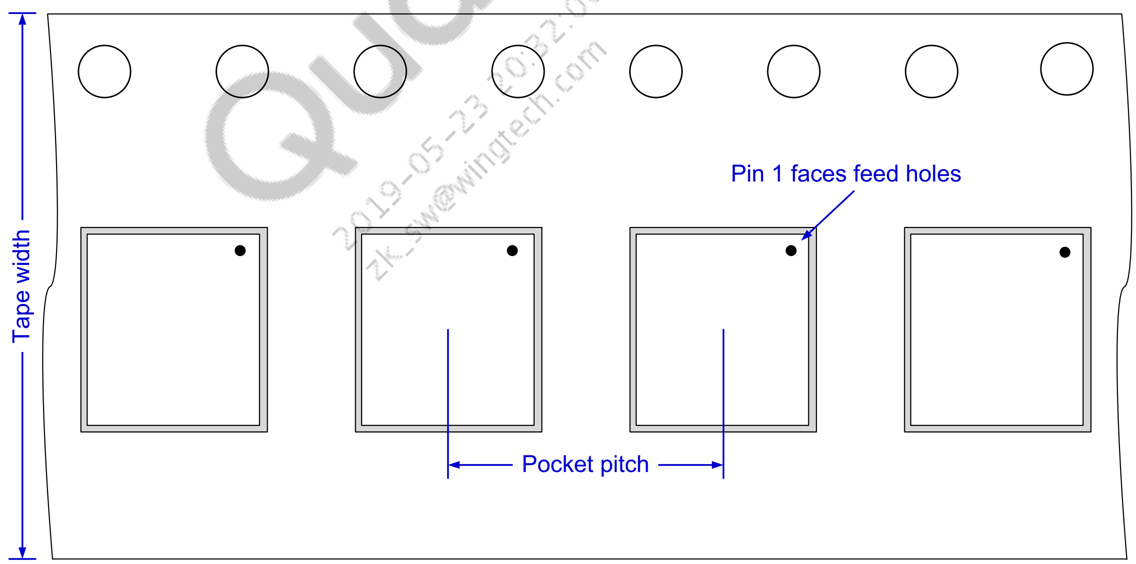
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI carrier tape systems conform to EIA-481 standards.

A simplified sketch of the PM670 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Taping direction →

Tape feed:	Single	Reel diameter:	330 mm	Tape width:	12 mm
Units per reel:	4000	Hub diameter:	178 mm	Pocket pitch:	8 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

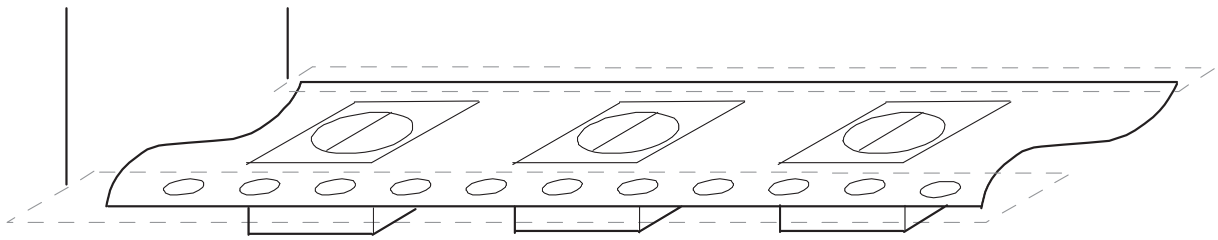


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

PM670 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags. Refer to the *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

Wafer-level packages such as the 219 WLPSP should not be baked.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

See the *IC Products Packing Method* (80-VK055-1) for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its SnAgCu solder balls use SAC405 composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, refer to the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE: Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.3 Daisy chain components

Daisy chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. The SMT process recommendations described in Section 6.2 can be performed using daisy chain components.

Ordering information is given in Section 4.3.3.

Daisy chain PCB routing recommendations are available for download.

NOTE: Click the following link to download the *Daisy Chain Interconnect, 219 WLPSP, 5.05 × 5.64 × 0.53 mm* (DS90-P6338-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/DS90-P6338-1

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

7 Part reliability

7.1 Reliability qualifications summary: GLOBALFOUNDRIES

Table 7-1 Silicon reliability results: GLOBALFOUNDRIES

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A Total samples from three different wafer lots	240	Pass DPPM < 1000 [1]
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A Total samples from three different wafer lots	240	Pass FIT < 50 [1]
Mean time to failure (MTTF) t = 1/λ in million hours Total samples from three different wafer lots	240	Pass MTTF > 20 [1]
ESD – HBM rating JESD22-A114-F Target: 1500 V Total samples from one wafer lot	3	Pass 1500 V
ESD – CDM rating JESD22-C101-D Target: 500 V Total samples from one wafer lot	3	Pass 500 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA Temperature: 85°C Total samples from one wafer lot	6	Pass
Latch-up (V supply overvoltage): EIA/JESD78A Trigger voltage: each VDD pin, stress at 1.5 × V_{DD} maximum per the device specification Temperature: 85°C Total samples from one wafer lot	6	Pass

1. The cumulative DPPM, FIT, and MTTF is based on multiple products under the GF 180 nm process.

Table 7-2 Package reliability results for GLOBALFOUNDRIES [1]

Tests, standards, and conditions	ASE-KH assembly source sample size	ATC assembly source sample size	SCS assembly source sample size	Result
Moisture resistance test (MRT): J-STD-020C Reflow at 260°C +0/-5°C Total samples from three different assembly lots	693	693	693	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8 to 10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	231	231	231	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hour duration or 110°C/85% RH and 264 hour duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	231	231	231	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96 hour duration or 110°C/85% RH and 264 hour duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	96	96	96	Pass
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hours Total samples from three different assembly lots	231	231	231	Pass
Flammability **Note**: flammability test – not required UL-STD-94 QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs are mounted are rated V-0 (better than V-1).	–	–	–	N/A
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document Total samples from three different assembly lots at each SAT	30	30	30	Pass

Table 7-2 Package reliability results for GLOBALFOUNDRIES [1] (cont.)

Tests, standards, and conditions	ASE-KH assembly source sample size	ATC assembly source sample size	SCS assembly source sample size	Result
Die Shear MIL-STD-883E, Method 2019 (Total samples from three different assembly lots at each SAT)	15	15	15	Pass
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT	30	30	30	Pass
Internal/external visual Total samples from three different assembly lots at each SAT	75	75	75	Pass

1. Package qualification results are leveraged from other previously qualified WLP packages, including QBT1000, PM8026, and PM8941, that are similar to this configuration.

7.2 Reliability qualifications summary: TSMC

Table 7-3 Silicon reliability results: TSMC

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A Total samples from three different wafer lots	240	Pass DPPM < 1000 [1]
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A Total samples from three different wafer lots	240	Pass FIT < 50 [1]
Mean time to failure (MTTF) t = 1/λ in million hours Total samples from three different wafer lots	240	Pass MTTF > 20 [1]
ESD – HBM rating JESD22-A114-F Target: 1500 V Total samples from one wafer lot	3	Pass 1500 V
ESD – CDM rating JESD22-C101-D Target: 500 V Total samples from one wafer lot	3	Pass 500 V

Table 7-3 Silicon reliability results: TSMC

Tests, standards, and conditions	Sample size	Result
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA Temperature: 85°C Total samples from one wafer lot	6	Pass
Latch-up (V supply overvoltage): EIA/JESD78A Trigger voltage: each VDD pin, stress at 1.5 × V_{DD} maximum per the device specification Temperature: 85°C Total samples from one wafer lot	6	Pass

1. The cumulative DPPM, FIT, and MTTF is based on multiple products under the GF 180 nm process.

Table 7-4 Package reliability results for TSMC [1]

Tests, standards, and conditions	ASE-KH assembly source sample size	ATC assembly source sample size	SCS assembly source sample size	Result
Moisture resistance test (MRT): J-STD-020C Reflow at 260°C +0/-5°C Total samples from three different assembly lots	693	693	693	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8 to 10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	231	231	231	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hour duration or 110°C/85% RH and 264 hour duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	231	231	231	Pass
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96 hour duration or 110°C/85% RH and 264 hour duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	96	96	96	Pass
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hours Total samples from three different assembly lots	231	231	231	Pass

Table 7-4 Package reliability results for TSMC [1] (cont.)

Tests, standards, and conditions	ASE-KH assembly source sample size	ATC assembly source sample size	SCS assembly source sample size	Result
Flammability **Note**: flammability test – not required UL-STD-94 QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs are mounted are rated V-0 (better than V-1).	–	–	–	N/A
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document Total samples from three different assembly lots at each SAT	30	30	30	Pass
Die Shear MIL-STD-883E, Method 2019 (Total samples from three different assembly lots at each SAT)	15	15	15	Pass
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT	30	30	30	Pass
Internal/external visual Total samples from three different assembly lots at each SAT	75	75	75	Pass

1. Package qualification results are leveraged from other previously qualified WLP packages, including PM8998, PM8994, and PM8026, that are similar to this configuration.

7.3 Reliability qualifications summary: MagnaChip

Table 7-5 Silicon reliability results: MagnaChip

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A Total samples from three different wafer lots	240	Pass DPPM < 1000 [1]
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A Total samples from three different wafer lots	240	Pass FIT < 50 [1]
Mean time to failure (MTTF) t = 1/λ in million hours Total samples from three different wafer lots	240	Pass MTTF > 20 [1]

Table 7-5 Silicon reliability results: MagnaChip

Tests, standards, and conditions	Sample size	Result
ESD – HBM rating JESD22-A114-F Target: 1500 V Total samples from one wafer lot	3	Pass 1500 V
ESD – CDM rating JESD22-C101-D Target: 500 V Total samples from one wafer lot	3	Pass 500 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA Temperature: 85°C Total samples from one wafer lot	6	Pass
Latch-up (V supply overvoltage): EIA/JESD78A Trigger voltage: each VDD pin, stress at 1.5 × V_{DD} maximum per the device specification Temperature: 85°C Total samples from one wafer lot	6	Pass

1. The cumulative DPPM, FIT, and MTTF is based on multiple products under the GF 180 nm process.

Table 7-6 Package reliability results for MagnaChip [1]

Tests, standards, and conditions	ATC assembly source sample size	SCS assembly source sample size	Result
Moisture resistance test (MRT): J-STD-020C Reflow at 260°C +0/-5°C Total samples from three different assembly lots	693	693	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8 to 10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	231	231	Pass
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hour duration or 110°C/85% RH and 264 hour duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C +0/-5°C Total samples from three different assembly lots	231	231	Pass

Table 7-6 Package reliability results for MagnaChip [1] (cont.)

Tests, standards, and conditions	ATC assembly source sample size	SCS assembly source sample size	Result
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96 hour duration or 110°C/85% RH and 264 hour duration Preconditioning: JESD22-A113-F MSL 1, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	96	96	Pass
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hours Total samples from three different assembly lots	231	231	Pass
Flammability **Note**: flammability test – not required UL-STD-94 QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs are mounted are rated V-0 (better than V-1).	–	–	N/A
Physical dimensions: JESD22-B100-A Case outline drawing: QTI internal document Total samples from three different assembly lots at each SAT	30	30	Pass
Die Shear MIL-STD-883E, Method 2019 (Total samples from three different assembly lots at each SAT)	15	15	Pass
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT	30	30	Pass
Internal/external visual Total samples from three different assembly lots at each SAT	75	75	Pass

1. Package qualification results are leveraged from other previously qualified WLP packages, including PM8953, that are similar to this configuration.

7.4 Qualification sample description

Table 7-7 Device characteristics

Category	Definition
Device name	PM670
Package type	219 WLPSP
Package body size	5.05 mm × 5.64 mm × 0.53 mm
Ball composition	SAC405
Fab process	0.18 µm CMOS
Fab sites	■ TSMC ■ GLOBALFOUNDRIES ■ MagnaChip
Assembly sites	■ Amkor, China ■ STATS ChipPAC, Singapore ■ ASE, Taiwan
Solder ball pitch	0.35 mm

8 Revision history

Bars appearing in the margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	July 2017	Initial release
B	February 2018	■ Global: □ Updated TBD values □ Removed references to Qnovo ■ Table 2-2 Pin descriptions – input power management functions: □ Updated the functional description for pad numbers 122, 133, 165, 177, 194, 204, and 214 □ Updated the configurable function for GPIO_11 and GPIO_13 ■ Added Section 3 Electrical specifications ■ Added the following sections to Chapter 4 Mechanical information: □ Section 4.2 Part marking □ Section 4.3 Device ordering information □ Section 4.4 Device moisture-sensitivity level □ Section 4.5 Thermal characteristics ■ Added the following chapters: □ Chapter 5 Carrier, storage, and handling information □ Chapter 6 PCB mounting guidelines □ Chapter 7 Part reliability
C	May 2018	■ Global: Updated the document for PM670/PME605 support

Revision	Date	Description
D	June 2018	■ Section 1.3 Comparison between PM670 and PME605: Added this section ■ Section 3.6 Output power management: Updated the details for PME605. ■ Table 2-2 Pin descriptions – input power management functions: Updated the functional description for pin 122 and 133. ■ Table 2-3 Pin descriptions – output power management functions: Updated the functional description for LDO inputs ■ Figure 3-1 PM670 input power management functional block diagram: Updated the block diagram ■ Figure 3-2 PME605 input power management functional block diagram: Added the block diagram ■ Table 3-10 SMPS regulator summary for PM670: Added the SMPS regulator summary values ■ Table 3-11 Linear/low-voltage regulator summary for PM670: Added the linear/low-voltage regulator summary values ■ Table 3-37 PME605 power-on sequence: Added the power-on sequence for PME605 ■ Figure 4-2 PM670/PME605 device marking (top view, not to scale): Updated the device marking diagram
E	September 2018	■ Global: Updated the entire document to align with changes as per the plan of record. Read document in its entirety ■ Table 4-4 Device identification details for PME605: Updated the device identification details for ES1 and ES2 samples
F	January 2019	■ Global: □ Deleted WiPower information and updated the wireless charging support □ Deleted P50SP parameter throughout the document ■ Table 2-7 *Pin descriptions – general-purpose input/output functions*: Added the fixed supply GPIO options ■ Table 3-7 *Battery charger specifications*: □ Updated the specification for CC voltages and parameters when PMIC is source and sink □ Updated the fast-charge current accuracy conditions □ Deleted the charge-termination current accuracy parameter and conditions □ Updated the low battery voltage detector parameter and conditions □ Added a footnote for fast-charge current range conditions

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

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