Qualcomm Technologies, Inc.

PM660

Device Revision Guide

80-P7905-4 Rev. F

May 10, 2018

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

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Revision history

Revision	Date	Description
A	January 2017	Initial release
B	March 7, 2017	■ Table 2-2, Device identification code/ordering information details: Updated the pre-ES and ES sample details ■ Table 3-1, PMIC known issues – all sample types and revisions: □ Updated the sample type as ES □ Added Issue 4-2, The SDM660 device fails to power on during dead battery or no battery boot □ Added Issue 4-3, Residual clock of very low amplitude seen on RFCLKx □ Added Issue 4-4, PM660 XO frequency drift □ Added Issue 5-2, When BATFET is open during charging, an unexpected battery current is consumed internally under high VBATT condition □ Added Issue 5-4, PM660 fails to detect an On-The-Go device during a regular reboot □ Added Issue 5-5, Leakage on USB_IN upon battery insertion □ Added Issue 5-6, Charger slow plug-in fails due to the default FMB configuration □ Added Issue 5-7, VCONN circuit damage upon 15 V VBUS insertion ■ Issue 4-1, Unexpected system shutdown when VPH_PWR is below 3.3 V/3.6 V: Updated details in the workaround ■ Added Issue 4-2, The SDM660 device fails to power on during dead battery or no battery boot ■ Added Issue 4-3, Residual clock of very low amplitude seen on RFCLKx ■ Added Issue 4-4, PM660 XO frequency drift ■ Added Issue 5-2, When BATFET is open during charging, an unexpected battery current is consumed internally under high VBATT condition ■ Added Issue 5-4, PM660 fails to detect an On-The-Go device during a regular reboot ■ PM660 fails to detect an On-The-Go device during a regular reboot ■ Added Issue 5-5, Leakage on USB_IN upon battery insertion ■ Added Issue 5-6, Charger slow plug-in fails due to the default FMB configuration ■ Added Issue 5-7, VCONN circuit damage upon 15 V VBUS insertion

Revision	Date	Description
C	April 2017	■ Table 2-2, Device identification code/ordering information details: Updated the device identification details for CS samples ■ Table 3-1, PMIC known issues – all sample types and revisions: □ Updated the values for CS samples □ Added Issue 4-5, KPD_PWR_N PON active signal debounce does not work for deassertion glitches □ Updated Issue 5-4, PM660 fails to detect an On-The-Go device during a regular reboot □ Added Issue 5-8, PM660 fails to detect the charger removal or the OTG during sleep wake up □ Added Issue 5-9, PM660 charger current has a periodic dip every 700 µs □ Added Issue 5-10, PM660 charger fails to meet 100 ms Qualcomm® WiPower™ PON timing requirement □ Added Issue 5-11, PM660 USB_EN pin has a glitch during dead battery or no battery □ Added Issue 5-12, APSD runs only after both VBUS and CC are deglitched □ Added Issue 5-13, Certain low power rated QC3/QC2 adapters collapse during large system load resulting in failure to charge □ Added Issue 5-14, Legacy cable cannot be detected reliably □ Added Issue 5-15, Incorrect APSD detection during PON with no battery or weak battery □ Added Issue 5-16, Device does not boot when placed on WiPower PTU even after several seconds □ Added Issue 6-1, PM660 200 kHz standby oscillator drifts with die temperature change ■ Added Issue 4-5, KPD_PWR_N PON active signal debounce does not work for deassertion glitches ■ Updated Issue 5-4, PM660 fails to detect an On-The-Go device during a regular reboot ■ Added Issue 5-8, PM660 fails to detect the charger removal or the OTG during sleep wake up ■ Added Issue 5-9, PM660 charger current has a periodic dip every 700 µs ■ Added Issue 5-10, PM660 charger fails to meet 100 ms Qualcomm® WiPower™ PON timing requirement ■ Added Issue 5-11, PM660 USB_EN pin has a glitch during dead battery or no battery ■ Added Issue 5-12, APSD runs only after both VBUS and CC are deglitched ■ Added Issue 5-13, Certain low power rated QC3/QC2 adapters collapse during large system load resulting in failure to charge ■ Added Issue 5-14, Legacy cable cannot be detected reliably ■ Added Issue 5-15, Incorrect APSD detection during PON with no battery or weak battery ■ Added Issue 5-16, Device does not boot when placed on WiPower PTU even after several seconds ■ Added Issue 6-1, PM660 200 kHz standby oscillator drifts with die temperature change
D	May 2017	■ Table 3-1, PMIC known issues – all sample types and revisions: Added Issue 4-6, VCOIN feature may prevent phones from powering on ■ Added Issue 4-6, VCOIN feature may prevent phones from powering on

Revision	Date	Description
E	October 2017	■ Table 2-2 Device identification code/ordering information details: □ Added the device identification details for CS 2.0 samples. □ Added the footnote to indicate the fab sources used for CS 2.0 samples. ■ Table 3-1 PMIC known issues – all sample types and revisions: Updated for CS 2.0 ■ Issue 6 VCOIN feature may prevent phones from powering on: Updated to indicate that this issue is fixed in CS Rev. 2.0. ■ Updated the affected revisions for the following issues: □ Issue 3 Residual clock of very low amplitude seen on RFCLKx □ Issue 4 PM660 XO frequency drift □ Issue 5 KPD_PWR_N PON active signal debounce does not work for deassertion glitches □ Issue 2 When BATFET is open during charging, an unexpected battery current is consumed internally under high Vbatt condition □ Issue 3 Battery continues to discharge when protection FETs open with in battery pack differential sensing □ Issue 5 Leakage on USB_IN upon battery insertion □ Issue 6 Charger slow plug-in fails due to the default FMB configuration □ Issue 7 VCONN circuit damage upon 15 V VBUS insertion □ Issue 8 PM660 fails to detect the charger removal or the OTG during sleep wake up □ Issue 9 PM660 charger current has a periodic dip every 700 µs □ Issue 11 PM660 USB_EN pin has a glitch during dead battery or no battery □ Issue 12 APSD runs only after both VBUS and CC are deglitched □ Issue 13 Certain low power rated QC3/QC2 adapters collapse during large system load resulting in failure to charge □ Issue 14 Legacy cable cannot be detected reliably □ Issue 15 Incorrect APSD detection during PON with no battery or weak battery □ Issue 16 Device does not boot when placed on WiPower PTU even after several seconds □ Issue 1 PM660 200 kHz standby oscillator drifts with die temperature change
F	May 2018	■ Table 3-1 *PMIC known issues – all sample types and revisions*: □ Updated the workaround for Issue 4-6 □ Updated the workaround for Issue 5-8

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Tables

1 Introduction

Technical information for the PM660 device is primarily covered by the documents listed in Table 1-1. Released PM660 documents are posted on the Qualcomm® CreatePoint website (https://createpoint.qti.qualcomm.com) and are available for download.

Table 1-1 Primary PM660 documents

Document number	Document title
80-P7905-1	*PM660 Power Management IC Device Specification*
80-P7905-2X	*PM660 Hardware Register Description*
80-P7905-4 (this document)	*PM660 Device Revision Guide*

1.1 Scope and intended audience

This device revision guide identifies issues with all PM660 samples released to date. It is intended for new product developers who are designing, testing, or evaluating products that include the PM660 device.

2 Device identification

The PM660 device is identified by markings on its top surface and by the contents of an identification register; these identification techniques are described in Section 2.1 and Section 2.2, respectively. Further details about each sample type are presented in Section 2.3.

2.1 Part marking

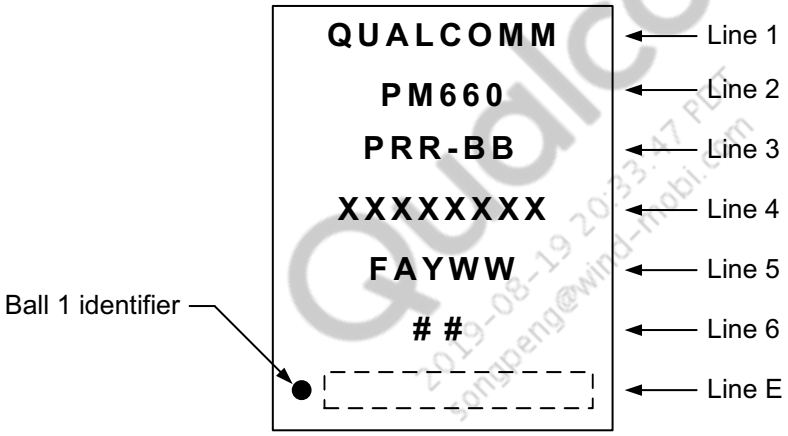

Figure 2-1 PM660 device marking (top view, not to scale)

Table 2-1 PM660 device marking line definitions

Line	Marking	Description
1	QUALCOMM	Qualcomm name or logo
2	PM660	Qualcomm Technologies, Inc. (QTI) product name
3	PRR-BB	P = product configuration code ■ See Table 2-2 for the assigned values. RR = product revision ■ See Table 2-2 for the assigned values. BB = feature code ■ See Table 2-2 for the assigned values.
4	XXXXXXXX	XXXXXXXX = traceability number

Table 2-1 PM660 device marking line definitions (cont.)

Line	Marking	Description
5	FAYWW	F = supply source code ■ F = F for TSMC ■ F = H for GLOBALFOUNDRIES ■ F = E for MagnaChip A = assembly site code ■ A = U for Amkor, China ■ A = M for STATS ChipPAC, Singapore ■ A = E for ASE, Taiwan Y = single-digit year WW = work week (based on calendar year)
6	##	## = 2-digit wafer number
E	Blank or variable	Additional content as necessary

2.2 Device identification for each sample type

Device identification details for all samples available to date are summarized in Table 2-2.

Table 2-2 Device identification code/ordering information details

Device	Product configuration code (*P*)	Product revision (*RR*)	Hardware revision number	Sample type	S value [1]	BB value [2]
PM660	0	00	1.0	Pre-ES	0	N/A
PM660	0	01	1.1	ES	1	N/A
PM660	0	01	1.1	CS	1	01
PM660 [3]	0	02	2.0	CS2	1	N/A

1. S is the source configuration code that identifies all of the qualified die fabrication-source combinations available when the particular sample type was shipped.
2. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants.
3. The PM660 2.0 samples are sourced from the TSMC and GLOBALFOUNDRIES fab sources.

2.3 Sample testing

2.3.1 Engineering samples (ES)

These devices undergo limited testing and sometimes have significant feature limitations. They are suitable to assist with PCB development, to conduct board-level electrical evaluation tests, and to explore manufacturing considerations. Engineering samples should not be used for product-level qualification.

2.3.2 Commercial samples (CS)

These devices undergo full production-level testing, and meet the specifications and features described in the device specification, except as otherwise noted in this document. They have passed device-level qualification. Commercial samples are suitable for performance testing, and also for product-level production and qualification.

3 Known issues

3.1 Summary of known issues

All known issues for each revision of the PM660 device are summarized in Table 3-1. The text within the *Issue* column provides links to the sections of this document that explain the issues, regardless of the sample type (or types) on which they occur. An *X* in one or more of the sample type columns indicates that the issue occurs in the corresponding sample type.

The following information is provided for each issue:

- Issue description
- Impact to system performance
- Possible workarounds to minimize impact

Table 3-1 PMIC known issues – all sample types and revisions

Issue #	Issue description	Workaround	PM660 Pre-ES P = 0 RR = 00 [1]	PM660 ES P = 0 RR = 01	PM660 CS P = 0 RR = 01	PM660 CS2 P = 0 RR = 02
General issues						
Issue 4-1	Unexpected system shutdown when VPH_PWR is below 3.3 V/3.6 V	Always maintain VPH_PWR above 3.8 V so that the MBG mux always uses VPH_PWR under all scenario.	X			
Issue 4-2	The SDM660 device fails to power on during dead battery or no battery boot	No workaround	X			
Issue 4-3	Residual clock of very low amplitude seen on RFCLKx	No workaround	X	X	X	X
Issue 4-4	PM660 XO frequency drift	A software workaround is available with CR 2008185 and CR 2008480, which implements the ESR QUIET mode during the GPS active state. There is no hardware workaround for this issue.	X	X	X	X
Issue 4-5	KPD_PWR_N PON active signal debounce does not work for deassertion glitches	There is no hardware workaround for this issue. A software workaround (CR2032520) is available	X	X	X	X
Issue 4-6	VCOIN feature may prevent phones from powering on	This issue is fixed in CS2 devices (RR = 02).	X	X	X	
Charger issues						
Issue 5-1	Input overvoltage lockout causes the specification to fail for a 9 V input or a 5 V to 9 V setting	No workaround	X			
Issue 5-2	When BATFET is open during charging, an unexpected battery current is consumed internally under high Vbatt condition	No workaround	X	X	X	X
Issue 5-3	Battery continues to discharge when protection FETs open with in battery pack differential sensing	No workaround	X	X	X	X

Table 3-1 PMIC known issues – all sample types and revisions (cont.)

Issue #	Issue description	Workaround	PM660 Pre-ES P = 0 RR = 00 [1]	PM660 ES P = 0 RR = 01	PM660 CS P = 0 RR = 01	PM660 CS2 P = 0 RR = 02
Issue 5-4	PM660 fails to detect an On-The-Go device during a regular reboot	This issue is partially corrected in Rev 1.1 CS Software workaround available.	X	X		
Issue 5-5	Leakage on USB_IN upon battery insertion	Software workaround available (CR 2005474). Hardware workaround available, but has limitations.	X	X	X	X
Issue 5-6	Charger slow plug-in fails due to the default FMB configuration	FMB will be disabled by default	X	X	X	X
Issue 5-7	VCONN circuit damage upon 15 V VBUS insertion	Hardware workaround available	X	X	X	X
Issue 5-8	PM660 fails to detect the charger removal or the OTG during sleep wake up	Software workaround available (CR 2020299)	X	X	X	X
Issue 5-9	PM660 charger current has a periodic dip every 700 µs	No workaround	X	X	X	X
Issue 5-10	PM660 charger fails to meet 100 ms Qualcomm® WiPower™ PON timing requirement	This issue is fixed in Rev 1.1 CS	X	X		
Issue 5-11	PM660 USB_EN pin has a glitch during dead battery or no battery	No workaround	X	X	X	X
Issue 5-12	APSD runs only after both VBUS and CC are deglitched	No workaround	X	X	X	X
Issue 5-13	Certain low power rated QC3/QC2 adapters collapse during large system load resulting in failure to charge	Software workaround available (CR 2003030)	X	X	X	X
Issue 5-14	Legacy cable cannot be detected reliably	Software workaround available (CR 2015561)	X	X	X	X
Issue 5-15	Incorrect APSD detection during PON with no battery or weak battery	Software workaround available (CR 922874)	X	X	X	X
Issue 5-16	Device does not boot when placed on WiPower PTU even after several seconds	There is no workaround for this issue.	X	X	X	X

Table 3-1 PMIC known issues – all sample types and revisions (cont.)

Issue #	Issue description	Workaround	PM660 Pre-ES P = 0 RR = 00 [1]	PM660 ES P = 0 RR = 01	PM660 CS P = 0 RR = 01	PM660 CS2 P = 0 RR = 02
Fuel-gauge issues						
Issue 6-1	PM660 200 kHz standby oscillator drifts with die temperature change	There is no hardware workaround for this issue. A software workaround (CR2032069) is available	X	X	X	X
User-interface issues						
No known issues						

1. RR values are detailed in Table 2-2.

4 General issues

4.1 IC-level interfaces

Issue 4-1 Unexpected system shutdown when VPH_PWR is below 3.3 V/3.6 V

Description	When VPH_PWR ramps down to less than a certain specific voltage, the internal MBG multiplexer selector switches to VREG_BOB. This creates a coupling to PON reference, resulting in an MBG fault; hence the PMIC shuts down. An issue can occur in the following two cases: 1: When VREG_BOB is 3.3 V and VPH_PWR falls below 3.3 V 2: When VREG_BOB is 3.6 V and VPH_PWR falls below 3.6 V
Impact	There is an unexpected system shutdown during low VBAT.
Workaround	Always maintain VPH_PWR above 3.8 V so that the MBG mux always uses VPH_PWR under all scenario. This issue will be corrected in the next revision.
Affected revs	RR = 00

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Issue 4-2 The SDM660 device fails to power on during dead battery or no battery boot

Description	The GPIO1 pin of PM660 is used as an optional pin to decode the SDM660 and SDM630 platform. If the GPIO1 pin is configured as Hi-Z, the SDM660 platform is detected, and if the GPIO1 pin is configured as GND, the SDM630 platform is detected. During a dead battery or no battery boot condition, GPIO1 pin always falsely detects the SDM630 platform. This detection does not power up the SDM660 device completely, and PS_HOLD is never asserted.
Impact	The SDM660 device does not boot. If there is a protected battery, then PM660 cannot recover the battery because the system keeps rebooting and the charger never gets enabled.
Workaround	There is no workaround for this issue. This issue will be corrected in the next revision.
Affected revs	RR = 00

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4.2 General housekeeping

Issue 4-3 Residual clock of very low amplitude seen on RFCLKx

Description	When RFCLK1 is disabled and RFCLK2 is enabled, a residual clock of very low amplitude is observed on RFCLK1. This condition is also true when RFCLK2 is disabled and RFCLK1 is enabled. This issue occurs due to the internal feed through to the clock output buffer when one of the other clock buffers is enabled.
Impact	There is no system impact, because the residual clock has a very low amplitude.
Workaround	There is no workaround for this issue.
Affected revs	RR = 00, RR = 01, and RR = 02

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Issue 4-4 PM660 XO frequency drift

Description	The GPS NBIQ test fails due to the XO frequency drift. Periodic drift coincides with the FG ESR pulse measurement. The ESR pulse measurement couples thermally to XO_THERM measurement resulting in drift.
Impact	GPS NBIQ test failure
Workaround	A software workaround is available with CR 2008185 and CR 2008480, which implements the ESR QUIET mode during the GPS active state. There is no hardware workaround for this issue.
Affected revs	RR = 00, RR = 01, and RR = 02

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4.3 PON

Issue 4-5 KPD_PWR_N PON active signal debounce does not work for deassertion glitches

Description	Irrespective of the debounce timer set, KPD_PWR_N PON active signal debounce does not work for glitch pulses less than ~80 µs. This is due to the internal digital hardware logic race condition that results in invalid IRQs.
Impact	Unexpected behavior of screen wake up or off during KPD_PWR_N press.
Workaround	There is no hardware workaround for this issue. A software workaround (CR2032520) is available that ignores invalid IRQs due to KPD_PWR_N debounce after valid IRQ.
Affected revs	RR = 00, RR = 01, and RR = 02

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Issue 4-6 VCOIN feature may prevent phones from powering on

Description	The VCOIN feature, which is used for Sudden Momentary Power Loss (SMPL) and Real Time Clock (RTC), prevents the phones from powering on. If the main battery is removed and the VCOIN node discharges and has a residual voltage, the phone may not power on when the main battery is reconnected and the power key is pressed. The root cause investigation is going on.
Impact	When the main battery is connected to the phone while a residual voltage is on VCOIN, phones may not power on. This can occur in the factory or when an end user reconnects a battery to the phone.
Workaround	The VCOIN feature is exclusively used for SMPL and powering the RTC when the main battery is disconnected. Since removing the phone batteries is not common, it is recommended to disable the VCOIN feature. To disable the VCOIN feature, the coin cell charger must be disabled in SBL. Note that the coin cell charger is disabled by default in hardware (only enabled during SBL). Keeping the coin cell charger disabled is all that is necessary to ensure that the VCOIN feature is disabled. As a precautionary measure, it is also recommended to leave the VCOIN node floating (remove the VCOIN bulk capacitor or coin cell battery). A PCB change is not necessary to float VCOIN; not installing the VCOIN bulk cap or coin cell battery is all that is needed. Please contact Qualcomm Technologies, Inc. for software support to disable VCOIN charging. The impact of not using the VCOIN feature is: ■ The RTC will not operate when the main phone battery is disconnected. The RTC, however, will operate normally when the main phone battery is connected. ■ SMPL events, such as a short battery removal, will power down the phone instead of automatically powering back on. The only impact is that the user has to press the power key, instead of SMPL automatically powering on the phone. Note that SMPL will continue to operate normally when the battery FET is opened for BCL mitigation Level - F. Refer to the *PM660 and PM660A/PM660L Power Management ICs Design Guidelines/Training Slides* (80-P7905-5A) for the PM660 mitigation level actions. This issue is fixed in Rev 2.0 CS.
Affected revs	RR = 00 and RR = 01

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5 Charger issues

Issue 5-1 Input overvoltage lockout causes the specification to fail for a 9 V input or a 5 V to 9 V setting

Description	The threshold for overvoltage lockout (OVLO) is kept at 10.3 V, although the maximum operating voltage is only 10 V. This causes the specification to fail on the operating input range.
Impact	Potential damage or overstressing of device at higher input voltage can occur.
Workaround	There is no workaround for this issue. This issue will be corrected in the next revision.
Affected revs	RR = 00

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Issue 5-2 When BATFET is open during charging, an unexpected battery current is consumed internally under high Vbatt condition

Description	When the BATFET is open (after charging has been terminated or disabled) and Vbatt is high, it is observed that a few mAs of battery current (varies from part to part) are discharged into the PMIC. The current can go up to a maximum of 6 mA on a few randomly tested samples.
Impact	There is no major system impact. There will be a state of charge (SoC) drop due to the leakage. This drop can be masked through software, and the UI can be made to display 100% for an improved user experience, until Vbatt reaches the recharge threshold. This feature can be enabled by adding the `qcom,hold-soc-while-full` property in the .dtsi file.
Workaround	There is no hardware workaround for this issue. The software can adjust the SoC to mask the drop.
Affected revs	RR = 00, RR = 01, and RR = 02

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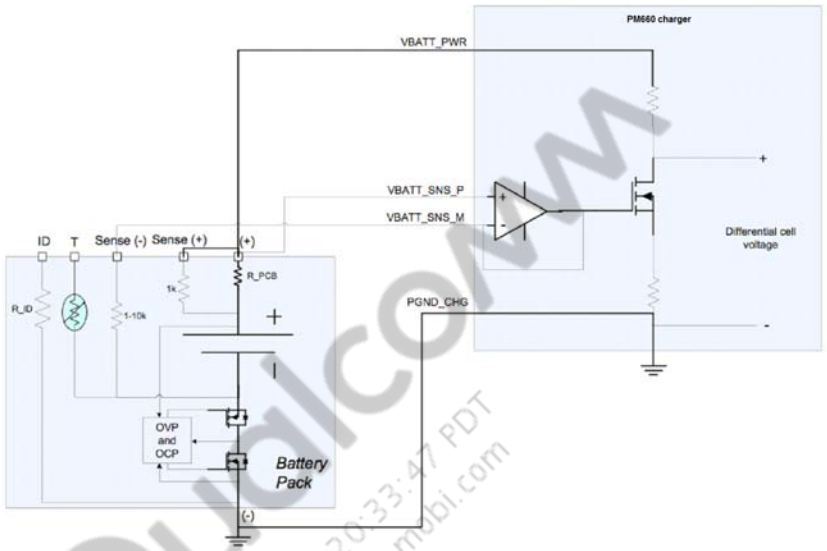
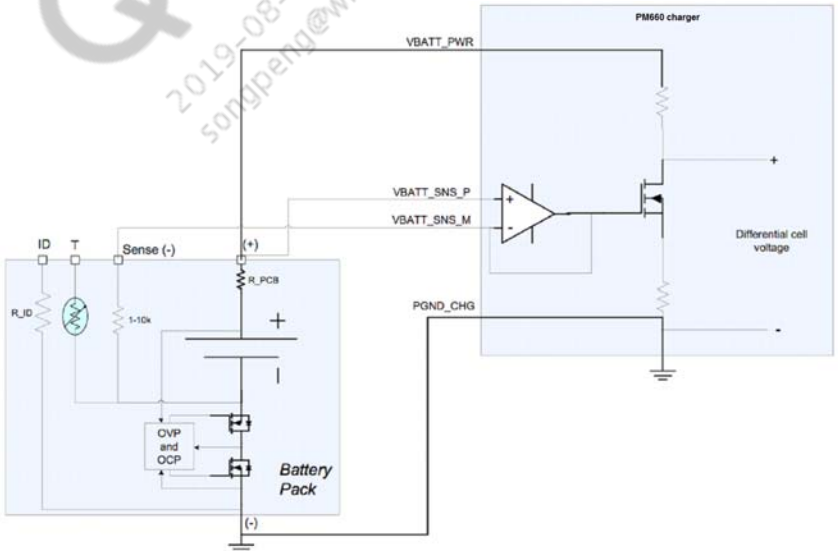
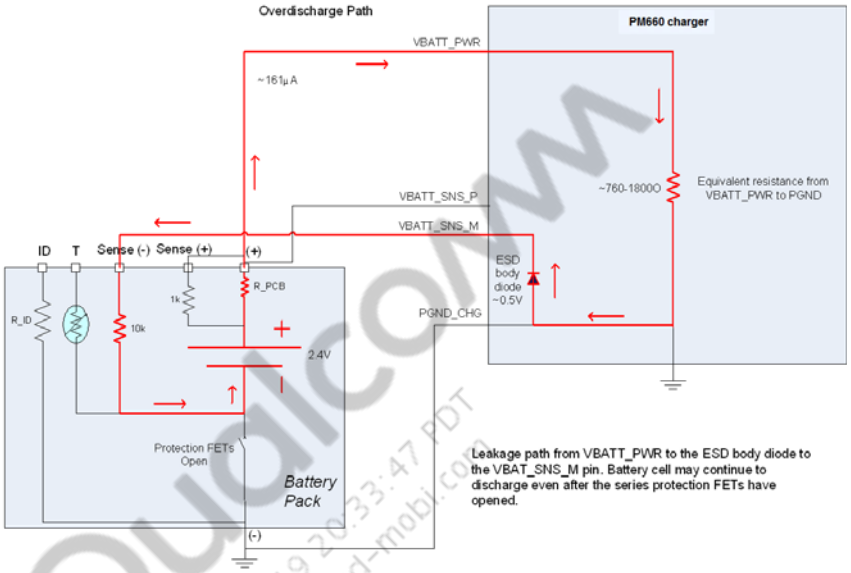
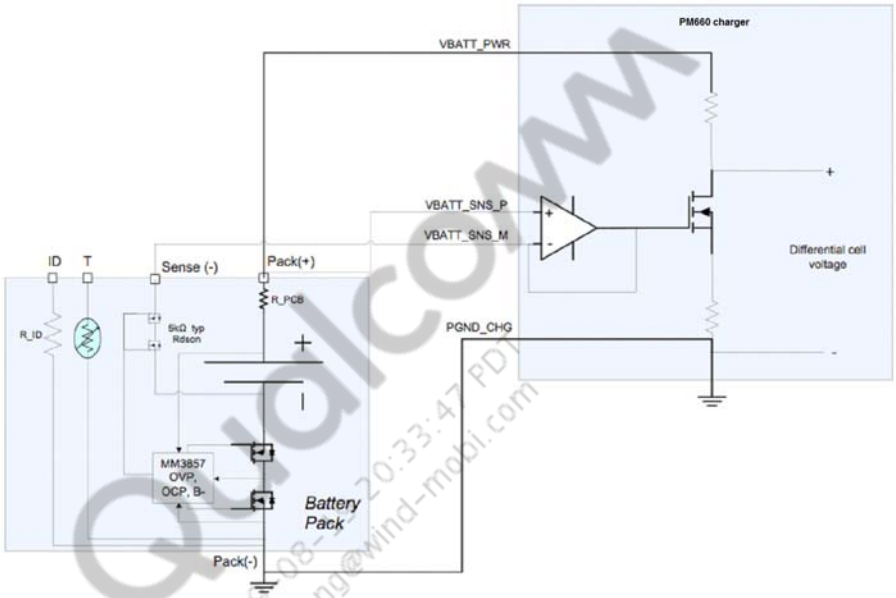
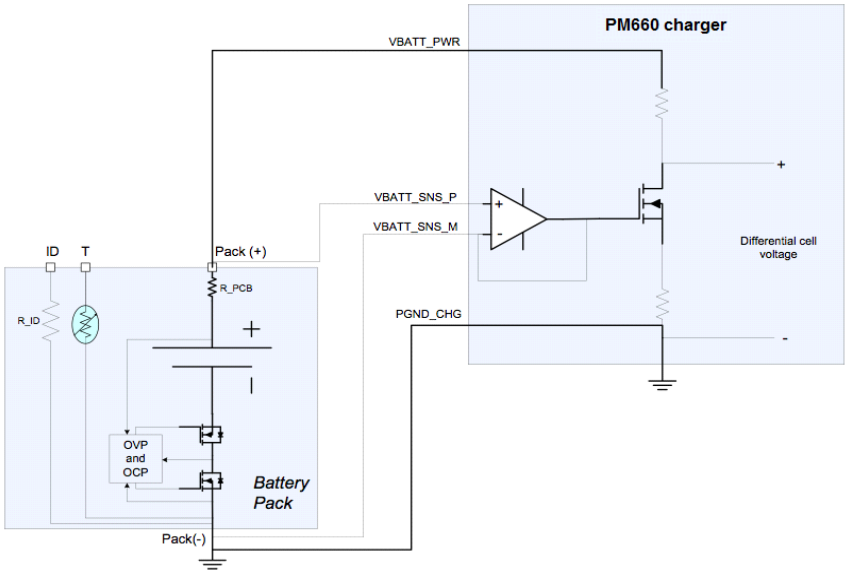
Issue 5-3 Battery continues to discharge when protection FETs open with in battery pack differential sensing

Description	PM660 has the ability to differentially sense at the battery connector or internal to the battery pack and charge a battery. Example implementations are shown below for in battery pack differential battery voltage sensing: ■ Typical 6-pin differential battery pack:  ■ Typical 5-pin differential battery pack: 

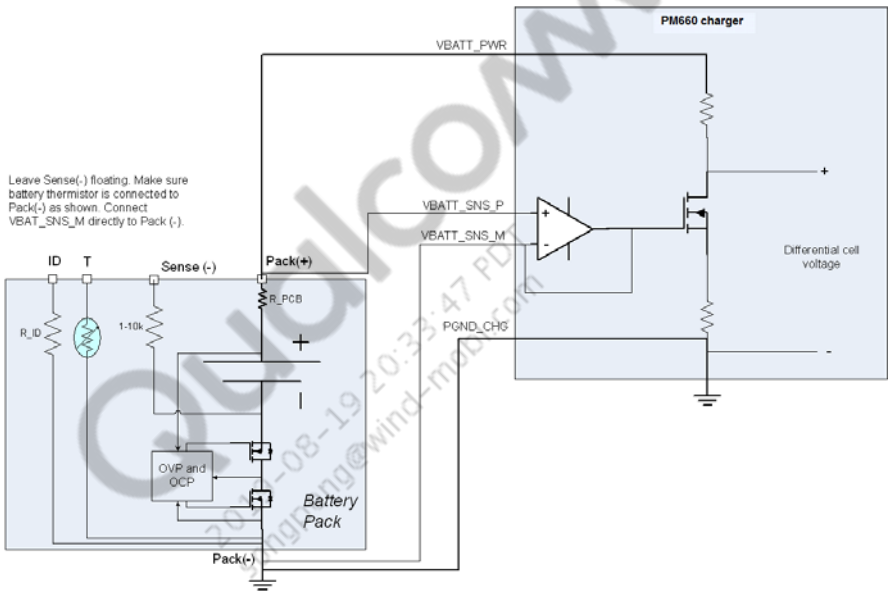
Issue 5-3 Battery continues to discharge when protection FETs open with in battery pack differential sensing (cont.)

Description (cont.)	When using the “in battery pack” differential sensing feature, a leakage path on the negative sense line causes the battery to continuously discharge even with battery protection FETs open. For example, a 2.4 V battery has a leakage of ~161 µA with 10 k series resistor on VBAT_SNS_M. The leakage is higher for a lower series resistance. As such, the “in battery pack” differential sensing feature cannot be used at this time. 
Impact	The battery cell continues to discharge even when protection FETs open. This could result in an overdischarged battery from becoming further discharged.

Issue 5-3 Battery continues to discharge when protection FETs open with in battery pack differential sensing (cont.)

Workaround	QTI recommends against using "in battery pack" differential sensing on the SDM660 platform for now. QTI is working on a potential solution to resolve this differential sensing issue. The potential solution involves using a battery protection IC in the battery pack that disconnects VBAT_SNS_M when the OVP/OCP protection FETs open, thus breaking the discharge path. The timeframe for this solution to be available is mid 2017. QTI still supports differential sensing to the battery pack connector. Potential solution with Mitsumi MM3857 battery protection IC:  OEMs that were planning to use a 5-pin or 6-pin differential battery pack, are advised to migrate to a 4-pin nondifferential battery pack as shown below: Recommendation for OEMs that can change their differential pack to nondifferential pack: 

Issue 5-3 Battery continues to discharge when protection FETs open with in battery pack differential sensing (cont.)

Workaround (cont.)	If migrating to a 4-pin battery pack is not possible due to certain constraints, the OEM may continue to use the differential battery pack with the following modifications: 1. Sense(-) pin of the battery pack must be left floating. 2. VBAT_SNS_M of PM660 must be connected to the negative terminal of the battery pack. 3. The battery thermistor must be connected after the protection FETs. Connecting the thermistor before the protection circuit causes errors in BAT_THERM measurement at high charge and discharge currents. Recommendation for OEMs that cannot change their differential pack to nondifferential pack: 
Affected revs	RR = 00, RR = 01, and RR = 02

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Issue 5-4 PM660 fails to detect an On-The-Go device during a regular reboot

Description	PM660 occasionally fails to detect an OTG device if operated in µUSB mode. In Micro USB mode, GPIO9 must be grounded and CC1_ID must be connected to USB ID. During a regular PON, the configuration to change the mode from Type-C to Micro USB violates the timing requirement that results in locking up the status registers. The lock up can be recovered only after the battery is re-inserted. The Type-C module is enabled in PM660 by default. If µUSB must be configured, then Type-C must be disabled. To disable Type-C, perform the following sequential steps: 1. Sink enable command disabled 0x1368[2] = 0 2. Disable Type-C detection 0x1368[0]=1 3. Wait for approximately 200 ms 4. Change the value to 0, that is, 0x1358[0] = 0 (for Type-C mode) 5. Wait for approximately 10 ms 6. Enable Type-C mode 0x1368[0] = 0 7. Wait for approximately 100 ms 8. Disable Type-C mode 0x1368[0] = 1 9. Wait for approximately 200 ms 10. Change the value to 1, that is, 0x1358[0] = 1 (for µUSB mode) 11. Wait for approximately 10 ms 12. Enable Type-C detection 0x1368[0] = 0 If the above mentioned sequence is not followed, there could be a potential Type-C FSM failure that results in OTG detection failure, status register corruption, and so on.
Impact	The device fails to detect the OTG after a reboot and does not recover (unless a proper Type-C disable sequence is followed)
Workaround	This issue is partially corrected in Rev 1.1 CS. However, an additional software workaround is required to address multiple use cases. This issue can be fixed by following the sequence implemented in the software, for the CRs: 2017880: HLOS 2020297, 2020299: BOOT
Affected revs	RR = 00 and RR = 01

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Issue 5-5 Leakage on USB_IN upon battery insertion

Description	PM660 has an input coarse detection threshold of 1 V; if 1 V or higher voltage is present on USB_IN for ~20 ms, it triggers a PON. Insertion of a battery with higher charge can cause voltage leakage from USB_IN_MID to USB_IN via the front-porch FET. Due to the load absence on USB_IN, the leakage can be seen for a duration of up to 20 ms.
Impact	Upon battery insertion, if the leakage on USB_IN is greater than the coarse detection threshold for a duration of approximately 20 ms, the PM660 turns on.
Workaround	Software workaround: CR2005474 addresses this issue by monitoring PON REASON and USB_IN UV IRQ. Any false detection shuts down the device or continues to boot. Hardware workaround: OEMs can add an external pull-down resistor of 10 kΩ on USB_IN to reduce the potential risk of powering on automatically during device production. There are two limitations to this workaround: ■ With a 5 V input, an additional leakage of ~ 500 µA occurs on USB_IN. The maximum USB suspend current of the PM660 is 1 mA. The total current consumption during the USB suspend state is ~1.5 mA. ■ During the power source mode (OTG), OEMs see ~500 µA of additional current consumption due to the pull-down resistor.
Affected revs	RR = 00, RR = 01, and RR = 02

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Issue 5-6 Charger slow plug-in fails due to the default FMB configuration

Description	If the charger is slowly plugged in so that the CC pins make contact ~500 ms after VBUS has made contact, then the charger is deemed to be a noncompliant Type-C charger by PM660. In such a case, PM660 does not indicate charger plug-in orientation to the SDM device. The root cause of the problem is FMB being enabled by default. The PM660 device does FMB/non-compliant Type-C charger detection ~500 msec after VBUS is applied. Therefore, a slow plug-in can result in noncompliant charger detection since CC lines may be floating when this action is performed.
Impact	Upon a slow plug-in, the charger may be deemed a noncompliant Type-C charger. As PM660 does not indicate charger plug-in orientation to the SDM device, enumeration will be blocked for 60 seconds when the SDM660 enters EDL mode. This delays the software download to the handset.
Workaround	FMB will be disabled by default.
Affected revs	RR = 00, RR = 01, and RR = 02

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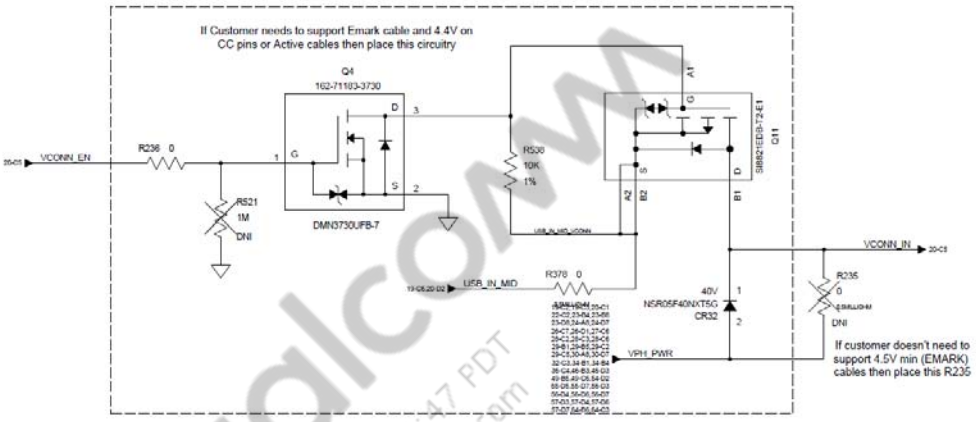
Issue 5-7 VCONN circuit damage upon 15 V VBUS insertion

Description	The VCONN_EN NFET has a drain-to-source capacitance that appears during high-voltage transients. This capacitance creates an RC circuit with the pull-up resistor from the gate of the PFET to USB_IN_MID. When high voltage is directly applied to USB_IN_MID, this capacitance acts as a short for some time, bringing the gate of the PFET low. As a result, the PFET turns on and VCONN_IN is connected to USB_IN_MID. VCONN_EN is left floating by the PM660 device unless a resistance is attached to the CC pins. Therefore, the PM660 device does not force the VCONN_EN NFET off. The VCONN circuit without workarounds: 
Impact	When a 15 V voltage is directly applied to USB_IN, the VCONN_IN pin is shorted to USB_IN_MID for a short time, and the VCONN circuit in the PM660 is damaged.
Workaround	The workaround for this issue involves three steps: 1. Add a 0.1 µF, 6.3 V capacitor in parallel to the pull-up resistor from the gate of the PFET to USB_IN_MID. This creates an AC short between USB_IN_MID and the gate of the PFET during high transient events. 2. Change the pull-up resistor to 100 kΩ to reduce the leakage current to the VCONN circuit. 3. Add a 10 kΩ pull-down resistor on VCONN_EN to prevent the VCONN_EN from floating.
Affected revs	RR = 00, RR = 01, and RR = 02

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Issue 5-8 PM660 fails to detect the charger removal or the OTG during sleep wake up

Description	To save power in sleep, configure the charger clock to 200 kHz on the SDM660 sleep entry sequence. If a charger or an OTG is connected and the device goes into sleep, changing the charger switching clock locks the charger module.
Impact	The system fails to detect the charger removal or detect the OTG device.
Workaround	The sleep exit sequence will be corrected in the next SBL version to unlock the charger. Also, the software CR 2020299 fixes this issue.
Affected revs	RR = 00, RR = 01, and RR = 02

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Issue 5-9 PM660 charger current has a periodic dip every 700 µs

Description	The PM660 charger current has periodic pulses every 700 µs. The dip in current is close to 250 mA in some conditions. This is due to the internal coupling of the current sense signal with the charger reference module.
Impact	There is no system impact as the current dips are of short duration.
Workaround	There is no workaround for this issue.
Affected revs	RR = 00, RR = 01, and RR = 02

Return to Table 3-1

Issue 5-10 PM660 charger fails to meet 100 ms Qualcomm® WiPower™ PON timing requirement

Description	PM660 WiPower PON timing from a dead or a deeply discharged battery fails to meet the 100 ms window to bring up the Bluetooth module and to acknowledge with the charging. The external soft start circuit to reduce the inrush and prevent the input from going into UVLO or OVLO must be less than 1 ms to prevent reverse boosting. The external soft start circuit will be updated in the *SDM660 + PM660 + PM660A/PM660L Reference Schematic* (80-P7747-41).
Impact	The device cannot be charged from a dead or deeply discharged battery from the WiPower charging pad.
Workaround	This issue is fixed in Rev 1.1 CS
Affected revs	RR = 00 and RR = 01

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Issue 5-11 PM660 USB_EN pin has a glitch during dead battery or no battery

Description	During a dead battery or no battery condition, the USB_EN can show an ~ 15 ms glitch while enabling the external OVPIC.
Impact	Unexpected turning on of the OVPIC for short duration before the debounce can occur.
Workaround	There is no workaround for this issue. OVPIC debounces USBIN for 50 ms prior to enabling the output when a charger is attached.
Affected revs	RR = 00, RR = 01, and RR = 02

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Issue 5-12 APSD runs only after both VBUS and CC are deglitched

Description	The PM660 device is configured to run the APSD only after both VBUS and CC are deglitched. This means that if a charger with CC pin floating is applied to the PM660 device, it is detected as an unknown charger. In this case, the PM660 device draws 500 mA from the charger and battery charging is enabled.
Impact	In factory, if only VBUS is applied to the handset with CC pin floating, the PM660 device detects the charger type as unknown. As a result, the SDM can take upto 60 sec to enter the download mode.
Workaround	There is no workaround for this issue. OEMs are recommended to make sure that in factory, they apply both VBUS and CC to PM660 in order to prevent the 60 sec delay from entering the download mode
Affected revs	RR = 00, RR = 01, and RR = 02

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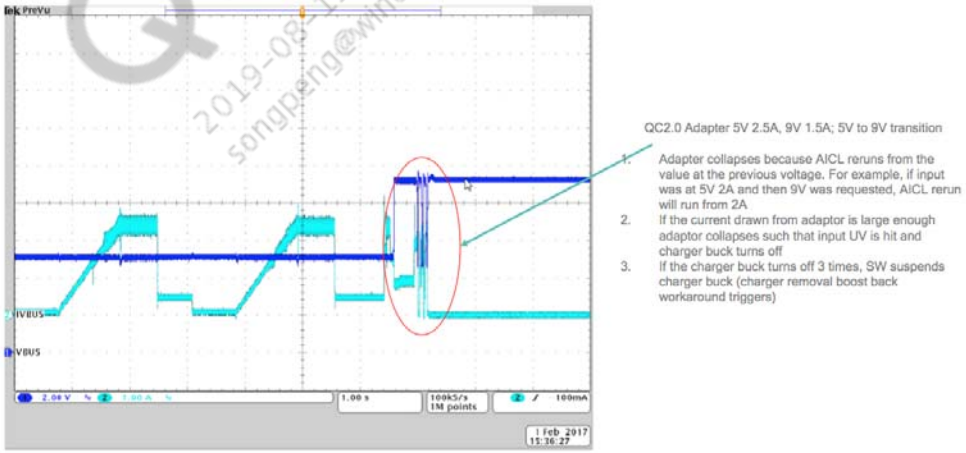
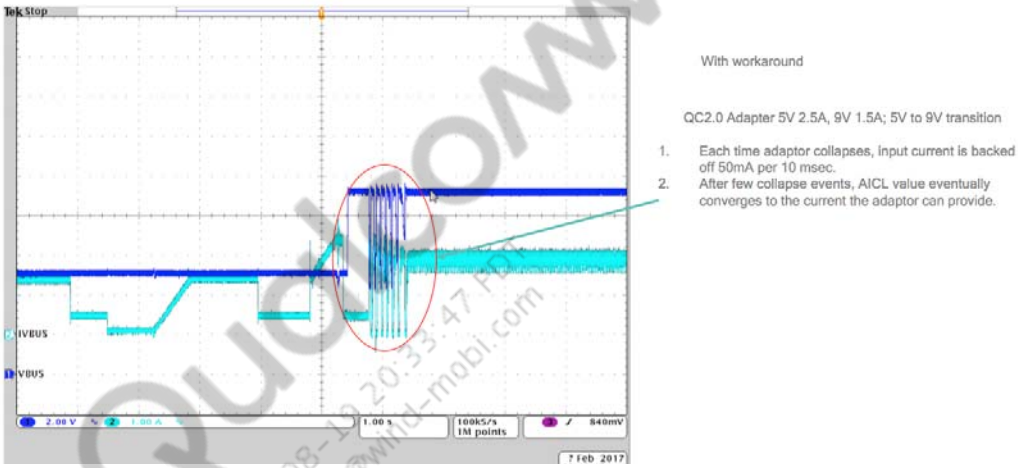
Issue 5-13 Certain low power rated QC3/QC2 adapters collapse during large system load resulting in failure to charge

Description	It is observed that certain low power rated QC3/QC2 adapters collapse when a voltage increment is requested due to large system load. If the adapter collapses below the input UVLO threshold for 20 msec, then the charger buck is turned off. If the charger buck is turned off three times in 1 second, then the software suspends the charger buck. 
Impact	The root cause of the adapter collapse is a bug in the way HW AICL runs. When a voltage increment is requested from a QC adapter, AICL is re-run at the new voltage from the value at the previous voltage. For example, in case of QC2 adapter, if input was at 5 V 2 A and then 9 V was requested, AICL is re-run from 2 A. This may result in collapsing a low power rated adapter such as one shown in plot above. The charger buck gets suspended because the charger removal boost back workaround kicks in. This software workaround looks at how many times the charge buck shutsdown in 1 second. If it shuts down 3 times in 1 second, then it is deemed that charger is accidentally reverse boosting and charger buck is suspended. The reason this software workaround is needed is because of a hardware bug, which prevents the PM660 device from running input missing poller to prevent accidental reverse boost upon charger removal.

Issue 5-13 Certain low power rated QC3/QC2 adapters collapse during large system load resulting in failure to charge (cont.)

Workaround	There is no workaround to prevent a low power rated charger adapter from collapsing when voltage increment is requested during a large system load. Each time the adapter collapses, the PM660 device decrements the input current by 50 mA per 10 ms before the charger buck is shutdown due to input UVLO. Eventually, after a few collapse events, the PM660 device converges at the right current that the adapter can provide. The software workaround to prevent accidental reverse boost must be modified to make sure that it does not suspend the charger buck when it shuts down 3 times in 1 sec. This is implemented in CR 2003030. The plot below show the adapter behavior with SW CR 2003030 implemented. As mentioned above, the adapter collapses a couple of times before the PM660 device converges to the right current that the adapter can provide. 
Affected revs	RR = 00, RR = 01, and RR = 02

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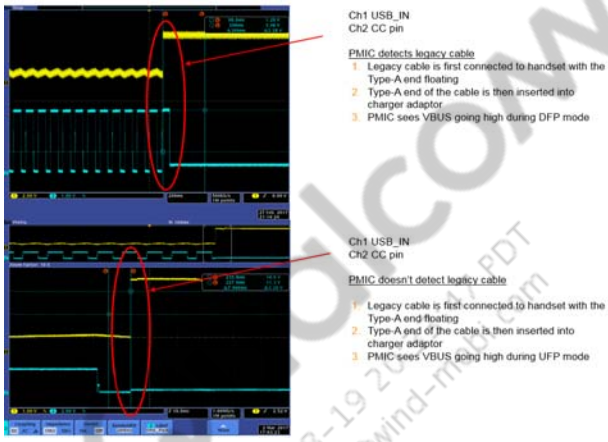
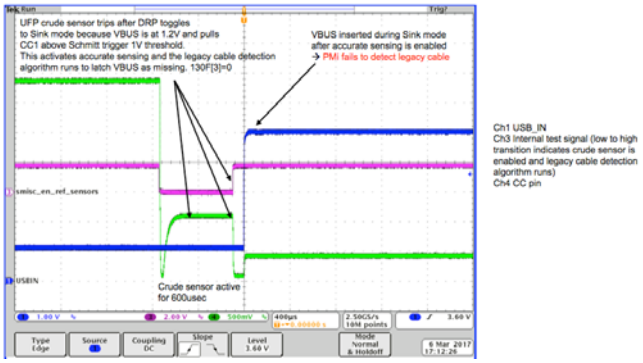
Issue 5-14 Legacy cable cannot be detected reliably

Description	The PM660 device has the ability to detect a legacy (Type-A to Type-C) cable from a non-legacy (Type-C to Type-C) cable by looking at when VBUS is attached with respect to CC pin. Furthermore, if a cable is detected as legacy cable and charger type is SDP/CDP, the PM660 device looks at the pull-up resistance (Rp) from CC to VBUS to deem whether the cable is compliant (Rp = 56 K) or non-compliant (Rp = 10 K or lower). If the cable is deemed non-compliant, then the hardware automatically limits the max input current limit to 500 mA/1500 mA in case of SDP/CDP. If a legacy cable is attached with a 10 K or lower Rp, then QC is blocked in HLOS by software to prevent damaging the CC pin. In HLOS software, PM660 is configured to operate in DRP mode where it continuously cycles between DFP and UFP mode. It is observed that PM660 fails to detect legacy cable in the following use case: ■ Legacy cable is first connected to handset with the Type-A end floating ■ Type-A end of the cable is then inserted into the charger adapter ■ PM660 sees VBUS going high during UFP mode If the PM660 device sees VBUS going high during DFP mode, then it detects the legacy cable successfully. See plots below for reference.  The root cause of the issue is related to leakage present on USB_IN in the above use case. When the PM660 device goes in DFP mode, it charges the USB_IN cap through Rp pull-up in the legacy cable. When the PM660 transitions to UFP mode, the leakage present on USB_IN causes the crude sensor on CC to trip and accurate sensing gets enabled. The legacy cable detection algorithm runs when accurate sensing is enabled and it looks for USB_IN voltage. If USB_IN is greater than 3.6 V then PM660 deems the cable as legacy cable; otherwise, it is deemed as non-legacy cable. 
Impact	This issue has two system impacts: 1. If a non-compliant legacy cable (Rp = 10 K or less) is connected to a legacy PC/laptop port and cable is misdetected as non-legacy, then PM660 may draw more current (as advertised by Rp) than what the port can provide. This may result in collapsing the ports. 2. If a non-compliant legacy cable with direct short from CC to VBUS (Rp = 0 Ohms) is connected to a Quick Charge adapter and cable is misdetected as non-legacy, then PM660 may request a voltage increment when load is high. A voltage higher than 6 V on VBUS can end up damaging the CC pin.

Issue 5-14 Legacy cable cannot be detected reliably (cont.)

Workaround	A software workaround (CR 2015561) has been identified that mitigates this problem. The workaround limits the max input current to 500 mA before the charger is attached. Upon charge attach if the charger type is SDP or CDP, then the max input current is limited to 500 mA or 1500 mA respectively. Furthermore, if a QC adapter is detected, then it reruns Type-C detection, which causes legacy cable detection to re-run and detect legacy cable properly.
Affected revs	RR = 00, RR = 01, and RR = 02

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Issue 5-15 Incorrect APSD detection during PON with no battery or weak battery

Description	During no battery or weak battery boot through charger insertion, there can be APSD misdetection. The root cause is that the SDM660 PHY clamps D+/D- lines until it is powered (by VREG_L10A) during the power-on sequence. APSD is run much before the PON sequence is complete. This results in incorrect APSD results and affects the input current limit or affects enumeration.
Impact	During PON with no battery or weak battery, it is possible for APSD to detect incorrect adapter types. For example, an SDP may be detected as DCP or a DCP may be detected as SDP. Another impact is enumeration failure during factory test mode (FTM) when SDP being detected as DCP.
Workaround	There is no hardware workaround available to fix the APSD misdetection. A software workaround (CR2032590) has been identified to prevent the misdetection, which will re-run APSD after the port detection. For factory test mode (FTM), customer must emulate battery presence and battery voltage greater than 3.2 V in their test jig for proper APSD detection. If battery emulation is difficult to achieve, then use external USB mux to isolate the SDM USB PHY from PM660.
Affected revs	RR = 00, RR = 01, and RR = 02

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Issue 5-16 Device does not boot when placed on WiPower PTU even after several seconds

Description	The device does not boot with good battery and when placed on a PTU. It starts booting after the device is taken off from the PTU.
Impact	The device cannot be charged or allowed booting when placed on WiPower charging pad. This is due to the incorrect PON sequence for supporting fast boot for embedded mode charging. WIPWR_RST_N does not de-assert if the sequence is not followed and this results in device always being in reset state.
Workaround	There is no workaround for this issue. Customers who need WiPower embedded mode charging please contact respective TAM.
Affected revs	RR = 00, RR = 01, and RR = 02

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6 Fuel-gauge issues

Issue 6-1 PM660 200 kHz standby oscillator drifts with die temperature change

Description	The PM660 standby oscillator is set at 200 kHz and is observed to drift with change in die temperature. With increase or decrease in die temperature there is a shift of 20 kHz at 95°C die temperature for 200 kHz oscillator.
Impact	Fuel gauge based reading will be incorrect.
Workaround	There is no hardware workaround for this issue. A software workaround (CR2032069) has been identified to compensate for the shift in fuel gauge time-base.
Affected revs	RR = 00, RR = 01, and RR = 02

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7 User-interface issues

Currently, no known issues exist for this module. When issues are discovered for this module, they will be added to this section.