Qualcomm Technologies, Inc.

SDM670/SDM710 Chipset Thermal Power Projection

80-PB873-12 Rev.B

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.

Revision History

Revision	Date	Description
A	October 2017	Initial release
B	May 2018	Global: Document has been updated to align with the SDM670 and SDM710 CS details and configuration. Read in entirety.

Thermal Power Concurrency Projection Breakout for the SDM670/SDM710 Chipset (1 of 2)

General Information

- The thermal power projection data is intended to be used ONLY for:
  - Performing system-level thermal analysis and simulation
- The data in this document is NOT intended to be used for:
  - System power consumption targets, PDN, or power budgeting purposes
  - To derive current consumption estimates (because the data is not based on actual measurements for these chipsets)
- Qualcomm Technologies, Inc. (QTI) provides two sets of data for performing thermal simulation:
  - Thermal power concurrency projection (this document)
  - Chipset packages thermal models
- The combination of thermal power projection and chipset package thermal model data that QTI provides should enable customers to perform the necessary thermal simulation on their systems.

The table on slide 6 lists the projected concurrency thermal power dissipation data, broken out at the physical die-block level for each ASIC package in the SDM670/SDM710 chipset. It is the responsibility of the customer to address any hardware configuration that deviates from the configuration presented in the table.

Note: Licensed customers can access this document and other thermal related documents such as package thermal models and other thermal design supporting documents at the Qualcomm CreatePoint website: https://createpoint.qti.qualcomm.com.

Thermal Power Concurrency Projection Breakout for the SDM670/SDM710 Chipset (2 of 2)

General Information (cont.)

The power values listed in this document are general and forward-looking.

- These values represent thermal power projections for known thermally challenging use-cases and benchmarks to exercise various aspects of the chipset hardware configuration.
- Projection numbers are subject to change and data will be updated periodically as QTI acquires more detailed information.
- Customers are encouraged to review this document regularly for updates.

The thermal power values in the table on slide 6 are unmitigated and will be lowered via software thermal mitigation routines when the thermal limits have been reached in the handset system.

Thermal power projections are provided in range values to accommodate:

- Variations in semiconductor processes and manufacturing maturity
- Any leakage associated with high power and elevated temperature environment

Non-QTI components, such as PAs, display panels, and so on, are:

- Unless otherwise stated, not included in this document.
- Specifically thermal power for display brightness and PA transmission thermal losses is not included.

Thermal Power Projection Breakdown for the SDM670/SDM710 Chipset

Thermal power use-cases and hardware description	Projection evaluated at device junction temperature T_j	Chipset hardware configuration							Total
		SDM670/ SDM710 (SoC only)	Non-PoP – 4 GB LPDDR4X	WCD9335/ WCD9340/ WCD9341	WCN3990/ WCN3980	SDR660: (3G/4G chain)	Qualcomm® RF360™: QPA	PM670	
		Units: mW							
Graphics Intensive: Manhattan (30 fps)	45ºC	1217–1474	246	–	–	–	–	373–411	1836–2131
CPU intensive: Pirates	45ºC	1340–1490	200	–	–	–	–	431–454	1971–2144
SDM670 PA intensive: LTE FDD Cat9, 3X CA, 20 MHz + 20 MHz + 20 MHz (450/50 DL/UL + B3 (Tx) + B7 + B20), 23 dBm	45ºC	835–1035	99	–	–	–	1653	406–421	2993–3223
SDM710 PA intensive: LTE FDD Cat15, 2X CA 4 × 4 MIMO, (800/150 DL/UL, B7 + B7), 21 dBm	65ºC	1297–1557	84	–	–	370	894	506–714	3151–3618
VENUS Intensive: UHD at 30 fps encode with FD, EIS 3.0, sensor 12 MP at 30 fps	45ºC	1080–1299	245	–	–	–	–	303–336	1628–1880
Camera Intensive: 12 MP at 20 fps burst shot with FD, sensor 16 MP at 30 fps	55ºC	2119–2340	303	–	–	–	–	500–533	2922–3176
SDM670 Dhrystone (Octa core CPU)	85ºC	2700–3200	50	–	–	–	–	650–780	3400–4030
SDM710 Dhrystone (Octa core CPU)	85ºC	3015–3608	50	–	–	–	–	741–889	4548–3806

Thermal Power Projection for the SDM670/SDM710 Chipset

System Configuration

This table provides background information regarding system configuration and boundary condition assumptions used to generate the thermal power data in the thermal power projection table. The configuration is for a typical smartphone form-factor, WQXGA (2560 × 1600) display resolution, LPDDR4 non-PoP, 4 GB, 12 MP sensor, and 4 MP sensor.

Use-case	Description
SDM670 CPU Intensive Dhrystone	SDM670, 2x Kryo Gold Dhrystone, 2.016 GHz
SDM710 CPU Intensive Dhrystone	SDM710, 2x Kryo Gold Dhrystone, 2.208 GHz
12 MP at 20 fps burst shot with FD	12 MP at 20 fps burst shot with FD, sensor 16 MP at 30 fps
Manhattan 3.0	1080p (single frame), 30 fps, on-screen
Pirates	–
LTE FDD Cat9	3X CA, 20 MHz + 20 MHz + 20 MHz (450/50 DL/UL, B3 (Tx) + B7 + B20), 23 dBm
LTE FDD Cat15	2X CA(4 × 4 MIMO) -800 DL/150 UP, B7 + B7, 21 dBm
UHD at 30 fps encode with FD, EIS 3.0	Sensor 12 MP at 30 fps

Notes:

1. All use-cases assume that the AC adapter is the power source (not battery power mode).
2. Unless stated otherwise, BL, LCD, and sensor power data is NOT included in the above estimates.
3. In this document, the PMIC regulator efficiency losses are grouped under the PMIC, and include dissipation in external components, such as inductors. See the next two slides for further general-purpose information related to the PMIC, charging related efficiency, and performance curves.

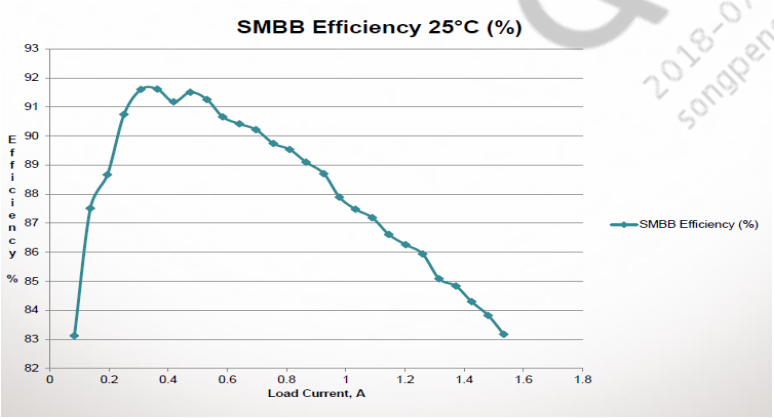
Battery Charging Thermal Power (1 of 2)

The typical battery charging path includes a USB cable/connector, PWB trace, PMIC, peripheral components (inductor, FET, and capacitor), battery, and so on. Any resistance from components on the path can convert the power to heat. To simplify the calculation, only PMIC/SMB is considered, which is the main contributor for battery charging thermal power.

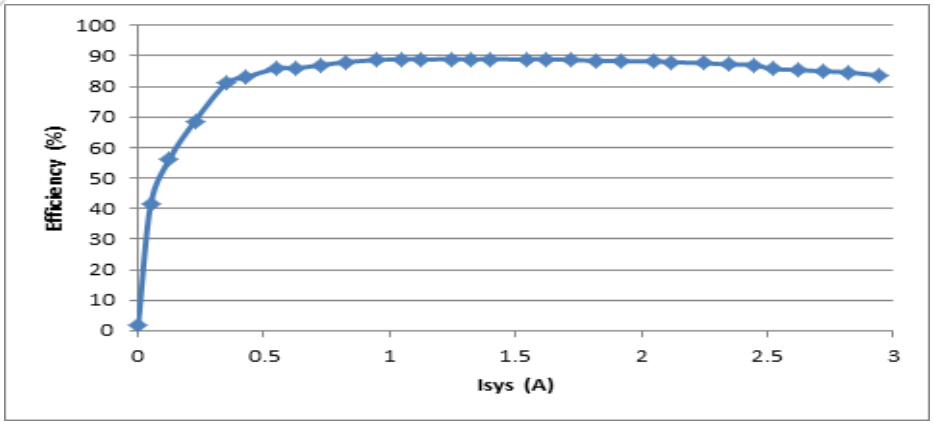
To calculate the power dissipation during battery charging, the following efficiency formula can be used:

$$P\_dissipation = \frac{P_{out} \times (1-\eta)}{\eta}$$

where P_{out} is the charging output power of a PMIC or SMB chip, and η is the conversion efficiency. The following curves show the typical PMIC and SMB chip charging efficiency vs. load.



PMIC SMBC efficiency vs. load



SMB chip charging efficiency vs. load

Battery Charging Thermal Power (2 of 2)

Taking PMIC as an example: the efficiency is approximately 87% when the charging current is 1 A; therefore, the total loss is:

$$P_{dissipation} = (3.9\ V \times 1\ A) \times (1\text{-}0.87)/0.87 = 0.58\ W$$

where 3.9 V is the average battery voltage for a 4.2 V battery during constant current charging.

However, only ~75%−78% of this power is dissipated on the die with 1 A charging current (it is ~65% with 3 A charging current), and the rest is dissipated off chip components, such as the inductors (DRC + core losses) and capacitors, so the final thermal power is:

$$P_{thermal} = 0.58 \times 0.78 = 0.45\ W$$

Note: The above analysis and calculations are based on typical PMICs and SMB chips. It is not specific for the PMIC or SMB chip that is companying the MSM™/APQ/MDM mentioned in the previous slides. See the *SDM670 Device Specification* (80-PB873-1) and *SDM710 Device Specification* (80-PG301-1) or contact the engineering support team for a more accurate efficiency curve or calculations for specific PMIC/SMB chip.

Questions?

For additional information or to submit technical questions, go to:
https://createpoint.qti.qualcomm.com