Qualcomm Technologies, Inc.

PMI8937/PMI8940

Hardware Register Description

80-P2563-2X Rev. B

September 23, 2016

For additional information or to submit technical questions go to https://createpoint.qti.qualcomm.com

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Revision history

Bars appearing in the left margin (as shown here) indicate where technical changes have occurred for this revision. The following tables list the technical content changes for all revisions.

Revision A, January 2016, initial release

Revision B, August 2016

Chapter	Description
Global	Updated PMI8937 to PMI8937/PMI8940
12	0x00001307 and 0x000013F2: Updated the register description to indicate the values applicable for PMI8940
14	0x000014F4 and 0x000014F5: Added the register
24	0x0001D84D: Updated the voltage values for WLED1_CTRL_WLED_OVP register
26	Added the IBB_IBB (applicable only for PMI8940) chapter
27	Added the LAB_LAB (applicable only for PMI8940) chapter

Contents

1 Introduction

1.1 Overview

The power management integrated circuit (PMIC) device consists of two slave IDs. Each slave ID has 64K addresses. These addresses are subdivided into 256 groups of 256 addresses. Each of these groups is known as a peripheral.

Because each PMIC device has two slave IDs, the address map can support up to 512 peripherals. The MSM™ device supports up to only 256 peripherals.

The top eight bits are known as the *peripheral address* and the bottom eight bits are known as the *register offset*.

Two identical peripherals (for example, LDOs) have different peripheral IDs, but the registers within each peripheral have the same register offset. The unique slave ID (USID) allows the MSM device to access more peripherals by increasing the available register map.

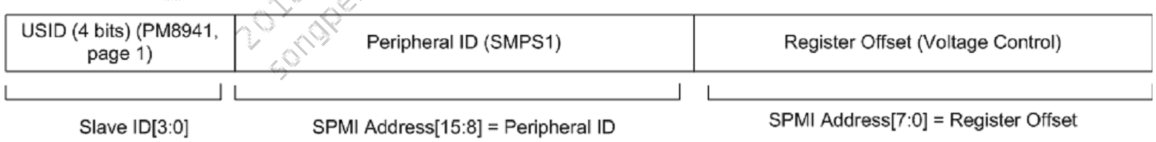


Figure 1-1 Addressing structure

1.2 Slave ID

The PMIC device has two unique slave IDs (USID):

- USID 0 and 1 are reserved for the primary PMIC (PM8937/PM8940 device)
- USID 2 and 3 are reserved for the secondary PMIC (PMI8937/PMI8940 device)

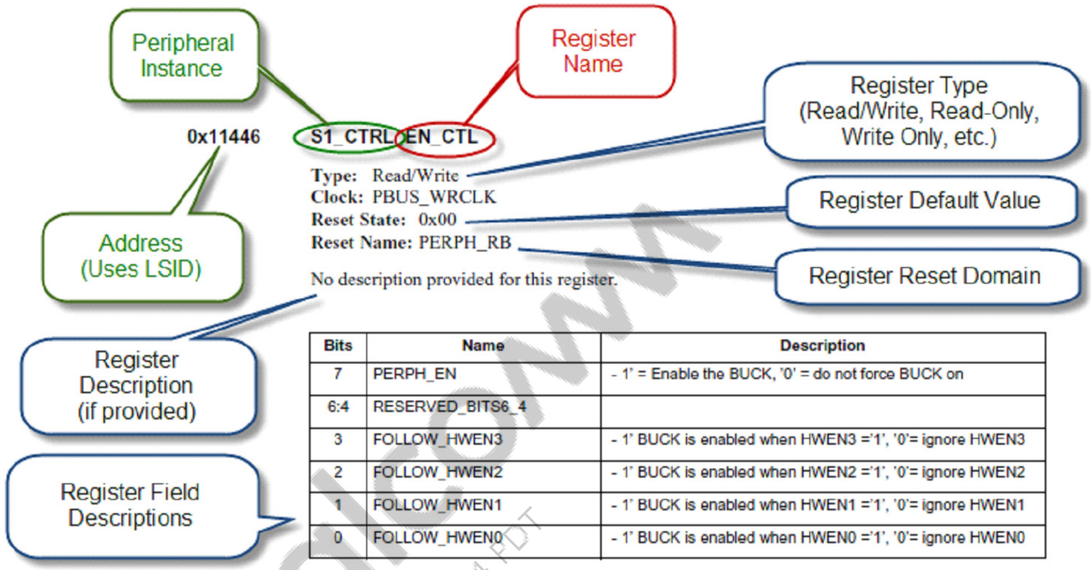
Internally, the USID is translated into a local slave ID (LSID).

- The first USID maps to LSID 0
- The second USID maps to LSID 1

The PMIC device could have up to four LSIDs, but only the first two are addressable from the SPMI bus.

1.3 Register description

Figure 1-2 illustrates each element of a register description.



Bits	Name	Description
7	PERPH_EN	- 1' = Enable the BUCK, '0' = do not force BUCK on
6:4	RESERVED_BITS6_4	
3	FOLLOW_HWEN3	- 1' BUCK is enabled when HWEN3 ='1', '0'= ignore HWEN3
2	FOLLOW_HWEN2	- 1' BUCK is enabled when HWEN2 ='1', '0'= ignore HWEN2
1	FOLLOW_HWEN1	- 1' BUCK is enabled when HWEN1 ='1', '0'= ignore HWEN1
0	FOLLOW_HWEN0	- 1' BUCK is enabled when HWEN0 ='1', '0'= ignore HWEN0

Figure 1-2 PMIC register map

The address is broken down into LSID, PID, and register offset.

For example, in the address 0x11446, from left to right:

- 1 is the unique slave ID
- 14 is the peripheral ID
- 46 is the register offset

The LSID is provided in all the register maps. In most applications, where the PMIC device is accessed from the SPMI bus, the USID is used.

1.4 Peripheral register map

Each peripheral has 256 registers that are subdivided into sections. The subsections of the peripheral register map are as follows:

- Peripheral status
- Interrupts
- Control
- Reserved

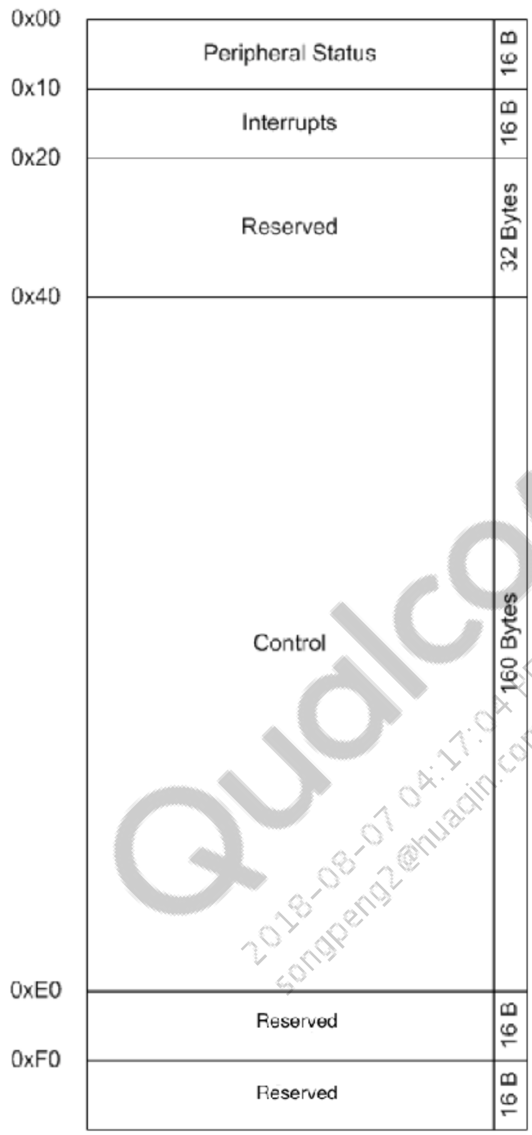


Figure 1-3 Peripheral register map

1.5 Peripheral interrupts

Each peripheral has interrupts contained within its register map. Each register is reserved for a different function. Each bit defines a different interrupt. For example, for the GPIO_IN interrupt:

- Bit 0 is reserved
- 0x10[0] holds real-time status
- 0x11[0] defines type (level/edge)
- 0x12[0] defines polarity

This setup reduces the number of transactions required to service interrupts. All of the real-time status bits for the interrupts within the module can be read with a single read of the INT_RT_STS register.

Similarly, the status of the latched interrupts is acquired with a single read of the INT_LATCHED_STS register.

Table 1-1 Example of interrupt register map

Offset	Register	MSB	LSB	Bit	Default	Description
0x10	INT_RT_STS	1	1	GPIO_HI_RT_STS	0	Interrupt real time status bits
		0	0	GPIO_IN_RT_STS	0	
0x12	INT_POLARITY_HIGH	1	1	GPIO_HI_HIGH	0	1: Interrupt triggers on a level high (rising edge) event. 0: Level HIGH triggering is disabled.
		0	0	GPIO_IN_HIGH	0	
0x13	INT_POLARITY_LOW	1	1	GPIO_HI_LOW	0	1: Interrupt triggers on a level low (falling edge) event. 0: Level low triggering is disabled.
		0	0	GPIO_IN_LOW	0	
0x14	INT_LATCHED_CLR	1	1	GPIO_HI_LATCHED_CLR	0	1: Rearms the interrupt when an interrupt is pending. Clears the internal latched status.
		0	0	GPIO_IN_LATCHED_CLR	0	
0x15	INT_EN_SET	1	1	GPIO_HI_EN_SET	0	0: Has no effect. 1: Enables the corresponding interrupt. Reading this register returns enable status.
		0	0	GPIO_IN_EN_SET	0	
0x16	INT_EN_CLR	1	1	GPIO_HI_EN_CLR	0	0: Has no effect. 1: Disables the corresponding interrupt. Reading this register returns enable status.
		0	0	GPIO_IN_EN_CLR	0	
0x18	INT_LATCHED_STS	1	1	GPIO_HI_LATCHED_STS	0	Latched Interrupt. 1: indicates the interrupt has triggered. Once the latched bit is set, it can be cleared by writing the clear bit.
		0	0	GPIO_IN_LATCHED_STS	0	
0x19	INT_PENDING_STS	1	1	GPIO_HI_PENDING_STS	0	Pending is set if interrupt has been sent but not cleared.
		0	0	GPIO_IN_PENDING_STS	0	
0x1A	INT_MID_SEL	1	0	INT_MID_SEL	0	Selects the MID that receives the interrupt.
0x1B	INT_PRIORITY	0	0	INT_PRIORITY	0	SR = 0 A = 1

1.6 Interrupt configuration

1.6.1 Set and forget registers

INT_MID_SEL: There is only one master (the MSM), so the MID is 0x00 for every peripheral.

INT_PRIORITY: SPMI supports two levels of priority. Every interrupt should use low priority; there are no high priority use cases identified.

1.6.2 Enabling interrupts

Interrupts default to disabled. To enable an interrupt, set the TYPE, PRIORITY_HIGH, and PRORITY_LOW fields. Use read-modify-write to control these registers.

Once the interrupts are configured, they can be enabled. There are two INT_EN registers: INT_EN_SET and INT_EN_CLR.

Enable the interrupt by setting the corresponding bit in INT_EN_SET. Disable the interrupt by setting the corresponding bit in INT_EN_CLR. No read-modify-write is required for these registers. Writing a 0 to these registers has no effect. Reading either register returns an enable status.

1.6.3 Interrupt detection

Interrupts are sent to the master using the SPMI master write command. The interrupt message includes the peripheral ID and the triggered interrupt. In one message, all the interrupt information is communicated to the MSM device.

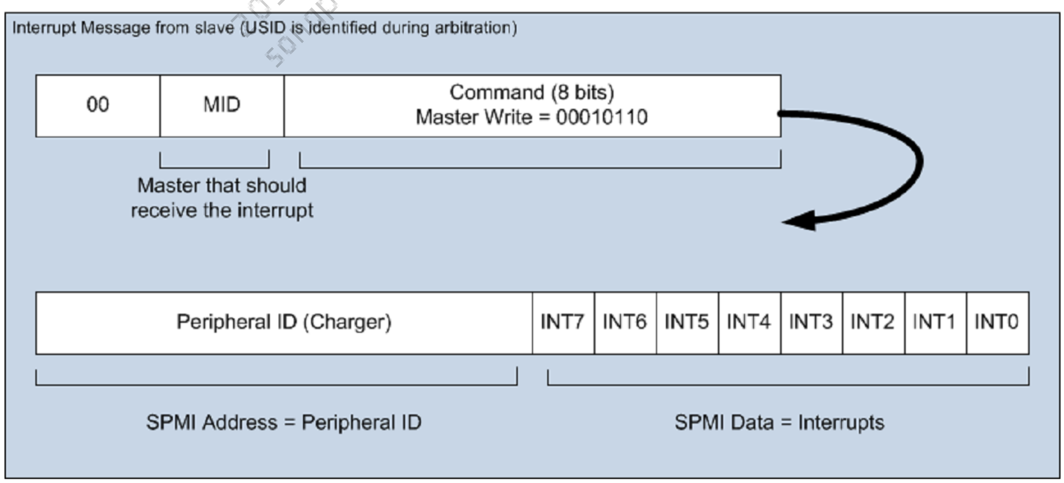


Figure 1-4 Interrupt message

1.6.4 Clearing interrupts

Assuming an interrupt is fired by GPIO_01 (peripheral ID 0x25):

1. The interrupt is generated in the PMIC device. The message is sent to the peripheral owner (RPM) via SPMI and the PMIC arbiter (in the MSM device). The message indicates that the interrupt came from GPIO_01 (PID = 0x25) and that the VREG_OK interrupt triggered.
2. (Optional) Software performs a 6-byte read starting at address 0x2510. Software is able to read status, type (level/edge), en_high, en_low, and enable state in a single read.
3. Software performs a 1-byte write of 0x01 to register 0x2516 to disable the interrupt.
4. The interrupt handler takes care of the interrupt.
5. When software is ready, a 2-byte write of 0x0101 to 0x2514 clears the interrupt and then re-enables the interrupt.

1.7 Charger and fuel gauge default register values

The charger and fuel gauge have a register structure that differs from other modules. The difference is due to the charger and fuel gauge IP integrated in the PMI8937/PMI8940 and future PMICs. The register structure stores a default value in an one-time programmable (OTP) table. The default value is copied to a charger and a fuel gauge register when a valid power supply initially connects to a power input—once all the power supplies have been removed (cold boot).

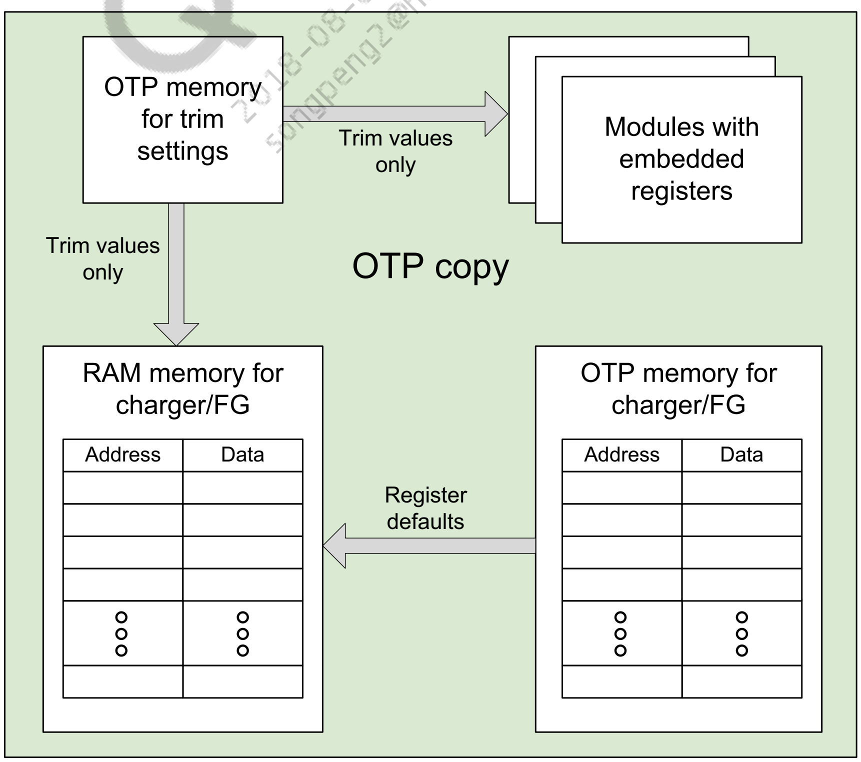


Figure 1-5 OTP copy including charger and fuel gauge OTP settings

The OTP table is programmed into the OTP ROM during manufacturing. Except for trim values copied to their respective trim registers, other PMIC modules do not use an OTP table for their default settings. Instead, register defaults are embedded in the digital design for the module.

The PMI8937/PMI8940 software interface does not indicate the true default settings for the charger and fuel gauge registers because the default values are overwritten by the OTP table. Chapter 2 lists the charger and fuel gauge OTP settings for each PMIC version.

2 Charger and fuel gauge OTP settings

2.1 Charger

Table 2-1 lists the charger OTP settings. See Table 2-2 for fuel gauge OTP settings.

Table 2-1 Charger OTP settings

Address	Data values
	ES
0x000010F0	0x00
0x000010F1	0x03
0x000010F2	0x0B
0x000010F3	0x00
0x000010F4	0x23
0x000010F5	0x05
0x000010F6	0x00
0x000010F7	0x00
0x000010F8	0x03
0x000010F9	0x05
0x000010FA	0x0F
0x000010FB	0x45
0x000010FC	0xD1
0x000010FD	0x0F
0x000010FE	0x00
0x000010FF	0x09
0x000011F0	0x00
0x000011F1	0x68
0x000011F2	0x00
0x000011F3	0x03
0x000011F4	0x00
0x000011F5	0x00
0x000011F6	0x00
0x000011F7	0x00

Table 2-1 Charger OTP settings (cont.)

Address	Data values
	ES
0x000011F8	0x00
0x000011F9	0xA1
0x000011FA	0x00
0x000011FB	0x00
0x000011FC	0x00
0x000011FD	0x00
0x000011FE	0x00
0x000011FF	0x00
0x000012F0	0x00
0x000012F1	0x04
0x000012F2	0x26
0x000012F3	0xC3
0x000012F4	0x02
0x000012F5	0x03
0x000012F6	0x03
0x000012F7	0x01
0x000012F8	0x01
0x000012F9	0x00
0x000012FA	0x84
0x000012FB	0x84
0x000013F0	0x00
0x000013F1	0x05
0x000013F2	0x10
0x000013F3	0x04
0x000013F4	0x09
0x000013F5	0xAB
0x000013F6	0x00
0x000013F7	0x00
0x000013F8	0x00
0x000013F9	0x00
0x000013FA	0x18
0x000013FB	0x80
0x000013FC	0x03
0x000013FD	0x40
0x000013FE	0x00
0x000014F0	0x00
0x000014F6	0x0C

Table 2-1 Charger OTP settings (cont.)

Address	Data values
	ES
0x000014F7	0x00
0x000014F8	0x00
0x000014F9	0x60
0x000014FA	0x00
0x000014FB	0x00
0x000014FC	0x03
0x000014FD	0x0F
0x000014FE	0x00
0x000014FF	0x00
0x000016F0	0x00
0x000016F1	0x00
0x000016F2	0xCC
0x000016F3	0x00
0x000016F4	0x35
0x000016F5	0xD8
0x000016F6	0x18
0x000016F7	0x00
0x000016F8	0x00
0x000016F9	0x00
0x000016FA	0x00
0x000016FB	0x00
0x000016FC	0x00
0x000016FD	0x00
0x000016FE	0x00
0x000016FF	0x02

2.2 Fuel gauge

Table 2-2 lists the fuel gauge OTP settings.

Table 2-2 Fuel gauge OTP settings

Address	Data
	ES
0x000040F0	0x00
0x000040F1	0x00
0x000040F2	0x00

Table 2-2 Fuel gauge OTP settings (cont.)

Address	Data
	ES
0x000040F3	0x00
0x000040F4	0x00
0x000040F5	0xEE
0x000040F6	0x00
0x000040F7	0x00
0x000040F8	0x00
0x000040F9	0x00
0x000040FA	0x00
0x000041F0	0x00
0x000041F1	0x01
0x000041F2	0x00
0x000041F3	0x78
0x000041F4	0x02
0x000041F5	0x01
0x000041F6	0x01
0x000041F7	0x03

3 REVID_REVID_PMI8937/PMI8940

0x00000100 REVID_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

REVID_REVISION1

Bits	Name	Description
7:0	RFU	Reserved for future use

0x00000101 REVID_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

REVID_REVISION2

Bits	Name	Description
7:0	VARIANT	This field indicates the chip variant

0x00000102 REVID_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

REVID_REVISION3

Bits	Name	Description
7:0	METAL	This number is incremented on a metal-only revision of the chip

0x00000103 REVID_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [31:24]

REVID_REVISION4

Bits	Name	Description
7:0	ALL_LAYER	This number is incremented every time there is an all layer revision of the chip

0x00000104 REVID_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x51

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

REVID_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	REVID (This tells you that you are talking to a PMIC)

0x00000105 REVID_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x11

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

REVID_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	This is PMI8937/PMI8940.

0x00000150 REVID_SBL_ID_0

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: xVdd_rb

REVID_SBL_ID_0

Bits	Name	Description
7:0	VERSION	Number associated with each SBL version

0x00000151 REVID_SBL_ID_1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: xVdd_rb

REVID_SBL_ID_1

Bits	Name	Description
7:0	VERSION	Number associated with each SBL version

0x00000154 REVID_PBS_OTP_ID_0

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: xVdd_rb

REVID_PBS_OTP_ID_0

Bits	Name	Description
7:0	VERSION	Number associated with each PBS_OTP version

0x000001D0 REVID_SEC_ACCESS

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKING

REVID_SEC_ACCESS

Bits	Name	Description
7:0	SEC_UNLOCK	Unlock the Secure Registers (0xTBD) by writing 0xA5 to this register. Lock is rearmed after the next write to the module.

4 BUS_INTBUS_ARB_DIG

0x00000400 BUS_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

BUS_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	

0x00000401 BUS_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

BUS_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x00000404 BUS_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x0B

Reset Name: N/A

Peripheral Type

BUS_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	0xB: INTERFACE

0x00000405 BUS_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: N/A

Peripheral SubType

BUS_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x2: INTBUS_ARB

0x00000408 BUS_STATUS1

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: N/A

Status Registers

BUS_STATUS1

Bits	Name	Description
3:0	INTBUS_ARB_GNT	Grant Values

0x00000444 BUS_TIMEOUT

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

PMIC_SYNC=clk_19_2m:dVdd_rb

BUS_TIMEOUT

Bits	Name	Description
7:4	TIMEOUT_MANT	after TIMEOUT_MANT(2^(TIMEOUT_EXP+4))*52 ns that a master holds onto the bus, a new arbitration is forced. Write zero if no timeout desired.
3:0	TIMEOUT_EXP	after TIMEOUT_MANT(2^(TIMEOUT_EXP+4))*52 ns that a master holds onto the bus, a new arbitration is forced. Write zero if no timeout desired.

5 INT_INTR_DIG

0x00000500 INT_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x03

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

INT_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00000501 INT_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

INT_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x00000504 INT_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x0A

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

INT_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	0xA: INTERRUPT

0x00000505 INT_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

INT_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x1: PNP_INTERRUPT

0x00000508 INT_STATUS1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

Status Register 1

INT_STATUS1

Bits	Name	Description
1	CLK_REQ	Or of all clk_requests 0x0: NO_CLOCK_REQ 0x1: CLOCK_REQUESTED
0	SEND_REQ	Or of all send_requests 0x0: NO_SEND_REQ 0x1: SEND_REQUESTED

0x00000509 INT_STATUS2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

Status Register 2

INT_STATUS2

Bits	Name	Description
7:0	LAST_WINNER	Last Arbitration Winner

0x00000540 INT_INT_RESEND_ALL

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Clear all Sent bits and resend all interrupts.

INT_INT_RESEND_ALL

Bits	Name	Description
0	INT_RESEND_ALL	Clear all Sent bits and resend all interrupts. 0x1: RESEND_ALL

0x00000546 INT_EN_CTL1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

INT_EN_CTL1

Bits	Name	Description
7	INTR_EN	INTR enable 0 = disables INTR from sending messages 1 = INTR is enabled and can send messages 0x0: PERIPHERAL_DISABLED 0x1: PERIPHERAL_ENABLED

6 SPMI_SPMI_P_DIG

0x00000600 SPMI_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x05

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

SPMI_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00000601 SPMI_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

SPMI_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x00000602 SPMI_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

SPMI_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00000603 SPMI_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

SPMI_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x00000604 SPMI_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x0B

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

SPMI_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	0xB: INTERFACE

0x00000605 SPMI_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

SPMI_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x1: SPMI

0x00000608 SPMI_ERROR_SYNDROME

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Status Register

SPMI_ERROR_SYNDROME

Bits	Name	Description
7:0	ERROR_SYNDROME	Error Syndrome from SPMI

0x0000060B SPMI_ERROR_DATA

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Status Register

SPMI_ERROR_DATA

Bits	Name	Description
7:0	ERROR_DATA	Data upon data parity error

0x0000060C SPMI_ERROR_ADDR_LO

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Status Register

SPMI_ERROR_ADDR_LO

Bits	Name	Description
7:0	ERROR_ADDR_LO	lower 8 bits of address upon data or addr parity error

0x0000060D SPMI_ERROR_ADDR_MD

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Status Register

SPMI_ERROR_ADDR_MD

Bits	Name	Description
7:0	ERROR_ADDR_MD	middle 8 bits of address upon data or addr parity error

0x0000060E SPMI_ERROR_ADDR_HI

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Status Register

SPMI_ERROR_ADDR_HI

Bits	Name	Description
3:0	ERROR_ADDR_HI	higher 4 bits of address upon data or addr parity error

0x00000610 SPMI_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Interrupt Real Time Status Bits

SPMI_INT_RT_STS

Bits	Name	Description
0	SPMI_INT_RT_STS	

0x00000611 SPMI_INT_SET_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

SPMI_INT_SET_TYPE

Bits	Name	Description
0	SPMI_INT_TYPE	

0x00000612 SPMI_INT_POLARITY_HIGH

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

SPMI_INT_POLARITY_HIGH

Bits	Name	Description
0	SPMI_INT_HIGH	

0x00000613 SPMI_INT_POLARITY_LOW

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

SPMI_INT_POLARITY_LOW

Bits	Name	Description
0	SPMI_INT_LOW	

0x00000614 SPMI_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

SPMI_INT_LATCHED_CLR

Bits	Name	Description
0	SPMI_INT_LATCHED_CLR	

0x00000615 SPMI_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

SPMI_INT_EN_SET

Bits	Name	Description
0	SPMI_INT_EN_SET	

0x00000616 SPMI_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

SPMI_INT_EN_CLR

Bits	Name	Description
0	SPMI_INT_EN_CLR	

0x00000618 SPMI_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

SPMI_INT_LATCHED_STS

Bits	Name	Description
0	SPMI_INT_LATCHED_STS	

0x00000619 SPMI_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

SPMI_INT_PENDING_STS

Bits	Name	Description
0	SPMI_INT_PENDING_STS	

0x0000061A SPMI_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

SPMI_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	

0x0000061B SPMI_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

SPMI_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	

0x00000640 SPMI_SPMI_BUF_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: PERPH_RB

SPMI_SPMI_BUF_CFG

Bits	Name	Description
1:0	BUFFER_STRENGTH	SPMI Buffer Drive Strength Configuration 0x0: LOW10PF 0x1: MID20PF 0x2: HIGH40PF 0x3: VERYHIGH50PF

0x00000641 SPMI_SSC_DETECT_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

SCC Detection Configuration

SPMI_SSC_DETECT_CFG

Bits	Name	Description
2:0	SSC_DETECT_CFG	Bit0=Q1_DELAY_DISABLE when bit=1 then the delay between q1 and q2 is disabled, there is a mux between the flops and the bit is connected to the mux_select. When at default=0,q2 uses q1_delayed and glitch should be masked. Bit1=WINDOW_ENABLE when bit=1 then SSC detects only when it is expected,default=0 detect SSC all time. Bit2=Reserved 0x0: WINDOW_DISABLED_Q1_DELAY_ENABLED 0x1: WINDOW_DISABLED_Q1_DELAY_DISABLED 0x2: WINDOW_ENABLED_Q1_DELAY_ENABLED 0x3: WINDOW_ENABLED_Q1_DELAY_DISABLED

7 PON_PON

0x00000800 PON_REVISION1

Type: R
Clock: pbus_wrclk
Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PON_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00000801 PON_REVISION2

Type: R
Clock: pbus_wrclk
Reset State: 0x04

Reset Name: N/A

HW Version Register [15:8]

PON_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x00000802 PON_REVISION3

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

PON_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00000803 PON_REVISION4

Type: R
Clock: pbus_wrclk
Reset State: 0x01

Reset Name: N/A

HW Version Register [31:24]

PON_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x00000804 PON_PERPH_TYPE

Type: R
Clock: pbus_wrclk
Reset State: 0x01

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

PON_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	0x1: PON

0x00000805 PON_PERPH_SUBTYPE

Type: R
Clock: pbus_wrclk
Reset State: 0x02

Reset Name: N/A

Peripheral SubType

PON_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x1: PON_PRIMARY 0x2: PON_SECONDARY 0x3: PON_1REG

0x00000807 PON_PON_PBL_STATUS

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

Stage 2 reset generation and register access error status.

PON_PON_PBL_STATUS

Bits	Name	Description
7	DVDD_RB_OCCURRED	DVDD_RB was asserted during the last power cycle 0x0: NO_RESET 0x1: RESET_OCCURRED
6	XVDD_RB_OCCURRED	XVDD_RB was asserted during the last power cycle 0x0: NO_RESET 0x1: RESET_OCCURRED
1	POFF_FAULT_OCCURRED	POFF did not follow normal sequence 0x0: NO_FAULT 0x1: FAULT_OCCURRED

0x00000808 PON_PON_REASON1

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: raw_xVdd_rb

Reasons that the PMIC left the off state. All zeros mean that no trigger received

PON_PON_REASON1

Bits	Name	Description
7	KPDPWR_N	Triggered from new KPDPWR press 0x1: TRIGGER_RECEIVED
6	CBLPWR_N	Triggered from CBL_PWR1_N 0x1: TRIGGER_RECEIVED
5	PON1	Triggered from PON1 0x1: TRIGGER_RECEIVED
4	USB_CHG	Triggered from USB charger 0x1: TRIGGER_RECEIVED
3	DC_CHG	Triggered from DC charger 0x1: TRIGGER_RECEIVED
2	RTC	Triggered from RTC 0x1: TRIGGER_RECEIVED
1	SMPL	Triggered from SMPL 0x1: TRIGGER_RECEIVED
0	HARD_RESET	Triggered from a Hard Reset event (check POFF reason for the trigger) 0x1: TRIGGER_RECEIVED

0x0000080A PON_WARM_RESET_REASON1

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: raw_xVdd_rb

Reasons that PMIC entered the Warm Reset state (pst_13).

This register is automatically reset when the PMIC turns on (i.e. PON_WARM_REASON_CLEAR register field 1) or by writing to this address. This is a synchronized address so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.

PON_WARM_RESET_REASON1

Bits	Name	Description
7	KPDPWR_N	Triggered by KPDPWR_N 0x1: TRIGGER_RECEIVED
6	RESIN_N	Triggered by RESIN_N 0x1: TRIGGER_RECEIVED
5	KPDPWR_AND_RESIN	Triggered by simultaneous KPDPWR_N + RESIN_N 0x1: TRIGGER_RECEIVED
4	GP2	Triggered by Keypad_Reset2 0x1: TRIGGER_RECEIVED
3	GP1	Triggered by Keypad_Reset1 0x1: TRIGGER_RECEIVED
2	PMIC_WD	Triggered by PMIC Watchdog 0x1: TRIGGER_RECEIVED
1	PS_HOLD	Triggered by PS_HOLD 0x1: TRIGGER_RECEIVED
0	SOFT	Triggered by Software 0x1: TRIGGER_RECEIVED

0x0000080B PON_WARM_RESET_REASON2

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: raw_xVdd_rb

Reasons that PMIC entered the Warm Reset state (pst_13). This register is automatically reset when the PMIC turns on (i.e. PON_WARM_REASON_CLEAR register field 1) or by writing to WARM_RESET_REASON1 register address.

PON_WARM_RESET_REASON2

Bits	Name	Description
4	AFP	Triggered AFP 0x1: TRIGGER_RECEIVED

0x0000080C PON_POFF_REASON1

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: raw_xVdd_rb

Reasons that the PMIC left the on state and commenced a shutdown sequence. All zeros mean that no trigger received or a master bandgap or phone power fault occurred.

PON_POFF_REASON1

Bits	Name	Description
7	KPDPWR_N	Triggered by KPDPWR_N 0x1: TRIGGER_RECEIVED
6	RESIN_N	Triggered by RESIN_N 0x1: TRIGGER_RECEIVED
5	KPDPWR_AND_RESIN	Triggered by simultaneous KPDPWR_N + RESIN_N 0x1: TRIGGER_RECEIVED
4	GP2	Triggered by Keypad_Reset2 0x1: TRIGGER_RECEIVED
3	GP1	Triggered by Keypad_Reset1 0x1: TRIGGER_RECEIVED
2	PMIC_WD	Triggered by PMIC Watchdog 0x1: TRIGGER_RECEIVED
1	PS_HOLD	Triggered by PS_HOLD 0x1: TRIGGER_RECEIVED
0	SOFT	Triggered by Software 0x1: TRIGGER_RECEIVED

0x0000080D PON_POFF_REASON2

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: raw_xVdd_rb

Reasons that the PMIC left the on state and commenced a shutdown sequence. All zeros mean that no trigger received or a master bandgap or phone power fault occurred.

PON_POFF_REASON2

Bits	Name	Description
7	STAGE3	Triggered by stage3 reset 0x1: TRIGGER_RECEIVED
6	OTST3	Triggered by Overtemp 0x1: TRIGGER_RECEIVED
5	UVLO	Triggered by UVLO 0x1: TRIGGER_RECEIVED
4	AFP	Triggered by AFP 0x1: TRIGGER_RECEIVED
3	CHARGER	Triggered by Charger (ENUM_TIMER, BOOT_DONE) 0x1: TRIGGER_RECEIVED
2	AVDD_RB	Triggered by AVDD_RB 0x1: TRIGGER_RECEIVED

0x0000080E PON_SOFT_RESET_REASON1

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: raw_xVdd_rb

Reasons that the PMIC registers were reset. All zeros mean that no trigger received.

Clear both soft reason registers by writing to this register. This is a synchronized address so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.

PON_SOFT_RESET_REASON1

Bits	Name	Description
7	KPDPWR_N	Triggered by KPDPWR_N 0x1: TRIGGER_RECEIVED
6	RESIN_N	Triggered by RESIN_N 0x1: TRIGGER_RECEIVED
5	KPDPWR_AND_RESIN	Triggered by simultaneous KPDPWR_N + RESIN_N 0x1: TRIGGER_RECEIVED
4	GP2	Triggered by Keypad_Reset2 0x1: TRIGGER_RECEIVED
3	GP1	Triggered by Keypad_Reset1 0x1: TRIGGER_RECEIVED

PON_SOFT_RESET_REASON1 (cont.)

Bits	Name	Description
2	PMIC_WD	Triggered by PMIC Watchdog 0x1: TRIGGER_RECEIVED
1	PS_HOLD	Triggered by PS_HOLD 0x1: TRIGGER_RECEIVED
0	SOFT	Triggered by Software 0x1: TRIGGER_RECEIVED

0x0000080F PON_SOFT_RESET_REASON2

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: raw_xVdd_rb

Reasons that the PMIC registers were reset. All zeros mean that no trigger received. Clear the soft reason registers by writing to the SOFT_RESET_REASON1 register

PON_SOFT_RESET_REASON2

Bits	Name	Description
4	AFP	Triggered AFP 0x1: TRIGGER_RECEIVED

0x00000810 PON_INT_RT_STS

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

Interrupt Real Time Status Bits

PON_INT_RT_STS

Bits	Name	Description
7	SOFT_RESET_OCCURED	warning that a reset event has been triggered by the PMIC Watchdog timer 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH

PON_INT_RT_STS (cont.)

Bits	Name	Description
6	PMIC_WD_BARK	warning that a reset event has been triggered by the PMIC Watchdog timer 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
5	K_R_BARK	warning that a reset event has been triggered by asserting RESIN_N and KPDPWR_N simultaneously 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
4	RESIN_BARK	warning that a reset event has been triggered by RESIN_N 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
3	KPDPWR_BARK	warning that a reset event has been triggered by KPDPWR_N 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
2	CBLPWR_ON	CBLPWR_N has been asserted for longer than his debounce timer 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
1	RESIN_ON	RESIN_N has been asserted for longer than his debounce timer 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
0	KPDPWR_ON	KPDPWR_N has been asserted for longer than his debounce timer 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH

0x00000811 PON_INT_SET_TYPE

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

0 = use level trigger interrupts, 1 = use edge trigger interrupts

PON_INT_SET_TYPE

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: LEVEL 0x1: EDGE
6	PMIC_WD_BARK	0x0: LEVEL 0x1: EDGE

PON_INT_SET_TYPE (cont.)

Bits	Name	Description
5	K_R_BARK	0x0: LEVEL 0x1: EDGE
4	RESIN_BARK	0x0: LEVEL 0x1: EDGE
3	KPDPWR_BARK	0x0: LEVEL 0x1: EDGE
2	CBLPWR_ON	0x0: LEVEL 0x1: EDGE
1	RESIN_ON	0x0: LEVEL 0x1: EDGE
0	KPDPWR_ON	0x0: LEVEL 0x1: EDGE

0x00000812 PON_INT_POLARITY_HIGH

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

PON_INT_POLARITY_HIGH

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
6	PMIC_WD_BARK	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
5	K_R_BARK	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
4	RESIN_BARK	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
3	KPDPWR_BARK	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
2	CBLPWR_ON	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
1	RESIN_ON	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

PON_INT_POLARITY_HIGH (cont.)

Bits	Name	Description
0	KPDPWR_ON	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x00000813 PON_INT_POLARITY_LOW

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

PON_INT_POLARITY_LOW

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
6	PMIC_WD_BARK	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
5	K_R_BARK	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
4	RESIN_BARK	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
3	KPDPWR_BARK	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
2	CBLPWR_ON	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
1	RESIN_ON	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
0	KPDPWR_ON	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x00000814 PON_INT_LATCHED_CLR

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PON_INT_LATCHED_CLR

Bits	Name	Description
7	SOFT_RESET_OCCURED	
6	PMIC_WD_BARK	
5	K_R_BARK	
4	RESIN_BARK	
3	KPDPWR_BARK	
2	CBLPWR_ON	
1	RESIN_ON	
0	KPDPWR_ON	

0x00000815 PON_INT_EN_SET

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

PON_INT_EN_SET

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: INT_DISABLED 0x1: INT_ENABLED
6	PMIC_WD_BARK	0x0: INT_DISABLED 0x1: INT_ENABLED
5	K_R_BARK	0x0: INT_DISABLED 0x1: INT_ENABLED
4	RESIN_BARK	0x0: INT_DISABLED 0x1: INT_ENABLED
3	KPDPWR_BARK	0x0: INT_DISABLED 0x1: INT_ENABLED
2	CBLPWR_ON	0x0: INT_DISABLED 0x1: INT_ENABLED

PON_INT_EN_SET (cont.)

Bits	Name	Description
1	RESIN_ON	0x0: INT_DISABLED 0x1: INT_ENABLED
0	KPDPWR_ON	0x0: INT_DISABLED 0x1: INT_ENABLED

0x00000816 PON_INT_EN_CLR

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

PON_INT_EN_CLR

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: INT_DISABLED 0x1: INT_ENABLED
6	PMIC_WD_BARK	0x0: INT_DISABLED 0x1: INT_ENABLED
5	K_R_BARK	0x0: INT_DISABLED 0x1: INT_ENABLED
4	RESIN_BARK	0x0: INT_DISABLED 0x1: INT_ENABLED
3	KPDPWR_BARK	0x0: INT_DISABLED 0x1: INT_ENABLED
2	CBLPWR_ON	0x0: INT_DISABLED 0x1: INT_ENABLED
1	RESIN_ON	0x0: INT_DISABLED 0x1: INT_ENABLED
0	KPDPWR_ON	0x0: INT_DISABLED 0x1: INT_ENABLED

0x00000818 PON_INT_LATCHED_STS

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

PON_INT_LATCHED_STS

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
6	PMIC_WD_BARK	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
5	K_R_BARK	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
4	RESIN_BARK	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
3	KPDPWR_BARK	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
2	CBLPWR_ON	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
1	RESIN_ON	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
0	KPDPWR_ON	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED

0x00000819 PON_INT_PENDING_STS

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

PON_INT_PENDING_STS

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

PON_INT_PENDING_STS (cont.)

Bits	Name	Description
6	PMIC_WD_BARK	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
5	K_R_BARK	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
4	RESIN_BARK	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
3	KPDPWR_BARK	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
2	CBLPWR_ON	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
1	RESIN_ON	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
0	KPDPWR_ON	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

0x0000081A PON_INT_MID_SEL

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Selects the MID that will receive the interrupt

PON_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x0000081B PON_INT_PRIORITY

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

PON_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR 0x1: A

0x00000840 PON_KPDPWR_N_RESET_S1_TIMER

Type: RW
Clock: pbus_wrclk
Reset State: 0x0F

Reset Name: dVdd_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

PON_KPDPWR_N_RESET_S1_TIMER

Bits	Name	Description
3:0	S1_TIMER	Time that the debounced trigger must be held before bark is sent to MSM This field can only be updated when block is disabled (i.e. 5 sleep clock cycles after writing 0 to S2_RESET_EN and PON_TRIGGER_EN:KPDPWR_N fields). 0x0: MS_0 0x1: MS_32 0x2: MS_56 0x3: MS_80 0x4: MS_128 0x5: MS_184 0x6: MS_272 0x7: MS_408 0x8: MS_608 0x9: MS_904 0xA: MS_1352 0xB: MS_2048 0xC: MS_3072 0xD: MS_4480 0xE: MS_6720 0xF: MS_10256

0x00000841 PON_KPDPWR_N_RESET_S2_TIMER

Type: RW
Clock: pbus_wrclk
Reset State: 0x07

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_KPDPWR_N_RESET_S2_TIMER

Bits	Name	Description
2:0	S2_TIMER	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s} This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: MS_0 0x1: MS_10 0x2: MS_50 0x3: MS_100 0x4: MS_250 0x5: MS_500 0x6: S_1 0x7: S_2

0x00000842 PON_KPDPWR_N_RESET_S2_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x04

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_KPDPWR_N_RESET_S2_CTL

Bits	Name	Description
3:0	RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: RESERVED0 0x1: WARM_RESET 0x2: IMMEDIATE_XVDD_SHUTDOWN 0x3: RESERVED3 0x4: SHUTDOWN 0x5: DVDD_SHUTDOWN 0x6: XVDD_SHUTDOWN 0x7: HARD_RESET 0x8: DVDD_HARD_RESET 0x9: XVDD_HARD_RESET 0xA: WARM_RESET_AND_DVDD_SHUTDOWN 0xB: WARM_RESET_AND_XVDD_SHUTDOWN 0xC: WARM_RESET_AND_SHUTDOWN 0xD: WARM_RESET_THEN_HARD_RESET 0xE: WARM_RESET_THEN_DVDD_HARD_RESET 0xF: WARM_RESET_THEN_XVDD_HARD_RESET

0x00000843 PON_KPDPWR_N_RESET_S2_CTL2

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_KPDPWR_N_RESET_S2_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable Stage 2 reset Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles. 0x0: DISABLED 0x1: ENABLED

0x00000844 PON_RESIN_N_RESET_S1_TIMER

Type: RW
Clock: pbus_wrclk
Reset State: 0x0F

Reset Name: dVdd_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

PON_RESIN_N_RESET_S1_TIMER

Bits	Name	Description
3:0	S1_TIMER	Time that the debounced trigger must be held before bark is sent to MSM -- This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: MS_0 0x1: MS_32 0x2: MS_56 0x3: MS_80 0x4: MS_128 0x5: MS_184 0x6: MS_272 0x7: MS_408 0x8: MS_608 0x9: MS_904 0xA: MS_1352 0xB: MS_2048 0xC: MS_3072 0xD: MS_4480 0xE: MS_6720 0xF: MS_10256

0x00000845 PON_RESIN_N_RESET_S2_TIMER

Type: RW
Clock: pbus_wrclk
Reset State: 0x07

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_RESIN_N_RESET_S2_TIMER

Bits	Name	Description
2:0	S2_TIMER	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s} This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: MS_0 0x1: MS_10 0x2: MS_50 0x3: MS_100 0x4: MS_250 0x5: MS_500 0x6: S_1 0x7: S_2

0x00000846 PON_RESIN_N_RESET_S2_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x04

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_RESIN_N_RESET_S2_CTL

Bits	Name	Description
3:0	RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: RESERVED0 0x1: WARM_RESET 0x2: IMMEDIATE_XVDD_SHUTDOWN 0x3: RESERVED3 0x4: SHUTDOWN 0x5: DVDD_SHUTDOWN 0x6: XVDD_SHUTDOWN 0x7: HARD_RESET 0x8: DVDD_HARD_RESET 0x9: XVDD_HARD_RESET 0xA: WARM_RESET_AND_DVDD_SHUTDOWN 0xB: WARM_RESET_AND_XVDD_SHUTDOWN 0xC: WARM_RESET_AND_SHUTDOWN 0xD: WARM_RESET_THEN_HARD_RESET 0xE: WARM_RESET_THEN_DVDD_HARD_RESET 0xF: WARM_RESET_THEN_XVDD_HARD_RESET

0x00000847 PON_RESIN_N_RESET_S2_CTL2

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_RESIN_N_RESET_S2_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable Stage 2 reset Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles. 0x0: DISABLED 0x1: ENABLED

0x00000848 PON_RESIN_AND_KPDPWR_RESET_S1_TIMER

Type: RW
Clock: pbus_wrclk
Reset State: 0x0F

Reset Name: dVdd_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

PON_RESIN_AND_KPDPWR_RESET_S1_TIMER

Bits	Name	Description
3:0	S1_TIMER	Time that the debounced trigger must be held before bark is sent to MSM -- This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: MS_0 0x1: MS_32 0x2: MS_56 0x3: MS_80 0x4: MS_128 0x5: MS_184 0x6: MS_272 0x7: MS_408 0x8: MS_608 0x9: MS_904 0xA: MS_1352 0xB: MS_2048 0xC: MS_3072 0xD: MS_4480 0xE: MS_6720 0xF: MS_10256

0x00000849 PON_RESIN_AND_KPDPWR_RESET_S2_TIMER

Type: RW
Clock: pbus_wrclk
Reset State: 0x07

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_RESIN_AND_KPDPWR_RESET_S2_TIMER

Bits	Name	Description
2:0	S2_TIMER	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s} This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: MS_0 0x1: MS_10 0x2: MS_50 0x3: MS_100 0x4: MS_250 0x5: MS_500 0x6: S_1 0x7: S_2

0x0000084A PON_RESIN_AND_KPDPWR_RESET_S2_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x04

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_RESIN_AND_KPDPWR_RESET_S2_CTL

Bits	Name	Description
3:0	RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: RESERVED0 0x1: WARM_RESET 0x2: RESERVED2 0x3: RESERVED3 0x4: RESERVED4 0x5: RESERVED5 0x6: RESERVED6 0x7: HARD_RESET 0x8: DVDD_HARD_RESET 0x9: XVDD_HARD_RESET 0xA: RESERVED10 0xB: RESERVED11 0xC: RESERVED12 0xD: WARM_RESET_THEN_HARD_RESET 0xE: WARM_RESET_THEN_DVDD_HARD_RESET 0xF: WARM_RESET_THEN_XVDD_HARD_RESET

0x0000084B PON_RESIN_AND_KPDPWR_RESET_S2_CTL2

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_RESIN_AND_KPDPWR_RESET_S2_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable Stage 2 reset Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles. 0x0: DISABLED 0x1: ENABLED

0x0000084C PON_GP2_RESET_S1_TIMER

Type: RW
Clock: pbus_wrclk
Reset State: 0x0F

Reset Name: dVdd_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

PON_GP2_RESET_S1_TIMER

Bits	Name	Description
3:0	S1_TIMER	Time that the debounced trigger must be held before bark is sent to MSM. This field can only be updated when block is disabled (i.e. 5 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: MS_0 0x1: MS_32 0x2: MS_56 0x3: MS_80 0x4: MS_128 0x5: MS_184 0x6: MS_272 0x7: MS_408 0x8: MS_608 0x9: MS_904 0xA: MS_1352 0xB: MS_2048 0xC: MS_3072 0xD: MS_4480 0xE: MS_6720 0xF: MS_10256

0x0000084D PON_GP2_RESET_S2_TIMER

Type: RW
Clock: pbus_wrclk
Reset State: 0x07

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_GP2_RESET_S2_TIMER

Bits	Name	Description
2:0	S2_TIMER	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s} This field can only be updated when block is disabled (i.e. 5 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: MS_0 0x1: MS_10 0x2: MS_50 0x3: MS_100 0x4: MS_250 0x5: MS_500 0x6: S_1 0x7: S_2

0x0000084E PON_GP2_RESET_S2_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x04

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_GP2_RESET_S2_CTL

Bits	Name	Description
3:0	RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: RESERVED0 0x1: WARM_RESET 0x2: IMMEDIATE_XVDD_SHUTDOWN 0x3: RESERVED3 0x4: SHUTDOWN 0x5: DVDD_SHUTDOWN 0x6: XVDD_SHUTDOWN 0x7: HARD_RESET 0x8: DVDD_HARD_RESET 0x9: XVDD_HARD_RESET 0xA: WARM_RESET_AND_DVDD_SHUTDOWN 0xB: WARM_RESET_AND_XVDD_SHUTDOWN 0xC: WARM_RESET_AND_SHUTDOWN 0xD: WARM_RESET_THEN_HARD_RESET 0xE: WARM_RESET_THEN_DVDD_HARD_RESET 0xF: WARM_RESET_THEN_XVDD_HARD_RESET

0x0000084F PON_GP2_RESET_S2_CTL2

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_GP2_RESET_S2_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable Stage 2 reset Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles. 0x0: DISABLED 0x1: ENABLED

0x00000850 PON_GP1_RESET_S1_TIMER

Type: RW
Clock: pbus_wrclk
Reset State: 0x0F

Reset Name: dVdd_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

PON_GP1_RESET_S1_TIMER

Bits	Name	Description
3:0	S1_TIMER	Time that the debounced trigger must be held before bark is sent to MSM -- This field can only be updated when block is disabled (i.e. 5 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: MS_0 0x1: MS_32 0x2: MS_56 0x3: MS_80 0x4: MS_128 0x5: MS_184 0x6: MS_272 0x7: MS_408 0x8: MS_608 0x9: MS_904 0xA: MS_1352 0xB: MS_2048 0xC: MS_3072 0xD: MS_4480 0xE: MS_6720 0xF: MS_10256

0x00000851 PON_GP1_RESET_S2_TIMER

Type: RW
Clock: pbus_wrclk
Reset State: 0x07

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_GP1_RESET_S2_TIMER

Bits	Name	Description
2:0	S2_TIMER	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s} This field can only be updated when block is disabled (i.e. 5 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: MS_0 0x1: MS_10 0x2: MS_50 0x3: MS_100 0x4: MS_250 0x5: MS_500 0x6: S_1 0x7: S_2

0x00000852 PON_GP1_RESET_S2_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x04

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_GP1_RESET_S2_CTL

Bits	Name	Description
3:0	RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: RESERVED0 0x1: WARM_RESET 0x2: IMMEDIATE_XVDD_SHUTDOWN 0x3: RESERVED3 0x4: SHUTDOWN 0x5: DVDD_SHUTDOWN 0x6: XVDD_SHUTDOWN 0x7: HARD_RESET 0x8: DVDD_HARD_RESET 0x9: XVDD_HARD_RESET 0xA: WARM_RESET_AND_DVDD_SHUTDOWN 0xB: WARM_RESET_AND_XVDD_SHUTDOWN 0xC: WARM_RESET_AND_SHUTDOWN 0xD: WARM_RESET_THEN_HARD_RESET 0xE: WARM_RESET_THEN_DVDD_HARD_RESET 0xF: WARM_RESET_THEN_XVDD_HARD_RESET

0x00000853 PON_GP1_RESET_S2_CTL2

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_GP1_RESET_S2_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable Stage 2 reset Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles. 0x0: DISABLED 0x1: ENABLED

0x00000854 PON_PMIC_WD_RESET_S1_TIMER

Type: RW
Clock: pbus_wrclk
Reset State: 0x1F

Reset Name: dVdd_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

PON_PMIC_WD_RESET_S1_TIMER

Bits	Name	Description
6:0	S1_TIMER	Time that the debounced trigger must be held before bark is sent to MSM (seconds) -- 0 - 127 seconds, default 31 seconds. Program hex value of decimal count desired (not binary coded). This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles. 0x0: SEC_0 0x1: SEC_1 0x2: SEC_2 0x3: SEC_3 0x4: SEC_4 0x5: SEC_5 0x6: SEC_6 0x7: SEC_7 0x8: SEC_8 0x9: SEC_9 0xA: SEC_10 0xB: SEC_11 0xC: SEC_12 0xD: SEC_13 0xE: SEC_14 0xF: SEC_15 0x10: SEC_16 0x11: SEC_17 0x12: SEC_18 0x13: SEC_19 0x14: SEC_20 0x15: SEC_21 0x16: SEC_22 0x17: SEC_23 0x18: SEC_24 0x19: SEC_25 0x1A: SEC_26 0x1B: SEC_27 0x1C: SEC_28 0x1D: SEC_29 0x1E: SEC_30 0x1F: SEC_31 0x20: SEC_32 0x21: SEC_33 0x22: SEC_34 0x23: SEC_35 0x24: SEC_36 0x25: SEC_37 0x26: SEC_38

PON_PMIC_WD_RESET_S1_TIMER (cont.)

Bits	Name	Description
		0x27: SEC_39 0x28: SEC_40 0x29: SEC_41 0x2A: SEC_42 0x2B: SEC_43 0x2C: SEC_44 0x2D: SEC_45 0x2E: SEC_46 0x2F: SEC_47 0x30: SEC_48 0x31: SEC_49 0x32: SEC_50 0x33: SEC_51 0x34: SEC_52 0x35: SEC_53 0x36: SEC_54 0x37: SEC_55 0x38: SEC_56 0x39: SEC_57 0x3A: SEC_58 0x3B: SEC_59 0x3C: SEC_60 0x3D: SEC_61 0x3E: SEC_62 0x3F: SEC_63 0x40: SEC_64 0x41: SEC_65 0x42: SEC_66 0x43: SEC_67 0x44: SEC_68 0x45: SEC_69 0x46: SEC_70 0x47: SEC_71 0x48: SEC_72 0x49: SEC_73 0x4A: SEC_74 0x4B: SEC_75 0x4C: SEC_76 0x4D: SEC_77 0x4E: SEC_78 0x4F: SEC_79 0x50: SEC_80 0x51: SEC_81 0x52: SEC_82 0x53: SEC_83 0x54: SEC_84 0x55: SEC_85 0x56: SEC_86

PON_PMIC_WD_RESET_S1_TIMER (cont.)

Bits	Name	Description
		0x57: SEC_87 0x58: SEC_88 0x59: SEC_89 0x5A: SEC_90 0x5B: SEC_91 0x5C: SEC_92 0x5D: SEC_93 0x5E: SEC_94 0x5F: SEC_95 0x60: SEC_96 0x61: SEC_97 0x62: SEC_98 0x63: SEC_99 0x64: SEC_100 0x65: SEC_101 0x66: SEC_102 0x67: SEC_103 0x68: SEC_104 0x69: SEC_105 0x6A: SEC_106 0x6B: SEC_107 0x6C: SEC_108 0x6D: SEC_109 0x6E: SEC_110 0x6F: SEC_111 0x70: SEC_112 0x71: SEC_113 0x72: SEC_114 0x73: SEC_115 0x74: SEC_116 0x75: SEC_117 0x76: SEC_118 0x77: SEC_119 0x78: SEC_120 0x79: SEC_121 0x7A: SEC_122 0x7B: SEC_123 0x7C: SEC_124 0x7D: SEC_125 0x7E: SEC_126 0x7F: SEC_127

0x00000855 PON_PMIC_WD_RESET_S2_TIMER

Type: RW
Clock: pbus_wrclk
Reset State: 0x01

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_PMIC_WD_RESET_S2_TIMER

Bits	Name	Description
6:0	S2_TIMER	Time that debounced trigger must be held before S2 reset occurs - - 0 - 127 seconds (default = 32 seconds). Program hex value of decimal count desired (Not binary coded). Timer starts after WD bark expires This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles. 0x0: SEC_0 0x1: SEC_1 0x2: SEC_2 0x3: SEC_3 0x4: SEC_4 0x5: SEC_5 0x6: SEC_6 0x7: SEC_7 0x8: SEC_8 0x9: SEC_9 0xA: SEC_10 0xB: SEC_11 0xC: SEC_12 0xD: SEC_13 0xE: SEC_14 0xF: SEC_15 0x10: SEC_16 0x11: SEC_17 0x12: SEC_18 0x13: SEC_19 0x14: SEC_20 0x15: SEC_21 0x16: SEC_22 0x17: SEC_23 0x18: SEC_24 0x19: SEC_25 0x1A: SEC_26 0x1B: SEC_27 0x1C: SEC_28 0x1D: SEC_29 0x1E: SEC_30 0x1F: SEC_31 0x20: SEC_32 0x21: SEC_33 0x22: SEC_34 0x23: SEC_35 0x24: SEC_36 0x25: SEC_37 0x26: SEC_38

PON_PMIC_WD_RESET_S2_TIMER (cont.)

Bits	Name	Description
		0x27: SEC_39 0x28: SEC_40 0x29: SEC_41 0x2A: SEC_42 0x2B: SEC_43 0x2C: SEC_44 0x2D: SEC_45 0x2E: SEC_46 0x2F: SEC_47 0x30: SEC_48 0x31: SEC_49 0x32: SEC_50 0x33: SEC_51 0x34: SEC_52 0x35: SEC_53 0x36: SEC_54 0x37: SEC_55 0x38: SEC_56 0x39: SEC_57 0x3A: SEC_58 0x3B: SEC_59 0x3C: SEC_60 0x3D: SEC_61 0x3E: SEC_62 0x3F: SEC_63 0x40: SEC_64 0x41: SEC_65 0x42: SEC_66 0x43: SEC_67 0x44: SEC_68 0x45: SEC_69 0x46: SEC_70 0x47: SEC_71 0x48: SEC_72 0x49: SEC_73 0x4A: SEC_74 0x4B: SEC_75 0x4C: SEC_76 0x4D: SEC_77 0x4E: SEC_78 0x4F: SEC_79 0x50: SEC_80 0x51: SEC_81 0x52: SEC_82 0x53: SEC_83 0x54: SEC_84 0x55: SEC_85 0x56: SEC_86

PON_PMIC_WD_RESET_S2_TIMER (cont.)

Bits	Name	Description
		0x57: SEC_87 0x58: SEC_88 0x59: SEC_89 0x5A: SEC_90 0x5B: SEC_91 0x5C: SEC_92 0x5D: SEC_93 0x5E: SEC_94 0x5F: SEC_95 0x60: SEC_96 0x61: SEC_97 0x62: SEC_98 0x63: SEC_99 0x64: SEC_100 0x65: SEC_101 0x66: SEC_102 0x67: SEC_103 0x68: SEC_104 0x69: SEC_105 0x6A: SEC_106 0x6B: SEC_107 0x6C: SEC_108 0x6D: SEC_109 0x6E: SEC_110 0x6F: SEC_111 0x70: SEC_112 0x71: SEC_113 0x72: SEC_114 0x73: SEC_115 0x74: SEC_116 0x75: SEC_117 0x76: SEC_118 0x77: SEC_119 0x78: SEC_120 0x79: SEC_121 0x7A: SEC_122 0x7B: SEC_123 0x7C: SEC_124 0x7D: SEC_125 0x7E: SEC_126 0x7F: SEC_127

0x00000856 PON_PMIC_WD_RESET_S2_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x06

Reset Name: dVdd_rb

Stage 2 (bite) configuration. This register can only be written when PMIC_WD_LOCK field is 0x0.

PON_PMIC_WD_RESET_S2_CTL

Bits	Name	Description
3:0	RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: RESERVED0 0x1: WARM_RESET 0x2: IMMEDIATE_XVDD_SHUTDOWN 0x3: RESERVED3 0x4: SHUTDOWN 0x5: DVDD_SHUTDOWN 0x6: XVDD_SHUTDOWN 0x7: HARD_RESET 0x8: DVDD_HARD_RESET 0x9: XVDD_HARD_RESET 0xA: WARM_RESET_AND_DVDD_SHUTDOWN 0xB: WARM_RESET_AND_XVDD_SHUTDOWN 0xC: WARM_RESET_AND_SHUTDOWN 0xD: WARM_RESET_THEN_HARD_RESET 0xE: WARM_RESET_THEN_DVDD_HARD_RESET 0xF: WARM_RESET_THEN_XVDD_HARD_RESET

0x00000857 PON_PMIC_WD_RESET_S2_CTL2

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

Stage 2 (bite) configuration. This register can only be written when PMIC_WD_LOCK field is 0x0.

PON_PMIC_WD_RESET_S2_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable Stage 2 reset Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles. 0x0: DISABLED 0x1: ENABLED

0x00000858 PON_PMIC_WD_RESET_PET

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

Stage 2 (bite) configuration

PON_PMIC_WD_RESET_PET

Bits	Name	Description
0	WATCHDOG_PET	Writing '1' to this bit will clear the PMIC WD timer. Writing '0' has no effect. This is a synchronized field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles. 0x1: PET_WD

0x0000085A PON_PS_HOLD_RESET_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x04

Reset Name: dVdd_rb

PON_PS_HOLD_RESET_CTL

Bits	Name	Description
3:0	RESET_TYPE	This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 8 sleep clock cycles. 0x0: RESERVED0 0x1: WARM_RESET 0x2: IMMEDIATE_XVDD_SHUTDOWN 0x3: RESERVED3 0x4: SHUTDOWN 0x5: DVDD_SHUTDOWN 0x6: XVDD_SHUTDOWN 0x7: HARD_RESET 0x8: DVDD_HARD_RESET 0x9: XVDD_HARD_RESET 0xA: WARM_RESET_AND_DVDD_SHUTDOWN 0xB: WARM_RESET_AND_XVDD_SHUTDOWN 0xC: WARM_RESET_AND_SHUTDOWN 0xD: WARM_RESET_THEN_HARD_RESET 0xE: WARM_RESET_THEN_DVDD_HARD_RESET 0xF: WARM_RESET_THEN_XVDD_HARD_RESET

0x0000085B PON_PS_HOLD_RESET_CTL2

Type: RW
Clock: pbus_wrclk
Reset State: 0x80

Reset Name: dVdd_rb

PON_PS_HOLD_RESET_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable reset Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles. 0x0: DISABLED 0x1: ENABLED

0x00000862 PON_SW_RESET_S2_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

Software initiated shutdown (AFP)

PON_SW_RESET_S2_CTL

Bits	Name	Description
3:0	RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to SW_RESET_EN field). 0x0: SOFT_RESET 0x1: WARM_RESET 0x2: IMMEDIATE_XVDD_SHUTDOWN 0x3: RESERVED3 0x4: SHUTDOWN 0x5: DVDD_SHUTDOWN 0x6: XVDD_SHUTDOWN 0x7: HARD_RESET 0x8: DVDD_HARD_RESET 0x9: XVDD_HARD_RESET 0xA: WARM_RESET_AND_DVDD_SHUTDOWN 0xB: WARM_RESET_AND_XVDD_SHUTDOWN 0xC: WARM_RESET_AND_SHUTDOWN 0xD: WARM_RESET_THEN_HARD_RESET 0xE: WARM_RESET_THEN_DVDD_HARD_RESET 0xF: WARM_RESET_THEN_XVDD_HARD_RESET

0x00000863 PON_SW_RESET_S2_CTL2

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

Software initiated shutdown (AFP)

PON_SW_RESET_S2_CTL2

Bits	Name	Description
7	SW_RESET_EN	Enable SW reset Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles. 0x0: DISABLED 0x1: ENABLED

0x00000864 PON_SW_RESET_GO

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

Initiate SW Reset by writing 0xA5 to this register

PON_SW_RESET_GO

Bits	Name	Description
7:0	SW_RESET_GO	Initiate SW Reset by writing 0xA5 to this register This is a synchronized field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.

0x00000866 PON_OVERTEMP_RESET_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x04

Reset Name: dVdd_rb

Over temperature stage 3 plus charger FLCB stage 2 reset/shutdown control.

Note: For safety reasons, only shutdown and hard reset events are supported by the overtemp reset trigger.

PON_OVERTEMP_RESET_CTL

Bits	Name	Description
3:0	RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: RESERVED0 0x1: RESERVED1 0x2: IMMEDIATE_XVDD_SHUTDOWN 0x3: RESERVED3 0x4: SHUTDOWN 0x5: DVDD_SHUTDOWN 0x6: XVDD_SHUTDOWN 0x7: HARD_RESET 0x8: DVDD_HARD_RESET 0x9: XVDD_HARD_RESET 0xA: RESERVED10 0xB: RESERVED11 0xC: RESERVED12 0xD: RESERVED13 0xE: RESERVED14 0xF: RESERVED15

0x00000867 PON_OVERTEMP_RESET_CTL2

Type: RW
Clock: pbus_wrclk
Reset State: 0x80

Reset Name: dVdd_rb

Over temperature stage 3 plus charger FLCB stage 2 reset/shutdown control.

PON_OVERTEMP_RESET_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable stage 2 reset Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles. 0x0: DISABLED 0x1: ENABLED

0x0000086A PON_AFP_RESET_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x04

Reset Name: dVdd_rb

PON_AFP_RESET_CTL

Bits	Name	Description
3:0	RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field). 0x0: RESERVED0 0x1: RESERVED 0x2: IMMEDIATE_XVDD_SHUTDOWN 0x3: RESERVED3 0x4: SHUTDOWN 0x5: DVDD_SHUTDOWN 0x6: XVDD_SHUTDOWN 0x7: HARD_RESET 0x8: DVDD_HARD_RESET 0x9: XVDD_HARD_RESET 0xA: RESERVED10 0xB: RESERVED11 0xC: RESERVED12 0xD: RESERVED13 0xE: RESERVED14 0xF: RESERVED15

0x0000086B PON_AFP_RESET_CTL2

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

PON_AFP_RESET_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable stage 2reset Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles. 0x0: DISABLED 0x1: ENABLED

0x00000870 PON_PULL_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x07

Reset Name: soft_dVdd_rb

PON_PULL_CTL

Bits	Name	Description
3	PON1_PD_EN	0x0: PD_DISABLED 0x1: PD_ENABLED
2	CBLPWR_N_PU_EN	0x0: PD_DISABLED 0x1: PD_ENABLED
1	KPDPWR_N_PU_EN	0x0: PD_DISABLED 0x1: PD_ENABLED
0	RESIN_N_PU_EN	0x0: PD_DISABLED 0x1: PD_ENABLED

0x00000871 PON_DEBOUNCE_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

PON_DEBOUNCE_CTL

Bits	Name	Description
5:3	WIPWR_DEBOUNCE	PON_1: Time delay for general purpose input de-bouncing during wireless charger power on sequences (i.e. PON_1 input signal and WIPWR_DEBOUNCE_DLY field asserted). Only signal assertion is de-bounced. if X = 0 then delay = 0, else delay = (1/1024) seconds * 2 ^(X-1) where X = value of bits <2:0> This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles. 0x0: IMMEDIATE 0x1: MSEC_0P98 0x2: MSEC_1P95 0x3: MSEC_3P91 0x4: MSEC_7P81 0x5: MSEC_15P63 0x6: MSEC_31P25 0x7: MSEC_62P5
2:0	DEBOUNCE	KPD/CBL/RESIN/RESIN_AND_KPD/GP1/GP2: Time delay for keypad input, cable, reset input, reset input && keypad input, general purpose internal 1/2 input de-bouncing. Only signal assertion is de-bounced. PON_1: Time delay for general purpose input during non wireless charger power on sequences (i.e. WIPWR_DEBOUNCE_DLY field de-asserted). Only signal assertion is de-bounced. Delay = (1/1024)* 2^ (x+4) This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles. 0x0: MS_15P6 0x1: MS_31P2 0x2: MS_62P5 0x3: MS_125 0x4: MS_250 0x5: MS_500 0x6: MS_1000 0x7: MS_2000

0x00000875 PON_RESET_S3_TIMER

Type: RW
Clock: pbus_wrclk
Reset State: 0x04

Reset Name: xVdd_rb

Time trigger must be held before S3 reset occurs (seconds)

PMIC_LOCKED=SEC_ACCESS

PON_RESET_S3_TIMER

Bits	Name	Description
2:0	S3_TIMER	Time trigger must be held before S3 reset occurs. 000 = Instant, else 2^(x) seconds (2 to 128) for 50kHz LFRC For 32kHz LFRC 0 = instant 1 = 3.1s 2 = 6.1s 3 = 12.2s 4 = 24.2s 5 = 48.8s 6 = 97.7s 7 = 195.3s This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles. 0x0: IMMEDIATE 0x1: SEC_2 0x2: SEC_4 0x3: SEC_8 0x4: SEC_16 0x5: SEC_32 0x6: SEC_64 0x7: SEC_128

0x00000880 PON_PON_TRIGGER_EN

Type: RW
Clock: pbus_wrclk
Reset State: 0x20

Reset Name: soft_dVdd_rb

Power on trigger enables.

Each field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles.

PON_PON_TRIGGER_EN

Bits	Name	Description
7	KPDPWR_N	Enable PON trigger for new KPDPWR press 0x0: DISABLED 0x1: ENABLED
6	CBLPWR_N	Enable PON trigger for CBL_PWR_N 0x0: DISABLED 0x1: ENABLED
5	PON1	Enable PON trigger for PON1 0x0: DISABLED 0x1: ENABLED
4	USB_CHG	Enable PON trigger for USB CHG 0x0: DISABLED 0x1: ENABLED
3	DC_CHG	Enable PON trigger for DC CHG 0x0: DISABLED 0x1: ENABLED
2	RTC	Enable PON trigger for RTC 0x0: DISABLED 0x1: ENABLED
1	SMPL	Enable PON trigger for SMPL 0x0: DISABLED 0x1: ENABLED

0x00000883 PON_WATCHDOG_LOCK

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: shutdown2_rb

Write Once register that is reset at the end of the shutdown sequence

PMIC_WRITE_ONCE

PON_WATCHDOG_LOCK

Bits	Name	Description
7	PMIC_WD_LOCK	This is a write once register. '1' then PMIC_WD_RESET_S2_CTL is locked and the contents can no longer be modified. If '0' the register is programmable. 0x0: WD_UNLOCKED 0x1: WD_LOCKED

0x00000888 PON_UVLO

Type: RW
Clock: pbus_wrclk
Reset State: 0x1D

Reset Name: soft_dVdd_rb

UVLO Delay

PON_UVLO

Bits	Name	Description
5:3	WIPWR_UVLO_DLY	Time delay for UVLO detection de-bouncing during wireless charger power on sequences (i.e. PON_1 input signal and WIPWR_DEBOUNCE_DLY field asserted).Only signal assertion is de-bounced. if X = 0 then delay = 0, else delay = (1/1024) seconds * 2 ^(X-1) where X = value of bits <2:0> This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles. 0x0: IMMEDIATE 0x1: MSEC_0P98 0x2: MSEC_1P95 0x3: MSEC_3P91 0x4: MSEC_7P81 0x5: MSEC_15P63 0x6: MSEC_31P25 0x7: MSEC_62P5

PON_UVLO (cont.)

Bits	Name	Description
2:0	UVLO_DLY	Time delay for UVLO detection de-bouncing during non wireless charger power on sequences (i.e. WIPWR_DEBOUNCE_DLY field de-asserted or PON_1 input signal de-asserted and WIPWR_DEBOUNCE_DLY field asserted). Only signal assertion is de-bounced if X = 0 then delay = 0, else delay = (1/1024) seconds * 2 ^(X-1) where X = value of bits <2:0> This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles. 0x0: IMMEDIATE 0x1: MSEC_0P98 0x2: MSEC_1P95 0x3: MSEC_3P91 0x4: MSEC_7P81 0x5: MSEC_15P63 0x6: MSEC_31P25 0x7: MSEC_62P5

0x0000088A PON_AVDD_VPH

Type: RW
Clock: pbus_wrclk
Reset State: 0x70

Reset Name: perph_rb

Control for AVDD

PON_AVDD_VPH

Bits	Name	Description
6:5	AVDD_MODE_CTRL	0 = LPM/sleep mode 1 = follow automatic digital logic 2 = HPM/active mode 3 = HPM/active mode 0x0: LPM 0x1: AUTOM 0x2: HPM1 0x3: HPM2

PON_AVDD_VPH (cont.)

Bits	Name	Description
4	AVDD_REF_OVR	aVdd regulator Reference Adjust Override 0 - aVdd regulator switches it's voltage reference to the PMIC MBG when MBG_OK = 1. If MBG_OK = 0, aVdd regulator uses the internal PON mini-bg as a voltage reference 1 - aVdd regulator always uses the internal PON mini-bg as a voltage reference 0x0: AUTO 0x1: FORCE_MINI_BG

0x0000088B PON_DVDD_VPH

Type: RW
Clock: pbus_wrclk
Reset State: 0x20

Reset Name: perph_rb

Control for DVDD

PON_DVDD_VPH

Bits	Name	Description
6:5	DVDD_MODE_CTRL	0 = LPM/sleep mode 1 = follow automatic digital logic 2 = HPM/active mode 3 = HPM/active mode 0x0: LPM 0x1: AUTOM 0x2: HPM1 0x3: HPM2
3:2	XVDD_DVDD_SRC_CTRL	xVdd_dVdd_SRC_CTRL - 00: Use 1.8V LDO only - 01: Use 1.8V SMPS first priority, then 1.8V LDO - 1x: Do not use SMPS or LDO. 0x0: DVDD_SRC_FROM_LDO 0x1: DVDD_SRC_FROM_SMPS 0x2: DVDD_SRC_FROM_PON_DVDDREG 0x3: DVDD_SRC_FROM_PON_DVDDREG1

0x00000890 PON_PON1_INTERFACE

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: shutdown2_rb

PON module interface signaling.

PON_PON1_INTERFACE

Bits	Name	Description
7	PON_OUT	Field drives primary PMIC PON output buffer input. 0x0: LOW 0x1: HIGH

0x00000891 PON_PBS_INTERFACE

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: shutdown2_rb

PON module interface signaling.

PON_PBS_INTERFACE

Bits	Name	Description
6	ACK_NACK	write 0x01 to ACK the PON module, write 0x00 to NACK the PON module. A NACK will cause the PMIC to shutdown. This is a synchronized field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles. 0x0: NACK 0x1: ACK

8 MISC_MISC_PMI8937/PMI8940

0x00000900 MISC_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

MISC_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00000901 MISC_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

MISC_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x00000902 MISC_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

MISC_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00000903 MISC_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

MISC_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x00000904 MISC_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x14

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

MISC_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	0x14: MISC

0x00000905 MISC_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x14

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

MISC_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x1: MISC8941 0x2: MISC8841 0x3: VREF_LPDDR3 0x4: VREG_AFP 0x5: MISC8019 0x6: VREF_LPDDR2 0x7: MISC8026 0x8: MISC8110 0x9: MISC_LEGOLAS 0xA: VREF_LPDDR3_2CH 0xB: MISC_EOWYN 0xE: MISC_PMI8994

0x00000909 MISC_STATUS2

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: N/A

Status Registers

MISC_STATUS2

Bits	Name	Description
3:0	DTEST	0 = DTEST is 0 1 = DTEST is 1 0x0: DTEST_IS_0 0x1: DTEST_IS_1

0x00000942 MISC_XVDD_DVDD_SRC_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MISC_XVDD_DVDD_SRC_CTL

Bits	Name	Description
1:0	XVDD_DVDD_SRC_CTRL	xVdd_dVdd_SRC_CTRL 0x: Use 1.8V LDO only 1x: Do not use LDO. 0x0: USE_LDO 0x2: DO_NOT_USE_LDO

0x00000945 MISC_BUCK_CMN_CTL1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x08

Reset Name: PERPH_RB

MISC_BUCK_CMN_CTL1

Bits	Name	Description
7:6	VPRE_CHARGE_SEL	VPRE_CHARGE_SEL<1:0> for BUCK_CMN: 00 -> Vpre_charge_low_range=350mV (Default), 01 -> 400mV, 10 -> 450mV, 11 -> 500mV. 0x0: VPRE_CHARGE_LOW_RANGE_0P35V 0x1: VPRE_CHARGE_LOW_RANGE_0P40V 0x2: VPRE_CHARGE_LOW_RANGE_0P45V 0x3: VPRE_CHARGE_LOW_RANGE_0P50V
3	BYPASS_IBG_DLY	Bypass MBG current switching delay when transitioning from sleep to PWM. 0x0: BYPASS_IBG_DLY_DISABLED 0x1: BYPASS_IBG_DLY_ENABLED

0x00000947 MISC_LED_IZTC_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MISC_LED_IZTC_CTL

Bits	Name	Description
7	EN_ATEST_LED_IZTC	EN_ATEST_LED_IZTC 0x0: ATEST_IZTC_DISABLED 0x1: ATEST_IZTC_ENABLED

0x00000949 MISC_MISC_CTL1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MISC_MISC_CTL1

Bits	Name	Description
7	VDD_IO_PRECISE_DET_DIS	A control to set the state of the VDD_IO_Precise_Detector. VDD_IO_PRECISE_DET_DIS =0; VDD_IO_Precise_Detector enabled. (default) VDD_IO_PRECISE_DET_DIS =1; VDD_IO_Precise_Detector disabled. 0x0: VDD_IO_PRECISE_SET_ENABLED 0x1: VDD_IO_PRECISE_SET_DISABLED
6:0	MISC_CTL	Bits<6:0> Reserved.

0x0000094A MISC_TX_GTR_THRES_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MISC_TX_GTR_THRES_CTL

Bits	Name	Description
7	TX_GTR_THRES_REG	A signal sent by modem to indicate that a high power GSM transmit is about to happen (~100us before PA on ramp starts). It is de-asserted when the Tx transmit is over. 0x1: GSM_TRANSMIT 0x0: TRANSMIT_OVER
0	TX_GTR_THRES_SEL	A control to select the source of TX_GTR_THRES. TX_GTR_THRES_SEL = 0, use register value TX_GTR_THRES_REG (default value); TX_GTR_THRES_SEL = 1, use external value TX_GTR_THRES_DVDD (MPP/GPIO path).

0x000009D0 MISC_SEC_ACCESS

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKING

MISC_SEC_ACCESS

Bits	Name	Description
7:0	SEC_UNLOCK	Unlock the Secure Registers by writing 0xA5 to this register. Lock is rearmed after the next write to the module.

9 SMBCHGL_CHGR_SMBCHGL_CHGR

0x00001004 SMBCHGL_CHGR_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: NA

PMIC_CONSTANT

SMBCHGL_CHGR_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	

0x00001005 SMBCHGL_CHGR_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x51

Reset Name: NA

PMIC_CONSTANT

SMBCHGL_CHGR_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	

0x00001008 SMBCHGL_CHGR_CHG_OPTION

Type: R
Clock: PBUS_WRCLK
Reset State: 0x80

Reset Name: NA

SMBCHGL_CHGR_CHG_OPTION

Bits	Name	Description
7	PIN	

0x0000100B SMBCHGL_CHGR_VBAT_STATUS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_CHGR_VBAT_STATUS

Bits	Name	Description
1	ABOVE_VBAT_WEAK	0 = VBAT is below the VBAT_WEAK threshold, 1 = VBAT is above the VBAT_WEAK threshold

0x0000100C SMBCHGL_CHGR_FV_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_CHGR_FV_STS

Bits	Name	Description
7	FV_STS_EXTRA	DIV2_EN Deglitched Level 0 = Low 1 = High
6	AICL_STS	Hard Limit 0 = Not In Hard Limit 1 = In Hard Limit

SMBCHGL_CHGR_FV_STS (cont.)

Bits	Name	Description
5:0	FV_STS	Float Voltage Status 000000 = 3.60V .. 000101 = 3.60V 000110 = 3.62V 000111 = 3.64V 001000 = 3.66V .. 101110 = 4.40V 101111 = 4.42V 110000 = 4.44V 110001 = 4.46V 110010 = 4.48V 110011 = 4.50V .. 111111 = 4.50V

0x0000100D SMBCHGL_CHGR_ICHG_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_CHGR_ICHG_STS

Bits	Name	Description
7:5	PCC_STS	Pre-Charge Current Status 000 = 100mA 001 = 150mA 010 = 200mA 011 = 250mA 1XX = 550mA

SMBCHGL_CHGR_ICHG_STS (cont.)

Bits	Name	Description
4:0	FCC_STS	Fast-Charge Current Status 00000 = 300 mA 00001 = 400 mA 00010 = 450 mA 00011 = 475 mA 00100 = 500 mA 00101 = 550 mA 00110 = 600 mA 00111 = 650 mA 01000 = 700 mA 01001 = 900 mA 01010 = 950 mA 01011 = 1000 mA 01100 = 1100 mA 01101 = 1200 mA 01110 = 1400 mA 01111 = 1450 mA 10000 = 1500 mA 10001 = 1600 mA 10010 = 1800 mA 10011 = 1850 mA 10100 = 1880 mA 10101 = 1910 mA 10110 = 1930 mA 10111 = 1950 mA 11000 = 1970 mA 11001 = 2000 mA

0x0000100E SMBCHGL_CHGR_CHGR_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_CHGR_CHGR_STS

Bits	Name	Description
7	BAT_I_STS	Battery Current Status 0 = Net charging current 1 = Net dis-charging current
6	AUTO_FV_COMP_STS	Automatic Float Voltage Compensation Status 0 = Inactive 1 = Active

SMBCHGL_CHGR_CHGR_STS (cont.)

Bits	Name	Description
5	DONE_STS	Done Status 0 = No charging cycles have terminated since Charging first enabled 1 = At least 1 charging cycle has terminated since Charging first enabled
4	BATV_LT_2V	Battery Voltage < 2V Status 0 =False 1 = True
3	HOLD_OFF_STS	Hold-Off Status 0 = Charger not in hold-off 1 = Charger in hold-off
2:1	CHARGING_STS	Charging Status 00 = No charging 01 = Pre-charging 10 = Fast-charging 11 = Taper charging
0	CHG_EN	Charge Enable 0 = Charging Command/Pin is not asserted 1 = Charging Command/Pin is asserted

0x00001010 SMBCHGL_CHGR_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_CHGR_INT_RT_STS

Bits	Name	Description
7	BAT_TCC_REACHED_RT_STS	signals if the battery current has reached the termination threshold
6	BAT_TAPER_MODE_CHARGING_RT_STS	indicates if the charger is in constant voltage mode
5	BAT_LT_RECHG_THRESHOLD_RT_STS	Recharge Real Time Status reports the pulse that sets the IRQ not an indication of the Vrech threshold
4	BAT_FT_P2F_CHG_THRESHOLD_RT_STS	the battery voltage has crossed the pre-to-fast voltage threshold
3	CHGR_COMPLETE_CHG_SFT_RT_STS	indicates if the charger has stopped due to the expiration of the total charge safety timer
2	CHGR_PRECHG_SFT_RT_STS	indicates if the charger has stopped due to the expiration of the pre-charge safety timer

SMBCHGL_CHGR_INT_RT_STS (cont.)

Bits	Name	Description
1	CHGR_INHIBIT_RT_STS	indicates if charging is currently being held-off due to the battery voltage being above the charger inhibit voltage threshold
0	CHGR_ERROR_RT_STS	indicates if any of the following events have happened: safety timer expiration, battery over-voltage, battery missing via algorithm

0x00001011 SMBCHGL_CHGR_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_CHGR_INT_SET_TYPE

Bits	Name	Description
7	BAT_TCC_REACHED_TYPE	
6	BAT_TAPER_MODE_CHARGING_TYPE	
5	BAT_LT_RECHG_THRESHOLD_TYPE	
4	BAT_FT_P2F_CHG_THRESHOLD_TYPE	
3	CHGR_COMPLETE_CHG_SFT_TYPE	
2	CHGR_PRECHG_SFT_TYPE	
1	CHGR_INHIBIT_TYPE	
0	CHGR_ERROR_TYPE	

0x00001012 SMBCHGL_CHGR_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_CHGR_INT_POLARITY_HIGH

Bits	Name	Description
7	BAT_TCC_REACHED_HIGH	

SMBCHGL_CHGR_INT_POLARITY_HIGH (cont.)

Bits	Name	Description
6	BAT_TAPER_MODE_CHARGING_HIGH	
5	BAT_LT_RECHG_THRESHOLD_HIGH	
4	BAT_FT_P2F_CHG_THRESHOLD_HIGH	
3	CHGR_COMPLETE_CHG_SFT_HIGH	
2	CHGR_PRECHG_SFT_HIGH	
1	CHGR_INHIBIT_HIGH	
0	CHGR_ERROR_HIGH	

0x00001013 SMBCHGL_CHGR_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_CHGR_INT_POLARITY_LOW

Bits	Name	Description
7	BAT_TCC_REACHED_LOW	
6	BAT_TAPER_MODE_CHARGING_LOW	
5	BAT_LT_RECHG_THRESHOLD_LOW	
4	BAT_FT_P2F_CHG_THRESHOLD_LOW	
3	CHGR_COMPLETE_CHG_SFT_LOW	
2	CHGR_PRECHG_SFT_LOW	
1	CHGR_INHIBIT_LOW	
0	CHGR_ERROR_LOW	

0x00001014 SMBCHGL_CHGR_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_CHGR_INT_LATCHED_CLR

Bits	Name	Description
7	BAT_TCC_REACHED_LATCHED_CLR	
6	BAT_TAPER_MODE_CHARGING_LATCHED_CLR	
5	BAT_LT_RECHG_THRESHOLD_LATCHED_CLR	
4	BAT_FT_P2F_CHG_THRESHOLD_LATCHED_CLR	
3	CHGR_COMPLETE_CHG_SFT_LATCHED_CLR	
2	CHGR_PRECHG_SFT_LATCHED_CLR	
1	CHGR_INHIBIT_LATCHED_CLR	
0	CHGR_ERROR_LATCHED_CLR	

0x00001015 SMBCHGL_CHGR_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

PMIC_SET_MASK

SMBCHGL_CHGR_INT_EN_SET

Bits	Name	Description
7	BAT_TCC_REACHED_EN_SET	
6	BAT_TAPER_MODE_CHARGING_EN_SET	
5	BAT_LT_RECHG_THRESHOLD_EN_SET	

SMBCHGL_CHGR_INT_EN_SET (cont.)

Bits	Name	Description
4	BAT_FT_P2F_CHG_THRESHOLD_EN_SET	
3	CHGR_COMPLETE_CHG_SFT_EN_SET	
2	CHGR_PRECHG_SFT_EN_SET	
1	CHGR_INHIBIT_EN_SET	
0	CHGR_ERROR_EN_SET	

0x00001016 SMBCHGL_CHGR_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

PMIC_CLR_MASK=INT_EN_SET

SMBCHGL_CHGR_INT_EN_CLR

Bits	Name	Description
7	BAT_TCC_REACHED_EN_CLR	
6	BAT_TAPER_MODE_CHARGING_EN_CLR	
5	BAT_LT_RECHG_THRESHOLD_EN_CLR	
4	BAT_FT_P2F_CHG_THRESHOLD_EN_CLR	
3	CHGR_COMPLETE_CHG_SFT_EN_CLR	
2	CHGR_PRECHG_SFT_EN_CLR	
1	CHGR_INHIBIT_EN_CLR	
0	CHGR_ERROR_EN_CLR	

0x00001018 SMBCHGL_CHGR_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_CHGR_INT_LATCHED_STS

Bits	Name	Description
7	BAT_TCC_REACHED_LATCHED_STS	signals if the battery current has reached the termination threshold
6	BAT_TAPER_MODE_CHARGING_LATCHED_STS	indicates if the charger is in constant voltage mode
5	BAT_LT_RECHG_THRESHOLD_LATCHED_STS	signals if the battery voltage has dropped below the automatic recharge voltage threshold
4	BAT_FT_P2F_CHG_THRESHOLD_LATCHED_STS	the battery voltage has crossed the pre-to-fast voltage threshold
3	CHGR_COMPLETE_CHG_SFT_LATCHED_STS	indicates if the charger has stopped due to the expiration of the total charge safety timer
2	CHGR_PRECHG_SFT_LATCHED_STS	indicates if the charger has stopped due to the expiration of the pre-charge safety timer
1	CHGR_INHIBIT_LATCHED_STS	indicates if charging is currently being held-off due to the battery voltage being above the charger inhibit voltage threshold
0	CHGR_ERROR_LATCHED_STS	indicates if any of the following events have happened: safety timer expiration, battery over-voltage, battery missing via algorithm

0x00001019 SMBCHGL_CHGR_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_CHGR_INT_PENDING_STS

Bits	Name	Description
7	BAT_TCC_REACHED_PENDING_STS	
6	BAT_TAPER_MODE_CHARGING_PENDING_STS	
5	BAT_LT_RECHG_THRESHOLD_PENDING_STS	
4	BAT_FT_P2F_CHG_THRESHOLD_PENDING_STS	

SMBCHGL_CHGR_INT_PENDING_STS (cont.)

Bits	Name	Description
3	CHGR_COMPLETE_CHG_SFT_PENDING_STS	
2	CHGR_PRECHG_SFT_PENDING_STS	
1	CHGR_INHIBIT_PENDING_STS	
0	CHGR_ERROR_PENDING_STS	

0x0000101A SMBCHGL_CHGR_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_CHGR_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	

0x0000101B SMBCHGL_CHGR_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_CHGR_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	

0x000010F1 SMBCHGL_CHGR_PCC_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_PCC_CFG

Bits	Name	Description
2:0	PCC	Pre Charge Current 0x0: PCC_100MA 0x1: PCC_150MA 0x2: PCC_200MA 0x3: PCC_250MA 0x4: PCC_550MA

0x000010F2 SMBCHGL_CHGR_FCC_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_FCC_CFG

Bits	Name	Description
3:0	FCC	Fast Charge Current 0x0: FCC_300MA 0x1: FCC_400MA 0x2: FCC_450MA 0x3: FCC_475MA 0x4: FCC_500MA 0x5: FCC_550MA 0x6: FCC_600MA 0x7: FCC_650MA 0x8: FCC_700MA 0x9: FCC_900MA 0xA: FCC_950MA 0xB: FCC_1000MA 0xC: FCC_1100MA 0xD: FCC_1200MA 0xE: FCC_1400MA 0x10: FCC_1500MA 0x11: FCC_1600MA 0x12: FCC_1800MA 0x13: FCC_1850MA 0x14: FCC_1880MA 0x15: FCC_1910MA 0x16: FCC_1930MA 0x17: FCC_1950MA 0x18: FCC_1970MA 0x19: FCC_2000MA

0x000010F3 SMBCHGL_CHGR_FCC_CMP_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_FCC_CMP_CFG

Bits	Name	Description
1:0	FCC_COMP	JEITA Fast Charge Current Compensation 0x0: FCC_COMP_250MA 0x1: FCC_COMP_700MA 0x2: FCC_COMP_900MA 0x3: FCC_COMP_1200MA

0x000010F4 SMBCHGL_CHGR_FV_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_FV_CFG

Bits	Name	Description
5:0	FV	Float Voltage 0x5: FV_3P6 0x6: FV_3P62 0x7: FV_3P64 0x8: FV_3P66 0x9: FV_3P68 0xA: FV_3P70 0xB: FV_3P72 0xC: FV_3P74 0xD: FV_3P76 0xE: FV_3P78 0xF: FV_3P80 0x10: FV_3P82 0x11: FV_3P84 0x12: FV_3P86 0x13: FV_3P88 0x14: FV_3P90 0x15: FV_3P92 0x16: FV_3P94 0x17: FV_3P96 0x18: FV_4P98 0x19: FV_4P00 0x1A: FV_4P02 0x1B: FV_4P04 0x1C: FV_4P06 0x1D: FV_4P08 0x1E: FV_4P10 0x1F: FV_4P12 0x20: FV_4P14 0x21: FV_4P16 0x22: FV_4P18 0x23: FV_4P20 0x24: FV_4P22 0x25: FV_4P24 0x26: FV_4P26 0x27: FV_4P28 0x28: FV_4P30 0x29: FV_4P32 0x2A: FV_4P34 0x2B: FV_4P35 0x2C: FV_4P36 0x2D: FV_4P38 0x2E: FV_4P40 0x2F: FV_4P42 0x30: FV_4P44

SMBCHGL_CHGR_FV_CFG (cont.)

Bits	Name	Description
		0x31: FV_4P46 0x32: FV_4P48 0x33: FV_4P50

0x000010F5 SMBCHGL_CHGR_FV_CMP_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_FV_CMP_CFG

Bits	Name	Description
5:0	FV_COMP	JEITA Float Voltage Compensation 000000 JEITA Float Voltage = Float Voltage Code - 0 .... 111111 JEITA Float Voltage = Float Voltage Code - 63 0x0: FV_CMP_SUB_0 0x1: FV_CMP_SUB_1 0x2: FV_CMP_SUB_2 0x3: FV_CMP_SUB_3 0x4: FV_CMP_SUB_4 0x5: FV_CMP_SUB_5 0x6: FV_CMP_SUB_6 0x7: FV_CMP_SUB_7 0x8: FV_CMP_SUB_8 0x9: FV_CMP_SUB_9 0xA: FV_CMP_SUB_10 0xB: FV_CMP_SUB_11 0xC: FV_CMP_SUB_12 0xD: FV_CMP_SUB_13 0xE: FV_CMP_SUB_14 0xF: FV_CMP_SUB_15 0x10: FV_CMP_SUB_16 0x11: FV_CMP_SUB_17 0x12: FV_CMP_SUB_18 0x13: FV_CMP_SUB_19 0x14: FV_CMP_SUB_20 0x15: FV_CMP_SUB_21 0x16: FV_CMP_SUB_22 0x17: FV_CMP_SUB_23 0x18: FV_CMP_SUB_24 0x19: FV_CMP_SUB_25 0x1A: FV_CMP_SUB_26 0x1B: FV_CMP_SUB_27 0x1C: FV_CMP_SUB_28 0x1D: FV_CMP_SUB_29 0x1E: FV_CMP_SUB_30 0x1F: FV_CMP_SUB_31 0x20: FV_CMP_SUB_32 0x21: FV_CMP_SUB_33 0x22: FV_CMP_SUB_34 0x23: FV_CMP_SUB_35 0x24: FV_CMP_SUB_36 0x25: FV_CMP_SUB_37 0x26: FV_CMP_SUB_38 0x27: FV_CMP_SUB_39 0x28: FV_CMP_SUB_40

SMBCHGL_CHGR_FV_CMP_CFG (cont.)

Bits	Name	Description
		0x29: FV_CMP_SUB_41 0x2A: FV_CMP_SUB_42 0x2B: FV_CMP_SUB_43 0x2C: FV_CMP_SUB_44 0x2D: FV_CMP_SUB_45 0x2E: FV_CMP_SUB_46 0x2F: FV_CMP_SUB_47 0x30: FV_CMP_SUB_48 0x31: FV_CMP_SUB_49 0x32: FV_CMP_SUB_50 0x33: FV_CMP_SUB_51 0x34: FV_CMP_SUB_52 0x35: FV_CMP_SUB_53 0x36: FV_CMP_SUB_54 0x37: FV_CMP_SUB_55 0x38: FV_CMP_SUB_56 0x39: FV_CMP_SUB_57 0x3A: FV_CMP_SUB_58 0x3B: FV_CMP_SUB_59 0x3C: FV_CMP_SUB_60 0x3D: FV_CMP_SUB_61 0x3E: FV_CMP_SUB_62 0x3F: FV_CMP_SUB_63

0x000010F6 SMBCHGL_CHGR_CFG_AFVC

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_CFG_AFVC

Bits	Name	Description
2:0	CHGR_AUTO_FV_COMP	Bits 2:0 - sets automatic float voltage compensation level adjusted for 3A charging (CFG_AFVC<2:0>) 000 Disabled 001 25mV 010 50mV 011 75mV 100 100mV 101 125mV 110 150mV 111 175mV 0x0: AUTO_FV_DISABLED 0x1: AUTO_FV_25MV 0x2: AUTO_FV_50MV 0x3: AUTO_FV_75MV 0x4: AUTO_FV_100MV 0x5: AUTO_FV_125MV 0x6: AUTO_FV_150MV 0x7: AUTO_FV_175MV

0x000010F7 SMBCHGL_CHGR_CFG_CHG_INHIB

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_CFG_CHG_INHIB

Bits	Name	Description
1:0	CHGR_INHIBIT_THRESHOLD	sets charge inhibit level 00 = VFLT-50mV 01 = VFLT-100mV 10 = VFLT-200mV 11 = VFLT-300mV 0x0: INHIBIT_50MV 0x1: INHIBIT_100MV 0x2: INHIBIT_200MV 0x3: INHIBIT_300MV

0x000010F8 SMBCHGL_CHGR_CFG_P2F

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_CFG_P2F

Bits	Name	Description
1:0	P2F_CHG_THRESHOLD	Pre-charge to Fast-charge threshold 00 = 2.4V 01 = 2.6V 10 = 2.8V 11 = 3.0V 0x0: P2F_2P4 0x1: P2F_2P6 0x2: P2F_2P8 0x3: P2F_3P0

0x000010F9 SMBCHGL_CHGR_CFG_TCC

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_CFG_TCC

Bits	Name	Description
2:0	CHG_TERM_I	Termination current threshold 000 = 300mA 001 = 50mA 010 = 100mA 011 = 150mA 100 = 200mA 101 = 250mA 110 =500mA 111 = 600mA 0x0: TERM_ANA_300MA 0x1: TERM_ANA_50MA 0x2: TERM_ANA_100MA 0x3: TERM_ANA_150MA 0x4: TERM_ANA_200MA 0x5: TERM_ANA_250MA 0x6: TERM_ANA_500MA 0x7: TERM_ANA_600MA

0x000010FA SMBCHGL_CHGR_CCMP_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_CCMP_CFG

Bits	Name	Description
6	CCMP_CFG_6	Reserved
5	JEITA_TEMP_HARD_LIMIT	JEITA Temperature Hard Limit 0 = Enabled 1 = Disabled 0x0: JEITA_TEMP_HARD_LIMIT_EN 0x1: JEITA_TEMP_HARD_LIMIT_DIS
4	LOAD_BAT	Load Battery during Float Voltage Compensation 0 = Disable 1 = Enable 0x0: LOAD_BATT_FV_COMP_DIS 0x1: LOAD_BATT_FV_COMP_EN

SMBCHGL_CHGR_CCMP_CFG (cont.)

Bits	Name	Description
3	HOT_SL_FV_COMP	Hot SL Float Voltage Compensation 0 = Disable 1 = Enable 0x0: HOT_SOFT_LIMIT_FV_COMP_DIS 0x1: HOT_SOFT_LIMIT_FV_COMP_EN
2	COLD_SL_FV_COMP	Cold SL Float Voltage Compensation 0 = Disable 1 = Enable 0x0: COLD_SOFT_LIMIT_FV_COMP_DIS 0x1: COLD_SOFT_LIMIT_FV_COMP_EN
1	HOT_SL_CHG_I_COMP	Hot SL Charge Current Compensation 0 = Disable 1 = Enable 0x0: HOT_SOFT_LIMIT_CC_COMP_DIS 0x1: HOT_SOFT_LIMIT_CC_COMP_EN
0	COLD_SL_CHG_I_COMP	Cold SL Charge Current Compensation 0 = Disable 1 = Enable 0x0: COLD_SOFT_LIMIT_CC_COMP_DIS 0x1: COLD_SOFT_LIMIT_CC_COMP_EN

0x000010FB SMBCHGL_CHGR_CHGR_CFG1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_CHGR_CFG1

Bits	Name	Description
7	SYSOK_INOK_POL	SYSOK/INOK Polarity 0 = Table in DOS 1 = Inverse of Table in DOS 0x0: SYSOK_TABLE 0x1: SYSOK_TABLE_N

SMBCHGL_CHGR_CHGR_CFG1 (cont.)

Bits	Name	Description
6:4	SYSOK_OPTIONS	000 = INOK option 1 001 = INOK option 2 010 = SYSOK option A option 1 011 = SYSOK option A option 2 100 = SYSOK option B/C option 1 101 = SYSOK option B/C option 2 110 = Charge detect option 1 111 = Charge detect option 2 0x0: INOK_OPT_1 0x1: INOK_OPT_2 0x2: SYSOK_OPT_A_1 0x3: SYSOK_OPT_A_2 0x4: SYSOK_OPT_BC_1 0x5: SYSOK_OPT_BC_2 0x6: CHG_DET_OPT_1 0x7: CHG_DET_OPT_2
3	EARLY_TERM_STATUS	Termination on Stat Pin 0 = Disabled 1 = Enabled 0x0: EARLY_CURRENT_TERM_DIS 0x1: EARLY_CURRENT_TERM_EN
2	TERM_I_SRC	Termination Current Source 0 = Analog sensor 1 = Fuel GaugeADC 0x0: TERM_SRC_ANA 0x1: TERM_SRC_FG
1	RECHG_THRESHOLD_SRC	Recharge Threshold Source 0 = Analog sensor 1 = Fuel GaugeADC 0x0: RCHG_SRC_ANA 0x1: RCHG_SRC_FG
0	CHARGING_HOLDOFF	0 = Wait for FG Ready 1 = continue without FG Ready 0x0: WAIT_FOR_FG 0x1: NO_WAIT_FOR_FG

0x000010FC SMBCHGL_CHGR_CHGR_CFG2

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_CHGR_CFG2

Bits	Name	Description
7	CHG_EN_SRC	Charge Enable Source 0 = Command Register 1 = Enable Pin 0x0: CHG_EN_SRC_CMD 0x1: CHG_EN_SRC_PIN
6	CHG_EN_COMMAND	Charge Enable Command or Pin Polarity 0 = Active high (1 : enable charging) 1 = Active low (0 : enable charging) 0x0: CHG_EN_POL_HIGH 0x1: CHG_EN_POL_LOW
5	P2F_CHG_TRAN	Pre to Fast Charge Transition 0 = Automatic 1 = Requires command 0x0: PRE_FAST_AUTO 0x1: PRE_FAST_CMD
4	BAT_OV_ECC	Battery OV Ends Charge Cycle 0 = Disabled 1 = Enabled 0x0: BATT_OV_ENDS_CYCLE_DIS 0x1: BATT_OV_ENDS_CYCLE_EN
3	I_TERM	Current Termination 0 = Enabled 1 = Disabled 0x0: CURRENT_TERM_EN 0x1: CURRENT_TERM_DIS
2	AUTO_RECHG	Automatic Recharge 0 = Enabled 1 = Disabled 0x0: AUTO_RCHG_EN 0x1: AUTO_RCHG_DIS
1	HOLD_OFF_TIMER_CHARGING	Charging Hold-Off Timer after Plug-In 0 = 700us 1 = 350ms 0x0: HOLDOFF_TMR_700US 0x1: HOLDOFF_TMR_350MS
0	CHARGER_INHIBIT	0 = Disabled 1 = Enabled 0x0: CHG_INHIBIT_DIS 0x1: CHG_INHIBIT_EN

0x000010FD SMBCHGL_CHGR_SFT_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_SFT_CFG

Bits	Name	Description
5:4	SFT_EN	Safety Timer Enable 00 = Pre-Charge and Total Charge Safety Timers Enabled 01 = Pre-Charge Safety Timer Disabled, Total Charge Safety Timer Enabled 1X = Pre-Charge and Total Charge Safety Timers Disabled 0x0: PC_EN_TC_EN 0x1: PC_DIS_TC_EN 0x2: PC_DIS_TC_DIS
3:2	SFT_TIMEOUT	Total Charge Safety Timer Timeout 00 = 192min 01 = 384min 10 = 768min 11 = 1536min 0x0: TC_TMOUT_192MIN 0x1: TC_TMOUT_384MIN 0x2: TC_TMOUT_768MIN 0x3: TC_TMOUT_1536MIN
1:0	PRE_CHG_SFT_TIMEOUT	Pre Charge Safety Timer Timeout 00 = 24min 01 = 48min 10 = 96min 11 = 192min 0x0: PC_TMOUT_24MIN 0x1: PC_TMOUT_48MIN 0x2: PC_TMOUT_96MIN 0x3: PC_TMOUT_192MIN

0x000010FE SMBCHGL_CHGR_STAT_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_STAT_CFG

Bits	Name	Description
4	STAT_CFG_4	Reserved
3	TEMP_CHG_ERROR_BLINKING_EN	Temperature and Charge Error Blinking (only for Charging Status) 0 = Disabled 1 = Enabled 0x0: STAT_BLINKING_DIS 0x1: STAT_BLINKING_EN
2	STAT_PIN_SRC	STAT Pin Source 0 = Charging Status 1 = USB Fail Status 0x0: STAT_CHG_STS 0x1: STAT_USB_FAIL
1	STAT_PIN_OUTPUT_POL	STAT Pin Output Polarity 0 = Active low 1 = Active high 0x0: STAT_ACTIVE_LOW 0x1: STAT_ACTIVE_HIGH
0	STAT_PIN_OUTPUT_EN	STAT Pin Output 0 = Enabled 1 = Disabled 0x0: STAT_OUTPUT_EN 0x1: STAT_OUTPUT_DIS

0x000010FF SMBCHGL_CHGR_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x80

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_CHGR_CFG

Bits	Name	Description
7	CHG_OPTION_PIN_TRIM	This trim bit is fed back to CHG_OPTION_PIN of reg 0x08 of SMBCHGL_CHGR peripheral
3	CFG_VCHG_IIN	selects what VCHG pin outputs 0 = Battery Charge/Discharge current 1= Input current 0x0: VCHG_BATTERY_CURRENT 0x1: VCHG_INPUT_CURRENT

SMBCHGL_CHGR_CFG (cont.)

Bits	Name	Description
2	CFG_TAPER_DIS_AFVC	selects whether taper mode disables AFVC 0 = does not disable AFVC in taper 1 = does disable AFVC in taper 0x0: AFVC_ACTIVE_IN_TAPER 0x1: AFVC_DISABLE_IN_TAPER
1	CFG_VCHG	VCHG Function 0 = Disabled 1 = Enabled 0x0: VCHG_DIS 0x1: VCHG_EN
0	CFG_RCHG_LVL	selects recharge threshold 0= VFLT-100mV 1 = VFLT-200mV 0x0: RCHG_THRESH_100MV 0x1: RCHG_THRESH_200MV

10 SMBCHGL_OTG_SMBCHGL_OTG

0x00001104 SMBCHGL_OTG_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: NA

PMIC_CONSTANT

SMBCHGL_OTG_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	

0x00001105 SMBCHGL_OTG_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x58

Reset Name: NA

PMIC_CONSTANT

SMBCHGL_OTG_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	

0x00001110 SMBCHGL_OTG_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_OTG_INT_RT_STS

Bits	Name	Description
4	OTG_OC_DIS_SW_STS	OTG Overcurrent Disabled Switcher
3	RID_CHANGE_DET_STS	USBID Resistance Changed Detected (not valid for Fuel Gauge monitoring of USBID) - IRQ is set by a pulse - status has no meaning
2	RID_GND_DET_STS	USBID Grounded Detected (valid for Fuel Gauge and Non Fuel Gauge monitoring of USBID)
1	OTG_OVERCURRENT_RT_STS	The OTG output current reached the current limit setting, and caused the output voltage to drop below 3.6V
0	OTG_FAIL_RT_STS	OTG was running, but disabled due to some event

0x00001111 SMBCHGL_OTG_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_OTG_INT_SET_TYPE

Bits	Name	Description
4	OTG_OC_DIS_SW_TYPE	
3	RID_CHANGE_DET_TYPE	
2	RID_GND_DET_TYPE	
1	OTG_OVERCURRENT_TYPE	
0	OTG_FAIL_TYPE	

0x00001112 SMBCHGL_OTG_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_OTG_INT_POLARITY_HIGH

Bits	Name	Description
4	OTG_OC_DIS_SW_HIGH	
3	RID_CHANGE_DET_HIGH	
2	RID_GND_DET_HIGH	
1	OTG_OVERCURRENT_HIGH	
0	OTG_FAIL_HIGH	

0x00001113 SMBCHGL_OTG_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_OTG_INT_POLARITY_LOW

Bits	Name	Description
4	OTG_OC_DIS_SW_LOW	
3	RID_CHANGE_DET_LOW	
2	RID_GND_DET_LOW	
1	OTG_OVERCURRENT_LOW	
0	OTG_FAIL_LOW	

0x00001114 SMBCHGL_OTG_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_OTG_INT_LATCHED_CLR

Bits	Name	Description
4	OTG_OC_DIS_SW_LATCHED_CLR	
3	RID_CHANGE_DET_LATCHED_CLR	

SMBCHGL_OTG_INT_LATCHED_CLR (cont.)

Bits	Name	Description
2	RID_GND_DET_LATCHED_CLR	
1	OTG_OVERCURRENT_LATCHED_CLR	
0	OTG_FAIL_LATCHED_CLR	

0x00001115 SMBCHGL_OTG_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

PMIC_SET_MASK

SMBCHGL_OTG_INT_EN_SET

Bits	Name	Description
4	OTG_OC_DIS_SW_EN_SET	
3	RID_CHANGE_DET_EN_SET	
2	RID_GND_DET_EN_SET	
1	OTG_OVERCURRENT_EN_SET	
0	OTG_FAIL_EN_SET	

0x00001116 SMBCHGL_OTG_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

PMIC_CLR_MASK=INT_EN_SET

SMBCHGL_OTG_INT_EN_CLR

Bits	Name	Description
4	OTG_OC_DIS_SW_EN_CLR	

SMBCHGL_OTG_INT_EN_CLR (cont.)

Bits	Name	Description
3	RID_CHANGE_DET_EN_CLR	
2	RID_GND_DET_EN_CLR	
1	OTG_OVERCURRENT_EN_CLR	
0	OTG_FAIL_EN_CLR	

0x00001118 SMBCHGL_OTG_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_OTG_INT_LATCHED_STS

Bits	Name	Description
4	OTG_OC_DIS_SW_LATCHED_STS	OTG Overcurrent Disabled Switcher
3	RID_CHANGE_DET_LATCHED_STS	USBID Resistance Changed Detected (not valid for Fuel Gauge monitoring of USBID)
2	RID_GND_DET_LATCHED_STS	USBID Grounded Detected (valid for Fuel Gauge and Non Fuel Gauge monitoring of USBID)
1	OTG_OVERCURRENT_LATCHED_STS	The OTG output current reached the current limit setting, and caused the output voltage to drop below 3.6V
0	OTG_FAIL_LATCHED_STS	OTG was running, but disabled due to some event

0x00001119 SMBCHGL_OTG_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_OTG_INT_PENDING_STS

Bits	Name	Description
4	OTG_OC_DIS_SW_PENDING_STS	
3	RID_CHANGE_DET_PENDING_STS	

SMBCHGL_OTG_INT_PENDING_STS (cont.)

Bits	Name	Description
2	RID_GND_DET_PENDING_STS	
1	OTG_OVERCURRENT_PENDING_STS	
0	OTG_FAIL_PENDING_STS	

0x0000111A SMBCHGL_OTG_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_OTG_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	

0x0000111B SMBCHGL_OTG_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_OTG_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	

0x000011F1 SMBCHGL_OTG_OTG_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_OTG_OTG_CFG

Bits	Name	Description
7	OTG_OC_FLG	Reserved
6	OTG_OC_CFG	OTG Hiccup Mode 0 = Disabled 1 = Enabled 0x0: HICCUP_DISABLED 0x1: HICCUP_ENABLED
5	HV_OTG_PROTECTION	0 = Disabled 1 = Enabled 0x0: HV_OTG_DISABLED 0x1: HV_OTG_ENABLED
4	OTG_PIN_POL	0 = Active High 1 = Active Low 0x0: OTG_PIN_POL_HIGH 0x1: OTG_PIN_POL_LOW
3:2	OTG_CTRL	00 = Command register with RID Disabled (DO NOT USE) 01 = Pin control with RID Disabled (DO NOT USE) 10 = Command register with RID Enabled 11 = Auto OTG (RID Enabled) 0x2: OTG_CTRL_CMD 0x3: OTG_CTRL_AUTO
1:0	OTG_UVLO_SENSOR_SRC	0X = Analog comparator 10 = Fuel Gauge ADC 11 = OR of both 0x0: OTG_UVLO_SENSOR_ANA 0x2: OTG_UVLO_SENSOR_FG 0x3: OTG_UVLO_SENSOR_OR

0x000011F2 SMBCHGL_OTG_CFG_BATTUV

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_OTG_CFG_BATTUV

Bits	Name	Description
1:0	CFG_BATTUV	sets OTG battery under-voltage lockout 00 = 2.7V 01 = 2.9V 10 = 3.1V 11 = 3.3V 0x0: OTG_BATTUV_2P7 0x1: OTG_BATTUV_2P9 0x2: OTG_BATTUV_3P1 0x3: OTG_BATTUV_3P3

0x000011F3 SMBCHGL_OTG_OTG_ICFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_OTG_OTG_ICFG

Bits	Name	Description
1:0	OTG_ILIMIT	OTG mode output current limit settings 00 = 250mA 01 = 600mA 10 = 750mA 11 = 1000mA 0x0: OTG_ILIMIT_250MA 0x1: OTG_ILIMIT_600MA 0x2: OTG_ILIMIT_750MA 0x3: OTG_ILIMIT_1000MA

11 SMBCHGL_BAT_IF_SMBCHGL_BATIF

0x00001204 SMBCHGL_BAT_IF_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: NA

PMIC_CONSTANT

SMBCHGL_BAT_IF_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	

0x00001205 SMBCHGL_BAT_IF_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x53

Reset Name: NA

PMIC_CONSTANT

SMBCHGL_BAT_IF_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	

0x00001208 SMBCHGL_BAT_IF_BAT_PRES_STATUS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_BAT_IF_BAT_PRES_STATUS

Bits	Name	Description
7	BAT_PRES	Battery presence status: 0 = battery not present, 1 = battery present

0x00001210 SMBCHGL_BAT_IF_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_BAT_IF_INT_RT_STS

Bits	Name	Description
7	BAT_TERM_MISSING_RT_STS	the battery + voltage terminal has been determined to be missing via the internal algorithm
6	BAT_MISSING_RT_STS	the battery thermistor or ID terminal has been determined to be missing
5	BAT_LOW_RT_STS	The battery voltage has crossed the low battery voltage threshold
4	BAT_OV_RT_STS	the battery voltage is above the battery OV level of Vfloat + 100mV
3	COLD_BAT_SOFT_LIM_RT_STS	The battery temperature has crossed the cold soft limit temperature threshold
2	COLD_BAT_HARD_LIM_RT_STS	The battery temperature has crossed the cold hard limit temperature threshold
1	HOT_BAT_SOFT_LIM_RT_STS	The battery temperature has crossed the hot soft limit temperature threshold
0	HOT_BAT_HARD_LIM_RT_STS	The battery temperature has crossed the hot hard limit temperature threshold

0x00001211 SMBCHGL_BAT_IF_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_BAT_IF_INT_SET_TYPE

Bits	Name	Description
7	BAT_TERM_MISSING_TYPE	
6	BAT_MISSING_TYPE	
5	BAT_LOW_TYPE	
4	BAT_OV_TYPE	
3	COLD_BAT_SOFT_LIM_TYPE	
2	COLD_BAT_HARD_LIM_TYPE	
1	HOT_BAT_SOFT_LIM_TYPE	
0	HOT_BAT_HARD_LIM_TYPE	

0x00001212 SMBCHGL_BAT_IF_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_BAT_IF_INT_POLARITY_HIGH

Bits	Name	Description
7	BAT_TERM_MISSING_HIGH	
6	BAT_MISSING_HIGH	
5	BAT_LOW_HIGH	
4	BAT_OV_HIGH	
3	COLD_BAT_SOFT_LIM_HIGH	
2	COLD_BAT_HARD_LIM_HIGH	
1	HOT_BAT_SOFT_LIM_HIGH	

SMBCHGL_BAT_IF_INT_POLARITY_HIGH (cont.)

Bits	Name	Description
0	HOT_BAT_HARD_LIM_HIGH	

0x00001213 SMBCHGL_BAT_IF_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_BAT_IF_INT_POLARITY_LOW

Bits	Name	Description
7	BAT_TERM_MISSING_LOW	
6	BAT_MISSING_LOW	
5	BAT_LOW_LOW	
4	BAT_OV_LOW	
3	COLD_BAT_SOFT_LIM_LOW	
2	COLD_BAT_HARD_LIM_LOW	
1	HOT_BAT_SOFT_LIM_LOW	
0	HOT_BAT_HARD_LIM_LOW	

0x00001214 SMBCHGL_BAT_IF_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_BAT_IF_INT_LATCHED_CLR

Bits	Name	Description
7	BAT_TERM_MISSING_LATCHED_CLR	
6	BAT_MISSING_LATCHED_CLR	
5	BAT_LOW_LATCHED_CLR	
4	BAT_OV_LATCHED_CLR	

SMBCHGL_BAT_IF_INT_LATCHED_CLR (cont.)

Bits	Name	Description
3	COLD_BAT_SOFT_LIM_LATCHED_CLR	
2	COLD_BAT_HARD_LIM_LATCHED_CLR	
1	HOT_BAT_SOFT_LIM_LATCHED_CLR	
0	HOT_BAT_HARD_LIM_LATCHED_CLR	

0x00001215 SMBCHGL_BAT_IF_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

PMIC_SET_MASK

SMBCHGL_BAT_IF_INT_EN_SET

Bits	Name	Description
7	BAT_TERM_MISSING_EN_SET	
6	BAT_MISSING_EN_SET	
5	BAT_LOW_EN_SET	
4	BAT_OV_EN_SET	
3	COLD_BAT_SOFT_LIM_EN_SET	
2	COLD_BAT_HARD_LIM_EN_SET	
1	HOT_BAT_SOFT_LIM_EN_SET	
0	HOT_BAT_HARD_LIM_EN_SET	

0x00001216 SMBCHGL_BAT_IF_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

PMIC_CLR_MASK=INT_EN_SET

SMBCHGL_BAT_IF_INT_EN_CLR

Bits	Name	Description
7	BAT_TERM_MISSING_EN_CLR	
6	BAT_MISSING_EN_CLR	
5	BAT_LOW_EN_CLR	
4	BAT_OV_EN_CLR	
3	COLD_BAT_SOFT_LIM_EN_CLR	
2	COLD_BAT_HARD_LIM_EN_CLR	
1	HOT_BAT_SOFT_LIM_EN_CLR	
0	HOT_BAT_HARD_LIM_EN_CLR	

0x00001218 SMBCHGL_BAT_IF_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_BAT_IF_INT_LATCHED_STS

Bits	Name	Description
7	BAT_TERM_MISSING_LATCHED_STS	the battery + voltage terminal has been determined to be missing via the internal algorithm
6	BAT_MISSING_LATCHED_STS	the battery thermistor or ID terminal has been determined to be missing
5	BAT_LOW_LATCHED_STS	The battery voltage has crossed the low battery voltage threshold
4	BAT_OV_LATCHED_STS	the battery voltage is above the battery OV level of Vfloat + 100mV

SMBCHGL_BAT_IF_INT_LATCHED_STS (cont.)

Bits	Name	Description
3	COLD_BAT_SOFT_LIM_LATCHED_STS	The battery temperature has crossed the cold soft limit temperature threshold
2	COLD_BAT_HARD_LIM_LATCHED_STS	The battery temperature has crossed the cold hard limit temperature threshold
1	HOT_BAT_SOFT_LIM_LATCHED_STS	The battery temperature has crossed the hot soft limit temperature threshold
0	HOT_BAT_HARD_LIM_LATCHED_STS	The battery temperature has crossed the hot hard limit temperature threshold

0x00001219 SMBCHGL_BAT_IF_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_BAT_IF_INT_PENDING_STS

Bits	Name	Description
7	BAT_TERM_MISSING_PENDING_STS	
6	BAT_MISSING_PENDING_STS	
5	BAT_LOW_PENDING_STS	
4	BAT_OV_PENDING_STS	
3	COLD_BAT_SOFT_LIM_PENDING_STS	
2	COLD_BAT_HARD_LIM_PENDING_STS	
1	HOT_BAT_SOFT_LIM_PENDNG_STS	
0	HOT_BAT_HARD_LIM_PENDING_STS	

0x0000121A SMBCHGL_BAT_IF_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_BAT_IF_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	

0x0000121B SMBCHGL_BAT_IF_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_BAT_IF_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	

0x00001240 SMBCHGL_BAT_IF_SHIP_MODE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: ship_mode_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_BAT_IF_SHIP_MODE

Bits	Name	Description
0	SHIP_MODE_ENB	0 = Enables Ship Mode 1 = Not in Ship Mode

0x00001241 SMBCHGL_BAT_IF_CLR_DEAD_BAT_TIMER

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_BAT_IF_CLR_DEAD_BAT_TIMER

Bits	Name	Description
0	CLR_DEAD_BAT_TIMER	

0x00001242 SMBCHGL_BAT_IF_CMD_CHG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_BAT_IF_CMD_CHG

Bits	Name	Description
6	OTG_BYPASS_CMD	Reserved
5	WIRELESS_CHG_DIS	Reserved
4	CMD_CHG_4	Reserved
3	STAT_OUTPUT	Stat Output - 0 = STAT output enabled - 1 = Turn off STAT pim
2	FC_COM	Fast Charge Command 0 = Allow pre-charge current 1 = Force Fast Charge
1	EN_BAT_CHG	Enable Battery Charging 0 = Charge Disable/Enable (polarity from CHGR_CFG2[6] of Charger peripheral) 1 = Charge Enable/Disable (polarity from CHGR_CFG2[6] of Charger peripheral)
0	OTG_EN	OTG Enable 0 = Disable 1 = Enable

0x00001243 SMBCHGL_BAT_IF_CMD_CHG_LED

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: PERPH_rb

SMBCHGL_BAT_IF_CMD_CHG_LED

Bits	Name	Description
7:3	CHG_LED_EXTRA	Reserved
2:1	CHG_LED_BLINKING_CFG	CHG_LED Blinking Configuration 00 = Off 01 = Blinking Pattern 1 - 150ms on, 750ms off 10 = Blinking Pattern 2 - 500ms on, 3000ms off 11 = On

SMBCHGL_BAT_IF_CMD_CHG_LED (cont.)

Bits	Name	Description
0	EN_SW_CTRL	Enable Software Control 0 = Charger Controls Blinking 1 = Software Controls Blinking

0x000012D0 SMBCHGL_BAT_IF_SEC_ACCESS

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKING

SMBCHGL_BAT_IF_SEC_ACCESS

Bits	Name	Description
7:0	SEC_UNLOCK	Unlock the Secure Registers (0xTBD) by writing 0xA5 to this register. Lock is rearmed after the next write to the module.

0x000012F1 SMBCHGL_BAT_IF_VBL_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_BAT_IF_VBL_CFG

Bits	Name	Description
3:0	LOW_BAT_THRESHOLD	Low Battery Threshold 0000 = Disabled 0001 = 2.50V 0010 = 2.60V 0011 = 2.70V 0100 = 2.80V 0101 = 2.90V 0110 = 3.00V 0111 = 3.10V 1000 = 3.70V 1001 = 2.88V 1010 = 3.00V 1011 = 3.10V 1100 = 3.25V 1101 = 3.35V 1110 = 3.46V 1111 = 3.58V 0x0: LOW_BATTERY_DISABLED 0x1: LOW_BATTERY_THRESH_2P5 0x2: LOW_BATTERY_THRESH_2P6 0x3: LOW_BATTERY_THRESH_2P7 0x4: LOW_BATTERY_THRESH_2P8 0x5: LOW_BATTERY_THRESH_2P9 0x6: LOW_BATTERY_THRESH_3P0 0x7: LOW_BATTERY_THRESH_3P1 0x8: LOW_BATTERY_THRESH_3P7 0x9: LOW_BATTERY_THRESH_2P88 0xA: LOW_BATTERY_THRESH_3P00 0xB: LOW_BATTERY_THRESH_3P10 0xC: LOW_BATTERY_THRESH_3P25 0xD: LOW_BATTERY_THRESH_3P35 0xE: LOW_BATTERY_THRESH_3P46 0xF: LOW_BATTERY_THRESH_358

0x000012F2 SMBCHGL_BAT_IF_VBL_SEL_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_BAT_IF_VBL_SEL_CFG

Bits	Name	Description
7	VBL_SEL_CFG_7	Reserved
6	VBL_SEL_CFG_6	Reserved
5	SYSOK_BMA_OPTION	SYSOK BMA Option 0 = SYSOK waits for BMA result before enabling 1 = SYSOK does not wait for BMA result before enabling 0x0: SYSOK_WAIT 0x1: SYSOK_NO_WAIT
4	BM_IP	Battery Missing Poller Option 0 = BMP allowed when charging disabled 1 = BMP allowed only when charging reaches termination 0x0: BMA_CHG_DIS 0x1: BMA_CHG_TERM
3	SYSOK_BM_DONE	BMA Done Option for SYSOK Block 0 = BMA Done uses charge inhibit fix 1 = Old BMA Done Signal 0x0: NEW_DMA_DONE 0x1: OLD_BMA_DONE
2	VBAT_LOW_STATE	0 = Vbatt Low Deglitcher Output Defaults Low (VBATT > VBATT_LOW) 1 = Vbatt Low Deglitcher Output Defaults high (VBATT < VBATT_LOW) 0x0: LOW_BATT_DG_LOW 0x1: LOW_BATT_DG_HIGH
1	AICL_THRESH_5VTO9V	Reserved
0	DCD_TIMEOUT_DELAY	0 = 600ms DCD Timeout Delay 1 = 300ms DCD Timeout Delay 0x0: DCD_600MS 0x1: DCD_300MS

0x000012F3 SMBCHGL_BAT_IF_BM_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_BAT_IF_BM_CFG

Bits	Name	Description
7:6	BMD_RMV_CFG	Battery Missing detection timer 00 = 80us 01 = 160us 10 = 320us 11 = 640us 0x0: BMD_RMV_80US 0x1: BMD_RMV_160US 0x2: BMD_RMV_320US 0x3: BMD_RMV_640US
5	BAT_FET_CFG	Battery FET Configuration 0 = Normal operation 1 = override (turn off FET) 0x0: BATT_FET_NORMAL 0x1: BATT_FET_OVERRIDE
4	BAT_MISSING_INPUT_PLUGIN	Battery Missing on Input Plug-In 0 = Disabled 1 = Enabled 0x0: BMA_PLUG_IN_DIS 0x1: BMA_PLUG_IN_EN
3	BAT_MISSING_2S6_POLLER	Battery Missing 2.6s Poller 0 = Disabled 1 = Enabled 0x0: BMA_POLLER_DIS 0x1: BMA_POLLER_EN
2	BAT_MISSING_ALGORITHM	Battery Missing Algorithm 0 = Disabled 1 = Enabled 0x0: BMA_DIS 0x1: BMA_EN
1:0	BAT_MISSING_PIN_SRC	0X = Do Not Use THERM pin 1X = Use THERM pin X0 = Do Not Use BMD pin X1 = Use BMD pin

0x000012F4 SMBCHGL_BAT_IF_CFG_SYSMIN

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_BAT_IF_CFG_SYSMIN

Bits	Name	Description
1:0	CFG_SYSMIN	Minimum system voltage setting 00 = 3.15V 01 = 3.45V 10 = 3.60V 11 = 3.60V 0x0: SYSMIN_3P15 0x1: SYSMIN_3P45 0x2: SYSMIN_3P6 0x3: SYSMIN_3P60

0x000012F5 SMBCHGL_BAT_IF_CFG_SYSTH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_BAT_IF_CFG_SYSTH

Bits	Name	Description
1	CFG_EN_100M	0 = MAX VSYS=VFLT+200mv 1 = MAX VSYS= VFLT+100mv 0x0: VSYS_VBATT_TRACK_200MV 0x1: VSYS_VBATT_TRACK_100MV
0	CFG_SYSTH	selects VSYS regulation voltage when charging is disabled 0 = when charging disabled, VBATT tracking up to VSYSMAX 1 = VSYS tracking VBATT when charging disabled, this bit should always set to 1 to prevent boost back 0x0: VSYS_SYSMAX 0x1: VSYS_VBATT

0x000012F7 SMBCHGL_BAT_IF_TRIM7

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_BAT_IF_TRIM7

Bits	Name	Description
5:3	TR_STDBYOSC_TEMP_TRIM	Standby Oscillator Temperature Trim
2	CFG_TLLS	OTST1 Trip Point 0 =OTST1 @ 92C 1 = OTST1 @ 101C 0x0: OTST1_92C 0x1: OTST1_101C
1	TRIM7_1	Reserved
0	CFG_EN_FREQFOLD	0 =disables frequency foldback mode 1 = enables frequency foldback mode 0x0: FREQ_FOLDBACK_DIS 0x1: FREQ_FOLDBACK_EN

12 SMBCHGL_USB_SMBCHGL_USB

0x00001304 SMBCHGL_USB_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: NA

PMIC_CONSTANT

SMBCHGL_USB_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	

0x00001305 SMBCHGL_USB_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x54

Reset Name: NA

PMIC_CONSTANT

SMBCHGL_USB_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	

0x00001307 SMBCHGL_USB_ICL_STS_1

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_USB_ICL_STS_1

Bits	Name	Description
7	OTST1	0 = Not in Temperature Regulation 1 = In Temperature Regulation
6	ICL_MIN	AICL Status 0 = AICL did not enter Suspend 1 = AICL entered Suspend
5	AICL_STS	AICL Status 0 = AICL in progress 1 = AICL complete
4:0	ICL_STS	Input Current Limit 00000 = 300 mA 00001 = 400 mA 00010 = 450 mA 00011 = 475 mA 00100 = 500 mA 00101 = 550 mA 00110 = 600 mA 00111 = 650 mA 01000 = 700 mA 01001 = 900 mA 01010 = 950 mA 01011 = 1000 mA 01100 = 1100 mA 01101 = 1200 mA 01110 = 1400 mA 01111 = 1450 mA 10000 = 1500 mA 10001 = 1600 mA (only for PMI8940) 10010 = 1800 mA (only for PMI8940) 10011 = 1850 mA (only for PMI8940) 10100 = 1880 mA (only for PMI8940) 10101 = 1910 mA (only for PMI8940) 10110 = 1930 mA (only for PMI8940) 10111 = 1950 mA (only for PMI8940) 11000 = 1970 mA (only for PMI8940) 11001 = 2000 mA (only for PMI8940)

0x00001308 SMBCHGL_USB_PWR_PTH_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_USB_PWR_PTH_STS

Bits	Name	Description
1:0	POWER_PATH	PMIC power path status 00: not used 01: powered from battery 10: powered from USB charger 11: powered from DC charger

0x00001309 SMBCHGL_USB_ICL_STS_2

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_USB_ICL_STS_2

Bits	Name	Description
7	SOFT_ILIMIT	0 = Not in Soft Limit 1 = In Soft Limit
6	HIGH_DUTY_CYCLE_PULSE	0 = Switcher not in High Duty Cycle 1 = Switcher in High Duty Cycle
5:4	ICL_MODE	Input Current Limit Mode 00 = High Current 01 = 100mA 10 = 500mA 11 = Reserved
3	USBIN_SUSPEND_STS	USBIN Suspend Status 0 = Not suspended 1 = Suspended
2	DCIN_SUSPEND_STS	Reserved
1	USBIN_ACTIVE_PWR_SRC	USBIN active power source 0 = Not USBIN 1 = USBIN
0	DCIN_ACTIVE_PWR_SRC	Reserved

0x0000130A SMBCHGL_USB_APSD_DG_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_USB_APSD_DG_STS

Bits	Name	Description
3	DCD_TIMEOUT	DCD Timeout status 0 = Data Connect Device Not Time Out 1 = Data Connect Device Timed Out
2	DCD_GOOD_DG	Data Connect Device Deglitch status 0 = Data Connect Device Not Deglitched 1 = Data Connect Device Deglitched
1	OCD_GOOD_DG	Other Charger Device Data Connect Deglitch status 0 = Other Charger Device Data Connect Not Deglitched 1 = Other Charger Device Data Connect Deglitched
0	RID_ABC_DG	RID-A/B/C Data Connect Detect Deglitch status SMB RID Algorithm Only) 0 = RID-A/B/C Data Connect Detect Not Deglitched 1 = RID-A/B/C Data Connect Detect Deglitched

0x0000130B SMBCHGL_USB_RID_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_USB_RID_STS

Bits	Name	Description
3:0	RID_STS	RID Status 0000 = RID State Machine detected RID_GND 1XXX = RID State Machine detected RID_FLOAT

0x0000130D SMBCHGL_USB_INPUT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_USB_INPUT_STS

Bits	Name	Description
5:3	USBIN_INPUT_STS	USBIN Input Status 000 = No USBIN Charger Detected 100 = 9V USBIN Charger Detected 010 = Reserved 001 = 5V or 5V-9V USBIN Charger Detected
2:0	DCIN_INPUT_STS	Reserved

0x0000130E SMBCHGL_USB_USBID_VALID_ID_11_8

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_USB_USBID_VALID_ID_11_8

Bits	Name	Description
3:0	USBID_VALID_ID_11_8	

0x0000130F SMBCHGL_USB_USBID_VALID_ID_7_0

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_USB_USBID_VALID_ID_7_0

Bits	Name	Description
7:0	USBID_VALID_ID_7_0	

0x00001310 SMBCHGL_USB_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_USB_INT_RT_STS

Bits	Name	Description
6	USBID_CHANGE_INTR_RT_STS	The resistance attached to the USB_ID pin has changed by more than Xohms within the last 500ms (from Fuel Gauge)
5	AICL_DONE_RT_STS	AICL has completed, which means the adapter voltage has collapsed below the AICL threshold
4	IRQ_SPARE_STS	Reserved
3	QC_AUTHENTICATION_DONE_STS	Quick Charge Authentication Algorithm Done
2	USBIN_SRC_DET_STS_RT_STS	BC1.2 Automatic Power Source Detection (APSD) has completed
1	USBIN_OV_RT_STS	The USBIN voltage has crossed the over-voltage threshold
0	USBIN_UV_RT_STS	The USBIN voltage has crossed the under-voltage threshold

0x00001311 SMBCHGL_USB_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_USB_INT_SET_TYPE

Bits	Name	Description
6	USBID_CHANGE_INTR_TYPE	
5	AICL_DONE_TYPE	
4	IRQ_SPARE_TYPE	
3	QC_AUTHENTICATION_DONE_TYPE	
2	USBIN_SRC_DET_STS_TYPE	
1	USBIN_OV_TYPE	
0	USBIN_UV_TYPE	

0x00001312 SMBCHGL_USB_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_USB_INT_POLARITY_HIGH

Bits	Name	Description
6	USBID_CHANGE_INTR_HIGH	
5	AICL_DONE_HIGH	
4	IRQ_SPARE_HIGH	
3	QC_AUTHENTICATION_DONE_HIGH	
2	USBIN_SRC_DET_STS_HIGH	
1	USBIN_OV_HIGH	
0	USBIN_UV_HIGH	

0x00001313 SMBCHGL_USB_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_USB_INT_POLARITY_LOW

Bits	Name	Description
6	USBID_CHANGE_INTR_LOW	
5	AICL_DONE_LOW	
4	IRQ_SPARE_LOW	
3	QC_AUTHENTICATION_DONE_LOW	
2	USBIN_SRC_DET_STS_LOW	
1	USBIN_OV_LOW	
0	USBIN_UV_LOW	

0x00001314 SMBCHGL_USB_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_USB_INT_LATCHED_CLR

Bits	Name	Description
6	USBID_CHANGE_INTR_LATCHED_CLR	
5	AICL_DONE_LATCHED_CLR	
4	IRQ_SPARE_LATCHED_CLR	
3	QC_AUTHENTICATION_DONE_LATCHED_CLR	
2	USBIN_SRC_DET_STS_LATCHED_CLR	
1	USBIN_OV_LATCHED_CLR	
0	USBIN_UV_LATCHED_CLR	

0x00001315 SMBCHGL_USB_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

PMIC_SET_MASK

SMBCHGL_USB_INT_EN_SET

Bits	Name	Description
6	USBID_CHANGE_INTR_EN_SET	
5	AICL_DONE_EN_SET	
4	IRQ_SPARE_EN_SET	
3	QC_AUTHENTICATION_DONE_EN_SET	
2	USBIN_SRC_DET_STS_EN_SET	
1	USBIN_OV_EN_SET	

SMBCHGL_USB_INT_EN_SET (cont.)

Bits	Name	Description
0	USBIN_UV_EN_SET	

0x00001316 SMBCHGL_USB_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

PMIC_CLR_MASK=INT_EN_SET

SMBCHGL_USB_INT_EN_CLR

Bits	Name	Description
6	USBID_CHANGE_INTR_EN_CLR	
5	AICL_DONE_EN_CLR	
4	IRQ_SPARE_EN_CLR	
3	QC_AUTHENTICATION_DONE_EN_CLR	
2	USBIN_SRC_DET_STS_EN_CLR	
1	USBIN_OV_EN_CLR	
0	USBIN_UV_EN_CLR	

0x00001318 SMBCHGL_USB_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_USB_INT_LATCHED_STS

Bits	Name	Description
6	USBID_CHANGE_INTR_LATCHED_STS	The resistance attached to the USB_ID pin has changed by more than Xohms within the last 500ms (from Fuel Gauge)
5	AICL_DONE_LATCHED_STS	AICL has completed, which means the adapter voltage has collapsed below the AICL threshold

SMBCHGL_USB_INT_LATCHED_STS (cont.)

Bits	Name	Description
4	IRQ_SPARE_LATCHED_STS	Reserved
3	QC_AUTHENTICATION_DONE_LATCHED_STS	Quick Charge Authentication Algorithm Done
2	USBIN_SRC_DET_STS_LATCHED_STS	BC1.2 Automatic Power Source Detection (APSD) has completed
1	USBIN_OV_LATCHED_STS	The USBIN voltage has crossed the over-voltage threshold
0	USBIN_UV_LATCHED_STS	The USBIN voltage has crossed the under-voltage threshold

0x00001319 SMBCHGL_USB_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_USB_INT_PENDING_STS

Bits	Name	Description
6	USBID_CHANGE_INTR_PENDING_STS	
5	AICL_DONE_PENDING_STS	
4	IRQ_SPARE_PENDING_STS	
3	QC_AUTHENTICATION_DONE_PENDING_STS	
2	USBIN_SRC_DET_STS_PENDING_STS	
1	USBIN_OV_PENDING_STS	
0	USBIN_UV_PENDING_STS	

0x0000131A SMBCHGL_USB_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_USB_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	

0x0000131B SMBCHGL_USB_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_USB_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	

0x00001340 SMBCHGL_USB_CMD_IL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_USB_CMD_IL

Bits	Name	Description
6	SHDN_N_CLEAR_CMD	Reserved
5	BAT_2_SYS_FET_DIS	Battery-to-System FET Disable 0 = normal 1 = FET off
4	USBIN_SUSPEND	USBIN Suspend 0 = normal 1 = suspend
3	DCIN_SUSPEND	Reserved
2	ICL_OVERRIDE	ICL Override 0 = Use ICL from APSD 1 = Override APSD with Command Register
1	USB51_MODE	USB5/1 Mode 0 = USB 100mA/500mA mode (polarity from CFG[2] of USB peripheral) 1 = USB 500mA/100mA Mode (polarity from CFG[2] of USB peripheral)

SMBCHGL_USB_CMD_IL (cont.)

Bits	Name	Description
0	USBIN_MODE_CHG	USBIN Mode Charge 0 = USB5/1 or USB9/1.5 Current Levels 1 = HC Mode Current Level

0x00001341 SMBCHGL_USB_CMD_APSD

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_USB_CMD_APSD

Bits	Name	Description
0	APSD_RERUN	1 = Rerun APSD Algorithm (Self clearing)

0x000013F1 SMBCHGL_USB_USBIN_CHGR_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_USB_USBIN_CHGR_CFG

Bits	Name	Description
2	USBIN_5V_OV_SEL	0 - USBIN 5V Over Voltage Threshold = 6.4V 1 - USBIN 5V Over Voltage Threshold = 7.3V 0x0: USBIN_5V_OV_6P3 0x1: USBIN_5V_OV_7P4
1:0	ADAPTER_ALLOWANCE	USBIN Adapter Allowance 0x0: USBIN_ADAPTER_ALLOWANCE_5V 0x1: USBIN_ADAPTER_ALLOWANCE_5V_9V 0x2: USBIN_ADAPTER_ALLOWANCE_5V_TO_9V 0x3: USBIN_ADAPTER_ALLOWANCE_9V

0x000013F2 SMBCHGL_USB_USBIN_IL_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_USB_USBIN_IL_CFG

Bits	Name	Description
4:0	CURRENT_LIMIT	USBIN Input Current Limit 0x0: USBIN_IL_300MA 0x1: USBIN_IL_400MA 0x2: USBIN_IL_450MA 0x3: USBIN_IL_475MA 0x4: USBIN_IL_500MA 0x5: USBIN_IL_550MA 0x6: USBIN_IL_600MA 0x7: USBIN_IL_650MA 0x8: USBIN_IL_700MA 0x9: USBIN_IL_900MA 0xA: USBIN_IL_950MA 0xB: USBIN_IL_1000MA 0xC: USBIN_IL_1100MA 0xD: USBIN_IL_1200MA 0xE: USBIN_IL_1400MA 0xF: USBIN_IL_1450MA 0x10: USBIN_IL_1500MA 0x11: USBIN_IL_1600MA (only for PMI8940) 0x12: USBIN_IL_1800MA (only for PMI8940) 0x13: USBIN_IL_1850MA (only for PMI8940) 0x14: USBIN_IL_1880MA (only for PMI8940) 0x15: USBIN_IL_1910MA (only for PMI8940) 0x16: USBIN_IL_1930MA (only for PMI8940) 0x17: USBIN_IL_1950MA (only for PMI8940) 0x18: USBIN_IL_1970MA (only for PMI8940) 0x19: USBIN_IL_2000MA (only for PMI8940)

0x000013F3 SMBCHGL_USB_USB_AICL_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_USB_USB_AICL_CFG

Bits	Name	Description
6	OV_OPTION	0 = OV on DCIN will block USBIN current path, 1 = OV on DCIN will not block USBIN current path 0x0: USB_OV_BLOCK 0x1: USB_OV_NO_BLOCK
5	DEB_9V_ADAPTER_EN	Reserved
4	DEB_9V_ADAPTER_SEL	Reserved
3	DEB_5V_ADAPTER_SEL	USBIN Input Collapse Glitch Filter for 5V Select or 5V - 9V Adapter 0 = 5ms USBIN falling, 20ms USBIN rising, 1 = 15us USBIN falling, 20ms USBIN rising 0x0: USB_COLLAPSE_5VGF_5MS20MS 0x1: USB_COLLAPSE_5VGF_15US20MS
2	AICL	0 = Disabled, 1 = Enabled 0x0: USB_AICL_DISABLED 0x1: USB_AICL_ENABLED
1	DEB_HV_ADAPTER	Reserved
0	DEB_LV_ADAPTER	USBIN Input Collapse Option for LV adapter 0 = Input collapse does not turn off USBIN input FET, 1 = Input collapse turns off USBIN input FET 0x0: USB_COLLAPSE_LV_FET_ON 0x1: USB_COLLAPSE_LV_FET_OFF

0x000013F4 SMBCHGL_USB_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_USB_CFG

Bits	Name	Description
7	CFG_USB3P0_SEL	0 = sets USB 2.0 1 = sets USB 3.0 0x0: USB_2P0_SEL 0x1: USB_3P0_SEL

SMBCHGL_USB_CFG (cont.)

Bits	Name	Description
6	USBIN_SUSPEND_SRC	0 = BATID_UNKNOWN from FG does not prevent charging 1 = BATID_UNKNOWN from FG prevents charging 0x0: BATID_UNKNOWN_CHARGE 0x1: BATID_UNKNOWN_NO_CHARGE
5:4	HVDCP_ADAPTER_SEL	00 = 5V 01 = 9V 1X = Reserved 0x0: HVDCP_5V 0x1: HVDCP_9V
3	HVDCP_EN	0 = Disabled 1 = Enabled 0x0: HVDCP_DISABLE 0x1: HVDCP_ENABLE
2	USB51_COMMAND_POL	0 = Command 1: USB500, command 0: USB100 1 = Command 1: USB100, command 0: USB500 0x0: USB51AC_COMMAND1_500 0x1: USB51AC_COMMAND1_100
1	USB51AC_CTRL	0 = Command Register Controlled 1 = Pin Controlled 0x0: USB51_COMMAND_CONTROL 0x1: USB51_PIN_CONTROL
0	USB51AC_PIN_CTRL	0 = Tri-State Input 1 = Dual-State Input 0x0: USB51AC_TRISTATE 0x1: USB51AC_DUALSTATE

0x000013F5 SMBCHGL_USB_APSD_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_USB_APSD_CFG

Bits	Name	Description
7	INPUT_PRIORITY	Reserved

SMBCHGL_USB_APSD_CFG (cont.)

Bits	Name	Description
6	USB_FAIL_OPTION	0 = Normal 1 = Use Power-OK thresholds for HV adapter 0x0: USB_FAIL_NORMAL 0x1: USB_FAIL_POK_HV
5	OCD_ISEL	0 = ICL 500mA 1 = ICL HC 0x0: OCD_ISEL_500 0x1: OCD_ISEL_HC
4	SDP_SUSPEND	0 = Normal SDP operation 1 = SDP enters suspend 0x0: SDP_NORMAL 0x1: SDP_SUSPEND
3	VBATT_LOW_SDP	0 = VBATT_LOW during SDP has no effect 1 = VBATT_LOW during SDP forces 500ma ICL 0x0: VBATT_SDP_NORMAL 0x1: VBATT_SDP_500MA
2	RID_CLK_SEL	0 = RID State Machine Frequency 1kHz 1 = RID State Machine Frequency 2kHz 0x0: RID_1KHZ 0x1: RID_2KHZ
1	DCD_OPTION	0 = DCD Option - Deglitchers and Timeout 1 = DCD Option - Timeout only 0x0: DCD_DG_TMOUT 0x1: DCD_TMOUT
0	AUTO_SRC_DETECT	0 = Disabled 1 = Enabled 0x0: AUTO_SRC_DETECT_DIS 0x1: AUTO_SRC_DETECT_EN

0x000013FC SMBCHGL_USB_NEAL6

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_USB_NEAL6

Bits	Name	Description
7	SCHGP_OPTION4	Disable batt FET gate pre-bias to battery voltage which helps improve Vbatt tracking to full-on transition. Otherwise, gate voltage starts at ground
6	SCHGP_OPTION3	Reserved
5	SCHGP_OPTION2	Enable OTG startup reset. This was unnecessary left-over circuitry
4	SCHGP_OPTION1	Increase OTG OC by 40%
3	FG_LP_OSC_OPTION_BIT	0 = SYS_CLK is STANDBY_OSC only 1 = SYS_CLK can be either STANDBY_OSC or PWM_OSC
2	EN_IIN_OPT	0 = EN_IIN_BUF controlled by INPUT_SS_DONE 1 = EN_IIN_BUF controlled by EN_SYSON_LDO 0x0: EN_IIN_BUF_SS_DONE 0x1: EN_IIN_BUF_SYSON_LDO
1	OC_OPT	0 = VSYS Short Detection Disabled 1 = VSYS Short Detection Enabled 0x0: VSYS_SHORT_DIS 0x1: VSYS_SHORT_EN
0	SYSON_OPT	0 = SYSON LDO Enable Default 1 = SYSON LDO Enable on INPUT FET ON Enable 0x0: SYSON_LDO_DEFAULT 0x1: SYSON_LDO_INPUT_FET_ON

13 SMBCHGL_DC_SMBCHGL_DC

0x00001404 SMBCHGL_DC_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: NA

PMIC_CONSTANT

SMBCHGL_DC_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	

0x00001405 SMBCHGL_DC_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x55

Reset Name: NA

PMIC_CONSTANT

SMBCHGL_DC_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	

0x000014F6 SMBCHGL_DC_TEMP_COMP_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

Temperature Compensation Configuration

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_DC_TEMP_COMP_CFG

Bits	Name	Description
6	CFG_EN_TLOOP	0 = Enable System Regulation Fix that removes Vsys_max 1 = Disable System Regulation Fix that removes Vsys_max
5	CFG_DIS_TLOOP	Reserved
4	CFG_DIS_DIG_TLOOP	Disable temp sensor output to HK ADC 0 = Enable temp sensor output 1 = Disable temp sensor output
3	INT_TEMP_COMP_EN	Internal Temperature Compensation Enable 0 = Disabled 1 = Enable 0x0: INT_TEMP_COMP_EN_DIS 0x1: INT_TEMP_COMP_EN_EN
2	INT_TEMP_COMP_SETTIN G	Internal Temperature Compensation Setting 0 = Alert level brings current limit setting to 0000b 1 = Alert level brings current limit setting to less than 15% of programmed setting 0x0: INT_TEMP_COMP_SETTING_0 0x1: INT_TEMP_COMP_SETTING_15PCT
1:0	INT_TEMP_COMP_CYCLE_ TIME	Internal Temperature Compensation Cycle Time 00 = 350ms 01 = 700ms 10 = 1.4s 11 = 2.8s 0x0: AINT_TEMP_COMP_CYCLE_TIME_350MS 0x1: INT_TEMP_COMP_CYCLE_TIME_700MS 0x2: INT_TEMP_COMP_CYCLE_TIME_31P4S 0x3: INT_TEMP_COMP_CYCLE_TIME_2P8S

0x000014F9 SMBCHGL_DC_TRIM9

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_DC_TRIM9

Bits	Name	Description
7:4	TR_DUTY	TR_DUTY<3> When = 1: Enables open drain option for SYSOK pin TR_DUTY<2> When =1: Enables shoot through protection circuit of the power stage. Default preference = 1 TR_DUTY<1> When = 1: Reduces dead time for the Low side drive signal. Default preference = 1 TR_DUTY<0> When = 1: one shot BST refresh
3:2	TR_ZDTR	TR_ZDTR - Zero Cross Detect Trim
1:0	TR_BLTR	TR_BLTR<1:0> Lower two bits for trim blanking time in oscillator block

0x000014FB SMBCHGL_DC_TRIM11

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_DC_TRIM11

Bits	Name	Description
4	TR_HICAP_VMODE	Reserved
3	TR_SOFT	Program soft-limit threshold (point where charge current reduction took place). 0 = charge current reduction threshold=VSYS-75mV 1 = charge current reduction threshold=VSYS-150mV,this option should not be used when VSYS tracking VBAT by 100mv is set
2	TR_BT	0 = set VSYS tracking VBATT by 100mV 1= set VSYS tracking VBATT by 150mV
1	TR_DIS_SSUD	TR_DIS_SSUD = 1: Disables charger current soft start

SMBCHGL_DC_TRIM11 (cont.)

Bits	Name	Description
0	TR_NEW_TRIM	Reserved

14 SMBCHGL_MISC_SMBCHGL_MISC

0x00001600 SMBCHGL_MISC_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: NA

HW Version Register [7:0]

PMIC_CONSTANT

SMBCHGL_MISC_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x00001601 SMBCHGL_MISC_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: NA

HW Version Register [15:8]

PMIC_CONSTANT

SMBCHGL_MISC_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x00001602 SMBCHGL_MISC_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: NA

HW Version Register [23:16]

SMBCHGL_MISC_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x00001603 SMBCHGL_MISC_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: NA

HW Version Register [31:24]

SMBCHGL_MISC_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x00001604 SMBCHGL_MISC_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: NA

Peripheral Type

PMIC_CONSTANT

SMBCHGL_MISC_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	Charger

0x00001605 SMBCHGL_MISC_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x57

Reset Name: NA

Peripheral SubType

PMIC_CONSTANT

SMBCHGL_MISC_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	SMBCHGL_MISC

0x00001608 SMBCHGL_MISC_IDEV_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_MISC_IDEV_STS

Bits	Name	Description
7:0	SRC_DETECT_STS	Source detected 1XXX XXXX = Charging Downstream Port X1XX XXXX = Dedicated Charging Port XX1X XXXX = Other Charging Port XXX1 XXXX = Standard Downstream Port XXXX 1XXX = FMB UART ON XXXX X1XX = FMB UART OFF XXXX XX1X = FMB USB ON XXXX XXX1 = FMB USB OFF

0x00001610 SMBCHGL_MISC_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_MISC_INT_RT_STS

Bits	Name	Description
5	OTST3_RT_STS	does not exist anymore
4	OTST2_RT_STS	indicates when the internal die temperature has crossed 100C, 110C, 120C, or 130C
3	FLASH_FAIL_RT_STS	Flash was running, but disabled due to some event
2	WDOG_TIMER_RT_STS	indicates when the watchdog timer has expired
1	TEMP_SHUTDOWN_RT_STS	OTST1_RT_STS - indicates when the internal die temperature has crossed 90C or 100C
0	POWER_OK_RT_STS	indicates when the input power is valid, such that the charger buck has enabled

0x00001611 SMBCHGL_MISC_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_MISC_INT_SET_TYPE

Bits	Name	Description
5	OTST3_TYPE	
4	OTST2_TYPE	
3	FLASH_FAIL_TYPE	
2	WDOG_TIMER_TYPE	
1	TEMP_SHUTDOWN_TYPE	OTST1_TYPE
0	POWER_OK_TYPE	

0x00001612 SMBCHGL_MISC_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_MISC_INT_POLARITY_HIGH

Bits	Name	Description
5	OTST3_HIGH	
4	OTST2_HIGH	
3	FLASH_FAIL_HIGH	
2	WDOG_TIMER_HIGH	
1	TEMP_SHUTDOWN_HIGH	OTST1_HIGH
0	POWER_OK_HIGH	

0x00001613 SMBCHGL_MISC_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_MISC_INT_POLARITY_LOW

Bits	Name	Description
5	OTST3_LOW	
4	OTST2_LOW	
3	FLASH_FAIL_LOW	
2	WDOG_TIMER_LOW	
1	TEMP_SHUTDOWN_LOW	OTST1_LOW
0	POWER_OK_LOW	

0x00001614 SMBCHGL_MISC_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_MISC_INT_LATCHED_CLR

Bits	Name	Description
5	OTST3_LATCHED_CLR	
4	OTST2_LATCHED_CLR	
3	FLASH_FAIL_LATCHED_CLR	
2	WDOG_TIMER_LATCHED_CLR	
1	TEMP_SHUTDOWN_LATCHED_CLR	OTST1_LATCHED_CLR
0	POWER_OK_LATCHED_CLR	

0x00001615 SMBCHGL_MISC_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

PMIC_SET_MASK

SMBCHGL_MISC_INT_EN_SET

Bits	Name	Description
5	OTST3_EN_SET	
4	OTST2_EN_SET	
3	FLASH_FAIL_EN_SET	
2	WDOG_TIMER_EN_SET	
1	TEMP_SHUTDOWN_EN_SET	OTST1_EN_SET
0	POWER_OK_EN_SET	

0x00001616 SMBCHGL_MISC_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

PMIC_CLR_MASK=INT_EN_SET

SMBCHGL_MISC_INT_EN_CLR

Bits	Name	Description
5	OTST3_EN_CLR	
4	OTST2_EN_CLR	
3	FLASH_FAIL_EN_CLR	
2	WDOG_TIMER_EN_CLR	
1	TEMP_SHUTDOWN_EN_CLR	OTST1_EN_CLR
0	POWER_OK_EN_CLR	

0x00001618 SMBCHGL_MISC_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_MISC_INT_LATCHED_STS

Bits	Name	Description
5	OTST3_LATCHED_STS	does not exist anymore
4	OTST2_LATCHED_STS	indicates when the internal die temperature has crossed 100C, 110C, 120C, or 130C
3	FLASH_FAIL_LATCHED_STS	Flash was running, but disabled due to some event
2	WDOG_TIMER_LATCHED_STS	indicates when the watchdog timer has expired
1	TEMP_SHUTDOWN_LATCHED_STS	OTST1_LATCHED_STS - indicates when the internal die temperature has crossed 90C or 100C
0	POWER_OK_LATCHED_STS	indicates when the input power is valid, such that the charger buck has enabled

0x00001619 SMBCHGL_MISC_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

SMBCHGL_MISC_INT_PENDING_STS

Bits	Name	Description
5	OTST3_PENDING_STS	
4	OTST2_PENDING_STS	
3	FLASH_FAIL_PENDING_STS	
2	WDOG_TIMER_PENDING_STS	
1	TEMP_SHUTDOWN_PENDING_STS	
0	POWER_OK_PENDING_STS	

0x0000161A SMBCHGL_MISC_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_MISC_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	

0x0000161B SMBCHGL_MISC_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_MISC_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	

0x00001640 SMBCHGL_MISC_WDOG_RST

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_MISC_WDOG_RST

Bits	Name	Description
7	WDOG_RST	

0x00001641 SMBCHGL_MISC_AFP_MODE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x80

Reset Name: afp_mode_rb

SMBCHGL_MISC_AFP_MODE

Bits	Name	Description
7	AFP_MODE_ENB	

0x00001642 SMBCHGL_MISC_GSM_PA_ON_ADJ_EN

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SMBCHGL_MISC_GSM_PA_ON_ADJ_EN

Bits	Name	Description
7	GSM_PA_ON_ADJ_EN	

0x000016F1 SMBCHGL_MISC_WD_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_MISC_WD_CFG

Bits	Name	Description
7	AFP_WDOG_ENABLE	Watchdog Starts AFP 0 = Disabled 1 = Enabled 0x0: AFP_WDOG_DIS 0x1: AFP_WDOG_EN
6:5	WDOG_TIMEOUT	Watchdog Timeout 00 = 18s 01 = 36s 1X = 72s 0x0: WDOG_TMOUT_18S 0x1: WDOG_TMOUT_36S 0x2: WDOG_TMOUT_72S
4:3	SFT_AFTER_WDOG_IRQ	Safety Timer after Watchdog IRQ 00= 12min 01 = 24min 10 = 48min 11 = 96min 0x0: TIMER_AFTER_WDOG_12MIN 0x1: TIMER_AFTER_WDOG_24MIN 0x2: TIMER_AFTER_WDOG_48MIN 0x3: TIMER_AFTER_WDOG_96MIN
2	WDOG_IRQ_SFT	Watchdog IRQ Safety Timer 0 = Disabled 1 = Enabled 0x0: WDOG_IRQ_TIMER_DIS 0x1: WDOG_IRQ_TIMER_EN
1	WDOG_OPTION	Watchdog Option 0 = Run after ACK after reload 1 = Run always 0x0: WDOG_AFTER_ACK 0x1: WDOG_ALWAYS
0	WDOG_TIMER_EN	Watchdog Timer 0 = Disabled 1 = Enabled 0x0: WDOG_DIS 0x1: WDOG_EN

0x000016F2 SMBCHGL_MISC_MISC_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_MISC_MISC_CFG

Bits	Name	Description
7	MISC_CFG_7	Reserved
6	WIPWR_UVLO_IRQ_OPT	Reserved
5	CFG_NTCVOUT	Reserved
4	PMUX_OTG_DLY_EN	Reserved
3	CHG_OK	Reserved
2	MISC_CFG_2	Reserved
1	GSM_PA_ON_ADJ_SEL	PA_ON Software Function 0 = Disabled 1 = Enabled 0x0: PA_ON_DIS 0x1: PA_ON_EN
0	MISC_CFG_0	Reserved

0x000016F5 SMBCHGL_MISC_CHGR_TRIM_OPTIONS_15_8

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_MISC_CHGR_TRIM_OPTIONS_15_8

Bits	Name	Description
7	AICL_INIT	AICL Initial value 0 = AICL is 0 1 = AICL is ICL 0x0: AICL_INITIAL_0 0x1: AICL_INITIAL_ICL

SMBCHGL_MISC_CHGR_TRIM_OPTIONS_15_8 (cont.)

Bits	Name	Description
6	AICL_ADC	AICL ADC Function 0 = Disabled 1 = Enabled 0x0: AICL_ADC_DIS 0x1: AICL_ADC_EN
5	USBIN_RERUN_AICL	USB Rerun for AICL 0 = Disabled 1 = Enabled 0x0: AICL_USB_RERUN_DIS 0x1: AICL_USB_RERUN_EN
4	DCIN_RERUN_AICL	Reserved
3	SYSOK_DCIN_SEL	SYSOK B/C Select 0 = SYSOK B 1 = SYSOK C 0x0: SYSOK_OPT_B 0x1: SYSOK_OPT_C
2	PRE_BYPASS_GF_TBIT	Pre Bypass GF TBIT 0 = Disabled 1 = Enabled 0x0: BYPASS_GF_DIS 0x1: BYPASS_GF_EN
1	STANDBY_OSC_EN	Standby oscillator enable 0 = Disabled 1 = Enabled 0x0: STDBY_OSC_OVERRIDE_DIS 0x1: STDBY_OSC_OVERRIDE_EN
0	MAIN_OSC_EN	Main oscillator enable 0 = Disabled 1 = Enabled 0x0: MAIN_OSC_OVERRIDE_DIS 0x1: MAIN_OSC_OVERRIDE_EN

0x000016F6 SMBCHGL_MISC_CHGR_TRIM_OPTIONS_7_0

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_MISC_CHGR_TRIM_OPTIONS_7_0

Bits	Name	Description
7	ESR_DURING_TAPER	0 = Enable ESR adjustment during Taper 1 = Disable ESR adjustment during Taper 0x0: TAPER_ESR_EN 0x1: TAPER_ESR_DIS
6	TLIM_DIS_TBIT	0 = TLIM Enabled (default) 1 = Disabled 0x0: TLIM_EN 0x1: TLIM_DIS
5:4	OV_OPTION_TBIT	Over Voltage Option 1 0X = Reserved 1X = Reserved X0 = OV on opposite channel causes load on channel MID (default) X1 = OV on opposite channel does not causes load on channel MID 0x0: OV_OPT_MID_LOAD 0x1: OV_OPT_NO_MID_LOAD
3	TBIT_IMP_EN	Input Missing Poller 0 = Disabled 1 = Enabled (default) 0x0: INPUT_MISSING_POLLER_DIS 0x1: INPUT_MISSING_POLLER_EN
2	TRIM_OPT_2	Reserved
1	DIS_ARB_FIX_TBIT	DIS_ARB_FIX_TBIT 0 = Arbitration threshold for battery raised if input > UV (default) 1 = Arbitration can select battery even if input is > UV 0x0: RAISE_ARB_THRESHOLD 0x1: ARB_THRESHOLD_SEL
0	DB_TMR_DIS_TBIT	Dead Battery Timer 0 = Enabled (default) 1 = Disabled 0x0: DEAD_BATT_TIMER_EN 0x1: DEAD_BATT_TIMER_DIS

0x000016FF SMBCHGL_MISC_CFG_TEMP_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_MISC_CFG_TEMP_SEL

Bits	Name	Description
1:0	CFG_TEMP_SEL	selects temperature for both analog and digital thermal loops 00 = 100 degrees 01 = 110 degrees 10 = 120 degrees 11 = 130 degrees 0x0: TEMP_LOOP_100DEG 0x1: TEMP_LOOP_110DEG 0x2: TEMP_LOOP_120DEG 0x3: TEMP_LOOP_130DEG

0x000014F4 SMBCHGL_DC_DC_AICL_CFG2

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_DC_DC_AICL_CFG2

Bits	Name	Description
2	DEB_UV	0 = 20ms DCIN falling, 20ms DCIN rising, 1 = 10us DCIN falling, 10ms DCIN rising 0x0: DC_UV_GF_20MS20MS 0x1: DC_UV_GF_10US10MS
1	AICL_THRESHOLD_5V_TO_9V	0 = 6.25v (VBL_SEL_CFG[1]=0), 4.25v (VBL_SEL_CFG[1]=1) 1 = 6.75v (VBL_SEL_CFG[1]=0), 4.40v (VBL_SEL_CFG[1] =1) 0x0: DC_AICL_6P25_OR_4P25 0x1: DC_AICL_6P75_OR_4P40
0	AICL_THRESHOLD_5V	DCIN 5V AICL Threshold 0 = 4.25V 1 = 4.67V 0x0: DC_AICL_5V_4P25 0x1: DC_AICL_5V_4P67

0x000014F5 SMBCHGL_DC_AICL_WL_SEL_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

SMBCHGL_DC_AICL_WL_SEL_CFG

Bits	Name	Description
2:0	AICL_RESTART_TIMER	000 = 2.8s 001 = 5.6s 010 = 11.3s 011 = 22.5s 100 = 45s 101 = 1.5min 110 = 3min 111 = 6min 0x0: AICL_RESTART_TIMER_2P8S 0x1: AICL_RESTART_TIMER_5P6S 0x2: AICL_RESTART_TIMER_11P3S 0x3: AICL_RESTART_TIMER_22P5S 0x4: AICL_RESTART_TIMER_45S 0x5: AICL_RESTART_TIMER_1P5MIN 0x6: AICL_RESTART_TIMER_3MIN 0x7: AICL_RESTART_TIMER_6MIN

15 BSI_BSI

0x00001B00 BSI_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: NA

HW Version Register [7:0]

PMIC_CONSTANT

BSI_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x00001B01 BSI_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: NA

HW Version Register [15:8]

PMIC_CONSTANT

BSI_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software. 1 - Digital change related to fg_bsi_tx_disable is not SW backwards compatible.

0x00001B02 BSI_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: NA

HW Version Register [23:16]

BSI_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00001B03 BSI_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: NA

HW Version Register [31:24]

BSI_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software. 1 - New signal fg_bsi_tx_disable from analog is not SW backward compatible.

0x00001B04 BSI_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: NA

Peripheral Type

PMIC_CONSTANT

BSI_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	CHARGER 0x2: CHARGER

0x00001B05 BSI_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x11

Reset Name: NA

Peripheral SubType

PMIC_CONSTANT

BSI_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	BSI_MIPI_BIF 0x10: BSI 0x11: BSI_MIPI_BIF

0x00001B08 BSI_BSI_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

BSI real time status

BSI_BSI_STS

Bits	Name	Description
7	BSI_ACTIVE	clock request. 0x1: BSI_ACTIVE 0x0: BSI_NOT_ACTIVE
6	BSI_TX_DISABLE	TX disable signal from analog circuit. 1: BSI shall finish any existing ongoing TX then stop. 0: BSI can start or resume TX transactions. 0x1: TX_DISABLED 0x0: TX_ENABLED
4	MIPI_BIF_ERR_FLAG	0: BIF does not encounter an error. 1: BIF encounters the first error. a) TX and RX are frozen immediately on error. b)rx_data and error code are latched on error. c) SW needs to write to MIPI_BIF_CLEAR_ERR reg to clear the err and start a new TX or RX transaction. 0x1: ERROR 0x0: OK
3	MIPI_BIF_TX_BUSY	1: Transmitter is busy transmitting data or pulse. TX_FSM is at TX_PUL or TX_BAT_IRQ or TX_DATA_STATE or TX_STOP state. 0: Transmitter is not actively transmitting data or pulse. TX_FSM is at TX_IDLE or TX_WAIT_CLR_ERR state. 0x1: TX_BUSY 0x0: TX_IDLE
2	MIPI_BIF_RX_BUSY	1: Receiver is busy receiving data or battery initiated interrupt. RX_FSM is at RX_BCF or RX_NOT_BCF or RX_DATA_STATE or RX_STOP or RX_BAT_IRQ states. 0: Receiver is not actively receiving data or battery initiated interrupt. RX_FSM is at RX_IDLE or RX_WAIT_CLR_ERR state. 0x1: RX_BUSY 0x0: RX_IDLE
1	MIPI_BIF_TX_GO_STATUS	TX flow control status bit. 0: HW is transmitting the programmed transaction. SW can program the next TX transaction 1: HW has not started transmitting the programmed transaction. SW can't programing the next TX transaction 0x1: TX_GO_SET 0x0: TX_GO_CLEAR

BSI_BSI_STS (cont.)

Bits	Name	Description
0	MIPI_BIF_RX_FLOW_STATUS	If FIFO is enabled: 0: RX battery data are not available in RX FIFO. 1: RX battery data are available in RX FIFO. If FIFO is disabled: 0: No RX battery data available in MIPI_BIF_DATA_RX_* registers for SW to fetch. 1: RX battery data available in MIPI_BIF_DATA_RX_* registers for SW to fetch. 0x1: RX_DATA_AVAIL 0x0: NO_RX_DATA

0x00001B0A BSI_RX_FIFO_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

BSI_RX_FIFO_STS

Bits	Name	Description
3:0	WORD_NUM	Available burst read word number for SW to fetch

0x00001B0D BSI_BSI_BAT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

BSI battery real time status

BSI_BSI_BAT_STS

Bits	Name	Description
3	BAT_MISS_DEB	Input from analog: batt_miss_deb 0x1: BATT_GONE 0x0: BATT_PRESENT
2	BAT_MISS_RAW	Input from analog: batt_miss_raw 0x1: BATT_GONE 0x0: BATT_PRESENT

BSI_BSI_BAT_STS (cont.)

Bits	Name	Description
1	BAT_DEB_PRES_STATUS	Battery presence/removal detection starts only after BSI is enabled (BSI_EN = 1). There can be an uncertainty time before the initial battery presence status is detected. 0: Battery is present after programmed debounce time 1: Battery is removed after programmed debounce time 0x1: BATT_GONE 0x0: BATT_PRESENT
0	BAT_NODEB_PRES_STATUS	Battery presence/removal detection starts only after BSI is enabled (BSI_EN = 1). There can be an uncertainty time before the initial battery presence status is detected. 0: Battery is present without debounce 1: Battery is removed without debounce 0x1: BATT_GONE 0x0: BATT_PRESENT

0x00001B10 BSI_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Interrupt Real Time Status Bits

BSI_INT_RT_STS

Bits	Name	Description
5	DEB_BAT_PRES_RT_STS	Edge sensitive interrupt 0: debounced battery presence based on SW selected battery missing input 1: debounced battery removal based on SW selected battery missing input 0x1: INT_RT_STATUS_HIGH 0x0: INT_RT_STATUS_LOW
4	NODEB_BAT_PRES_RT_STS	Edge sensitive interrupt 0: non debounced raw battery presence 1: non debounced raw battery removal 0x1: INT_RT_STATUS_HIGH 0x0: INT_RT_STATUS_LOW

BSI_INT_RT_STS (cont.)

Bits	Name	Description
3	TX_DISABLE_RT_STS	Edge sensitive interrupt from analog circuit 0: BSI TX is normal 1: BSI TX activity halted (rising edge) or BSI Tx activity resumed (falling edge) 0x1: INT_RT_STATUS_HIGH 0x0: INT_RT_STATUS_LOW
2	MIPI_BIF_TX_INT_RT_STS	1: A TX transaction completes without error 0x1: INT_RT_STATUS_HIGH 0x0: INT_RT_STATUS_LOW
1	MIPI_BIF_RX_INT_RT_STS	1: A battery initiated RX transaction completes without error 0x1: INT_RT_STATUS_HIGH 0x0: INT_RT_STATUS_LOW
0	MIPI_BIF_ERR_INT_RT_STS	1: Error happened during either a TX or RX transaction. Fetch MIPI_BIF_ERR for details 0x1: INT_RT_STATUS_HIGH 0x0: INT_RT_STATUS_LOW

0x00001B11 BSI_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

0 = use level trigger interrupts, 1 = use edge trigger interrupts

BSI_INT_SET_TYPE

Bits	Name	Description
5	DEB_BAT_PRES_SET_TYPE	Edge sensitive interrupt 0: debounced battery presence based on SW selected battery missing input 1: debounced battery removal based on SW selected battery missing input 0x0: LEVEL 0x1: EDGE
4	NODEB_BAT_PRES_SET_TYPE	Edge sensitive interrupt 0: non debounced raw battery presence 1: non debounced raw battery removal 0x0: LEVEL 0x1: EDGE

BSI_INT_SET_TYPE (cont.)

Bits	Name	Description
3	TX_DISABLE_SET_TYPE	Edge sensitive interrupt from analog circuit 0: BSI TX is normal 1: BSI TX activity halted (rising edge) or BSI Tx activity resumed (falling edge) 0x0: LEVEL 0x1: EDGE
2	MIPI_BIF_TX_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
1	MIPI_BIF_RX_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
0	MIPI_BIF_ERR_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE

0x00001B12 BSI_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

BSI_INT_POLARITY_HIGH

Bits	Name	Description
5	DEB_BAT_PRES_POLARITY_HIGH	Edge sensitive interrupt 0: debounced battery presence based on SW selected battery missing input 1: debounced battery removal based on SW selected battery missing input 0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
4	NODEB_BAT_PRES_POLARITY_HIGH	Edge sensitive interrupt 0: non debounced raw battery presence 1: non debounced raw battery removal 0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
3	TX_DISABLE_POLARITY_HIGH	Edge sensitive interrupt from analog circuit 0: BSI TX is normal 1: BSI TX activity halted (rising edge) or BSI Tx activity resumed (falling edge) 0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

BSI_INT_POLARITY_HIGH (cont.)

Bits	Name	Description
2	MIPI_BIF_TX_INT_POLARITY_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
1	MIPI_BIF_RX_INT_POLARITY_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
0	MIPI_BIF_ERR_INT_POLARITY_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x00001B13 BSI_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

BSI_INT_POLARITY_LOW

Bits	Name	Description
5	DEB_BAT_PRES_POLARITY_LOW	Edge sensitive interrupt 0: debounced battery presence based on SW selected battery missing input 1: debounced battery removal based on SW selected battery missing input 0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
4	NODEB_BAT_PRES_POLARITY_LOW	Edge sensitive interrupt 0: non debounced raw battery presence 1: non debounced raw battery removal 0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
3	TX_DISABLE_POLARITY_LOW	Edge sensitive interrupt from analog circuit 0: BSI TX is normal 1: BSI TX activity halted (rising edge) or BSI Tx activity resumed (falling edge) 0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
2	MIPI_BIF_TX_INT_POLARITY_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
1	MIPI_BIF_RX_INT_POLARITY_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

BSI_INT_POLARITY_LOW (cont.)

Bits	Name	Description
0	MIPI_BIF_ERR_INT_POLARITY_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x00001B14 BSI_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

BSI_INT_LATCHED_CLR

Bits	Name	Description
5	DEB_BAT_PRES_LATCHED_CLR	Edge sensitive interrupt 0: debounced battery presence based on SW selected battery missing input 1: debounced battery removal based on SW selected battery missing input
4	NODEB_BAT_PRES_LATCHED_CLR	Edge sensitive interrupt 0: non debounced raw battery presence 1: non debounced raw battery removal
3	TX_DISABLE_LATCHED_CLR	Edge sensitive interrupt from analog circuit 0: BSI TX is normal 1: BSI TX activity halted (rising edge) or BSI Tx activity resumed (falling edge)
2	MIPI_BIF_TX_INT_LATCHED_CLR	
1	MIPI_BIF_RX_INT_LATCHED_CLR	
0	MIPI_BIF_ERR_INT_LATCHED_CLR	

0x00001B15 BSI_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

BSI_INT_EN_SET

Bits	Name	Description
5	DEB_BAT_PRES_EN_SET	Edge sensitive interrupt 0: debounced battery presence based on SW selected battery missing input 1: debounced battery removal based on SW selected battery missing input 0x0: INT_DISABLED 0x1: INT_ENABLED
4	NODEB_BAT_PRES_EN_SET	Edge sensitive interrupt 0: non debounced raw battery presence 1: non debounced raw battery removal 0x0: INT_DISABLED 0x1: INT_ENABLED
3	TX_DISABLE_EN_SET	Edge sensitive interrupt from analog circuit 0: BSI TX is normal 1: BSI TX activity halted (rising edge) or BSI Tx activity resumed (falling edge) 0x0: INT_DISABLED 0x1: INT_ENABLED
2	MIPI_BIF_TX_INT_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
1	MIPI_BIF_RX_INT_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
0	MIPI_BIF_ERR_INT_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED

0x00001B16 BSI_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

BSI_INT_EN_CLR

Bits	Name	Description
5	DEB_BAT_PRES_EN_CLR	Edge sensitive interrupt 0: debounced battery presence based on SW selected battery missing input 1: debounced battery removal based on SW selected battery missing input 0x0: INT_DISABLED 0x1: INT_ENABLED
4	NODEB_BAT_PRES_EN_CLR	Edge sensitive interrupt 0: non debounced raw battery presence 1: non debounced raw battery removal 0x0: INT_DISABLED 0x1: INT_ENABLED
3	TX_DISABLE_EN_CLR	Edge sensitive interrupt from analog circuit 0: BSI TX is normal 1: BSI TX activity halted (rising edge) or BSI Tx activity resumed (falling edge) 0x0: INT_DISABLED 0x1: INT_ENABLED
2	MIPI_BIF_TX_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
1	MIPI_BIF_RX_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
0	MIPI_BIF_ERR_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

0x00001B18 BSI_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

BSI_INT_LATCHED_STS

Bits	Name	Description
5	DEB_BAT_PRES_LATCHED_STS	Edge sensitive interrupt 0: debounced battery presence based on SW selected battery missing input 1: debounced battery removal based on SW selected battery missing input 0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
4	NODEB_BAT_PRES_LATCHED_STS	Edge sensitive interrupt 0: non debounced raw battery presence 1: non debounced raw battery removal 0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
3	TX_DISABLE_LATCHED_STS	Edge sensitive interrupt from analog circuit 0: BSI TX is normal 1: BSI TX activity halted (rising edge) or BSI Tx activity resumed (falling edge) 0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
2	MIPI_BIF_TX_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
1	MIPI_BIF_RX_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
0	MIPI_BIF_ERR_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

0x00001B19 BSI_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Debug: Pending is set if interrupt has been sent but not cleared.

BSI_INT_PENDING_STS

Bits	Name	Description
5	DEB_BAT_PRES_PENDING_STS	Edge sensitive interrupt 0: debounced battery presence based on SW selected battery missing input 1: debounced battery removal based on SW selected battery missing input 0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
4	NODEB_BAT_PRES_PENDING_STS	Edge sensitive interrupt 0: non debounced raw battery presence 1: non debounced raw battery removal 0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
3	TX_DISABLE_PENDING_STS	Edge sensitive interrupt from analog circuit 0: BSI TX is normal 1: BSI TX activity halted (rising edge) or BSI Tx activity resumed (falling edge) 0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
2	MIPI_BIF_TX_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
1	MIPI_BIF_RX_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
0	MIPI_BIF_ERR_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

0x00001B1A BSI_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Selects the MID that will receive the interrupt

BSI_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x00001B1B BSI_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SR=0 A=1

BSI_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR 0x1: A

0x00001B46 BSI_BSI_EN

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

BSI Enable/Disable

BSI_BSI_EN

Bits	Name	Description
7	BSI_EN	0: BIF is disabled. a) SW should checks all transactions completed before disable BSI. b) BIF does not detect battery slave initiated interrupts when BSI is disabled. 1: BSI is enabled. a) SW enables BSI before starting any transactions. 0x0: BSI_DISABLED 0x1: BSI_ENABLED

0x00001B4F BSI_MIPI_BIF_ERR_CLEAR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

A pulse is generated when SW writes 1 to the register bit.

BSI_MIPI_BIF_ERR_CLEAR

Bits	Name	Description
7	MIPI_BIF_CLEAR_ERR	Write 1 to the register bit clears BIF error code and BIF Rx data and defreeze TX and RX FSM for new transactions.

0x00001B51 BSI_MIPI_BIF_FORCE_BCL_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

MIPI BIF Hard Reset

BSI_MIPI_BIF_FORCE_BCL_LOW

Bits	Name	Description
7	MIPI_BIF_FORCE_BCL_LOW	0: Releases BCL 1: Force BCL low. 0x0: BCL_RELEASED 0x1: BCL_FORCED_LOW

0x00001B52 BSI_MIPI_BIF_TAU_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

MIPI BIF Clock Enables Configuration

BSI_MIPI_BIF_TAU_CFG

Bits	Name	Description
4	MIPI_BIF_SAMPLE_RATE	Sample rate used to measure Time Distance Coding pulse width after edge detection 0: 4X sample rate. 1: 8X sample rate. 0x0: SAMPLE_RATE_4X 0x1: SAMPLE_RATE_8X

BSI_MIPI_BIF_TAU_CFG (cont.)

Bits	Name	Description
2:0	MIPI_BIF_SEL_TAU	Tau programming: 000 150.42us (4x); 150.42us(8x) 001 122.08us (4x); 122.08us(8x) 010 61.04us (4x); 63.33 us(8x) 011 31.67us (4x); 31.67us(8x) 100 15.83us (4x); 15.83us(8x) 101 7.92us(4x); 7.92us(8x) 110 3.96us(4x); 4.17us(8x) 111 2.08us(4x); 2.08us(8x) 0x0: TAU_150US 0x1: TAU_122US 0x2: TAU_62US 0x3: TAU_32US 0x4: TAU_16US 0x5: TAU_8US 0x6: TAU_4US 0x7: TAU_2US

0x00001B53 BSI_MIPI_BIF_MODE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

MIPI BIF Modes Configuration

BSI_MIPI_BIF_MODE

Bits	Name	Description
4	MIPI_BIF_TX_PULSE_MODE	Data/Pulse transmission 0: MIPI BIF transmits data. 1: MIPI BIF transmits INT or PUL pulses. 0x0: TX_DATA_MODE 0x1: TX_PULSE_MODE
3	MIPI_BIF_RX_PULSE_MODE	Data/Interrupt receiving 0: MIPI BIF receives data from BCL. 1: MIPI BIF detects interrupt from battery slave. 0x0: RX_DATA_MODE 0x1: RX_PULSE_MODE

BSI_MIPI_BIF_MODE (cont.)

Bits	Name	Description
2	MIPI_BIF_TX_PULSE_TYPE	Indicates the type of pulse to transmit. 0: PHY transmits a one tau INT pulse. 1: PHY transmits a TPUL (240us) pulse to wake up battery slave. 0x0: TX_PULSE_1_TAU 0x1: TX_PULSE_240US
1	MIPI_BIF_RX_DATA_FORMAT	Receiver 11b/17b data format selection. 0: MIPI BIF PHY receiver operates in 11-bit communication mode. Parity and inversion is performed by PHY. 11-bit data (BCF, 10-bit payload, D9-D0) is stored in MIPI_BIF_DATA_RX registers. 1: MIPI BIF PHY receiver operates in 17-bit data mode. Parity and inversion is performed by SW. Full 17-bit BIF word (BCF, BCFn+10-bit data+4-bit parity+INV) is stored in MIPI_BIF_DATA_RX registers. 0x0: RX_11BIT_MODE 0x1: RX_17BIT_MODE
0	MIPI_BIF_TX_DATA_FORMAT	Transmitter 11b/17b data format selection. 0: MIPI BIF PHY transmitter operates in 11-bit communication mode. Parity and inversion is performed by PHY. Only 11-bit data is (BCF, 10-bit payload) is stored in MIPI_BIF_DATA_TX registers. 1: MIPI BIF PHY transmitter operates in 17-bit data mode. Parity and inversion is performed by SW. Full 17-bit BIF word (BCF, BCFn+10-bit data+4-bit parity+INV) is stored in MIPI_BIF_DATA_TX registers. 0x0: TX_11BIT_MODE 0x1: TX_17BIT_MODE

0x00001B54 BSI_MIPI_BIF_EN

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

MIPI BIF Enable/Disable

BSI_MIPI_BIF_EN

Bits	Name	Description
7	MIPI_BIF_TX_EN	MIPI BIF transmitter enable 1: Enable MIPI_BIF transmitter to transmit data or generate pulse 0: Disable MIPI BIF transmitter, Tx word in-progress will complete, Tx word pending will be discarded 0x0: TX_DISABLED 0x1: TX_ENABLED

BSI_MIPI_BIF_EN (cont.)

Bits	Name	Description
6	MIPI_BIF_RX_EN	MIPI BIF receiver enable 1: Enable MIPI_BIF receiver to received data or pulse 0: Disable receiver. When BSI_EN is set to 1, MIPI_BIF_TX_EN is set to 0, and MIPI_BIF_RX_EN is set to 0, BIF is set to low power mode (no clock requested). In low power mode, BIF detects slave initiated interrupt only when RX_PULSE_MODE is set to 1. 0x0: RX_DISABLED 0x1: RX_ENABLED

0x00001B55 BSI_MIPI_BIF_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

BSI_MIPI_BIF_CFG

Bits	Name	Description
7	MIPI_BIF_PU_EN	Pull up resistor enable 0: Disable chip internal pull-up resistor. 1: Enable chip internal pull-up resistor. 0x0: PULLUP_DISABLED 0x1: PULLUP_ENABLED

0x00001B56 BSI_MIPI_BIF_RX_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x03

Reset Name: PERPH_rb

BSI_MIPI_BIF_RX_CFG

Bits	Name	Description
4	FIFO_EN	Enable/Disable RX FIFO. SW shall configure this register bit only when bus is idle. 0: Disable RX FIFO. When RX FIFO is disabled, the whole RX flow control and interrupt generation scheme works the same as the legacy usage: RX interrupt is generated after each battery data word is received. SW shall fetch RX battery data from MIPI_BIF_DATA_RX_* registers only upon receiving RX interrupt. Flow control error is set when SW can't keep up with RX speed. 1: Enable RX FIFO. If RX FIFO is enabled, RX battery data are stored in a 8 deep buffer. Interrupt is generated based on RX_IRQ_FREQ value. SW shall fetch RX battery data from RX_FIFO_WORD* registers. Flow control error is set when the RX FIFO overflows. RX FIFO stores 11 bit battery data word only. If RX data format is set to 17 bit, SW shall expect no inversion, parity error check on received battery data. 0x1: FIFO_ENABLED 0x0: FIFO_DISABLED
2:0	RX_IRQ_FREQ	Supported only when RX FIFO is enabled. Program RX interrupt generation frequency while receiving data from battery. Frequency = bit[2:0] + 1. During the middle of a RX burst, a RX interrupt is generated after receiving every bit[2:0]+1 words. At the end of a RX burst, a RX interrupt is always generated. If FIFO is disabled, a RX interrupt is generated after receiving each battery data word. This register value will not cause a difference. 0x7: FREQ_8_WORDS 0x6: FREQ_7_WORDS 0x5: FREQ_6_WORDS 0x4: FREQ_5_WORDS 0x3: FREQ_4_WORDS 0x2: FREQ_3_WORDS 0x1: FREQ_2_WORDS 0x0: FREQ_1_WORD

0x00001B5A BSI_MIPI_BIF_DATA_TX_0

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

BSI_MIPI_BIF_DATA_TX_0

Bits	Name	Description
7:0	MIPI_BIF_DATA_TX	Transmit data byte 0. 17-bit data format: bit[7] D3 bit[6] D2 bit[5] D1 bit[4] P2 bit[3] D0 bit[2] P1 bit[1] P0 bit[0] INV 11-bit data format: bit[7:0] D7-D0

0x00001B5B BSI_MIPI_BIF_DATA_TX_1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

BSI_MIPI_BIF_DATA_TX_1

Bits	Name	Description
7:0	MIPI_BIF_DATA_TX	Transmit data byte 1. 17-bit data format: bit[7] BCFn bit[6:1] D9-D4 bit[0] P3 11-bit data format: bit[7:3] Not Used bit [2] BCF bit [1:0] D9-D8

0x00001B5C BSI_MIPI_BIF_DATA_TX_2

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

BSI_MIPI_BIF_DATA_TX_2

Bits	Name	Description
0	MIPI_BIF_DATA_TX	Transmit data byte 2 for 17-bit data format. 17-bit data format: BCF. 11-bit data format: Not Used.

0x00001B5D BSI_MIPI_BIF_TX_CTL

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

MIPI BIF Control Registers. A pulse is generated on each SW write.

BSI_MIPI_BIF_TX_CTL

Bits	Name	Description
0	MIPI_BIF_TX_GO	Writes 1 to the register bit initiates the TX transaction. BSI must be enabled before setting the register.

0x00001B60 BSI_MIPI_BIF_DATA_RX_0

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

BSI_MIPI_BIF_DATA_RX_0

Bits	Name	Description
7:0	MIPI_BIF_DATA_RX	Received data byte 0. 17-bit data format: bit[7] D3 bit[6] D2 bit[5] D1 bit[4] P2 bit[3] D0 bit[2] P1 bit[1] P0 bit[0] INV 11-bit data format: bit[7:0] D7-D0

0x00001B61 BSI_MIPI_BIF_DATA_RX_1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

BSI_MIPI_BIF_DATA_RX_1

Bits	Name	Description
7:0	MIPI_BIF_DATA_RX	Received data byte 1. 17-bit data format: bit[7] BCFn bit[6:1] D9-D4 bit[0] P3 11-bit data format: bit[7:3] Not Used bit [2] BCF bit [1:0] D9-D8

0x00001B62 BSI_MIPI_BIF_DATA_RX_2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

MIPI BIF Read Data

BSI_MIPI_BIF_DATA_RX_2

Bits	Name	Description
4	MIPI_BIF_DATA_LOOPBACK_TAG	Loopback tag. 1: The received data was transmitted by MIPI BIF itself. 0: The received data was initiated from Battery 0x0: NORMAL_DATA 0x1: LOOPBACK_DATA
0	MIPI_BIF_DATA_RX	Received data byte 2 for 17-bit data format. 17-bit data format: BCF 11-bit data format: Not used.

0x00001B63 BSI_RX_FIFO_WORD1_0

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Supported 11-bit data format only

BSI_RX_FIFO_WORD1_0

Bits	Name	Description
7:0	RX_DATA	11-bit data format only bit[7:0]: D7-D0

0x00001B64 BSI_RX_FIFO_WORD1_1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Supported 11-bit data format only

BSI_RX_FIFO_WORD1_1

Bits	Name	Description
7	DATA_VALID	0. FIFO is empty. This data is not valid FIFO data. 1. This data is valid FIFO data. 0x1: DATA_VALID 0x0: DATA_NOT_VALID

BSI_RX_FIFO_WORD1_1 (cont.)

Bits	Name	Description
6	ERROR_FLAG	1: Error happened on this RX word. The data is for debugging purpose. RX transaction is frozen after BSI seeing the error. 0: No error on this data. 0x1: DATA_ERROR 0x0: DATA_OK
2:0	RX_DATA	bit [2]: BCF bit [1:0]: D9-D8

0x00001B65 BSI_RX_FIFO_WORD2_0

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Supported 11-bit data format only

BSI_RX_FIFO_WORD2_0

Bits	Name	Description
7:0	RX_DATA	11-bit data format only bit[7:0]: D7-D0

0x00001B66 BSI_RX_FIFO_WORD2_1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Supported 11-bit data format only

BSI_RX_FIFO_WORD2_1

Bits	Name	Description
7	DATA_VALID	0. FIFO is empty. This data is not valid FIFO data. 1. This data is valid FIFO data. 0x1: DATA_VALID 0x0: DATA_NOT_VALID

BSI_RX_FIFO_WORD2_1 (cont.)

Bits	Name	Description
6	ERROR_FLAG	1: Error happened on this RX word. The data is for debugging purpose. RX transaction is frozen after BSI seeing the error. 0: No error on this data. 0x1: DATA_ERROR 0x0: DATA_OK
2:0	RX_DATA	bit [2]: BCF bit [1:0]: D9-D8

0x00001B67 BSI_RX_FIFO_WORD3_0

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Supported 11-bit data format only

BSI_RX_FIFO_WORD3_0

Bits	Name	Description
7:0	RX_DATA	11-bit data format only bit[7:0]: D7-D0

0x00001B68 BSI_RX_FIFO_WORD3_1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Supported 11-bit data format only

BSI_RX_FIFO_WORD3_1

Bits	Name	Description
7	DATA_VALID	0. FIFO is empty. This data is not valid FIFO data. 1. This data is valid FIFO data. 0x1: DATA_VALID 0x0: DATA_NOT_VALID

BSI_RX_FIFO_WORD3_1 (cont.)

Bits	Name	Description
6	ERROR_FLAG	1: Error happened on this RX word. The data is for debugging purpose. RX transaction is frozen after BSI seeing the error. 0: No error on this data. 0x1: DATA_ERROR 0x0: DATA_OK
2:0	RX_DATA	bit [2]: BCF bit [1:0]: D9-D8

0x00001B69 BSI_RX_FIFO_WORD4_0

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Supported 11-bit data format only

BSI_RX_FIFO_WORD4_0

Bits	Name	Description
7:0	RX_DATA	11-bit data format only bit[7:0]: D7-D0

0x00001B6A BSI_RX_FIFO_WORD4_1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Supported 11-bit data format only

BSI_RX_FIFO_WORD4_1

Bits	Name	Description
7	DATA_VALID	0. FIFO is empty. This data is not valid FIFO data. 1. This data is valid FIFO data. 0x1: DATA_VALID 0x0: DATA_NOT_VALID

BSI_RX_FIFO_WORD4_1 (cont.)

Bits	Name	Description
6	ERROR_FLAG	1: Error happened on this RX word. The data is for debugging purpose. RX transaction is frozen after BSI seeing the error. 0: No error on this data. 0x1: DATA_ERROR 0x0: DATA_OK
2:0	RX_DATA	bit [2]: BCF bit [1:0]: D9-D8

0x00001B6D BSI_MIPI_BIF_BCL_RAW

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: N/A

Raw sample of BCL for SW to use

BSI_MIPI_BIF_BCL_RAW

Bits	Name	Description
0	MIPI_BIF_BCL_RAW	Raw sample of BCL for SW to use 0x0: BCL_STATE_LOW 0x1: BCL_STATE_HIGH

0x00001B70 BSI_MIPI_BIF_ERROR

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

MIPI BIF Error Code

BSI_MIPI_BIF_ERROR

Bits	Name	Description
3:0	MIPI_BIF_ERROR_CODE	Stores the first error code when BIF encounters an error during TX or RX transaction. Error code is cleared only when SW sets MIPI_BIF_CLEAR_ERR register. If both inversion error and parity error happen, only inversion error is reported. 0: No Error 1: RX data bit number is over 17 2: RX data parity error 3: RX data inversion error -- more than half of the 14 data + parity bits are 1 4: Flow control error -- If RX FIFO is disabled: SW hasn't fetched the battery data from last transaction before a new battery initiated data is received and ready to load. No flow control for loopback data. If RX FIFO is enabled: this register indicates RX FIFO overflow. 5: Bus Collision -- PHY attempted to drive BCL low when it was not idle (high) at the start of a transmission 6: bit timing equal to 2 Tau 7: bit timing greater or equal to 4 Tau 8: BCF equals to BCFn 0x0: NO_ERROR 0x1: LENGTH_ERR 0x2: PARITY_ERR 0x3: INVERSION_ERR 0x4: FLOW_CONTROL_ERR 0x5: BUS_COLLISION_ERR 0x6: TIMING_2TAU_ERR 0x7: TIMING_4TAU_ERR 0x8: BCF_ERR

0x00001BA8 BSI_BAT_RMV_DEB_TIMER

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x11

Reset Name: PERPH_rb

BSI_BAT_RMV_DEB_TIMER

Bits	Name	Description
4:0	RMV_TIMER	Program battery removal debouncer timing (unit: Sleep Clock Cycle) Programmable Range: 0 - 31 Sleep clocks A maximum one sleep clock cycle uncertainty shall be expected on top of each programmed value. For example: 0: 0 - 1 sleep clock 1: 1 - 2 sleep clocks 31: 31 - 32 sleep clocks Battery detection is active only when BSI is enabled (BSI_EN=1). 0x0: SCLK0_1 0x1: SCLK1_2 0x2: SCLK2_3 0x3: SCLK3_4 0x4: SCLK4_5 0x5: SCLK5_6 0x6: SCLK6_7 0x7: SCLK7_8 0x8: SCLK8_9 0x9: SCLK9_10 0xA: SCLK10_11 0xB: SCLK11_12 0xC: SCLK12_13 0xD: SCLK13_14 0xE: SCLK14_15 0xF: SCLK15_16 0x10: SCLK16_17 0x11: SCLK17_18 0x12: SCLK18_19 0x13: SCLK19_20 0x14: SCLK20_21 0x15: SCLK21_22 0x16: SCLK22_23 0x17: SCLK23_24 0x18: SCLK24_25 0x19: SCLK25_26 0x1A: SCLK26_27 0x1B: SCLK27_28 0x1C: SCLK28_29 0x1D: SCLK29_30 0x1E: SCLK30_31 0x1F: SCLK31_32

0x00001BA9 BSI_BAT_PRES_DEB_TIMER

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

BSI_BAT_PRES_DEB_TIMER

Bits	Name	Description
4:0	PRES_TIMER	Program battery presence debouncer timing (unit: Sleep Clock Cycle) Programmable Range: 0 - 31 Sleep clocks A maximum one sleep clock cycle uncertainty shall be expected on top of each programmed value. For example: 0: 0 - 1 sleep clock 1: 1 - 2 sleep clocks 31: 31 - 32 sleep clocks Battery detection is active only when BSI is enabled (BSI_EN=1). 0x0: SCLK0_1 0x1: SCLK1_2 0x2: SCLK2_3 0x3: SCLK3_4 0x4: SCLK4_5 0x5: SCLK5_6 0x6: SCLK6_7 0x7: SCLK7_8 0x8: SCLK8_9 0x9: SCLK9_10 0xA: SCLK10_11 0xB: SCLK11_12 0xC: SCLK12_13 0xD: SCLK13_14 0xE: SCLK14_15 0xF: SCLK15_16 0x10: SCLK16_17 0x11: SCLK17_18 0x12: SCLK18_19 0x13: SCLK19_20 0x14: SCLK20_21 0x15: SCLK21_22 0x16: SCLK22_23 0x17: SCLK23_24 0x18: SCLK24_25 0x19: SCLK25_26 0x1A: SCLK26_27 0x1B: SCLK27_28 0x1C: SCLK28_29 0x1D: SCLK29_30 0x1E: SCLK30_31 0x1F: SCLK31_32

16 BUA_BUA_BATT_GONE

0x00001C00 BUA_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

BUA_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00001C01 BUA_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

BUA_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x00001C02 BUA_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

BUA_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00001C03 BUA_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

BUA_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x00001C04 BUA_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x1E

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

BUA_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	

0x00001C05 BUA_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x05

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

BUA_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x0: BUA 0x1: BUA_NO_CHARGER 0x3: BUA_4UICC 0x4: BUA_EXT_CHARGER 0x5: BUA_BATT_GONE

0x00001C08 BUA_STATUS1

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: N/A

Status Registers

BUA_STATUS1

Bits	Name	Description
7	BUA_OK	0 = BUA is disabled 1 = BUA is enabled 0x1: BUA_ENABLED 0x0: BUA_DISABLED

0x00001C40 BUA_BUA_CTL1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x10

Reset Name: PERPH_RB

Programmable battery removal debounce time

BUA_BUA_CTL1

Bits	Name	Description
6:4	BATT_RMV_DEB	BAT_GONE debounce timer 3'b000: 0-1 sclk 3'b001: 1-2 sclk (default) 3'b010: 2-3 sclk 3'b011: 5-6 sclk 3'b100: 8-9 sclk 3'b101: 11-12 sclk 3'b110: 15-16 sclk 3'b111: 31-32 sclk 0x0: SCLK_0_TO_1 0x1: SCLK_1_TO_2 0x2: SCLK_2_TO_3 0x3: SCLK_5_TO_6 0x4: SCLK_8_TO_9 0x5: SCLK_11_TO_12 0x6: SCLK_15_TO_16 0x7: SCLK_31_TO_32

0x00001C46 BUA_EN_CTL1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

BUA enable

BUA_EN_CTL1

Bits	Name	Description
7	BUA_EN	0 = BUA is disabled 1 = BUA is enabled 0x1: BUA_ENABLED 0x0: BUA_DISABLED

17 MBG1_MBG_DIG

0x00002C00 MBG1_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

MBG1_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00002C01 MBG1_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [15:8]

MBG1_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x00002C02 MBG1_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: n/a

HW Version Register [23:16]

MBG1_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00002C03 MBG1_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [31:24]

MBG1_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x00002C04 MBG1_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x0E

Reset Name: n/a

Peripheral Type

MBG1_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	0xE: MBG

0x00002C05 MBG1_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: n/a

Peripheral SubType

MBG1_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	

0x00002C08 MBG1_STATUS1

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: n/a

Status Registers

MBG1_STATUS1

Bits	Name	Description
7	MBG_OK	1= MBG has started up and the Vref1p25 is charged up to at least vbg_pon level 0x0: MBG_NOT_OK 0x1: MBG_OK
1	NPM_TRUE	1 = MBG is on and in NPM 0x0: MBG_LPM 0x1: MBG_NPM

0x00002C44 MBG1_MODE_CTRL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x91

Reset Name: perph_rb

MBG1_MODE_CTRL

Bits	Name	Description
7	FORCE_NPM	Force NPM whenever this bit is set 0x0: NO_FORCE_LPM 0x1: FORCE_NPM
4	NPM_FOLLOW_SLEEPB	1' = transition to NPM, whenever PMIC is awake, '0' = LPM (IPTAT_EN and IREF_EN must be set 0x0: NO_FOLLOW 0x1: FOLLOW_SLEEP_B
3	FORCE_FASTVBG	set this bit high will force fast charge mode always on instead of the auto mode controlled by the MBG_OK signal. 0x0: NORMAL_MODE 0x1: FORCE_FAST_VBG
2	FORCE_MBGCC_EN	set this bit high will force the curvature correction block on in both normal mode and sleep mode if Iref and Iptat is available 0x0: CC_DISABLED 0x1: CC_ENABLED
1	FORCE_IPTAT_EN	set this bit high will force the IPTAT block on in sleep mode 0x0: NO_FORCE_IPTAT 0x1: FORCE_IPTAT
0	FORCE_IREF_EN	set this bit high will force Iref block on in sleep mode 0x0: NO_FORCE_IREF 0x1: FORCE_IREF

0x00002C46 MBG1_EN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

MBG1_EN_CTL

Bits	Name	Description
7	MBG_EN	this bit is one of the multiple MBG_EN signals that are from different sources and ORed together to control the ON/OFF of MBG block 0x0: MBG_DISABLED 0x1: MBG_ENABLED

18 VADC1_USR_VADC

0x00003100 VADC1_USR_REVISION1

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

VADC1_USR_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00003101 VADC1_USR_REVISION2

Type: R
Clock: pbus_wrclk
Reset State: 0x04

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

VADC1_USR_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x00003102 VADC1_USR_REVISION3

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

VADC1_USR_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00003103 VADC1_USR_REVISION4

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

VADC1_USR_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x00003104 VADC1_USR_PERPH_TYPE

Type: R
Clock: pbus_wrclk
Reset State: 0x08

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

VADC1_USR_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	ADC

0x00003105 VADC1_USR_PERPH_SUBTYPE

Type: R
Clock: pbus_wrclk
Reset State: 0x40

Reset Name: N/A

Peripheral SubType

VADC1_USR_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	ADC sub type

0x00003108 VADC1_USR_STATUS1

Type: R
Clock: pbus_wrclk
Reset State: 0x01

Reset Name: N/A

Status Registers

VADC1_USR_STATUS1

Bits	Name	Description
4:3	OP_MODE	Selects basic mode of operation 0x0: NORM_MODE 0x1: CONV_SEQ_MODE 0x2: MEAS_INT_MODE
2	MEAS_INTERVAL_EN_STS	Interval Mode 0x0: INTERVAL_MODE_DISABLED 0x1: INTERVAL_MODE_ENABLED
1	REQ_STS	REQ_STS mirrors the REQ bit. When REQ is asserted the arbiter stores a descriptor in the conversion request queue. Bit is cleared when ADC conversion is completed. 0x0: REQ_NOT_IN_PROGRESS 0x1: REQ_IN_PROGRESS

VADC1_USR_STATUS1 (cont.)

Bits	Name	Description
0	EOC	End of conversion status flag. Bit is de-asserted when arbiter is servicing a conversion request and asserted when conversion is completed. After a conversion is requested, the EOC and REQ_STS bits can be polled to determine ADC conversion status as follows: REQ_STS EOC Arbiter state 1 1 Waiting for ADC to complete another process's conversion request. 1 0 ADC conversion occurring. 0 1 ADC conversion completed. 0 0 Invalid 0x0: CONV_NOT_COMPLETE 0x1: CONV_COMPLETE

0x00003109 VADC1_USR_STATUS2

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: N/A

Status Registers

VADC1_USR_STATUS2

Bits	Name	Description
7:3	CONV_SEQ_STATE	Conversion request and control states selected by SEL_FSM register field. SEL_FSM Signal 0 {conversion error, Request FSM state[3;0]} 1 VADC conversion control FSM state[4:0] 2 Sample average count[4:0] 3 Sample average count[9:5] Enumerations are Request FSM state[3:0]. VADC conversion control FSM state[4:0] encodings are: 0 IDLE 1 WAIT_VREG_OK_S 2 ENABLE_ADC_S 3 RESET_FILTER_S 4 WAIT_ADC_EOC_S 5 WAIT_SAMPLE_ACC_S 6 INCREMENT_READ_POINTER_S 7 WAIT_STORE_REQ_S 8 LATCH_FIFO_READ_DATA_S 9 COMPARE_OLD_NEW_REQ_S 10 WAIT_VREG_OK_D 11 WAIT1_IADC_FSM 12 ENABLE_ADC_D 13 WAIT2_IADC_FSM 14 RESET_FILTER_D 15 WAIT_ADC_EOC_D 16 WAIT3_IADC_FSM 17 WAIT_SAMPLE_ACC 18 INCREMENT_RD_POINTER_D 19 WAIT_STORE_WRITE_POINTERS 20 WAIT_COMPARE_RW_POINTERS 21 WAIT_STORE_REQ_D 22 LATCH_FIFO_READ_DATE_D 23 COMPARE_OLD_NEW_REQ_D 24 WAIT_PRECHARGE_S 25 DISABLE_ADC 0x0: IDLE_S 0x1: WAIT_TRIG_S 0x2: WAIT_HOLDOFF_S 0x3: CLEAR_ACC_S 0x4: STORE_REQ_S 0x5: WAIT_ADC_EOC_S 0x6: GEN_IRQ_S 0x7: IDLE_D 0x8: WAIT_TRIG_D

VADC1_USR_STATUS2 (cont.)

Bits	Name	Description
		0x9: WAIT_HOLDOFF_D 0xA: CLEAR_ACC_D 0xB: STORE_WRITE_POINTERS 0xC: COMPARE_RW_POINTERS 0xD: STORE_REQ_D 0xE: WAIT_ADC_EOC_D 0xF: GEN_IRQ_D
1	FIFO_NOT_EMPTY_FLAG	Indicates conversion sequencer request written to FIFO when it was not empty. 0x0: FIFO_EMPTY_WHEN_REQ_MADE 0x1: FIFO_NOT_EMPTY_WHEN_REQ_MADE
0	CONV_SEQ_TIMEOUT_STS	Indicates conversion sequencer conversion was triggered by time out. 0x0: CONV_SEQ_TIMEOUT_FALSE 0x1: CONV_SEQ_TIMEOUT_TRUE

0x00003110 VADC1_USR_INT_RT_STS

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Interrupt Real Time Status Bits

VADC1_USR_INT_RT_STS

Bits	Name	Description
4	LOW_THR_INT_RT_STS	ADC output lower than low threshold. Active high signal. 0x0: LOW_THR_INT_FALSE 0x1: LOW_THR_INT_TRUE
3	HIGH_THR_INT_RT_STS	ADC output higher than high threshold. Active high signal. 0x0: HIGH_THR_INT_FALSE 0x1: HIGH_THR_INT_TRUE
2	CONV_SEQ_TIMEOUT_INT_RT_STS	Indicates conversion sequencer conversion was triggered by SBI register field conversion request time out. 0x0: CONV_SEQ_TIMEOUT_FALSE 0x1: CONV_SEQ_TIMEOUT_TRUE
1	FIFO_NOT_EMPTY_INT_RT_STS	Indicates conversion sequencer request written to FIFO when it was not empty. 0x0: FIFO_NOT_EMPTY_INT_FALSE 0x1: FIFO_EMPTY_INT_TRUE

VADC1_USR_INT_RT_STS (cont.)

Bits	Name	Description
0	EOC_INT_RT_STS	Secure process end of conversion interrupt. Active high signal two tcxo_clk cycles wide. 0x0: CONV_COMPLETE_INT_FALSE 0x1: CONV_COMPLETE_INT_TRUE

0x00003111 VADC1_USR_INT_SET_TYPE

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

0 = use level trigger interrupts, 1 = use edge trigger interrupts

VADC1_USR_INT_SET_TYPE

Bits	Name	Description
4	LOW_THR_INT_SET_TYPE	Low threshold interrupt set type 0x0: LOW_THR_INT_LEVEL 0x1: LOW_THR_INT_EDGE
3	HIGH_THR_INT_SET_TYPE	High threshold interrupt set type 0x0: HIGH_THR_INT_LEVEL 0x1: HIGH_THR_INT_EDGE
2	CONV_SEQ_TIMEOUT_INT_SET_TYPE	Conversion sequencer timeout interrupt set type 0x0: CONV_SEQ_TIMEOUT_LEVEL 0x1: CONV_SEQ_TIMEOUT_EDGE
1	FIFO_NOT_EMPTY_INT_SET_TYPE	FIFO not empty interrupt set type 0x0: FIFO_NOT_EMPTY_LEVEL 0x1: FIFO_NOT_EMPTY_EDGE
0	EOC_SET_INT_TYPE	EOC interrupt set type 0x0: EOC_LEVEL 0x1: EOC_EDGE

0x00003112 VADC1_USR_INT_POLARITY_HIGH

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

VADC1_USR_INT_POLARITY_HIGH

Bits	Name	Description
4	LOW_THR_INT_HIGH	Low threshold interrupt high polarity enabled 0x0: LOW_THR_INT_POL_HIGH_DISABLED 0x1: LOW_THR_INT_POL_HIGH_ENABLED
3	HIGH_THR_INT_HIGH	High threshold interrupt high polarity enabled 0x0: HIGH_THR_INT_POL_HIGH_DISABLED 0x1: HIGH_THR_INT_POL_HIGH_ENABLED
2	CONV_SEQ_TIMEOUT_INT_HIGH	Conversion sequencer interrupt high polarity enabled 0x0: CONV_SEQ_TIMEOUT_INT_POL_HIGH_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_POL_HIGH_ENABLED
1	FIFO_NOT_EMPTY_INT_HIGH	FIFO not empty interrupt high polarity enabled 0x0: FIFO_NOT_EMPTY_INT_POL_HIGH_DISABLED 0x1: FIFO_NOT_EMPTY_INT_POL_HIGH_ENABLED
0	EOC_INT_HIGH	EOC interrupt high polarity enabled 0x0: EOC_INT_POL_HIGH_DISABLED 0x1: EOC_INT_POL_HIGH_ENABLED

0x00003113 VADC1_USR_INT_POLARITY_LOW

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

VADC1_USR_INT_POLARITY_LOW

Bits	Name	Description
4	LOW_THR_INT_HIGH	Low threshold interrupt low polarity enabled 0x0: LOW_THR_INT_POL_LOW_DISABLED 0x1: LOW_THR_INT_POL_LOW_ENABLED
3	HIGH_THR_INT_HIGH	High threshold interrupt low polarity enabled 0x0: HIGH_THR_INT_POL_LOW_DISABLED 0x1: HIGH_THR_INT_POL_LOW_ENABLED
2	CONV_SEQ_TIMEOUT_INT_LOW	Conversion sequencer interrupt low polarity enabled 0x0: CONV_SEQ_TIMEOUT_INT_POL_LOW_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_POL_LOW_ENABLED
1	FIFO_NOT_EMPTY_INT_LOW	FIFO not empty interrupt low polarity enabled 0x0: FIFO_NOT_EMPTY_INT_POL_LOW_DISABLED 0x1: FIFO_NOT_EMPTY_INT_POL_LOW_ENABLED

VADC1_USR_INT_POLARITY_LOW (cont.)

Bits	Name	Description
0	EOC_INT_LOW	EOC interrupt low polarity enabled 0x0: EOC_INT_POL_LOW_DISABLED 0x1: EOC_INT_POL_LOW_ENABLED

0x00003114 VADC1_USR_INT_LATCHED_CLR

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Writing a '1' to a bit in this register will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

VADC1_USR_INT_LATCHED_CLR

Bits	Name	Description
4	LOW_THR_INT_LATCHED_CLR	Low threshold interrupt latched clear
3	HIGH_THR_INT_LATCHED_CLR	High threshold interrupt latched clear
2	CONV_SEQ_TIMEOUT_INT_LATCHED_CLR	Conversion sequencer interrupt latched clear
1	FIFO_NOT_EMPTY_INT_LATCHED_CLR	FIFO not empty interrupt latched clear
0	EOC_INT_LATCHED_CLR	EOC interrupt latched clear

0x00003115 VADC1_USR_INT_EN_SET

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Writing '0' to a bit in this register has no effect. Writing a '1' to a bit in this register will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

VADC1_USR_INT_EN_SET

Bits	Name	Description
4	LOW_THR_INT_EN_SET	Low threshold interrupt enable set 0x0: LOW_THR_INT_DISABLED 0x1: LOW_THR_INT_ENBLED
3	HIGH_THR_INT_EN_SET	High threshold interrupt enable set 0x0: HIGH_THR_INT_DISABLED 0x1: HIGH_THR_INT_ENBLED
2	CONV_SEQ_TIMEOUT_INT_EN_SET	Conversion sequencer interrupt enable set 0x0: CONV_SEQ_TIMEOUT_INT_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_ENBLED
1	FIFO_NOT_EMPTY_INT_EN_SET	FIFO not empty interrupt enable set 0x0: FIFO_NOT_EMPTY_INT_DISABLED 0x1: FIFO_NOT_EMPTY_INT_ENBLED
0	EOC_INT_EN_SET	EOC interrupt enable set 0x0: EOC_INT_DISABLED 0x1: EOC_INT_ENBLED

0x00003116 VADC1_USR_INT_EN_CLR

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Writing a '0' to a bit in this register has no effect. Writing a '1' to a bit in this register will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

VADC1_USR_INT_EN_CLR

Bits	Name	Description
4	LOW_THR_INT_EN_CLR	Low threshold interrupt enable clear 0x0: LOW_THR_INT_DISABLED 0x1: LOW_THR_INT_ENBLED
3	HIGH_THR_INT_EN_CLR	High threshold interrupt enable clear 0x0: HIGH_THR_INT_DISABLED 0x1: HIGH_THR_INT_ENBLED
2	CONV_SEQ_TIMEOUT_INT_EN_CLR	Conversion sequencer interrupt enable clear 0x0: CONV_SEQ_TIMEOUT_INT_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_ENBLED

VADC1_USR_INT_EN_CLR (cont.)

Bits	Name	Description
1	FIFO_NOT_EMPTY_INT_EN_CLR	FIFO not empty interrupt enable clear 0x0: FIFO_NOT_EMPTY_INT_DISABLED 0x1: FIFO_NOT_EMPTY_INT_ENBLED
0	EOC_INT_EN_CLR	EOC interrupt enable clear 0x0: EOC_INT_DISABLED 0x1: EOC_INT_ENBLED

0x00003118 VADC1_USR_INT_LATCHED_STS

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

VADC1_USR_INT_LATCHED_STS

Bits	Name	Description
4	LOW_THR_INT_LATCHED_STS	Low threshold interrupt latched 0x0: LOW_THR_INT_LATCHED_FALSE 0x1: LOW_THR_INT_LATCHED_TRUE
3	HIGH_THR_INT_LATCHED_STS	High threshold interrupt latched 0x0: HIGH_THR_INT_LATCHED_FALSE 0x1: HIGH_THR_INT_LATCHED_TRUE
2	CONV_SEQ_TIMEOUT_INT_LATCHED_STS	Conversion sequencer interrupt latched 0x0: CONV_SEQ_TIMEOUT_INT_LATCHED_FALSE 0x1: CONV_SEQ_TIMEOUT_INT_LATCHED_TRUE
1	FIFO_NOT_EMPTY_INT_LATCHED_STS	FIFO not empty interrupt latched 0x0: FIFO_NOT_EMPTY_INT_LATCHED_FALSE 0x1: FIFO_NOT_EMPTY_INT_LATCHED_TRUE
0	EOC_INT_LATCHED_STS	EOC interrupt latched 0x0: EOC_INT_LATCHED_FALSE 0x1: EOC_INT_LATCHED_TRUE

0x00003119 VADC1_USR_INT_PENDING_STS

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Debug: Pending is set if interrupt has been sent but not cleared.

VADC1_USR_INT_PENDING_STS

Bits	Name	Description
4	LOW_THR_INT_PENDING_STS	Low threshold interrupt pending 0x0: LOW_THR_INT_PENDING_FALSE 0x1: LOW_THR_INT_PENDING_TRUE
3	HIGH_THR_INT_PENDING_STS	High threshold interrupt pending 0x0: HIGH_THR_INT_PENDING_FALSE 0x1: HIGH_THR_INT_PENDING_TRUE
2	CONV_SEQ_TIMEOUT_INT_PENDING_STS	Conversion sequencer interrupt pending 0x0: CONV_SEQ_TIMEOUT_INT_PENDING_FALSE 0x1: CONV_SEQ_TIMEOUT_INT_PENDING_TRUE
1	FIFO_NOT_EMPTY_INT_PENDING_STS	FIFO not empty interrupt pending 0x0: FIFO_NOT_EMPTY_INT_PENDING_FALSE 0x1: FIFO_NOT_EMPTY_INT_PENDING_TRUE
0	EOC_INT_PENDING_STS	EOC interrupt pending 0x0: EOC_INT_PENDING_FALSE 0x1: EOC_INT_PENDING_TRUE

0x0000311A VADC1_USR_INT_MID_SEL

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Selects the MID that will receive the interrupt

VADC1_USR_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	Selects the MID that will receive the interrupt

0x0000311B VADC1_USR_INT_PRIORITY

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Selects the SPMI interrupt priority

VADC1_USR_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	Selects the SPMI interrupt priority 0x0: SR 0x1: A

0x00003140 VADC1_USR_MODE_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x03

Reset Name: uvlo_perph_rb

Settings Common to Input and Output

VADC1_USR_MODE_CTL

Bits	Name	Description
4:3	OP_MODE	Selects basic mode of operation: 00=Normal Mode - Single measurement 01=Conversion Sequencer - Single measurement using conversion sequencer 10=Measurement Interval - Single or Continuous measurements at specified delay/interval 0x0: NORM_MODE 0x1: CONV_SEQ_MODE 0x2: MEAS_INT_MODE
2	VREF_XO_THM_FORCE	When cleared, VDD_REF is connected to XO thermistor in active mode, disconnected in sleep mode When set, force VDD_REF to be connected to the XO thermistor regardless the status of sleep 0x0: VREF_XO_THM_FORCE_FALSE 0x1: VREF_XO_THM_FORCE_TRUE
1	AMUX_TRIM_EN	Enable AMUX trim 0x0: AMUX_TRIM_DISABLED 0x1: AMUX_TRIM_ENABLED

VADC1_USR_MODE_CTL (cont.)

Bits	Name	Description
0	ADC_TRIM_EN	Enable ADC trim 0x0: ADC_TRIM_DISABLED 0x1: ADC_TRIM_ENABLED

0x00003146 VADC1_USR_EN_CTL1

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Enables ADC module.

VADC1_USR_EN_CTL1

Bits	Name	Description
7	ADC_EN	Enables ADC module. 0x0: ADC_DISABLED 0x1: ADC_ENABLED

0x00003148 VADC1_USR_ADC_CH_SEL_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x06

Reset Name: uvlo_perph_rb

ADC Channel selection.

VADC1_USR_ADC_CH_SEL_CTL

Bits	Name	Description
7:0	ADC_CH_SEL	ADC Channel selection.

0x00003150 VADC1_USR_ADC_DIG_PARAM

Type: RW
Clock: pbus_wrclk
Reset State: 0x04

Reset Name: uvlo_perph_rb

ADC Digital Parameters

VADC1_USR_ADC_DIG_PARAM

Bits	Name	Description
3:2	DEC_RATIO_SEL	Decimation ratio: 0x0: DECI_512 0x1: DECI_1K 0x2: DECI_2K 0x3: DECI_4K
1:0	CLK_SEL	Select ADC clock rate: 0x0: CLK_SEL_2P4MHZ 0x1: CLK_SEL_4P8MHZ 0x2: CLK_SEL_9P6MHZ 0x3: CLK_SEL_19P2MHZ

0x00003151 VADC1_USR_HW_SETTLE_DELAY

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Settle Delay

VADC1_USR_HW_SETTLE_DELAY

Bits	Name	Description
3:0	HW_SETTLE_DELAY	Time between AMUX getting configured and the ADC starting conversion. Delay = 100us*(value) for value<11, and 2ms*(value-10) otherwise 0x0: HW_SETTLE_DELAY_0US 0x1: HW_SETTLE_DELAY_100US 0x2: HW_SETTLE_DELAY_200US 0x3: HW_SETTLE_DELAY_300US 0x4: HW_SETTLE_DELAY_400US 0x5: HW_SETTLE_DELAY_500US 0x6: HW_SETTLE_DELAY_600US 0x7: HW_SETTLE_DELAY_700US 0x8: HW_SETTLE_DELAY_800US 0x9: HW_SETTLE_DELAY_900US 0xA: HW_SETTLE_DELAY_1MS 0xB: HW_SETTLE_DELAY_2MS 0xC: HW_SETTLE_DELAY_4MS 0xD: HW_SETTLE_DELAY_6MS 0xE: HW_SETTLE_DELAY_8MS 0xF: HW_SETTLE_DELAY_10MS

0x00003152 VADC1_USR_CONV_REQ

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: req_rb

Conversion Request

VADC1_USR_CONV_REQ

Bits	Name	Description
7	REQ	Conversion request strobe. When bit is asserted the arbiter stores a descriptor in the conversion request queue. Bit is cleared when ADC conversion is completed. 0x0: CONV_REQ_FALSE 0x1: CONV_REQ_TRUE

0x00003154 VADC1_USR_CONV_SEQ_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x45

Reset Name: uvlo_perph_rb

Conversion Sequencer Control

VADC1_USR_CONV_SEQ_CTL

Bits	Name	Description
7:4	CONV_SEQ_HOLDOFF	Select delay from conversion trigger signal (i.e. adc_conv_seq_trig) transition to ADC enable. Delay = 25us*(value+1). Actual delay will be longer if request is stored in a non empty FIFO and/or conversion needs to wait for LDO OK handshake. 0x0: SEQ_HOLD_25US 0x1: SEQ_HOLD_50US 0x2: SEQ_HOLD_75US 0x3: SEQ_HOLD_100US 0x4: SEQ_HOLD_125US 0x5: SEQ_HOLD_150US 0x6: SEQ_HOLD_175US 0x7: SEQ_HOLD_200US 0x8: SEQ_HOLD_225US 0x9: SEQ_HOLD_250US 0xA: SEQ_HOLD_275US 0xB: SEQ_HOLD_300US 0xC: SEQ_HOLD_325US 0xD: SEQ_HOLD_350US 0xE: SEQ_HOLD_375US 0xF: SEQ_HOLD_400US
3:0	CONV_SEQ_TIMEOUT	Select delay (0 to 15ms) from conversion request to triggering conversion sequencer hold off timer. 0x0: SEQ_TIMEOUT_0MS 0x1: SEQ_TIMEOUT_1MS 0x2: SEQ_TIMEOUT_2MS 0x3: SEQ_TIMEOUT_3MS 0x4: SEQ_TIMEOUT_4MS 0x5: SEQ_TIMEOUT_5MS 0x6: SEQ_TIMEOUT_6MS 0x7: SEQ_TIMEOUT_7MS 0x8: SEQ_TIMEOUT_8MS 0x9: SEQ_TIMEOUT_9MS 0xA: SEQ_TIMEOUT_10MS 0xB: SEQ_TIMEOUT_11MS 0xC: SEQ_TIMEOUT_12MS 0xD: SEQ_TIMEOUT_13MS 0xE: SEQ_TIMEOUT_14MS 0xF: SEQ_TIMEOUT_15MS

0x00003155 VADC1_USR_CONV_SEQ_TRIG_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Conversion Sequencer Trigger Select

VADC1_USR_CONV_SEQ_TRIG_CTL

Bits	Name	Description
7	CONV_SEQ_TRIG_COND	Select conversion trigger condition(s) that starts ADC conversion hold off timer. 0x0 - Falling edge 0x1 - Rising edge 0x0: FALLING_EDGE 0x1: RISING_EDGE
1:0	CONV_SEQ_TRIG_SEL	Select conversion sequencer trigger input signal. 0x0: ADC_TRIG0 0x1: ADC_TRIG1 0x2: ADC_TRIG2 0x3: ADC_TRIG3

0x00003157 VADC1_USR_MEAS_INTERVAL_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Interval Mode Control

VADC1_USR_MEAS_INTERVAL_CTL

Bits	Name	Description
3:0	MEAS_INTERVAL_TIME	Select measurement interval time (i.e., If value=0, use 0ms, else use 2^(value+4)/32768). 0x0: MEAS_INTERVAL_0MS 0x1: MEAS_INTERVAL_1P0MS 0x2: MEAS_INTERVAL_2P0MS 0x3: MEAS_INTERVAL_3P9MS 0x4: MEAS_INTERVAL_7P8MS 0x5: MEAS_INTERVAL_15P6MS 0x6: MEAS_INTERVAL_31P3MS 0x7: MEAS_INTERVAL_62P5MS 0x8: MEAS_INTERVAL_125MS 0x9: MEAS_INTERVAL_250MS 0xA: MEAS_INTERVAL_500MS 0xB: MEAS_INTERVAL_1S 0xC: MEAS_INTERVAL_2S 0xD: MEAS_INTERVAL_4S 0xE: MEAS_INTERVAL_8S 0xF: MEAS_INTERVAL_16S

0x00003159 VADC1_USR_MEAS_INTERVAL_OP_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Interval mode select

VADC1_USR_MEAS_INTERVAL_OP_CTL

Bits	Name	Description
7	MEAS_INTERVAL_OP	Interval mode select 0x0: INTERVAL_MODE_DISABLED 0x1: INTERVAL_MODE_ENABLED

0x0000315A VADC1_USR_FAST_AVG_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Fast Average Control

VADC1_USR_FAST_AVG_CTL

Bits	Name	Description
3:0	FAST_AVG_SAMPLES	Select number of samples for use in fast average mode (i.e. 2^(value). 0x0: AVG_1_SAMPLE 0x1: AVG_2_SAMPLES 0x2: AVG_4_SAMPLES 0x3: AVG_8_SAMPLES 0x4: AVG_16_SAMPLES 0x5: AVG_32_SAMPLES 0x6: AVG_64_SAMPLES 0x7: AVG_128_SAMPLES 0x8: AVG_256_SAMPLES 0x9: AVG_512_SAMPLES

0x0000315B VADC1_USR_FAST_AVG_EN

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Fast Average Enable

VADC1_USR_FAST_AVG_EN

Bits	Name	Description
7	FAST_AVG_EN	Select low latency for multiple conversions 0x0: FAST_AVG_DISABLED 0x1: FAST_AVG_ENABLED

0x0000315C VADC1_USR_LOW_THR0

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Low Threshold Byte 0

VADC1_USR_LOW_THR0

Bits	Name	Description
7:0	LOW_THR_7_0	Low byte of low threshold detector

0x0000315D VADC1_USR_LOW_THR1

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Low Threshold Byte 1

VADC1_USR_LOW_THR1

Bits	Name	Description
7:0	LOW_THR_15_8	High byte of low threshold detector

0x0000315E VADC1_USR_HIGH_THR0

Type: RW
Clock: pbus_wrclk
Reset State: 0xFF

Reset Name: uvlo_perph_rb

High Threshold Byte 0

VADC1_USR_HIGH_THR0

Bits	Name	Description
7:0	HIGH_THR_7_0	Low byte of high threshold detector

0x0000315F VADC1_USR_HIGH_THR1

Type: RW
Clock: pbus_wrclk
Reset State: 0xFF

Reset Name: uvlo_perph_rb

High Threshold Byte 1

VADC1_USR_HIGH_THR1

Bits	Name	Description
7:0	HIGH_THR_15_8	High byte of high threshold detector

0x00003160 VADC1_USR_DATA0

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: uvlo_perph_rb

ADC Sample Byte 0

VADC1_USR_DATA0

Bits	Name	Description
7:0	DATA_7_0	Low byte of ADC output

0x00003161 VADC1_USR_DATA1

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: uvlo_perph_rb

ADC Sample Byte 1

VADC1_USR_DATA1

Bits	Name	Description
7:0	DATA_15_8	High byte of ADC output

0x00003162 VADC1_USR_MIN_LOW_THR0

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Minimum Low Threshold Byte 0

VADC1_USR_MIN_LOW_THR0

Bits	Name	Description
7:0	MIN_LOW_THR_7_0	Low byte of minimum low threshold detector

0x00003163 VADC1_USR_MIN_LOW_THR1

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: uvlo_perph_rb

Minimum Low Threshold Byte 1

VADC1_USR_MIN_LOW_THR1

Bits	Name	Description
7:0	MIN_LOW_THR_15_8	High byte of minimum low threshold detector

0x00003166 VADC1_USR_MIN_DATA0

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: uvlo_perph_rb

Minimum ADC Sample Byte 0

VADC1_USR_MIN_DATA0

Bits	Name	Description
7:0	MIN_DATA_7_0	Low byte of minimum ADC output

0x00003167 VADC1_USR_MIN_DATA1

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: uvlo_perph_rb

Minimum ADC Sample Byte 1

VADC1_USR_MIN_DATA1

Bits	Name	Description
7:0	MIN_DATA_15_8	High byte of minimum ADC output

0x000031D0 VADC1_USR_SEC_ACCESS

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

Secure Access

PMIC_LOCKING

VADC1_USR_SEC_ACCESS

Bits	Name	Description
7:0	SEC_UNLOCK	Unlock the Secure Registers by writing 0xA5 to this register. Lock is rearmed after the next write to the module.

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0x00014000 LDO1_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC_CONSTANT

LDO1_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00014001 LDO1_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC_CONSTANT

LDO1_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x00014002 LDO1_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: n/a

HW Version Register [23:16]

LDO1_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00014003 LDO1_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

LDO1_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x00014004 LDO1_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x04

Reset Name: n/a

Peripheral Type

PMIC_CONSTANT

LDO1_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	LDO

0x00014005 LDO1_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x28

Reset Name: n/a

Peripheral SubType

LDO1_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	P50 for example

0x00014008 LDO1_STATUS1

Type: R
Clock: PBUS_WRCLK
Reset State: 0bXX000XX

Reset Name: n/a

Status Registers

LDO1_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode 0x1: LDO_VOLTAGE_OK 0x0: LDO_VOLTAGE_LOW
5	ILS_DETECTED	upper limit is programmed to a value less than the lower limit 0x1: UPPER_LIMIT_SETTING_ERR 0x0: UPPER_LIMIT_SETTING_OK
4	UL_VOLTAGE_DETECTED	Last voltage set was above UL_Voltage 0x1: VOLTAGE_LEVEL_SETTING_OVERLIMIT 0x0: VOLTAGE_LEVEL_SETTING_OK

LDO1_STATUS1 (cont.)

Bits	Name	Description
3	LL_VOLTAGE_DETECTED	Last voltage set was below LL_Voltage 0x1: VOLTAGE_LEVEL_SETTING_UNDERLIMIT 0x0: VOLTAGE_LEVEL_SETTING_OK
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

0x00014009 LDO1_STATUS2

Type: R
Clock: PBUS_WRCLK
Reset State: 0b0000000X

Reset Name: n/a

Status Registers

LDO1_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode 0x1: SOFTSTART_DONE 0x0: SOFTSTART_NOT_DONE
6	OVER_CURRENT_DETECTED	current limit of the LDO is reached 0x1: OVER_CURRENT_DETECTED 0x0: NO_OVER_CURRENT_DETECTED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF
0	LDO_RANGE_EXT	range extension control bit going to LDO 0x1: LDO_RANGE_EXTENDED 0x0: LDO_RANGE_NOT_EXTENDED

0x0001400A LDO1_STATUS3

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: n/a

Status Registers

LDO1_STATUS3

Bits	Name	Description
7	LDO_RANGE_SEL	range selection control bit going to LDO 0x1: LDO_RANGE_SELECTED 0x0: LDO_RANGE_NOT_SELECTED
6:0	LDO_VSET	voltage programming bits going to LDO 0x1: LDO_PROGRAM_SELECTED 0x0: LDO_PROGRAM_NOT_SELECTED

0x00014010 LDO1_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

LDO1_INT_RT_STS

Bits	Name	Description
1	LIMIT_ERROR_RT_STS	Last voltage set was below or equal to LL_Voltage 0x1: VOLTAGE_LEVEL_SETTING_UNDERLIMIT 0x0: VOLTAGE_LEVEL_SETTING_OK
0	VREG_OK_RT_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_ERR

0x00014011 LDO1_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

LDO1_INT_SET_TYPE

Bits	Name	Description
1	LIMIT_ERROR_TYPE	Interrupt type, edge or level 0x1: LIMIT_ERROR_LEVEL_TRIGGERED 0x0: LIMIT_ERROR_EDGE_TRIGGERED

LDO1_INT_SET_TYPE (cont.)

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level 0x1: VREG_OK_LEVEL_TRIGGERED 0x0: VREG_OK_EDGE_TRIGGERED

0x00014012 LDO1_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

LDO1_INT_POLARITY_HIGH

Bits	Name	Description
1	LIMIT_ERROR_HIGH	Edge type, rising or Level type, high true 0x1: LIMIT_ERROR_HIGH_TRIGGERED 0x0: LIMIT_ERROR_HIGH_DISABLED
0	VREG_OK_HIGH	Edge type, rising or Level type, high true 0x1: VREG_OK_LOW_TRIGGERED 0x0: VREG_OK_LOW_DISABLED

0x00014013 LDO1_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

LDO1_INT_POLARITY_LOW

Bits	Name	Description
1	LIMIT_ERROR_LOW	Edge type, falling or Level type, low true 0x1: LIMIT_ERROR_RISING_TRIGGERED 0x0: LIMIT_ERROR_FALLING_TRIGGERED
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

0x00014014 LDO1_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

LDO1_INT_LATCHED_CLR

Bits	Name	Description
1	LIMIT_ERROR_LATCHED_CLR	0x1: LIMIT_ERROR_REARM 0x0: LIMIT_ERROR_NOT_REARM
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

0x00014015 LDO1_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

LDO1_INT_EN_SET

Bits	Name	Description
1	LIMIT_ERROR_EN_SET	0x1: LIMIT_ERROR_ENABLED 0x0: LIMIT_ERROR_DISABLED
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED 0x0: VREG_OK_ERROR_DISABLED

0x00014016 LDO1_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

LDO1_INT_EN_CLR

Bits	Name	Description
1	LIMIT_ERROR_EN_CLR	0x1: LIMIT_ERROR_ENABLED 0x0: LIMIT_ERROR_DISABLED
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED 0x0: VREG_OK_ERROR_DISABLED

0x00014018 LDO1_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

LDO1_INT_LATCHED_STS

Bits	Name	Description
1	LIMIT_ERROR_LATCHED_STS	Last voltage set was below or equal to LL_Voltage 0x1: VOLTAGE_LEVEL_SETTING_UNDERLIMIT 0x0: VOLTAGE_LEVEL_SETTING_OK
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled 0x1: LDO_VOLTAGE_LOW 0x0: LDO_VOLTAGE_OK

0x00014019 LDO1_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

LDO1_INT_PENDING_STS

Bits	Name	Description
1	LIMIT_ERROR_PENDING_STS	Last voltage set was below or equal to LL_Voltage 0x1: VOLTAGE_LEVEL_SETTING_UNDERLIMIT 0x0: VOLTAGE_LEVEL_SETTING_OK
0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

0x0001401A LDO1_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Selects the MID that will receive the interrupt

LDO1_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1 0x0: INT_MID_SEL_0

0x0001401B LDO1_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

LDO1_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

0x00014040 LDO1_VOLTAGE_CTL1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x03

Reset Name: perph_rb

This register is latched to VOLTAGE_CTL2 register. Need to write to VOLTAGE_CTL2 register after writing to this register to update the RANGE value.

LDO1_VOLTAGE_CTL1

Bits	Name	Description
2:0	RANGE	0x00: unused 0x01: unused 0x02: range 2 (Vmin=0.75 V, Vstep=12.5 mV) 0x03: range 3 Vmin=1.5 V, Vstep=25 mV 0x04: range 4 (Vmin=1.75 V, Vstep=50 mV)

0x00014041 LDO1_VOLTAGE_CTL2

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x0C

Reset Name: perph_rb

LDO1_VOLTAGE_CTL2

Bits	Name	Description
6:0	VSET	Range 2: 0.75V+0.0125V*X; X=0, 1, ..., 63 Range 3: 1.5V+0.025V*X; X=0, 1, ..., 63 Range 4: 1.75V+0.5V*X; X=0, 1, ..., 63

0x00014045 LDO1_MODE_CTL2

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x80

Reset Name: perph_rb

Define LDO Mode Transitions

LDO1_MODE_CTL2

Bits	Name	Description
7	NPM	Force NPM 0x1: FORCED_NPM 0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE 0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode 0x1: BYPASS_ENABLED 0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B) 0x1: FOLLOW_PMIC_AWAKE_TRUE 0x0: FOLLOW_PMIC_AWAKE_FALSE
3	NPM_FOLLOW_HW_EN3	NPM mode setting using HWEN3 0x1: NPM_FOLLOW_HW_EN3_TRUE 0x0: NPM_FOLLOW_HW_EN3_FALSE
2	NPM_FOLLOW_HW_EN2	NPM mode setting using HWEN2 0x1: NPM_FOLLOW_HW_EN2_TRUE 0x0: NPM_FOLLOW_HW_EN2_FALSE
1	NPM_FOLLOW_HW_EN1	NPM mode setting using HWEN1 0x1: NPM_FOLLOW_HW_EN1_TRUE 0x0: NPM_FOLLOW_HW_EN1_FALSE
0	NPM_FOLLOW_HW_EN0	NPM mode setting using HWEN0 0x1: NPM_FOLLOW_HW_EN0_TRUE 0x0: NPM_FOLLOW_HW_EN0_FALSE

0x00014046 LDO1_EN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

LDO1_EN_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
3	FOLLOW_HW_EN3	NPM enable setting using HWEN3 0x1: FOLLOW_HW_EN3_TRUE 0x0: FOLLOW_HW_EN3_FALSE

LDO1_EN_CTL (cont.)

Bits	Name	Description
2	FOLLOW_HW_EN2	NPM enable setting using HWEN2 0x1: FOLLOW_HW_EN2_TRUE 0x0: FOLLOW_HW_EN2_FALSE
1	FOLLOW_HW_EN1	NPM enable setting using HWEN1 0x1: FOLLOW_HW_EN1_TRUE 0x0: FOLLOW_HW_EN1_FALSE
0	FOLLOW_HW_EN0	NPM enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

0x00014048 LDO1_PD_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x80

Reset Name: perph_rb

LDO1_PD_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pull-down when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

0x0001404A LDO1_CURRENT_LIM_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x80

Reset Name: perph_rb

LDO1_CURRENT_LIM_CTL

Bits	Name	Description
7	CURRENT_LIM_EN	0x1: CURRENT_LIM_ENABLED 0x0: CURRENT_LIM_DISABLED
5	CURRENT_LIM_TESTMODE_EN	Current Limit for test mode (lower limit) 0x1: CURRENT_LIM_TESTMODE_ENABLED 0x0: CURRENT_LIM_TESTMODE_DISABLED

0x0001404C LDO1_SOFT_START_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x80

Reset Name: perph_rb

LDO1_SOFT_START_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED 0x0: SOFT_START_DISABLED

0x00014052 LDO1_CONFIG_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0xF0

Reset Name: perph_rb

LDO1_CONFIG_CTL

Bits	Name	Description
7:6	CLAMP_CTRL	For N1200 LDO only, changes the clamp voltage for undershoot improvement
5	CLAMP_EN	For N1200 LDO only, undershoot improvement 0x1: CLAMP_ENABLED 0x0: CLAMP_DISABLED
4	CASCADE	For NMOS LDO only 0x1: CASCADE_TRUE 0x0: CASCADE_FALSE
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED 0x0: ACT_BYPASS_BUFF_DISABLED

0x000140D0 LDO1_SEC_ACCESS

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

PMIC_LOCKING

LDO1_SEC_ACCESS

Bits	Name	Description
7:0	SEC_UNLOCK	Unlock the Secure Registers (0xTBD) by writing 0xA5 to this register. Lock is rearmed after the next write to the module. 0xA5: SEC_UNLOCK 0x0: SEC_LOCKED

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0x0000A000 MPP1_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

MPP1_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x0000A001 MPP1_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

MPP1_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x0000A002 MPP1_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

MPP1_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x0000A003 MPP1_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

MPP1_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x0000A004 MPP1_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x11

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

MPP1_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	0x11: MPP

0x0000A005 MPP1_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x05

Reset Name: N/A

Peripheral SubType

MPP1_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x3: MPP_4CH_SINK 0x5: MPP_4CH_AOUT 0x7: MPP_4CH_AOUT_SINK 0xB: MPP_8CH_SINK 0xD: MPP_8CH_AOUT 0xF: MPP_8CH_AOUT_SINK

0x0000A008 MPP1_STATUS1

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: N/A

Status Registers

MPP1_STATUS1

Bits	Name	Description
7	MPP_OK	0 = MPP is disabled 1 = MPP is enabled 0x0: MPP_DISABLED 0x1: MPP_ENABLED
0	MPP_VAL	Value read by the input buffer, if enabled 0x0: MPP_INPUT_LOW 0x1: MPP_INPUT_HIGH

0x0000A010 MPP1_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Interrupt Real Time Status Bits

MPP1_INT_RT_STS

Bits	Name	Description
0	MPP_IN_STS	0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH

0x0000A011 MPP1_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

MPP1_INT_SET_TYPE

Bits	Name	Description
0	MPP_IN_TYPE	0x0: LEVEL 0x1: EDGE

0x0000A012 MPP1_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

MPP1_INT_POLARITY_HIGH

Bits	Name	Description
0	MPP_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x0000A013 MPP1_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

MPP1_INT_POLARITY_LOW

Bits	Name	Description
0	MPP_IN_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x0000A014 MPP1_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

MPP1_INT_LATCHED_CLR

Bits	Name	Description
0	MPP_IN_LATCHED_CLR	

0x0000A015 MPP1_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

MPP1_INT_EN_SET

Bits	Name	Description
0	MPP_IN_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED

0x0000A016 MPP1_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

MPP1_INT_EN_CLR

Bits	Name	Description
0	MPP_IN_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

0x0000A018 MPP1_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

MPP1_INT_LATCHED_STS

Bits	Name	Description
0	MPP_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

0x0000A019 MPP1_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

MPP1_INT_PENDING_STS

Bits	Name	Description
0	MPP_IN_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

0x0000A01A MPP1_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

MPP1_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x0000A01B MPP1_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP1_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR 0x1: A

0x0000A040 MPP1_MODE_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

MPP1_MODE_CTL

Bits	Name	Description
6:4	MODE	MPP Type: 0x0: DIGITAL_INPUT 0x1: DIGITAL_OUTPUT 0x2: DIGITAL_IN_AND_OUT 0x3: BIDIRECTIONAL 0x4: ANALOG_INPUT 0x5: ANALOG_OUTPUT 0x6: CURRENT_SINK 0x7: RESERVED

MPP1_MODE_CTL (cont.)

Bits	Name	Description
3:0	EN_AND_SOURCE_SEL	When configured as a digital output Source select: 0000 = 0 0001 = 1 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4 Enable control when configured as AOUT, or Current Sink. MPP is enable whenever the selected condition is true. 0000 = 0 (mpp is always disabled) 0001 = 1 (mpp is always Enabled) 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4 0x0: LOW 0x1: HIGH 0x2: PAIRED_MPP 0x3: NOT_PAIRED_MPP 0x4: RESERVED4 0x5: RESERVED5 0x6: RESERVED6 0x7: RESERVED7 0x8: DTEST1 0x9: NOT_DTEST1

MPP1_MODE_CTL (cont.)

Bits	Name	Description
		0xA: DTEST2 0xB: NOT_DTEST2 0xC: DTEST3 0xD: NOT_DTEST3 0xE: DTEST4 0xF: NOT_DTEST4

0x0000A041 MPP1_DIG_VIN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP1_DIG_VIN_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source: 0x0: VIN0 0x1: VIN1 0x2: VIN2 0x3: VIN3

0x0000A042 MPP1_DIG_PULL_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP1_DIG_PULL_CTL

Bits	Name	Description
2:0	PULLUP_SEL	Pull-up Resistor Control in bidirectional mode only. 00: 0.6k ** 01: open (infinite resistance) 10: 10K 11: 30K * 0x0: R600OHM 0x1: OPEN 0x2: R10KOHM 0x3: R30KOHM

0x0000A043 MPP1_DIG_IN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Enable DTEST buffers

MPP1_DIG_IN_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED
1	DTEST2	Route to DTEST2 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED

0x0000A046 MPP1_EN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP1_EN_CTL

Bits	Name	Description
7	PERPH_EN	MPP Master enable 0 = puts MPP_PAD at high Z and disables the block 1 = MPP is enabled 0x0: MPP_DISABLED 0x1: MPP_ENABLED

0x0000A048 MPP1_ANA_OUT_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP1_ANA_OUT_CTL

Bits	Name	Description
2:0	REF_SEL	Analog Output Control 0x0: Output = vref_1V25 = REF_BYP pin, typically 1.25 V 0x1: Output = vref_V625 = 0.625 V (internal use only) 0x2: Output = vref_V3125 = 0.3125 V (internal use only) 0x3: Output = paired MPP input (internal use only) 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved

0x0000A04A MPP1_ANA_IN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP1_ANA_IN_CTL

Bits	Name	Description
2:0	ROUTE_SEL	AMUX Channel Control 0x0: Route to hkadc5 0x1: Route to hkadc6 0x2: Route to hkadc7 0x3: Route to hkadc8 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved

0x0000A04C MPP1_SINK_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP1_SINK_CTL

Bits	Name	Description
2:0	CURRENT_SEL	Current Sink Output Control 0x0: CURRENT_5MA 0x1: CURRENT_10MA 0x2: CURRENT_15MA 0x3: CURRENT_20MA 0x4: CURRENT_25MA 0x5: CURRENT_30MA 0x6: CURRENT_35MA 0x7: CURRENT_40MA

21 MPP2_MPP

0x0000A100 MPP2_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

MPP2_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x0000A101 MPP2_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

MPP2_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x0000A102 MPP2_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

MPP2_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x0000A103 MPP2_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

MPP2_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x0000A104 MPP2_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x11

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

MPP2_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	0x11: MPP

0x0000A105 MPP2_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x03

Reset Name: N/A

Peripheral SubType

MPP2_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x3: MPP_4CH_SINK 0x5: MPP_4CH_AOUT 0x7: MPP_4CH_AOUT_SINK 0xB: MPP_8CH_SINK 0xD: MPP_8CH_AOUT 0xF: MPP_8CH_AOUT_SINK

0x0000A108 MPP2_STATUS1

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: N/A

Status Registers

MPP2_STATUS1

Bits	Name	Description
7	MPP_OK	0 = MPP is disabled 1 = MPP is enabled 0x0: MPP_DISABLED 0x1: MPP_ENABLED
0	MPP_VAL	Value read by the input buffer, if enabled 0x0: MPP_INPUT_LOW 0x1: MPP_INPUT_HIGH

0x0000A110 MPP2_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Interrupt Real Time Status Bits

MPP2_INT_RT_STS

Bits	Name	Description
0	MPP_IN_STS	0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH

0x0000A111 MPP2_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

MPP2_INT_SET_TYPE

Bits	Name	Description
0	MPP_IN_TYPE	0x0: LEVEL 0x1: EDGE

0x0000A112 MPP2_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

MPP2_INT_POLARITY_HIGH

Bits	Name	Description
0	MPP_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x0000A113 MPP2_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

MPP2_INT_POLARITY_LOW

Bits	Name	Description
0	MPP_IN_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x0000A114 MPP2_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

MPP2_INT_LATCHED_CLR

Bits	Name	Description
0	MPP_IN_LATCHED_CLR	

0x0000A115 MPP2_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

MPP2_INT_EN_SET

Bits	Name	Description
0	MPP_IN_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED

0x0000A116 MPP2_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

MPP2_INT_EN_CLR

Bits	Name	Description
0	MPP_IN_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

0x0000A118 MPP2_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

MPP2_INT_LATCHED_STS

Bits	Name	Description
0	MPP_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

0x0000A119 MPP2_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

MPP2_INT_PENDING_STS

Bits	Name	Description
0	MPP_IN_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

0x0000A11A MPP2_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

MPP2_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x0000A11B MPP2_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP2_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR 0x1: A

0x0000A140 MPP2_MODE_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

MPP2_MODE_CTL

Bits	Name	Description
6:4	MODE	MPP Type: 0x0: DIGITAL_INPUT 0x1: DIGITAL_OUTPUT 0x2: DIGITAL_IN_AND_OUT 0x3: BIDIRECTIONAL 0x4: ANALOG_INPUT 0x5: ANALOG_OUTPUT 0x6: CURRENT_SINK 0x7: RESERVED

MPP2_MODE_CTL (cont.)

Bits	Name	Description
3:0	EN_AND_SOURCE_SEL	When configured as a digital output Source select: 0000 = 0 0001 = 1 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4 Enable control when configured as AOUT, or Current Sink. MPP is enable whenever the selected condition is true. 0000 = 0 (mpp is always disabled) 0001 = 1 (mpp is always Enabled) 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4 0x0: LOW 0x1: HIGH 0x2: PAIRED_MPP 0x3: NOT_PAIRED_MPP 0x4: RESERVED4 0x5: RESERVED5 0x6: RESERVED6 0x7: RESERVED7 0x8: DTEST1 0x9: NOT_DTEST1

MPP2_MODE_CTL (cont.)

Bits	Name	Description
		0xA: DTEST2 0xB: NOT_DTEST2 0xC: DTEST3 0xD: NOT_DTEST3 0xE: DTEST4 0xF: NOT_DTEST4

0x0000A141 MPP2_DIG_VIN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP2_DIG_VIN_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source: 0x0: VIN0 0x1: VIN1 0x2: VIN2 0x3: VIN3

0x0000A142 MPP2_DIG_PULL_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP2_DIG_PULL_CTL

Bits	Name	Description
2:0	PULLUP_SEL	Pull-up Resistor Control in bidirectional mode only. 00: 0.6k ** 01: open (infinite resistance) 10: 10K 11: 30K * 0x0: R600OHM 0x1: OPEN 0x2: R10KOHM 0x3: R30KOHM

0x0000A143 MPP2_DIG_IN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Enable DTEST buffers

MPP2_DIG_IN_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED
1	DTEST2	Route to DTEST2 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED

0x0000A146 MPP2_EN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP2_EN_CTL

Bits	Name	Description
7	PERPH_EN	MPP Master enable 0 = puts MPP_PAD at high Z and disables the block 1 = MPP is enabled 0x0: MPP_DISABLED 0x1: MPP_ENABLED

0x0000A148 MPP2_ANA_OUT_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP2_ANA_OUT_CTL

Bits	Name	Description
2:0	REF_SEL	Analog Output Control 0x0: Output = vref_1V25 = REF_BYP pin, typically 1.25 V 0x1: Output = vref_V625 = 0.625 V (internal use only) 0x2: Output = vref_V3125 = 0.3125 V (internal use only) 0x3: Output = paired MPP input (internal use only) 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved

0x0000A14A MPP2_ANA_IN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP2_ANA_IN_CTL

Bits	Name	Description
2:0	ROUTE_SEL	AMUX Channel Control 0x0: Route to hkadc5 0x1: Route to hkadc6 0x2: Route to hkadc7 0x3: Route to hkadc8 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved

0x0000A14C MPP2_SINK_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP2_SINK_CTL

Bits	Name	Description
2:0	CURRENT_SEL	Current Sink Output Control 0x0: CURRENT_5MA 0x1: CURRENT_10MA 0x2: CURRENT_15MA 0x3: CURRENT_20MA 0x4: CURRENT_25MA 0x5: CURRENT_30MA 0x6: CURRENT_35MA 0x7: CURRENT_40MA

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0x0000A300 MPP4_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

MPP4_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x0000A301 MPP4_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

MPP4_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x0000A302 MPP4_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

MPP4_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x0000A303 MPP4_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

MPP4_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x0000A304 MPP4_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x11

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

MPP4_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	0x11: MPP

0x0000A305 MPP4_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x03

Reset Name: N/A

Peripheral SubType

MPP4_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x3: MPP_4CH_SINK 0x5: MPP_4CH_AOUT 0x7: MPP_4CH_AOUT_SINK 0xB: MPP_8CH_SINK 0xD: MPP_8CH_AOUT 0xF: MPP_8CH_AOUT_SINK

0x0000A308 MPP4_STATUS1

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: N/A

Status Registers

MPP4_STATUS1

Bits	Name	Description
7	MPP_OK	0 = MPP is disabled 1 = MPP is enabled 0x0: MPP_DISABLED 0x1: MPP_ENABLED
0	MPP_VAL	Value read by the input buffer, if enabled 0x0: MPP_INPUT_LOW 0x1: MPP_INPUT_HIGH

0x0000A310 MPP4_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Interrupt Real Time Status Bits

MPP4_INT_RT_STS

Bits	Name	Description
0	MPP_IN_STS	0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH

0x0000A311 MPP4_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

MPP4_INT_SET_TYPE

Bits	Name	Description
0	MPP_IN_TYPE	0x0: LEVEL 0x1: EDGE

0x0000A312 MPP4_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

MPP4_INT_POLARITY_HIGH

Bits	Name	Description
0	MPP_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x0000A313 MPP4_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

MPP4_INT_POLARITY_LOW

Bits	Name	Description
0	MPP_IN_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x0000A314 MPP4_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

MPP4_INT_LATCHED_CLR

Bits	Name	Description
0	MPP_IN_LATCHED_CLR	

0x0000A315 MPP4_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

MPP4_INT_EN_SET

Bits	Name	Description
0	MPP_IN_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED

0x0000A316 MPP4_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

MPP4_INT_EN_CLR

Bits	Name	Description
0	MPP_IN_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

0x0000A318 MPP4_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

MPP4_INT_LATCHED_STS

Bits	Name	Description
0	MPP_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

0x0000A319 MPP4_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

MPP4_INT_PENDING_STS

Bits	Name	Description
0	MPP_IN_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

0x0000A31A MPP4_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

MPP4_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x0000A31B MPP4_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP4_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR 0x1: A

0x0000A340 MPP4_MODE_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

MPP4_MODE_CTL

Bits	Name	Description
6:4	MODE	MPP Type: 0x0: DIGITAL_INPUT 0x1: DIGITAL_OUTPUT 0x2: DIGITAL_IN_AND_OUT 0x3: BIDIRECTIONAL 0x4: ANALOG_INPUT 0x5: ANALOG_OUTPUT 0x6: CURRENT_SINK 0x7: RESERVED

MPP4_MODE_CTL (cont.)

Bits	Name	Description
3:0	EN_AND_SOURCE_SEL	When configured as a digital output Source select: 0000 = 0 0001 = 1 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4 Enable control when configured as AOUT, or Current Sink. MPP is enable whenever the selected condition is true. 0000 = 0 (mpp is always disabled) 0001 = 1 (mpp is always Enabled) 0010 = paired MPP 0011 = inverted paired MPP 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = DTEST1 1001 = inverted DTEST1 1010 = DTEST2 1011 = inverted DTEST2 1100 = DTEST3 1101 = inverted DTEST3 1110 = DTEST4 1111 = inverted DTEST4 0x0: LOW 0x1: HIGH 0x2: PAIRED_MPP 0x3: NOT_PAIRED_MPP 0x4: RESERVED4 0x5: RESERVED5 0x6: RESERVED6 0x7: RESERVED7 0x8: DTEST1 0x9: NOT_DTEST1

MPP4_MODE_CTL (cont.)

Bits	Name	Description
		0xA: DTEST2 0xB: NOT_DTEST2 0xC: DTEST3 0xD: NOT_DTEST3 0xE: DTEST4 0xF: NOT_DTEST4

0x0000A341 MPP4_DIG_VIN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP4_DIG_VIN_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source: 0x0: VIN0 0x1: VIN1 0x2: VIN2 0x3: VIN3

0x0000A342 MPP4_DIG_PULL_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP4_DIG_PULL_CTL

Bits	Name	Description
2:0	PULLUP_SEL	Pull-up Resistor Control in bidirectional mode only. 00: 0.6k ** 01: open (infinite resistance) 10: 10K 11: 30K * 0x0: R600OHM 0x1: OPEN 0x2: R10KOHM 0x3: R30KOHM

0x0000A343 MPP4_DIG_IN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Enable DTEST buffers

MPP4_DIG_IN_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED
1	DTEST2	Route to DTEST2 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED

0x0000A346 MPP4_EN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP4_EN_CTL

Bits	Name	Description
7	PERPH_EN	MPP Master enable 0 = puts MPP_PAD at high Z and disables the block 1 = MPP is enabled 0x0: MPP_DISABLED 0x1: MPP_ENABLED

0x0000A348 MPP4_ANA_OUT_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP4_ANA_OUT_CTL

Bits	Name	Description
2:0	REF_SEL	Analog Output Control 0x0: Output = vref_1V25 = REF_BYP pin, typically 1.25 V 0x1: Output = vref_V625 = 0.625 V (internal use only) 0x2: Output = vref_V3125 = 0.3125 V (internal use only) 0x3: Output = paired MPP input (internal use only) 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved

0x0000A34A MPP4_ANA_IN_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP4_ANA_IN_CTL

Bits	Name	Description
2:0	ROUTE_SEL	AMUX Channel Control 0x0: Route to hkadc5 0x1: Route to hkadc6 0x2: Route to hkadc7 0x3: Route to hkadc8 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved

0x0000A34C MPP4_SINK_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

MPP4_SINK_CTL

Bits	Name	Description
2:0	CURRENT_SEL	Current Sink Output Control 0x0: CURRENT_5MA 0x1: CURRENT_10MA 0x2: CURRENT_15MA 0x3: CURRENT_20MA 0x4: CURRENT_25MA 0x5: CURRENT_30MA 0x6: CURRENT_35MA 0x7: CURRENT_40MA

23 FLASH1_FLSH_DRVR

0x0001D300 FLASH1_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: N/A

HW Version Register [7:0]

FLASH1_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x0001D301 FLASH1_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

FLASH1_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x0001D302 FLASH1_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [23:16]

FLASH1_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x0001D303 FLASH1_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [31:24]

FLASH1_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x0001D304 FLASH1_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x18

Reset Name: N/A

Peripheral Type

FLASH1_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	Flash driver

0x0001D305 FLASH1_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

Peripheral SubType

FLASH1_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	Flash driver

0x0001D308 FLASH1_LED_FAULT_STATUS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Status Register

FLASH1_LED_FAULT_STATUS

Bits	Name	Description
5	VREG_OK_FAULT	0 = No vreg_ok fault 1 = vreg_ok fault occurred
4	THERMAL_DERATE	0 = No thermal derating happened 1 = Thermal derating happened. Use ADC to measure DAC reference voltage.
3	LED2_OPEN_FAULT	0 = No open fault occurred on LED2 1 = Open fault occurred on LED2
2	LED1_OPEN_FAULT	0 = No open fault occurred on LED1 1 = Open fault occurred on LED1
1	LED2_SHORT_FAULT	0 = No short fault occurred on LED2 1 = Short fault occurred on LED2
0	LED1_SHORT_FAULT	0 = No short fault occurred on LED1 1 = Short fault occurred on LED1

0x0001D309 FLASH1_LED1_IRAMP_STATUS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

FLASH1_LED1_IRAMP_STATUS

Bits	Name	Description
7:0	LED1_RAMP_CURRENT	This register reads back LED1's current code when vph_pwr_droop last happened,,,,'

0x0001D30A FLASH1_LED2_IRAMP_STATUS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

FLASH1_LED2_IRAMP_STATUS

Bits	Name	Description
7:0	LED2_RAMP_CURRENT	This register reads back LED2's current code when vph_pwr_droop last happened,,,,'

0x0001D30B FLASH1_LED1_MASK_RAMP_STATUS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Valid only when MASK_RAMP_CTRL=0

FLASH1_LED1_MASK_RAMP_STATUS

Bits	Name	Description
7:0	LED1_MASK_CLIP_CURRENT	This register reads back LED1's current code when mask goes away,,,,'

0x0001D30C FLASH1_LED2_MASK_RAMP_STATUS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Valid only when MASK_RAMP_CTRL=0

FLASH1_LED2_MASK_RAMP_STATUS

Bits	Name	Description
7:0	LED2_MASK_CLIP_CURRENT	This register reads back LED2's current code when mask goes away,,,,'

0x0001D310 FLASH1_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Interrupt Real Time Status Bits

FLASH1_INT_RT_STS

Bits	Name	Description
7	FLSH_EXP_RT_STS	Flash Safety timer expiration
6	DOG_EXP_RT_STS	Video watchdog timer expiration
5	LED_FLT_RT_STS	LED fault (short/open/thrm drt/vreg_ok)
4	VPH_DROOP_RT_STS	low Vph_pwr detect (Vph_pwr < threshold)
3	LED1_RMP_UP_DONE_RT_STS	LED1 Flash current ramp up complete
2	LED1_RMP_DN_DONE_RT_STS	LED1 Flash current ramp down complete
1	LED2_RMP_UP_DONE_RT_STS	LED2 Flash current ramp up complete
0	LED2_RMP_DN_DONE_RT_STS	LED2 Flash current ramp down complete

0x0001D311 FLASH1_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

FLASH1_INT_SET_TYPE

Bits	Name	Description
7	FLSH_EXP_TYPE	0x0: LEVEL 0x1: EDGE
6	DOG_EXP_TYPE	0x0: LEVEL 0x1: EDGE
5	LED_FLT_TYPE	0x0: LEVEL 0x1: EDGE
4	VPH_DROOP_TYPE	0x0: LEVEL 0x1: EDGE
3	LED1_RMP_UP_DONE_TYPE	0x0: LEVEL 0x1: EDGE
2	LED1_RMP_DN_DONE_TYPE	0x0: LEVEL 0x1: EDGE
1	LED2_RMP_UP_DONE_TYPE	0x0: LEVEL 0x1: EDGE
0	LED2_RMP_DN_DONE_TYPE	0x0: LEVEL 0x1: EDGE

0x0001D312 FLASH1_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

FLASH1_INT_POLARITY_HIGH

Bits	Name	Description
7	FLSH_EXP_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

FLASH1_INT_POLARITY_HIGH (cont.)

Bits	Name	Description
6	DOG_EXP_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
5	LED_FLT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
4	VPH_DROOP_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
3	LED1_RMP_UP_DONE_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
2	LED1_RMP_DN_DONE_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
1	LED2_RMP_UP_DONE_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
0	LED2_RMP_DN_DONE_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x0001D313 FLASH1_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1 = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

FLASH1_INT_POLARITY_LOW

Bits	Name	Description
7	FLSH_EXP_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
6	DOG_EXP_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
5	LED_FLT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
4	VPH_DROOP_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
3	LED1_RMP_UP_DONE_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
2	LED1_RMP_DN_DONE_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

FLASH1_INT_POLARITY_LOW (cont.)

Bits	Name	Description
1	LED2_RMP_UP_DONE_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
0	LED2_RMP_DN_DONE_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x0001D314 FLASH1_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

FLASH1_INT_LATCHED_CLR

Bits	Name	Description
7	FLSH_EXP_LATCHED_CLR	
6	DOG_EXP_LATCHED_CLR	
5	LED_FLT_LATCHED_CLR	
4	VPH_DROOP_LATCHED_CLR	
3	LED1_RMP_UP_DONE_LATCHED_CLR	
2	LED1_RMP_DN_DONE_LATCHED_CLR	
1	LED2_RMP_UP_DONE_LATCHED_CLR	
0	LED2_RMP_DN_DONE_LATCHED_CLR	

0x0001D315 FLASH1_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

FLASH1_INT_EN_SET

Bits	Name	Description
7	FLSH_EXP_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
6	DOG_EXP_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
5	LED_FLT_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
4	VPH_DROOP_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
3	LED1_RMP_UP_DONE_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
2	LED1_RMP_DN_DONE_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
1	LED2_RMP_UP_DONE_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
0	LED2_RMP_DN_DONE_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED

0x0001D316 FLASH1_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

FLASH1_INT_EN_CLR

Bits	Name	Description
7	FLSH_EXP_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
6	DOG_EXP_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
5	LED_FLT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

FLASH1_INT_EN_CLR (cont.)

Bits	Name	Description
4	VPH_DROOP_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
3	LED1_RMP_UP_DONE_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
2	LED1_RMP_DN_DONE_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
1	LED2_RMP_UP_DONE_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
0	LED2_RMP_DN_DONE_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

0x0001D318 FLASH1_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

FLASH1_INT_LATCHED_STS

Bits	Name	Description
7	FLSH_EXP_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
6	DOG_EXP_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
5	LED_FLT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
4	VPH_DROOP_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
3	LED1_RMP_UP_DONE_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
2	LED1_RMP_DN_DONE_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
1	LED2_RMP_UP_DONE_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

FLASH1_INT_LATCHED_STS (cont.)

Bits	Name	Description
0	LED2_RMP_DN_DONE_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

0x0001D319 FLASH1_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

FLASH1_INT_PENDING_STS

Bits	Name	Description
7	FLSH_EXP_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
6	DOG_EXP_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
5	LED_FLT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
4	VPH_DROOP_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
3	LED1_RMP_UP_DONE_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
2	LED1_RMP_DN_DONE_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
1	LED2_RMP_UP_DONE_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
0	LED2_RMP_DN_DONE_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

0x0001D31A FLASH1_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

FLASH1_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x0001D31B FLASH1_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

SR=0 A=1

FLASH1_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR 0x1: A

0x0001D340 FLASH1_FLASH_SAFETY_TIMER

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x13

Reset Name: PERPH_RB

FLASH1_FLASH_SAFETY_TIMER

Bits	Name	Description
6:0	FLASH_TIMER_DURATION	Timer = 10ms * code + 10ms 00..0 = 10ms 11..1 = 1280ms 0x0: TIMER_10MS 0x1: TIMER_20MS 0x2: TIMER_30MS 0x3: TIMER_40MS 0x4: TIMER_50MS 0x5: TIMER_60MS 0x6: TIMER_70MS 0x7: TIMER_80MS 0x8: TIMER_90MS 0x9: TIMER_100MS 0xA: TIMER_110MS 0xB: TIMER_120MS 0xC: TIMER_130MS 0xD: TIMER_140MS 0xE: TIMER_150MS 0xF: TIMER_160MS 0x10: TIMER_170MS 0x11: TIMER_180MS 0x12: TIMER_190MS 0x13: TIMER_200MS 0x14: TIMER_210MS 0x15: TIMER_220MS 0x16: TIMER_230MS 0x17: TIMER_240MS 0x18: TIMER_250MS 0x19: TIMER_260MS 0x1A: TIMER_270MS 0x1B: TIMER_280MS 0x1C: TIMER_290MS 0x1D: TIMER_300MS 0x1E: TIMER_310MS 0x1F: TIMER_320MS 0x20: TIMER_330MS 0x21: TIMER_340MS 0x22: TIMER_350MS 0x23: TIMER_360MS 0x24: TIMER_370MS 0x25: TIMER_380MS 0x26: TIMER_390MS 0x27: TIMER_400MS 0x28: TIMER_410MS 0x29: TIMER_420MS

FLASH1_FLASH_SAFETY_TIMER (cont.)

Bits	Name	Description
		0x2A: TIMER_430MS 0x2B: TIMER_440MS 0x2C: TIMER_450MS 0x2D: TIMER_460MS 0x2E: TIMER_470MS 0x2F: TIMER_480MS 0x30: TIMER_490MS 0x31: TIMER_500MS 0x32: TIMER_510MS 0x33: TIMER_520MS 0x34: TIMER_530MS 0x35: TIMER_540MS 0x36: TIMER_550MS 0x37: TIMER_560MS 0x38: TIMER_570MS 0x39: TIMER_580MS 0x3A: TIMER_590MS 0x3B: TIMER_600MS 0x3C: TIMER_610MS 0x3D: TIMER_620MS 0x3E: TIMER_630MS 0x3F: TIMER_640MS 0x40: TIMER_650MS 0x41: TIMER_660MS 0x42: TIMER_670MS 0x43: TIMER_680MS 0x44: TIMER_690MS 0x45: TIMER_700MS 0x46: TIMER_710MS 0x47: TIMER_720MS 0x48: TIMER_730MS 0x49: TIMER_740MS 0x4A: TIMER_750MS 0x4B: TIMER_760MS 0x4C: TIMER_770MS 0x4D: TIMER_780MS 0x4E: TIMER_790MS 0x4F: TIMER_800MS 0x50: TIMER_810MS 0x51: TIMER_820MS 0x52: TIMER_830MS 0x53: TIMER_840MS 0x54: TIMER_850MS 0x55: TIMER_860MS 0x56: TIMER_870MS

FLASH1_FLASH_SAFETY_TIMER (cont.)

Bits	Name	Description
		0x57: TIMER_880MS 0x58: TIMER_890MS 0x59: TIMER_900MS 0x5A: TIMER_910MS 0x5B: TIMER_920MS 0x5C: TIMER_930MS 0x5D: TIMER_940MS 0x5E: TIMER_950MS 0x5F: TIMER_960MS 0x60: TIMER_970MS 0x61: TIMER_980MS 0x62: TIMER_990MS 0x63: TIMER_1000MS 0x64: TIMER_1010MS 0x65: TIMER_1020MS 0x66: TIMER_1030MS 0x67: TIMER_1040MS 0x68: TIMER_1050MS 0x69: TIMER_1060MS 0x6A: TIMER_1070MS 0x6B: TIMER_1080MS 0x6C: TIMER_1090MS 0x6D: TIMER_1100MS 0x6E: TIMER_1110MS 0x6F: TIMER_1120MS 0x70: TIMER_1130MS 0x71: TIMER_1140MS 0x72: TIMER_1150MS 0x73: TIMER_1160MS 0x74: TIMER_1170MS 0x75: TIMER_1180MS 0x76: TIMER_1190MS 0x77: TIMER_1200MS 0x78: TIMER_1210MS 0x79: TIMER_1220MS 0x7A: TIMER_1230MS 0x7B: TIMER_1240MS 0x7C: TIMER_1250MS 0x7D: TIMER_1260MS 0x7E: TIMER_1270MS 0x7F: TIMER_1280MS

0x0001D341 FLASH1_MAX_FLSH_CURRENT

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

This is a quick, one register setting to limit the flash current for flash LEDs with different current rating capability

led current <= min(max flash current, programmed current)

FLASH1_MAX_FLSH_CURRENT

Bits	Name	Description
7:0	MAX_LED_CURRENT	00 - 4F : 12.5mA / LSB 00 = 12.5mA extra codes are reserved 0x0: MAX_FLSH_12P5MA 0x1: MAX_FLSH_25MA 0x2: MAX_FLSH_37P5MA 0x3: MAX_FLSH_50MA 0x4: MAX_FLSH_62P5MA 0x5: MAX_FLSH_75MA 0x6: MAX_FLSH_87P5MA 0x7: MAX_FLSH_100MA 0x8: MAX_FLSH_112P5MA 0x9: MAX_FLSH_125MA 0xA: MAX_FLSH_137P5MA 0xB: MAX_FLSH_150MA 0xC: MAX_FLSH_162P5MA 0xD: MAX_FLSH_175MA 0xE: MAX_FLSH_187P5MA 0xF: MAX_FLSH_200MA 0x10: MAX_FLSH_212P5MA 0x11: MAX_FLSH_225MA 0x12: MAX_FLSH_237P5MA 0x13: MAX_FLSH_250MA 0x14: MAX_FLSH_262P5MA 0x15: MAX_FLSH_275MA 0x16: MAX_FLSH_287P5MA 0x17: MAX_FLSH_300MA 0x18: MAX_FLSH_312P5MA 0x19: MAX_FLSH_325MA 0x1A: MAX_FLSH_337P5MA 0x1B: MAX_FLSH_350MA 0x1C: MAX_FLSH_362P5MA 0x1D: MAX_FLSH_375MA 0x1E: MAX_FLSH_387P5MA 0x1F: MAX_FLSH_400MA 0x20: MAX_FLSH_412P5MA 0x21: MAX_FLSH_425MA 0x22: MAX_FLSH_437P5MA 0x23: MAX_FLSH_450MA 0x24: MAX_FLSH_462P5MA 0x25: MAX_FLSH_475MA 0x26: MAX_FLSH_487P5MA 0x27: MAX_FLSH_500MA 0x28: MAX_FLSH_512P5MA 0x29: MAX_FLSH_525MA

FLASH1_MAX_FLSH_CURRENT (cont.)

Bits	Name	Description
		0x2A: MAX_FLSH_537P5MA 0x2B: MAX_FLSH_550MA 0x2C: MAX_FLSH_562P5MA 0x2D: MAX_FLSH_575MA 0x2E: MAX_FLSH_587P5MA 0x2F: MAX_FLSH_600MA 0x30: MAX_FLSH_612P5MA 0x31: MAX_FLSH_625MA 0x32: MAX_FLSH_637P5MA 0x33: MAX_FLSH_650MA 0x34: MAX_FLSH_662P5MA 0x35: MAX_FLSH_675MA 0x36: MAX_FLSH_687P5MA 0x37: MAX_FLSH_700MA 0x38: MAX_FLSH_712P5MA 0x39: MAX_FLSH_725MA 0x3A: MAX_FLSH_737P5MA 0x3B: MAX_FLSH_750MA 0x3C: MAX_FLSH_762P5MA 0x3D: MAX_FLSH_775MA 0x3E: MAX_FLSH_787P5MA 0x3F: MAX_FLSH_800MA 0x40: MAX_FLSH_812P5MA 0x41: MAX_FLSH_825MA 0x42: MAX_FLSH_837P5MA 0x43: MAX_FLSH_850MA 0x44: MAX_FLSH_862P5MA 0x45: MAX_FLSH_875MA 0x46: MAX_FLSH_887P5MA 0x47: MAX_FLSH_900MA 0x48: MAX_FLSH_912P5MA 0x49: MAX_FLSH_925MA 0x4A: MAX_FLSH_937P5MA 0x4B: MAX_FLSH_950MA 0x4C: MAX_FLSH_962P5MA 0x4D: MAX_FLSH_975MA 0x4E: MAX_FLSH_987P5MA 0x4F: MAX_FLSH_1000MA

0x0001D342 FLASH1_LED1_CURRENT_PRGM

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Target current for LED1

FLASH1_LED1_CURRENT_PRGM

Bits	Name	Description
7:0	LED1_CURRENT_CONTROL	00 - 4F : 12.5mA / LSB 00 = 12.5mA extra codes are reserved 0x0: FLSH1_CURR_12P5MA 0x1: FLSH1_CURR_25MA 0x2: FLSH1_CURR_37P5MA 0x3: FLSH1_CURR_50MA 0x4: FLSH1_CURR_62P5MA 0x5: FLSH1_CURR_75MA 0x6: FLSH1_CURR_87P5MA 0x7: FLSH1_CURR_100MA 0x8: FLSH1_CURR_112P5MA 0x9: FLSH1_CURR_125MA 0xA: FLSH1_CURR_137P5MA 0xB: FLSH1_CURR_150MA 0xC: FLSH1_CURR_162P5MA 0xD: FLSH1_CURR_175MA 0xE: FLSH1_CURR_187P5MA 0xF: FLSH1_CURR_200MA 0x10: FLSH1_CURR_212P5MA 0x11: FLSH1_CURR_225MA 0x12: FLSH1_CURR_237P5MA 0x13: FLSH1_CURR_250MA 0x14: FLSH1_CURR_262P5MA 0x15: FLSH1_CURR_275MA 0x16: FLSH1_CURR_287P5MA 0x17: FLSH1_CURR_300MA 0x18: FLSH1_CURR_312P5MA 0x19: FLSH1_CURR_325MA 0x1A: FLSH1_CURR_337P5MA 0x1B: FLSH1_CURR_350MA 0x1C: FLSH1_CURR_362P5MA 0x1D: FLSH1_CURR_375MA 0x1E: FLSH1_CURR_387P5MA 0x1F: FLSH1_CURR_400MA 0x20: FLSH1_CURR_412P5MA 0x21: FLSH1_CURR_425MA 0x22: FLSH1_CURR_437P5MA 0x23: FLSH1_CURR_450MA 0x24: FLSH1_CURR_462P5MA 0x25: FLSH1_CURR_475MA 0x26: FLSH1_CURR_487P5MA 0x27: FLSH1_CURR_500MA 0x28: FLSH1_CURR_512P5MA

FLASH1_LED1_CURRENT_PRGM (cont.)

Bits	Name	Description
		0x29: FLSH1_CURR_525MA
		0x2A: FLSH1_CURR_537P5MA
		0x2B: FLSH1_CURR_550MA
		0x2C: FLSH1_CURR_562P5MA
		0x2D: FLSH1_CURR_575MA
		0x2E: FLSH1_CURR_587P5MA
		0x2F: FLSH1_CURR_600MA
		0x30: FLSH1_CURR_612P5MA
		0x31: FLSH1_CURR_625MA
		0x32: FLSH1_CURR_637P5MA
		0x33: FLSH1_CURR_650MA
		0x34: FLSH1_CURR_662P5MA
		0x35: FLSH1_CURR_675MA
		0x36: FLSH1_CURR_687P5MA
		0x37: FLSH1_CURR_700MA
		0x38: FLSH1_CURR_712P5MA
		0x39: FLSH1_CURR_725MA
		0x3A: FLSH1_CURR_737P5MA
		0x3B: FLSH1_CURR_750MA
		0x3C: FLSH1_CURR_762P5MA
		0x3D: FLSH1_CURR_775MA
		0x3E: FLSH1_CURR_787P5MA
		0x3F: FLSH1_CURR_800MA
		0x40: FLSH1_CURR_812P5MA
		0x41: FLSH1_CURR_825MA
		0x42: FLSH1_CURR_837P5MA
		0x43: FLSH1_CURR_850MA
		0x44: FLSH1_CURR_862P5MA
		0x45: FLSH1_CURR_875MA
		0x46: FLSH1_CURR_887P5MA
		0x47: FLSH1_CURR_900MA
		0x48: FLSH1_CURR_912P5MA
		0x49: FLSH1_CURR_925MA
		0x4A: FLSH1_CURR_937P5MA
		0x4B: FLSH1_CURR_950MA
		0x4C: FLSH1_CURR_962P5MA
		0x4D: FLSH1_CURR_975MA
		0x4E: FLSH1_CURR_987P5MA
		0x4F: FLSH1_CURR_1000MA

0x0001D343 FLASH1_LED2_CURRENT_PRGM

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Target current for LED2

FLASH1_LED2_CURRENT_PRGM

Bits	Name	Description
7:0	LED2_CURRENT_CONTROL	00 - 4F : 12.5mA / LSB 00 = 12.5mA extra codes are reserved 0x0: FLSH2_CURR_12P5MA 0x1: FLSH2_CURR_25MA 0x2: FLSH2_CURR_37P5MA 0x3: FLSH2_CURR_50MA 0x4: FLSH2_CURR_62P5MA 0x5: FLSH2_CURR_75MA 0x6: FLSH2_CURR_87P5MA 0x7: FLSH2_CURR_100MA 0x8: FLSH2_CURR_112P5MA 0x9: FLSH2_CURR_125MA 0xA: FLSH2_CURR_137P5MA 0xB: FLSH2_CURR_150MA 0xC: FLSH2_CURR_162P5MA 0xD: FLSH2_CURR_175MA 0xE: FLSH2_CURR_187P5MA 0xF: FLSH2_CURR_200MA 0x10: FLSH2_CURR_212P5MA 0x11: FLSH2_CURR_225MA 0x12: FLSH2_CURR_237P5MA 0x13: FLSH2_CURR_250MA 0x14: FLSH2_CURR_262P5MA 0x15: FLSH2_CURR_275MA 0x16: FLSH2_CURR_287P5MA 0x17: FLSH2_CURR_300MA 0x18: FLSH2_CURR_312P5MA 0x19: FLSH2_CURR_325MA 0x1A: FLSH2_CURR_337P5MA 0x1B: FLSH2_CURR_350MA 0x1C: FLSH2_CURR_362P5MA 0x1D: FLSH2_CURR_375MA 0x1E: FLSH2_CURR_387P5MA 0x1F: FLSH2_CURR_400MA 0x20: FLSH2_CURR_412P5MA 0x21: FLSH2_CURR_425MA 0x22: FLSH2_CURR_437P5MA 0x23: FLSH2_CURR_450MA 0x24: FLSH2_CURR_462P5MA 0x25: FLSH2_CURR_475MA 0x26: FLSH2_CURR_487P5MA 0x27: FLSH2_CURR_500MA 0x28: FLSH2_CURR_512P5MA 0x29: FLSH2_CURR_525MA

FLASH1_LED2_CURRENT_PRGM (cont.)

Bits	Name	Description
		0x2A: FLSH2_CURR_537P5MA 0x2B: FLSH2_CURR_550MA 0x2C: FLSH2_CURR_562P5MA 0x2D: FLSH2_CURR_575MA 0x2E: FLSH2_CURR_587P5MA 0x2F: FLSH2_CURR_600MA 0x30: FLSH2_CURR_612P5MA 0x31: FLSH2_CURR_625MA 0x32: FLSH2_CURR_637P5MA 0x33: FLSH2_CURR_650MA 0x34: FLSH2_CURR_662P5MA 0x35: FLSH2_CURR_675MA 0x36: FLSH2_CURR_687P5MA 0x37: FLSH2_CURR_700MA 0x38: FLSH2_CURR_712P5MA 0x39: FLSH2_CURR_725MA 0x3A: FLSH2_CURR_737P5MA 0x3B: FLSH2_CURR_750MA 0x3C: FLSH2_CURR_762P5MA 0x3D: FLSH2_CURR_775MA 0x3E: FLSH2_CURR_787P5MA 0x3F: FLSH2_CURR_800MA 0x40: FLSH2_CURR_812P5MA 0x41: FLSH2_CURR_825MA 0x42: FLSH2_CURR_837P5MA 0x43: FLSH2_CURR_850MA 0x44: FLSH2_CURR_862P5MA 0x45: FLSH2_CURR_875MA 0x46: FLSH2_CURR_887P5MA 0x47: FLSH2_CURR_900MA 0x48: FLSH2_CURR_912P5MA 0x49: FLSH2_CURR_925MA 0x4A: FLSH2_CURR_937P5MA 0x4B: FLSH2_CURR_950MA 0x4C: FLSH2_CURR_962P5MA 0x4D: FLSH2_CURR_975MA 0x4E: FLSH2_CURR_987P5MA 0x4F: FLSH2_CURR_1000MA

0x0001D344 FLASH1_MASK_CLAMP_CURRENT

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x0F

Reset Name: PERPH_RB

Mask clamp current is applied to each LED driver.

For e.g, if max clamp current = 150mA

AND if flash driver = 700mA and video driver = 200mA

then both flash driver and video driver will be reduced to 150mA EACH.

This has to be the case since there is only (1) programming table for each LED channel

and LED current ramp down follows the programming table

FLASH1_MASK_CLAMP_CURRENT

Bits	Name	Description
7:0	MASK_CURRENT	00 - 4F : 12.5mA / LSB 00 = 12.5mA extra codes are reserved 0x0: CLAMP_CURR_12P5MA 0x1: CLAMP_CURR_25MA 0x2: CLAMP_CURR_37P5MA 0x3: CLAMP_CURR_50MA 0x4: CLAMP_CURR_62P5MA 0x5: CLAMP_CURR_75MA 0x6: CLAMP_CURR_87P5MA 0x7: CLAMP_CURR_100MA 0x8: CLAMP_CURR_112P5MA 0x9: CLAMP_CURR_125MA 0xA: CLAMP_CURR_137P5MA 0xB: CLAMP_CURR_150MA 0xC: CLAMP_CURR_162P5MA 0xD: CLAMP_CURR_175MA 0xE: CLAMP_CURR_187P5MA 0xF: CLAMP_CURR_200MA 0x10: CLAMP_CURR_212P5MA 0x11: CLAMP_CURR_225MA 0x12: CLAMP_CURR_237P5MA 0x13: CLAMP_CURR_250MA 0x14: CLAMP_CURR_262P5MA 0x15: CLAMP_CURR_275MA 0x16: CLAMP_CURR_287P5MA 0x17: CLAMP_CURR_300MA 0x18: CLAMP_CURR_312P5MA 0x19: CLAMP_CURR_325MA 0x1A: CLAMP_CURR_337P5MA 0x1B: CLAMP_CURR_350MA 0x1C: CLAMP_CURR_362P5MA 0x1D: CLAMP_CURR_375MA 0x1E: CLAMP_CURR_387P5MA 0x1F: CLAMP_CURR_400MA 0x20: CLAMP_CURR_412P5MA 0x21: CLAMP_CURR_425MA 0x22: CLAMP_CURR_437P5MA 0x23: CLAMP_CURR_450MA 0x24: CLAMP_CURR_462P5MA 0x25: CLAMP_CURR_475MA 0x26: CLAMP_CURR_487P5MA 0x27: CLAMP_CURR_500MA 0x28: CLAMP_CURR_512P5MA 0x29: CLAMP_CURR_525MA

FLASH1_MASK_CLAMP_CURRENT (cont.)

Bits	Name	Description
		0x2A: CLAMP_CURR_537P5MA 0x2B: CLAMP_CURR_550MA 0x2C: CLAMP_CURR_562P5MA 0x2D: CLAMP_CURR_575MA 0x2E: CLAMP_CURR_587P5MA 0x2F: CLAMP_CURR_600MA 0x30: CLAMP_CURR_612P5MA 0x31: CLAMP_CURR_625MA 0x32: CLAMP_CURR_637P5MA 0x33: CLAMP_CURR_650MA 0x34: CLAMP_CURR_662P5MA 0x35: CLAMP_CURR_675MA 0x36: CLAMP_CURR_687P5MA 0x37: CLAMP_CURR_700MA 0x38: CLAMP_CURR_712P5MA 0x39: CLAMP_CURR_725MA 0x3A: CLAMP_CURR_737P5MA 0x3B: CLAMP_CURR_750MA 0x3C: CLAMP_CURR_762P5MA 0x3D: CLAMP_CURR_775MA 0x3E: CLAMP_CURR_787P5MA 0x3F: CLAMP_CURR_800MA 0x40: CLAMP_CURR_812P5MA 0x41: CLAMP_CURR_825MA 0x42: CLAMP_CURR_837P5MA 0x43: CLAMP_CURR_850MA 0x44: CLAMP_CURR_862P5MA 0x45: CLAMP_CURR_875MA 0x46: CLAMP_CURR_887P5MA 0x47: CLAMP_CURR_900MA 0x48: CLAMP_CURR_912P5MA 0x49: CLAMP_CURR_925MA 0x4A: CLAMP_CURR_937P5MA 0x4B: CLAMP_CURR_950MA 0x4C: CLAMP_CURR_962P5MA 0x4D: CLAMP_CURR_975MA 0x4E: CLAMP_CURR_987P5MA 0x4F: CLAMP_CURR_1000MA

0x0001D346 FLASH1_ENABLE_CONTROL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x60

Reset Name: PERPH_RB

FLASH1_ENABLE_CONTROL

Bits	Name	Description
7	MODULE_ENABLE	0 = Module disable 1 = Module enable 0x0: MOD_DIS 0x1: MOD_EN
6	LED1_DRVR_SEL	0 = Enable 200mA flash / video driver, total current = 200mA/LED max, source is VIN_5V 1 = Enable 1A flash driver, total current = 1000mA / LED max, source is VIN_FLASH 0x0: TORCH_EN 0x1: FLASH_EN
5	LED2_DRVR_SEL	0 = Enable 200mA flash / video driver, total current = 200mA/LED max, source is VIN_5V 1 = Enable 1A flash driver, total current = 1000mA / LED max, source is VIN_FLASH 0x0: TORCH_EN 0x1: FLASH_EN

0x0001D347 FLASH1_LED_STROBE_CONTROL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

SW strobe and enable is the desired method of controlling flash

For legacy support a HW strobe is provided. The HW strobe is common to both LEDs

SW output enable takes priority over HW strobe.

HW strobing :

1. Select HW strobe as part of initialization when the module is enabled.

2. Enable the LED(s)

3. The LED(s) current will ramp up when HW strobe is asserted.

4. The LED(s) current will ramp down when HW strobe is deasserted

5. Disable the LED(s)

When the strobe is level triggered, the flash current is active as long as the strobe level is active or the flash safety timer expires.

When the strobe is edge triggered, flash current is deactivated when the flash safety timer expires

SW strobing (POR) :

1. Select SW strobe as part of init when the module is enabled

2. Enable the LED(s). The current starts to ramp up right away

3. Disable the LED(s). The current will ramp down right away

Strobe EN_LED1 EN_LED2 Results

0 0 0 No current

1 0 0 No current even if HW strobe arrives since LED current sources are not enabled

1 1 1 HW strobe : When HW strobe arrives, the LED current output starts

0 1 1 SW strobe : Output current starts immediately after the EN_LED1/2 bits are written

FLASH1_LED_STROBE_CONTROL

Bits	Name	Description
7	EN_LED1_OUTPUT	0 = Disable LED1 current output 1 = Enable LED1 current output 0x0: LED1_DIS 0x1: LED1_EN
6	EN_LED2_OUTPUT	0 = Disable LED2 current output 1 = Enable LED2 current output 0x0: LED2_DIS 0x1: LED2_EN
2	HW_SW_STROBE_SEL	0 = SW strobe 1 = HW strobe 0x0: STROBE_SW 0x1: STROBE_HW
1	HW_STROBE_TRIGGER	0 = level triggered 1 = edge triggered 0x0: LEVEL 0x1: EDGE
0	HW_STROBE_POLARITY	0 = active_low / falling edge 1 = active high / rising edge 0x0: ACTIVE_LOW 0x1: ACTIVE_HIGH

0x0001D348 FLASH1_LED_TMR_CONTROL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

FLASH1_LED_TMR_CONTROL

Bits	Name	Description
1	TIMER1_SEL	0 = Enable flash timer for LED1 1 = Enable watchdog timer for LED1 0x0: LED1_TIMER_FLASH 0x1: LED1_TIMER_WTCHDG
0	TIMER2_SEL	0 = Enable flash timer for LED2 1 = Enable watchdog timer for LED2 0x0: LED2_TIMER_FLASH 0x1: LED2_TIMER_WTCHDG

0x0001D349 FLASH1_WATCHDOG_TIMER

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x0A

Reset Name: PERPH_RB

FLASH1_WATCHDOG_TIMER

Bits	Name	Description
4:0	WATCHDOG_TIMER_DURATION	Timer = 1sec * code + 2 sec 00..0 = 2s 11..1 = 33s 0x0: WTCHDG_TIME_2S 0x1: WTCHDG_TIME_3S 0x2: WTCHDG_TIME_4S 0x3: WTCHDG_TIME_5S 0x4: WTCHDG_TIME_6S 0x5: WTCHDG_TIME_7S 0x6: WTCHDG_TIME_8S 0x7: WTCHDG_TIME_9S 0x8: WTCHDG_TIME_10S 0x9: WTCHDG_TIME_11S 0xA: WTCHDG_TIME_12S 0xB: WTCHDG_TIME_13S 0xC: WTCHDG_TIME_14S 0xD: WTCHDG_TIME_15S 0xE: WTCHDG_TIME_16S 0xF: WTCHDG_TIME_17S 0x10: WTCHDG_TIME_18S 0x11: WTCHDG_TIME_19S 0x12: WTCHDG_TIME_20S 0x13: WTCHDG_TIME_21S 0x14: WTCHDG_TIME_22S 0x15: WTCHDG_TIME_23S 0x16: WTCHDG_TIME_24S 0x17: WTCHDG_TIME_25S 0x18: WTCHDG_TIME_26S 0x19: WTCHDG_TIME_27S 0x1A: WTCHDG_TIME_28S 0x1B: WTCHDG_TIME_29S 0x1C: WTCHDG_TIME_30S 0x1D: WTCHDG_TIME_31S 0x1E: WTCHDG_TIME_32S 0x1F: WTCHDG_TIME_33S

0x0001D34C FLASH1_MASK_ENABLE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

FLASH1_MASK_ENABLE

Bits	Name	Description
7	EN_MASK3	0 = disable mask3 1 = enable mask3 to force flash current to mask clamp current 0x0: MASK3_DIS 0x1: MASK3_EN
6	EN_MASK2	0 = disable mask2 1 = enable mask2 to force flash current to mask clamp current 0x0: MASK2_DIS 0x1: MASK2_EN
5	EN_MASK1	0 = disable mask1 (same as TX_GTR_THRES mask) 1 = enable mask1 to force flash current to mask clamp current 0x0: VPH_DROOP_DIS 0x1: VPH_DROOP_EN

0x0001D34D FLASH1_LED1_FINE_CURRENT_PRGM

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

This current is added to the LED1 current set in Register 0x42

FLASH1_LED1_FINE_CURRENT_PRGM

Bits	Name	Description
3:0	LED1_FINE_CURRENT_CONTROL	0000 = 0mA 0001 = 1mA 0010 = 2mA 0100 = 4mA 1000 = 8mA 0x0: LED1_FINE_CURR_0MA 0x1: LED1_FINE_CURR_1MA 0x2: LED1_FINE_CURR_2MA 0x4: LED1_FINE_CURR_4MA 0x8: LED1_FINE_CURR_8MA

0x0001D34E FLASH1_LED2_FINE_CURRENT_PRGM

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

This current is added to the LED2 current set in Register 0x43

FLASH1_LED2_FINE_CURRENT_PRGM

Bits	Name	Description
3:0	LED2_FINE_CURRENT_CONTROL	0000 = 0mA 0001 = 1mA 0010 = 2mA 0100 = 4mA 1000 = 8mA 0x0: LED2_FINE_CURR_0MA 0x1: LED2_FINE_CURR_1MA 0x2: LED2_FINE_CURR_2MA 0x4: LED2_FINE_CURR_4MA 0x8: LED2_FINE_CURR_8MA

0x0001D350 FLASH1_MASK_CONFIG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x07

Reset Name: PERPH_RB

FLASH1_MASK_CONFIG

Bits	Name	Description
2	MASK3_POLARITY	0 = mask3 is active low 1 = mask3 is active high 0x0: MASK3_ACTIVE_LOW 0x1: MASK3_ACTIVE_HIGH
1	MASK2_POLARITY	0 = mask2 is active low 1 = mask2 is active high 0x0: MASK2_ACTIVE_LOW 0x1: MASK2_ACTIVE_HIGH
0	MASK1_POLARITY	0 = mask1 is active low 1 = mask1 is active high 0x0: MASK1_ACTIVE_LOW 0x1: MASK1_ACTIVE_HIGH

0x0001D351 FLASH1_FAULT_DETECT

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x80

Reset Name: PERPH_RB

FLASH1_FAULT_DETECT

Bits	Name	Description
7	EN_SELF_CHECK	0 = disable self check 1 = enable self check 0x0: SELF_CHECK_DIS 0x1: SELF_CHECK_EN

0x0001D352 FLASH1_THERMAL_DERATE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x82

Reset Name: PERPH_RB

FLASH1_THERMAL_DERATE

Bits	Name	Description
7	EN_THERMAL_DERATE	0 = disable internal thermal derating 1 = enable internal thermal derating 0x0: THERM_DERATE_DIS 0x1: THERM_DERATE
5:3	DERATE_RATE	000 = 1% per deg C 001 = 1.25% per deg C 010 = 2% per deg C 011 = 2.5% per deg C 100 = 5% per deg C 101 = reserved 110 = reserved 111 = reserved 0x0: RATE_1_PERCENT 0x1: RATE_1P25_PERCENT 0x2: RATE_2_PERCENT 0x3: RATE_2P5_PERCENT 0x4: RATE_5_PERCENT

FLASH1_THERMAL_DERATE (cont.)

Bits	Name	Description
2:0	DERATE_THRESHOLD	000 = 95C 001 = 105C 010 = 115C 011 = 125C 101 = reserved 110 = reserved 111 = reserved 0x0: THRESHOLD_95C 0x1: THRESHOLD_105C 0x2: THRESHOLD_115C 0x3: THRESHOLD_125C

0x0001D354 FLASH1_LED_CURRENT_RAMP

Type: RW
Clock: PBUS_WRCLK
Reset State: 0xAD

Reset Name: PERPH_RB

When MASK1 is enabled and is active or on a fault, the ramp down setting is overridden by 'ALT_RAMP_DN' register at any given time in the flash event

FLASH1_LED_CURRENT_RAMP

Bits	Name	Description
7	EN_RAMP	0 = no ramp, this is a step change in current, not recommended for actual operation 1 =use ramp programmed settings 0x0: RAMP_DIS 0x1: RAMP_EN

FLASH1_LED_CURRENT_RAMP (cont.)

Bits	Name	Description
5:3	RAMP_UP_STEP	000 = 0.2us 001 = 0.4us 010 = 0.8us 011 = 1.6us 100 = 3.3us 101 = 6.7us 110 = 13.5us 111 = 27us 0x0: RAMP_UP_STEP_0P2US 0x1: RAMP_UP_STEP_0P4US 0x2: RAMP_UP_STEP_0P8US 0x3: RAMP_UP_STEP_1P6US 0x4: RAMP_UP_STEP_3P3US 0x5: RAMP_UP_STEP_6P7US 0x6: RAMP_UP_STEP_13P5US 0x7: RAMP_UP_STEP_27US
2:0	RAMP_DN_STEP	000 = 0.2us 001 = 0.4us 010 = 0.8us 011 = 1.6us 100 = 3.3us 101 = 6.7us 110 = 13.5us 111 = 27us 0x0: RAMP_DN_STEP_0P2US 0x1: RAMP_DN_STEP_0P4US 0x2: RAMP_DN_STEP_0P8US 0x3: RAMP_DN_STEP_1P6US 0x4: RAMP_DN_STEP_3P3US 0x5: RAMP_DN_STEP_6P7US 0x6: RAMP_DN_STEP_13P5US 0x7: RAMP_DN_STEP_27US

0x0001D355 FLASH1_ALT_RAMP_DN

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x03

Reset Name: PERPH_RB

This is the ramp rate used whenever the TX_GTR_THRES mask (mask 1) is active or on a fault condition (open/short/'bst_pwr_ok'=0)

FLASH1_ALT_RAMP_DN

Bits	Name	Description
1:0	ALTERNATE_RAMP_DN	00 = 0.2us 01 = 0.4us 10 = 0.8us 11 = 1.6us 0x0: ALT_RMP_DWN_0P2US 0x1: ALT_RMP_DWN_0P4US 0x2: ALT_RMP_DWN_0P8US 0x3: ALT_RMP_DWN_1P6US

0x0001D356 FLASH1_WATCHDOG_PET

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

FLASH1_WATCHDOG_PET

Bits	Name	Description
7	PET_WATCHDOG	1 = reset watchdog timer This register needs to be auto clearing. After the register bit is written to, it goes back to logic 0 Reading this register will give back logic 0

0x0001D35A FLASH1_VPH_PWR_DROOP

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: PERPH_RB

FLASH1_VPH_PWR_DROOP

Bits	Name	Description
7	EN_VPH_PWR_DROOP	0 = do not use this feature 1 = enable this feature 0x0: VPH_DROOP_DIS 0x1: VPHDROOP_EN

FLASH1_VPH_PWR_DROOP (cont.)

Bits	Name	Description
6:4	VPH_PWR_DROOP_THRESHOLD	000 = 2.5V 001 = 2.6V 010 = 2.7V 011 = 2.8V 100 = 2.9V 101 = 3.0V 110 = 3.1V 111 = 3.2V 0x0: VDIP_THRES_2P5V 0x1: VDIP_THRES_2P6V 0x2: VDIP_THRES_2P7V 0x3: VDIP_THRES_2P8V 0x4: VDIP_THRES_2P9V 0x5: VDIP_THRES_3V 0x6: VDIP_THRES_3P1V 0x7: VDIP_THRES_3P2V
1:0	DEBOUNCE_TIME_VPH_PWR_DROOP	00 = 0us 01 = 10us 10 = 32us 11 = 64us 0x0: VPH_DROOP_DEBOUNCE_0US 0x1: VPH_DROOP_DEBOUNCE_10US 0x2: VPH_DROOP_DEBOUNCE_32US 0x3: VPH_DROOP_DEBOUNCE_64US

0x0001D35B FLASH1_MASK_RAMP_CTRL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: PERPH_RB

Applies to all masks

FLASH1_MASK_RAMP_CTRL

Bits	Name	Description
0	MASK_RAMP_CTRL	0 = do not ramp up after MASK is de-asserted 1 = ramp up after MASK is de-asserted 0x0: MASK_RAMP_DIS 0x1: MASK_RAMP_EN

24 WLED1_CTRL_WLED_CTRL

0x0001D800 WLED1_CTRL_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

WLED1_CTRL_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x0001D801 WLED1_CTRL_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

WLED1_CTRL_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x0001D802 WLED1_CTRL_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

WLED1_CTRL_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x0001D803 WLED1_CTRL_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: N/A

HW Version Register [31:24]

WLED1_CTRL_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x0001D804 WLED1_CTRL_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x17

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

WLED1_CTRL_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	WLED

0x0001D805 WLED1_CTRL_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x10

Reset Name: N/A

Peripheral SubType

WLED1_CTRL_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	WLED_CTRL

0x0001D808 WLED1_CTRL_FAULT_STATUS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x08

Reset Name: N/A

Status Register

WLED1_CTRL_FAULT_STATUS

Bits	Name	Description
3	RFU1	
2	SC_FAULT	0 = no fault 1 = Short circuit condition detected
1	OVP_FAULT	0 = no fault 1 = Over-voltage condition detected
0	RFU0	

0x0001D810 WLED1_CTRL_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Interrupt Real Time Status Bits

WLED1_CTRL_INT_RT_STS

Bits	Name	Description
2	SC_FAULT_RT_STS	
1	OVP_FAULT_RT_STS	
0	RFU	

0x0001D811 WLED1_CTRL_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

WLED1_CTRL_INT_SET_TYPE

Bits	Name	Description
2	SC_FAULT_TYPE	
1	OVP_FAULT_TYPE	
0	RFU	This bit should always be programmed 0

0x0001D812 WLED1_CTRL_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

WLED1_CTRL_INT_POLARITY_HIGH

Bits	Name	Description
2	SC_FAULT_HIGH	
1	OVP_FAULT_HIGH	
0	RFU	This bit should always be programmed 0

0x0001D813 WLED1_CTRL_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

WLED1_CTRL_INT_POLARITY_LOW

Bits	Name	Description
2	SC_FAULT_LOW	
1	OVP_FAULT_LOW	
0	RFU	This bit should always be programmed 0

0x0001D814 WLED1_CTRL_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

WLED1_CTRL_INT_LATCHED_CLR

Bits	Name	Description
2	SC_FAULT_LATCHED_CLR	
1	OVP_FAULT_LATCHED_CLR	
0	RFU	This bit should always be programmed 0

0x0001D815 WLED1_CTRL_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

WLED1_CTRL_INT_EN_SET

Bits	Name	Description
2	SC_FAULT_EN_SET	
1	OVP_FAULT_EN_SET	
0	RFU	This bit should always be programmed 0

0x0001D816 WLED1_CTRL_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

WLED1_CTRL_INT_EN_CLR

Bits	Name	Description
2	SC_FAULT_EN_CLR	
1	OVP_FAULT_EN_CLR	
0	RFU	This bit should always be programmed 0

0x0001D818 WLED1_CTRL_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

WLED1_CTRL_INT_LATCHED_STS

Bits	Name	Description
2	SC_FAULT_LATCHED_STS	
1	OVP_FAULT_LATCHED_STS	
0	RFU	

0x0001D819 WLED1_CTRL_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Debug: Pending is set if interrupt has been sent but not cleared.

WLED1_CTRL_INT_PENDING_STS

Bits	Name	Description
2	SC_FAULT_PENDING_STS	
1	OVP_FAULT_PENDING_STS	
0	RFU	

0x0001D81A WLED1_CTRL_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

WLED1_CTRL_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	

0x0001D81B WLED1_CTRL_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

SR=0 A=1

WLED1_CTRL_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	

0x0001D846 WLED1_CTRL_MODULE_ENABLE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

WLED1_CTRL_MODULE_ENABLE

Bits	Name	Description
7	EN_MODULE	0 = module disable. Lowest power state of module. Shuts down analog and digital. No clock requests. Overrides other bits of this register. 1 = Module enable. Boost is active even if current sinks are disabled

0x0001D848 WLED1_CTRL_FEEDBACK_CONTROL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Forces selection of LED output as feedback node for the Boost

WLED1_CTRL_FEEDBACK_CONTROL

Bits	Name	Description
2:0	FEEDBACK_CONTROL	0d, 5d, 6d, 7d = automatic selection = min(WLED1,WLED2) 1d = Select LED1 output 2d = Select LED2 output 3d = Reserved 4d = Reserved 7d = automatic selection & disable fast transient function

0x0001D84D WLED1_CTRL_WLED_OVP

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: PERPH_RB

WLED1_CTRL_WLED_OVP

Bits	Name	Description
1:0	WLED_OVP	WLED OVP AMOLED VOUT 00 = 31V 7.54V 01 = 29.5V 7.46V 10 = 19.4V 5.9V 11 = 17.8V 5.6V

0x0001D84E WLED1_CTRL_WLED_ILIM

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x03

Reset Name: PERPH_RB

Boost current limit selection. Current limit after soft start is complete

WLED1_CTRL_WLED_ILIM

Bits	Name	Description
7	OVERWRITE	

WLED1_CTRL_WLED_ILIM (cont.)

Bits	Name	Description
2:0	WLED_ILIM	Code 8994 000 105mA 001 385mA (default for AMOLED) 010 660mA 011 980mA (default for WLED 4s4p) 100 1150mA 101 1420mA 110 1700mA 111 1980mA

0x0001D853 WLED1_CTRL_SOFTSTART_RAMP_DELAY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: PERPH_RB

WLED1_CTRL_SOFTSTART_RAMP_DELAY

Bits	Name	Description
2:0	SOFTSTART_RAMP_DELAY	Time to ramp Ilim from 0 to 100% of Ilim threshold during soft start Ramp time = 3 * (1/32kHz) * (sstart_ramp_t + 1)

0x0001D859 WLED1_CTRL_EN_HW_BL_REDN

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

WLED1_CTRL_EN_HW_BL_REDN

Bits	Name	Description
7	EN_HW_BL_REDN	when enabled AND signal asserted on HW pin This will cut the backlight current by half for e.g. TX_GTR_THRES can be connected to the HW pin when a high power transmit is sent, the backlight current is reduced by 1/2 0 = BL current reduction feature is disabled 1 = BL current reduction feature is enabled

0x0001D85A WLED1_CTRL_EN_PSM

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

WLED1_CTRL_EN_PSM

Bits	Name	Description
7	EN_PSM	Enable Pulse Skipping mode (PSM) 0 = PSM disabled 1 = PSM enabled

25 WLED1_SINK_WLED_SINK

0x0001D900 WLED1_SINK_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

WLED1_SINK_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x0001D901 WLED1_SINK_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

WLED1_SINK_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x0001D902 WLED1_SINK_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [23:16]

WLED1_SINK_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x0001D903 WLED1_SINK_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

WLED1_SINK_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x0001D904 WLED1_SINK_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x17

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

WLED1_SINK_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	WLED

0x0001D905 WLED1_SINK_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x11

Reset Name: N/A

Peripheral SubType

WLED1_SINK_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	WLED_SINK

0x0001D946 WLED1_SINK_CURRENT_SINK_EN

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

WLED1_SINK_CURRENT_SINK_EN

Bits	Name	Description
7	EN_CURRENT_SINK4	Reserved
6	EN_CURRENT_SINK3	Reserved
5	EN_CURRENT_SINK2	0 = LED2 disabled 1 = LED2 active
4	EN_CURRENT_SINK1	0 = LED1 disabled 1 = LED1 active

0x0001D947 WLED1_SINK_ILED_SYNC_BIT

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

WLED1_SINK_ILED_SYNC_BIT

Bits	Name	Description
3	SYNC_LED4	Reserved
2	SYNC_LED3	Reserved
1	SYNC_LED2	Writing to this register will update the 12 bit register values to the modulator and the full scale current setting register - LED2
0	SYNC_LED1	Writing to this register will update the 12 bit register values to the modulator and the full scale current setting register - LED1

0x0001D94B WLED1_SINK_HYBRID_DIMMING_TRESH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x03

Reset Name: PERPH_RB

Valid only on PM8994

PMIC_SYNC=clk_19p2:logic_rb

WLED1_SINK_HYBRID_DIMMING_TRESH

Bits	Name	Description
2:0	HYBRID_DIM_THRESH	Combined dimming threshold control 000 - 0.78 %001 - 1.56 %010 - 3.13 %011 - 6.25 %100 - 12.5 %101 - 25 %110 - 50 %111 - 100%

0x0001D950 WLED1_SINK_LED1_MODULATOR_EN

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: PERPH_RB

PMIC_SYNC=clk_19p2:logic_rb

WLED1_SINK_LED1_MODULATOR_EN

Bits	Name	Description
7	LED1_EN_MODULATOR	0 = modulator is disabled 1 = modulator is enabled
0	CS_GATEDRV	0 = disable this function. 1 = enable this function. Turn off 83% CS NMOS.

0x0001D951 WLED1_SINK_LED1_IDAC_SYNC_DELAY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: PERPH_RB

PMIC_SYNC=clk_32k:logic_rb

WLED1_SINK_LED1_IDAC_SYNC_DELAY

Bits	Name	Description
2:0	LED1_IDAC_SYNC_DELAY	Delay of activation of WLED_FULL_SCALE_SETTING<4:0> register to IDAC relative to write of WLED_SYNC bit. WLED_SYNC is used to synchronize IDAC and modulator updates 000 : No delay after LED_sync write 001 : 200us delay 010 : 400us delay 011 : 600us delay 100 : 800us delay 101 : 1ms delay 110 : 1.2ms delay 111 : 1.4ms delay

0x0001D952 WLED1_SINK_LED1_FULL_SCALE_CURRENT

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x0C

Reset Name: PERPH_RB

WLED1_SINK_LED1_FULL_SCALE_CURRENT

Bits	Name	Description
3:0	LED1_FULL_SCALE_CURRENT	00000 = 0 mA 00001 = 2.5mA 00010 = 5mA .. 1100 = 30mA code above 30mA maps to 1100

0x0001D953 WLED1_SINK_LED1_MODULATOR_SRC_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

PMIC_SYNC=clk_19p2:logic_rb

WLED1_SINK_LED1_MODULATOR_SRC_SEL

Bits	Name	Description
0	LED1_MODULATOR_SRC_SEL	0 = use internally generated modulator signals for dimming 1 = use externally generated modulator signals (i.e LPG) for dimming

0x0001D956 WLED1_SINK_LED1_CABC_EN

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

PMIC_SYNC=clk_19p2:logic_rb

WLED1_SINK_LED1_CABC_EN

Bits	Name	Description
7	LED1_CABC_EN	0 = CABC function disabled for current sink 1 = CABC is modulated with brightness register setting

0x0001D957 WLED1_SINK_LED1_BRIGHTNESS_SETTING_LSB

Type: RW
Clock: PBUS_WRCLK
Reset State: 0xFF

Reset Name: PERPH_RB

WLED1_SINK_LED1_BRIGHTNESS_SETTING_LSB

Bits	Name	Description
7:0	LED1_BRIGHTNESS_SETTING_LSB	LSB = 0.61uA/ segment, 12 segments in total At FSC = 30mA, LSB = 7.3uA FSC = 25mA, LSB = 6.1uA FSC = 15mA, LSB = 3.7uA

0x0001D958 WLED1_SINK_LED1_BRIGHTNESS_SETTING_MSB

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x0F

Reset Name: PERPH_RB

WLED1_SINK_LED1_BRIGHTNESS_SETTING_MSB

Bits	Name	Description
3:0	LED1_BRIGHTNESS_SETTING_MSB	LSB = 156uA/ segment, 12 segments in total At FSC = 30mA, LSB = 1.875mA FSC = 25mA, LSB = 1.563mA FSC = 15mA, LSB = 0.938mA

0x0001D960 WLED1_SINK_LED2_MODULATOR_EN

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: PERPH_RB

PMIC_SYNC=clk_19p2:logic_rb

WLED1_SINK_LED2_MODULATOR_EN

Bits	Name	Description
7	LED2_EN_MODULATOR	0 = modulator is disabled 1 = modulator is enabled

WLED1_SINK_LED2_MODULATOR_EN (cont.)

Bits	Name	Description
0	CS_GATEDRV	0 = disable this function. 1 = enable this function. Turn off 83% CS NMOS.

0x0001D961 WLED1_SINK_LED2_IDAC_SYNC_DELAY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: PERPH_RB

PMIC_SYNC=clk_32k:logic_rb

WLED1_SINK_LED2_IDAC_SYNC_DELAY

Bits	Name	Description
2:0	LED2_IDAC_SYNC_DELAY	Delay of activation of WLED_FULL_SCALE_SETTING<4:0> register to IDAC relative to write of WLED_SYNC bit. WLED_SYNC is used to synchronize IDAC and modulator updates 000 : No delay after LED_sync write 001 : 200us delay 010 : 400us delay 011 : 600us delay 100 : 800us delay 101 : 1ms delay 110 : 1.2ms delay 111 : 1.4ms delay

0x0001D962 WLED1_SINK_LED2_FULL_SCALE_CURRENT

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x0C

Reset Name: PERPH_RB

WLED1_SINK_LED2_FULL_SCALE_CURRENT

Bits	Name	Description
3:0	LED2_FULL_SCALE_CURRENT	00000 = 0 mA 00001 = 2.5mA 00010 = 5mA .. 1100 = 30mA code above 30mA maps to 1100

0x0001D963 WLED1_SINK_LED2_MODULATOR_SRC_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

PMIC_SYNC=clk_19p2:logic_rb

WLED1_SINK_LED2_MODULATOR_SRC_SEL

Bits	Name	Description
0	LED2_MODULATOR_SRC_SEL	0 = use internally generated modulator signals for dimming 1 = use externally generated modulator signals (i.e LPG) for dimming

0x0001D966 WLED1_SINK_LED2_CABC_EN

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

PMIC_SYNC=clk_19p2:logic_rb

WLED1_SINK_LED2_CABC_EN

Bits	Name	Description
7	LED2_CABC_EN	0 = CABC function disabled for current sink 1 = CABC is modulated with brightness register setting

0x0001D967 WLED1_SINK_LED2_BRIGHTNESS_SETTING_LSB

Type: RW
Clock: PBUS_WRCLK
Reset State: 0xFF

Reset Name: PERPH_RB

WLED1_SINK_LED2_BRIGHTNESS_SETTING_LSB

Bits	Name	Description
7:0	LED2_BRIGHTNESS_SETTING_LSB	LSB = 0.61uA/ segment, 12 segments in total At FSC = 30mA, LSB = 7.3uA FSC = 25mA, LSB = 6.1uA FSC = 15mA, LSB = 3.7uA

0x0001D968 WLED1_SINK_LED2_BRIGHTNESS_SETTING_MSB

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x0F

Reset Name: PERPH_RB

WLED1_SINK_LED2_BRIGHTNESS_SETTING_MSB

Bits	Name	Description
3:0	LED2_BRIGHTNESS_SETTING_MSB	LSB = 156uA/ segment, 12 segments in total At FSC = 30mA, LSB = 1.875mA FSC = 25mA, LSB = 1.563mA FSC = 15mA, LSB = 0.938mA

26 IBB_IBB (applicable only for PMI8940)

0x0001DC00 IBB_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

IBB_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x0001DC01 IBB_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

IBB_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x0001DC02 IBB_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [23:16]

IBB_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x0001DC03 IBB_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

IBB_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x0001DC04 IBB_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x20

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

IBB_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	IBB

0x0001DC05 IBB_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

IBB_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	IBB

0x0001DC08 IBB_STATUS1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Status Register 1

IBB_STATUS1

Bits	Name	Description
7	VREG_OK	Regulator abs(Vout) > 90% of abs(target voltage) 0x0: VREG_NOTOK 0x1: VREG_OK
6	SC_DETECT	Module Short Circuit detected 0x1: MODULE_SHORT_CIRCUIT 0x0: MODULE_NO_SC_FAULT
5	ILIMIT_ERROR	0 = no current limit error, 1 = current limit error 0x0: NO_ILIMIT_ERROR 0x1: ILIMIT_ERROR

0x0001DC09 IBB_STATUS2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Status Register 2: this register needs to written once with any value before reading

IBB_STATUS2

Bits	Name	Description
5:0	CURRENT_OUTPUT_VOLTAGE	The current output voltage setting that IBB has, Vout = -(1.4 + 100mV * code) 0x0: V_M1P4V 0x1: V_M1P5V 0x2: V_M1P6V 0x3: V_M1P7V 0x4: V_M1P8V 0x5: V_M1P9V 0x6: V_M2P0V 0x7: V_M2P1V 0x8: V_M2P2V 0x9: V_M2P3V 0xA: V_M2P4V 0xB: V_M2P5V 0xC: V_M2P6V 0xD: V_M2P7V 0xE: V_M2P8V 0xF: V_M2P9V 0x10: V_M3P0V 0x11: V_M3P1V 0x12: V_M3P2V 0x13: V_M3P3V 0x14: V_M3P4V 0x15: V_M3P5V 0x16: V_M3P6V 0x17: V_M3P7V 0x18: V_M3P8V 0x19: V_M3P9V 0x1A: V_M4P0V 0x1B: V_M4P1V 0x1C: V_M4P2V 0x1D: V_M4P3V 0x1E: V_M4P4V 0x1F: V_M4P5V 0x20: V_M4P6V 0x21: V_M4P7V 0x22: V_M4P8V 0x23: V_M4P9V 0x24: V_M5P0V 0x25: V_M5P1V 0x26: V_M5P2V 0x27: V_M5P3V 0x28: V_M5P4V 0x29: V_M5P5V 0x2A: V_M5P6V

IBB_STATUS2 (cont.)

Bits	Name	Description
		0x2B: V_M5P7V 0x2C: V_M5P8V 0x2D: V_M5P9V 0x2E: V_M6P0V 0x2F: V_M6P1V 0x30: V_M6P2V 0x31: V_M6P3V 0x32: V_M6P4V 0x33: V_M6P5V 0x34: V_M6P6V 0x35: V_M6P7V 0x36: V_M6P8V 0x37: V_M6P9V 0x38: V_M7P0V 0x39: V_M7P1V 0x3A: V_M7P2V 0x3B: V_M7P3V 0x3C: V_M7P4V 0x3D: V_M7P5V 0x3E: V_M7P6V 0x3F: V_M7P7V

0x0001DC0A IBB_STATUS3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Status Register 3: this register needs to written once with any value before reading

IBB_STATUS3

Bits	Name	Description
7:0	IBB_STATUS	The current IBB status. 0: IBB is in off mode, 4-7: IBB is in powering-up mode, 14-15: IBB is in normal operation mode, 8-13: IBB is in powering-down mode 0x0: IBB_OFF 0x4: IBB_PWRUP1 0x5: IBB_PWRUP2 0x6: IBB_PWRUP3 0x7: IBB_PWRUP4 0xE: IBB_ON1 0xF: IBB_ON2 0x8: IBB_PWRDN1 0x9: IBB_PWRDN2 0xA: IBB_PWRDN3 0xB: IBB_PWRDN4 0xC: IBB_PWRDN5 0xD: IBB_PWRDN6

0x0001DC10 IBB_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Interrupt Real Time Status Bits

IBB_INT_RT_STS

Bits	Name	Description
2	SC_ERROR_RT_STS	Real-time SC detection flag 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
1	ILIMIT_ERROR_RT_STS	Current limit exceeded for x consecutive cycles 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
0	VREG_NOT_OK_RT_STS	Real-Time VREG_NOT_OK flag 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH

0x0001DC11 IBB_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

IBB_INT_SET_TYPE

Bits	Name	Description
2	SC_ERROR_TYPE	0x0: LEVEL 0x1: EDGE
1	ILIMIT_ERROR_TYPE	0x0: LEVEL 0x1: EDGE
0	VREG_NOT_OK_TYPE	0x0: LEVEL 0x1: EDGE

0x0001DC12 IBB_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

IBB_INT_POLARITY_HIGH

Bits	Name	Description
2	SC_ERROR_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
1	ILIMIT_ERROR_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
0	VREG_NOT_OK_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x0001DC13 IBB_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

IBB_INT_POLARITY_LOW

Bits	Name	Description
2	SC_ERROR_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
1	ILIMIT_ERROR_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
0	VREG_NOT_OK_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x0001DC14 IBB_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

IBB_INT_LATCHED_CLR

Bits	Name	Description
2	SC_ERROR_LATCHED_CLR	
1	ILIMIT_ERROR_LATCHED_CLR	
0	VREG_NOT_OK_LATCHED_CLR	

0x0001DC15 IBB_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

IBB_INT_EN_SET

Bits	Name	Description
2	SC_ERROR_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
1	ILIMIT_ERROR_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
0	VREG_NOT_OK_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED

0x0001DC16 IBB_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

IBB_INT_EN_CLR

Bits	Name	Description
2	SC_ERROR_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
1	ILIMIT_ERROR_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
0	VREG_NOT_OK_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

0x0001DC18 IBB_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

IBB_INT_LATCHED_STS

Bits	Name	Description
2	SC_ERROR_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
1	ILIMIT_ERROR_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
0	VREG_NOT_OK_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

0x0001DC19 IBB_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

IBB_INT_PENDING_STS

Bits	Name	Description
2	SC_ERROR_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
1	ILIMIT_ERROR_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
0	VREG_NOT_OK_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

0x0001DC1A IBB_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

IBB_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x0001DC1B IBB_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Selects priority (high / low) of interrupt

IBB_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	SR = 0, A = 1 0x0: SR 0x1: A

0x0001DC41 IBB_OUTPUT_VOLTAGE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

Vout = -(1.4 + 100mV * code). Default depends on LCD/AMOLED bit.

Code = 0x00 to 0x46

IBB_OUTPUT_VOLTAGE

Bits	Name	Description
7	OVERRIDE_OUTPUT_VOLTAGE	0 = Default output voltage depending on LCD/AMOLED mode (-5.5V for LCD and -4V for AMOLED), 1 = Output voltage given by SET_OUTPUT_VOLTAGE field 0x0: DEFAULT_OUTPUT_VOLTAGE 0x1: OVERRIDE_OUTPUT_VOLTAGE

IBB_OUTPUT_VOLTAGE (cont.)

Bits	Name	Description
5:0	SET_OUTPUT_VOLTAGE	Vout = -(1.4 + 100mV * code) if OVERRIDE_OUTPUT_VOLTAGE is 1 0x0: V_M1P4V 0x1: V_M1P5V 0x2: V_M1P6V 0x3: V_M1P7V 0x4: V_M1P8V 0x5: V_M1P9V 0x6: V_M2P0V 0x7: V_M2P1V 0x8: V_M2P2V 0x9: V_M2P3V 0xA: V_M2P4V 0xB: V_M2P5V 0xC: V_M2P6V 0xD: V_M2P7V 0xE: V_M2P8V 0xF: V_M2P9V 0x10: V_M3P0V 0x11: V_M3P1V 0x12: V_M3P2V 0x13: V_M3P3V 0x14: V_M3P4V 0x15: V_M3P5V 0x16: V_M3P6V 0x17: V_M3P7V 0x18: V_M3P8V 0x19: V_M3P9V 0x1A: V_M4P0V 0x1B: V_M4P1V 0x1C: V_M4P2V 0x1D: V_M4P3V 0x1E: V_M4P4V 0x1F: V_M4P5V 0x20: V_M4P6V 0x21: V_M4P7V 0x22: V_M4P8V 0x23: V_M4P9V 0x24: V_M5P0V 0x25: V_M5P1V 0x26: V_M5P2V 0x27: V_M5P3V 0x28: V_M5P4V 0x29: V_M5P5V 0x2A: V_M5P6V 0x2B: V_M5P7V 0x2C: V_M5P8V

IBB_OUTPUT_VOLTAGE (cont.)

Bits	Name	Description
		0x2D: V_M5P9V 0x2E: V_M6P0V 0x2F: V_M6P1V 0x30: V_M6P2V 0x31: V_M6P3V 0x32: V_M6P4V 0x33: V_M6P5V 0x34: V_M6P6V 0x35: V_M6P7V 0x36: V_M6P8V 0x37: V_M6P9V 0x38: V_M7P0V 0x39: V_M7P1V 0x3A: V_M7P2V 0x3B: V_M7P3V 0x3C: V_M7P4V 0x3D: V_M7P5V 0x3E: V_M7P6V 0x3F: V_M7P7V

0x0001DC42 IBB_RING_SUPPRESSION_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

IBB_RING_SUPPRESSION_CTL

Bits	Name	Description
7	ENABLE_RING_SUPPRESSION	Enable/Disable ring suppression feature in DCM 0x0: RING_SUPPRESSION_DISABLED 0x1: RING_SUPPRESSION_ENABLED

0x0001DC46 IBB_ENABLE_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

When IBB is enabled, it is switching and regulating

When IBB is disabled, output is floating

IBB_ENABLE_CTL

Bits	Name	Description
7	MODULE_EN	1 = module enable 0 = module disable (lowest power state) 0x0: MODULE_DIS 0x1: MODULE_EN
6	SWIRE_RDY	1 = ready to listen to S-Wire 0 = not ready to listen to S-Wire 0x0: SWIRE_NOT_RDY 0x1: SWIRE_RDY

0x0001DC47 IBB_PD_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x80

Reset Name: dVdd_rb

IBB_PD_CTL

Bits	Name	Description
7	ENABLE_PD	This field has to be updated before the module is disabled to take effect, 0 = Disable Discharge, 1 = Enable Discharge 0x0: PD_DISABLE 0x1: PD_ENABLE
0	PD_STRENGTH	0 = Full Strength, 1 = Half Strength 0x0: PD_FULLSTRENGTH 0x1: PD_HALFSTRENGTH

0x0001DC50 IBB_PS_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x05

Reset Name: dVdd_rb

IBB_PS_CTL

Bits	Name	Description
7	EN_PS	1 = enable pulse skipping, 0 = disable pulse skipping 0x0: DIS_PS 0x1: EN_PS
2:0	PS_THRESHOLD	modulation of the pulse_skipping threshold, bias current= code*0.5uA 0x0: UA0 0x1: UA0P5 0x2: UA1 0x3: UA1P5 0x4: UA2 0x5: UA2P5 0x6: UA3 0x7: UA3P5

0x0001DC58 IBB_PWRUP_PWRDN_CTL_1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0xC4

Reset Name: dVdd_rb

PMIC_LOCKED=SEC_ACCESS

IBB_PWRUP_PWRDN_CTL_1

Bits	Name	Description
7	PWRUP_DLY1_SRC	0 = IBB power stage delay source is after IBB's bias active, 1 = IBB power stage delay source is after VREG_OK from LAB and IBB's bias active 0x0: BIAS_ACTIVE 0x1: LAB_VREG_OK
6	EN_PWRUP_DLY1	0 = disable the PWRUP_DLY1, 1 = enable the PWRUP_DLY1 0x0: DIS_PWRUP_DLY1 0x1: EN_PWRUP_DLY1
5:4	PWRUP_DLY1	00 = 1ms, 01 = 2ms, 10 = 4ms, 11 = 8ms 0x0: MS1 0x1: MS2 0x2: MS4 0x3: MS8

IBB_PWRUP_PWRDN_CTL_1 (cont.)

Bits	Name	Description
2	PWRDN_DLY2_SRC	0 = LAB power-down delay source is after IBB disable, 1 = LAB power-down delay is after IBB's discharged 0x0: IBB_DIS 0x1: IBB_DISCHARGE
1:0	PWRDN_DLY2	00 = 1ms, 01 = 2ms, 10 = 4ms, 11 = 8ms 0x0: MS1 0x1: MS2 0x2: MS4 0x3: MS8

0x0001DC5F IBB_SOFT_START_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: dVdd_rb

IBB_SOFT_START_CTL

Bits	Name	Description
1:0	SOFT_START	The charging resistance is modified only on startup. Time constant is ref_cap*charging resistor. 0: Charging resistor = 300k Ohms, 1: Charging resistor = 64k Ohms, 2: Charging resistor = 32k Ohms, 3: Charging resistor = 16k Ohms,

27 LAB_LAB (applicable only for PMI8940)

0x0001DE00 LAB_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

LAB_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x0001DE01 LAB_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

LAB_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x0001DE02 LAB_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: N/A

HW Version Register [23:16]

LAB_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x0001DE03 LAB_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

LAB_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x0001DE04 LAB_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x24

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

LAB_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	LAB

0x0001DE05 LAB_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

LAB_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	LAB

0x0001DE08 LAB_STATUS1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Status Register

LAB_STATUS1

Bits	Name	Description
7	VREG_OK	Regulator abs(Vout) > 90% of abs(target voltage) 0x0: VREG_NOTOK 0x1: VREG_OK
6	SC_DETECT	Module Short Circuit detected 0x1: MODULE_SHORT_CIRCUIT 0x0: MODULE_NO_SC_FAULT
5	LAB_STATUS	The current LAB status: 0=DISABLED, 1=ENABLED 0x0: DISABLED 0x1: ENABLED

0x0001DE10 LAB_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Interrupt Real Time Status Bits

LAB_INT_RT_STS

Bits	Name	Description
1	SC_ERROR_RT_STS	Current limit exceeded for x consecutive cycles 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
0	VREG_OK_RT_STS	Real-Time VREG_OK flag 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH

0x0001DE11 LAB_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

0 = use level trigger interrupts, 1 = use edge trigger interrupts

LAB_INT_SET_TYPE

Bits	Name	Description
1	SC_ERROR_TYPE	0x0: LEVEL 0x1: EDGE
0	VREG_OK_TYPE	0x0: LEVEL 0x1: EDGE

0x0001DE12 LAB_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

LAB_INT_POLARITY_HIGH

Bits	Name	Description
1	SC_ERROR_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
0	VREG_OK_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x0001DE13 LAB_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

LAB_INT_POLARITY_LOW

Bits	Name	Description
1	SC_ERROR_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
0	VREG_OK_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x0001DE14 LAB_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

LAB_INT_LATCHED_CLR

Bits	Name	Description
1	SC_ERROR_LATCHED_CL R	
0	VREG_OK_LATCHED_CLR	

0x0001DE15 LAB_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

LAB_INT_EN_SET

Bits	Name	Description
1	SC_ERROR_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
0	VREG_OK_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED

0x0001DE16 LAB_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

LAB_INT_EN_CLR

Bits	Name	Description
1	SC_ERROR_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
0	VREG_OK_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

0x0001DE18 LAB_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

LAB_INT_LATCHED_STS

Bits	Name	Description
1	SC_ERROR_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
0	VREG_OK_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

0x0001DE19 LAB_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

LAB_INT_PENDING_STS

Bits	Name	Description
1	SC_ERROR_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
0	VREG_OK_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

0x0001DE1A LAB_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Selects the MID that will receive the interrupt

LAB_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x0001DE1B LAB_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Selects priority (high / low) of interrupt

LAB_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	SR = 0, A = 1 0x0: SR 0x1: A

0x0001DE41 LAB_OUTPUT_VOLTAGE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

LAB_OUTPUT_VOLTAGE

Bits	Name	Description
7	OVERRIDE_OUTPUT_VOLTAGE	0=default output voltage depending on LCD/AMOLED mode (5.5V for LCD and 4.6V for AMOLED), 1=output voltage given by SET_OUTPUT_VOLTAGE field
3:0	SET_OUTPUT_VOLTAGE	Vout = (4.6 + 100mV * code). Default depends on LCD/AMOLED bit. Code = 0x00 to 0xF

0x0001DE42 LAB_RING_SUPPRESSION_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x80

Reset Name: dVdd_rb

LAB_RING_SUPPRESSION_CTL

Bits	Name	Description
7	ENABLE_RING_SUPPRESSION	Enable/Disable ring suppression feature in DCM

0x0001DE46 LAB_ENABLE_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

When LAB is enabled, it is switching and regulating

When LAB is disabled, output is floating

LAB_ENABLE_CTL

Bits	Name	Description
7	MODULE_EN	1 = module enable, 0 = module disable (lowest power state) 0x0: MODULE_DIS 0x1: MODULE_EN

0x0001DE47 LAB_PD_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: dVdd_rb

LAB_PD_CTL

Bits	Name	Description
1	DIS_PULLDOWN	0= enable pull-down, 1= disable pull-down 0x0: EN_PD 0x1: DIS_PD

LAB_PD_CTL (cont.)

Bits	Name	Description
0	PD_STRENGTH	0=weak pull-down, 1= strong pull-down 2x Strength 0x0: PD_WEAK 0x1: PD_STRONG

0x0001DE50 LAB_PS_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x82

Reset Name: dVdd_rb

LAB_PS_CTL

Bits	Name	Description
7	EN_PS	1 = enable PS, 0= disable PS 0x0: PWM 0x1: PULSE_SKIP
3	SEL_DIG_PS	1 = select the digital PS, 0 = select the analog PS 0x1: DIGITAL_PS 0x0: ANALOG_PS
2	SEL_PS_TABLE	1 = select table1, 0 = select table 0 0x0: PS_TABLE_0 0x1: PS_TABLE_1
1:0	PS_THRESHOLD	Threshold for when pulse-skip mode is entered 00 = 20mA 01 = 30mA 10 = 40mA 11 = 50mA 0x0: MA20 0x1: MA30 0x2: MA40 0x3: MA50

0x0001DE5F LAB_SOFT_START_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: dVdd_rb

LAB_SOFT_START_CTL

Bits	Name	Description
1:0	SELECT_THE_MAX_SOFT_START_TIME	max soft-start time 00 = 200us 01 = 400us 10 = 600us 11 = 800us 0x0: US200 0x1: US400 0x2: US600 0x3: US800

28 FG_SOC_FG_SOC

0x00004004 FG_SOC_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x0D

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

FG_SOC_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	

0x00004005 FG_SOC_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x09

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

FG_SOC_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	

0x00004006 FG_SOC_FG_ALG_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

FG_SOC_FG_ALG_STS

Bits	Name	Description
7	RDY	FG Algorithm READY Status bit asserted at the end of each SOC update, cleared on a battery missing event and on a shutdown event 0x0: FG_NOT_READY 0x1: FG_READY
6	BOOT_DONE	FG Algorithm status bit to notify that the First estimate of SoC is done, cleared on a battery missing event 0x0: FG_BOOT_NOT_DONE 0x1: FG_BOOT_DONE
5	FIRST_ITER_DONE	FG Algorithm status bit to notify that the first iteration after a first SoC estimate is completed 0x0: FG_FIRST_ITER_NOT_DONE 0x1: FG_FIRST_ITER_DONE
4	RESTART_DONE	FG Algorithm status bit to notify that the RELOAD/RESTART sequence is done, cleared when RESTART.GO is cleared 0x0: FG_RESTART_NOT_DONE 0x1: FG_RESTART_DONE
3	RESTART_IN_PROGRESS	FG Algorithm status bit to notify that the RELOAD/RESTART sequence is in progress, cleared when the sequence is completed 0x0: FG_RESTART_NOT_IN_PROGRESS 0x1: FG_RESTART_IN_PROGRESS
2	WDOG_EXP	1 indicates a watchdog expiry event occurred since last time it was cleared, see FG_WDOG_EXP__CLR register 0x0: FG_WDOG_NOT_EXPIRED 0x1: FG_WDOG_EXPIRED
1	CYCLE_STRETCHED	1 indicates FG cycle was stretched due to memory not released by system in time; Cleared by writing 0x0: FG_CYCLE_NOT_STRETCHED 0x1: FG_CYCLE_STRETCHED

0x00004007 FG_SOC_FG_ALG_AUX_STS0

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

FG_SOC_FG_ALG_AUX_STS0

Bits	Name	Description
7	I_BELOW_TERMINATION	Charging current below termination current value 0x0: TERM_CURRENT_NOT_REACHED 0x1: TERM_CURRENT_REACHED
6	V_REACHED_FLOAT_THRESHOLD	Battery voltage reached float threshold 0x0: VBATT_FLOAT_NOT_REACHED 0x1: VBATT_FLOAT_REACHED
5	I_CC_AVAILABLE	Constant current measurement available 0x0: I_CC_INACTIVE 0x1: I_CC_ACTIVE
4	BATT_PREDICTION_CHARGE	For the purpose of the selection of OCV and the parameters of the battery model, the battery is considered as in charge 0x0: BATT_MODEL_DISCHARGE 0x1: BATT_MODEL_CHARGE
3	PULSE_APPROVED	The Battery pulse to estimate the resistance is approved 0x0: PULSE_NOT_APPROVED 0x1: PULSE_APPROVED
2	ONCONNECT_OCV	Lower resolution VBATT/IBAT reading used for initial OCV estimate 0x0: ONCONNECT_OCV_FALSE 0x1: ONCONNECT_OCV_TRUE

0x00004008 FG_SOC_SLEEP_SHUTDOWN_STS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

FG_SOC_SLEEP_SHUTDOWN_STS

Bits	Name	Description
7	FG_SLEEP_CC	FG requests that analog peripherals enter low power sleep state during long wait, CC conversion 0x0: SLEEP_CC_NOT_REQUESTED 0x1: SLEEP_CC_REQUESTED
6	FG_SLEEP_SYNC	FG requests that analog peripherals enter low power sleep state during sync conversion 0x0: SLEEP_SYNC_NOT_REQUESTED 0x1: SLEEP_SYNC_REQUESTED

FG_SOC_SLEEP_SHUTDOWN_STS (cont.)

Bits	Name	Description
5	SHUTDOWN_OR_SLEEP	FG receives acknowledge that analog peripherals are in low power sleep state 0x0: FG_AWAKE 0x1: FG_IN_SHDN_OR_SLEEP
4	FG_SHUTDOWN_REQ	FG receives shutdown request 0x0: SHUTDOWN_NOT_REQUESTED 0x1: SHUTDOWN_REQUESTED
3	FG_SHUTDOWN_ALLOWED	FG grants shutdown request 0x0: FG_NOT_IN_SHDN 0x1: FG_SHDN_ACK

0x00004009 FG_SOC_FG_MONOTONIC_SOC

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

FG_SOC_FG_MONOTONIC_SOC

Bits	Name	Description
7:0	STS	% State of Charge - monotonic, 0xFF indicates 100%

0x0000400A FG_SOC_FG_MONOTONIC_SOC_CP

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

FG_SOC_FG_MONOTONIC_SOC_CP

Bits	Name	Description
7:0	STS	Copy of reg FG_MONOTONIC_SOC; Burst read, compare for match

0x00004010 FG_SOC_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Interrupt Real Time Status Bits

FG_SOC_INT_RT_STS

Bits	Name	Description
6	UPDATE_SOC_RT_STS	IRQ to notify SoC got updated; Occurs every fuel gauge cycle @ approximately 1.47seconds 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
5	FIRST_EST_DONE_RT_STS	IRQ to notify that the First estimate of SoC is done, cleared on a battery missing event 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
4	DELTA_SOC_RT_STS	IRQ to notify that Monotonic SoC change exceeded the specified delta SoC threshold 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
3	EMPTY_SOC_RT_STS	IRQ to notify that Monotonic SoC = 0% 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
2	FULL_SOC_RT_STS	IRQ to notify that Monotonics SoC = 100% 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
1	LOW_SOC_RT_STS	IRQ to notify that Monotonics SoC < Low SoC Threshold 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
0	HIGH_SOC_RT_STS	IRQ to notify that Monotonics SoC > High SoC Threshold 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH

0x00004011 FG_SOC_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

0 = use level trigger interrupts, 1 = use edge trigger interrupts

FG_SOC_INT_SET_TYPE

Bits	Name	Description
6	UPDATE_SOC_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
5	FIRST_EST_DONE_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
4	DELTA_SOC_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
3	EMPTY_SOC_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
2	FULL_SOC_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
1	LOW_SOC_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
0	HIGH_SOC_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE

0x00004012 FG_SOC_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

1= Interrupt will trigger on a level high (rising edge event, 0 = level high triggering is disabled

FG_SOC_INT_POLARITY_HIGH

Bits	Name	Description
6	UPDATE_SOC_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
5	FIRST_EST_DONE_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
4	DELTA_SOC_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
3	EMPTY_SOC_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
2	FULL_SOC_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

FG_SOC_INT_POLARITY_HIGH (cont.)

Bits	Name	Description
1	LOW_SOC_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
0	HIGH_SOC_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x00004013 FG_SOC_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

1' = Interrupt will trigger on a level low (falling edge event, '0' = level low triggering is disabled

FG_SOC_INT_POLARITY_LOW

Bits	Name	Description
6	UPDATE_SOC_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
5	FIRST_EST_DONE_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
4	DELTA_SOC_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
3	EMPTY_SOC_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
2	FULL_SOC_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
1	LOW_SOC_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
0	HIGH_SOC_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x00004014 FG_SOC_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PMIC_ASYNC_PULSE_ONE

FG_SOC_INT_LATCHED_CLR

Bits	Name	Description
6	UPDATE_SOC_INT_LATCHED_CLR	
5	FIRST_EST_DONE_INT_LATCHED_CLR	
4	DELTA_SOC_INT_LATCHED_CLR	
3	EMPTY_SOC_INT_LATCHED_CLR	
2	FULL_SOC_INT_LATCHED_CLR	
1	LOW_SOC_INT_LATCHED_CLR	
0	HIGH_SOC_INT_LATCHED_CLR	

0x00004015 FG_SOC_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

FG_SOC_INT_EN_SET

Bits	Name	Description
6	UPDATE_SOC_INT_LATCHED_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
5	FIRST_EST_DONE_INT_LATCHED_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
4	DELTA_SOC_INT_LATCHED_SET	0x0: INT_DISABLED 0x1: INT_ENABLED

FG_SOC_INT_EN_SET (cont.)

Bits	Name	Description
3	EMPTY_SOC_INT_LATCHED_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
2	FULL_SOC_INT_LATCHED_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
1	LOW_SOC_INT_LATCHED_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
0	HIGH_SOC_INT_LATCHED_SET	0x0: INT_DISABLED 0x1: INT_ENABLED

0x00004016 FG_SOC_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

FG_SOC_INT_EN_CLR

Bits	Name	Description
6	UPDATE_SOC_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
5	FIRST_EST_DONE_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
4	DELTA_SOC_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
3	EMPTY_SOC_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
2	FULL_SOC_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
1	LOW_SOC_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
0	HIGH_SOC_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

0x00004018 FG_SOC_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Debug: Latched (Sticky Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

FG_SOC_INT_LATCHED_STS

Bits	Name	Description
6	UPDATE_SOC_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
5	FIRST_EST_DONE_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
4	DELTA_SOC_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
3	EMPTY_SOC_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
2	FULL_SOC_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
1	LOW_SOC_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
0	HIGH_SOC_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

0x00004019 FG_SOC_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Debug: Pending is set if interrupt has been sent but not cleared.

FG_SOC_INT_PENDING_STS

Bits	Name	Description
6	UPDATE_SOC_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
5	FIRST_EST_DONE_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

FG_SOC_INT_PENDING_STS (cont.)

Bits	Name	Description
4	DELTA_SOC_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
3	EMPTY_SOC_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
2	FULL_SOC_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
1	LOW_SOC_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
0	HIGH_SOC_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

0x0000401A FG_SOC_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Selects the MID that will receive the interrupt

FG_SOC_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x0000401B FG_SOC_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

SR=0 A=1

FG_SOC_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR 0x1: A

0x00004050 FG_SOC_BOOT_MOD

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Boot Mode Modification setting

PMIC_SYNC=fg_clk_1mhz_g:dVdd_rb

FG_SOC_BOOT_MOD

Bits	Name	Description
7	PREVENT_OTP_SYS_RELOAD	Not available
6	PREVENT_OTP_PROFILE_RELOAD	When a RELOAD/RESTART requires a First SoC re-detect prevent the reload of the battery profile from the OTP 0x0: DO_NOT_PREVENT_OTP_PROFILE_RELOAD 0x1: PREVENT_OTP_PROFILE_RELOAD

0x00004051 FG_SOC_RESTART

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

PMIC_SYNC=fg_clk_1mhz_g:dVdd_rb

FG_SOC_RESTART

Bits	Name	Description
4	REDO_BATID_DURING_FIRST_EST	"If a First SoC is requested RELOAD/RESTART sequence also perform a Battery ID detection" 0x0: FALSE 0x1: TRUE

FG_SOC_RESTART (cont.)

Bits	Name	Description
3	RERUN_FIRST_EST	"Execute a First SoC re-detection during a RELOAD/RESTART sequence" 0x0: FALSE 0x1: TRUE
2	RELOAD_PROFILE	Reload the profile settings during a RELOAD/RESTART sequence 0x0: FALSE 0x1: TRUE
1	RELOAD_SYS	Reload the system settings during a RELOAD/RESTART sequence 0x0: FALSE 0x1: TRUE
0	GO	Trigger a RELOAD/RESTART sequence 0x0: DO_NOT_EXECUTE_SEQUENCE 0x1: EXECUTE_SEQUENCE

0x00004052 FG_SOC_FG_WDOG_EXP

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

FG_SOC_FG_WDOG_EXP

Bits	Name	Description
7	CLR	Any write to this register clears WDOG_EXP bit in FG_ALG_STS register

0x00004053 FG_SOC_STS_CLR

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

FG_SOC_STS_CLR

Bits	Name	Description
7	CYCLE_STRETCH_CLR	Writing a 1 to this bit clears FG_ALG_STS__CYCLE_STRETCHED status 0x0: NORMAL 0x1: CLEAR

0x000040F5 FG_SOC_LOW_PWR_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: dVdd_rb

Enable and configure lower power consumption - sleep during CC and sync conversion, operation at lower clock frequency

FG_SOC_LOW_PWR_CFG

Bits	Name	Description
7	CC_SLEEP_EN	Enable sleep during constant current timer mode conversion (long wait), dropping power consumption to a lower level 0x0: DISABLE 0x1: ENABLE
6	SYNC_SLEEP_EN	Enable sleep and timer mode conversions for some sync conversions 0x0: DISABLE 0x1: ENABLE
5:4	SYNC_SLEEP_CFG	Configure the number of consecutive cycles that are sleep timer mode; Keep it stable during enable or change during CC time period; Logic consumes it unsynchronized 0x0: ACTIVE2_SLEEP2 0x1: ACTIVE2_SLEEP4 0x2: ACTIVE2_SLEEP8 0x3: ACTIVE2_SLEEP14
3	SYNC_SLEEP_REGEN_ESR_EN	Enable re-generation of ESR pulse that was blocked due to sync sleep; Pulse will occur during II active cycle; 0x0: DISABLE 0x1: ENABLE
2	SYNC_SLEEP_BCL1_EN	Enable one BCL conversion during sync sleep cycle - delays sleeping and power savings by one BCL conversion time period ~(2**8) * 5us; 0x0: DISABLE 0x1: ENABLE
1	SYNC_SLEEP_THRSH2_EN	Enable second threshold for current, apart from the one that decides LPM, to enter sync sleep cycle; 0x0: DISABLE 0x1: ENABLE
0	LO_FRQ_CLKSWITCH_EN	0=FG clk at 1MHz throughout; 1=starts at 1MHz; switched to lower frequency ADC clock (200KHz) after first SoC estimate, obviating 1MHz oscillator for further FG needs 0x0: DISABLE 0x1: ENABLE

29 FG_BATT_FG_BATT

0x00004104 FG_BATT_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x0D

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

FG_BATT_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	

0x00004105 FG_BATT_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x0A

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

FG_BATT_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	

0x00004106 FG_BATT_BATTERY

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

FG_BATT_BATTERY

Bits	Name	Description
7:6	ID	Battery Profile ID currently in use by the algorithm

0x00004107 FG_BATT_SYS_BATT

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

FG_BATT_SYS_BATT

Bits	Name	Description
7:5	STS	FG System status, ISMISSING=0, CHARGING_CV=1, CHARGING_CC=2, SYSTEM_FULL=3, DISCHARGING=4, AUTOMATIC_RECHARGE=5, SUPPLEMENTAL=6, EMPTY=7 0x0: ISMISSING 0x1: CHARGING_CV 0x2: CHARGING_CC 0x3: SYSTEM_FULL 0x4: DISCHARGING 0x5: AUTOMATIC_RECHARGE 0x6: SUPPLEMENTAL 0x7: EMPTY
4	BATT_REMOVED_LATCHED_STS	1: battery is/was removed; Once set can be cleared only through a software write of BATT_REMOVED_LATCHED__CLR 0x0: BATT_PRESENT 0x1: BATT_REMOVED_LATCHED
3	BATT_LOW_RT_STS	1: battery voltage low - comparator output 0x0: BATT_VOLTAGE_NORMAL 0x1: BATT_VOLTAGE_LOW
2	BATT_PROFILE_STS	1: Battery profile data store in RAM does not match OTP data 0x0: BATT_PROFILE_ORIGINAL 0x1: BATT_PROFILE_CHANGED

0x00004108 FG_BATT_BATT_DET

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: NA

FG_BATT_BATT_DET

Bits	Name	Description
7	ERR	Battery ID detection error,FALSE=0,TRUE=1 0x0: BATT_ID_DETECTION_OK 0x1: BATT_ID_DETECTION_ERR
6	SMART	Battery ID is smart 0x0: BATT_ID_DETECTION_NOT_SMART 0x1: BATT_ID_DETECTION_SMART
5	FLOAT	Battery ID is floating to ground 0x0: BATTERY_ID_NOT_FLOAT_TO_GND 0x1: BATTERY_ID_FLOAT_TO_GND
4	GND	Battery ID is shorted to ground 0x0: BATT_ID_NOT_SHORTED_TO_GND 0x1: BATT_ID_SHORTED_GND

0x00004109 FG_BATT_BATT_INFO_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0bX00XXX

Reset Name: NA

FG_BATT_BATT_INFO_STS

Bits	Name	Description
7	ESR_UPDATE	1=Battery Estimated Resistance updated by FG algorithm this cycle (a cycle is 1.4 seconds) 0x0: ESR_NOT_UPDATED_THIS_CYCLE 0x1: ESR_UPDATED_THIS_CYCLE
6	JEITA_HARD_HOT_RT_STS	0x0: JEITA_BELOW_HARD_HOT_THRESHOLD 0x1: JEITA_ABOVE_HARD_HOT_THRESHOLD
5	JEITA_HARD_COLD_RT_STS	0x0: JEITA_BELOW_HARD_COLD_THRESHOLD 0x1: JEITA_ABOVE_HARD_COLD_THRESHOLD

0x00004110 FG_BATT_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Interrupt Real Time Status Bits

FG_BATT_INT_RT_STS

Bits	Name	Description
7	BATT_MATCH_RT_STS	0x0: BATT_MATCH_RT_STS_FALSE 0x1: BATT_MATCH_RT_STS_TRUE
6	BATT_MISSING_RT_STS	0x0: BATT_MISSING_RT_STS_FALSE 0x1: BATT_MISSING_RT_STS_TRUE
5	BATT_UNKNOWN_RT_STS	0x0: BATT_UNKNOWN_RT_STS_FALSE 0x1: BATT_UNKNOWN_RT_STS_TRUE
4	BATT_ID_REQ_RT_STS	0x0: BATT_ID_REQ_RT_STS_FALSE 0x1: BATT_ID_REQ_RT_STS_TRUE
3	BATT_ID_DONE_RT_STS	0x0: BATT_IDENTIFIED_RT_STS_FALSE 0x1: BATT_IDENTIFIED_RT_STS_TRUE
2	VBATT_LOW_RT_STS	0x0: VBATT_LOW_RT_STS_FALSE 0x1: VBATT_LOW_RT_STS_TRUE
1	JEITA_SOFT_HOT_RT_STS	0x0: JEITA_SOFT_HOT_RT_STS_FALSE 0x1: JEITA_SOFT_HOT_RT_STS_TRUE
0	JEITA_SOFT_COLD_RT_STS	0x0: JEITA_SOFT_COLD_RT_STS_FALSE 0x1: JEITA_SOFT_COLD_RT_STS_TRUE

0x00004111 FG_BATT_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

0 = use level trigger interrupts, 1 = use edge trigger interrupts

FG_BATT_INT_SET_TYPE

Bits	Name	Description
7	BATT_MATCH_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE

FG_BATT_INT_SET_TYPE (cont.)

Bits	Name	Description
6	BATT_MISSING_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
5	BATT_UNKNOWN_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
4	BATT_ID_REQ_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
3	BATT_ID_DONE_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
2	VBATT_LOW_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
1	JEITA_SOFT_HOT_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
0	JEITA_SOFT_COLD_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE

0x00004112 FG_BATT_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

FG_BATT_INT_POLARITY_HIGH

Bits	Name	Description
7	BATT_MATCH_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
6	BATT_MISSING_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
5	BATT_UNKNOWN_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
4	BATT_ID_REQ_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
3	BATT_ID_DONE_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
2	VBATT_LOW_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

FG_BATT_INT_POLARITY_HIGH (cont.)

Bits	Name	Description
1	JEITA_SOFT_HOT_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
0	JEITA_SOFT_COLD_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x00004113 FG_BATT_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

FG_BATT_INT_POLARITY_LOW

Bits	Name	Description
7	BATT_MATCH_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
6	BATT_MISSING_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
5	BATT_UNKNOWN_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
4	BATT_ID_REQ_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
3	BATT_ID_DONE_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
2	VBATT_LOW_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
1	JEITA_SOFT_HOT_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
0	JEITA_SOFT_COLD_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x00004114 FG_BATT_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PMIC_ASYNC_PULSE_ONE

FG_BATT_INT_LATCHED_CLR

Bits	Name	Description
7	BATT_MATCH_INT_LATCHED_CLR	0x0: INT_LATCH_CLEAR_FALSE 0x1: INT_LATCH_CLEAR_TRUE
6	BATT_MISSING_INT_LATCHED_CLR	0x0: INT_LATCH_CLEAR_FALSE 0x1: INT_LATCH_CLEAR_TRUE
5	BATT_UNKNOWN_INT_LATCHED_CLR	0x0: INT_LATCH_CLEAR_FALSE 0x1: INT_LATCH_CLEAR_TRUE
4	BATT_ID_REQ_INT_LATCHED_CLR	0x0: INT_LATCH_CLEAR_FALSE 0x1: INT_LATCH_CLEAR_TRUE
3	BATT_ID_DONE_INT_LATCHED_CLR	0x0: INT_LATCH_CLEAR_FALSE 0x1: INT_LATCH_CLEAR_TRUE
2	VBATT_LOW_INT_LATCHED_CLR	0x0: INT_LATCH_CLEAR_FALSE 0x1: INT_LATCH_CLEAR_TRUE
1	JEITA_SOFT_HOT_INT_LATCHED_CLR	0x0: INT_LATCH_CLEAR_FALSE 0x1: INT_LATCH_CLEAR_TRUE
0	JEITA_SOFT_COLD_INT_LATCHED_CLR	0x0: INT_LATCH_CLEAR_FALSE 0x1: INT_LATCH_CLEAR_TRUE

0x00004115 FG_BATT_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

FG_BATT_INT_EN_SET

Bits	Name	Description
7	BATT_MATCH_INT_LATCHED_SET	0x0: INT_ENABLED_FALSE 0x1: INT_ENABLED_TRUE
6	BATT_MISSING_INT_LATCHED_SET	0x0: INT_ENABLED_FALSE 0x1: INT_ENABLED_TRUE
5	BATT_UNKNOWN_INT_LATCHED_SET	0x0: INT_ENABLED_FALSE 0x1: INT_ENABLED_TRUE
4	BATT_ID_REQ_INT_LATCHED_SET	0x0: INT_ENABLED_FALSE 0x1: INT_ENABLED_TRUE
3	BATT_ID_DONE_INT_LATCHED_SET	0x0: INT_ENABLED_FALSE 0x1: INT_ENABLED_TRUE
2	VBATT_LOW_INT_LATCHED_SET	0x0: INT_ENABLED_FALSE 0x1: INT_ENABLED_TRUE
1	JEITA_SOFT_HOT_INT_LATCHED_SET	0x0: INT_ENABLED_FALSE 0x1: INT_ENABLED_TRUE
0	JEITA_SOFT_COLD_INT_LATCHED_SET	0x0: INT_ENABLED_FALSE 0x1: INT_ENABLED_TRUE

0x00004116 FG_BATT_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

FG_BATT_INT_EN_CLR

Bits	Name	Description
7	BATT_MATCH_INT_EN_CLR	0x0: INT_DISABLED_FALSE 0x1: INT_DISABLED_TRUE
6	BATT_MISSING_INT_EN_CLR	0x0: INT_DISABLED_FALSE 0x1: INT_DISABLED_TRUE
5	BATT_UNKNOWN_INT_EN_CLR	0x0: INT_DISABLED_FALSE 0x1: INT_DISABLED_TRUE

FG_BATT_INT_EN_CLR (cont.)

Bits	Name	Description
4	BATT_ID_REQ_INT_EN_CLR	0x0: INT_DISABLED_FALSE 0x1: INT_DISABLED_TRUE
3	BATT_ID_DONE_INT_EN_CLR	0x0: INT_DISABLED_FALSE 0x1: INT_DISABLED_TRUE
2	VBATT_LOW_INT_EN_CLR	0x0: INT_DISABLED_FALSE 0x1: INT_DISABLED_TRUE
1	JEITA_SOFT_HOT_INT_EN_CLR	0x0: INT_DISABLED_FALSE 0x1: INT_DISABLED_TRUE
0	JEITA_SOFT_COLD_INT_EN_CLR	0x0: INT_DISABLED_FALSE 0x1: INT_DISABLED_TRUE

0x00004118 FG_BATT_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

FG_BATT_INT_LATCHED_STS

Bits	Name	Description
7	BATT_MATCH_INT_LATCHED_STS	0x0: INT_TRIGGERED_FALSE 0x1: INT_TRIGGERED_TRUE
6	BATT_MISSING_INT_LATCHED_STS	0x0: INT_TRIGGERED_FALSE 0x1: INT_TRIGGERED_TRUE
5	BATT_UNKNOWN_INT_LATCHED_STS	0x0: INT_TRIGGERED_FALSE 0x1: INT_TRIGGERED_TRUE
4	BATT_ID_REQ_INT_LATCHED_STS	0x0: INT_TRIGGERED_FALSE 0x1: INT_TRIGGERED_TRUE
3	BATT_ID_DONE_INT_LATCHED_STS	0x0: INT_TRIGGERED_FALSE 0x1: INT_TRIGGERED_TRUE
2	VBATT_LOW_INT_LATCHED_STS	0x0: INT_TRIGGERED_FALSE 0x1: INT_TRIGGERED_TRUE
1	JEITA_SOFT_HOT_INT_LATCHED_STS	0x0: INT_TRIGGERED_FALSE 0x1: INT_TRIGGERED_TRUE

FG_BATT_INT_LATCHED_STS (cont.)

Bits	Name	Description
0	JEITA_SOFT_COLD_INT_LATCHED_STS	0x0: INT_TRIGGERED_FALSE 0x1: INT_TRIGGERED_TRUE

0x00004119 FG_BATT_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Debug: Pending is set if interrupt has been sent but not cleared.

FG_BATT_INT_PENDING_STS

Bits	Name	Description
7	BATT_MATCH_INT_PENDING_STS	0x0: INT_PENDING_FALSE 0x1: INT_PENDING_TRUE
6	BATT_MISSING_INT_PENDING_STS	0x0: INT_PENDING_FALSE 0x1: INT_PENDING_TRUE
5	BATT_UNKNOWN_INT_PENDING_STS	0x0: INT_PENDING_FALSE 0x1: INT_PENDING_TRUE
4	BATT_ID_REQ_INT_PENDING_STS	0x0: INT_PENDING_FALSE 0x1: INT_PENDING_TRUE
3	BATT_ID_DONE_INT_PENDING_STS	0x0: INT_PENDING_FALSE 0x1: INT_PENDING_TRUE
2	VBATT_LOW_INT_PENDING_STS	0x0: INT_PENDING_FALSE 0x1: INT_PENDING_TRUE
1	JEITA_SOFT_HOT_INT_PENDING_STS	0x0: INT_PENDING_FALSE 0x1: INT_PENDING_TRUE
0	JEITA_SOFT_COLD_INT_PENDING_STS	0x0: INT_PENDING_FALSE 0x1: INT_PENDING_TRUE

0x0000411A FG_BATT_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Selects the MID that will receive the interrupt

FG_BATT_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x0000411B FG_BATT_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

SR=0 A=1

FG_BATT_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: INT_PRIORITY0 0x1: INT_PRIORITY1

0x00004150 FG_BATT_SW_BATT_ID

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

PMIC_SYNC=fg_clk_1mhz_g:dVdd_rb

FG_BATT_SW_BATT_ID

Bits	Name	Description
7	FORCE	Force the Battery ID during a First SoC re-detection 0x0: FORCE_BATID_FALSE 0x1: FORCE_BATID_TRUE

0x00004152 FG_BATT_BATT_REMOVED_LATCHED

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: dVdd_rb

FG_BATT_BATT_REMOVED_LATCHED

Bits	Name	Description
7	CLR	Writing a 1, will clear FG_BATT_SYS_BATT.BATT_REMOVED_LATCH; If battery remains missing, the latch will get set again 0x0: BATT_REMOVED_LATCH_CLEAR_FALSE 0x1: BATT_REMOVED_LATCH_CLEAR_TRUE

30 FG_ADC_USR_FG_ADC

0x00004204 FG_ADC_USR_PERPH_TYPE

Type: R
Clock: pbus_wrclk
Reset State: 0x0D

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

FG_ADC_USR_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	FG_ADC

0x00004205 FG_ADC_USR_PERPH_SUBTYPE

Type: R
Clock: pbus_wrclk
Reset State: 0x0B

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

FG_ADC_USR_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	FG_ADC

0x00004210 FG_ADC_USR_INT_RT_STS

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Interrupt Real Time Status Bits

FG_ADC_USR_INT_RT_STS

Bits	Name	Description
1	VBAT_LT_THR_INT_RT_STS	IRQ indicating that VBAT is less than threshold defined in VBAT_INT__THR register 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
0	IBAT_GT_THR_RT_STS	IRQ indicating that IBAT is greater than threshold defined in IBAT_INT__THR register 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH

0x00004211 FG_ADC_USR_INT_SET_TYPE

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

0 = use level trigger interrupts, 1 = use edge trigger interrupts

FG_ADC_USR_INT_SET_TYPE

Bits	Name	Description
1	VBAT_LT_THR_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
0	IBAT_GT_THR_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE

0x00004212 FG_ADC_USR_INT_POLARITY_HIGH

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

FG_ADC_USR_INT_POLARITY_HIGH

Bits	Name	Description
1	VBAT_LT_THR_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
0	IBAT_GT_THR_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x00004213 FG_ADC_USR_INT_POLARITY_LOW

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

FG_ADC_USR_INT_POLARITY_LOW

Bits	Name	Description
1	VBAT_LT_THR_INT_HIGH	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
0	IBAT_GT_THR_INT_HIGH	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x00004214 FG_ADC_USR_INT_LATCHED_CLR

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PMIC_ASYNC_PULSE_ONE

FG_ADC_USR_INT_LATCHED_CLR

Bits	Name	Description
1	VBAT_LT_THR_INT_LATCHED_CLR	

FG_ADC_USR_INT_LATCHED_CLR (cont.)

Bits	Name	Description
0	IBAT_GT_THR_INT_LATCHED_CLR	

0x00004215 FG_ADC_USR_INT_EN_SET

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

FG_ADC_USR_INT_EN_SET

Bits	Name	Description
1	VBAT_LT_THR_INT_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
0	IBAT_GT_THR_INT_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED

0x00004216 FG_ADC_USR_INT_EN_CLR

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

FG_ADC_USR_INT_EN_CLR

Bits	Name	Description
1	VBAT_LT_THR_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
0	IBAT_GT_THR_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

0x00004218 FG_ADC_USR_INT_LATCHED_STS

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

FG_ADC_USR_INT_LATCHED_STS

Bits	Name	Description
1	VBAT_LT_THR_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
0	IBAT_GT_THR_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

0x00004219 FG_ADC_USR_INT_PENDING_STS

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Debug: Pending is set if interrupt has been sent but not cleared.

FG_ADC_USR_INT_PENDING_STS

Bits	Name	Description
1	VBAT_LT_THR_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
0	IBAT_GT_THR_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

0x0000421A FG_ADC_USR_INT_MID_SEL

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Selects the MID that will receive the interrupt

FG_ADC_USR_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x0000421B FG_ADC_USR_INT_PRIORITY

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

FG_ADC_USR_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR 0x1: A

0x00004246 FG_ADC_USR_EN_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x80

Reset Name: perph_rb

FG_ADC_USR_EN_CTL

Bits	Name	Description
7	FG_ADC_EN	Enables FG_ADC module for Battery Current Limiting (BCL) S/W use 0x0: BCL_MONITORING_DISABLE 0x1: BCL_MONITORING_ENABLE

0x00004253 FG_ADC_USR_BCL_VALUES

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

FG_ADC_USR_BCL_VALUES

Bits	Name	Description
7	RDY	After the first readings from ADC are obtained, this bit is set to 1; At reset and shutdown, this bit gets automatically cleared; Once ready, inhibit does not have an effect 0x0 : NOT_RDY 0x1 : RDY
6	V_RDY	After the first readings from vADC are obtained, this bit is set to 1; At reset and shutdown, this bit gets automatically cleared; Once ready, inhibit does not have an effect 0x0 : NOT_RDY 0x1 : RDY
5	V_INBT	Behaves similarly to I_INBT; Additionally it is paused, when thermistor/usbID readings are taken 0x0 : NOT_INBT 0x1 : INBT
4	V_LAG	When iAdc readings are obtained alone, without vAdc readings due to its inhibit, then it is true, until the readings are obtained 0x0 : INPHASE 0x1 : LAG
3	I_RDY	After the first readings from iADC are obtained, this bit is set to 1; At reset and shutdown, this bit gets automatically cleared; Once ready, inhibit does not have an effect 0x0 : NOT_RDY 0x1 : RDY
2	I_INBT	iAdc conversions are paused ~1 s for power savings, during LPM mode only 0x0 : NOT_INBT 0x1 : INBT

0x00004254 FG_ADC_USR_VBAT

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_VBAT

Bits	Name	Description
7:0	STS	8 bit signed partial ADC value, MSB = 0 is positive voltage (positive number), 1 LSB = 39 mV

0x00004255 FG_ADC_USR_IBAT

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_IBAT

Bits	Name	Description
7:0	STS	8 bit signed partial ADC value, MSB = 0 is discharging current (positive number), 1 LSB = 39 mA

0x00004256 FG_ADC_USR_VBAT_CP

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_VBAT_CP

Bits	Name	Description
7:0	STS	Copy of register VBAT; Burst read, compare for match

0x00004257 FG_ADC_USR_IBAT_CP

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_IBAT_CP

Bits	Name	Description
7:0	STS	Copy of register IBAT; Burst read, compare for match

0x00004258 FG_ADC_USR_VBAT_MIN

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_VBAT_MIN

Bits	Name	Description
7:0	STS	Running Vbat Min stored and then cleared by SW

0x00004259 FG_ADC_USR_IBAT_MAX

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_IBAT_MAX

Bits	Name	Description
7:0	STS	Running Ibat Max stored and then cleared by SW; Only positive discharge currents are logged

0x0000425A FG_ADC_USR_VBAT_MIN_CP

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_VBAT_MIN_CP

Bits	Name	Description
7:0	STS	Copy of register VBAT_MIN; Burst read, compare for match

0x0000425B FG_ADC_USR_IBAT_MAX_CP

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_IBAT_MAX_CP

Bits	Name	Description
7:0	STS	Copy of register IBAT_MAX; Burst read, compare for match

0x0000425C FG_ADC_USR_BAT_RES_7_0

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_BAT_RES_7_0

Bits	Name	Description
7:0	STS	Battery resistance; HALF-FLOATING point encoding, 15:11 exp, bit 10 sign, 9:0 mantissa, 1=1 ohm

0x0000425D FG_ADC_USR_BAT_RES_15_8

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_BAT_RES_15_8

Bits	Name	Description
7:0	STS	Battery resistance; HALF-FLOATING point encoding, 15:11 exp, bit 10 sign, 9:0 mantissa, 1=1 ohm

0x0000425E FG_ADC_USR_BCL_MODE

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: perph_rb

FG_ADC_USR_BCL_MODE

Bits	Name	Description
7:6	STS	00 = lpm - low power mode 01 = hpm - high power mode 10 = mpm - medium (normal) power mode 11 = not used 0x0: BCL_IS_LPM 0x1: BCL_IS_HPM 0x2: BCL_IS_MPM 0x3: BCL_IS_INVALID_MODE

0x00004260 FG_ADC_USR_BCL_V_GAIN_BATT

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_BCL_V_GAIN_BATT

Bits	Name	Description
7:0	STS	Gain correction for Battery Voltage, [MSB] = SIGN, 1 = negative

0x00004261 FG_ADC_USR_BCL_I_GAIN_RSENSE

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_BCL_I_GAIN_RSENSE

Bits	Name	Description
7:0	STS	Gain correction for Battery Current, external sensing, [MSB] = SIGN, 1 = negative

0x00004262 FG_ADC_USR_BCL_I_OFFSET_RSENSE

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_BCL_I_OFFSET_RSENSE

Bits	Name	Description
7:0	STS	[MSB] = SIGN, 1 = negative

0x00004263 FG_ADC_USR_BCL_I_GAIN_BATFET

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_BCL_I_GAIN_BATFET

Bits	Name	Description
7:0	STS	Gain correction for Battery Current, internal sensing, [MSB] = SIGN: 1 = negative

0x00004264 FG_ADC_USR_BCL_I_OFFSET_BATFET

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_BCL_I_OFFSET_BATFET

Bits	Name	Description
7:0	STS	[MSB] = SIGN, 1 = negative

0x00004265 FG_ADC_USR_BCL_I_SENSE_SOURCE

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_USR_BCL_I_SENSE_SOURCE

Bits	Name	Description
0	STS	Source used for current sense

0x00004266 FG_ADC_USR_VBAT_MIN_CLR

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

FG_ADC_USR_VBAT_MIN_CLR

Bits	Name	Description
7	CTL	Any write to this register clears stored running Vbat Min value

0x00004267 FG_ADC_USR_IBAT_MAX_CLR

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

FG_ADC_USR_IBAT_MAX_CLR

Bits	Name	Description
7	CTL	Any write to this register clears stored running Ibat Max value

0x00004268 FG_ADC_USR_VBAT_INT

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Settable threshold for interrupt

FG_ADC_USR_VBAT_INT

Bits	Name	Description
7:0	THR	8 bit signed partial ADC value, MSB = 0 is positive voltage (positive number), only positive voltages are compared, 1 LSB = 39 mV

0x00004269 FG_ADC_USR_IBAT_INT

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Settable threshold for interrupt

FG_ADC_USR_IBAT_INT

Bits	Name	Description
7:0	THR	8 bit signed partial ADC value, MSB = 0 is discharging current (positive number), only discharging currents are compared, 1 LSB = 39 mA

31 FG_ADC_MDM_FG_ADC

0x00004304 FG_ADC_MDM_PERPH_TYPE

Type: R
Clock: pbus_wrclk
Reset State: 0x0D

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

FG_ADC_MDM_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	FG_ADC

0x00004305 FG_ADC_MDM_PERPH_SUBTYPE

Type: R
Clock: pbus_wrclk
Reset State: 0x0B

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

FG_ADC_MDM_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	FG_ADC

0x00004310 FG_ADC_MDM_INT_RT_STS

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Interrupt Real Time Status Bits

FG_ADC_MDM_INT_RT_STS

Bits	Name	Description
1	VBAT_LT_THR_INT_RT_STS	IRQ indicating that VBAT is less than threshold defined in VBAT_INT__THR register 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
0	IBAT_GT_THR_RT_STS	IRQ indicating that IBAT is greater than threshold defined in IBAT_INT__THR register 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH

0x00004311 FG_ADC_MDM_INT_SET_TYPE

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

0 = use level trigger interrupts, 1 = use edge trigger interrupts

FG_ADC_MDM_INT_SET_TYPE

Bits	Name	Description
1	VBAT_LT_THR_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
0	IBAT_GT_THR_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE

0x00004312 FG_ADC_MDM_INT_POLARITY_HIGH

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

FG_ADC_MDM_INT_POLARITY_HIGH

Bits	Name	Description
1	VBAT_LT_THR_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
0	IBAT_GT_THR_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x00004313 FG_ADC_MDM_INT_POLARITY_LOW

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

FG_ADC_MDM_INT_POLARITY_LOW

Bits	Name	Description
1	VBAT_LT_THR_INT_HIGH	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
0	IBAT_GT_THR_INT_HIGH	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x00004314 FG_ADC_MDM_INT_LATCHED_CLR

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PMIC_ASYNC_PULSE_ONE

FG_ADC_MDM_INT_LATCHED_CLR

Bits	Name	Description
1	VBAT_LT_THR_INT_LATCHED_CLR	

FG_ADC_MDM_INT_LATCHED_CLR (cont.)

Bits	Name	Description
0	IBAT_GT_THR_INT_LATCHED_CLR	

0x00004315 FG_ADC_MDM_INT_EN_SET

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

FG_ADC_MDM_INT_EN_SET

Bits	Name	Description
1	VBAT_LT_THR_INT_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED
0	IBAT_GT_THR_INT_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED

0x00004316 FG_ADC_MDM_INT_EN_CLR

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

FG_ADC_MDM_INT_EN_CLR

Bits	Name	Description
1	VBAT_LT_THR_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
0	IBAT_GT_THR_INT_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

0x00004318 FG_ADC_MDM_INT_LATCHED_STS

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

FG_ADC_MDM_INT_LATCHED_STS

Bits	Name	Description
1	VBAT_LT_THR_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
0	IBAT_GT_THR_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

0x00004319 FG_ADC_MDM_INT_PENDING_STS

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Debug: Pending is set if interrupt has been sent but not cleared.

FG_ADC_MDM_INT_PENDING_STS

Bits	Name	Description
1	VBAT_LT_THR_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
0	IBAT_GT_THR_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

0x0000431A FG_ADC_MDM_INT_MID_SEL

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Selects the MID that will receive the interrupt

FG_ADC_MDM_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x0000431B FG_ADC_MDM_INT_PRIORITY

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

FG_ADC_MDM_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR 0x1: A

0x00004346 FG_ADC_MDM_EN_CTL

Type: RW
Clock: pbus_wrclk
Reset State: 0x80

Reset Name: perph_rb

FG_ADC_MDM_EN_CTL

Bits	Name	Description
7	FG_ADC_EN	Enables FG_ADC module for Battery Current Limiting (BCL) S/W use 0x0: BCL_MONITORING_DISABLE 0x1: BCL_MONITORING_ENABLE

0x00004353 FG_ADC_MDM_BCL_VALUES

Type: R
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

FG_ADC_MDM_BCL_VALUES

Bits	Name	Description
7	RDY	After the first readings from ADC are obtained, this bit is set to 1; At reset and shutdown, this bit gets automatically cleared; Once ready, inhibit does not have an effect 0x0 : NOT_RDY 0x1 : RDY
6	V_RDY	After the first readings from vADC are obtained, this bit is set to 1; At reset and shutdown, this bit gets automatically cleared; Once ready, inhibit does not have an effect 0x0 : NOT_RDY 0x1 : RDY
5	V_INBT	Behaves similarly to I_INBT; Additionally it is paused, when thermistor/usbID readings are taken 0x0 : NOT_INBT 0x1 : INBT
4	V_LAG	When iAdc readings are obtained alone, without vAdc readings due to its inhibit, then it is true, until the readings are obtained 0x0 : INPHASE 0x1 : LAG
3	I_RDY	After the first readings from iADC are obtained, this bit is set to 1; At reset and shutdown, this bit gets automatically cleared; Once ready, inhibit does not have an effect 0x0 : NOT_RDY 0x1 : RDY
2	I_INBT	iAdc conversions are paused ~1 s for power savings, during LPM mode only 0x0 : NOT_INBT 0x1 : INBT

0x00004354 FG_ADC_MDM_VBAT

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_VBAT

Bits	Name	Description
7:0	STS	8 bit signed partial ADC value, MSB = 0 is positive voltage (positive number), 1 LSB = 39 mV

0x00004355 FG_ADC_MDM_IBAT

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_IBAT

Bits	Name	Description
7:0	STS	8 bit signed partial ADC value, MSB = 0 is discharging current (positive number), 1 LSB = 39 mA

0x00004356 FG_ADC_MDM_VBAT_CP

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_VBAT_CP

Bits	Name	Description
7:0	STS	Copy of register VBAT; Burst read, compare for match

0x00004357 FG_ADC_MDM_IBAT_CP

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_IBAT_CP

Bits	Name	Description
7:0	STS	Copy of register IBAT; Burst read, compare for match

0x00004358 FG_ADC_MDM_VBAT_MIN

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_VBAT_MIN

Bits	Name	Description
7:0	STS	Running Vbat Min stored and then cleared by SW

0x00004359 FG_ADC_MDM_IBAT_MAX

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_IBAT_MAX

Bits	Name	Description
7:0	STS	Running Ibat Max stored and then cleared by SW; Only positive discharge currents are logged

0x0000435A FG_ADC_MDM_VBAT_MIN_CP

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_VBAT_MIN_CP

Bits	Name	Description
7:0	STS	Copy of register VBAT_MIN; Burst read, compare for match

0x0000435B FG_ADC_MDM_IBAT_MAX_CP

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_IBAT_MAX_CP

Bits	Name	Description
7:0	STS	Copy of register IBAT_MAX; Burst read, compare for match

0x0000435C FG_ADC_MDM_BAT_RES_7_0

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_BAT_RES_7_0

Bits	Name	Description
7:0	STS	Battery resistance; HALF-FLOATING point encoding, 15:11 exp, bit 10 sign, 9:0 mantissa, 1=1 ohm

0x0000435D FG_ADC_MDM_BAT_RES_15_8

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_BAT_RES_15_8

Bits	Name	Description
7:0	STS	Battery resistance; HALF-FLOATING point encoding, 15:11 exp, bit 10 sign, 9:0 mantissa, 1=1 ohm

0x0000435E FG_ADC_MDM_BCL_MODE

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: perph_rb

FG_ADC_MDM_BCL_MODE

Bits	Name	Description
7:6	STS	00 = lpm - low power mode 01 = hpm - high power mode 10 = mpm - medium (normal) power mode 11 = not used 0x0: BCL_IS_LPM 0x1: BCL_IS_HPM 0x2: BCL_IS_MPM 0x3: BCL_IS_INVALID_MODE

0x00004360 FG_ADC_MDM_BCL_V_GAIN_BATT

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_BCL_V_GAIN_BATT

Bits	Name	Description
7:0	STS	Gain correction for Battery Voltage, [MSB] = SIGN, 1 = negative

0x00004361 FG_ADC_MDM_BCL_I_GAIN_RSENSE

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_BCL_I_GAIN_RSENSE

Bits	Name	Description
7:0	STS	Gain correction for Battery Current, external sensing, [MSB] = SIGN, 1 = negative

0x00004362 FG_ADC_MDM_BCL_I_OFFSET_RSENSE

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_BCL_I_OFFSET_RSENSE

Bits	Name	Description
7:0	STS	[MSB] = SIGN, 1 = negative

0x00004363 FG_ADC_MDM_BCL_I_GAIN_BATFET

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_BCL_I_GAIN_BATFET

Bits	Name	Description
7:0	STS	Gain correction for Battery Current, internal sensing, [MSB] = SIGN: 1 = negative

0x00004364 FG_ADC_MDM_BCL_I_OFFSET_BATFET

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_BCL_I_OFFSET_BATFET

Bits	Name	Description
7:0	STS	[MSB] = SIGN, 1 = negative

0x00004365 FG_ADC_MDM_BCL_I_SENSE_SOURCE

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

FG_ADC_MDM_BCL_I_SENSE_SOURCE

Bits	Name	Description
0	STS	Source used for current sense

0x00004366 FG_ADC_MDM_VBAT_MIN_CLR

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

FG_ADC_MDM_VBAT_MIN_CLR

Bits	Name	Description
7	CTL	Any write to this register clears stored running Vbat Min value

0x00004367 FG_ADC_MDM_IBAT_MAX_CLR

Type: W
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

FG_ADC_MDM_IBAT_MAX_CLR

Bits	Name	Description
7	CTL	Any write to this register clears stored running Ibat Max value

0x00004368 FG_ADC_MDM_VBAT_INT

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Settable threshold for interrupt

FG_ADC_MDM_VBAT_INT

Bits	Name	Description
7:0	THR	8 bit signed partial ADC value, MSB = 0 is positive voltage (positive number), only positive voltages are compared, 1 LSB = 39 mV

0x00004369 FG_ADC_MDM_IBAT_INT

Type: RW
Clock: pbus_wrclk
Reset State: 0x00

Reset Name: perph_rb

Settable threshold for interrupt

FG_ADC_MDM_IBAT_INT

Bits	Name	Description
7:0	THR	8 bit signed partial ADC value, MSB = 0 is discharging current (positive number), only discharging currents are compared, 1 LSB = 39 mA

32 FG_MEMIF_FG_MEMIF

0x00004400 FG_MEMIF_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

FG_MEMIF_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00004401 FG_MEMIF_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x03

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

FG_MEMIF_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x00004402 FG_MEMIF_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: N/A

HW Version Register [23:16]

FG_MEMIF_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x00004403 FG_MEMIF_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [31:24]

FG_MEMIF_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x00004404 FG_MEMIF_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x0D

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

FG_MEMIF_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	

0x00004405 FG_MEMIF_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x0C

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

FG_MEMIF_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	

0x00004410 FG_MEMIF_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Interrupt Real Time Status Bits

FG_MEMIF_INT_RT_STS

Bits	Name	Description
2	Reserved	Reserved
1	Reserved	Reserved
0	FG_MEM_RT_STS	For conventional memory access (CMA), behaves as Memory Available; For IMA, behaves as Ready/End of Transaction depending on configuration 0x0: FG_MEM_ST0 0x1: FG_MEM_ST1

0x00004411 FG_MEMIF_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

0 = use level trigger interrupts, 1 = use edge trigger interrupts

FG_MEMIF_INT_SET_TYPE

Bits	Name	Description
2	Reserved	Reserved
1	Reserved	Reserved
0	FG_MEM_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE

0x00004412 FG_MEMIF_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

FG_MEMIF_INT_POLARITY_HIGH

Bits	Name	Description
2	Reserved	Reserved
1	Reserved	Reserved
0	FG_MEM_INT_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x00004413 FG_MEMIF_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

FG_MEMIF_INT_POLARITY_LOW

Bits	Name	Description
2	Reserved	Reserved
1	Reserved	Reserved
0	FG_MEM_INT_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x00004414 FG_MEMIF_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

PMIC_ASYNC_PULSE_ONE

FG_MEMIF_INT_LATCHED_CLR

Bits	Name	Description
2	Reserved	Reserved
1	Reserved	Reserved
0	FG_MEM_INT_LATCHED_CLR	0x0: INT_LATCH_CLEAR_FALSE 0x1: INT_LATCH_CLEAR_TRUE

0x00004415 FG_MEMIF_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

FG_MEMIF_INT_EN_SET

Bits	Name	Description
2	Reserved	Reserved
1	Reserved	Reserved
0	FG_MEM_INT_EN_SET	0x0: INT_ENABLED_FALSE 0x1: INT_ENABLED_TRUE

0x00004416 FG_MEMIF_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

FG_MEMIF_INT_EN_CLR

Bits	Name	Description
2	Reserved	Reserved
1	Reserved	Reserved
0	FG_MEM_INT_EN_CLR	0x0: INT_DISABLED_FALSE 0x1: INT_DISABLED_TRUE

0x00004418 FG_MEMIF_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

FG_MEMIF_INT_LATCHED_STS

Bits	Name	Description
2	Reserved	Reserved
1	Reserved	Reserved

FG_MEMIF_INT_LATCHED_STS (cont.)

Bits	Name	Description
0	FG_MEM_INT_LATCHED_STS	0x0: INT_TRIGGERED_FALSE 0x1: INT_TRIGGERED_TRUE

0x00004419 FG_MEMIF_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Debug: Pending is set if interrupt has been sent but not cleared.

FG_MEMIF_INT_PENDING_STS

Bits	Name	Description
2	Reserved	Reserved
1	Reserved	Reserved
0	FG_MEM_INT_PENDING_STS	0x0: INT_PENDING_FALSE 0x1: INT_PENDING_TRUE

0x0000441A FG_MEMIF_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

Selects the MID that will receive the interrupt

FG_MEMIF_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x0000441B FG_MEMIF_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: perph_rb

SR=0 A=1

FG_MEMIF_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: INT_PRIORITY0 0x1: INT_PRIORITY1

0x00004450 FG_MEMIF_MEM_INTF_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Memory Interface Configuration

FG_MEMIF_MEM_INTF_CFG

Bits	Name	Description
7	RIF_MEM_ACCESS_REQ	Enables RIF memory interface and the RIF Memory Access Mode 0x0: RIF_MEM_ACCESS_REQ_FALSE 0x1: RIF_MEM_ACCESS_REQ_TRUE
6	LOW_LATENCY_ACS_EN	Applicable to Conventional access mode only; 1: RIF is granted access to FG memory any time during long CC conversion period rather than at the beginning of this period. Helps in reducing latency for access to FG Memory; Has potential to extend FG cycle and upset SoC estimation. To be used sparingly, preferably at boot only 0x0: LOW_LATENCY_ACS_EN_FALSE 0x1: LOW_LATENCY_ACS_EN_TRUE
5	IACS_SLCT	0: Conventional memory access mode; 1: Interleave memory access (IMA) mode 0x0: CONVENTIONAL_ACS_MODE 0x1: INTERLEAVE_ACS_MODE

0x00004451 FG_MEMIF_MEM_INTF_CTL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Memory Interface Control

PMIC_SYNC=clk:dVdd_rb

FG_MEMIF_MEM_INTF_CTL

Bits	Name	Description
7	BURST	Defines Single/Burst Access 0x0: MEM_ACS_SINGLE 0x1: MEM_ACS_BURST
6	WR_EN	Defines Write/Read Access 0x0: READ_ACCESS 0x1: WRITE_ACCESS

0x00004452 FG_MEMIF_IMA_CFG

Type: RW
Clock: pbus_wrclk
Reset State: 0x10

Reset Name: perph_rb

Interleave memory access configuration

FG_MEMIF_IMA_CFG

Bits	Name	Description
7	CFG_FGXCT_PRD	Configure FG transaction period; 0: Just the SoC computation period (higher performance) 1: All time periods FG is active (access period) - superset of compute period 0x0: SOC_COMPUTE_PRD 0x1: FG_ACS_PRD
6	EN_WR_FGXCT_PRD	0: Write request from SPMI/pBus is kept pending until FG exits its transaction period and is then executed; 1: Write transaction from SPMI/pBus is executed any time including FG transactions period; 0x0: DISABLE_WR_FGXCT_PRD 0x1: ENABLE_WR_FGXCT_PRD

FG_MEMIF_IMA_CFG (cont.)

Bits	Name	Description
5	EN_RD_FGXCT_PRD	0: Read request from SPMI/pBus is kept pending until FG exits its transaction period and is then executed; 1: Read transaction from SPMI/pBus is executed any time including FG transactions period; 0x0: DISABLE_RD_FGXCT_PRD 0x1: ENABLE_RD_FGXCT_PRD
4	STATIC_CLK_EN	Timing of clock access request; 0: Dynamic - only when transaction is pending; 1: Static - when interleave access is enabled 0x0: IACS_DYNAMIC_CLK_EN 0x1: IACS_STATIC_CLK_EN
3	IACS_INTR_SRC_SLCT	Interrupt source; 0: End of transaction; 1: Interleave access ready (note: when interleave access is not pending it will assert true) 0x0: END_OF_TRANSACTION 0x1: IACS_RDY
2	IACS_CLR	Interleave access sub-system clear; 0: Normal operation; 1: Clear operation; If a SPMI/pBus transaction is issued, even before the previous transaction completes, it will result in error. Please see register IMA_EXCEPTION_STS; To clear the error set this bit to 1 and perform these transactions to reset the sub-system; write to adrsMsbRg, dataWrMsbRg; read from dataRdMsbRg; Then clear this bit back to 0 0x0: IACS_NORMAL_MODE 0x1: IACS_CLEAR_MODE

0x00004454 FG_MEMIF_IMA_OPERATION_STS

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

Interleave memory access operation status

FG_MEMIF_IMA_OPERATION_STS

Bits	Name	Description
7	FGXCT_PRD	Fuel gauge is in transaction period, accessing memory frequently and changing variables 0x0: FG_FREE_PRD 0x1: FG_XCT_PERIOD
6	WR_FGXCT_PRD_LOG	Log indicating memory write occurred during transaction period 0x0: INTERLEAVE_WR_FGFREE_PRD 0x1: INTERLEAVE_WR_FGXCT_PRD

FG_MEMIF_IMA_OPERATION_STS (cont.)

Bits	Name	Description
5	RD_FGXCT_PRD_LOG	Log indicating memory read occurred during transaction period 0x0: INTERLEAVE_RD_FGFREE_PRD 0x1: INTERLEAVE_RD_FGXCT_PRD
4	IACS_CLK_REQ	Interleave access logic has requested clock for operation 0x0: INTERLEAVE_ACS_CLK_REQ_IDLE 0x1: INTERLEAVE_ACS_CLK_REQ_ACTIVE
3	IACS_INTR_STS	Interleave access logic has asserted access interrupt; fleeting if end of transaction is used as interrupt source and hence use IACS_RDY; Excludes IMA exception interrupt 0x0: IACS_INTR_IDLE 0x1: IACS_INTR_PENDING
2	CACS_INTR_STS	Conventional access logic has asserted memory available interrupt 0x0: CACS_INTR_IDLE 0x1: CACS_INTR_PENDING
1	IACS_RDY	Interleave access not pending and is ready to accept new transaction request; Becomes true only if IMA is enabled 0x0: INTERLEAVE_ACS_IN_PROGRESS 0x1: INTERLEAVE_ACS_IDLE

0x00004455 FG_MEMIF_IMA_EXCEPTION_STS

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

Interleave memory access exception status

FG_MEMIF_IMA_EXCEPTION_STS

Bits	Name	Description
7	ADDR_SRC_ERR	Address changed by register write in midst of transaction; previous transaction not over 0x0: NO_ERR 0x1: ERR
6	ADDR_RNG_ERR	Address range improper for access 0x0: NO_ERR 0x1: ERR
5	ADDR_BURST_WRAP	Address wrapped around for burst access; not implemented yet 0x0: NO_WRAP 0x1: WRAP

FG_MEMIF_IMA_EXCEPTION_STS (cont.)

Bits	Name	Description
4	DATA_WR_ERR	Data changed by register write in midst of write transaction; previous transaction not over 0x0: NO_ERR 0x1: ERR
3	DATA_RD_ERR	Data read in midst of read transaction, previous transaction not over 0x0: NO_ERR 0x1: ERR
2	BE_BURSTWR_WARN	For burst writes, BE is typically expected to be all 1, if not a warning; not implemented yet 0x0: NO_WARN 0x1: WARN
1	XCT_TYPE_ERR	Read/Write control changed in midst of transaction, previous transaction not over; not implemented yet 0x0: NO_ERR 0x1: ERR
0	IACS_ERR	iAcs transaction encountered error; Please execute clear sequence 0x0: NO_ERR 0x1: ERR

0x00004456 FG_MEMIF_IMA_HARDWARE_STS

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

Interleave memory access hardware status

FG_MEMIF_IMA_HARDWARE_STS

Bits	Name	Description
7	ADDR_MSB_WR_TGL	Toggles (changes state 0->1, 1->0) upon write to addrMsbRg; triggers read interleave memory access 0x0: ST0 0x1: ST1
6	DATA_MSB_WR_TGL	Toggles (changes state 0->1, 1->0) upon write to dataMsbWrRg; triggers write interleave access 0x0: ST0 0x1: ST1

FG_MEMIF_IMA_HARDWARE_STS (cont.)

Bits	Name	Description
5	DATA_MSB_RD_TGL	Toggles (changes state 0->1, 1->0) upon read to dataMsbRdRg, triggers burst read interleave access 0x0: ST0 0x1: ST1
4	RESERVED4	reserved
3	ADDR_MSB_WR_TGL_RCV	Acquires the state of addrMsbWrTgl upon completion of interleave memory transaction 0x0: ST0 0x1: ST1
2	DATA_MSB_WR_TGL_RCV	Acquires the state of dataMsbWrTgl upon completion of write interleave memory transaction 0x0: ST0 0x1: ST1
1	DATA_MSB_RD_TGL_RCV	Acquires the state of dataMsbRdTgl upon completion of read interleave memory transaction 0x0: ST0 0x1: ST1
0	RESERVED0	reserved

0x00004457 FG_MEMIF_FG_BEAT_COUNT

Type: R
Clock: pbus_wrclk
Reset State: Undefined

Reset Name: N/A

Fuel gauge beat count: cnt++ @begin and again @end of computation period

FG_MEMIF_FG_BEAT_COUNT

Bits	Name	Description
3:0	BEAT_CNT	FG beat count; increments twice every period; For multi location access, read before and after; Should match for integrity, else discard and re-read

0x00004460 FG_MEMIF_IMA_BYTE_EN

Type: RW
Clock: pbus_wrclk
Reset State: 0x0F

Reset Name: perph_rb

Interleave memory write access byte enables

FG_MEMIF_IMA_BYTE_EN

Bits	Name	Description
3	BE3	Enable write of data[31:24], mem_intf_wr_data_3, interleave access only 0x0: BE3_DSBL 0x1: BE3_EN
2	BE2	Enable write of data[23:16], mem_intf_wr_data_2, interleave access only 0x0: BE2_DSBL 0x1: BE2_EN
1	BE1	Enable write of data[15:8], mem_intf_wr_data_1, interleave access only 0x0: BE1_DSBL 0x1: BE1_EN
0	BE0	Enable write of data[7:0], mem_intf_wr_data_0, interleave access only 0x0: BE0_DSBL 0x1: BE0_EN

0x00004461 FG_MEMIF_MEM_INTF_ADDR_LSB

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Memory Interface Address[7:0]

FG_MEMIF_MEM_INTF_ADDR_LSB

Bits	Name	Description
7:0	MEM_INTF_ADDR_LSB	Address for Single Memory Access. Initial Address for Burst Memory Access.

0x00004462 FG_MEMIF_MEM_INTF_ADDR_MSB

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Memory Interface Address[15:8]

FG_MEMIF_MEM_INTF_ADDR_MSB

Bits	Name	Description
7:0	MEM_INTF_ADDR_MSB	Address for Single Memory Access. Initial Address for Burst Memory Access. OTP memory starts at address 0. RAM starts at address 0x400.

0x00004463 FG_MEMIF_MEM_INTF_WR_DATA0

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Write Data [7:0]

FG_MEMIF_MEM_INTF_WR_DATA0

Bits	Name	Description
7:0	MEM_INTF_WR_DATA_0	Memory Interface Write Data

0x00004464 FG_MEMIF_MEM_INTF_WR_DATA1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Write Data [15:8]

FG_MEMIF_MEM_INTF_WR_DATA1

Bits	Name	Description
7:0	MEM_INTF_WR_DATA_1	Memory Interface Write Data

0x00004465 FG_MEMIF_MEM_INTF_WR_DATA2

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Write Data [23:16]

FG_MEMIF_MEM_INTF_WR_DATA2

Bits	Name	Description
7:0	MEM_INTF_WR_DATA_2	Memory Interface Write Data

0x00004466 FG_MEMIF_MEM_INTF_WR_DATA3

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Write Data [31:24]

FG_MEMIF_MEM_INTF_WR_DATA3

Bits	Name	Description
7:0	MEM_INTF_WR_DATA_3	Memory Interface Write Data (for use with RAM only)

0x00004467 FG_MEMIF_MEM_INTF_RD_DATA0

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: N/A

Read Data [7:0] (for use with RAM only)

FG_MEMIF_MEM_INTF_RD_DATA0

Bits	Name	Description
7:0	MEM_INTF_RD_DATA_0	Memory Interface Read Data

0x00004468 FG_MEMIF_MEM_INTF_RD_DATA1

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: N/A

Read Data [15:8]

FG_MEMIF_MEM_INTF_RD_DATA1

Bits	Name	Description
7:0	MEM_INTF_RD_DATA_1	Memory Interface Read Data

0x00004469 FG_MEMIF_MEM_INTF_RD_DATA2

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: N/A

Read Data [23:16]

FG_MEMIF_MEM_INTF_RD_DATA2

Bits	Name	Description
7:0	MEM_INTF_RD_DATA_2	Memory Interface Read Data

0x0000446A FG_MEMIF_MEM_INTF_RD_DATA3

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: N/A

Read Data [31:24] (for use with RAM only)

FG_MEMIF_MEM_INTF_RD_DATA3

Bits	Name	Description
7:0	MEM_INTF_RD_DATA_3	Memory Interface Read Data (for use with RAM only)

33 TRIM_TRIM

0x0000FE00 TRIM_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

TRIM_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x0000FE01 TRIM_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

TRIM_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x0000FE02 TRIM_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

TRIM_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

0x0000FE03 TRIM_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

TRIM_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x0000FE04 TRIM_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x0C

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

TRIM_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	TRIM 0xC: TRIM

0x0000FE05 TRIM_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x01

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

TRIM_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	TRIM Core 0x1: TRIM

0x0000FE08 TRIM_TRIM_REG_INIT_STATUS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: N/A

TRIM Register Initialization Status Registers

TRIM_TRIM_REG_INIT_STATUS

Bits	Name	Description
4	TRIM_OTP_NOT_PROG	Indicates if OTP is not programmed. Set when an attempt to initialize the Trim registers is performed before the OTP has been programmed. 0x0: OTP_PROGRAMMED 0x1: OTP_NOT_PROGRAMMED
3	SW_TRIM_REG_INIT_EXEC	Indicates SW triggered TRIM Register Initialization has been executed. 0x0: TRIM_NOT_RUN 0x1: TRIM_COMPLETED

TRIM_TRIM_REG_INIT_STATUS (cont.)

Bits	Name	Description
2	SW_TRIM_REG_INIT_ON	Indicates SW triggered TRIM Register Initialization is ongoing. 0x0: TRIM_IDLE 0x1: TRIM_ACTIVE
1	HW_TRIM_REG_INIT_EXEC	Indicates HW triggered TRIM Register Initialization has been executed. 0x0: TRIM_NOT_RUN 0x1: TRIM_COMPLETED
0	HW_TRIM_REG_INIT_ON	Indicates HW triggered TRIM Register Initialization is ongoing. 0x0: TRIM_IDLE 0x1: TRIM_ACTIVE

0x0000FE09 TRIM_OTP_PROG_STATUS

Type: R
Clock: PBUS_WRCLK
Reset State: Undefined

Reset Name: N/A

OTP Programming Status Registers

TRIM_OTP_PROG_STATUS

Bits	Name	Description
2	TRIM_OTP_ALREADY_PRO G	Indicates if OTP is already programmed. Set when an attempt to program the OTP is performed after the OTP has already been programmed. 0x0: NO_ERROR 0x1: DOUBLE_PROGRAMMING_DETECTED
1	OTP_PROG_EXEC	Indicates if the requested OTP Programming operation has been executed. 0x0: PROGRAMMING_NOT_RUN 0x1: PROGRAMMING_COMPLETED
0	TRIM_OTP_PROG_ON	TRIM OTP Programming Ongoing 0x0: PROGRAMMING_IDLE 0x1: PROGRAMMING_ACTIVE

34 HAPTICS_HAPTICS

0x0001C000 HAPTICS_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: NA

HW Version Register [7:0]

PMIC_CONSTANT

HAPTICS_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x0001C001 HAPTICS_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: NA

HW Version Register [15:8]

PMIC_CONSTANT

HAPTICS_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x0001C002 HAPTICS_REVISION3

Type: R
Clock: PBUS_WRCLK
Reset State: 0x02

Reset Name: NA

HW Version Register [7:0]

HAPTICS_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x0001C003 HAPTICS_REVISION4

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: NA

HW Version Register [15:8]

HAPTICS_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

0x0001C004 HAPTICS_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x15

Reset Name: NA

Peripheral Type

PMIC_CONSTANT

HAPTICS_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	HAPTICS

0x0001C005 HAPTICS_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x09

Reset Name: NA

Peripheral SubType

PMIC_CONSTANT

HAPTICS_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	Haptics Driver

0x0001C00A HAPTICS_STATUS_1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Haptics real time status

HAPTICS_STATUS_1

Bits	Name	Description
7	EN_STS	Haptics enable status 0x1: ENABLED 0x0: DISABLED
4	AUTO_RES_ERROR	1 : Auto Resonance Period out of range

HAPTICS_STATUS_1 (cont.)

Bits	Name	Description
3	SC_FLAG	Short circuit flag 0: Haptics does not encounter short circuit condition. 1: Haptics encounters short circuit condition. a) All the four switches of h-bridge are driven high-Z when short circuit happens b) SW needs to write to SC_CLR reg to clear the SC flag before start playing a new waveform 0x0: NO_SC 0x1: SC_DET
2	OC_FLAG	reserved for future
1	BUSY	1: Haptics driver is busy playing a waveform. 0: Haptics driver is idle 0x0: IDLE 0x1: BUSY
0	PLAY_STS	reserved for future

0x0001C00B HAPTICS_LRA_AUTO_RES_LO

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Lower 8-bits of 12-bit auto resonance period of LRA

HAPTICS_LRA_AUTO_RES_LO

Bits	Name	Description
7:0	PERIOD	LRA resonant period setting resonant period=(96*code)/(19.2MHz) resonant frequency = (19.2MHz)/(96*code)

0x0001C00C HAPTICS_LRA_AUTO_RES_HI

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Higher 4 bits of 12-bit auto resonance period of LRA

HAPTICS_LRA_AUTO_RES_HI

Bits	Name	Description
7:4	PERIOD	Data

0x0001C010 HAPTICS_INT_RT_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Interrupt Real Time Status Bits

HAPTICS_INT_RT_STS

Bits	Name	Description
1	PLAY_INT_RT_STS	1: haptics driver has read the waveform register and loaded into shadow buffer for playing. S/W can write new waveform pattern 0 : 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
0	SC_INT_RT_STS	1: Haptics driver encounters short circuit condition 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH

0x0001C011 HAPTICS_INT_SET_TYPE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

0 = use level trigger interrupts, 1 = use edge trigger interrupts

HAPTICS_INT_SET_TYPE

Bits	Name	Description
1	PLAY_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE
0	SC_INT_SET_TYPE	0x0: LEVEL 0x1: EDGE

0x0001C012 HAPTICS_INT_POLARITY_HIGH

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

HAPTICS_INT_POLARITY_HIGH

Bits	Name	Description
1	PLAY_INT_POLARITY_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED
0	SC_INT_POLARITY_HIGH	0x0: HIGH_TRIGGER_DISABLED 0x1: HIGH_TRIGGER_ENABLED

0x0001C013 HAPTICS_INT_POLARITY_LOW

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

HAPTICS_INT_POLARITY_LOW

Bits	Name	Description
1	PLAY_INT_POLARITY_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED
0	SC_INT_POLARITY_LOW	0x0: LOW_TRIGGER_DISABLED 0x1: LOW_TRIGGER_ENABLED

0x0001C014 HAPTICS_INT_LATCHED_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

HAPTICS_INT_LATCHED_CLR

Bits	Name	Description
1	PLAY_INT_LATCHED_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED
0	SC_INT_LATCHED_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

0x0001C015 HAPTICS_INT_EN_SET

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC_SET_MASK

HAPTICS_INT_EN_SET

Bits	Name	Description
1	PLAY_INT_EN_SET	0x1: INT_ENABLED
0	SC_INT_EN_SET	0x1: INT_ENABLED

0x0001C016 HAPTICS_INT_EN_CLR

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC_CLR_MASK=INT_EN_SET

HAPTICS_INT_EN_CLR

Bits	Name	Description
1	PLAY_INT_EN_CLR	0x1: INT_DISABLED
0	SC_INT_EN_CLR	0x1: INT_DISABLED

0x0001C018 HAPTICS_INT_LATCHED_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

HAPTICS_INT_LATCHED_STS

Bits	Name	Description
1	PLAY_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
0	SC_INT_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

0x0001C019 HAPTICS_INT_PENDING_STS

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Debug: Pending is set if interrupt has been sent but not cleared.

HAPTICS_INT_PENDING_STS

Bits	Name	Description
1	PLAY_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
0	SC_INT_PENDING_STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

0x0001C01A HAPTICS_INT_MID_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Selects the MID that will receive the interrupt

HAPTICS_INT_MID_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0 0x1: MID1 0x2: MID2 0x3: MID3

0x0001C01B HAPTICS_INT_PRIORITY

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

SR=0 A=1

HAPTICS_INT_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR 0x1: A

0x0001C046 HAPTICS_EN_CTL1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Haptics Enable/Disable

HAPTICS_EN_CTL1

Bits	Name	Description
7	HAPTICS_EN	0: Haptics driver is disabled. SW should checks that no waveform is being played before disabling haptics driver. 1: Haptics driver is enabled. SW enables haptics driver before playing a waveform. 0x0: HAPTICS_DIS 0x1: HAPTICS_EN

0x0001C04C HAPTICS_CFG1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Haptics Actuator Type

HAPTICS_CFG1

Bits	Name	Description
0	ACTUATOR_TYPE	Type of actuator connected at the haptics driver output 0: LRA 1: ERM 0x0: LRA 0x1: ERM

0x0001C04E HAPTICS_SEL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Haptics waveform source

HAPTICS_SEL

Bits	Name	Description
5:4	WF_SOURCE	Source of haptics waveform input 00: Actuator is played directly with constant Vmax drive 01: Haptics waveform is read from buffer HAPTICS_WF_S0-S7 10: Haptics waveform is played from audio analog on LINE_IN/PWM 11: Haptics waveform is played from external PWM on LINE_IN/PWM 0x0: VMAX 0x1: BUFFER 0x2: AUDIO 0x3: EXT_PWM

HAPTICS_SEL (cont.)

Bits	Name	Description
0	TRIGGER	Enables mode to trigger the haptics waveform from external signal on LINE_IN/PWM when WF_SOURCE=VMAX or BUFFER. Set this bit to 0 if WF_SOURCE = EXT_PWM or AUDIO. 0: Waveform is played when register PLAY=1 1: Waveform is played when signal LINE_IN/PWM=1 0x0: HAPTICS_PLAY 0x1: LINE_IN

0x0001C051 HAPTICS_VMAX_CFG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x22

Reset Name: PERPH_rb

Maximum output driver voltage

HAPTICS_VMAX_CFG

Bits	Name	Description
5:0	VMAX	0-9: reserved 10-36: VMAX<5:1>*116mV

0x0001C054 HAPTICS_RATE_CFG1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x77

Reset Name: PERPH_rb

lower 8-bits of play rate period for each sample

HAPTICS_RATE_CFG1

Bits	Name	Description
7:0	RATE_7_0	play rate period=(96*code)/(19.2MHz)

0x0001C055 HAPTICS_RATE_CFG2

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x04

Reset Name: PERPH_rb

4 MSBs of play rate period for each sample

HAPTICS_RATE_CFG2

Bits	Name	Description
3:0	RATE_11_8	

0x0001C057 HAPTICS_EXTERNAL_PWM

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

External Line-in PWM frequency

HAPTICS_EXTERNAL_PWM

Bits	Name	Description
1:0	FREQ_SEL	0x0: EXT_PWM_25KHZ 0x1: EXT_PWM_50KHZ 0x2: EXT_PWM_75KHZ 0x3: EXT_PWM_100KHZ

0x0001C059 HAPTICS_SC_CLR

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

A pulse is generated when SW writes 1 to the register bit.

HAPTICS_SC_CLR

Bits	Name	Description
0	SC_CLR	Write 1 to the register bit clears short circuit flag. 0x0: SC_DIS 0x1: SC_CLR

0x0001C05C HAPTICS_BRAKE

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x1B

Reset Name: PERPH_rb

Auto braking pattern

HAPTICS_BRAKE

Bits	Name	Description
7:6	PATTERN4	00 : 0 01 : VMAX/4 10 : VAMX/2 11 : VMAX 0x0: ZERO 0x1: VMAX_DIV4 0x2: VMAX_DIV2 0x3: VMAX
5:4	PATTERN3	00 : 0 01 : VMAX/4 10 : VAMX/2 11 : VMAX 0x0: ZERO 0x1: VMAX_DIV4 0x2: VMAX_DIV2 0x3: VMAX
3:2	PATTERN2	00 : 0 01 : VMAX/4 10 : VAMX/2 11 : VMAX 0x0: ZERO 0x1: VMAX_DIV4 0x2: VMAX_DIV2 0x3: VMAX

HAPTICS_BRAKE (cont.)

Bits	Name	Description
1:0	PATTERN1	00 : 0 01 : VMAX/4 10 : VAMX/2 11 : VMAX 0x0: ZERO 0x1: VMAX_DIV4 0x2: VMAX_DIV2 0x3: VMAX

0x0001C05E HAPTICS_WF_REPEAT

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Repeating waveform

HAPTICS_WF_REPEAT

Bits	Name	Description
6:4	WF_REPEAT	Repeating 8-byte waveform buffer 0-7: repeat 2^N times 0x0: WF_REPEAT_1_TIMES 0x1: WF_REPEAT_2_TIMES 0x2: WF_REPEAT_4_TIMES 0x3: WF_REPEAT_8_TIMES 0x4: WF_REPEAT_16_TIMES 0x5: WF_REPEAT_32_TIMES 0x6: WF_REPEAT_64_TIMES 0x7: WF_REPEAT_128_TIMES
3:2	WF_REPEAT_RSVD	reserved for future
1:0	WF_S_REPEAT	Repeating sample byte 0-3: repeat 1, 2, 4 and 8 times 0x0: WF_S_REPEAT_1_TIMES 0x1: WF_S_REPEAT_2_TIMES 0x2: WF_S_REPEAT_4_TIMES 0x3: WF_S_REPEAT_8_TIMES

0x0001C060 HAPTICS_WF_S1

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

First byte of the waveform sample

HAPTICS_WF_S1

Bits	Name	Description
7	SIGN	drive direction 0: forward 1: reverse 0x0: FORWARD 0x1: REVERSE
6	OVD	overdrive 0: 1x drive 1: 2x drive 0x0: OVD_1X 0x1: OVD_2X
5:1	AMP	waveform amp AMP<5:1>*116mV

0x0001C061 HAPTICS_WF_S2

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Second byte of the waveform sample

HAPTICS_WF_S2

Bits	Name	Description
7	SIGN	drive direction 0: forward 1: reverse 0x0: FORWARD 0x1: REVERSE

HAPTICS_WF_S2 (cont.)

Bits	Name	Description
6	OVD	overdrive 0: 1x drive 1: 2x drive 0x0: OVD_1X 0x1: OVD_2X
5:1	AMP	waveform amp AMP<5:1>*116mV

0x0001C062 HAPTICS_WF_S3

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Third byte of the waveform sample

HAPTICS_WF_S3

Bits	Name	Description
7	SIGN	drive direction 0: forward 1: reverse 0x0: FORWARD 0x1: REVERSE
6	OVD	overdrive 0: 1x drive 1: 2x drive 0x0: OVD_1X 0x1: OVD_2X
5:1	AMP	waveform amp AMP<5:1>*116mV

0x0001C063 HAPTICS_WF_S4

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Fourth byte of the waveform sample

HAPTICS_WF_S4

Bits	Name	Description
7	SIGN	drive direction 0: forward 1: reverse 0x0: FORWARD 0x1: REVERSE
6	OVD	overdrive 0: 1x drive 1: 2x drive 0x0: OVD_1X 0x1: OVD_2X
5:1	AMP	waveform amp AMP<5:1>*116mV

0x0001C064 HAPTICS_WF_S5

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Fifth byte of the waveform sample

HAPTICS_WF_S5

Bits	Name	Description
7	SIGN	drive direction 0: forward 1: reverse 0x0: FORWARD 0x1: REVERSE
6	OVD	overdrive 0: 1x drive 1: 2x drive 0x0: OVD_1X 0x1: OVD_2X
5:1	AMP	waveform amp AMP<5:1>*116mV

0x0001C065 HAPTICS_WF_S6

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Sixth byte of the waveform sample

HAPTICS_WF_S6

Bits	Name	Description
7	SIGN	drive direction 0: forward 1: reverse 0x0: FORWARD 0x1: REVERSE
6	OVD	overdrive 0: 1x drive 1: 2x drive 0x0: OVD_1X 0x1: OVD_2X
5:1	AMP	waveform amp AMP<5:1>*116mV

0x0001C066 HAPTICS_WF_S7

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Seventh byte of the waveform sample

HAPTICS_WF_S7

Bits	Name	Description
7	SIGN	drive direction 0: forward 1: reverse 0x0: FORWARD 0x1: REVERSE

HAPTICS_WF_S7 (cont.)

Bits	Name	Description
6	OVD	overdrive 0: 1x drive 1: 2x drive 0x0: OVD_1X 0x1: OVD_2X
5:1	AMP	waveform amp AMP<5:1>*116mV

0x0001C067 HAPTICS_WF_S8

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Eighth byte of the waveform sample

HAPTICS_WF_S8

Bits	Name	Description
7	SIGN	drive direction 0: forward 1: reverse 0x0: FORWARD 0x1: REVERSE
6	OVD	overdrive 0: 1x drive 1: 2x drive 0x0: OVD_1X 0x1: OVD_2X
5:1	AMP	waveform amp AMP<5:1>*116mV

0x0001C070 HAPTICS_PLAY

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_rb

Play or Pause the haptics when WF_SOURCE=BUFFER or VMAX. Not valid for WF_SOURCE=AUDIO and EXT_PWM

HAPTICS_PLAY

Bits	Name	Description
7	PLAY	0: Stop haptics waveform 1: Play haptics waveform 0x0: STOP 0x1: PLAY
0	PAUSE	Pause playing 0x0: CONTINUE 0x1: PAUSE

35 PWM_PWM_SLICE

0x0001B000 PWM_REVISION1

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC_CONSTANT

PWM_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

0x0001B001 PWM_REVISION2

Type: R
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC_CONSTANT

PWM_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

0x0001B004 PWM_PERPH_TYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x13

Reset Name: N/A

Peripheral Type

PMIC_CONSTANT

PWM_PERPH_TYPE

Bits	Name	Description
7:0	TYPE	LPG

0x0001B005 PWM_PERPH_SUBTYPE

Type: R
Clock: PBUS_WRCLK
Reset State: 0x0B

Reset Name: N/A

Peripheral SubType

PMIC_CONSTANT

PWM_PERPH_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	PWM Channel

0x0001B041 PWM_PWM_SIZE_CLK

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x04

Reset Name: PERPH_RB

This register sets the PWM frequency according to the foll. formula

PWM_FREQ = PWM_FREQ_CLK_SELECT/(2^(PWM_SIZE))*(2^(PWM_FREQ_EXPONENT)*PWM_FREQ_PRE_DIVIDE)

PWM_PWM_SIZE_CLK

Bits	Name	Description
2	PWM_SIZE	0 = 6-bit PWM 1 = 9-bit PWM 0x0: PWM_6BIT 0x1: PWM_9BIT
1:0	PWM_FREQ_CLK_SELECT	sets the PWM master clock 00 = no clock 01 = 1 kHz 10 = 32 kHz 11 = 19.2 MHz 0x0: NOCLK 0x1: CLK_1KHZ 0x2: CLK_32KHZ 0x3: CLK_19P2MHZ

0x0001B042 PWM_PWM_FREQ_PREDIV_CLK

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

This register selects the pre-divide and exponent values to divide down the PWM master clock

PWM_PWM_FREQ_PREDIV_CLK

Bits	Name	Description
6:5	PWM_FREQ_PRE_DIVIDE	00 = 1 01 = 3 10 = 5 11 = 6 0x0: PREDIV_ONE 0x1: PREDIV_THREE 0x2: PREDIV_FIVE 0x3: PREDIV_SIX

PWM_PWM_FREQ_PREDIV_CLK (cont.)

Bits	Name	Description
2:0	PWM_FREQ_EXPONENT	000 = 0 001 = 1 .. 111 = 7 0x0: EXP_ZERO 0x1: EXP_ONE 0x2: EXP_TWO 0x3: EXP_THREE 0x4: EXP_FOUR 0x5: EXP_FIVE 0x6: EXP_SIX 0x7: EXP_SEVEN

0x0001B043 PWM_PWM_TYPE_CONFIG

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

PWM_PWM_TYPE_CONFIG

Bits	Name	Description
5	EN_GLITCH_REMOVAL	0 = no glitch removal, PWM outputs are updated immediately 1 = glitch removal, PWM outputs are updated only on PWM period boundaries 0x0: GLITCH_REMOVE_DIS 0x1: GLITCH_REMOVE_EN

0x0001B044 PWM_PWM_VALUE_LSB

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

PWM_VALUE_LSB

PWM_PWM_VALUE_LSB

Bits	Name	Description
7:0	PWM_VALUE_LSB	lower 8 bits of PWM

0x0001B045 PWM_PWM_VALUE_MSB

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

PWM_VALUE_MSB

PWM_PWM_VALUE_MSB

Bits	Name	Description
0	PWM_VALUE_MSB	MSB (bit 9) of PWM

0x0001B046 PWM_ENABLE_CONTROL

Type: RW
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

Enables PWM output

PWM_ENABLE_CONTROL

Bits	Name	Description
7	EN_MODULE	0 = Module disabled (High Z) 1 = Module enabled 0x0: PWM_DISABLE 0x1: PWM_ENABLE

0x0001B047 PWM_PWM_SYNC

Type: W
Clock: PBUS_WRCLK
Reset State: 0x00

Reset Name: PERPH_RB

PWM_PWM_SYNC

Bits	Name	Description
0	SYNC_PWM	Writing 1 to this register will update the 6/9-bit PWM value. This bit is auto-cleared

Index of registers