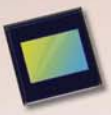

datasheet

PRODUCT SPECIFICATION

1/4" color CMOS 8 megapixel (3264 x 2448)
PureCel® image sensor

OV8856

color CMOS 8 megapixel (3264 x 2448) PureCel® image sensor

datasheet (COB)
PRODUCT SPECIFICATION

version 2.01
january 2017

To learn more about OmniVision Technologies, visit www.ovt.com.

applications

- cellular phones
- PC multimedia
- tablets

ordering information

- **OV08856-GA4A** (color, chip probing, 200 µm backgrinding, reconstructed wafer with good die)

features

- 1.12 µm x 1.12 µm pixel
- optical size of 1/4"
- 32.9° CRA for < 5mm Z-height
- programmable controls for frame rate, mirror and flip, cropping, and windowing
- supports images sizes: 8MP (4:3, 3264x2448), 8MP (16:9, 3264x1836), EIS 1080p (2112x1188), 1080p (1920x1080), EIS 720p (1408x792), and more
- 8MP at 30 fps (720Mbps/4-lane or 1.44Gbps/2-lane)
- two on-chip phase lock loops (PLLs)
- two-wire serial bus control (SCCB)
- 8k bits of embedded one-time programmable (OTP) memory
- image quality control: defect pixel correction, automatic black level calibration, lens shading correction and alternate row HDR
- suitable for module size of 8.5mm x 8.5mm x ~4mm

note The OV8856 supports LVDS interface. Contact your local FAE for details.

key specifications (typical)

- **active array size:** 3264 x 2448
- **power supply:**
  - analog: 2.6 ~ 3.0V (2.8V nominal)
  - core: 1.14 ~ 1.26V (1.2V nominal)
  - I/O: 1.7 ~ 1.9V (1.8V)
- **power requirements:**
  - active: 150 mW
  - standby: 0.8 µW
  - XSHUTDN: 1 µW
- **temperature range:**
  - operating: -30°C to +85°C junction temperature (see **table 7-2**)
  - stable image: 0°C to +60°C junction temperature (see **table 7-2**)
- **output interfaces:** up to 4-lane MIPI serial output
- **output formats:** 10-bit RGB RAW
- **lens chief ray angle:** 32.9° non-linear (see **figure 9-2**)
- **lens size:** 1/4"
- **input clock frequency:** 6~27 MHz
- **max S/N ratio:** 36.5 dB
- **dynamic range:** 70 dB @ 8x gain
- **maximum image transfer rate:**
  - 3264x2448: 30 fps (see **table 2-1**)
  - 3264x1836: 30 fps (see **table 2-1**)
  - 2112x1188: 60 fps (see **table 2-1**)
  - 1920x1080: 60 fps (see **table 2-1**)
  - 1408x792: 90 fps (see **table 2-1**)
- **sensitivity:** 480 mV/Lux-sec
- **scan mode:** progressive
- **pixel size:** 1.12 µm x 1.12 µm
- **dark current:** 12e^-/sec @ 60°C junction temperature
- **image area:** 3678.336 µm x 2767.68 µm
- **die dimensions:** 4806 µm x 3969 µm (COB), 4856 µm x 4019 µm (RW) (see **section 8** for details)

note higher junction temperature degrades image quality

note COB refers to whole wafers with known good die and RW refers to singulated good die on a reconstructed wafer. Die size differs between COB and RW.

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pad numbers for the OV8856 image sensor. The die information is shown in **section 8**.

table 1-1 signal descriptions (sheet 1 of 2)

pad number	signal name	pad type	description
01	DOGND	ground	I/O ground
02	DVDD	power	digital circuit power
03	AGND	ground	analog ground
04	AVDD	power	analog power
05	**SID**	input	SCCB last bit ID input 0: SCCB ID address = 0x6C 1: SCCB ID address = 0x20
06	**SCL**	input	SCCB interface input clock
07	**SDA**	I/O	SCCB interface data pin
08	**FSIN/VSYNC**	I/O	frame sync / video output vertical signal
09	DOVDD	power	I/O power
10	**XSHUTDN**	input	reset and power down (active low with pull down resistor)
11	**TM**	input	test mode (active high with pull down resistor)
12	DVDD	power	digital circuit power
13	DOGND	ground	I/O ground
14	AVDD	power	analog power
15	AGND	ground	analog ground
16	AGND	ground	analog ground
17	AVDD	power	analog power
18	VH	power	internal voltage reference
19	VN	power	internal voltage reference
20	DOGND	ground	I/O ground
21	**MDP2**	output	MIPI data positive output
22	**MDN2**	output	MIPI data negative output
23	**MDP0**	output	MIPI data positive output
24	**MDN0**	output	MIPI data negative output

table 1-1 signal descriptions (sheet 2 of 2)

pad number	signal name	pad type	description
25	EGND	ground	ground for MIPI circuit
26	PVDD	power	PLL analog power
27	EVDD	power	power for MIPI circuit
28	**MCP**	output	MIPI clock positive output
29	**MCN**	output	MIPI clock negative output
30	EGND	ground	ground for MIPI circuit
31	**MDP1**	output	MIPI data positive output
32	**MDN1**	output	MIPI data negative output
33	EVDD	power	power for MIPI circuit
34	**MDP3**	output	MIPI data positive output
35	**MDN3**	output	MIPI data negative output
36	DOVDD	power	I/O power
37	**XVCLK**	input	system clock input
38	DVDD	power	digital circuit power
39	DOGND	ground	I/O ground

table 1-2 configuration under various conditions (sheet 1 of 2)

pad	signal name	RESET[a]	after RESET release[b]	software standby[c]
05	SID	input	input	input
06	SCL	high-z	input	input
07	SDA	open drain	I/O	I/O
08	VSYNC	high-z	high-z	high-z by default (configurable)
08	FSIN	high-z	input	input (configurable)
10	XSHUTDN	input	input	input
11	TM	input	input	input
21	MDP2	high-z	high	high by default (configurable)
22	MDN2	high-z	high	high by default (configurable)
23	MDP0	high-z	high	high by default (configurable)
24	MDN0	high-z	high	high by default (configurable)

table 1-2 configuration under various conditions (sheet 2 of 2)

pad	signal name	RESET[a]	after RESET release[b]	software standby[c]
28	MCP	high-z	high	high by default (configurable)
29	MCN	high-z	high	high by default (configurable)
31	MDP1	high-z	high	high by default (configurable)
32	MDN1	high-z	high	high by default (configurable)
34	MDP3	high-z	high	high by default (configurable)
35	MDN3	high-z	high	high by default (configurable)
37	XVCLK	high-z	input	input

a. XSHUTDN = 0

b. XSHUTDN from 0 to 1

c. sensor set to sleep from streaming mode

figure 1-1 pad diagram

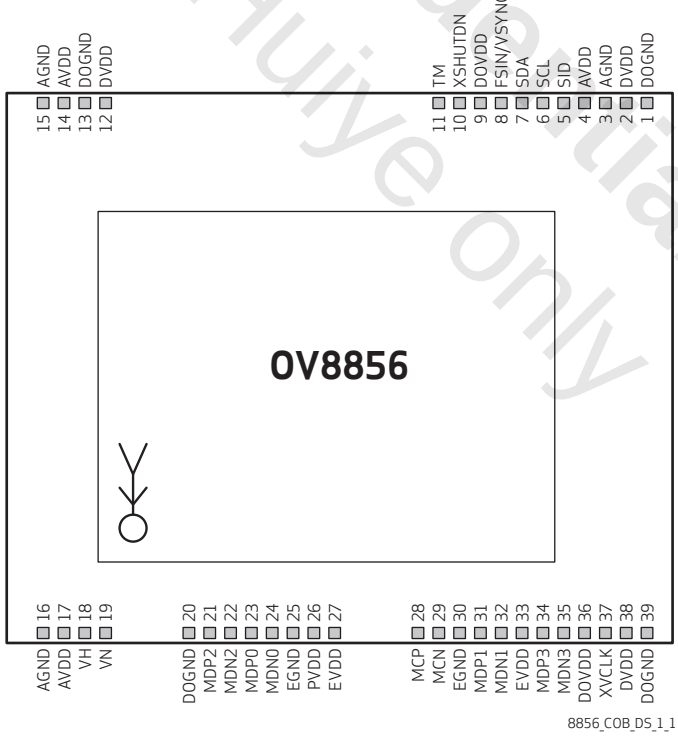
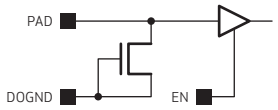
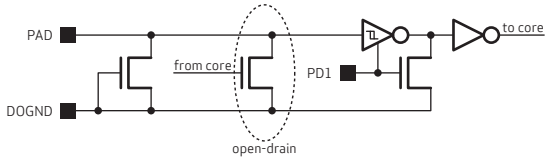
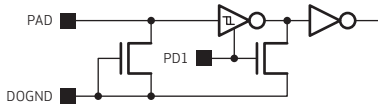
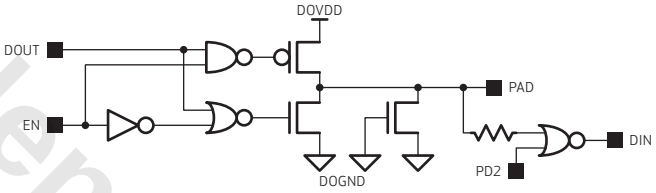
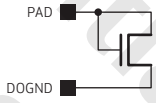
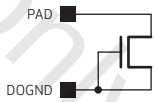
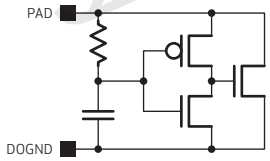
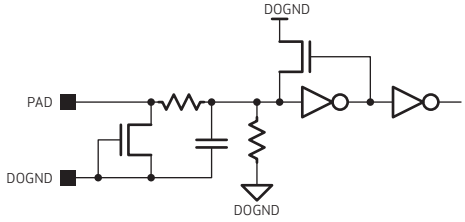


table 1-3 pad symbol and equivalent circuit

symbol	equivalent circuit
XVCLK, SID	
SDA	
SCL	
FSIN/VSYNC	
VN	
MDP3, MDP2, MDP1, MDP0, MDN3, VH, MDN2, MDN1, MDN0, MCP, MCN, EGND, AGND, DOGND	
AVDD, EVDD, DVDD, DOVDD, PVDD	
XSHUTDN, TM	

2 system level description

2.1 overview

The OV8856 RAW RGB PureCel® image sensor is a high performance, 1/4-inch 8 megapixel CMOS image sensor that delivers 3264x2448 at 30 fps. It provides full-frame, sub-sampled, and windowed 10-bit MIPI images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV8856 has an 8 megapixel image array capable of operating at up to 30 frames per second (fps) in 10-bit resolution with complete user control over image quality, formatting and output data transfer. Some image processing functions, such as defective pixel canceling, lens correction (LENC), etc., are programmable through the SCCB interface.

In addition, OmniVision image sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

For customized information purposes, the OV8856 includes 8k bits of one-time programmable (OTP) memory. The OV8856 has a MIPI interface of up to four lanes.

2.1.1 identifying the sensor's revision ID

For the OV8856, the sensor's revision ID can be read out from the first byte in Bank 0 of one-time program (OTP) memory. To read out data from OTP, perform the following steps:

```
6c 0100 01

6c 3d84 00

6c 3d81 01
```

Then, verify that register 0x7000 = 0x00, 0x7001 = 0x88, and 0x7002 = 0x56.

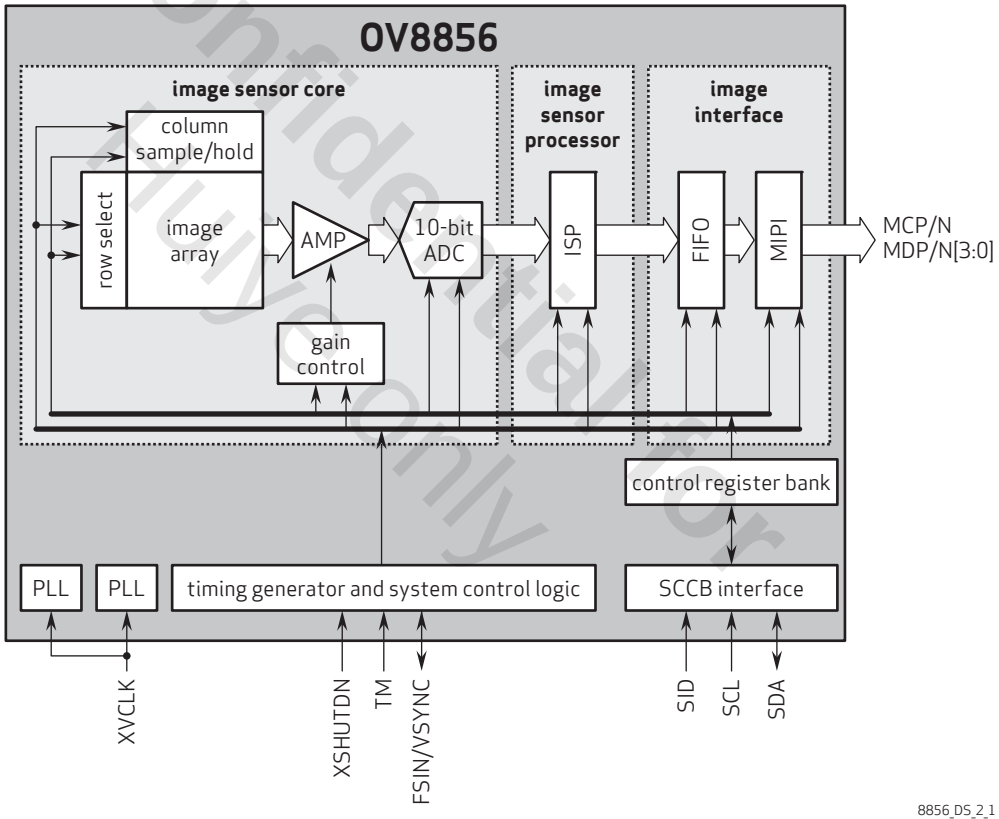
2.2 architecture

The OV8856 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OV8856 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, pre-charging and sampling the rows of the array sequentially. In the time between pre-charging and sampling a row, the charge in the pixels decreases with exposure to incident light. This is the exposure time in rolling shutter architecture.

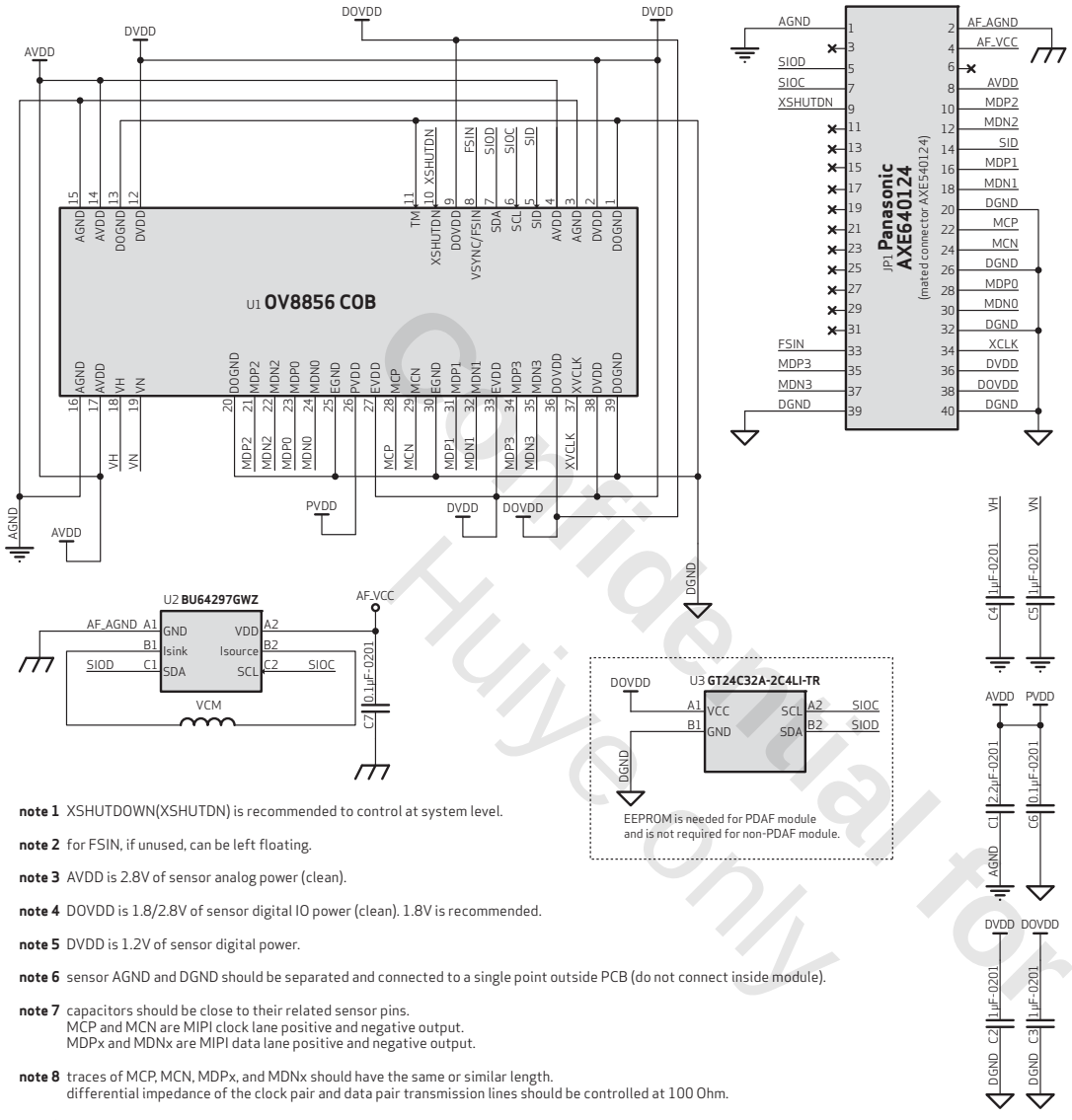
The exposure time is controlled by adjusting the time interval between pre-charging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs up to 10-bit data for each pixel in the array.

figure 2-1 OV8856 block diagram



8856_DS_2_1

figure 2-2 OV8856 reference schematic



note 1 XSHUTDOWN(XSHUTDN) is recommended to control at system level.

note 2 for FSIN, if unused, can be left floating.

note 3 AVDD is 2.8V of sensor analog power (clean).

note 4 DOVDD is 1.8/2.8V of sensor digital IO power (clean). 1.8V is recommended.

note 5 DVDD is 1.2V of sensor digital power.

note 6 sensor AGND and DGND should be separated and connected to a single point outside PCB (do not connect inside module).

note 7 capacitors should be close to their related sensor pins.
MCP and MCN are MIPI clock lane positive and negative output.
MDPx and MDNx are MIPI data lane positive and negative output.

note 8 traces of MCP, MCN, MDPx, and MDNx should have the same or similar length.
differential impedance of the clock pair and data pair transmission lines should be controlled at 100 Ohm.

note 9 SID pin should be pulled low for device address 0x6C and pulled high for device address 0x20.

note 10 AF_VCC and AF_AGND is the power supply for auto focus related circuitry.
although AF_VCC is 2.8-3.3V, it is recommeneded to use 3.3V for better auto focus performance.

note 11 EEPROM slave ID is 0xA4 for write and 0xA5 for read based on current configuration

8856_COB_DS_2_2

2.3 format and frame

The OV8856 supports RAW RGB output with one/two/four lane MIPI interface.

table 2-1 format and frame rate

format	resolution	max frame rate	methodology	10-bit output MIPI data rate
8 MP	3264 x 2448	30 fps	full resolution (4:3)	4-lane @ 720 Mbps/lane 2-lane @ 1.272 Gbps/lane
6 MP HD	3264 x1836	30 fps	full resolution (16:9)	4-lane @ 720 Mbps/lane 2-lane @ 1.272 Gbps/lane
EIS 1080p	2112 x 1188	60 fps	cropping	4-lane @ 720 Mbps/lane 2-lane @ 1.272 Gbps/lane
1080p	1920 x 1080	60 fps	cropping	4-lane @ 720 Mbps/lane 2-lane @ 1.272 Gbps/lane
EIS 720p	1408 x 792	90 fps	cropping + 2x binning	4-lane @ 360 Mbps/lane 2-lane @ 720 Mbps/lane
720p	1280 x 720	90 fps	cropping + 2x binning	4-lane @ 360 Mbps/lane 2-lane @ 720 Mbps/lane
VGA	640 x 480	120 fps	cropping + 4x binning	4-lane @ 180 Mbps/lane 2-lane @ 360 Mbps/lane

2.4 I/O control

The OV8856 can configure its I/O pads as an input or output. For the output signal, it follows one of two paths: either from the data path or from register control.

table 2-2 I/O control registers

function	register	description
output drive capability control	0x3011	Bit[6:5]: I/O pad drive capability 00: 1x 01: 2x 10: 3x 11: 4x
VSYNC I/O control	0x3000	Bit[5]: VSYNC output enable 0: input 1: output
VSYNC output select	0x300E	Bit[5]: enable VSYNC as GPIO controlled by register
VSYNC output value	0x3003	Bit[3]: register control VSYNC output

2.5 MIPI interface

The OV8856 supports a MIPI interface of up to 4-lanes. The MIPI interface can be configured for 1, 2, or 4 lanes and each lane is capable of a data transfer rate of up to 720 Mbps for 4-lane MIPI or 1.44 Gbps for 2-lane MIPI.

2.6 power management

Based on the system power configuration (XSHUTDN), the power up sequence will be different. OmniVision recommends cutting off all power supplies, including the external DVDD, when the sensor is not in use.

2.6.1 power up sequence

To avoid any glitch from a strong external noise source, OmniVision recommends controlling XSHUTDN.

Whether or not XSHUTDN is controlled by GPIO, the XSHUTDN rising cannot occur before AVDD and DOVDD.

table 2-3 power up sequence

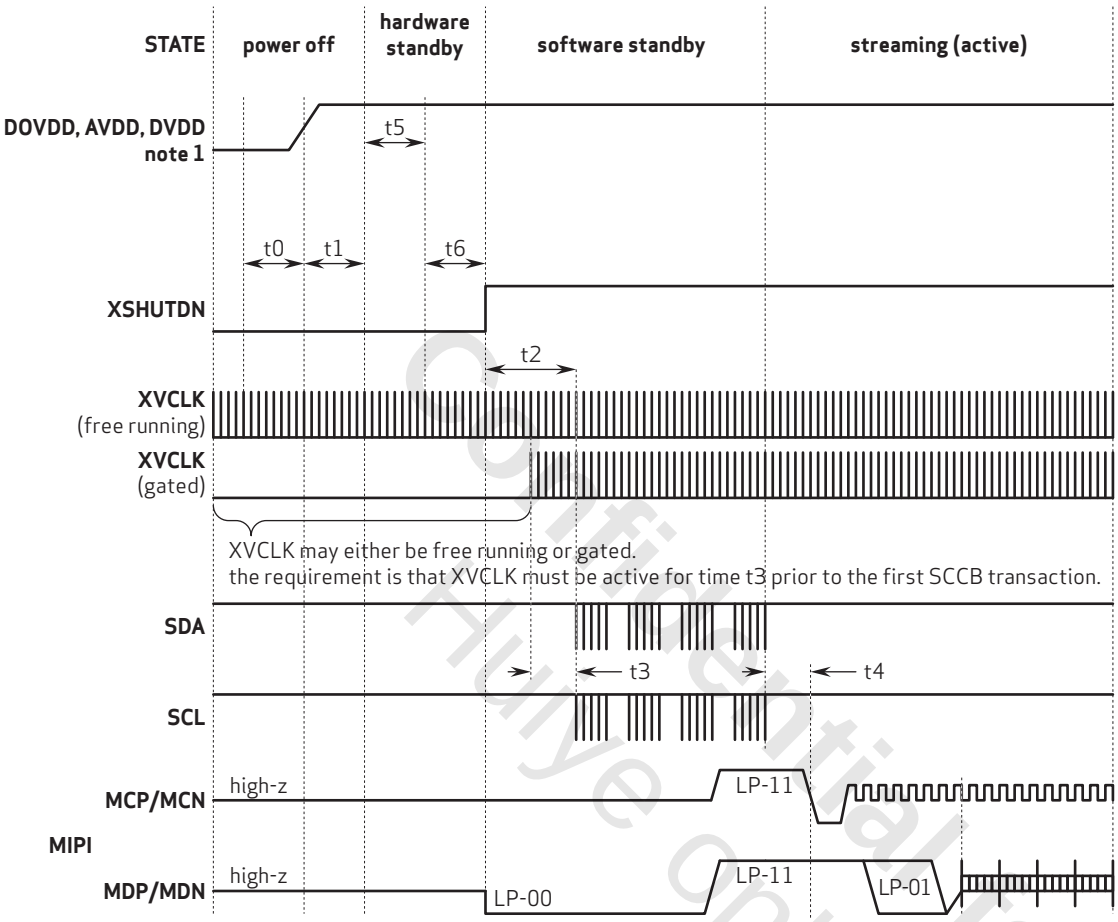
XSHUTDN	power up sequence requirement
GPIO	Refer to **figure 2-3** 1. DOVDD, AVDD, and DVDD can rise in any order 2. XSHUTDN rising must occur after AVDD, DOVDD and DVDD are stable

table 2-4 power up sequence timing constraints

constraint	label	min	max	unit
AVDD rising – DOVDD rising	t0[a]	0	∞	ns
DOVDD rising – AVDD rising	t1[a]			ns
XSHUTDN rising – first SCCB transaction	t2	8192		XVCLK cycles
minimum number of XVCLK cycles prior to the first SCCB transaction	t3	8192		XVCLK cycles
PLL lock period	t4	0.2		ms
AVDD or DOVDD, whichever is last – DVDD	t5[a]	0	∞	ns
DVDD – XSHUTDN rising	t6	0	∞	ns

a. only for OV8856, t0, t1, and t5 may rise in any order before XSHUTDN is pulled high

figure 2-3 power up sequence



note 1 DOVDD, AVDD and DVDD may rise in any order

8855_8856_DS_2.3

2.6.2 power down sequence

The digital and analog supply voltages can be powered down in any order (e.g., DOVDD, then AVDD or AVDD, then DOVDD). Similar to the power up sequence, the XVCLK input clock may be either gated or continuous. To avoid bad frames from the MIPI, OmniVision recommends to using group hold to send SCCB sleep command.

table 2-5 power down sequence

XSHUTDN	power down sequence requirement
GPIO	Refer to **figure 2-5** 1. software standby recommended 2. pull XSHUTDN low for minimum power consumption 3. cut off DVDD, pull AVDD, and DOVDD low in any order

table 2-6 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for the MIPI end code before entering the software for standby; otherwise, enter the software standby mode immediately		
minimum of XVCLK cycles after the last SCCB transaction or MIPI frame end	t1	512		XVCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDN falling	t2	512		XVCLK cycles
XSHUTDN falling – AVDD falling or DVDD or DOVDD falling whichever is first	t3[a]	0.0		ns

a. only for OV8856, DVDD, DOVDD, and AVDD may fall in any order after XSHUTDN is pulled low

figure 2-4 software standby sequence

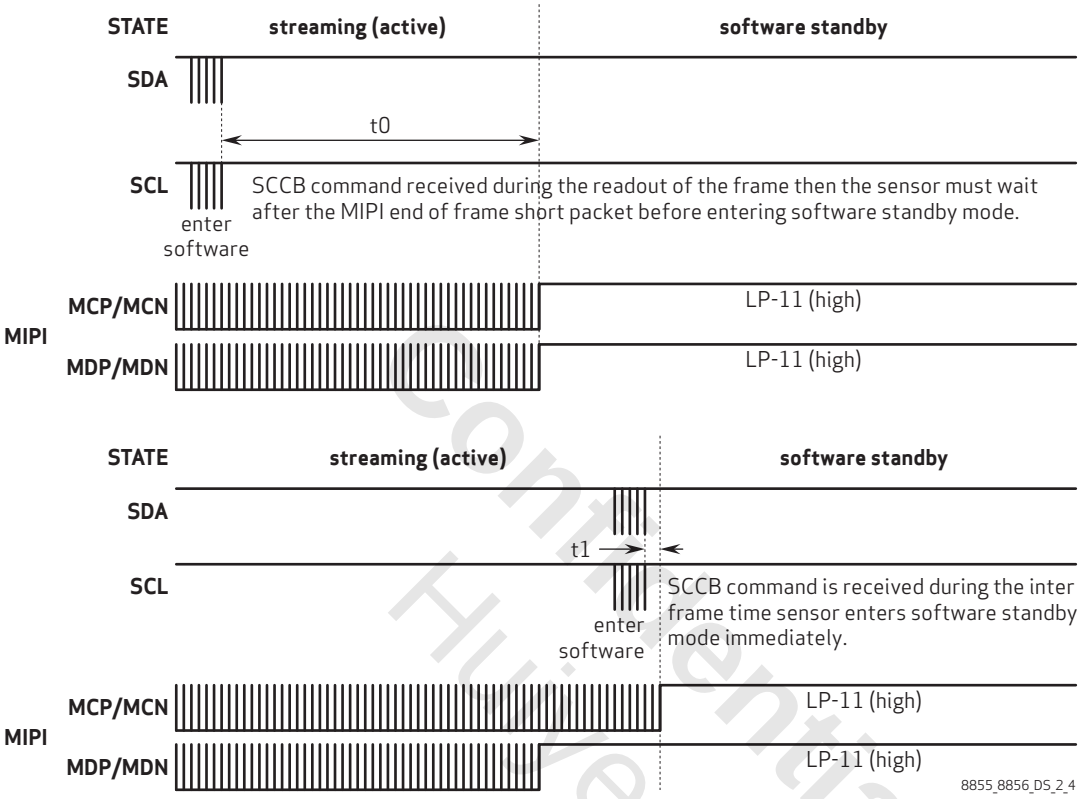
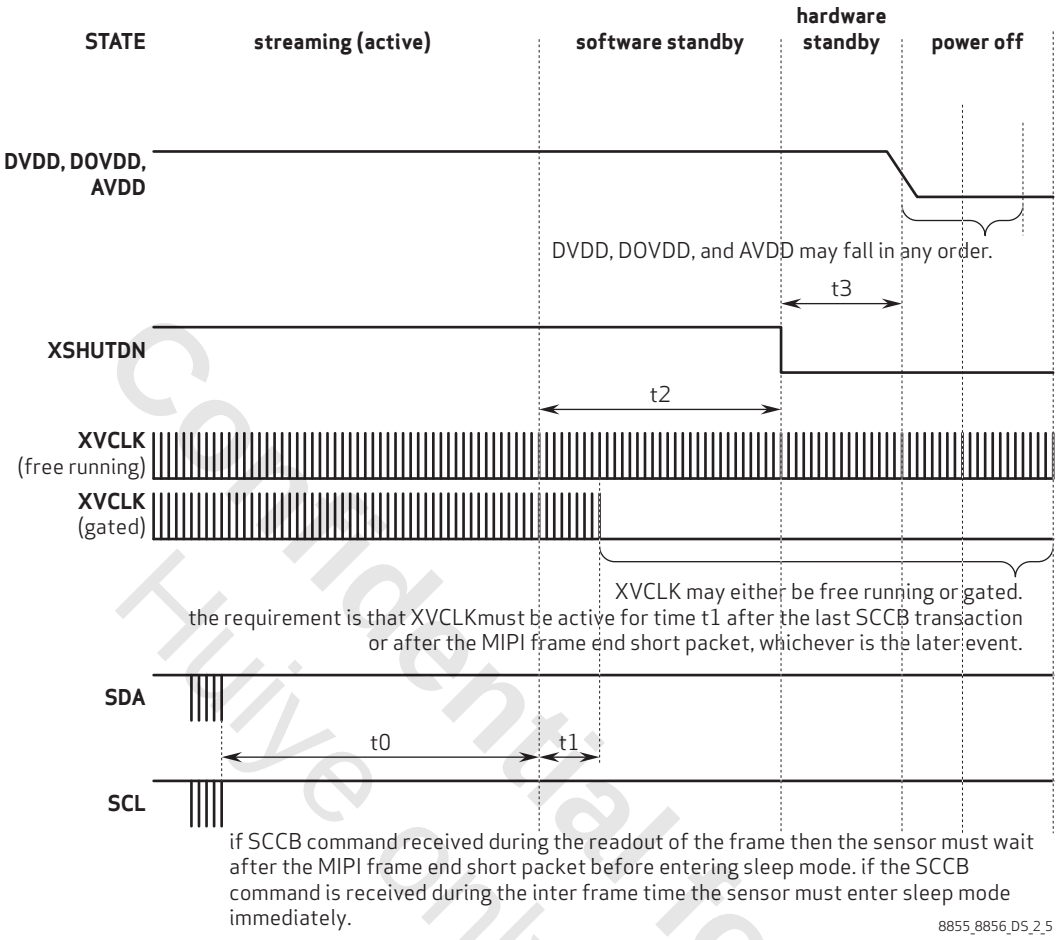


figure 2-5 power down sequence



2.7 reset

The whole chip will be reset during power up. Manually applying a hardware reset (XSHUTDN=0) upon power up is recommended even though the on-chip power up reset is included. The hardware reset is active low with an asynchronized design. The reset pulse width should be greater than or equal to 2 ms.

2.7.1 power ON reset

The power on reset can be controlled from an external pin. Additionally, in this sensor, a power on reset is generated after the core power becomes stable.

2.7.2 software reset

When register 0x0103[0] is configured as 1, all registers are reset to their default values.

2.8 hardware and software standby

Two suspend modes are available for the OV8856:

- hardware standby
- software standby

2.8.1 hardware standby

To initiate hardware standby mode, the XSHUTDN must be tied to low. When this occurs, the OV8856 internal device clock is halted even when the external clock source is still clocking and all internal counters are reset.

2.8.2 software standby

Executing a software power down (0x0100[0]) through the SCCB interface suspends internal circuit activity, but does not halt the device clock. All register content is maintained in standby mode. During the resume state, all the registers are restored to their original values.

table 2-7 hardware and standby description

mode	description
hardware standby with XSHUTDN	1. enabled by pulling XSHUTDN low 2. power down all blocks 3. register values are reset to default values 4. no SCCB communication 5. minimum power consumption
software standby	1. default mode after power on reset 2. power down all blocks except SCCB 3. register values are maintained 4. SCCB communication is available 5. low power consumption 6. GPIO can be configured as high/low/tri-state

2.9 system clock control

PLL settings can only be changed during sensor standby mode (0x0100 = 0).

2.9.1 PLL1

The PLL1 generates a default 90 MHz pixel clock and 720 MHz MIPI serial clock from a 6~27 MHz input clock. The VCO range is from 500 MHz to 960 MHz. A programmable clock is provided to generate different frequencies.

2.9.2 PLL2

The PLL2 generates a default 144 MHz system clock from a 6~27 MHz input clock. The VCO range is from 500 MHz to 960 MHz. A programmable clock divider is provided to generate different frequencies.

figure 2-6 clock scheme

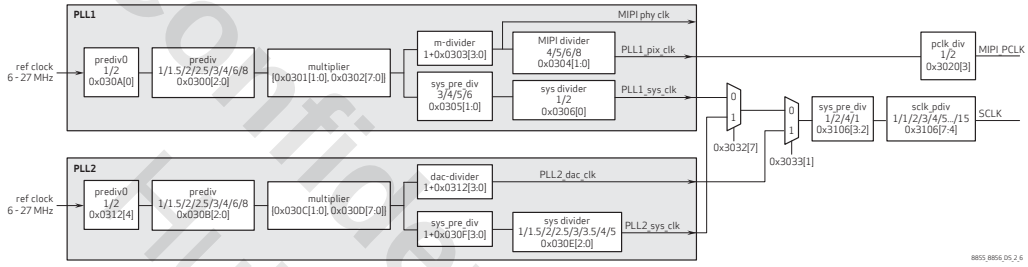


table 2-8 PLL registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x0300	PLL_CTRL_0	0x00	RW	Bit[2:0]: pll1_pre_div
0x0301	PLL_CTRL_1	0x00	RW	Bit[1:0]: pll1_multiplier[9:8]
0x0302	PLL_CTRL_2	0x19	RW	Bit[7:0]: pll1_multiplier[7:0]
0x0303	PLL_CTRL_3	0x00	RW	Bit[3:0]: pll1_divm
0x0304	PLL_CTRL_4	0x03	RW	Bit[1:0]: pll1_div_mipi
0x0305	PLL_CTRL_5	0x01	RW	Bit[1:0]: pll1_div_sp
0x0306	PLL_CTRL_6	0x01	RW	Bit[0]: pll1_div_s
0x0308	PLL_CTRL_8	0x00	RW	Bit[0]: pll1_bypass
0x0309	PLL_CTRL_9	0x01	RW	Bit[2:0]: pll1_cp
0x030A	PLL_CTRL_A	0x00	RW	Bit[0]: pll1_predivp
0x030B	PLL_CTRL_B	0x00	RW	Bit[2:0]: pll2_pre_div
0x030C	PLL_CTRL_C	0x00	RW	Bit[1:0]: pll2_r_divp[9:8]

table 2-8 PLL registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x030D	PLL_CTRL_D	0x1E	RW	Bit[7:0]: pll2_r_divp[7:0]
0x030E	PLL_CTRL_E	0x02	RW	Bit[2:0]: pll2_r_divs
0x030F	PLL_CTRL_F	0x02	RW	Bit[3:0]: pll2_r_divsp
0x0310	PLL_CTRL_10	0x01	RW	Bit[2:0]: pll2_r_cp
0x0311	PLL_CTRL_11	0x00	RW	Bit[0]: pll2_bypass
0x0312	PLL_CTRL_12	0x01	RW	Bit[4]: pll2_pre_div0 Bit[3:0]: pll2_r_divdac

table 2-9 sample PLL configuration

control name	address	input clock (XVCLK)	
		24 MHz	6 MHz
PLL1_PREDIVP	0x030A[0]	0x0	0x0
PLL1_PREDIV	0x0300[2:0]	0x0	0x0
PLL1_MULTIPLIER	{0x0301[1:0], 0x0302[7:0]}	0x1E	0x64
PLL1_DIV_MIPI	0x0304[1:0]	0x3	0x3
PLL1_DIVM	0x0303[3:0]	0x0	0x0
PLL1_DIVSP	0x0305[1:0]	0x1	0x1
PLL1_DIVS	0x0306[0]	0x1	0x1
PLL2_PREDIVP	0x3012[0]	0x0	0x0
PLL2_PREDIV	0x030B[2:0]	0x0	0x0
PLL2_MULTIPLIER	{0x030C[1:0], 0x030D[7:0]}	0x1E	0x78
PLL2_DIVSP	0x030F[3:0]	0x4	0x2
PLL2_DIVS	0x030E[2:0]	0x0	0x2
SCLK	–	144MHz	120MHz
PHY_SCLK	–	720MHz	600MHz
MIPI_PCLK	–	90MHz	75MHz

2.10 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

In the OV8856, the SCCB ID is controlled by the SID pin. If SID is low, the sensor's SCCB ID is 0x6C for write (0x6D for read). If SID is high, the sensor's SCCB ID is 0x20 for write (0x21 for read). The SCCB ID can also be programmed by registers. When 0x303F[0] is 1, the ID comes from register 0x3004 when SID=0 and register 0x3012 when SID=1.

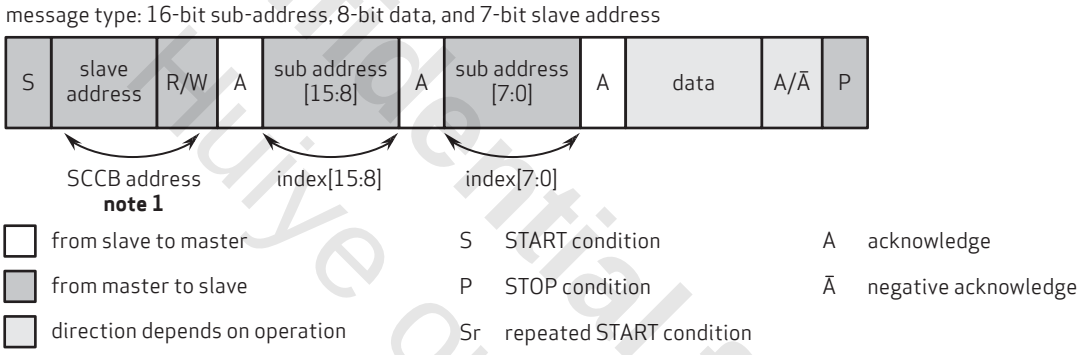
2.10.1 data transfer protocol

The data transfer of the OV8856 follows the SCCB protocol.

2.10.2 message format

The OV8856 supports the message format shown in **figure 2-7**. The repeated START (Sr) condition is not shown in **figure 2-8**, but is shown in **figure 2-9** and **figure 2-10**.

figure 2-7 message type



note 1 slave address must be 0x36 for SCCB write address to be 0x6C and for SCCB read address to be 0x6D

8855_8856_DS_2_7

2.10.3 read / write operation

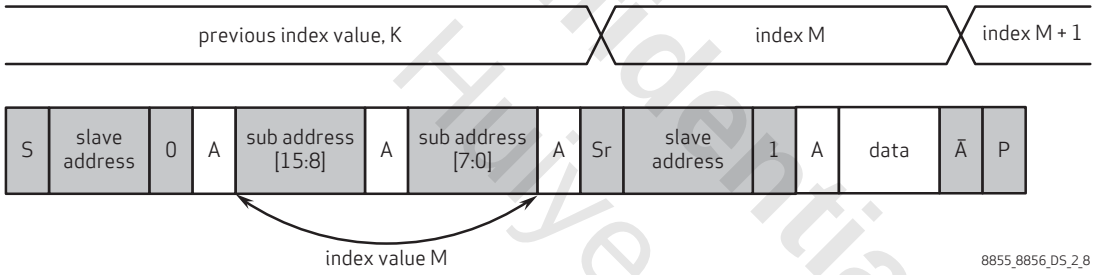
The OV8856 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

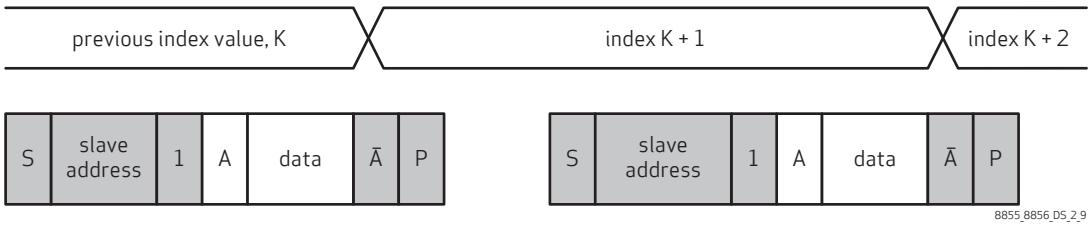
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 2-8**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-8 SCCB single read from random location



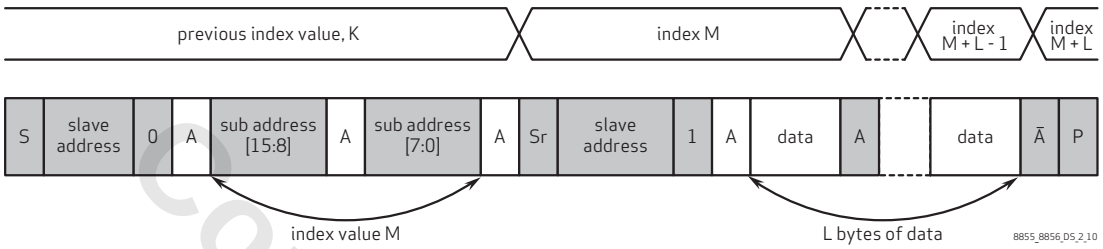
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 2-9**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-9 SCCB single read from current location



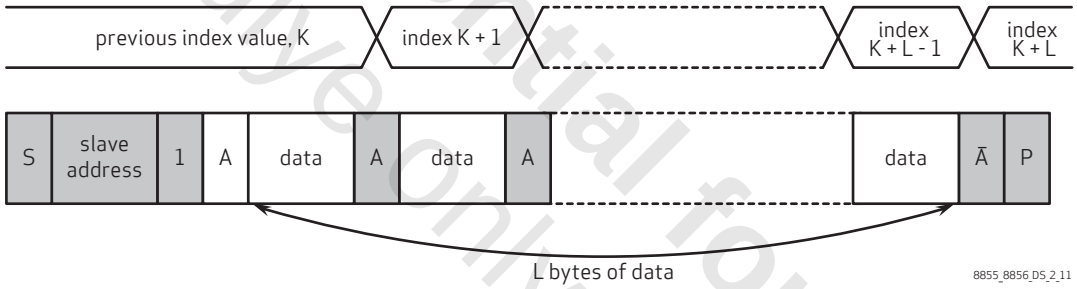
The sequential read from a random location is illustrated in **figure 2-10**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 2-10 SCCB sequential read from random location



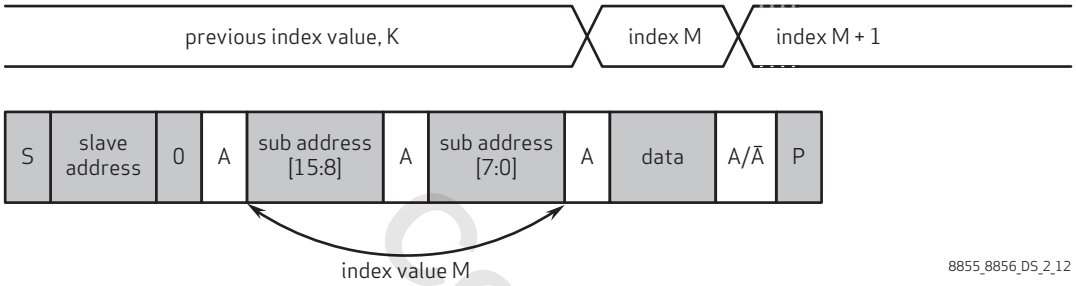
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation, as shown in **figure 2-11**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-11 SCCB sequential read from current location



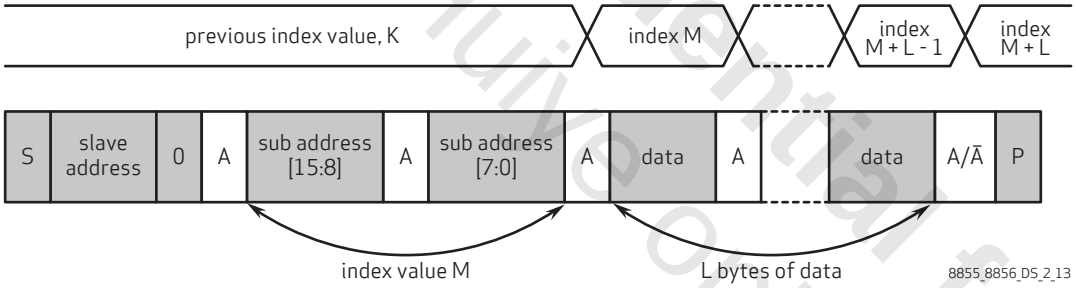
The write operation to a random location is illustrated in **figure 2-12**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 2-12 SCCB single write to random location



The sequential write is illustrated in **figure 2-13**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 2-13 SCCB sequential write to random location



2.10.4 SCCB timing

figure 2-14 SCCB interface timing

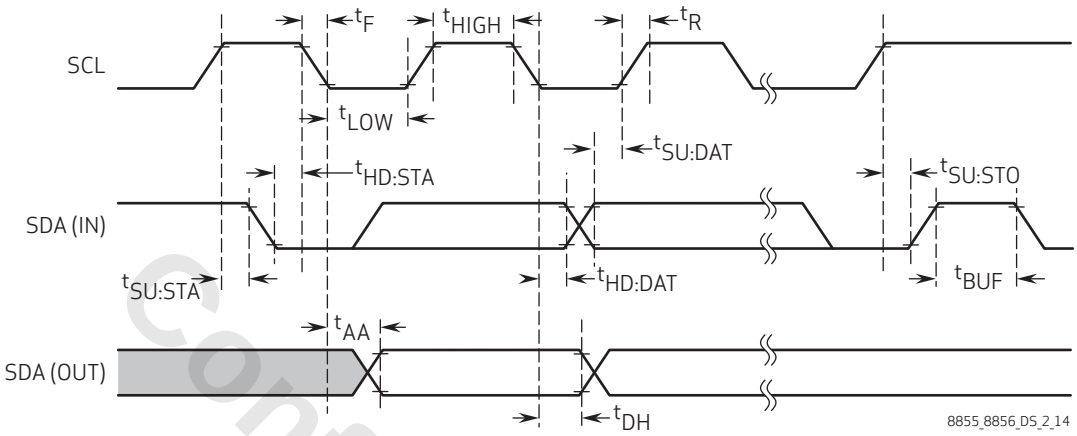


table 2-10 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency			400	kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SCL low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400kHz mode

b. timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 30%, timing measurement shown in the middle of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 70%

2.11 group write

Group write is supported in order to update a group of registers (except 0x31xx) in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary. If more than one group is going to be launched, the second group cannot be recorded or launched before the first group has effectively been launched.

The OV8856 supports up to four groups. These groups share 1024 bytes of memory and the size of each group is programmable by adjusting the start address.

table 2-11 context switching control

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Group Access Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group delay launch 1110: Group quick launch Others: Reserved Bit[3:0]: Group ID 0000: Group bank 0, default start from address 0x00 0001: Group bank 1, default start from address 0x40 0010: Group bank 2, default start from address 0x80 0011: Group bank 3, default start from address 0xB0 Others: Reserved
0x3209	GRP0_PERIOD	0x00	RW	Frames For Staying in First Group (must be Group 0) 0 Means Always Stay in Group 0
0x320A	GRP1_PERIOD	0x00	RW	Frames For Staying in Second Group (can be Group 1-3) 0 Means Always Stay in Group 1
0x320B	GRP_SWCTRL	0x01	RW	Bit[7]: Auto switch Bit[3]: group_switch_repeat_en Enable the first group (group 0) and second group repeatable switch Bit[2]: context_en Enable to switch from second group back to first group (group 0) automatically Bit[1:0]: Second group selection
0x320D	GRP_ACT	–	R	Indicates Which Group is Active
0x320E	FRAME_CNT_GRP0	–	R	frame_cnt_grp0
0x320F	FRAME_CNT_GRP1	–	R	frame_cnt_grp1

2.11.1 hold

After the groups are configured, users can perform a hold operation to store register settings into the SRAM of each group. The hold of each group starts and ends with the control register 0x3208. The lower 4 bits of register 0x3208 control which group to access, and the upper 4 bits control the start (0x0: hold start) and end (0x1: hold end) of the hold operation.

The example setting below shows the sequence to hold group 0:

```
6C  3208  00    group 0 hold start
6C  3800  11    first register into group 0
6C  3911  22    second register into group 0
6C  3208  10    group 0 hold end
```

2.11.2 launch

After the contents of each group are defined in the hold operation, all registers belonging to each group are stored in SRAM, and ready to be written into target registers (i.e., the launch of that group).

There are five launch modes as described in sections **section 2.11.2.1** to **section 2.11.2.5**.

2.11.2.1 launch mode 1 - quick manual launch

Manual launch is enabled by setting the register 0x320B to 0.

Quick manual launch is achieved by writing to control register 0x3208. The value written into this register is 0xEX, the upper 4 bits (0xE) are the quick launch command and the lower 4 bits (0xX) are the group number. For example, if users want to launch group 0, they just write the value 0xE0 to 0x3208, then the contents of group 0 will be written to the target registers immediately after the sensor gets this command through the SCCB. Below is a setting example.

```
6C  320B  00    manual launch on
6C  3208  E0    quick launch group 0
```

2.11.2.2 launch mode 2 - delay manual launch

Delay manual launch is achieved by writing to the register 0x3208. The value written into this register is 0xAX, where the upper 4 bits (0xA) are the delay launch command and the lower 4 bits (0xX) are the group number. For example, if users want to launch group 1, they just write the value 0xA1 to 0x3208, then the contents of group 1 will be written to the target registers. The difference with mode 1 is that the writing will wait for some internally defined time spot in vertical blanking, thus delayed. Below is a setting example.

```
6C  320B  00    manual launch on
6C  3208  A1    delay launch group 1
```

2.11.2.3 launch mode 3 - quick auto launch

Quick auto launch works like the mode 1, the difference is it will return to a specified group automatically. This is controlled by the register 0x3209, where bit[6:5] controls which group to return and bit[4:0] controls how many frames to stay before returning. The auto launch enable bit is the 0x320B[7].

The operation can be better understood with a setting example:

```
6C  3209  44    Bit[6:5]: 2, return to group 2, Bit[4:0]: 4: stay 4 frames
6C  320B  80    auto launch on
6C  3208  E0    quick launch group 0
```

In this example, sensor will quick launch group 0, stay at group 0 for 4 frames, then return to group 2 after that.

2.11.2.4 launch mode 4: delay auto launch

Delay auto launch works like mode 2 in the delay launch part and like the mode 3 in the return part.

The operation can be better understood with a setting example:

```
6C  3209  44    Bit[6:5]: 2, return to group 2, Bit[4:0]: 4: stay 4 frames
6C  320B  80    auto launch on
6C  3208  A0    delay launch group 0
```

In this example, sensor will delay launch group 0, stay at group 0 for 4 frames, then return to group 2 after that.

2.11.2.5 launch mode 5: repeat launch

Repeat launch is controlled by registers 0x3209, 0x320A, and 0x320B. In this mode, the launch is repeated automatically between the first group (must be group 0) and the second group (can be either one of groups 1-3, which is specified by register 0x320B[1:0]). The register 0x3209 defines how many frames remain at group 0, and register 0x320A defines how many frames remain at the second group.

The operation can be better understood with a setting example:

```
6C  3209  02    Bit[7:0]: 2, stay 2 frames in group 0
6C  320A  03    Bit[7]: 3, stay 3 frames in the second group
6C  320B  0E    Bit[3:2]: 3, repeat launch on, Bit[1:0]: 2, second group select:
                group 2
6C  3208  A0    always use a0 for repeat launch
```

In this example, sensor will delay launch group 0, stay at group 0 for 2 frames, then switch to group 2 for 3 frames, then back to group 0 for 2 frames, group 2 for 3 frames and so on.

Below is another example to apply launch mode 2 (delay manual launch) first, sensor stays at group 2 for an indefinite number of frames, then apply launch mode 5 (repeat launch). The sensor will switch to group 0 for 2 frames, then group 2 for 3 frames, and so on.

```
6C  320B  00    manual launch on
6C  3208  A2    delay launch group 2 stay at group 2 for indefinite frames
6C  3209  02    Bit[7:0]: 2, stay 2 frames in group 0
6C  320A  03    Bit[7:0]: 3, stay 3 frames in the second group
6C  320B  0E    Bit[3:2]: 3, repeat launch on, Bit[1:0]: 2, second group select:
                group 2
6C  3208  A0    always use A0 for repeat launch
```

Switch to group 0 for 2 frames, then group 2 for 3 frames, and so on.

2.12 register re-mapping

The OV8856 supports register re-mapping function to re-map a source address to a continuous destination one. One use is to make some discontinuous address to a consecutive address, so the user can use sequential write through SCCB to access these registers. This will speed up the SCCB access. The OV8856 supports up to 32 registers which can be re-mapped to a continuous address.

```
6C  3101  32 ; Bit[5] enable re-mapping function
6C  3108  90 ; Destination start address
6C  3109  00
6C  3110  35 ; source address0
6C  3111  00 ;
6C  3112  35 ; source address1
6C  3113  01 ;
6C  3114  35 ; source address2
6C  3115  02 ;
6C  3116  35 ; source address3
6C  3117  08 ;
6C  3118  35 ; source address4
6C  3119  09 ;
```

Then, if the user wants to write 0x3500~0x3503 and 0x3508-0x3509:

```
6C  9000  AA; will write 0x3500 to 0xAA
6C  9001  BB; will write 0x3501 to 0xBB
6C  9002  CC; will write 0x3502 to 0xCC
6C  9003  DD; will write 0x3508 to 0xDD
6C  9004  EE; will write 0x3509 to 0xEE
```

table 2-12 register re-mapping

address	register name	default value	R/W	description
0x314E	SRC ADDR1F H	0x00	RW	High Byte of Number 1F Source Register Address
0x314F	SRC ADDR1F L	0x00	RW	Low Byte of Number 1F Source Register Address

3 block level description

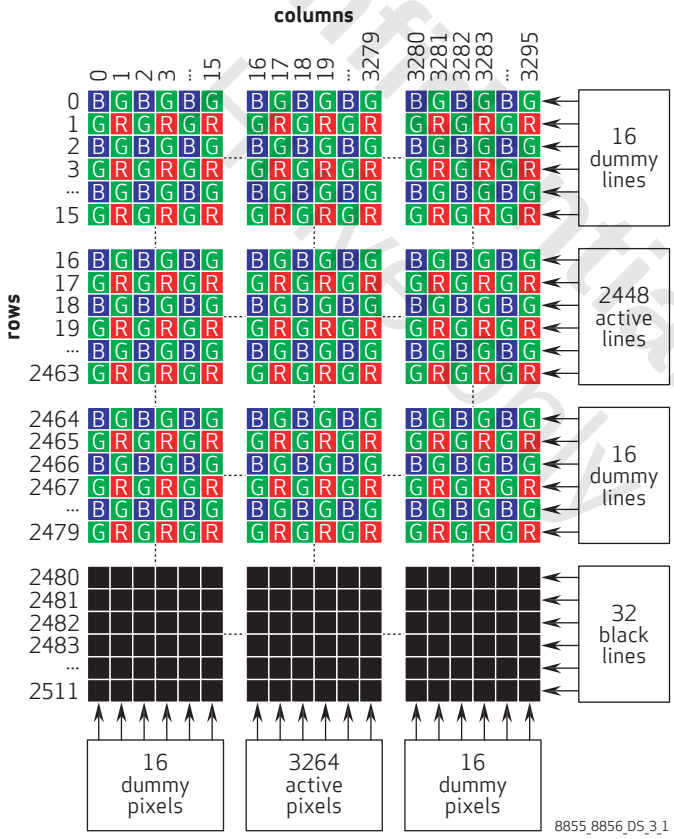
3.1 pixel array structure

The OV8856 sensor has an image array of 3296 columns by 2512 rows (8,279,552 pixels including 32 black lines). figure 3-1 shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 8,279,552 pixels, 7,990,272 (3264x2448) are active pixels and can be output. The other pixels are used for black level calibration and interpolation. The center 3264x2448 pixels is suggested to be output from the whole active pixel array. The backend processor can use the boundary pixels for additional processing.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

figure 3-1 sensor array region color filter layout



3.2 subsampling

The OV8856 supports a binning mode to provide a lower resolution output while maintaining the field of view. With binning mode ON, the voltage levels of adjacent pixels (of the same color) are averaged before being sent to the ADC. The OV8856 supports 2x2 binning, which is illustrated in **figure 3-2**, where the voltage levels of two horizontal (2x1) adjacent same-color pixels are averaged.

figure 3-2 example of 2x2 binning

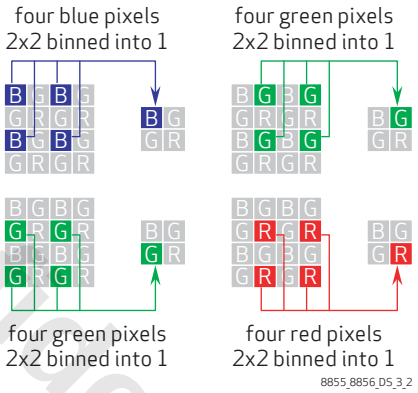


table 3-1 binning-related registers

address	register name	default value	R/W	description
0x3821	TIMING_FORMAT2	0x08	RW	Bit[7]: Vertical sum Bit[5]: Vertical binning Bit[4]: Horizontal binning Bit[3]: ISP horizontal VAR2
0x3814	X_ODD_INC	0x01	RW	Bit[3:0]: Horizontal increase number at odd pixel
0x3815	X_EVEN_INC	0x01	RW	Bit[3:0]: Horizontal increase number at even pixel
0x382A	Y_ODD_INC	0x01	RW	Bit[3:0]: Vertical increase number at odd row
0x382B	Y_EVEN_INC	0x01	RW	Bit[3:0]: Vertical increase number at even row

3.3 alternate row HDR

In HDR mode, the exposure is still controlled by a rolling shutter. However, the frame data is separated into "long exposure" and "short exposure" in every two rows, as shown in **figure 3-3**. Long exposure time is controlled by registers 0x3500, 0x3501, and 0x3502. Short exposure time is controlled by registers 0x3510, 0x3511, and 0x3512. The sequence of MIPI output in HDR mode is similar to normal mode. The output timing of long and short exposure lines is shown in **figure 3-4**

figure 3-3 alternate row HDR

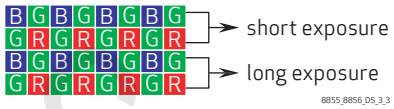


figure 3-4 HDR output timing

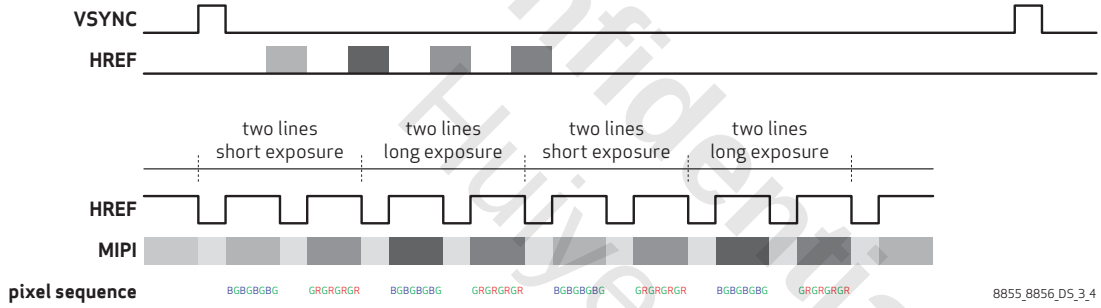


table 3-2 HDR control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3820	TIMING_FORMAT	0x80	RW	Bit[0]: hdr_en HDR enable 0: Disable 1: Enable
0x3500	MEC LONG EXPO	0x00	RW	Long Exposure Bit[3:0]: Long exposure[19:16]
0x3501	MEC LONG EXPO	0x02	RW	Long Exposure Bit[7:0]: Long exposure[15:8]
0x3502	MEC LONG EXPO	0x00	RW	Long Exposure Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits

table 3-2 HDR control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3503	AEC MANUAL	0x00	RW	Bit[6]: Digital fraction gain delay option 0: Delay 1 frame 1: Do not delay 1 frame Bit[5]: Gain change delay option 0: Delay 1 frame 1: Do not delay 1 frame Bit[4]: Gain delay option 0: Delay 1 frame 1: Do not delay 1 frame Bit[3]: Not used Bit[2]: Gain manual as sensor gain 0: Input gain as real gain format 1: Input gain as sensor gain format Bit[1]: Exposure delay option (must be 0) 0: Delay 1 frame 1: Not used Bit[0]: Exposure change delay option (must be 0) 0: Delay 1 frame 1: Not used
0x3508	LONG GAIN	0x00	RW	Bit[4:0]: Long_gain[12:8]
0x3509	LONG GAIN	0x80	RW	Bit[7:0]: Gain[7:0] If 0x3503[2]=0, then Gain[12:0] is real gain format, where low 7 bits are fraction bits, real_gain = Gain[12:0]/128 For example, 0x080 is 1x gain, 0x100 is 2x gain. If 0x3503[2]=1, then Gain[12:0] is sensor gain format, where: Gain[12:8]: Coarse gain 00000: 1x 00001: 2x 00011: 4x 00111: 8x Gain[7]: 1'b1 Gain[6:3]: Fine gain Gain[2:0]: Always 0 For example, 0x080 is 1x gain, 0x180 is 2x gain, and 0x380 is 4x gain.
0x350C	SHORT GAIN	0x00	RW	Bit[4:0]: Short gain[12:8]
0x350D	SHORT GAIN	0x80	RW	Bit[7:0]: Short gain[7:0] Use group function to change 0x366A[6:4] with the same rule as long gain
0x3510	MEC SHORT EXPO	0x00	RW	Short Exposure Bit[3:0]: Short exposure[19:16]

table 3-2 HDR control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3511	MEC SHORT EXPO	0x02	RW	Short Exposure Bit[7:0]: Short exposure[15:8]
0x3512	MEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits

3.4 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

3.5 10-bit A/D converters

The balanced signal is then digitized by the on-chip 10-bit ADC.

4 image sensor core digital functions

4.1 mirror and flip

The OV8856 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

table 4-1 mirror and flip registers

address	register name	default value	R/W	description
0x3820	FORMAT1	0x00	RW	Timing Control Register Bit[2]: Digital vertical flip enable 0: Normal 1: Vertical flip Bit[1]: Array vertical flip enable 0: Normal 1: Vertical flip
0x3821	FORMAT2	0x00	RW	Timing Control Register Bit[2]: Digital horizontal mirror control 0: Mirrored image 1: Normal image Bit[1]: Array horizontal mirror control 0: Mirrored image 1: Normal image

4.2 image windowing

An image windowing area is defined by four parameters, horizontal start (HS), horizontal end (HE), vertical start (VS), and vertical end (VE). By properly setting the parameters, any portion within the sensor array size can output as a visible area. Windowing is achieved by masking off the pixels outside of the window; thus, the original timing is not affected.

Horizontal crop start {0x3800, 0x3801} and crop end (0x3804, 0x3805 + 1) shall be a multiple of 16. Change VFIFO {0x4600, 0x4601} start size to be h_output_size/8-1 or less, where h_output_size is {0x3808, 0x3809} values. This is needed if ouptut h_output_size is reduced from the default output size.

figure 4-2 image windowing

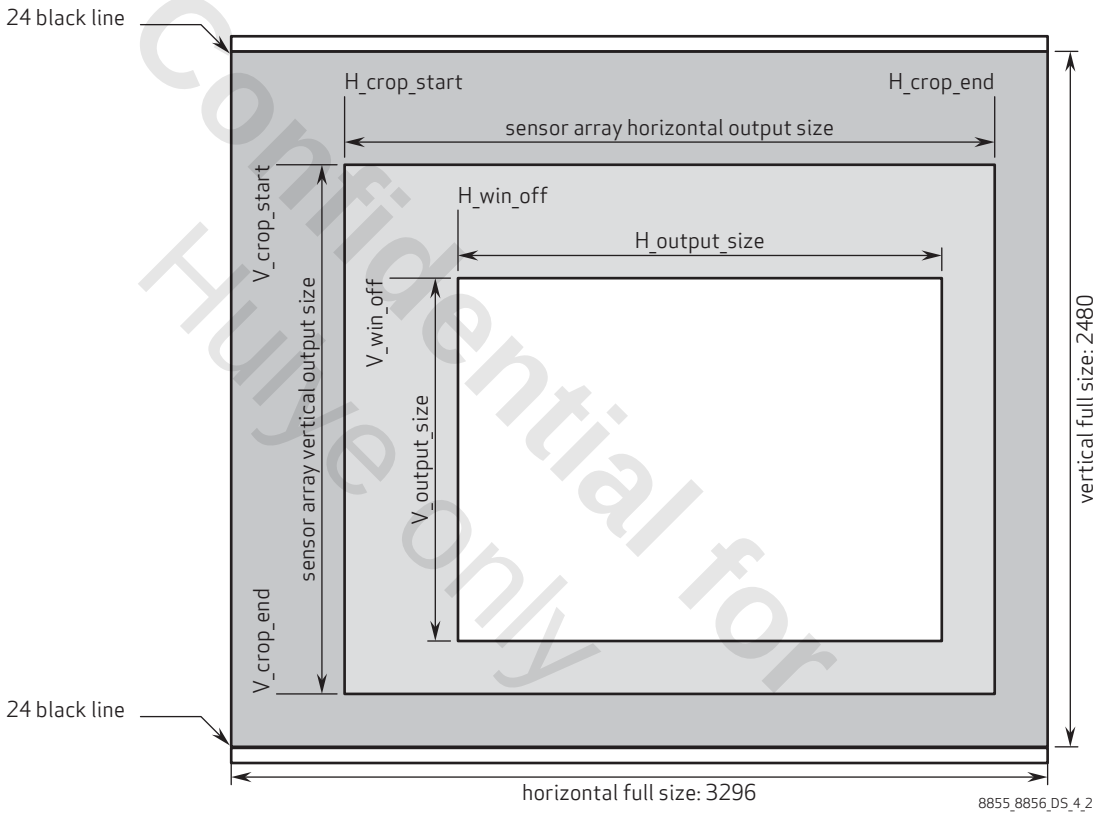


table 4-2 image windowing control functions

address	register name	default value	R/W	description
0x3800	H_CROP_START	0x00	RW	Bit[3:0]: Manual horizontal crop start address[11:8]
0x3801	H_CROP_START	0x00	RW	Bit[7:0]: Manual horizontal crop start address[7:0]
0x3802	V_CROP_START	0x00	RW	Bit[3:0]: Manual vertical crop start address[11:8]
0x3803	V_CROP_START	0x0C	RW	Bit[7:0]: Manual vertical crop start address[7:0]
0x3804	H_CROP_END	0x0C	RW	Bit[3:0]: Manual horizontal crop end address[11:8]
0x3805	H_CROP_END	0xDF	RW	Bit[7:0]: Manual horizontal crop end address[7:0]
0x3806	V_CROP_END	0x09	RW	Bit[3:0]: Manual vertical crop end address[11:8]
0x3807	V_CROP_END	0xA3	RW	Bit[7:0]: Manual vertical crop end address[7:0]
0x3808	H_OURPUT_SIZE	0x0C	RW	Bit[3:0]: Horizontal output size[11:8]
0x3809	H_OUTPUT_SIZE	0xC0	RW	Bit[7:0]: Horizontal output size[7:0]
0x380A	V_OUTPUT_SIZE	0x09	RW	Bit[3:0]: Vertical output size[11:8]
0x380B	V_OUTPUT_SIZE	0x90	RW	Bit[7:0]: Vertical output size[7:0]
0x380C	TIMING_HTS	0x07	RW	Bit[7:0]: Horizontal total size[15:8]
0x380D	TIMING_HTS	0x90	RW	Bit[7:0]: Horizontal total size[7:0]
0x380E	TIMING_VTS	0x09	RW	Bit[7:0]: Vertical total size[15:8]
0x380F	TIMING_VTS	0xB0	RW	Bit[7:0]: Vertical total size[7:0]
0x3810	H_WIN_OFF	0x00	RW	Bit[3:0]: Manual horizontal windowing offset[11:8]
0x3811	H_WIN_OFF	0x04	RW	Bit[7:0]: Manual horizontal windowing offset[7:0]
0x3812	V_WIN_OFF	0x00	RW	Bit[3:0]: Manual vertical windowing offset[11:8]
0x3813	V_WIN_OFF	0x02	RW	Bit[7:0]: Manual vertical windowing offset[7:0]
0x3814	H_INC_ODD	0x01	RW	Bit[3:0]: Horizontal sub-sample odd increase number
0x3815	H_INC_EVEN	0x01	RW	Bit[3:0]: Horizontal sub-sample even increase number
0x382A	V_INC_ODD	0x01	RW	Bit[3:0]: Vertical sub-sample odd increase number
0x382B	V_INC_EVEN	0x01	RW	Bit[3:0]: Vertical sub-sample even increase number

4.3 test pattern

For testing purposes, the OV8856 offers three types of test patterns: color bar, square and random data. The OV8856 also offers two digital effects: transparent effect and rolling bar effect. The output type of digital test pattern is controlled by the test_pattern_type register (0x5E00[3:2]). The digital test pattern function is controlled by register 0x5E00[7].

4.3.1 color bar

There are four types of color bars which are switched by bar-style in register 0x5E00[3:2] (see **figure 4-3**).

figure 4-3 color bar types

8855_8856_DS_4_3

4.3.2 square

There are two types of squares: color square and black-white square. The squ_bw register (0x5E00[4]) decides which type of square will be output.

figure 4-4 color, black and white square bars

8855_8856_DS_4_4

4.3.3 random data

There are two types of random data test patterns: frame-changing and frame-fixed random data.

4.3.4 transparent effect

The transparent effect is enabled by transparent_en register (0x5E00[5]). If this register is set, the transparent test pattern will be displayed. The following image is an example showing a transparent color bar image (see **figure 4-5**).

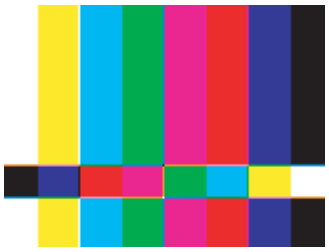
figure 4-5 transparent effect

8855_8856_DS_4_5

4.3.5 rolling bar effect

The rolling bar is set by rolling_bar_en register (0x5E00[6]). If it is set, an inverted-color rolling bar will roll from up to down. The following image is an example showing a rolling bar on color bar image (see **figure 4-6**).

figure 4-6 rolling bar effect



8855_8856_DS_4_6

table 4-3 test pattern registers

address	register name	default value	R/W	description
0x5E00	PRE CTRL00	0x00	RW	Bit[7]: Test pattern enable Bit[6]: Rolling bar function enable Bit[5]: Transparent enable 0: Disable transparent effect function 1: Enable transparent effect function Bit[4]: Square mode 0: Color square 1: Black-white square Bit[3:2]: Color bar style 00: Standard color bar 01: Top-bottom darker color bar 10: Right-left darker color bar 11: Bottom-top darker color bar Bit[1:0]: Test pattern mode 00: Color bar 01: Random data 10: Square pattern 11: Black image
0x5E01	PRE CTRL01	0x41	RW	Bit[6]: Window cut enable 0: Do not cut the redundant pixels 1: Cut the redundant pixels Bit[5]: two_lsb_0_en When set, two LSBs of output data are 0 Bit[4]: Same seed enable When set, the seed used to generate the random data are same which is set in seed register Bit[3:0]: Random seed Seed used in generating random data

4.4 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines and optically shielded (black) pixels on the right side. These lines and columns are used as reference for black level calibration. The main function of the BLC is to adjust all normal pixel values based on the values of the black levels. Register 0x4020~0x4027 are defined reference windows for black level calibration, these registers can be adjusted manually through an output window.

Black level adjustments can be made with registers 0x4000, 0x4004, and 0x4005.

table 4-4 BLC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x4000	BLC CTRL 00	0x03	RW	Bit[7:5]: r_num_add_o Bit[4]: r_black_line_sel_o Bit[3]: Target adjust disable Use offset to adjust target 0: Enable 1: Disable Bit[2]: Compensation enable Adjust on offset due to gain change 0: Disable 1: Enable Bit[1]: Dither_en 1 bit dithering 0: Disable 1: Enable Bit[0]: Median_en Median filter function enable
0x4001	BLC CTRL 01	0xE0	RW	Bit[7]: r_gain_trig_beh_o Bit[6]: r_format_trig_beh_o Bit[5]: Kocef manual enable Bit[4]: Zero line out enable Bit[3]: Black line out enable Bit[1:0]: Bypass mode
0x4002	BLC CTRL 02	0x00	RW	Bit[1:0]: Blacklevel target[9:8] High 2 bits
0x4003	BLC CTRL 03	0x10	RW	Bit[7:0]: Blacklevel target[7:0] Low 8 bits
0x4004	BLC CTRL 04	0x00	RW	Bit[3:0]: Horizontal win start[11:8] Horizontal win start high 4 bits
0x4005	BLC CTRL 05	0x02	RW	Bit[7:0]: Horizontal win start[7:0] Horizontal win start low 8 bits
0x4006	BLC CTRL 06	0x00	RW	Bit[3:0]: Horizontal win pad[11:8] Horizontal win pad high 4 bits

table 4-4 BLC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x4007	BLC CTRL 07	0x02	RW	Bit[7:0]: Horizontal win pad[7:0] Horizontal win pad low 8 bits
0x4008	BLC CTRL 08	0x02	RW	Bit[7:0]: Black line start line
0x4009	BLC CTRL 09	0x05	RW	Bit[7:0]: Black line end line
0x400A	BLC CTRL 0A	0x02	RW	Bit[7:0]: Offset trigger threshold[15:8] Offset limit threshold high 8 bits
0x400B	BLC CTRL 0B	0x00	RW	Bit[7:0]: Offset trigger threshold[7:0] Offset limit threshold low 8 bits
0x400C	BLC CTRL 0C	0x00	RW	Bit[7:0]: CVDN black lines start
0x400D	BLC CTRL 0D	0x00	RW	Bit[7:0]: CVDN black lines end
0x400E	BLC CTRL 0E	0x00	RW	Bit[7]: r_zero_ln_sel Bit[6:0]: r_mf_th_o
0x400F	BLC CTRL 0F	0x80	RW	Bit[7]: r_exp_chg_trig_en_o Bit[6]: r_set_zb_o Bit[5:4]: r_manu_cvdn_out_en Bit[3]: r_v15_one-channel_en Bit[2]: r_en_adp_k_o Bit[1]: r_dc_offset_mode_o Bit[0]: r_compute_offset_v15_o
0x4010	BLC CTRL 10	0xF0	RW	Bit[7]: Offset trigger enable Bit[6]: Gain change trigger enable Bit[5]: Format change trigger enable Bit[4]: Reset trigger enable Bit[3]: Manual average enable Bit[2]: Manual trigger Bit[1]: Freeze enable Bit[0]: Offset always update
0x4011	BLC CTRL 11	0xFF	RW	Bit[7]: offset_cmp_man_en Bit[6]: Offset trigger multiframe enable Bit[5]: Format trigger multiframe enable Bit[4]: Gain trigger multiframe enable Bit[3]: Reset trigger multiframe enable Bit[2]: Offset trigger multiframe mode Bit[1]: Format trigger multiframe mode Bit[0]: Gain trigger multiframe mode
0x4012	BLC CTRL 12	0x08	RW	Bit[5:0]: Reset trigger frame number
0x4013	BLC CTRL 13	0x02	RW	Bit[5:0]: Format trigger frame number
0x4014	BLC CTRL 14	0x02	RW	Bit[5:0]: Gain trigger frame number
0x4015	BLC CTRL 15	0x02	RW	Bit[5:0]: Offset trigger frame number

table 4-4 BLC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x4016	BLC CTRL 16	0x00	RW	Bit[1:0]: Offset trigger threshold[9:8] Offset trigger threshold high 2 bits
0x4017	BLC CTRL 17	0x04	RW	Bit[7:0]: Offset trigger threshold[7:0] Offset trigger threshold low 8 bits
0x4020	BLC CTRL 20	0x00	RW	Bit[5:0]: Offset compensation k000
0x4021	BLC CTRL 21	0x00	RW	Bit[5:0]: Offset compensation k001
0x4022	BLC CTRL 22	0x00	RW	Bit[5:0]: Offset compensation k010
0x4023	BLC CTRL 23	0x00	RW	Bit[5:0]: Offset compensation k011
0x4024	BLC CTRL 24	0x00	RW	Bit[5:0]: Offset compensation th000
0x4025	BLC CTRL 25	0x00	RW	Bit[5:0]: Offset compensation th001
0x4026	BLC CTRL 26	0x00	RW	Bit[5:0]: Offset compensation th010
0x4027	BLC CTRL 27	0x00	RW	Bit[5:0]: Offset compensation th011
0x4030	BLC CTRL 30	0x00	RW	Bit[1:0]: Offset man 000[9:8]
0x4031	BLC CTRL 31	0x00	RW	Bit[7:0]: Offset man 000[7:0]
0x4032	BLC CTRL 32	0x00	RW	Bit[1:0]: Offset man 001[9:8]
0x4033	BLC CTRL 33	0x00	RW	Bit[7:0]: Offset man 001[7:0]
0x4034	BLC CTRL 34	0x00	RW	Bit[1:0]: Offset man 010[9:8]
0x4035	BLC CTRL 35	0x00	RW	Bit[7:0]: Offset man 010[7:0]
0x4036	BLC CTRL 36	0x00	RW	Bit[1:0]: Offset man 011[9:8]
0x4037	BLC CTRL 37	0x00	RW	Bit[7:0]: Offset man 011[7:0]
0x4038	BLC CTRL 38	0x00	RW	Bit[1:0]: Offset man 100[9:8]
0x4039	BLC CTRL 39	0x00	RW	Bit[7:0]: Offset man 100[7:0]
0x403A	BLC CTRL 3A	0x00	RW	Bit[1:0]: Offset man 101[9:8]
0x403B	BLC CTRL 3B	0x00	RW	Bit[7:0]: Offset man 101[7:0]
0x403C	BLC CTRL 3C	0x00	RW	Bit[1:0]: Offset man 110[9:8]
0x403D	BLC CTRL 3D	0x00	RW	Bit[7:0]: Offset man 110[7:0]
0x403E	BLC CTRL 3E	0x00	RW	Bit[1:0]: Offset man 111[9:8]
0x403F	BLC CTRL 3F	0x00	RW	Bit[7:0]: Offset man 111[7:0]
0x4040	BLC CTRL 40	0x00	RW	Bit[7:0]: Zline start
0x4041	BLC CTRL 41	0x01	RW	Bit[7:0]: Zline end
0x4042	BLC CTRL 42	0x00	RW	Bit[1:0]: kcoef_b_man[9:8]

table 4-4 BLC control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x4043	BLC CTRL 43	0x80	RW	Bit[7:0]: kcoef_b_man[7:0]
0x4044	BLC CTRL 44	0x00	RW	Bit[1:0]: kcoef_gb_man[9:8]
0x4045	BLC CTRL 45	0x80	RW	Bit[7:0]: kcoef_gb_man[7:0]
0x4046	BLC CTRL 46	0x00	RW	Bit[1:0]: kcoef_gr_man[9:8]
0x4047	BLC CTRL 47	0x80	RW	Bit[7:0]: kcoef_gr_man[7:0]
0x4048	BLC CTRL 48	0x00	RW	Bit[1:0]: kcoef_r_man[9:8]
0x4049	BLC CTRL 49	0x80	RW	Bit[7:0]: kcoef_r_man[7:0]
0x404A	BLC CTRL 4A	0x30	RW	Bit[7:0]: dc_th_1
0x404B	BLC CTRL 4B	0x18	RW	Bit[7:0]: dc_th_1
0x404C	BLC CTRL 4C	0x60	RW	Bit[6]: rst_trig_opt Bit[5:0]: Average weight
0x404D	BLC CTRL 4D	0x00	RW	Bit[1:0]: rnd_gain_th[9:8]
0x404E	BLC CTRL 4E	0x00	RW	Bit[7:0]: rnf_gain_th[7:0]
0x404F	BLC CTRL 4F	0x00	RW	Bit[7:0]: dc_th_1_s
0x4050	BLC CTRL 50	0x00	RW	Bit[7:0]: dc_th_2_s
0x4060	BLC CTRL 60	–	R	Bit[1:0]: BLC_offset000[9:8]
0x4061	BLC CTRL 61	–	R	Bit[7:0]: BLC_offset000[7:0]
0x4062	BLC CTRL 62	–	R	Bit[1:0]: BLC_offset001[9:8]
0x4063	BLC CTRL 63	–	R	Bit[7:0]: BLC_offset001[7:0]
0x4064	BLC CTRL 64	–	R	Bit[1:0]: BLC_offset010[9:8]
0x4065	BLC CTRL 65	–	R	Bit[7:0]: BLC_offset010[7:0]
0x4066	BLC CTRL 66	–	R	Bit[1:0]: BLC_offset011[9:8]
0x4067	BLC CTRL 67	–	R	Bit[7:0]: BLC_offset011[7:0]

4.5 one time programmable (OTP) memory

The OV8856 supports a maximum of 1024 bytes of one-time programmable (OTP) memory to store chip identification and manufacturing information, which can be used to update the sensor's default setting and can be controlled through the SCCB (see **table 4-5**). Out of 8k bits (1024 bytes), 4k bits are reserved for OmniVision and 4k bits are reserved for customers.

4.5.1 OTP other functions

OTP loading data can be triggered when power up or writing 0x01 to register 0x3D81. Power up loading data is enabled by register 0x3D85[2], by default it is off. Auto mode and manual mode can be chosen by setting register 0x3D84[6] to 0 and 1, respectively, and by default, it is in auto mode. In auto mode, all data in the OTP will be loaded to the OTP buffer; while in manual mode, part of the data which is defined by the start address ({0x3D88,0x3D89}) and the end address ({0x3D8A,0x3D8B}) of the OTP will be loaded to the OTP buffer.

The OV8856 supports loading setting. When 0xDD as a head byte is read out from the start address, which is set by {0x3D8C, 0x3D8D}, setting is recognized. While the setting is being read out from the OTP, it is being written to the OTP buffer, and at the same time, interpreting to the register write command. Loading setting is controlled by registers 0x3D85[1] and 0x3D85[0], which enable power up loading setting and writing register loading setting, respectively. When accessing OTP content (i.e., programming or loading OTP), OTP option must be disabled by setting register bit 0x5001[3] = 0.

OTP data can be loaded from 0x7000 to 0x73FF through SCCB interface using a total of 1k bytes. 0x7000 ~ 0x700F and 0x7210 ~ 0x73FF are reserved for OmniVision, while 0x7010 ~ 0x720F (512 bytes) are reserved for customer use.

To program the OTP:

```
6C 5001 00; [3] OTP option disable
6C 3D84 40; [6] manual mode enable
6C 3D85 00
6C 3D88 71; manual OTP start address for access
6C 3D89 00
6C 3D8A 71; manual OTP end address for access
6C 3D8B 0C
6C 0100 01; stream mode enable
;delay 20ms
6C 7100 DD
6C 7101 A3
6C 7102 30
6C 7103 00
6C 7104 11
6C 7105 22
6C 7106 33
6C 7107 44
6C 7108 53
6C 7109 55
```

```
6C 710A 66
6C 710B 77
6C 710C 88
6C 3D80 01;[0] program enable
;delay 200ms
6C 3D80 00
```

Setting for loading:

```
...
6C 5001 00; [3] OTP option disable
6C 3D88 71; manual OTP start address for access
6C 3D89 00
6C 3D8A 71; manual OTP end address for access
6C 3D8B 0C
6C 3D85 06; [2] OTP load data enable
; [1] OTP load setting enable
6C 3D8C 01; Start address OTP setting table, the first byte of OTP setting table should
be 0xDD
6C 3D8D 00;
6C 0100 01; stream mode enable, after streaming of the first power up, OV8856 will load
setting from OTP if 3D85[2:1]=2'b11
```

The OV8856 supports OTP BIST. When register 0x3D85[4] is set to 1, the BIST function is enabled. When OTP loading data, the data which is read out from the OTP can be compared with zero or the data with the same address in the register, which can be controlled by setting register 0x3D85[5] to 1 or 0, respectively. After the BIST done, the BIST done flag can be read out from register 0x3D81[4], the BIST error flag can be read out from 0x3D81[5], and the address of the first error can be read out from {0x3D8E, 0x3D8F}.

table 4-5 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x7000~ 0x75FF	OTP_SRAM	0x00	RW	Bit[7:0]: OTP buffer
0x3D80	OTP_PROGRAM_CTRL	–	RW	Bit[7]: OTP_wr_busy (read only) Bit[0]: OTP_program_enable (write only)
0x3D81	OTP_LOAD_CTRL	–	RW	Bit[7]: OTP_rd_busy (read only) Bit[5]: OTP_bist_error (read only) Bit[4]: OTP_bist_done (read only) Bit[0]: OTP_load_enable (read and write)

table 4-5 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D84	OTP_MODE_CTRL	0x00	RW	Bit[7]: Program disable 1: Disable Bit[6]: Mode select 0: Auto mode 1: Manual mode
0x3D85	OTP_REG85	0x13	RW	Bit[5]: OTP_bist_select 0: Compare with SRAM 1: Compare with zero Bit[4]: OTP_bist_enable Bit[2]: OTP power up load data enable Bit[1]: OTP power up load setting enable Bit[0]: OTP write register load setting enable
0x3D88	OTP_START_ADDRESS	0x00	RW	OTP Start High Address for Manual Mode
0x3D89	OTP_START_ADDRESS	0x00	RW	OTP Start Low Address for Manual Mode
0x3D8A	OTP_END_ADDRESS	0x00	RW	OTP End High Address For Manual Mode
0x3D8B	OTP_END_ADDRESS	0x00	RW	OTP End Low Address For Manual Mode
0x3D8C	OTP_SETTING_STT_ADDRESS	0x00	RW	OTP Start High Address For Load Setting
0x3D8D	OTP_SETTING_STT_ADDRESS	0x00	RW	OTP Start Low Address For Load Setting
0x3D8E	OTP_BIST_ERR_ADDRESS	–	R	OTP Check Error Address High
0x3D8F	OTP_BIST_ERR_ADDRESS	–	R	OTP Check Error Address Low

5 image sensor processor digital functions

5.1 ISP top

The main purpose of the ISP top includes:

- integrate all sub-modules
- create necessary control signals

table 5-1 ISP top registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x77	RW	Bit[7]: blc_hdr_en Bit[6]: dcblc_en Bit[5]: lenc_en Bit[4]: awb_gain_en Bit[3]: r_long_short_rvs Bit[2]: bc_en Bit[1]: wc_en Bit[0]: blc_en
0x5001	ISP CTRL01	0x0A	RW	Bit[7]: blc_vsync_sel Bit[6]: pre_vsync_sel Bit[5]: r_rlong_sel Bit[4]: lenc_real_gain_rvs Bit[3]: otp_option_en Bit[2]: rblue_in_rvs Bit[1]: awbm_bias_on Bit[0]: latch_en
0x5002	ISP CTRL02	0x20	RW	Bit[7:6]: dig_gain_blc Bit[5]: bufctrl_en Bit[4:2]: ln_delay Bit[1]: man_noswap_en Bit[0]: blc_hdr_ls_rvs
0x5003	ISP CTRL03	0xC8	RW	Bit[7]: lenc_bias_on Bit[6:5]: lenc_px_order_man Bit[4]: lenc_px_order_man_en Bit[3]: insize_auto Bit[2]: dpc_hdr_ls_rvs Bit[1]: gfirst_rvs Bit[0]: rblue_rvs
0x5004	ISP CTRL04	0x00	RW	Bit[4]: r_dig_sel_from_reg Bit[2]: blc_mirror_opt Bit[1]: dig_gain_en Bit[0]: lenc_decomp_en
0x5005	ISP CTRL05	0x00	RW	Bit[7]: isp_bypass_mode Bit[5]: bypass_isp

table 5-1 ISP top registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5006	ISP CTRL06	0x00	RW	Bit[3:0]: hsize_in_r[11:8]
0x5007	ISP CTRL07	0x00	RW	Bit[7:0]: hsize_in_r[7:0]
0x5008	ISP CTRL08	0x00	RW	Bit[3:0]: vsize_in_r[11:8]
0x5009	ISP CTRL09	0x00	RW	Bit[7:0]: vsize_in_r[7:0]
0x500E	ISP CTRL0E	0x00	RW	Bit[3:0]: dpc_hsize_in[11:8]
0x500F	ISP CTRL0F	0x00	RW	Bit[7:0]: dpc_hsize_in[7:0]
0x5010	ISP CTRL10	0x00	RW	Bit[3:0]: dpc_vsize_in[11:8]
0x5011	ISP CTRL11	0x00	RW	Bit[7:0]: dpc_vsize_in[7:0]
0x5012	ISP CTRL12	0x00	RW	Bit[3:0]: dig_gain_l[11:8]
0x5013	ISP CTRL13	0x00	RW	Bit[7:0]: dig_gain_l[7:0]
0x5014	ISP CTRL14	0x00	RW	Bit[3:0]: dig_gain_s[11:8]
0x5015	ISP CTRL15	0x00	RW	Bit[7:0]: dig_gain_s[7:0]
0x5016	ISP CTRL16	0x00	RW	Bit[7]: r_cen_sel Bit[6]: r_cen Bit[1]: dpc_size_man
0x5017	ISP CTRL17	0x00	RW	Bit[5]: sram_test_dpc2 Bit[4]: sram_test_dpc1 Bit[1]: sram_rme_dpc2 Bit[0]: sram_rme_dpc1
0x5018	ISP CTRL18	0x00	RW	Bit[7:4]: sram_rm_dpc2 Bit[3:0]: sram_rm_dpc1
0x5019	ISP CTRL19	0x04	RW	Bit[3:0]: mwb_r_gain_man_l[11:8]
0x501A	ISP CTRL1A	0x00	RW	Bit[7:0]: mwb_r_gain_man_l[7:0]
0x501B	ISP CTRL1B	0x04	RW	Bit[3:0]: mwb_g_gain_man_l[11:8]
0x501C	ISP CTRL1C	0x00	RW	Bit[7:0]: mwb_g_gain_man_l[7:0]
0x501D	ISP CTRL1D	0x04	RW	Bit[3:0]: mwb_b_gain_man_l[11:8]
0x501E	ISP CTRL1E	0x00	RW	Bit[7:0]: mwb_b_gain_man_l[7:0]
0x501F	ISP CTRL1F	0x04	RW	Bit[3:0]: mwb_r_gain_man_s[11:8]
0x5020	ISP CTRL20	0x00	RW	Bit[7:0]: mwb_r_gain_man_s[7:0]
0x5021	ISP CTRL21	0x04	RW	Bit[3:0]: mwb_g_gain_man_s[11:8]
0x5022	ISP CTRL22	0x00	RW	Bit[7:0]: mwb_g_gain_man_s[7:0]
0x5023	ISP CTRL23	0x04	RW	Bit[3:0]: mwb_b_gain_man_s[11:8]

table 5-1 ISP top registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5024	ISP CTRL24	0x00	RW	Bit[7:0]: mwb_b_gain_man_s[7:0]
0x5025	ISP CTRL25	0x18	RW	Bit[5]: r_embed_line_en Bit[3]: r_isp_raw_en Bit[2:0]: r_win_y_offset_adjust
0x5026	ISP CTRL26	0x2A	RW	Bit[5]: r_dmy_auto_en Bit[4]: r_bias_man_en Bit[3]: vsync_puls Bit[1:0]: px_order_man
0x502D	ISP CTRL2D	0x00	RW	Bit[7:0]: snr_bias_man
0x502E	ISP CTRL2e	0x00	RW	Bit[7]: blc_px_man_en Bit[6:5]: blc_px_man Bit[4]: r_blc_rblue_man_en Bit[3]: r_blc_rblue_man Bit[2]: pre_px_man_en Bit[1]: r_zero_rblue_man_en Bit[0]: r_zero_rblue_man
0x502F	ISP CTRL2F	0x00	RW	Bit[7]: dpc_data_switch Bit[6]: dpc_px_man_en Bit[5:4]: dpc_px_man Bit[2]: r_awb_px_man_en Bit[1:0]: r_awb_px_man
0x5030	ISP CTRL30	0x41	RW	Bit[7:6]: isp_sof_sel Bit[1:0]: isp_eof_sel

5.2 pre_DSP

The main purposes of the pre_DSP module include:

- adjust RBlue signals and data
- create color bar image
- determine the sizes of input image by removing redundant data
- create control signals

table 5-2 pre_DSP registers

address	register name	default value	R/W	description
0x5E00	PRE CTRL00	0x00	RW	Bit[7]: Test pattern enable Bit[6]: Rolling bar function enable Bit[5]: Transparent enable 0: Disable transparent effect function 1: Enable transparent effect function Bit[4]: Square mode 0: Color square 1: Black-white square Bit[3:2]: Color bar style 00: Standard color bar 01: Top-bottom darker color bar 10: Right-left darker color bar 11: Bottom-top darker color bar Bit[1:0]: Test pattern mode 00: Color bar 01: Random data 10: Square pattern 11: Black image
0x5E01	PRE CTRL01	0x41	RW	Bit[6]: Window cut enable Bit[5]: two_lsb_0_en Set lowest two bits to 0 Bit[4]: Same seed enable Reset seed to 0x5E01[3:0] each frame Bit[3:0]: Random seed Seed used in generating random data

5.3 defective pixel cancellation (DPC)

The DPC uses a one line buffer and removes defect pixels. It also supports black/white mode.

table 5-3 DPC control registers

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x77	RW	Bit[6]: DPC function enable

5.4 window cut (WINC)

The main purpose of the WINC module is to make the image size to be real size by removing offset.

table 5-4 WINC control registers

address	register name	default value	R/W	description
0x5A00	WINC CTRL00	0x00	RW	Bit[3:0]: x_start_offset[11:8] Start address in horizontal
0x5A01	WINC CTRL01	0x00	RW	Bit[7:0]: x_start_offset[7:0]
0x5A02	WINC CTRL02	0x00	RW	Bit[3:0]: y_start_offset[11:8] Start address in vertical
0x5A03	WINC CTRL03	0x00	RW	Bit[7:0]: y_start_offset[7:0]
0x5A04	WINC CTRL04	0x0C	RW	Bit[3:0]: window_width[11:8] Select whole zone width
0x5A05	WINC CTRL05	0xE0	RW	Bit[7:0]: window_width[7:0] Select whole zone width
0x5A06	WINC CTRL06	0x09	RW	Bit[3:0]: window_height[11:8] Select whole zone height
0x5A07	WINC CTRL07	0xB0	RW	Bit[7:0]: window_height[7:0] Select whole zone height
0x5A08	WINC CTRL08	0x06	RW	Bit[3]: Window valid select option (for debug) 0: Select new valid_1d 1: Select original valid_1d Bit[2]: Select embedded line flag 0: Select first line as embedded flag 1: Select last line as embedded flag Bit[1]: Window enable option 0: Disable window after last valid line 1: Get enable from register Bit[0]: Manual window enable 0: Window size from window top 1: Window size from 0x5A00 to 0x5A07

5.5 lens correction (LENC)

The LENC algorithm compensates for the illumination drop off in the corners due to the lens. Based on the radius of each pixel to the lens, the algorithm calculates a gain for each pixel and then corrects each pixel with the calculated gain to compensate for the light distribution due to the lens curvature. Additionally, the LENC supports subsampling in both the horizontal and vertical directions. LENC is performed in the RGB domain.

Both luminance channel and color channel consist of 80 (10x8) control points. **figure 5-1** displays the control points of B,G, and R channels.

figure 5-1 control points of luminance and color channels

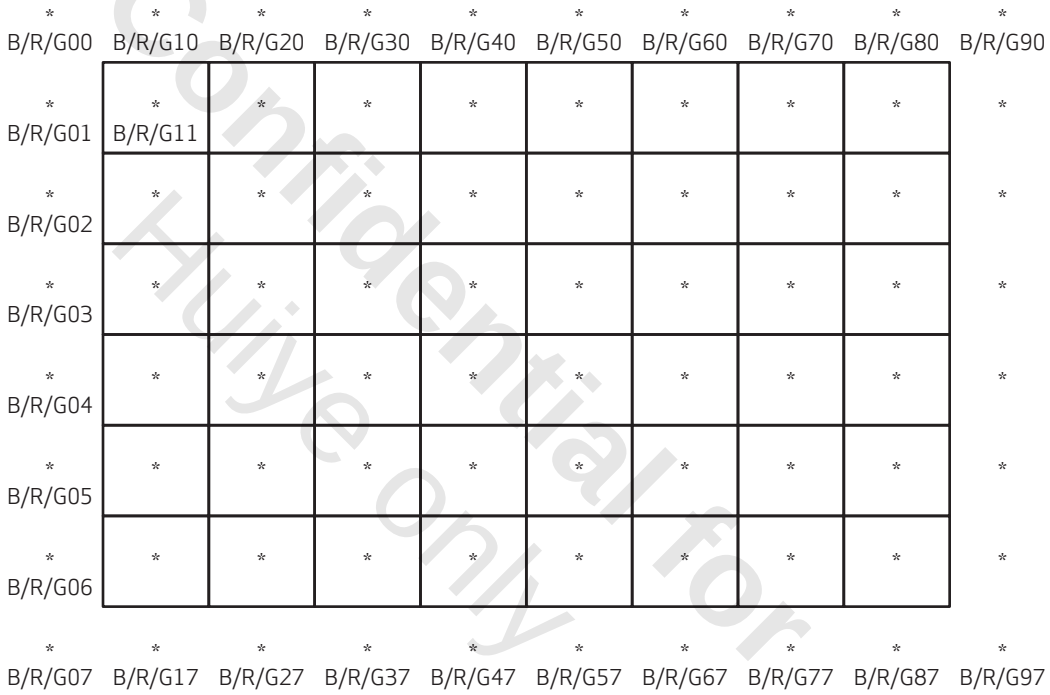
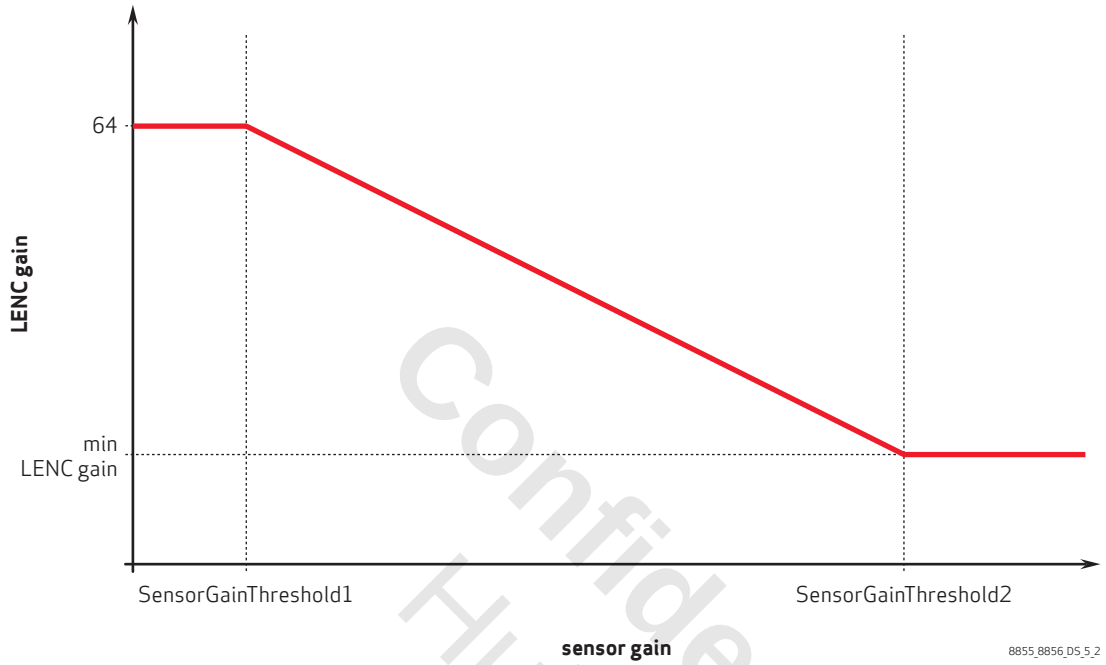


figure 5-2 luminance compensation level calculation



note There is a lens calibration tool that can be used for calibrating these settings required for a specific module. Contact your local OmniVision FAE for generating these settings.

table 5-5 LENC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5900	LENC G00	0x00	RW	Bit[5:0]: Control point G00 for luminance compensation
0x5901	LENC G01	0x00	RW	Bit[5:0]: Control point G01 for luminance compensation
0x5902	LENC G02	0x00	RW	Bit[5:0]: Control point G02 for luminance compensation
0x5903	LENC G03	0x00	RW	Bit[5:0]: Control point G03 for luminance compensation
0x5904	LENC G04	0x00	RW	Bit[5:0]: Control point G04 for luminance compensation
0x5905	LENC G05	0x00	RW	Bit[5:0]: Control point G05 for luminance compensation
0x5906	LENC G10	0x00	RW	Bit[5:0]: Control point G10 for luminance compensation

table 5-5 LENC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5907	LENC G11	0x00	RW	Bit[5:0]: Control point G11 for luminance compensation
0x5908	LENC G12	0x00	RW	Bit[5:0]: Control point G12 for luminance compensation
0x5909~ 0x594E	LENC G13~LENC G96	0x00	RW	Bit[5:0]: Control point G13~G54 for luminance compensation
0x594F	LENC G97	0x00	RW	Bit[5:0]: Control point G55 for luminance compensation
0x5950	LENC B00	0x80	RW	Bit[4:0]: Control point B00 for blue channel compensation
0x5951	LENC B01	0x80	RW	Bit[4:0]: Control point B01 for blue channel compensation
0x5952	LENC B02	0x80	RW	Bit[4:0]: Control point B02 for blue channel compensation
0x5953	LENC B03	0x80	RW	Bit[4:0]: Control point B03 for blue channel compensation
0x5954	LENC B04	0x80	RW	Bit[4:0]: Control point B04 for blue channel compensation
0x5955	LENC B05	0x80	RW	Bit[4:0]: Control point B05 for blue channel compensation
0x5956	LENC B10	0x80	RW	Bit[4:0]: Control point B10 for blue channel compensation
0x5957	LENC B11	0x80	RW	Bit[4:0]: Control point B11 for blue channel compensation
0x5958	LENC B12	0x80	RW	Bit[4:0]: Control point B12 for blue channel compensation
0x5959~ 0x599E	LENC B13~LENC B96	0x80	RW	Bit[4:0]: Control point B13~B54 for blue channel compensation
0x599F	LENC B97	0x80	RW	Bit[4:0]: Control point B55 for blue channel compensation
0x59A0	LENC R00	0x80	RW	Bit[4:0]: Control point R00 for red channel compensation
0x59A1	LENC R01	0x80	RW	Bit[4:0]: Control point R01 for red channel compensation
0x59A2	LENC R02	0x80	RW	Bit[4:0]: Control point R02 for red channel compensation
0x59A3	LENC R03	0x80	RW	Bit[4:0]: Control point R03 for red channel compensation

table 5-5 LENC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x59A4	LENC R04	0x80	RW	Bit[4:0]: Control point R04 for red channel compensation
0x59A5	LENC R05	0x80	RW	Bit[4:0]: Control point R05 for red channel compensation
0x59A6	LENC R10	0x80	RW	Bit[4:0]: Control point R10 for red channel compensation
0x59A7	LENC R11	0x80	RW	Bit[4:0]: Control point R11 for red channel compensation
0x59A8	LENC R12	0x80	RW	Bit[4:0]: Control point R12 for red channel compensation
0x59A9~ 0x59EE	LENC R13~LENC R96	0x80	RW	Bit[4:0]: Control point R13~R54 for red channel compensation
0x59EF	LENC R97	0x80	RW	Bit[4:0]: Control point R55 for red channel compensation
0x59F0	LENC MAXGAIN	0x60	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will be the minimum value (min LENC gain). Register value is 16 times sensor gain
0x59F1	LENC MINGAIN	0x40	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will start to decrease; otherwise, the amplitude will not change. Register value is 16 times sensor gain.
0x59F2	LENC MAXQ	0x40	RW	Bit[6:0]: This value indicates the minimum amplitude which luminance channel compensates when AutoLensSwitchEnable is true. Value should be in the range [0~64]
0x59F3	LENC MINQ	0x18	RW	Bit[6:0]: Minq

table 5-5 LENC control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x59F4	LENC CTRL	0x36	RW	Bit[5]: Add BLC target after applying compensation Bit[4]: Enable BLC target for LENC 0: Disable BLC target 1: Enable BLC target Bit[3]: Br2xmode Bit[2]: autoq_en Bit[1]: dither_en Bit[0]: g2xgain_en
0x59F5	LENC HSCALE	0x02	RW	Bit[4:0]: HScale[12:8] For horizontal gain calculation, this value indicates the step between two connected horizontal pixels, where HScale = 4 × 2^18 / image width
0x59F6	LENC HSCALE	0x7C	RW	Bit[7:0]: HScale[7:0]
0x59F7	LENC VSCALE	0x01	RW	Bit[4:0]: VScale[12:8] For vertical gain calculation, this value indicates the step between two connected vertical pixels, where VScale = 4 × 2^17 / image height
0x59F8	LENC VSCALE	0x40	RW	Bit[7:0]: VScale[7:0]
0x59F9	LENC DECOMP ADDR	0x00	RW	Bit[7:0]: LENC decompression start address[15:8]
0x59FA	LENC DECOMP ADDR	0x00	RW	Bit[7:0]: LENC decompression start address[7:0]
0x59FB	RO_INFO_SEL	0x00	RW	Bit[7:0]: ro_info sel
0x59FC	LENC YOFFSET	–	R	Bit[7:0]: Input sensor vertical offset[7:0]
0x59FD	LENC INPUT	–	R	Bit[5]: Input sensor flip Bit[4]: Input sensor mirror Bit[3:2]: Input sensor Y skip Bit[1:0]: Input sensor X skip
0x59FE	LENC OVERFLOW	–	R	Bit[1]: Vertical overflow for debug Bit[0]: Horizontal overflow for debug
0x59FF	LENC QVALUE	–	R	Bit[6:0]: Real amplitude Q value

5.6 manual exposure compensation/ manual gain compensation (MEC/MGC)

Manual exposure provides exposure time settings and sensor gain.The exposure value in register 0x3500~0x3502 and 0x3510~0x3512 are in units of 1/16 line. The minimum exposure of the sensor is 6 lines and maximum exposure is VTS {0x380E, 0x380F} - 6.

Manual gain provides analog gain settings. The OV8856 has a maximum 16x analog gain.

note
For optimal performance, minimum exposure of sensor is 6 lines and maximum exposure is VTS {0x380E, 0x380F} - 6.

table 5-6 MEC/MGC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3500	LONG EXPO	0x00	RW	Bit[3:0]: Long exposure[19:16]
0x3501	LONG EXPO	0x02	RW	Bit[7:0]: Long exposure[15:8]
0x3502	LONG EXPO	0x00	RW	Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits. Shall always be 0.
0x3503	AEC MANUAL	0x00	RW	Bit[7]: priority_6 Bit[6]: Digital fraction gain delay option 0: Delay 1 frame 1: Do not delay 1 frame Bit[5]: Gain change delay option 0: Delay 1 frame 1: Do not delay 1 frame Bit[4]: Gain delay option 0: Delay 1 frame 1: Do not delay 1 frame Bit[3]: gain_prec16_en Bit[2]: Gain manual as sensor gain 0: Input gain as real gain format 1: Input gain as sensor gain format Bit[1]: Exposure delay option (must be 0) 0: Delay 1 frame Bit[0]: Exposure change delay option (must be 0) 0: Delay 1 frame
0x3505	GCVT OPTION	0x80	RW	Gain Conversation Option Bit[7]: DAC fixed gain bit Bit[6]: switch_snr_gain_en Bit[5:4]: Sensor gain fixed bit Bit[3:2]: Sensor gain pregain option (debug only, always set it to 0) Bit[1:0]: Sensor gain option for transferring real gain to sensor gain format
0x3507	GAIN SHIFT	0x00	RW	Bit[1:0]: Gain shift option 00: No shift 01: Left shift 1 bit 10: Left shift 2 bits 11: Left shift 3 bits

table 5-6 MEC/MGC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3508	LONG GAIN	0x00	RW	Bit[4:0]: Long gain[12:8]
0x3509	LONG GAIN	0x80	RW	Bit[7:0]: Long gain[7:0] If 0x3503[2]=0, gain[12:0] is real gain format, where low 7 bits are fraction bits, real_gain = gain[12:0]/128, for example: 0x080 is 1x gain, 0x100 is 2x gain If 0x3503[2]=1, gain[12:0] is sensor gain format, gain[12:8] is coarse gain, 00000: 1x, 00001: 2x, 00011: 4x, 00111: 8x, gain[7] is 1, gain[6:3] is fine gain, gain[2:0] is always 0. For example: 0x080 is 1x gain, 0x180 is 2x gain, 0x380 is 4x gain
0x350A	LONG DIGIGAIN	0x04	RW	Bit[3:0]: Long digital gain[11:8]
0x350B	LONG DIGIGAIN	0x00	RW	Bit[7:0]: Long digital gain[7:0]
0x350C	SHORT GAIN	0x00	RW	Bit[4:0]: Short gain[12:8]
0x350D	SHORT GAIN	0x80	RW	Bit[7:0]: Short gain[7:0]
0x350E	SHORT DIGIGAIN	0x04	RW	Bit[7:0]: Short digital gain[11:4]
0x350F	SHORT DIGIGAIN	0x00	RW	Bit[5:2]: Short digital gain Low 10 bits are fraction bits
0x3510	SHORT EXPO	0x00	RW	Bit[3:0]: Short exposure[19:16]
0x3511	SHORT EXPO	0x02	RW	Bit[7:0]: Short exposure[15:8]
0x3512	SHORT EXPO	0x00	RW	Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits
0x3513	SNR_GAIN_L	–	R	Bit[5:0]: Long sensor gain[13:8]
0x3514	SNR_GAIN_L	–	R	Bit[7:0]: Long sensor gain[7:0]
0x3515	FINE_SNR_GAIN_L	–	R	Bit[5:0]: Long fine sensor gain
0x3516	SNR_GAIN_S	–	R	Bit[5:0]: Short sensor gain[13:8]
0x3517	SNR_GAIN_S	–	R	Bit[7:0]: Short sensor gain[7:0]
0x3518	FINE_SNR_GAIN_S	–	R	Bit[5:0]: Short fine sensor gain

6 register tables

The following tables provide descriptions of the device control registers contained in the OV8856. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x6C for write and 0x6D for read (when SID=1, 0x20 for write and 0x21 for read).

6.1 PLL control [0x0300 - 0x0312, 0x031B - 0x031C, 0x031E]

table 6-1 PLL control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x0300	PLL_CTRL_0	0x04	RW	Bit[7:3]: Not used Bit[2:0]: pll1_pre_div
0x0301	PLL_CTRL_1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pll1_multiplier[9:8]
0x0302	PLL_CTRL_2	0x7D	RW	Bit[7:0]: pll1_multiplier[7:0]
0x0303	PLL_CTRL_3	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pll1_divm
0x0304	PLL_CTRL_4	0x03	RW	Bit[7:2]: Not used Bit[1:0]: pll1_div_mipi
0x0305	PLL_CTRL_5	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pll1_div_sp
0x0306	PLL_CTRL_6	0x01	RW	Bit[7:1]: Not used Bit[0]: pll1_div_s
0x0307	NOT USED	–	–	Not Used
0x0308	PLL_CTRL_8	0x00	RW	Bit[7:1]: Not used Bit[0]: pll1_bypass
0x0309	PLL_CTRL_9	0x01	RW	Bit[7:3]: Not used Bit[2:0]: pll1_cp
0x030A	PLL_CTRL_A	0x00	RW	Bit[7:4]: Not used Bit[3:1]: pll1_reserve Bit[0]: pll1_predivp
0x030B	PLL_CTRL_B	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pll2_pre_div
0x030C	PLL_CTRL_C	0x00	RW	Bit[7:2]: Not used Bit[1:0]: pll2_r_divp[9:8]
0x030D	PLL_CTRL_D	0x1E	RW	Bit[7:0]: pll2_r_divp[7:0]
0x030E	PLL_CTRL_E	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pll2_r_divs

table 6-1 PLL control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x030F	PLL_CTRL_F	0x06	RW	Bit[7:4]: Not used Bit[3:0]: pll2_r_divsp
0x0310	PLL_CTRL_10	0x01	RW	Bit[7:3]: Not used Bit[2:0]: pll2_r_cp
0x0311	PLL_CTRL_11	0x00	RW	Bit[7:1]: Not used Bit[0]: pll2_bypass
0x0312	PLL_CTRL_12	0x01	RW	Bit[7:6]: pll2_reserve Bit[5]: pll2_sync_rst Bit[4]: pll2_pre_div0 Bit[3:0]: pll2_r_divdac
0x031B	PLL_CTRL_1B	0x00	RW	Bit[7:1]: Not used Bit[0]: pll1_rst
0x031C	PLL_CTRL_1C	0x00	RW	Bit[7:1]: Not used Bit[0]: pll2_rst
0x031E	PLL_CTRL_1E	0x04	RW	Bit[7:4]: Not used Bit[3]: pll1_no_lat Bit[2]: Not used Bit[1:0]: mipi_bitsel_man

6.2 system control [0x3000 - 0x3024, 0x302A, 0x3030 - 0x3040, 0x3043]

table 6-2 system control registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x3000	PAD OEN0	0x00	RW	Bit[7:6]: Not used Bit[5]: io_fsin_oen Bit[4:0]: Not used
0x3001	NOT USED	–	–	Not Used
0x3002	PAD OEN2	0x21	RW	Bit[7]: Reserved Bit[6]: io_ulpm_oen Bit[5:0]: Not used
0x3003	GPIO IN	–	R	Bit[7]: Not used Bit[6]: p_sid_i Bit[5]: p_ulpm_i Bit[4]: p_strobe_i Bit[3]: io_fsin_i Bit[2:0]: Reserved

table 6-2 system control registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x3004	SCCB ID	0x6C	RW	Bit[7:0]: sccb_id SCCB programed ID
0x3005	CLKRST5	0xF0	RW	Bit[7:6]: Not used Bit[5]: sclk_src Bit[4]: sclk_syncfifo Bit[3]: Not used Bit[2]: rst_dpcm Bit[1]: rst_src Bit[0]: rst_syncfifo
0x3006	SCCB ID2	0x42	RW	Bit[7:0]: sccb_id2 SCCB ID2
0x3007	R ISPOUT BITSEL	0x20	RW	Bit[7]: pll12_daclk_sel Bit[6]: r_pump_clk_sel Bit[5]: r_rgbc Bit[4]: r_ilpwm_out_sel Bit[3]: r_rst_pll_sleep_dis Bit[2]: r_db_out_en Bit[1:0]: r_vsync_sel 00: mipi_vsync 01: lvds_vsync 10: fmt_vsync 11: tc_vsync
0x3008~ 0x3009	NOT USED	–	–	Not Used
0x300A	CHIP ID	0x00	R	Bit[7:0]: chip_id[23:16]
0x300B	CHIP ID	0x88	R	Bit[7:0]: chip_id[15:8]
0x300C	CHIP ID	0x5A	R	Bit[7:0]: chip_id[7:0] For PID, read OTP register 0x7000 = 0x00, register 0x7001 = 0x88, and register 0x7002 = 0x56**section 2.1.1**)
0x300D	PAD OUT2	0x00	RW	Bit[7:4]: Not used Bit[3]: io_strobe_o Bit[2]: io_sda_o Bit[1:0]: Reserved
0x300E	PAD OUT3	0x00	RW	Bit[7:6]: Not used Bit[5]: io_fsin_sel Bit[4:0]: Not used
0x300F	NOT USED	–	–	Not Used

table 6-2 system control registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x3010	PAD SEL2	0x00	RW	Bit[7:4]: Not used Bit[3]: io_strobe_sel Bit[2]: io_sda_sel Bit[1:0]: Reserved
0x3011	PAD	0x00	RW	Bit[7]: a_pad_o Bit[6:5]: drive_strength 00: 1x 01: 2x 10: 3x 11: 4x Bit[4:3]: Reserved Bit[2]: Disable FSIN input Bit[1]: Disable FREX input Bit[0]: Not used
0x3012	SCCB R12	0x20	RW	Bit[7:0]: sccb_id_r12
0x3013~ 0x3014	NOT USED	–	–	Not Used
0x3015	PUMP CLK DIV	0x00	RW	Bit[7:4]: Npump clock div /1 ~ /15 Bit[3:0]: Ppump clock div /1 ~ /15
0x3016~ 0x3017	NOT USED	–	–	Not Used
0x3018	MIPI SC CTRL	0x32	RW	Bit[7:5]: mipi_lane_mode N+1 lane Bit[4]: mipi_en 0: LVDS enable 1: MIPI enable Bit[3:2]: r_phy_pd_mipi Bit[1]: phy_rst option 1: Reset PHY when rst_sync Bit[0]: lane_dis option 1: Disable lanes when pd_mipi
0x3019	MIPI SC CTRL	0x00	RW	Bit[7:0]: MIPI lane disable
0x301A	CLKRST0	0xF0	RW	Bit[7]: sclk_gt Bit[6]: sclk_stb Bit[5]: sclk_ac Bit[4]: sclk_tc Bit[3]: mipi_phy_rst_o Bit[2]: rst_stb Bit[1]: rst_ac Bit[0]: rst_tc

table 6-2 system control registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x301B	CLKRST1	0xF0	RW	Bit[7]: sclk_blc Bit[6]: sclk_isp Bit[5]: sclk_testmode Bit[4]: sclk_vfifo Bit[3]: rst_blc Bit[2]: rst_isp Bit[1]: rst_testmode Bit[0]: rst_vfifo
0x301C	CLKRST2	0xF0	RW	Bit[7]: Not used Bit[6]: sclk_mipi Bit[5]: sclk_dpcm Bit[4]: sclk_otp Bit[3]: Not used Bit[2]: rst_mipi Bit[1]: rst_dpcm Bit[0]: rst_otp
0x301D	CLKRST3	0xF0	RW	Bit[7]: sclk_asram_tst Bit[6]: sclk_grp Bit[5]: sclk_bist Bit[4]: sclk_aec Bit[3]: rst_asram_tst Bit[2]: rst_grp Bit[1]: rst_bist Bit[0]: rst_aec
0x301E	CLKRST4	0xF0	RW	Bit[7]: sclk_ilpwm Bit[6]: pclk_lvds Bit[5]: pclk_vfifo Bit[4]: pclk_mipi Bit[3]: rst_ilpwm Bit[2]: rst_lvds Bit[1]: Not used Bit[0]: rst_dpcm
0x301F	FREX RST MASK0	0x00	RW	Bit[7]: frex_mask_aec Bit[6]: frex_mask_blc Bit[5]: frex_mask_isp Bit[4]: Not used Bit[3]: frex_mask_mipi Bit[2]: frex_mask_vfifo Bit[1]: frex_mask_testmode Bit[0]: frex_mask_mipi_phy

table 6-2 system control registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x3020	CLOCK SEL	0x93	RW	Bit[7]: CLK switch output Bit[6]: pclk_ratio_exp 1: Exponential pclk_ratio_i to 2^n Bit[5]: yuv_out_en 0: SOC sensor, output RAW data, or RAW sensor 1: SOC sensor, output YUV dat Bit[4]: dvp_sclk_en 1: use pll_sclk_i instead pll_pclk_i for DVP Bit[3]: pclk_sel Bit[2:1]: Not used Bit[0]: sclk2x_sel
0x3021	MISC CTRL	0x03	RW	Bit[7]: Not used Bit[6]: Sleep no latch option 1: No latch Bit[5]: Not used Bit[4]: mipi_ctr_en 0: Disable the function 1: Enable MIPI remote reset and suspend control sc Bit[3]: mipi_rst_sel 0: MIPI remote reset all registers 1: MIPI remote reset all digital module Bit[2]: gpio_pclk_en Bit[1]: frex_ef_sel Bit[0]: cen_global_o
0x3022	MIPI SC CTRL	0x01	RW	Bit[7:4]: Not used Bit[3]: lvds_mode_o Bit[2]: Clock lane 1 disable Bit[1]: Clock lane 0 disable Bit[0]: pd_mipi enable when rst_sync
0x3023	MIPI LPTX SEL	0x00	RW	Bit[7:0]: mipi_lptx_sel[7:0]
0x3024	REG24	0x00	RW	Bit[7:5]: Not used Bit[4]: mipi_lptx_sel_opt Bit[3]: Not used Bit[2]: rst_ana Bit[1:0]: mipi_lptx_cksel
0x302A	SUB ID	–	R	Bit[7:4]: Process Bit[3:0]: Version
0x3030	REG30	0x00	RW	Bit[7:6]: Not used Bit[5]: Sclk inv Bit[4]: Pclk inv Bit[3:0]: Not used

table 6-2 system control registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x3031	REG31	0x0A	RW	Bit[7:5]: Not used Bit[4:0]: mipi_bit_sel 0x8: 8-bit mode 0xA: 10-bit mode 0xC: 12-bit mode Others: Not used
0x3032	REG32	0x80	RW	Bit[7]: pll2_sysclk_sel Bit[6]: asram_clk_sel Bit[5]: array_hskip_man_en Bit[4]: r_rst_otp_sleep_dis Bit[3]: r_rst_ana_sleep_dis Bit[2:0]: array_hskip_man[3:1]
0x3033	REG33	0x24	RW	Bit[7]: array_hskip_man Bit[6]: emb_ana_gain_sel Bit[5]: r_fmt_eof_sel Bit[4]: sync_point_sel Bit[3]: rip_sof_en Bit[2]: r_vln_en_stop Bit[1]: pll_sysclk_sel Bit[0]: mipi_sel_aslp_dis
0x3034	REG34	0x00	RW	Bit[7]: r_bit_shift_clip_en Bit[6:4]: r_bit_shift_mode Bit[3:2]: Not used Bit[1]: bp_half Bit[0]: Not used
0x3035	REG35	0x18	RW	Bit[7:0]: Reserved
0x3036	REG36	0x01	RW	Bit[7:0]: Reserved
0x3037	REG37	0x00	RW	Bit[7:1]: Reserved Bit[0]: r_sid
0x3038	REG38	0x60	RW	Bit[7:0]: Reserved
0x3039	PD_CTRL0	0xF0	RW	Bit[7:6]: Reserved Bit[5]: pd_ana_vbk_src Bit[4]: pd_ana_vbk_syncfifo Bit[3:0]: Reserved
0x303A	PD_CTRL1	0xF0	RW	Bit[7]: pd_ana_vbk_gt Bit[6]: pd_ana_vbk_stb Bit[5]: pd_ana_vbk_ac Bit[4]: pd_ana_vbk_tc Bit[3:0]: Reserved

table 6-2 system control registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x303B	PD_CTRL2	0xF0	RW	Bit[7]: pd_ana_vbk_blc Bit[6]: pd_ana_vbk_isp Bit[5]: pd_ana_vbk_tst Bit[4]: pd_ana_vbk_vfifo Bit[3:0]: Reserved
0x303C	PD_CTRL3	0xFF	RW	Bit[7]: pd_ana_vbk_dvp Bit[6]: pd_ana_vbk_mipi Bit[5]: pd_ana_vbk_cif Bit[4]: pd_ana_vbk_otp Bit[3]: pd_ana_vbk_sclk_core Bit[2]: sclk_core enable Bit[1]: pd_ana_vbk_sclk2x_core Bit[0]: sclk2x_core enable
0x303D	PD_CTRL4	0xF0	RW	Bit[7]: pd_ana_vbk_s2p Bit[6]: pd_ana_vbk_grp Bit[5]: pd_ana_vbk_bist Bit[4]: pd_ana_vbk_aec Bit[3]: rst_pwr_sw Bit[2:0]: Reserved
0x303E	PD_CTRL5	0xFF	RW	Bit[7]: pd_ana_vbk_ilpwm Bit[6]: pd_ana_vbk_mipisc Bit[5]: pd_ana_vbk_pvfifo Bit[4]: pd_ana_vbk_mipi Bit[3]: pd_sys_vbk_npump_clk Bit[2]: npump clk enable Bit[1]: pd_sys_vbk_ppump_clk Bit[0]: Ppump clock enable
0x303F	CTRL3F	0x00	RW	Bit[7:2]: Not used Bit[1]: sccb_id2_nack Bit[0]: sccb_pgm_id_en
0x3040	CTRL00	0xF0	RW	Bit[7]: sclk_isp_fc_en Bit[6]: sclk_fc_en Bit[5]: sclk_tpm_en Bit[4]: sclk_fmt_en Bit[3]: rst_isp_fc_force Bit[2]: rst_fc_force Bit[1]: rst_tpm_force Bit[0]: rst_fmt_force
0x3043	FREX RST MASK1	0xF0	RW	Bit[7]: frex_mask_isp_fc Bit[6]: frex_mask_fc Bit[5]: frex_mask_tpm Bit[4]: frex_mask_fmt Bit[3:0]: Not used

6.3 SCCB control [0x3100 - 0x3107]

table 6-3 SCCB control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3100	SCCB CTRL	0x00	RW	Bit[7:4]: Not used Bit[3]: r_sda_dly_en Bit[2:0]: r_sda_dly
0x3101	SCCB OPT	0x32	RW	Bit[7:6]: Not used Bit[5]: Enable register address translating table Bit[4]: en_ss_addr_inc Bit[3]: r_sda_byp_sync 0: Two clock stage sync for sda_i 1: No sync for sda_i Bit[2]: r_scl_byp_sync 0: Two clock stage sync for scl_i 1: No sync for scl_i Bit[1]: r_msk_glitch Bit[0]: r_msk_stop
0x3102	SCCB FILTER	0x00	RW	Bit[7:4]: r_sda_num Bit[3:0]: r_scl_num
0x3103	SCCB SYSREG	0x00	RW	Bit[7]: Not used Bit[6]: ctrl_rst_mipisc Bit[5]: ctrl_rst_srb Bit[4]: ctrl_rst_sccb_s Bit[3]: ctrl_rst_pon_sccb_s Bit[2]: ctrl_rst_clkmod Bit[1]: ctrl_mipi_phy_rst_o Bit[0]: ctrl_pll_rst_o
0x3104	PWUP DIS	0x01	RW	Bit[7:5]: Not used Bit[4]: r_srb_clk_syn_en Bit[3]: pwup_dis2 Bit[2]: pwup_dis1 Bit[1]: pll_clk_sel Bit[0]: pwup_dis0
0x3105	PADCLK DIV	0x11	RW	Bit[7:6]: Not used Bit[5:0]: padclk_div
0x3106	SRB HOST INPUT DIS	0x11	RW	Bit[7:4]: sclk_div Bit[3]: ctrl_aec_done Bit[2]: ctrl_mipi_host Bit[1]: ctrl_mc_host Bit[0]: ctrl_bist_host

table 6-3 SCCB control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3107	SC_CTRL	0x01	RW	Bit[7]: Reserved Bit[6]: npump_clk_sw Bit[5]: auto_sleep_en Bit[4]: pd_mipi_dis_aslp Bit[3]: pumpclk_cutoff_byp Bit[2]: pclk_cutoff_byp Bit[1]: clk_cutoff_byp Bit[0]: pd_ana_vbk_arb

6.4 group hold control [0x3200 - 0x320F]

table 6-4 group hold control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Group0 Start Address in SRAM Actual Address is {0x3200[5:0], 4'h0}
0x3201	GROUP ADR1	0x08	RW	Group1 Start Address in SRAM Actual Address is {0x3201[5:0], 4'h0}
0x3202	GROUP ADR2	0x10	RW	Group2 Start Address in SRAM Actual Address is {0x3202[5:0], 4'h0}
0x3203	GROUP ADR3	0x18	RW	Group3 Start Address in SRAM Actual Address is {0x3203[5:0], 4'h0}
0x3204	GROUP LEN0	–	R	Length of Group0
0x3205	GROUP LEN1	–	R	Length of Group1
0x3206	GROUP LEN2	–	R	Length of Group2
0x3207	GROUP LEN3	–	R	Length of Group3
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch 1110: Fast group launch Others: Reserved Bit[3:0]: Group ID 0000: Group bank 0 0001: Group bank 1 0010: Group bank 2 0011: Group bank 3 Others: Reserved

table 6-4 group hold control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3209	GROUP0 PERIOD	0x00	RW	Bit[7]: Not used Bit[6:5]: Switch back group Bit[4:0]: Number of frames to stay in group 0
0x320A	GROUP1 PERIOD	0x00	RW	Number of Frames to Stay in Group 1
0x320B	GRP_SW_CTRL	0x11	RW	Bit[7]: auto_sw Bit[6:5]: Not used Bit[4]: frame_cnt_trig Bit[3]: group_switch_repeat Bit[2]: context_en Bit[1:0]: Second group select
0x320C	SRAM TEST	0x02	RW	Bit[7:5]: Not used Bit[4]: Group hold SRAM test enable bit Bit[3:0]: Group hold SRAM RM[3:0]
0x320D	GRP_ACT	–	R	Active Group Indicator
0x320E	FM_CNT_GRP0	–	R	Group 0 Frame Count
0x320F	FM_CNT_GRP1	–	R	Group 1 Frame Count

6.5 MEC/MGC control [0x3500 - 0x3503, 0x3505, 0x3507 - 0x3518]

table 6-5 MEC/MGC control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3500	LONG EXPO	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Long exposure[19:16]
0x3501	LONG EXPO	0x02	RW	Bit[7:0]: Long exposure[15:8]
0x3502	LONG EXPO	0x00	RW	Bit[7:0]: Long exposure[7:0] Low 4 bits are fraction bits. Shall always be 0.

table 6-5 MEC/MGC control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3503	AEC MANUAL	0x00	RW	Bit[7]: priority_6 Bit[6]: Digital fraction gain delay option 0: Delay 1 frame 1: Do not delay 1 frame Bit[5]: Gain change delay option 0: Delay 1 frame 1: Do not delay 1 frame Bit[4]: Gain delay option 0: Delay 1 frame 1: Do not delay 1 frame Bit[3]: gain_prec16_en Bit[2]: Gain manual as sensor gain 0: Input gain as real gain format 1: Input gain as sensor gain format Bit[1]: Exposure delay option (must be 0) 0: Delay 1 frame 1: Not used Bit[0]: Exposure change delay option (must be 0) 0: Delay 1 frame 1: Not used
0x3505	GCVT OPTION	0x80	RW	Gain Conversation Option Bit[7]: DAC fixed gain bit Bit[6]: switch_snr_gain_en Bit[5:4]: Sensor gain fixed bit Bit[3:2]: Sensor gain pregain option (debug only, always set it to 0) Bit[1:0]: Sensor gain option for transferring real gain to sensor gain format
0x3507	GAIN SHIFT	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gain shift option 00: No shift 01: Left shift 1 bit 10: Left shift 2 bits 11: Left shift 3 bits
0x3508	LONG GAIN	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Long gain[12:8]

table 6-5 MEC/MGC control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3509	LONG GAIN	0x80	RW	Bit[7:0]: Long gain[7:0] If 0x3503[2]=0, gain[12:0] is real gain format, where low 7 bits are fraction bits, real_gain = gain[12:0]/128, for example: 0x080 is 1x gain, 0x100 is 2x gain If 0x3503[2]=1, gain[12:0] is sensor gain format, gain[12:8] is coarse gain, 00000: 1x, 00001: 2x, 00011: 4x, 00111: 8x, gain[7] is 1, gain[6:3] is fine gain, gain[2:0] is always 0. For example: 0x080 is 1x gain, 0x180 is 2x gain, 0x380 is 4x gain
0x350A	LONG DIGIGAIN	0x04	RW	Bit[3:0]: Long digital gain[11:8]
0x350B	LONG DIGIGAIN	0x00	RW	Bit[7:0]: Long digital gain[7:0]
0x350C	SHORT GAIN	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Short gain[12:8]
0x350D	SHORT GAIN	0x80	RW	Bit[7:0]: Short gain[7:0]
0x350E	SHORT DIGIGAIN	0x04	RW	Bit[7:0]: Short digital gain[11:4]
0x350F	SHORT DIGIGAIN	0x00	RW	Bit[7:6]: Not used Bit[5:2]: Short digital gain Low 10 bits are fraction bits Bit[1:0]: Reserved
0x3510	SHORT EXPO	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Short exposure[19:16]
0x3511	SHORT EXPO	0x02	RW	Bit[7:0]: Short exposure[15:8]
0x3512	SHORT EXPO	0x00	RW	Bit[7:0]: Short exposure[7:0] Low 4 bits are fraction bits
0x3513	SNR_GAIN_L	–	R	Bit[7:6]: Not used Bit[5:0]: Long sensor gain[13:8]
0x3514	SNR_GAIN_L	–	R	Bit[7:0]: Long sensor gain[7:0]
0x3515	FINE_SNR_GAIN_L	–	R	Bit[7:6]: Not used Bit[5:0]: Long fine sensor gain
0x3516	SNR_GAIN_S	–	R	Bit[7:6]: Not used Bit[5:0]: Short sensor gain[13:8]
0x3517	SNR_GAIN_S	–	R	Bit[7:0]: Short sensor gain[7:0]
0x3518	FINE_SNR_GAIN_S	–	R	Bit[7:6]: Not used Bit[5:0]: Short fine sensor gain

6.6 analog control [0x3600 - 0x36FF]

table 6-6 analog control registers

address	register name	default value	R/W	description
0x3600~ 0x36FF	ANALOG CONTROL	–	–	Analog Control Registers

6.7 array control [0x3700 - 0x37FF]

table 6-7 array control registers

address	register name	default value	R/W	description
0x3700~ 0x37FF	ARRAY CONTROL	–	–	Array Control Registers

6.8 timing control [0x3800 - 0x3848, 0x3861 - 0x3863, 0x3870 - 0x3872]

table 6-8 timing control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x3800	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[15:8] Array horizontal start point high byte
0x3801	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[7:0] Array horizontal start point low byte
0x3802	Y ADDR START	0x00	RW	Bit[7:0]: y_addr_start[15:8] Array vertical start point high byte
0x3803	Y ADDR START	0x0C	RW	Bit[7:0]: y_addr_start[7:0] Array vertical start point low byte
0x3804	X ADDR END	0x0C	RW	Bit[7:0]: x_addr_end[15:8] Array horizontal end point high byte
0x3805	X ADDR END	0xDF	RW	Bit[7:0]: x_addr_end[7:0] Array horizontal end point low byte
0x3806	Y ADDR END	0x09	RW	Bit[7:0]: y_addr_end[11:8] Array vertical end point high byte

table 6-8 timing control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x3807	Y ADDR END	0xA3	RW	Bit[7:0]: y_addr_end[7:0] Array vertical end point low byte
0x3808	X OUTPUT SIZE	0x0C	RW	Bit[7:0]: x_output_size[15:8] ISP horizontal output width high byte
0x3809	X OUTPUT SIZE	0xC0	RW	Bit[7:0]: x_output_size[7:0] ISP horizontal output width low byte
0x380A	Y OUTPUT SIZE	0x09	RW	Bit[7:0]: y_output_size[15:8] ISP vertical output height high byte
0x380B	Y OUTPUT SIZE	0x90	RW	Bit[7:0]: y_output_size[7:0] ISP vertical output height low byte
0x380C	HTS	0x07	RW	Bit[7:0]: HTS[15:8] Total horizontal timing size high byte
0x380D	HTS	0x90	RW	Bit[7:0]: HTS[7:0] Total horizontal timing size low byte
0x380E	VTS	0x09	RW	Bit[7:0]: VTS[15:8] Total vertical timing size high byte
0x380F	VTS	0xB0	RW	Bit[7:0]: VTS[7:0] Total vertical timing size low byte
0x3810	ISP X WIN	0x00	RW	Bit[7:0]: isp_x_win[15:8] ISP horizontal windowing offset high byte
0x3811	ISP X WIN	0x04	RW	Bit[7:0]: isp_x_win[7:0] ISP horizontal windowing offset low byte
0x3812	ISP Y WIN	0x00	RW	Bit[7:0]: isp_y_win[11:8] ISP vertical windowing offset high byte
0x3813	ISP Y WIN	0x02	RW	Bit[7:0]: isp_y_win[7:0] ISP vertical windowing offset low byte
0x3814	X INC ODD	0x01	RW	Bit[7:4]: Not used Bit[3:0]: x_odd_inc
0x3815	X INC EVEN	0x01	RW	Bit[7:4]: Not used Bit[3:0]: x_even_inc
0x3816	VSYNC START	0x00	RW	Bit[7:0]: vsync_start[15:8] VSYNC start point high byte
0x3817	VSYNC START	0x00	RW	Bit[7:0]: vsync_start[7:0] VSYNC start point low byte

table 6-8 timing control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x3818	VSYNC END	0x00	RW	Bit[7:0]: vsync_end[15:8] VSYNC end point high byte
0x3819	VSYNC END	0x00	RW	Bit[7:0]: vsync_end[7:0] VSYNC end point low byte
0x381A	HSYNC FIRST H	0x04	RW	Bit[7:0]: hsync_first[15:8] HSYNC first active row start position high byte
0x381B	HSYNC FIRST L	0x00	RW	Bit[7:0]: hsync_first[7:0] HSYNC first active row start position low byte
0x381C~ 0x381F	NOT USED	–	–	Not Used
0x3820	FORMAT1	0x80	RW	Bit[7]: vsub48_blc Bit[6]: vflip_blc Bit[5:4]: Not used Bit[3]: byp_isp_o Bit[2]: vflip_dig Bit[1]: vflip_arr Bit[0]: hdr_en
0x3821	FORMAT2	0x40	RW	Bit[7]: dig_hbin4 Bit[6]: hsync_en_o Bit[5]: fst_vbin Bit[4]: fst_hbin Bit[3]: isp_hvar2 Bit[2]: Digital horizontal mirror control 0: Mirrored image 1: Normal image Bit[1]: Array horizontal mirror control 0: Mirrored image 1: Normal image Bit[0]: dig_hbin2
0x3822	REG22	0x8C	RW	Bit[7:5]: addr0_num Bit[4:0]: ablc_num
0x3823	REG23	0x08	RW	Bit[7]: ext_vs_re Bit[6]: ext_vs_en Bit[5]: vts_no_latch Bit[4]: init_man Bit[3:0]: Not used
0x3824	CS RST FSIN	0x00	RW	Bit[7:0]: cs_rst_fsin[15:8] CS reset value high byte at vs_ext
0x3825	CS RST FSIN	0x20	RW	Bit[7:0]: cs_rst_fsin[7:0] CS reset value low byte at vs_ext

table 6-8 timing control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x3826	R RST FSIN	0x00	RW	Bit[7:0]: r_rst_fsin[15:8] R reset value high byte at vs_ext
0x3827	R RST FSIN	0x08	RW	Bit[7:0]: r_rst_fsin[7:0] R reset value low byte at vs_ext
0x3828	REG28	0x00	RW	Bit[7]: ext_hs_re Bit[6]: ext_hs_en Bit[5]: asp_start_sel 0: Use sync output 1: Use sensor output Bit[4]: hts_inc_en Bit[3]: r_gate_vs_b Bit[2]: VSYNC polarity Bit[1:0]: href_w
0x3829	NOT USED	–	–	Not Used
0x382A	Y INC ODD	0x01	RW	Bit[7:4]: Not used Bit[3:0]: y_odd_inc
0x382B	Y INC EVEN	0x01	RW	Bit[7:4]: Not used Bit[3:0]: y_even_inc
0x382C	BLC COL ST L	0x01	RW	Bit[7:0]: blc_col_st_l[7:0] Left black column start address
0x382D	BLC COL END L	0x00	RW	Bit[7:0]: blc_col_end_l[7:0] Left black column end address
0x382E	BLC COL ST R	0x00	RW	Bit[7]: Not used Bit[6:0]: blc_col_st_r[6:0] Right black column start address
0x382F	BLC COL END R	0x00	RW	Bit[7]: Not used Bit[6:0]: blc_col_end_r[6:0] Right black column end address
0x3830	BLC NUM OPTION	0x04	RW	Bit[7:5]: ablc_adj Bit[4:0]: ablc_use_num
0x3831	BLC NUM MAN	0x00	RW	Bit[7:6]: Not used Bit[5]: man_blc_num_sel Bit[4:0]: man_blc_num
0x3832	FRACTION HTS	0x00	RW	Bit[7:0]: fraction_hts[15:8]
0x3833	FRACTION HTS	0x00	RW	Bit[7:0]: fraction_hts[7:0]
0x3834	EXT DIV FACTORS	0x01	RW	Bit[7:4]: ext_vs_div Bit[3:0]: ext_hs_div

table 6-8 timing control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x3835	GROUP WRITE OPTION	0x01	RW	Bit[7]: Not used Bit[6:5]: ext_vsync_sel Bit[4]: r_grp_wr_pt_sel 0: Gain trigger 1: End of frame Bit[3:0]: Group write adjust number
0x3836	ZLINE NUM OPTION	0x02	RW	Bit[7:5]: Not used Bit[4:0]: zline_use_num
0x3837	REG37	0x00	RW	Bit[7:5]: Not used Bit[4]: vts_add_dis Bit[3:0]: cexp_gt_vts offs
0x3838	RGBC	0x10	RW	Bit[7]: Not used Bit[6:5]: rgbc_hbin_opt Bit[4]: bypass_hsub Bit[3]: rgb_only Bit[2]: w_only Bit[1]: rgbc_hbin Bit[0]: rgbc_hsub
0x3839~ 0x383F	NOT USED	–	–	Not Used
0x3840	GRP WR MAN	–	RW	Bit[7:0]: grp_wr_man Manual group command
0x3841~ 0x3847	NOT USED	–	–	Not Used
0x3848	OTP_DPC_RST	0x01	RW	Bit[7]: r_rst_otp_dpc_en Bit[6:5]: Not used Bit[4:0]: r_otp_dpc_rst_r
0x3861	PD1	0x80	RW	Bit[7:5]: r_zline_row_rst[2:0] Bit[4:2]: r_grp_adj[10:8] Bit[1:0]: r_zline_num[9:8]
0x3862	PD2	0x00	RW	Bit[7:0]: r_zline_num[7:0]
0x3863	PD3	0x02	RW	Bit[7:0]: r_grp_adj[7:0]
0x3870	ROW COUNTER LATCH	–	R	Bit[7:0]: row_counter_latch Read this register will trigger a latch of row counter
0x3871	ROW COUNTER H	–	R	Bit[7:0]: row_counter[15:8]
0x3872	ROW COUNTER L	–	R	Bit[7:0]: row_counter[7:0]

6.9 LPM control [0x3C80 - 0x3C87]

table 6-9 power saving mode control registers

address	register name	default value	R/W	description
0x3C80	LPM REG0	0x00	RW	Bit[7:4]: Reserved Bit[3]: psv_auto_on_dis 0: PSV mode auto enable if VTS > threshold 1: Disable PSV auto-on mode, only depending on 0x3C80[2] Bit[2]: psv_mode_en Bit[1]: Reserved Bit[0]: psv_mode 0: Keep sclk on, frame timing based on sclk 1: Shut off sclk at blanking, frame timing switch to pad_clk domain
0x3C81	LPM REG1	0x00	RW	Bit[7:4]: Reserved Bit[3]: tc_sof_sync_en Bit[2]: vblkp_sync_dis Bit[1:0]: blank_retime_opt
0x3C82	LPM REG2	0x00	RW	Bit[7:0]: hts_pad_clk[15:8]
0x3C83	LPM REG3	0xB1	RW	Bit[7:0]: hts_pad_clk[7:0]
0x3C84	LPM REG4	0x00	RW	Bit[7:0]: cs_cnt_initial[15:8]
0x3C85	LPM REG5	0x0F	RW	Bit[7:0]: cs_cnt_initial[7:0]
0x3C86	LPM REG6	0x08	RW	Bit[7:0]: stream_st_offset
0x3C87	LPM REG7	0x08	RW	Bit[7:0]: pchg_st_offset

6.10 power control [0x3CC0 - 0x3CC8]

table 6-10 power control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3CC0	PSRR_SW0	0x13	RW	Bit[7:6]: Not used Bit[5]: psrr_on_man Bit[4]: psrr_on_man_en Bit[3]: psrr_dis Bit[2:0]: detect_wid_opt

table 6-10 power control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3CC1	PSRR_SW1	0x10	RW	Bit[7:0]: threshold_gap
0x3CC2	PSRR_SW2	0x00	RW	Bit[7:0]: pwr_detect[15:8]
0x3CC3	PSRR_SW3	0x00	RW	Bit[7:0]: pwr_detect[7:0]
0x3CC4	PSRR_SW4	0x07	RW	Bit[7:0]: psrr_sw_threshold[15:8]
0x3CC5	PSRR_SW5	0xF0	RW	Bit[7:0]: psrr_sw_threshold[7:0]
0x3CC6	PSRR_SW6	–	R	Bit[7]: psrr_on Bit[6]: pwr_detect_en Bit[5]: vblank_i Bit[4:0]: Not used
0x3CC7	PSRR_SW7	–	R	Bit[7:0]: Noise_cnt[15:8]
0x3CC8	PSRR_SW8	–	R	Bit[7:0]: Noise_cnt[7:0]

6.11 OTP_SC control [0x3D80 - 0x3D91]

table 6-11 OTP_SC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3D80	OTP_PROGRAM_CTRL	–	RW	Bit[7]: OTP_wr_busy (read only) Bit[6:1]: Not used Bit[0]: OTP_program_enable (write only)
0x3D81	OTP_LOA_CTRL	–	RW	Bit[7]: OTP_rd_busy (read only) Bit[6]: Not used Bit[5]: OTP_bist_error (read only) Bit[4]: OTP_bist_done (read only) Bit[3:1]: Not used Bit[0]: OTP_load_enable (read/write)
0x3D82	OTP_PGM_PULSE	0x55	RW	Program Strobe Pulse Width Unit: 8 × system clock period
0x3D83	OTP_LOAD_PULSE	0x08	RW	Load Strobe Pulse Width Unit: system clock period
0x3D84	OTP_MODE_CTRL	0x00	RW	Bit[7]: Program disable 1: Disable Bit[6]: Mode select 0: Auto mode 1: Manual mode Bit[5:0]: Debug mode

table 6-11 OTP_SC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D85	OTP_REG85	0x13	RW	Bit[7:6]: Debug mode Bit[5]: OTP_bist_select 0: Compare with SRAM 1: Compare with zero Bit[4]: OTP_bist_enable Bit[3]: Debug mode Bit[2]: OTP power up load data enable Bit[1]: OTP power up load setting enable Bit[0]: OTP write register load setting enable
0x3D86	SRAM_TEST_ SIGNALS	0x02	RW	Bit[7:3]: Debug mode Bit[2]: r_test Bit[1:0]: r_rm
0x3D87	OTP_PS2CS	0x0A	RW	OTP PS to CSB Delay Unit: System Clock Period
0x3D88	OTP_START_ ADDRESS	0x00	RW	OTP Start High Address for Manual Mode
0x3D89	OTP_START_ ADDRESS	0x00	RW	OTP Start Low Address for Manual Mode
0x3D8A	OTP_EN_ADDRESS	0x00	RW	OTP End High Address for Manual Mode
0x3D8B	OTP_END_ ADDRESS	0x00	RW	OTP End Low Address for Manual Mode
0x3D8C	OTP_SETTING_STT _ADDRESS	0x00	RW	OTP Start High Address for Load Setting
0x3D8D	OTP_SETTING_STT _ADDRESS	0x00	RW	OTP Start Low Address for Load Setting
0x3D8E	OTP_BIST_ERR_ ADDRESS	–	R	OTP Check Error Address High
0x3D8F	OTP_BIT_ERR_ ADDRESS	–	R	OTP Check Error Address Low
0x3D90	OTP_CTRL	0x14	RW	Bit[7:0]: Gap between strobe pulse when programming
0x3D91	OTP_CTRL	0x06	RW	Bit[7:0]: Gap between strobe pulse when loading

6.12 PSRAM control [0x3F00 - 0x3F0F]

table 6-12 PSRAM control registers

address	register name	default value	R/W	description
0x3F00~ 0x3F0F	PSRAM CONTROL	–	–	PSRAM Control Registers

6.13 BLC control [0x4000 - 0x4027, 0x4030 - 0x4050, 0x4060 - 0x4067]

table 6-13 BLC control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x4000	BLC CTRL 00	0x03	RW	Bit[7:5]: r_num_add_o Bit[4]: r_black_line_sel_o Bit[3]: Target adjust disable Use offset to adjust target 0: Enable 1: Disable Bit[2]: Compensation enable Adjust on offset due to gain change 0: Disable 1: Enable Bit[1]: Dither_en 1 bit dithering 0: Disable 1: Enable Bit[0]: Median_en Median filter function enable
0x4001	BLC CTRL 01	0xE0	RW	Bit[7]: r_gain_trig_beh_o Bit[6]: r_format_trig_beh_o Bit[5]: Kocef manual enable Bit[4]: Zero line out enable Bit[3]: Black line out enable Bit[2]: Not used Bit[1:0]: Bypass mode
0x4002	BLC CTRL 02	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Blacklevel target[9:8] High 2 bits
0x4003	BLC CTRL 03	0x10	RW	Bit[7:0]: Blacklevel target[7:0] Low 8 bits

table 6-13 BLC control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x4004	BLC CTRL 04	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Horizontal win start[11:8] Horizontal win start high 4 bits
0x4005	BLC CTRL 05	0x02	RW	Bit[7:0]: Horizontal win start[7:0] Horizontal win start low 8 bits
0x4006	BLC CTRL 06	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Horizontal win pad[11:8] Horizontal win pad high 4 bits
0x4007	BLC CTRL 07	0x02	RW	Bit[7:0]: Horizontal win pad[7:0] Horizontal win pad low 8 bits
0x4008	BLC CTRL 08	0x02	RW	Bit[7:0]: Black line start line
0x4009	BLC CTRL 09	0x05	RW	Bit[7:0]: Black line end line
0x400A	BLC CTRL 0A	0x02	RW	Bit[7:0]: Offset trigger threshold[15:8] Offset limit threshold high 8 bits
0x400B	BLC CTRL 0B	0x00	RW	Bit[7:0]: Offset trigger threshold[7:0] Offset limit threshold low 8 bits
0x400C	BLC CTRL 0C	0x00	RW	Bit[7:0]: CVDN black lines start
0x400D	BLC CTRL 0D	0x00	RW	Bit[7:0]: CVDN black lines end
0x400E	BLC CTRL 0E	0x00	RW	Bit[7]: r_zero_ln_sel Bit[6:0]: r_mf_th_o
0x400F	BLC CTRL 0F	0x80	RW	Bit[7]: r_exp_chg_trig_en_o Bit[6]: r_set_zb_o Bit[5:4]: r_manu_cvdn_out_en Bit[3]: r_v15_one-channel_en Bit[2]: r_en_adp_k_o Bit[1]: r_dc_offset_mode_o Bit[0]: r_compute_offset_v15_o
0x4010	BLC CTRL 10	0xF0	RW	Bit[7]: Offset trigger enable Bit[6]: Gain change trigger enable Bit[5]: Format change trigger enable Bit[4]: Reset trigger enable Bit[3]: Manual average enable Bit[2]: Manual trigger Bit[1]: Freeze enable Bit[0]: Offset always update

table 6-13 BLC control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x4011	BLC CTRL 11	0xFF	RW	Bit[7]: offset_cmp_man_en Bit[6]: Offset trigger multiframe enable Bit[5]: Format trigger multiframe enable Bit[4]: Gain trigger multiframe enable Bit[3]: Reset trigger multiframe enable Bit[2]: Offset trigger multiframe mode Bit[1]: Format trigger multiframe mode Bit[0]: Gain trigger multiframe mode
0x4012	BLC CTRL 12	0x08	RW	Bit[7:6]: Not used Bit[5:0]: Reset trigger frame num
0x4013	BLC CTRL 13	0x02	RW	Bit[7:6]: Not used Bit[5:0]: Format trigger frame num
0x4014	BLC CTRL 14	0x02	RW	Bit[7:6]: Not used Bit[5:0]: Gain trigger frame num
0x4015	BLC CTRL 15	0x02	RW	Bit[7:6]: Not used Bit[5:0]: Offset trigger frame num
0x4016	BLC CTRL 16	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Offset trigger threshold[9:8] Offset trigger threshold high 2 bits
0x4017	BLC CTRL 17	0x04	RW	Bit[7:0]: Offset trigger threshold[7:0] Offset trigger threshold low 8 bits
0x4018~ 0x401F	NOT USED	–	–	Not Used
0x4020	BLC CTRL 20	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Offset compensation k000
0x4021	BLC CTRL 21	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Offset compensation k001
0x4022	BLC CTRL 22	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Offset compensation k010
0x4023	BLC CTRL 23	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Offset compensation k011
0x4024	BLC CTRL 24	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Offset compensation th000
0x4025	BLC CTRL 25	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Offset compensation th001
0x4026	BLC CTRL 26	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Offset compensation th010
0x4027	BLC CTRL 27	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Offset compensation th011

table 6-13 BLC control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x4030	BLC CTRL 30	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Offset man 000[9:8]
0x4031	BLC CTRL 31	0x00	RW	Bit[7:0]: Offset man 000[7:0]
0x4032	BLC CTRL 32	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Offset man 001[9:8]
0x4033	BLC CTRL 33	0x00	RW	Bit[7:0]: Offset man 001[7:0]
0x4034	BLC CTRL 34	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Offset man 010[9:8]
0x4035	BLC CTRL 35	0x00	RW	Bit[7:0]: Offset man 010[7:0]
0x4036	BLC CTRL 36	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Offset man 011[9:8]
0x4037	BLC CTRL 37	0x00	RW	Bit[7:0]: Offset man 011[7:0]
0x4038	BLC CTRL 38	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Offset man 100[9:8]
0x4039	BLC CTRL 39	0x00	RW	Bit[7:0]: Offset man 100[7:0]
0x403A	BLC CTRL 3A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Offset man 101[9:8]
0x403B	BLC CTRL 3B	0x00	RW	Bit[7:0]: Offset man 101[7:0]
0x403C	BLC CTRL 3C	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Offset man 110[9:8]
0x403D	BLC CTRL 3D	0x00	RW	Bit[7:0]: Offset man 110[7:0]
0x403E	BLC CTRL 3E	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Offset man 111[9:8]
0x403F	BLC CTRL 3F	0x00	RW	Bit[7:0]: Offset man 111[7:0]
0x4040	BLC CTRL 40	0x00	RW	Bit[7:0]: Zline start
0x4041	BLC CTRL 41	0x01	RW	Bit[7:0]: Zline end
0x4042	BLC CTRL 42	0x00	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_b_man[9:8]
0x4043	BLC CTRL 43	0x80	RW	Bit[7:0]: kcoef_b_man[7:0]
0x4044	BLC CTRL 44	0x00	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_gb_man[9:8]
0x4045	BLC CTRL 45	0x80	RW	Bit[7:0]: kcoef_gb_man[7:0]
0x4046	BLC CTRL 46	0x00	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_gr_man[9:8]

table 6-13 BLC control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x4047	BLC CTRL 47	0x80	RW	Bit[7:0]: kcoef_gr_man[7:0]
0x4048	BLC CTRL 48	0x00	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_r_man[9:8]
0x4049	BLC CTRL 49	0x80	RW	Bit[7:0]: kcoef_r_man[7:0]
0x404A	BLC CTRL 4A	0x30	RW	Bit[7:0]: dc_th_1
0x404B	BLC CTRL 4B	0x18	RW	Bit[7:0]: dc_th_1
0x404C	BLC CTRL 4C	0x60	RW	Bit[7]: Not used Bit[6]: rst_trig_opt Bit[5:0]: Average weight
0x404D	BLC CTRL 4D	0x00	RW	Bit[7:2]: Not used Bit[1:0]: rnd_gain_th[9:8]
0x404E	BLC CTRL 4E	0x00	RW	Bit[7:0]: rnf_gain_th[7:0]
0x404F	BLC CTRL 4F	0x00	RW	Bit[7:0]: dc_th_1_s
0x4050	BLC CTRL 50	0x00	RW	Bit[7:0]: dc_th_2_s
0x4060	BLC CTRL 60	–	R	Bit[7:2]: Not used Bit[1:0]: BLC_offset000[9:8]
0x4061	BLC CTRL 61	–	R	Bit[7:0]: BLC_offset000[7:0]
0x4062	BLC CTRL 62	–	R	Bit[7:2]: Not used Bit[1:0]: BLC_offset001[9:8]
0x4063	BLC CTRL 63	–	R	Bit[7:0]: BLC_offset001[7:0]
0x4064	BLC CTRL 64	–	R	Bit[7:2]: Not used Bit[1:0]: BLC_offset010[9:8]
0x4065	BLC CTRL 65	–	R	Bit[7:0]: BLC_offset010[7:0]
0x4066	BLC CTRL 66	–	R	Bit[7:2]: Not used Bit[1:0]: BLC_offset011[9:8]
0x4067	BLC CTRL 67	–	R	Bit[7:0]: BLC_offset011[7:0]

6.14 FC control [0x4200 - 0x4203]

table 6-14 FC control registers

address	register name	default value	R/W	description
0x4200	R0	0x08	RW	Bit[7:4]: Not used Bit[3]: sof_after_line0 Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fcnt_reset
0x4201	R1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_on_number
0x4202	R2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_off_number
0x4203	R3	0x80	RW	Bit[7]: zero_line_mask_dis Bit[6]: blue_mask_dis Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

6.15 format control [0x4300 - 0x4317, 0x4320 - 0x4329]

table 6-15 format control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x4300	CLIP MAX HI	0xFF	RW	Bit[7:0]: clip_max_hi
0x4301	CLIP MIN HI	0x00	RW	Bit[7:0]: clip_min_hi
0x4302	CLIP LO	0x0F	RW	Bit[7:4]: clip_min_lo Bit[3:0]: clip_max_lo
0x4303	FORMAT CTRL3	0x00	RW	Bit[7]: r_inc_en Bit[6]: r_pat_inv Bit[5]: r_pad_lsb Bit[4]: r_bar_mux Bit[3]: r_bar_en Bit[2]: r_bit_tst_en Bit[1]: r_tst_bit8 Bit[0]: r_bit_tst_md

table 6-15 format control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x4304	FORMAT CTRL4	0x08	RW	Bit[7]: Not used Bit[6:4]: data_bit_swap Bit[3]: tst_full_win Bit[2:0]: bar_pad
0x4305	PAD LOW1	0x40	RW	Bit[7:6]: Pad99 Bit[5:4]: Pad66 Bit[3:2]: Pad33 Bit[1:0]: Pad00
0x4306	PAD LOW2	0x0E	RW	Bit[7:4]: Not used Bit[3:2]: Padff Bit[1:0]: Padcc
0x4307	EMBED CTRL	0x30	RW	Bit[7:2]: Not used Bit[1]: dpc_threshold_opt 0: For black pixel 1: For white pixel Bit[0]: embedded_en
0x4308	TST X START HIGH	0x00	RW	Bit[7:5]: Not used Bit[4:0]: tst_x_start[12:8]
0x4309	TST X START LOW	0x00	RW	Bit[7:1]: tst_x_start[7:1] Bit[0]: Not used
0x430A	TST Y START HIGH	0x00	RW	Bit[7:5]: Not used Bit[4:0]: tst_y_start[12:8]
0x430B	TST Y START LOW	0x00	RW	Bit[7:1]: tst_y_start[7:1] Bit[0]: Not used
0x430C	TST WIDTH HIGH	0x00	RW	Bit[7:4]: Not used Bit[3:0]: tst_width[11:8]
0x430D	TST WIDTH LOW	0x00	RW	Bit[7:0]: tst_width[7:0]
0x430E	TST HIGHT HIGH	0x00	RW	Bit[7:4]: Not used Bit[3:0]: tst_hight[11:8]
0x430F	TST HIGHT LOW	0x00	RW	Bit[7:0]: tst_hight[7:0]
0x4311	CTRL11	0x04	RW	Bit[7:0]: r_hsyvsy_neg_width[15:8]
0x4312	CTRL12	0x00	RW	Bit[7:0]: r_hsyvsy_neg_width[7:0]
0x4313	CTRL13	0x00	RW	Bit[7:5]: Not used Bit[4]: r_vsync_pol Bit[3:2]: r_vsyncout_sel Bit[1]: r_vsync3_mod Bit[0]: r_vsync2_mod
0x4314	CTRL14	0x00	RW	Bit[7:0]: r_seof_vsync_delay[23:16]
0x4315	CTRL15	0x00	RW	Bit[7:0]: r_seof_vsync_delay[15:8]

table 6-15 format control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x4316	CTRL16	0x00	RW	Bit[7:1]: r_seof_vsync_delay[7:1] Bit[0]: r_dpcm_en
0x4317	CTRL17	0x00	RW	Bit[7:1]: Not used Bit[0]: r_dpcm_en
0x4320	TEST PATTERN CTRL	0x80	RW	Bit[7:6]: pixel_order 00: GR/BG 01: RG/GB 10: BG/GR 11: GB/RG Bit[5]: byte_swap Bit[4]: bit_reverse Bit[3:2]: Not used Bit[1]: solid_color_en Bit[0]: pn31_enable
0x4321	PN31 CTRL	0x00	RW	Bit[7:4]: Not used Bit[3]: PN31 LSB first enable Bit[2]: PN31 reset by SOF enable Bit[1]: PN31 reset by HREF enable Bit[0]: PN9 enable
0x4322	SOLID COLOR B	0x00	RW	Bit[7:2]: Not used Bit[1:0]: solid_color_b[9:8]
0x4323	SOLID COLOR B	0x00	RW	Bit[7:0]: solid_color_b[7:0]
0x4324	SOLID COLOR GB	0x00	RW	Bit[7:2]: Not used Bit[1:0]: solid_color_gb[9:8]
0x4325	SOLID COLOR GB	0x00	RW	Bit[7:0]: solid_color_gb[7:0]
0x4326	SOLID COLOR R	0x00	RW	Bit[7:2]: Not used Bit[1:0]: solid_color_r[9:8]
0x4327	SOLID COLOR R	0x00	RW	Bit[7:0]: solid_color_r[7:0]
0x4328	SOLID COLOR GR	0x00	RW	Bit[7:2]: Not used Bit[1:0]: solid_color_gr[9:8]
0x4329	SOLID COLOR GR	0x00	RW	Bit[7:0]: solid_color_gr[7:0]

6.16 CADC sync control [0x4500 - 0x4505]

table 6-16 CADC sync control registers

address	register name	default value	R/W	description
0x4500	CTRL	0x68	RW	Bit[7:3]: FIFO read delay Bit[2]: Rblue rev Bit[1]: Not used Bit[0]: srclk_inv
0x4501	R1	0xC4	RW	Bit[7:2]: Not used Bit[1]: Mirror manual enable Bit[0]: Mirror manual
0x4502	R2	0x40	RW	Bit[7]: r_weight_fix Bit[6:5]: r_weight Bit[4]: r_hskip Bit[3:2]: r_hbin_opt Bit[1]: r_skip_opt Bit[0]: Swap SRAM input data from D0~D3 to D3~D0
0x4503	R3	0x00	RW	Bit[7:0]: r_data_offs
0x4504	R4	0x04	RW	Bit[7]: r_sync_mirror_re Bit[6]: r_sync_flip_re Bit[5]: r_sync_mirror_opt Bit[4]: r_sync_flip_opt Bit[3]: r_sync_data_sw Bit[2]: r_byp_rblue Bit[1:0]: Not used
0x4505	R5	0x8F	RW	Bit[7]: r_sync_avg Bit[6]: r_sync_byp Bit[5]: r_sync_sram_test Bit[4]: Not used Bit[3:0]: r_sync_sram_RM

6.17 VFIFO control [0x4600 - 0x4604]

table 6-17 VFIFO control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4600	R VFIFO READ START	0x00	RW	Bit[7:0]: r_vfifo_read_start[15:8] read_start size high byte

table 6-17 VFIFO control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4601	R VFIFO READ START	0x10	RW	Bit[7:0]: r_vfifo_read_start[7:0] read_start size low byte
0x4602	R2	0x02	RW	Bit[7:4]: r_rm Bit[3]: r_test1 Bit[2]: Not used Bit[1]: Frame reset enable Bit[0]: RAM bypass enable
0x4603	R3	–	R	Bit[7:4]: Not used Bit[3]: ram_full Bit[2]: ram_empty Bit[1]: fo_full Bit[0]: fo_empty
0x4604	R4	0x00	RW	Bit[7:2]: Not used Bit[1:0]: SRAM sclk select option

6.18 MIPI control [0x4800 - 0x4833, 0x4836 - 0x483D, 0x484A - 0x4853]

table 6-18 MIPI control registers (sheet 1 of 11)

address	register name	default value	R/W	description
0x4800	MIPI CTRL00	0x4C	RW	Bit[7]: Not used Bit[6]: gate_sc_vblk_en 1: Enable gate clock lane only when vblanking Bit[5]: gate_sc_en 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: line_sync_en 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3]: fst_stby_ctr 0: Software standby enter at v_blk 1: Software standby enter at l_blk Bit[2:0]: Not used

table 6-18 MIPI control registers (sheet 2 of 11)

address	register name	default value	R/W	description
0x4801	MIPI CTRL01	0x00	RW	Bit[7]: Not used Bit[6]: spkt_dt_sel 1: Use dt_spkt as short packet data Bit[5]: first_bit Change clk_lane first bit 0: Output 0x05 1: Output 0xAA Bit[4:2]: Not used Bit[1]: LPX_select for pclk domain 0: Auto calculate t_lpx_p, unit pclk2x cycle 1: Use lpx_p_min[7:0] Bit[0]: Not used
0x4802	MIPI CTRL02	0x00	RW	Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail_min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]

table 6-18 MIPI control registers (sheet 3 of 11)

address	register name	default value	R/W	description
0x4803	MIPI CTRL03	0x00	RW	Bit[7:4]: Not used Bit[3]: manu_ofset_o t_period manual offset SMIA Bit[2]: r_manu_half2one t_period half to 1 SMIA Bit[1]: clk_pre_half Bit[0]: hs_pre_half
0x4804	MIPI CTRL04	0x04	RW	Bit[7:4]: man_lane_num Bit[3]: lane_num_manual_enable Bit[2]: lane4_6b_en 1: Support 4, 7, 8-lane 6-bit Bit[1]: Vsub select 1: Valid in front 0: Valid in behind Bit[0]: vfifo_8x
0x4805	MIPI CTRL05	0x00	RW	Bit[7:4]: Not used Bit[3]: lpda_retim_manu_o Bit[2]: lpda_retim_sel_o 1: Manual Bit[1]: lpck_retim_manu_o Bit[0]: lpck_retim_sel_o 1: Manual
0x4806	MIPI CTRL06	0x10	RW	Bit[7]: Not used Bit[6]: Suspend latch at horizontal blanking Bit[5]: Suspend latch at vertical blanking Bit[4]: pu_mark_en_o Power up mark1 enable Bit[3]: mipi_remot_rst Bit[2]: mipi_susp Bit[1]: smia_lane_ch_en Bit[0]: tx_lsb_first 0: High bit first 1: Low power transmit low bit first
0x4807	MIPI CTRL07	0x03	RW	Bit[7:4]: Not used Bit[3:0]: sw_t_lpx ul_tx T_lpx
0x4808	MIPI CTRL08	0x0A	RW	Bit[7:0]: wkup_dly Mark1 wakeup delay/2^10
0x4809~ 0x480F	NOT USED	–	–	Not Used
0x4810	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[15:8] High byte of max frame counter of frame sync short packet

table 6-18 MIPI control registers (sheet 4 of 11)

address	register name	default value	R/W	description
0x4811	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[7:0] Low byte of max frame counter of frame sync short packet
0x4812	NOT USED	–	–	Not Used
0x4813	MIPI CTRL13	0x00	RW	Bit[7:3]: Not used Bit[2]: vc_sel Bit[1:0]: VC ID
0x4814	MIPI CTRL14	0x2A	RW	Bit[7]: Not used Bit[6]: lpkt_dt_sel 0: Use mipi_dt 1: Use dt_man_o as long packet data Bit[5:0]: dt_man Manual data type
0x4815	MIPI CTRL15	0x00	RW	Bit[7]: Not used Bit[6]: pclk_inv 0: Using falling edge of mipi_pclk_o to generate MIPI bus to PHY 1: Using rising edge of mipi_pclk_o to generate MIPI bus to PHY Bit[5:0]: manu_dt_short Manual type for short packet
0x4816	EMB DT	0x53	RW	Bit[7:6]: Not used Bit[5:0]: emb_dt Manual set embedded data type
0x4817	YUV420 FUN	0x00	RW	Bit[7:2]: Not used Bit[1]: yuv420_2x YUV420 2x in odd line, lcnt[0]=1 Bit[0]: yuv420_en
0x4818	HS ZERO MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_zero_min[9:8] High byte of minimum value of hs_zero, unit ns
0x4819	HS ZERO MIN	0x70	RW	Bit[7:0]: hs_zero_min[7:0] Low byte of minimum value of hs_zero hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	HS TRAIL MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_trail_min[9:8] High byte of minimum value of hs_trail, unit ns

table 6-18 MIPI control registers (sheet 5 of 11)

address	register name	default value	R/W	description
0x481B	HS TRAIL MIN	0x3C	RW	Bit[7:0]: hs_trail_min[7:0] Low byte of minimum value of hs_trail hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	CLK ZERO MIN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: clk_zero_min[9:8] High byte of minimum value of clk_zero, unit ns
0x481D	CLK ZERO MIN	0x2C	RW	Bit[7:0]: clk_zero_min[7:0] Low byte of minimum value of clk_zero clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o
0x481E	CLK PREPARE MAX	0x5F	RW	Bit[7:0]: clk_prepare_max[7:0] Maximum value of clk_prepare, unit ns
0x481F	CLK PREPARE MIN	0x26	RW	Bit[7:0]: clk_prepare_min[7:0] Minimum value of clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	CLK POST MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_post_min[9:8] High byte of minimum value of clk_post, unit ns
0x4821	CLK POST MIN	0x3C	RW	Bit[7:0]: clk_post_min[7:0] Low byte of minimum value of clk_post clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o
0x4822	CLK TRAIL MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_trail_min[9:8] High byte of minimum value of clk_trail, unit ns
0x4823	CLK TRAIL MIN	0x3C	RW	Bit[7:0]: clk_trail_min[7:0] Low byte of minimum value of clk_trail clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	LPX P MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: lpx_p_min[9:8] High byte of minimum value of lpx_p, unit ns

table 6-18 MIPI control registers (sheet 6 of 11)

address	register name	default value	R/W	description
0x4825	LPX P MIN	0x32	RW	Bit[7:0]: lpx_p_min[7:0] Low byte of minimum value of lpx_p lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x4826	HS PREPARE MIN	0x32	RW	Bit[7:0]: hs_prepare_min[7:0] Minimum value of hs_prepare, unit ns
0x4827	HS PREPARE MAX	0x55	RW	Bit[7:0]: hs_prepare_max[7:0] Maximum value of hs_prepare hs_prepare_real = hs_prepare_max_o + Tui*ui_hs_prepare_max_o
0x4828	HS EXIT MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_exit_min[9:8] High byte of minimum value of hs_exit, unit ns
0x4829	HS EXIT MIN	0x64	RW	Bit[7:0]: hs_exit_min[7:0] Low byte of minimum value of hs_exit hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	UI HS ZERO MIN	0x06	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_zero_min[5:0] Minimum UI value of hs_zero, unit UI
0x482B	UI HS TRAIL MIN	0x04	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_trail_min[5:0] Minimum UI value of hs_trail, unit UI
0x482C	UI CLK ZERO MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_zero_min[5:0] Minimum UI value of clk_zero, unit UI
0x482D	UI CLK PREPARE	0x00	RW	Bit[7:4]: ui_clk_prepare_max Maximum UI value of clk_prepare, unit UI Bit[3:0]: ui_clk_prepare_min Minimum UI value of clk_prepare, unit UI
0x482E	UI CLK POST MIN	0x34	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_post_min[5:0] Minimum UI value of clk_post, unit UI
0x482F	UI CLK TRAIL MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_trail_min[5:0] Minimum UI value of clk_trail, unit UI

table 6-18 MIPI control registers (sheet 7 of 11)

address	register name	default value	R/W	description
0x4830	UI LPX P MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_lpx_p_min[5:0] Minimum UI value of lpx_p (pclk2x domain), unit UI
0x4831	UI HS PREPARE	0x64	RW	Bit[7:4]: ui_hs_prepare_max Maximum UI value of hs_prepare, unit UI Bit[3:0]: ui_hs_prepare_min Minimum UI value of hs_prepare, unit UI
0x4832	UI HS EXIT MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_exit_min[5:0] Minimum UI value of hs_exit, unit UI
0x4833	MIPI PKT STAR SIZE	0x08	RW	Bit[7:6]: Not used Bit[5:0]: r_rdy_mark
0x4836	GLB MODE SEL	0x00	RW	Bit[7:1]: Not used Bit[0]: smia_cal_en 0: Use period to calculate 1: Use SMIA bitrate to calculate
0x4837	PCLK PERIOD	0x16	RW	Bit[7:0]: pclk_period[7:0] Period of pclk2x, pclk_div=1, and 1 bit decimal
0x4838	MIPI LP GPIO0	0x00	RW	Bit[7]: lp_sel0 0: Auto generate mipi_lp_dir0_o 1: Use lp_dir_man0 to be mipi_lp_dir0_o Bit[6]: lp_dir_man0 0: Input 1: Output Bit[5]: lp_p0_o Bit[4]: lp_n0_o Bit[3]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 to be mipi_lp_dir1_o Bit[2]: lp_dir_man1 0: Input 1: Output Bit[1]: p_p1_o Bit[0]: lp_n1_o

table 6-18 MIPI control registers (sheet 8 of 11)

address	register name	default value	R/W	description
0x4839	MIPI LP GPIO1	0x00	RW	Bit[7]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 to be mipi_lp_dir2_o Bit[6]: lp_dir_man2 0: Input 1: Output Bit[5]: lp_p2_o Bit[4]: lp_n2_o Bit[3]: lp_sel3 0: Auto generate mipi_lp_dir3_o 1: Use lp_dir_man3 to be mipi_lp_dir3_o Bit[2]: lp_dir_man3 0: Input 1: Output Bit[1]: lp_p3_o Bit[0]: lp_n3_o
0x483A	MIPI LP GPIO2	0x00	RW	Bit[7]: lp_sel4 0: Auto generate mipi_lp_dir4_o 1: Use lp_dir_man4 to be mipi_lp_dir4_o Bit[6]: lp_dir_man4 0: Input 1: Output Bit[5]: lp_p4_o Bit[4]: lp_n4_o Bit[3]: lp_sel5 0: Auto generate mipi_lp_dir5_o 1: Use lp_dir_man5 to be mipi_lp_dir5_o Bit[2]: lp_dir_man5 0: Input 1: Output Bit[1]: lp_p5_o Bit[0]: lp_n5_o

table 6-18 MIPI control registers (sheet 9 of 11)

address	register name	default value	R/W	description
0x483B	MIPI LP GPIO3	0x00	RW	Bit[7]: lp_sel6 0: Auto generate mipi_lp_dir6_o 1: Use lp_dir_man6 to be mipi_lp_dir6_o Bit[6]: lp_dir_man6 0: Input 1: Output Bit[5]: lp_p6_o Bit[4]: lp_n6_o Bit[3]: lp_sel7 0: Auto generate mipi_lp_dir7_o 1: Use lp_dir_man7 to be mipi_lp_dir7_o Bit[2]: lp_dir_man7 0: Input 1: Output Bit[1]: lp_p7_o Bit[0]: lp_n7_o
0x483C	MIPI CTRL3C	0x02	RW	Bit[7:4]: Not used Bit[3:0]: t_clk_pre Unit pclk2x cycle
0x483D	MIPI LP GPIO4	0x00	RW	Bit[7]: lp_ck_sel0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[6]: lp_ck_dir_man0 0: Input 1: Output Bit[5]: lp_ck_p0_o Bit[4]: lp_ck_n0_o Bit[3]: lp_ck_sel1 0: Auto generate mipi_ck_lp_dir1_o 1: Use lp_ck_dir_man1 to be mipi_ck_lp_dir1_o Bit[2]: lp_ck_dir_man1 0: Input 1: Output Bit[1]: lp_ck_p1_o Bit[0]: lp_ck_n1_o

table 6-18 MIPI control registers (sheet 10 of 11)

address	register name	default value	R/W	description
0x484A	SEL MIPI CTRL4A	0x27	RW	Bit[7:6]: Not used Bit[5]: slp_lp_pon_man_o Set for power up Bit[4]: slp_lp_pon_da Bit[3]: slp_lp_pon_ck Bit[2]: mipi_slp_man_st MIPI bus status manual control enable in sleep mode Bit[1]: clk_lane_state Bit[0]: data_lane_state
0x484B	SMIA OPTION	0x07	RW	Bit[7:3]: Not used Bit[2]: line_st_sel_o 0: Line starts after HREF 1: Line starts after fifo_st Bit[1]: clk_start_sel_o 0: Clock starts after SOF 1: Clock starts after reset Bit[0]: sof_sel_o 0: Frame starts after HREF 1: Frame starts after SOF
0x484C	SEL MIPI CTRL4C	0x03	RW	Bit[7:3]: Not used Bit[6]: smia_fcnt_i select Bit[5]: prbs_enable Bit[4]: hs_test_only MIPI high speed only test mode enable Bit[3]: set_frame_cnt_0 Set frame count to inactive mode (keep 0) Bit[2:0]: Not used
0x484D	TEST PATTEN DATA	0xB6	RW	Bit[7:0]: test_patten_data[7:0] Data lane test pattern register
0x484E	FE DLY	0x10	RW	Bit[7:0]: r_fe_dly_o Last packet to frame end delay / 2
0x484F	TEST PATTEN CK DATA	0x55	RW	Bit[7:2]: Not used Bit[1:0]: clk_test_patten_reg
0x4850	LANE SEL01	0x12	RW	Bit[7]: Not used Bit[6:4]: lane1_sel Bit[3]: Not used Bit[2:0]: lane0_sel
0x4851	LANE SEL23	0x03	RW	Bit[7]: Not used Bit[6:4]: lane3_sel Bit[3]: Not used Bit[2:0]: lane2_sel

table 6-18 MIPI control registers (sheet 11 of 11)

address	register name	default value	R/W	description
0x4852	LANE SEL45	0x54	RW	Bit[7]: Not used Bit[6:4]: lane5_sel Bit[3]: Not used Bit[2:0]: lane4_sel
0x4853	LANE SEL67	0x76	RW	Bit[7]: Not used Bit[6:4]: lane7_sel Bit[3]: Not used Bit[2:0]: lane6_sel

6.19 ISPFC control [0x4900 - 0x4903]

table 6-19 ISPFC control registers

address	register name	default value	R/W	description
0x4900	R0	0x00	RW	Bit[7:4]: Not used Bit[3]: sof_after_line0 Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fcnt_reset
0x4901	R1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_on_number
0x4902	R2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_off_number
0x4903	R3	0x00	RW	Bit[7]: zero_line_mask_dis Bit[6]: blue_mask_dis Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

6.20 ISP control [0x5000 - 0x5009, 0x500E - 0x5026, 0x502D - 0x5030]

table 6-20 ISP control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x77	RW	Bit[7]: blc_hdr_en Bit[6]: dcblc_en Bit[5]: lenc_en Bit[4]: awb_gain_en Bit[3]: r_long_short_rvs Bit[2]: bc_en Bit[1]: wc_en Bit[0]: blc_en
0x5001	ISP CTRL01	0x0A	RW	Bit[7]: blc_vsync_sel Bit[6]: pre_vsync_sel Bit[5]: r_rlong_sel Bit[4]: lenc_real_gain_rvs Bit[3]: otp_option_en Bit[2]: Not used Bit[1]: awbm_bias_on Bit[0]: latch_en
0x5002	ISP CTRL02	0x20	RW	Bit[7:6]: dig_gain_blc Bit[5]: bufctrl_en Bit[4:2]: ln_delay Bit[1]: man_noswap_en Bit[0]: blc_hdr_ls_rvs
0x5003	ISP CTRL03	0xC8	RW	Bit[7]: lenc_bias_on Bit[6:5]: lenc_px_order_man Bit[4]: lenc_px_order_man_en Bit[3]: insize_auto Bit[2]: dpc_hdr_ls_rvs Bit[1]: gfirst_rvs Bit[0]: rblue_rvs
0x5004	ISP CTRL04	0x00	RW	Bit[7:5]: Not used Bit[4]: r_dig_sel_from_reg Bit[3]: Not used Bit[2]: blc_mirror_opt Bit[1]: dig_gain_en Bit[0]: lenc_decomp_en
0x5005	ISP CTRL05	0x00	RW	Bit[7]: isp_bypass_mode Bit[6]: Not used Bit[5]: bypass_isp Bit[4:0]: Not used
0x5006	ISP CTRL06	0x00	RW	Bit[7:4]: Not used Bit[3:0]: hsize_in_r[11:8]
0x5007	ISP CTRL07	0x00	RW	Bit[7:0]: hsize_in_r[7:0]

table 6-20 ISP control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5008	ISP CTRL08	0x00	RW	Bit[7:4]: Not used Bit[3:0]: vsize_in_r[11:8]
0x5009	ISP CTRL09	0x00	RW	Bit[7:0]: vsize_in_r[7:0]
0x500E	ISP CTRL0E	0x00	RW	Bit[7:4]: Not used Bit[3:0]: dpc_hsize_in[11:8]
0x500F	ISP CTRL0F	0x00	RW	Bit[7:0]: dpc_hsize_in[7:0]
0x5010	ISP CTRL10	0x00	RW	Bit[7:4]: Not used Bit[3:0]: dpc_vsize_in[11:8]
0x5011	ISP CTRL11	0x00	RW	Bit[7:0]: dpc_vsize_in[7:0]
0x5012	ISP CTRL12	0x00	RW	Bit[7:4]: Not used Bit[3:0]: dig_gain_l[11:8]
0x5013	ISP CTRL13	0x00	RW	Bit[7:0]: dig_gain_l[7:0]
0x5014	ISP CTRL14	0x00	RW	Bit[7:4]: Not used Bit[3:0]: dig_gain_s[11:8]
0x5015	ISP CTRL15	0x00	RW	Bit[7:0]: dig_gain_s[7:0]
0x5016	ISP CTRL16	0x00	RW	Bit[7]: r_cen_sel Bit[6]: r_cen Bit[5:2]: Not used Bit[1]: dpc_size_man
0x5017	ISP CTRL17	0x00	RW	Bit[7:6]: Not used Bit[5]: sram_test_dpc2 Bit[4]: sram_test_dpc1 Bit[3]: Not used Bit[1]: sram_rme_dpc2 Bit[0]: sram_rme_dpc1
0x5018	ISP CTRL18	0x00	RW	Bit[7:4]: sram_rm_dpc2 Bit[3:0]: sram_rm_dpc1
0x5019	ISP CTRL19	0x04	RW	Bit[7:4]: Not used Bit[3:0]: mwb_r_gain_man_l[11:8]
0x501A	ISP CTRL1A	0x00	RW	Bit[7:0]: mwb_r_gain_man_l[7:0]
0x501B	ISP CTRL1B	0x04	RW	Bit[7:4]: Not used Bit[3:0]: mwb_g_gain_man_l[11:8]
0x501C	ISP CTRL1C	0x00	RW	Bit[7:0]: mwb_g_gain_man_l[7:0]
0x501D	ISP CTRL1D	0x04	RW	Bit[7:4]: Not used Bit[3:0]: mwb_b_gain_man_l[11:8]
0x501E	ISP CTRL1E	0x00	RW	Bit[7:0]: mwb_b_gain_man_l[7:0]

table 6-20 ISP control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x501F	ISP CTRL1F	0x04	RW	Bit[7:4]: Not used Bit[3:0]: mwb_r_gain_man_s[11:8]
0x5020	ISP CTRL20	0x00	RW	Bit[7:0]: mwb_r_gain_man_s[7:0]
0x5021	ISP CTRL21	0x04	RW	Bit[7:4]: Not used Bit[3:0]: mwb_g_gain_man_s[11:8]
0x5022	ISP CTRL22	0x00	RW	Bit[7:0]: mwb_g_gain_man_s[7:0]
0x5023	ISP CTRL23	0x04	RW	Bit[7:4]: Not used Bit[3:0]: mwb_b_gain_man_s[11:8]
0x5024	ISP CTRL24	0x00	RW	Bit[7:0]: mwb_b_gain_man_s[7:0]
0x5025	ISP CTRL25	0x18	RW	Bit[7:6]: Not used Bit[5]: r_embed_line_en Bit[4]: Not used Bit[3]: r_isp_raw_en Bit[2:0]: r_win_y_offset_adjust
0x5026	ISP CTRL26	0x2A	RW	Bit[7:6]: Not used Bit[5]: r_dmy_auto_en Bit[4]: r_bias_man_en Bit[3]: vsync_puls Bit[2]: Not used Bit[1:0]: px_order_man
0x502D	ISP CTRL2D	0x00	RW	Bit[7:0]: snr_bias_man
0x502E	ISP CTRL2E	0x00	RW	Bit[7]: blc_px_man_en Bit[6:5]: blc_px_man Bit[4]: r_blc_rblue_man_en Bit[3]: r_blc_rblue_man Bit[2]: pre_px_man_en Bit[1]: r_zero_rblue_man_en Bit[0]: r_zero_rblue_man
0x502F	ISP CTRL2F	0x00	RW	Bit[7]: dpc_data_switch Bit[6]: dpc_px_man_en Bit[5:4]: dpc_px_man Bit[3]: Not used Bit[2]: r_awb_px_man_en Bit[1:0]: r_awb_px_man
0x5030	ISP CTRL30	0x41	RW	Bit[7:6]: isp_sof_sel Bit[1:0]: isp_eof_sel

6.21 DPC long exposure control [0x5780 - 0x57B2]

table 6-21 DPC long exposure control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5780	DPC_CTRL0	0x14	RW	Bit[7:6]: Not used Bit[5]: Tail enable Bit[4]: Saturate cross-cluster enable Bit[3]: 3x3 cluster enable Bit[2]: Cross-cluster enable Bit[1]: General tail enable Bit[0]: Manual mode enable
0x5781	DPC_CTRL1	0x0F	RW	Bit[7:4]: Saturate Bit[3]: Different channel white pixel connection enable Bit[2]: Different channel black pixel connection enable Bit[1]: Same channel white pixel connection enable Bit[0]: Same channel black pixel connection enable
0x5782	DPC_CTRL2	0x44	RW	Bit[7:4]: Status threshold step Bit[3:0]: White threshold list0
0x5783	DPC_CTRL3	0x02	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list1
0x5784	DPC_CTRL4	0x01	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list2
0x5785	DPC_CTRL5	0x01	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list3
0x5786	DPC_CTRL6	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Adaptive pattern thresholds
0x5787	DPC_CTRL7	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Adaptive pattern step
0x5788	DPC_CTRL8	0x08	RW	Bit[7:4]: Not used Bit[3:0]: More connection case thresholds
0x5789	DPC_CTRL9	0x0F	RW	Bit[7:0]: DPC level list0
0x578A	DPC_CTRL10	0xFD	RW	Bit[7:0]: DPC level list1
0x578B	DPC_CTRL11	0xF5	RW	Bit[7:0]: DPC level list2
0x578C	DPC_CTRL12	0xF5	RW	Bit[7:0]: DPC level list3
0x578D	DPC_CTRL13	0x03	RW	Bit[7]: Not used Bit[6:0]: Gain list0

table 6-21 DPC long exposure control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x578E	DPC_CTRL14	0x0F	RW	Bit[7]: Not used Bit[6:0]: Gain list1
0x578F	DPC_CTRL15	0x3F	RW	Bit[7]: Not used Bit[6:0]: Gain list2
0x5790	DPC_CTRL16	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Matching thresholds
0x5791	DPC_CTRL17	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Status thresholds
0x5792	DPC_CTRL18	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Threshold ratio
0x5793	DPC_CTRL19	0x52	RW	Bit[7:6]: vnum_list1 Bit[5:4]: vnum_list0 Bit[3:2]: Not used Bit[1]: v153_en Bit[0]: Clip interpolate G enable
0x5794	DPC_CTRL20	0xA3	RW	Bit[7:6]: vnum_list3 Bit[5:4]: vnum_list2 Bit[3:2]: Not used Bit[1:0]: Edge option
0x5795	DPC_CTRL21	0x12	RW	Bit[7:6]: Not used Bit[5]: pd_man_inc_en Bit[4]: pd_pixel_en_l Bit[3:0]: pd_y
0x5796	DPC_CTRL22	0x20	RW	Bit[7:6]: Not used Bit[5:0]: pd_cycle_x
0x5797	DPC_CTRL23	0x20	RW	Bit[7:6]: Not used Bit[5:0]: pd_cycle_y
0x5798	DPC_CTRL24	0x2A	RW	Bit[7:4]: pd_x1 Bit[3:0]: pd_x2
0x5799	DPC_CTRL25	0x6E	RW	Bit[7:4]: pd_x3 Bit[3:0]: pd_x4
0x579A	DPC_CTRL26	0x00	RW	Bit[7:2]: Not used Bit[1:0]: win_start_x[9:8]
0x579B	DPC_CTRL27	0x40	RW	Bit[7:0]: win_start_x[7:0]
0x579C	DPC_CTRL28	0x00	RW	Bit[7:2]: Not used Bit[1:0]: win_start_y[9:8]
0x579D	DPC_CTRL29	0x40	RW	Bit[7:0]: win_start_y[7:0]
0x579E	DPC_CTRL30	0x0C	RW	Bit[7:2]: Not used Bit[3:0]: win_width[11:8]

table 6-21 DPC long exposure control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x579F	DPC_CTRL31	0x80	RW	Bit[7:0]: win_width[7:0]
0x57A0	DPC_CTRL32	0x0B	RW	Bit[7:4]: Not used Bit[3:0]: win_hight[11:8]
0x57A1	DPC_CTRL33	0x40	RW	Bit[7:0]: win_hight[7:0]
0x57A2	DPC_CTRL34	0x00	RW	Bit[7:0]: x_offset[15:8]
0x57A3	DPC_CTRL35	0x20	RW	Bit[7:0]: x_offset[7:0]
0x57A4	DPC_CTRL36	0x00	RW	Bit[7:0]: y_offset[15:8]
0x57A5	DPC_CTRL37	0x20	RW	Bit[7:0]: y_offset[7:0]
0x57A6	DPC_CTRL38	0x03	RW	Bit[7:4]: Not used Bit[3:0]: x_odd_inc
0x57A7	DPC_CTRL39	0x01	RW	Bit[7:4]: Not used Bit[3:0]: x_even_inc
0x57A8	DPC_CTRL40	0x03	RW	Bit[7:4]: Not used Bit[3:0]: y_odd_inc
0x57A9	DPC_CTRL41	0x01	RW	Bit[7:4]: Not used Bit[3:0]: y_even_inc
0x57AC	BLACK THRESHOLDS	–	R	Bit[7]: Not used Bit[6:0]: Black thresholds
0x57AD	WHITE THRESHOLDS	–	R	Bit[7:5]: Not used Bit[4:0]: White thresholds
0x57AE	THRESHOLD 1	–	R	Bit[7:5]: Not used Bit[4:0]: Threshold 1
0x57AF	THRESHOLD 2	–	R	Bit[7:6]: Not used Bit[5:0]: Threshold 2
0x57B0	THRESHOLD 3	–	R	Bit[7]: Not used Bit[6:0]: Threshold 3
0x57B1	THRESHOLD 4	–	R	Bit[7:5]: Not used Bit[4:0]: Threshold 4
0x57B2	LEVEL	–	R	Bit[7:4]: Not used Bit[3:0]: Level

6.22 DPC short exposure control [0x5800 - 0x5815, 0x582C - 0x5832]

table 6-22 DPC short exposure control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5800	DPC_CTRL0	0x14	RW	Bit[7:6]: Not used Bit[5]: Tail enable Bit[4]: Saturate cross-cluster enable Bit[3]: 3x3 cluster enable Bit[2]: Cross-cluster enable Bit[1]: General tail enable Bit[0]: Manual mode enable
0x5801	DPC_CTRL1	0x0F	RW	Bit[7:4]: Saturate Bit[3]: Different channel white pixel connection enable Bit[2]: Different channel black pixel connection enable Bit[1]: Same channel white pixel connection enable Bit[0]: Same channel black pixel connection enable
0x5802	DPC_CTRL2	0x44	RW	Bit[7:4]: Status threshold step Bit[3:0]: White threshold list0
0x5803	DPC_CTRL3	0x02	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list1
0x5804	DPC_CTRL4	0x01	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list2
0x5805	DPC_CTRL5	0x01	RW	Bit[7:4]: Not used Bit[3:0]: White threshold list3
0x5806	DPC_CTRL6	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Adaptive pattern thresholds
0x5807	DPC_CTRL7	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Adaptive pattern step
0x5808	DPC_CTRL8	0x08	RW	Bit[7:4]: Not used Bit[3:0]: More connection case thresholds
0x5809	DPC_CTRL9	0x0F	RW	Bit[7:0]: DPC level list0
0x580A	DPC_CTRL10	0xFD	RW	Bit[7:0]: DPC level list1
0x580B	DPC_CTRL11	0xF5	RW	Bit[7:0]: DPC level list2
0x580C	DPC_CTRL12	0xF5	RW	Bit[7:0]: DPC level list3
0x580D	DPC_CTRL13	0x03	RW	Bit[7]: Not used Bit[6:0]: Gain list0

table 6-22 DPC short exposure control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x580E	DPC_CTRL14	0x0F	RW	Bit[7]: Not used Bit[6:0]: Gain list1
0x580F	DPC_CTRL15	0x3F	RW	Bit[7]: Not used Bit[6:0]: Gain list2
0x5810	DPC_CTRL16	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Matching thresholds
0x5811	DPC_CTRL17	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Status thresholds
0x5812	DPC_CTRL18	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Threshold ratio
0x5813	DPC_CTRL19	0x52	RW	Bit[7:6]: vnum_list1 Bit[5:4]: vnum_list0 Bit[3:2]: Not used Bit[1]: v153_en Bit[0]: Clip interpolate G enable
0x5814	DPC_CTRL20	0xA3	RW	Bit[7:6]: vnum_list3 Bit[5:4]: vnum_list2 Bit[3:2]: Not used Bit[1:0]: edge option
0x5815	DPC_CTRL21	0x12	RW	Bit[7:5]: Not used Bit[4]: pd_pixel_en Bit[3:0]: Not used
0x582C	DPC_CTRL23	–	R	Bit[7]: Not used Bit[6:0]: Black thresholds
0x582D	DPC_CTRL24	–	R	Bit[7:5]: Not used Bit[4:0]: White thresholds
0x582E	DPC_CTRL25	–	R	Bit[7:5]: Not used Bit[4:0]: Threshold 1
0x582F	DPC_CTRL26	–	R	Bit[7:6]: Not used Bit[5:0]: Threshold 2
0x5830	DPC_CTRL27	–	R	Bit[7]: Not used Bit[6:0]: Threshold 3
0x5831	DPC_CTRL28	–	R	Bit[7:5]: Not used Bit[4:0]: threshold 4
0x5832	DPC_CTRL29	–	R	Bit[7:4]: Not used Bit[3:0]: Level

6.23 LENC control [0x5900 - 0x59FF]

table 6-23 LENC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5900	LENC G00	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Control point G00 for luminance compensation
0x5901	LENC G01	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Control point G01 for luminance compensation
0x5902	LENC G02	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Control point G02 for luminance compensation
0x5903	LENC G03	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Control point G03 for luminance compensation
0x5904	LENC G04	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Control point G04 for luminance compensation
0x5905	LENC G05	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Control point G05 for luminance compensation
0x5906	LENC G10	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Control point G10 for luminance compensation
0x5907	LENC G11	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Control point G11 for luminance compensation
0x5908	LENC G12	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Control point G12 for luminance compensation
0x5909~ 0x594E	LENC G13~ LENC G96	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Control point G13~G54 for luminance compensation
0x594F	LENC G97	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Control point G55 for luminance compensation
0x5950	LENC B00	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point B00 for blue channel compensation

table 6-23 LENC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5951	LENC B01	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point B01 for blue channel compensation
0x5952	LENC B02	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point B02 for blue channel compensation
0x5953	LENC B03	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point B03 for blue channel compensation
0x5954	LENC B04	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point B04 for blue channel compensation
0x5955	LENC B05	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point B05 for blue channel compensation
0x5956	LENC B10	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point B10 for blue channel compensation
0x5957	LENC B11	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point B11 for blue channel compensation
0x5958	LENC B12	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point B12 for blue channel compensation
0x5959~ 0x599E	LENC B13~LENC B96	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point B13~B54 for blue channel compensation
0x599F	LENC B97	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point B55 for blue channel compensation
0x59A0	LENC R00	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point R00 for red channel compensation
0x59A1	LENC R01	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point R01 for red channel compensation
0x59A2	LENC R02	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point R02 for red channel compensation

table 6-23 LENC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x59A3	LENC R03	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point R03 for red channel compensation
0x59A4	LENC R04	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point R04 for red channel compensation
0x59A5	LENC R05	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point R05 for red channel compensation
0x59A6	LENC R10	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point R10 for red channel compensation
0x59A7	LENC R11	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point R11 for red channel compensation
0x59A8	LENC R12	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point R12 for red channel compensation
0x59A9~ 0x59EE	LENC R13~LENC R96	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point R13~R54 for red channel compensation
0x59EF	LENC R97	0x80	RW	Bit[7:5]: Not used Bit[4:0]: Control point R55 for red channel compensation
0x59F0	LENC MAXGAIN	0x60	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will be the minimum value (min LENC gain). Register value is 16 times sensor gain
0x59F1	LENC MINGAIN	0x40	RW	Bit[7:0]: If AutoLensSwitchEnable is true and sensor gain is larger than this threshold, luminance compensation amplitude will start to decrease; otherwise, the amplitude will not change. Register value is 16 times sensor gain.
0x59F2	LENC MAXQ	0x40	RW	Bit[7]: Not used Bit[6:0]: This value indicates the minimum amplitude which luminance channel compensates when AutoLensSwitchEnable is true. Value should be in the range [0~64]

table 6-23 LENC control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x59F3	LENC MINQ	0x18	RW	Bit[7]: Not used Bit[6:0]: Minq
0x59F4	LENC CTRL	0x36	RW	Bit[7:6]: Not used Bit[5]: Add BLC target after applying compensation Bit[4]: Enable BLC target for LENC 0: Disable BLC target 1: Enable BLC target Bit[3]: Br2xmode Bit[2]: autoq_en Bit[1]: dither_en Bit[0]: g2xgain_en
0x59F5	LENC HSCALE	0x02	RW	Bit[7:5]: Not used Bit[4:0]: HScale[12:8] For horizontal gain calculation, this value indicates the step between two connected horizontal pixels, where HScale = 4*2^18 / image width
0x59F6	LENC HSCALE	0x7C	RW	Bit[7:0]: HScale[7:0]
0x59F7	LENC VSCALE	0x01	RW	Bit[7:5]: Not used Bit[4:0]: VScale[12:8] For vertical gain calculation, this value indicates the step between two connected vertical pixels, where VScale = 4*2^17 / image height
0x59F8	LENC VSCALE	0x40	RW	Bit[7:0]: VScale[7:0]
0x59F9	LENC DECOMP ADDR	0x00	RW	Bit[7:0]: LENC decompression start address[15:8]
0x59FA	LENC DECOMP ADDR	0x00	RW	Bit[7:0]: LENC decompression start address[7:0]
0x59FB	RO_INFO_SEL	0x00	RW	Bit[7:0]: ro_info select
0x59FC	LENC YOFFSET	–	R	Bit[7:0]: Input sensor vertical offset[7:0]
0x59FD	LENC INPUT	–	R	Bit[7:6]: Not used Bit[5]: Input sensor flip Bit[4]: Input sensor mirror Bit[3:2]: Input sensor Y skip Bit[1:0]: Input sensor X skip
0x59FE	LENC OVERFLOW	–	R	Bit[7:2]: Not used Bit[1]: Vertical overflow for debug Bit[0]: Horizontal overflow for debug
0x59FF	LENC QVALUE	–	R	Bit[7]: Not used Bit[6:0]: Real amplitude Q value

6.24 WINC control [0x5A00 - 0x5A0C]

table 6-24 WINC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5A00	WINC CTRL00	0x00	RW	Bit[7:4]: Not used Bit[3:0]: x_start_offset[11:8] Start address in horizontal
0x5A01	WINC CTRL01	0x00	RW	Bit[7:0]: x_start_offset[7:0]
0x5A02	WINC CTRL02	0x00	RW	Bit[7:4]: Not used Bit[3:0]: y_start_offset[11:8] Start address in vertical
0x5A03	WINC CTRL03	0x00	RW	Bit[7:0]: y_start_offset[7:0]
0x5A04	WINC CTRL04	0x0C	RW	Bit[7:4]: Not used Bit[3:0]: window_width[11:8] Select whole zone width
0x5A05	WINC CTRL05	0xE0	RW	Bit[7:0]: window_width[7:0] Select whole zone width
0x5A06	WINC CTRL06	0x09	RW	Bit[7:4]: Not used Bit[3:0]: window_height[11:8] Select whole zone height
0x5A07	WINC CTRL07	0xB0	RW	Bit[7:0]: window_height[7:0] Select whole zone height
0x5A08	WINC CTRL08	0x06	RW	Bit[7:4]: Reserved Bit[3]: Window valid select option (for debug) 0: Select new valid_1d 1: Select original valid_1d Bit[2]: Select embedded line flag 0: Select first line as embedded flag 1: Select last line as embedded flag Bit[1]: Window enable option 0: Disable window after last valid line 1: Get enable from register Bit[0]: Manual window enable 0: Window size from window top 1: Window size from 0x5A00 to 0x5A07
0x5A09	WINC RO09	–	R	Bit[7:4]: Not used Bit[3:0]: Pixel count[11:8] for debug
0x5A0A	WINC RO0A	–	R	Bit[7:0]: Pixel count[7:0] for debug

table 6-24 WINC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5A0B	WINC RO0B	–	R	Bit[7:4]: Not used Bit[3:0]: Line count[11:8] for debug
0x5A0C	WINC RO0C	–	R	Bit[7:0]: Line count[7:0] for debug

6.25 OTP control [0x5B00 - 0x5B0D, 0x5B10 - 0x5B23]

table 6-25 OTP control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5B00	OTP CTRL00	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Memory start address[9:8]
0x5B01	OTP CTRL01	0x00	RW	Bit[7:0]: Memory start address[7:0]
0x5B02	OTP CTRL02	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Memory end address[9:8]
0x5B03	OTP CTRL03	0xFF	RW	Bit[7:0]: Memory end address[7:0]
0x5B04	OTP CTRL04	0x42	RW	Bit[7]: Select xy_end signal for debug 0: xy_end keep 0 1: xy_end keep 1 after last cluster is read out Bit[6]: VSYNC reset enable 0: Do not use VSYNC to reset 3 enable signals 1: Use VSYNC to reset 3 enable signals to fix a bug Bit[5]: Threshold function enable 0: Disable recover threshold in register 0x5B09 (can recover black cluster) 1: Enable recover threshold in register 0x5B09 (can not recover black cluster) Bit[4]: Manual increase step enable Bit[3]: Disable mirror and flip Bit[2]: Disable OTP offset Bit[1]: Mirror option enable Bit[0]: Disable binning mode

table 6-25 OTP control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5B05	OTP CTRL05	0x6C	RW	Bit[7]: Not used Bit[6:5]: Recover method select 00: Left 1 neighbor pixel (on same channel) 01: Minimum of left 2 neighbor pixels 10: Average of left and right 1 neighbor pixel 11: Maximum between minimum of left 2 neighbor pixels and minimum of right 2 neighbor pixels Bit[4]: Use fixed pattern to recover cluster Bit[3]: Fixed pattern mode 0: Use 0x00 to recover cluster 1: Use 0x3FF to recover cluster Bit[2]: Flip option enable Bit[1]: Sensor exposure constrain enable Bit[0]: Sensor gain constrain enable
0x5B06	OTP CTRL06	0x00	RW	Bit[7]: Not used Bit[6:5]: Constrain exposure threshold[9:8] Bit[4:0]: Not used
0x5B07	OTP CTRL07	0x00	RW	Bit[7:0]: Constrain exposure threshold[7:0] Disable OTP function when sensor exposure is smaller than constrain exposure threshold
0x5B08	OTP CTRL08	0x07	RW	Bit[7:6]: Not used Bit[5:0]: Constrain gain threshold Disable OTP function when sensor gain is smaller than constrain gain threshold
0x5B09	OTP CTRL09	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Recover threshold Recover when high 8-bits of recovered data is bigger than original one by this threshold
0x5B0A	OTP CTRL0A	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual horizontal even increase step
0x5B0B	OTP CTRL0B	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual horizontal odd increase step
0x5B0C	OTP CTRL0C	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual vertical even increase step
0x5B0D	OTP CTRL0D	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual vertical odd increase step

table 6-25 OTP control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5B10	OTP RO10	–	R	Bit[7:4]: Not used Bit[3:0]: Horizontal offset[11:8]
0x5B11	OTP RO11	–	R	Bit[7:0]: Horizontal offset[7:0]
0x5B12	OTP RO12	–	R	Bit[7:4]: Not used Bit[3:0]: Vertical offset[11:8]
0x5B13	OTP RO13	–	R	Bit[7:0]: Vertical offset[7:0]
0x5B14	OTP RO14	–	R	Bit[7:5]: Not used Bit[4:0]: Horizontal even increase step
0x5B15	OTP RO15	–	R	Bit[7:5]: Not used Bit[4:0]: Horizontal odd increase step
0x5B16	OTP RO16	–	R	Bit[7:5]: Not used Bit[4:0]: Vertical even increase step
0x5B17	OTP RO17	–	R	Bit[7:5]: Not used Bit[4:0]: Vertical odd increase step
0x5B18~ 0x5B1F	NOT USED	–	–	Not Used
0x5B20	OTP CTRL20	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual X offset[11:8]
0x5B21	OTP CTRL21	0x00	RW	Bit[7:0]: Manual X offset[7:0]
0x5B22	OTP CTRL22	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual Y offset[11:8]
0x5B23	OTP CTRL23	0x00	RW	Bit[7:0]: Manual Y offset[7:0]

6.26 pre_DSP control [0x5E00 - 0x5E2E]

table 6-26 pre_DSP control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5E00	PRE CTRL00	0x00	RW	Bit[7]: Test pattern enable Bit[6]: Rolling bar function enable Bit[5]: Transparent enable Bit[4]: Square mode 0: Color square 1: Black-white square Bit[3:2]: Color bar style 00: Standard color bar 01: Top-bottom darker color bar 10: Right-left darker color bar 11: Bottom-top darker color bar Bit[1:0]: Test pattern mode 00: Color bar 01: Random data 10: Square 11: Black image
0x5E01	PRE CTRL01	0x41	RW	Bit[7]: Reserved Bit[6]: Window cut enable Bit[5]: two_lsb_0_en Set lowest two bits to 0 Bit[4]: Same seed enable Reset seed to 0x5E01[3:0] each frame Bit[3:0]: Random seed Seed used in generating random data
0x5E02	PRE CTRL02	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Line number interrupt[11:8]
0x5E03	PRE CTRL03	0x01	RW	Bit[7:0]: Line number interrupt[7:0]
0x5E04~ 0x5E07	RSVD	–	–	Reserved
0x5E08	PRE CTRL08	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Horizontal manual offset[11:8]
0x5E09	PRE CTRL09	0x00	RW	Bit[7:0]: Horizontal manual offset[7:0]
0x5E0A	PRE CTRL0A	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Vertical manual offset[11:8]
0x5E0B	PRE CTRL0B	0x00	RW	Bit[7:0]: Vertical manual offset[7:0]
0x5E0C	PRE RO0C	–	R	Bit[7:4]: Reserved Bit[3:0]: Input image pixel number[11:8]
0x5E0D	PRE RO0D	–	R	Bit[7:0]: Input image pixel number[7:0]

table 6-26 pre_DSP control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5E0E	PRE RO0E	–	R	Bit[7:4]: Reserved Bit[3:0]: Input image line number[11:8]
0x5E0F	PRE RO0F	–	R	Bit[7:0]: Input image line number[7:0]
0x5E10	PRE CTRL10	0x3C	RW	Bit[7]: Window X offset option Bit[6]: Window Y offset option Bit[5]: Take first pixel in same position with no mirror image enable Bit[4]: Take first pixel in same position with no flip image enable Bit[3]: Mirror option from window 0: First pixel is Gb or R with window output 1: First pixel is B or Gr with window output Bit[2]: Flip option from window 0: First line is GR with window output 1: First line is BG with window output Bit[1]: Offset manual enable Bit[0]: Reserved
0x5E11	PRE CTRL11	0x00	RW	Bit[7]: Manual clock/valid ratio enable Bit[6:4]: Manual dummy line number Bit[3]: Reduce HREF low length by half Bit[2:0]: Manual clock/valid ratio for dummy line
0x5E12	PRE RO12	–	R	Bit[7:0]: HREF blank length for dummy line[15:8]
0x5E13	PRE RO13	–	R	Bit[7:0]: HREF blank length for dummy line[7:0]
0x5E14	PRE RO14	–	R	Bit[7:0]: HREF length for dummy line[15:8]
0x5E15	PRE RO15	–	R	Bit[7:0]: HREF length for dummy line[7:0]
0x5E16	PRE RO16	–	R	Bit[7:5]: Reserved Bit[4]: Dummy error indicating signal Bit[3]: Reserved Bit[2:0]: Dummy line clock ratio output
0x5E17	PRE RO17	–	R	Bit[7:4]: Horizontal odd increase step Bit[3:0]: Vertical odd increase step
0x5E18	PRE RO18	–	R	Bit[7:4]: Reserved Bit[3:0]: Horizontal sensor offset[11:8]
0x5E19	PRE RO19	–	R	Bit[7:0]: Horizontal sensor offset[7:0]
0x5E1A	PRE RO1A	–	R	Bit[7:4]: Reserved Bit[3:0]: Vertical sensor offset[11:8]
0x5E1B	PRE RO1B	–	R	Bit[7:0]: Vertical sensor offset[7:0]

table 6-26 pre_DSP control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5E1C	PRE RO1C	–	R	Bit[7:4]: Reserved Bit[3:0]: Horizontal window offset[11:8]
0x5E1D	PRE RO1D	–	R	Bit[7:0]: Horizontal window offset[7:0]
0x5E1E	PRE RO1E	–	R	Bit[7:4]: Reserved Bit[3:0]: Vertical window offset[11:8]
0x5E1F	PRE RO1F	–	R	Bit[7:0]: Vertical window offset[7:0]
0x5E20	PRE RO20	–	R	Bit[7:5]: Reserved Bit[4:0]: Horizontal window output size[12:8]
0x5E21	PRE RO21	–	R	Bit[7:0]: Horizontal window output size[7:0]
0x5E22	PRE RO22	–	R	Bit[7:4]: Reserved Bit[3:0]: Vertical window output size[11:8]
0x5E23	PRE RO23	–	R	Bit[7:0]: Vertical window output size[7:0]
0x5E24	PRE RO24	–	R	Bit[7:6]: Reserved Bit[5:4]: Horizontal skip Bit[3:2]: Reserved Bit[1:0]: Vertical skip
0x5E25	PRE RO25	–	R	Bit[7:4]: Horizontal even increase step Bit[3:0]: Vertical even increase step
0x5E26	NOT USED	–	–	Not Used
0x5E27	PRE RO27	–	R	Bit[7:4]: Reserved Bit[3:0]: Cut top offset for bi-linear BLC[11:8]
0x5E28	PRE RO28	–	R	Bit[7:0]: Cut top offset for bi-linear BLC[7:0]
0x5E29	PRE RO29	–	R	Bit[7:4]: Reserved Bit[3:0]: Cut bottom offset for bi-linear BLC[11:8]
0x5E2A	PRE RO2A	–	R	Bit[7:0]: Cut bottom offset for bi-linear BLC[7:0]
0x5E2B	PRE CTRL2B	0x09	RW	Bit[7:4]: Reserved Bit[3:0]: Array height for bi-linear BLC[11:8]
0x5E2C	PRE CTRL2C	0xB0	RW	Bit[7:0]: Array height for bi-linear BLC[7:0]
0x5E2D	PRE CTRL2D	0x00	RW	Bit[7:6]: Reserved Bit[5]: Manual horizontal skip enable Bit[4:0]: Reserved
0x5E2E	PRE CTRL2E	0x00	RW	Bit[7:6]: Reserved Bit[5]: Manual vertical skip enable Bit[4:0]: Reserved

7 operating specifications

7.1 absolute maximum ratings

table 7-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 functional temperature

table 7-2 functional temperature

parameter	range
operating temperature (for applications up to 90 fps)[a]	-30°C to +85°C junction temperature
stable image temperature[b]	0°C to +60°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

7.3 DC characteristics

table 7-3 DC characteristics (-30°C < T_J < 85°C) (sheet 1 of 2)

symbol	parameter	min	typ	max[a]	unit
supply					
V_{DD-A}	supply voltage (analog)	2.6	2.8	3.0	V
V_{DD-D}	supply voltage (digital core for 4-lane MIPI up to 1000 Mbps/lane)	1.14	1.2	1.26	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	1.9	V
I_{DD-A}	active (operating) current[b,c] (full 8MP @ 30 fps)		22.5	28	mA
I_{DD-IO}			1.1	2.7	mA
I_{DD-D}			69.2	95	mA
I_{DD-A}	active (operating) current[b,c] (1080p @ 60 fps)		22.5	28	mA
I_{DD-IO}			1.1	2.7	mA
I_{DD-D}			48.6	65	mA
I_{DD-A}	active (operating) current[b,c] (1632x1224 @ 60 fps)		18	24	mA
I_{DD-IO}			1.1	2.7	mA
I_{DD-D}			38.6	52	mA
I_{DD-A}	active (operating) current[b,c] (720p @ 60 fps)		22	28	mA
I_{DD-IO}			1.1	2.7	mA
I_{DD-D}			39.2	53	mA
I_{DD-A}	active (operating) current[b,c] (800x600 @ 90 fps)		22	28	mA
I_{DD-IO}			1.1	2.7	mA
I_{DD-D}			36.2	52	mA
$I_{DDS-SCCB}$	standby current[b,d]		800	3000	µA
$I_{DDS-XSHUTDN}$			1	5	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.2V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF

table 7-3 DC characteristics (-30°C < T_J < 85°C) (sheet 2 of 2)

symbol	parameter	min	typ	max[a]	unit
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[e]	SCL and SDA	-0.5	0	0.54	V
V_{IH}	SCL and SDA	1.28	1.8	3.0	V

a. maximum active current is measured under typical supply voltage

b. power data is based on typical samples and may need adjustments after corner samples test

c. DVDD is provided by external regulator for lower power consumption. DVDD and EVDD are tied together. DOVDD = 1.8V

d. standby current is measured at room temperature with external clock off

e. based on DOVDD = 1.8V

7.4 timing characteristics

table 7-4 timing characteristics

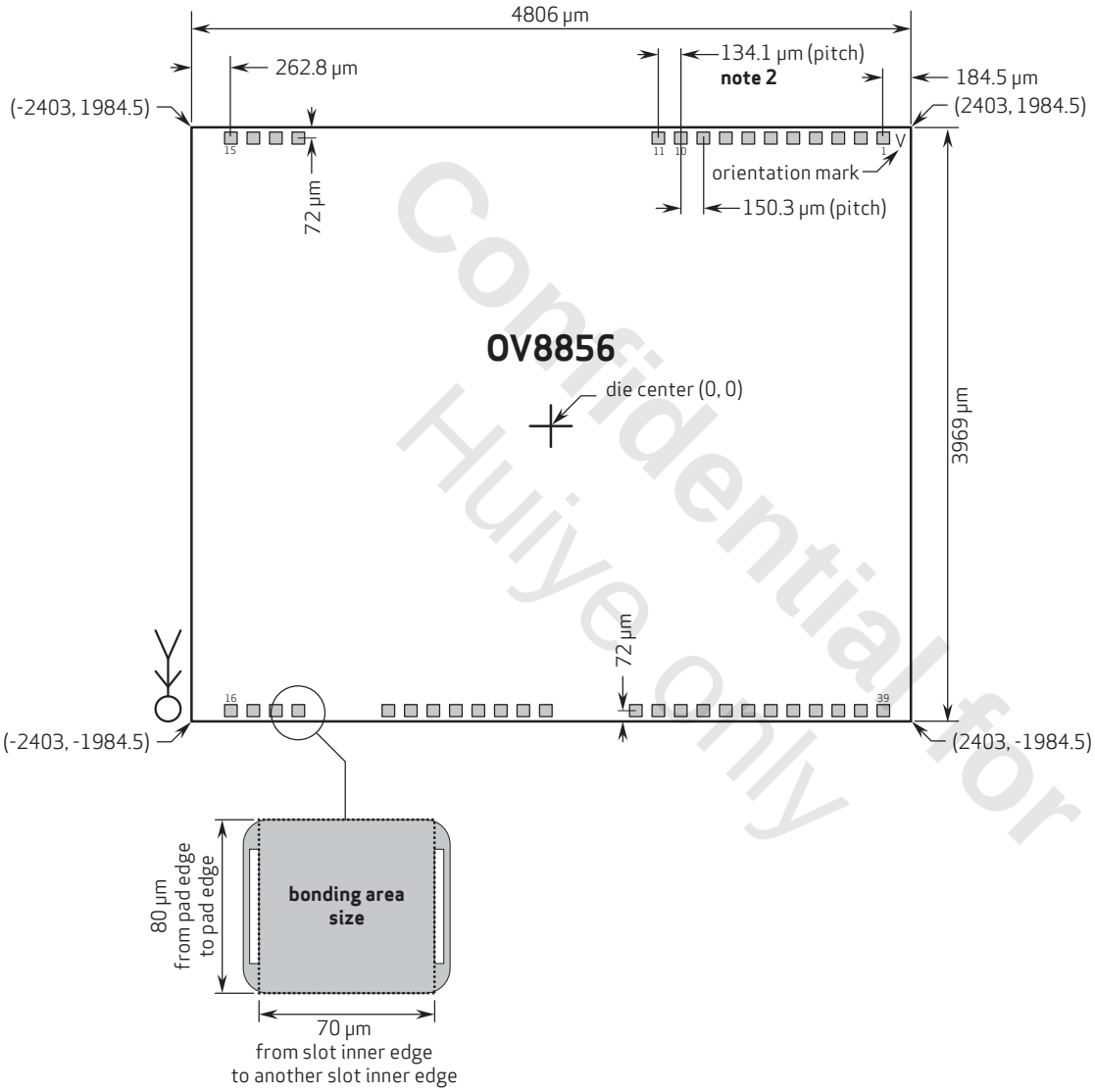
symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns
	clock input duty cycle	45	50	55	%

a. if using internal PLL

8 mechanical specifications

8.1 COB physical specifications

figure 8-1 COB die specifications



note 1 all dimensions and coordinates are in µm unless otherwise specified.

note 2 bond pitch between pads is 150.3µm except between pads 10 and 11 where bond pitch is 134.1µm

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table 8-1 pad location coordinates (sheet 1 of 2)

pad number	pad name	x coordinate	y coordinate	bonding area size
1	DOGND	2218.5	1912.5	70x80
2	DVDD	2068.2	1912.5	70x80
3	AGND	1917.9	1912.5	70x80
4	AVDD	1767.6	1912.5	70x80
5	SID	1617.3	1912.5	70x80
6	SCL	1467.0	1912.5	70x80
7	SDA	1316.7	1912.5	70x80
8	FSIN/VSYNC	1166.4	1912.5	70x80
9	DOVDD	1016.1	1912.5	70x80
10	XSHUTDN	865.8	1912.5	70x80
11	TM	731.7	1912.5	70x80
12	DVDD	-1689.3	1912.5	70x80
13	DOGND	-1839.6	1912.5	70x80
14	AVDD	-1989.9	1912.5	70x80
15	AGND	-2140.2	1912.5	70x80
16	AGND	-2140.2	-1912.5	70x80
17	AVDD	-1989.9	-1912.5	70x80
18	VH	-1839.6	-1912.5	70x80
19	VN	-1689.3	-1912.5	70x80
20	DOGND	-1088.1	-1912.5	70x80
21	MDP2	-937.8	-1912.5	70x80
22	MDN2	-787.5	-1912.5	70x80
23	MDP0	-637.2	-1912.5	70x80
24	MDN0	-486.9	-1912.5	70x80
25	EGND	-336.6	-1912.5	70x80
26	PVDD	-186.3	-1912.5	70x80
27	EVDD	-36.0	-1912.5	70x80
28	MCP	565.2	-1912.5	70x80
29	MCN	715.5	-1912.5	70x80
30	EGND	865.8	-1912.5	70x80

table 8-1 pad location coordinates (sheet 2 of 2)

pad number	pad name	x coordinate	y coordinate	bonding area size
31	MDP1	1016.1	-1912.5	70x80
32	MDN1	1166.4	-1912.5	70x80
33	EVDD	1316.7	-1912.5	70x80
34	MDP3	1467.0	-1912.5	70x80
35	MDN3	1617.3	-1912.5	70x80
36	DOVDD	1767.6	-1912.5	70x80
37	XVCLK	1917.9	-1912.5	70x80
38	DVDD	2068.2	-1912.5	70x80
39	DOGND	2218.5	-1912.5	70x80

8.2 reconstructed wafer (RW) physical specifications

- maximum total die count: 1279
- film frame: Compact Disco stainless SUS420
- carrier tape: UV tape

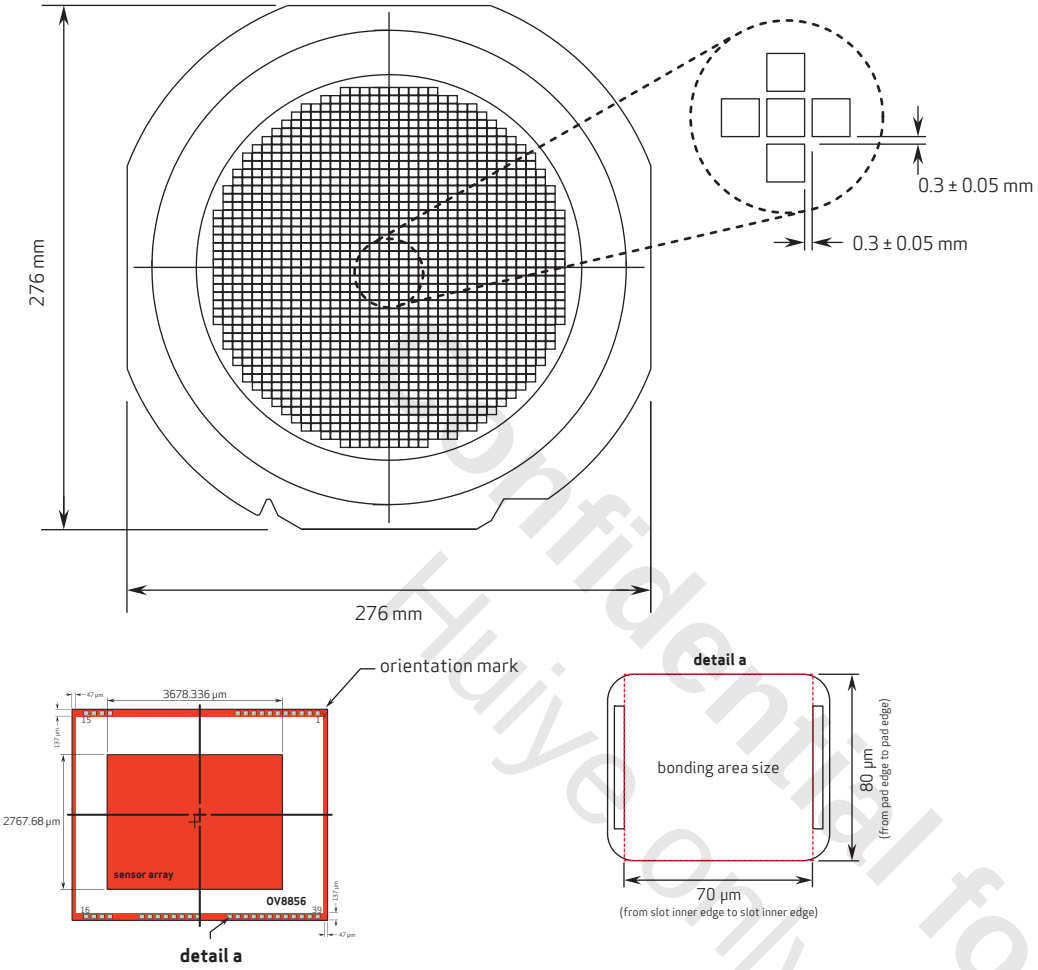
note
Actual die count varies and the absent die may be less than 10% of the maximum total die count (excluding the last frame of the wafer lot).

table 8-2 RW physical dimensions

feature	dimensions
RW physical dimensions	8" RW on 12" frame
wafer thickness (OVXXXXX-ABCD)	
C=4	200 µm ± 10 µm (7.9 mil ± 0.4 mil)
reconstructed wafer street width	300 µm ± 50 µm (11.8 mil ± 2 mil)
placement accuracy x, y, theta	± 50 µm (± 2 mil), <1.0 degree
singulated die size	
width	4856 µm ± 20 µm (191.2 mil ± 0.8 mil)
length	4019 µm ± 20 µm (158.2 mil ± 0.8 mil)
bond pad size	88 µm × 80 µm (3.5 mil × 3.1 mil)
minimum bond pad pitch	134.1 µm (5.3 mil)
bonding area size	70 µm × 80 µm (2.8 mil × 3.1 mil)
optical array	
die center	(0, 0)
optical center from die center[a]	-95.4 µm, -135 µm (-3.8 mil, -5.3 mil)

a. based on die orientation on frame with notch facing down position

figure 8-2 OV8856 RW physical diagram



note 1 bonding outside the defined bonding area is prohibited, it may potentially induce reliablity issues or functionality failure

note 2 keep-out-of-contact areas are highlighted in red color for related process fixtures/tools (e.g., nozzle, collets, etc).

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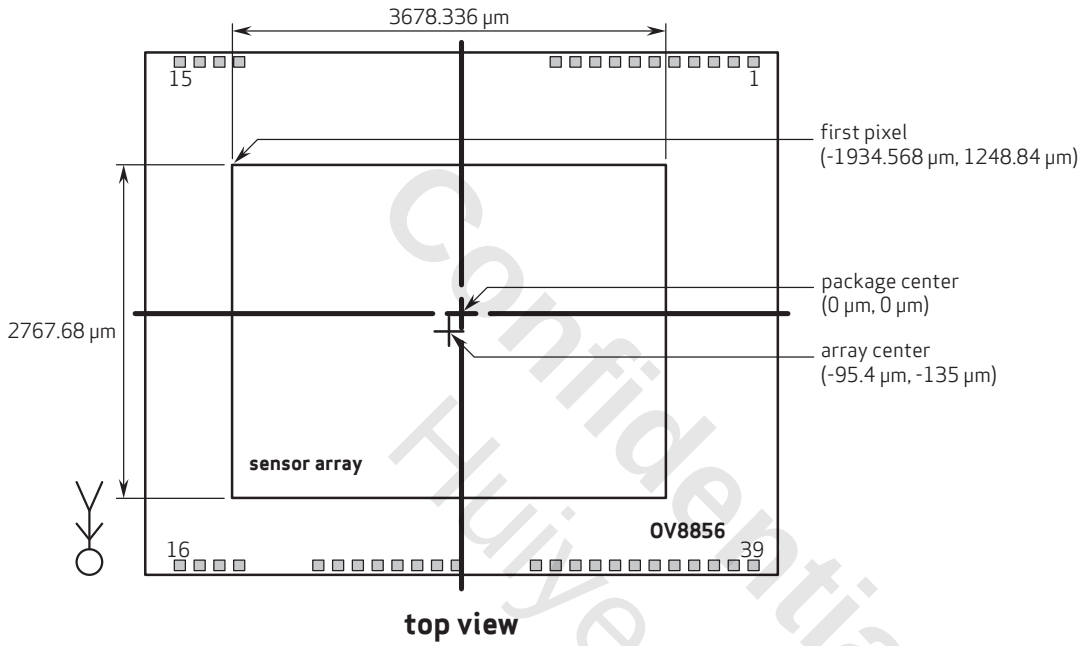
9 optical specifications

9.1 sensor array center

figure 9-1 sensor array center



note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pad 1 oriented down on the PCB.

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9.2 lens chief ray angle (CRA)

figure 9-2 chief ray angle (CRA)

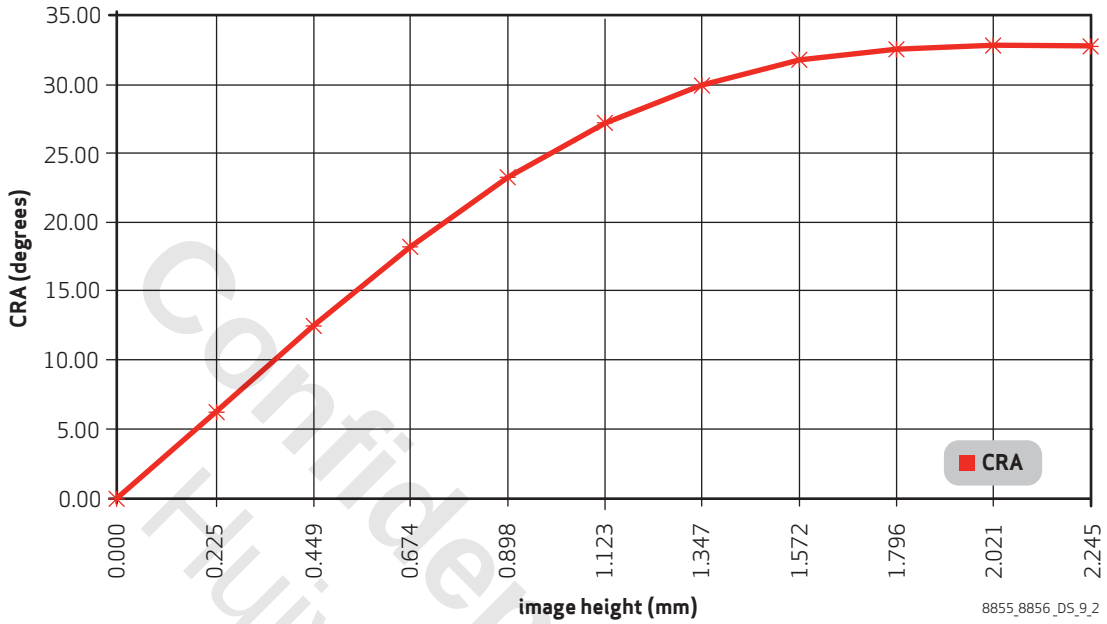

table 9-1 CRA versus image height plot

field (%)	image height (mm)	CRA (degrees)
0.00	0.000	0.00
0.10	0.229	6.35
0.20	0.457	12.55
0.30	0.686	18.30
0.40	0.914	23.29
0.50	1.143	27.26
0.60	1.371	30.07
0.70	1.600	31.80
0.80	1.828	32.63
0.90	2.057	32.86
1.00	2.285	32.78

appendix A handling of RW devices

A.1 ESD /EOS prevention

1. Ensure that there is 500V ESD control in all work areas.
2. Use ESD safety shoes, ground strap, and static control smocks in test areas.
3. Use grounded work carts and tables in inspection areas.
4. OmniVision recommends the use of ionized air in all work areas.

A.2 particles and cleanliness of environment

1. All production, inspection and packaging areas should meet Class10 environment requirements.
2. Use optical microscopes with 50X and 100X magnifications for particle inspection.
3. Ensure that there is good cassette sealing for particle protection during storage.
4. OmniVision recommends water cleaning to remove removable particles.
5. RW die should be stored in nitrogen gas purged cabinets with temperature less than 30°C and relative humidity of 60% before assembly.

A.3 other requirements

1. Reliability assurance of RW or COB bare die is certified by product reliability of the bare die in a CLCC, CSP or QFP package form factor. Precautions should be taken if the packaging form factor of the bare die is other than these specified.
2. Avoid exposure to strong sunlight for extended periods of time as the color filter of the image sensor may become discolored.
3. Avoid direct exposure of the sensor bare die to high temperature and/or humidity environment as sensor characteristics will be affected. Extra precautions should be exercised if the bare die experiences temperatures exceeding 260°C for more than 75 seconds.

revision history

version 1.0 05.20.2015

- initial release

version 1.01 09.04.2015

- in chapter 2, added section 2.1.1
- in table 5-6, changed description of register 0x350A to Bit[3:0]: Long digital gain[11:8] and description of register 0x350B to Bit[7:0]: Long digital gain[7:0]
- in table 6-2, changed default value for register 0x300B to 0x88 and default value for register 0x300C to 0x5A
- in table 6-2, added "For PID, read OTP register 0x7000 = 0x00, register 0x7001 = 0x88, and register 0x7002 = 0x56 (see section 2.1.1)
- in table 6-5, changed description of register 0x350A to Bit[3:0]: Long digital gain[11:8] and description of register 0x350B to Bit[7:0]: Long digital gain[7:0]

version 1.02 09.15.2015

- in figure 2-1, removed temperature sensor

version 1.1 10.29.2015

- in table 2-1, changed 10-bit output MIPI data rate for 8 MP, 6 MP HD, EIS1080p, and 1080p to "2-lane @ 1.272 Gbps/lane"
- in section 4.5.1, changed last sentence of second paragraph to "...register bit 0x5001[3] = 0" and changed 5002 to 5001 in first line to program OTP and in first line in setting for loading
- in table 6-2, changed description of register bit 0x3021[5] to Not used
- in table 6-18, changed description of register bit 0x4800[3] to "Bit[3]: fst_stby_ctr; 0: Software standby enter at v_blk; 1: Software standby enter at l_blk"
- in chapter 8, updated figure 8-1 and figure 8-2
- in table 8-1, changed x-coordinate of TM pad (pad 11) from 715.5µm to 731.7µm
- in table 8-2, updated minimum bond pad pitch and bonding area size

version 1.11 12.17.2015

- in key specifications, changed active power requirements to 150 mW, standby power requirements to 0.8 mW, XSHUTDN power requirements to 1 µW, max S/N ratio to 36.5 dB, dynamic range to 70 dB @ 8x gain, sensitivity to 480 mV/Lux-sec, and dark current to 12e^-/s @ 60°C junction temperature
- in chapter 3, added section 3.3
- in section 4.2, added second paragraph

- in section 5.6, added "The minimum exposure of the sensor is 6 lines and maximum exposure is VTS {0x380E, 0x380F} - 6." at end of first paragraph and changed sidebar note to "For optimal performance, minimum exposure of sensor is 6 lines and maximum exposure is VTS {0x380E, 0x380F} - 6."
- in table 7-3, replaced all TBDs with real values and added table footnote b, "power data is based on typical samples and may need adjustments after corner samples test"

version 1.12 01.14.2016

- in table 3-2, removed note at end of description of register 0x3509

version 1.13 01.27.2016

- in table 4-1, changed description of register bit 0x3821[2] to Bit[2]: Digital horizontal mirror control, 0: Mirrored image, 1: Normal image and changed description of register bit 0x3821[1] to Bit[1]: Array horizontal mirror control, 0: Mirrored image, 1: Normal image
- in table 6-8, changed description of register bit 0x3821[2] to Bit[2]: Digital horizontal mirror control, 0: Mirrored image, 1: Normal image and changed description of register bit 0x3821[1] to Bit[1]: Array horizontal mirror control, 0: Mirrored image, 1: Normal image

version 1.14 03.14.2016

- in section 5.5, removed paragraph under figure 5-1

version 2.0 05.16.2016

- changed datasheet from Preliminary Specification to Product Specification

version 2.01 01.20.2017

- in table 4-2, changed bit description for register 0x380E[6:0] from "Bit[6:0]..." to "Bit[7:0]..."

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