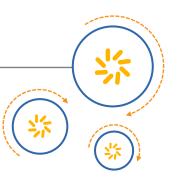


Qualcomm Technologies, Inc.



# **PM8937**

# Hardware Register Description

80-P2564-2X Rev. B April 15, 2016

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## **Revision history**

Bars appearing in the left margin (as shown here) indicate where technical changes have occurred for this revision. The following tables list the technical content changes for all revisions.

## Revision A, December 2015, initial release

#### Revision B, April 2016

Chapter	Section	Description
82	0x0001F145 CDC_A_TX_1_2_ATEST_CTL_2	Added TX1N configuration register details for CDC_A_TX_1_2_ATEST_CTL_2
	2018-09-21 oli Com 2018-su@mindreth.com	

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# 1 Introduction

## 1.1 Overview

The PMIC (power management integrated circuit) device consists of two slave IDs. Each slave ID has 64K addresses. These addresses are subdivided into 256 groups of 256 addresses. Each of these groups is known as a peripheral.

Because each PMIC device has two slave IDs, the address map can support up to 512 peripherals. The MSM<sup>TM</sup> device supports up to only 256 peripherals.

The top eight bits are known as the peripheral address and the bottom eight bits are known as the *register offset*.

Two identical peripherals (for example, LDOs) have different peripheral IDs, but the registers within each peripheral have the same register offset. The unique slave ID (USID) allows the MSM device to access more peripherals by increasing the available register map.

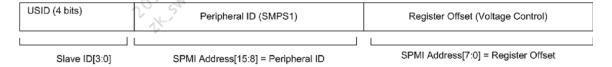


Figure 1-1 Addressing structure

Peripheral IDs are predefined and specified.

## 1.2 Slave ID

The PMIC device has two unique slave IDs (USID):

- USID 0 and 1 are reserved for the primary PMIC (PM8937 device)
- USID 2 and 3 are reserved for the secondary PMIC (PM8937 device)

Internally, the USID is translated into a local slave ID (LSID).

- The first USID maps to LSID 0
- The second USID maps to LSID 1

The PMIC device could have up to four LSIDs, but only the first two are addressable from the SPMI bus.

# 1.3 Register description

Figure 1-2 illustrates each element of a register description.

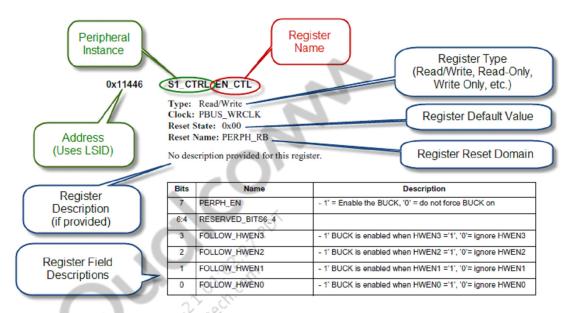


Figure 1-2 PMIC register map

The address is broken down into LSID, PID, and register offset.

For example, in the address 0x11446, from left to right:

- 1 is the unique slave ID
- 14 is the peripheral ID
- 46 is the register offset

The LSID is provided in all the register maps. In most applications, where the PMIC device is accessed from the SPMI bus, the USID is used.

## 1.4 Peripheral register map

Each peripheral has 256 registers that are sub-divided into sections. The subsections of the peripheral register map are as follows:

- Peripheral status
- Interrupts
- Control
- Reserved

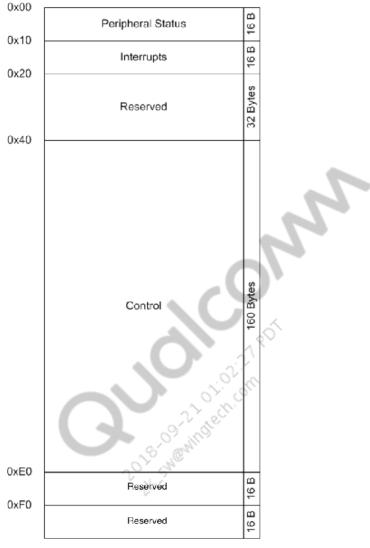


Figure 1-3 Peripheral register map

## 1.5 Peripheral interrupts

Each peripheral has interrupts contained within its register map. Each register is reserved for a different function. Each bit defines a different interrupt. For example, for the GPIO IN interrupt:

- Bit 0 is reserved
- 0x10[0] holds real-time status
- 0x11[0] defines type (level/edge)
- 0x12[0] defines polarity

This setup reduces the number of transactions required to service interrupts. All of the real-time status bits for the interrupts within the module can be read with a single read of the INT\_RT\_STS register.

Similarly, the status of the latched interrupts is acquired with a single read of the INT LATCHED STS register.

Table 1-1 Example of interrupt register map

Offset	Register	MSB	LSB	Bit	Default	Description
0x10	INT_RT_STS	1	1	GPIO_HI_RT_STS	0	Interrupt real time status bits
		0	0	GPIO_IN_RT_STS	0	
0x12	INT_POLARITY_HIGH	1	1	GPIO_HI_HIGH	0	1: Interrupt triggers on a level high
		0	0	GPIO_IN_HIGH	0	<ul><li>(rising edge) event.</li><li>0: Level HIGH triggering is disabled.</li></ul>
0x13	INT_POLARITY_LOW	1	1	GPIO_HI_LOW	0	1: Interrupt triggers on a level low
		0	0	GPIO_IN_LOW	0	(falling edge) event. 0: Level low triggering is disabled.
0x14	INT_LATCHED_CLR	1	1	GPIO_HI_LATCHED_CLR	0	1: Rearms the interrupt when an
		0	0	GPIO_IN_LATCHED_CLR	0	interrupt is pending. Clears the internal latched status.
0x15	INT_EN_SET	1	1	GPIO_HI_EN_SET	0	0: Has no effect.
		0	0	GPIO_IN_EN_SET	0	Enables the corresponding interrupt. Reading this register returns enable status.
0x16	INT_EN_CLR	1	1	GPIO_HI_EN_CLR	0	0: Has no effect.
		0	0	GPIO_IN_EN_CLR	0	Disables the corresponding interrupt. Reading this register returns enable status.
0x18	INT_LATCHED_STS	1	\ <sup>9</sup> 1.©	GPIO_HI_LATCHED_STS	0	Latched Interrupt.
		0	110	GPIO_IN_LATCHED_STS	0	1: indicates the interrupt has triggered. Once the latched bit is set, it can be cleared by writing the clear bit.
0x19	INT_PENDING_STS	1	1	GPIO_HI_PENDING_STS	0	Pending is set if interrupt has been
		0	0	GPIO_IN_PENDING_STS	0	sent but not cleared.
0x1A	INT_MID_SEL	1	0	INT_MID_SEL	0	Selects the MID that receives the interrupt.
0x1B	INT_PRIORITY	0	0	INT_PRIORITY	0	SR = 0 A = 1

# 1.6 Interrupt configuration

## 1.6.1 Set and forget registers

INT\_MID\_SEL: There is only one master (the MSM), so the MID is 0x00 for every peripheral.

INT\_PRIORITY: SPMI supports two levels of priority. Every interrupt should use low priority; there are no high priority use cases identified.

## 1.6.2 Enabling interrupts

Interrupts default to disabled. To enable an interrupt, set the TYPE, PRIORITY\_HIGH, and PRORITY LOW fields. Use read-modify-write to control these registers.

Once the interrupts are configured, they can be enabled. There are two INT\_EN registers: INT\_EN\_SET and INT\_EN\_CLR.

Enable the interrupt by setting the corresponding bit in INT\_EN\_SET. Disable the interrupt by setting the corresponding bit in INT\_EN\_CLR. No read-modify-write is required for these registers. Writing 0 to these registers has no effect. Reading either register returns an enable status.

## 1.6.3 Interrupt detection

Interrupts are sent to the master using the SPMI master write command. The interrupt message includes the peripheral ID and the triggered interrupt. In one message, all the interrupt information is communicated to the MSM device.

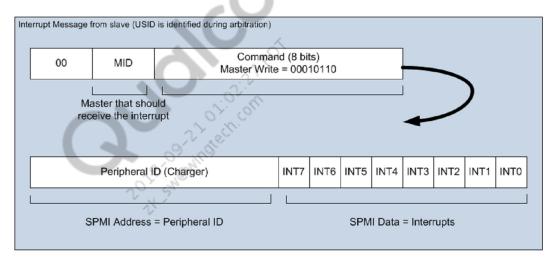


Figure 1-4 Interrupt message

## 1.6.4 Clearing interrupts

Assuming an interrupt is fired by GPIO 01 (peripheral ID 0x25):

- 1. The interrupt is generated in the PMIC device. The message is sent to the peripheral owner (RPM) via SPMI and the PMIC arbiter (in the MSM device). The message indicates that the interrupt came from GPIO\_01 (PID = 0x25) and that the VREG\_OK interrupt triggered.
- 2. (Optional) Software performs a 6-byte read starting at address 0x2510. Software is able to read status, type (level/edge), en high, en low, and enable state in a single read.
- 3. Software performs a 1-byte write of 0x01 to register 0x2516 to disable the interrupt.
- 4. The interrupt handler takes care of the interrupt.
- 5. When software is ready, a 2-byte write of 0x0101 to 0x2514 clears the interrupt and then reenables the interrupt.

# 2 Revid\_PM8937 Registers

## 0x00000100 REVID\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

#### REVID\_REVISION1

Bits	Name	Description
7:0	RFU CONTROL	Reserved for future use

## 0x00000101 REVID\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

#### **REVID\_REVISION2**

Bits	Name	Description
7:0	VARIANT	This field indicates the chip variant

## 0x00000102 REVID\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### **REVID\_REVISION3**

Bits	Name	Description
7:0	METAL	This number is incremented on a metal-only revision of the chip

#### 0x00000103 REVID\_REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [31:24]

#### REVID\_REVISION4

Bits	Name	Description
7:0	ALL_LAYER	This number is incremented every time there is an all layer revision of the chip

#### 0x00000104 REVID\_PERPH\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x51

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### REVID\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	REVID (This tells you that you are talking to a PMIC)

## 0x00000105 REVID\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x19

Reset Name: N/A

Peripheral SubType

PMIC\_CONSTANT

### REVID\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	This is PM8937

## 0x00000108 REVID\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Status Registers

#### **REVID\_STATUS1**

Bits	Name	Description
3:2	OPTION2	Option Pin State 11: VDD 10: HiZ 00: GND
1:0	OPTION1	Option Pin State 11: VDD 10: HiZ 00: GND

## 0x00000150 REVID\_SBL\_ID\_0

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: xVdd rb

#### REVID\_SBL\_ID\_0

Bits	Name	Description
7:0	VERSION	Number associated with each SBL version

## 0x00000151 REVID\_SBL\_ID\_1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: xVdd\_rb

#### REVID\_SBL\_ID\_1

Bits	Name	Description
7:0	VERSION	Number associated with each SBL version

## 0x00000154 REVID\_PBS\_OTP\_ID\_0

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: xVdd\_rb

## REVID\_PBS\_OTP\_ID\_0

Bits	Name	Description
7:0	VERSION	Number associated with each PBS_OTP version

## 0x000001D0 REVID\_SEC\_ACCESS

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: dVdd\_rb

PMIC\_LOCKING

#### REVID\_SEC\_ACCESS

Bits	Name	Description
7:0	SEC_UNLOCK	Unlock the Secure Registers (0xTBD) by writing 0xA5 to this register. Lock is rearmed after the next write to the module.

# 3 Intbus\_arb\_dig Registers

## 0x00000400 BUS\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

#### **BUS REVISION1**

Bits	Name	20,	Description
7:0	DIG_MINOR	3 . W.	

## 0x00000401 BUS\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

#### **BUS\_REVISION2**

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x00000404 BUS\_PERPH\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x0B Reset Name: N/A

Peripheral Type

#### BUS\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0xB: INTERFACE

## 0x00000405 BUS\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02 Reset Name: N/A

Peripheral SubType

### **BUS\_PERPH\_SUBTYPE**

Bits	Name	Description
7:0	SUBTYPE	0x2: INTBUS_ARB

## 0x00000408 BUS\_STATUS1

**Type:** R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: N/A

Status Registers

#### **BUS\_STATUS1**

Bits	Name	Description
3:0	INTBUS_ARB_GNT	Grant Values

## 0x00000444 BUS\_TIMEOUT

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_SYNC=clk\_19\_2m:dVdd\_rb

## **BUS\_TIMEOUT**

Bits	Name	Description
7:4	TIMEOUT_MANT	after TIMEOUT_MANT(2^(TIMEOUT_EXP+4))*52 ns that a master holds onto the bus, a new arbitration is forced. Write zero if no timeout desired.
3:0	TIMEOUT_EXP	after TIMEOUT_MANT(2^(TIMEOUT_EXP+4))*52 ns that a master holds onto the bus, a new arbitration is forced. Write zero if no timeout desired.
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# 4 Intr\_dig Registers

## 0x00000500 INT\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x03

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

## INT\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00000501 INT\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### INT\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x00000504 INT\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x0A

Reset Name: N/A

Peripheral Type

PMIC\_CONSTANT

#### INT\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0xA: INTERRUPT

## 0x00000505 INT\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### INT\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x1: PNP_INTERRUPT

#### 0x00000508 INT\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: dVdd\_rb

Status Register 1

#### **INT\_STATUS1**

Bits	Name	Description
1	CLK_REQ	Or of all clk_requests
		0x0: NO_CLOCK_REQ
		0x1: CLOCK_REQUESTED
0	SEND_REQ	Or of all send_requests
		0x0: NO_SEND_REQ
		0x1: SEND_REQUESTED

## 0x00000509 INT\_STATUS2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: dVdd rb

Status Register 2

#### INT\_STATUS2

Bits	Name	Description
7:0	LAST_WINNER	Last Arbitration Winner

## 0x00000540 INT\_INT\_RESEND\_ALL

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

Clear all Sent bits and resend all interrupts.

### INT\_INT\_RESEND\_ALL

Bits	Name	Description
0	INT_RESEND_ALL	Clear all Sent bits and resend all interrupts.  0x1: RESEND_ALL

## 0x00000546 INT\_EN\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### INT\_EN\_CTL1

Bits	Name	Description
7	INTR_EN	INTR enable
		0 = disables INTR from sending messages
		1 = INTR is enabled and can send messages
		0x0: PERIPHERAL_DISABLED
		0x1: PERIPHERAL_ENABLED

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# 5 Spmi\_p\_dig Registers

## 0x00000600 SPMI\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x05

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### SPMI\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00000601 SPMI\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### SPMI\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x00000602 SPMI\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### SPMI\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00000603 SPMI\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### SPMI\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00000604 SPMI\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x0B

Reset Name: N/A

Peripheral Type

PMIC\_CONSTANT

#### SPMI\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0xB: INTERFACE

## 0x00000605 SPMI\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### **SPMI PERPH SUBTYPE**

Bits	Name	Description
7:0	SUBTYPE	0x1: SPMI

## 0x00000608 SPMI\_ERROR\_SYNDROME

**Type:** R

Clock: PBUS\_WRCLK

**Reset State:** 0x00

Reset Name: N/A

Status Register

## SPMI\_ERROR\_SYNDROME

Bits	Name	Description
7:0	ERROR_SYNDROME	Error Syndrome from SPMI

## 0x0000060B SPMI\_ERROR\_DATA

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Status Register

#### SPMI\_ERROR\_DATA

Bits	Name	Description
7:0	ERROR_DATA	Data upon data parity error

## 0x0000060C SPMI\_ERROR\_ADDR\_LO

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Status Register

#### SPMI\_ERROR\_ADDR\_LO

Bits	Name	Description
7:0	ERROR_ADDR_LO	lower 8 bits of address upon data or addr parity error

## 0x0000060D SPMI\_ERROR\_ADDR\_MD

Type: R

Clock: PBUS WRCLK

Reset State: 0x00

Reset Name: N/A

Status Register

#### SPMI\_ERROR\_ADDR\_MD

Bits	Name	Description
7:0	ERROR_ADDR_MD	middle 8 bits of address upon data or addr parity error

## 0x0000060E SPMI\_ERROR\_ADDR\_HI

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Status Register

#### SPMI\_ERROR\_ADDR\_HI

Bits	Name	Description
3:0	ERROR_ADDR_HI	higher 4 bits of address upon data or addr parity error

## 0x00000610 SPMI\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Interrupt Real Time Status Bits

#### SPMI\_INT\_RT\_STS

Bits	Name	Description
0	SPMI_INT_RT_STS	180

## 0x00000611 SPMI\_INT\_SET\_TYPE

Type: R

Clock: PBUS\_WRCLK

Reset State: 0x01

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### SPMI\_INT\_SET\_TYPE

Bits	Name	Description
0	SPMI_INT_TYPE	

## 0x00000612 SPMI\_INT\_POLARITY\_HIGH

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### SPMI\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	SPMI_INT_HIGH	

#### 0x00000613 SPMI\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### SPMI\_INT\_POLARITY\_LOW

Bits	Name	Description
0	SPMI_INT_LOW	180

## 0x00000614 SPMI\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK

Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### SPMI\_INT\_LATCHED\_CLR

Bits	Name	Description
0	SPMI_INT_LATCHED_CLR	

### 0x00000615 SPMI\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### SPMI\_INT\_EN\_SET

Bits	Name	Description
0	SPMI_INT_EN_SET	

#### 0x00000616 SPMI\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### SPMI\_INT\_EN\_CLR

Bits	Name	Description
0	SPMI_INT_EN_CLR	

#### 0x00000618 SPMI\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

### SPMI\_INT\_LATCHED\_STS

Bits	Name	Description
0	SPMI_INT_LATCHED_STS	

## 0x00000619 SPMI\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### SPMI\_INT\_PENDING\_STS

Bits	Name	Description
0	SPMI_INT_PENDING_STS	

## 0x0000061A SPMI\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

### SPMI\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	

## 0x0000061B SPMI\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### SPMI\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	

## 0x00000640 SPMI\_SPMI\_BUF\_CFG

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

#### SPMI\_SPMI\_BUF\_CFG

Bits	Name	Description
1:0	BUFFER_STRENGTH	SPMI Buffer Drive Strength Configuration
		0x0: LOW10PF
		0x1: MID20PF
		0x2: HIGH40PF
		0x3: VERYHIGH50PF
1		

## 0x00000641 SPMI\_SSC\_DETECT\_CFG

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

SCC Detection Configuration

## SPMI\_SSC\_DETECT\_CFG

Bits	Name	Description
2:0	SSC_DETECT_CFG	Bit0=Q1_DELAY_DISABLE
		when bit=1 then the delay between q1 and q2 is disabled, there is a mux between the flops and the bit is connected to the mux_select. When at default=0,q2 uses q1_delayed and glitch should be masked.
		Bit1=WINDOW_ENABLE
		when bit=1 then SSC detects only when it is expected,default=0 detect SSC all time.
		Bit2=Reserved
		0x0: WINDOW_DISABLED_Q1_DELAY_ENABLED
		0x1: WINDOW_DISABLED_Q1_DELAY_DISABLED
		0x2: WINDOW_ENABLED_Q1_DELAY_ENABLED
		0x3: WINDOW_ENABLED_Q1_DELAY_DISABLED

# 6 Pon Registers

## 0x00000800 PON\_REVISION1

Type: R

Clock: pbus\_wrclk Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### PON\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00000801 PON\_REVISION2

**Type:** R

Clock: pbus\_wrclk
Reset State: 0x03

Reset Name: N/A

HW Version Register [15:8]

PMIC\_CONSTANT

#### PON\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x00000802 PON\_REVISION3

Type: R

Clock: pbus\_wrclk Reset State: 0x03

Reset Name: N/A

HW Version Register [23:16]

#### PON\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00000803 PON REVISION4

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### PON\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00000804 PON\_PERPH\_TYPE

Type: R

Clock: pbus\_wrclk Reset State: 0x01

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### PON\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0x1: PON

## 0x00000805 PON\_PERPH\_SUBTYPE

Type: R

Clock: pbus\_wrclk
Reset State: 0x01

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### PON\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x1: LV_PON

## 0x00000807 PON\_PON\_PBL\_STATUS

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: N/A

Stage 2 reset generation and register access error status.

#### PON\_PON\_PBL\_STATUS

Bits	Name	Description
7	DVDD_RB_OCCURRED	DVDD_RB was asserted during the last power cycle 0x0: NO_RESET 0x1: RESET_OCCURRED
6	XVDD_RB_OCCURRED	XVDD_RB was asserted during the last power cycle 0x0: NO_RESET 0x1: RESET_OCCURRED
5	REG_WRITE_ERROR	A register field write was attempted when a block was enabled. Writing to this address clears field.  0x0: NO_ERROR  0x1: ERROR_OCCURRED

## PON\_PON\_PBL\_STATUS (cont.)

Bits	Name	Description
4	REG_RESET_ERROR	A register field write was attempted when reset was asserted. Writing to this address clears field. 0x0: NO_ERROR 0x1: ERROR_OCCURRED
3	REG_SYNC_ERROR	Indicates a synchronized register field was over written before it's contents were latched by logic. Writing to this address clears field.,'NO_ERROR=0, ERROR_OCCURRED=1',,,'

## 0x00000808 PON\_PON\_REASON1

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: raw xVdd rb

Reasons that the PMIC left the off state. All zeros mean that no trigger received

## PON\_PON\_REASON1

Bits	Name	Description
7	KPDPWR_N	Triggered from new KPDPWR press 0x1: TRIGGER RECEIVED
6	CBLPWR N	Triggered from CBL PWR1 N
	OBEI WICING	0x1: TRIGGER_RECEIVED
5	PON1	Triggered from PON1
		0x1: TRIGGER_RECEIVED
4	USB_CHG	Triggered from USB charger
		0x1: TRIGGER_RECEIVED
3	DC_CHG	Triggered from DC charger
		0x1: TRIGGER_RECEIVED
2	RTC	Triggered from RTC
		0x1: TRIGGER_RECEIVED
1	SMPL	Triggered from SMPL
		0x1: TRIGGER_RECEIVED
0	HARD_RESET	Triggered from a Hard Reset event (check POFF reason for the trigger)
		0x1: TRIGGER_RECEIVED

#### 0x0000080A PON\_WARM\_RESET\_REASON1

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: raw xVdd rb

Reasons that PMIC entered the Warm Reset state (pst 13).

This register is automatically reset when the PMIC turns on (i.e.

PON\_WARM\_REASON\_CLEAR register field 1) or by writing to this address. This is a synchronized address so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.

#### PON\_WARM\_RESET\_REASON1

Bits	Name	Description
7	KPDPWR_N	Triggered by KPDPWR_N 0x1: TRIGGER_RECEIVED
6	RESIN_N	Triggered by RESIN_N 0x1: TRIGGER_RECEIVED
5	KPDPWR_AND_RESIN	Triggered by simultaneous KPDPWR_N + RESIN_N 0x1: TRIGGER_RECEIVED
4	GP2	Triggered by Keypad_Reset2 0x1: TRIGGER_RECEIVED
3	GP1	Triggered by Keypad_Reset1 0x1: TRIGGER_RECEIVED
2	PMIC_WD	Triggered by PMIC Watchdog 0x1: TRIGGER_RECEIVED
1	PS_HOLD	Triggered by PS_HOLD 0x1: TRIGGER_RECEIVED
0	SOFT	Triggered by Software 0x1: TRIGGER_RECEIVED

## 0x0000080B PON\_WARM\_RESET\_REASON2

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: raw xVdd rb

Reasons that PMIC entered the Warm Reset state (pst\_13). This register is automatically reset when the PMIC turns on (i.e. PON\_WARM\_REASON\_CLEAR register field 1) or by writing to WARM RESET REASON1 register address.

#### PON\_WARM\_RESET\_REASON2

Bits	Name	Description
4	AFP	Triggered AFP
		0x1: TRIGGER_RECEIVED

#### 0x0000080C PON\_POFF\_REASON1

**Type:** R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: raw\_xVdd\_rb

Reasons that the PMIC left the on state and commenced a shutdown sequence. All zeros mean that no trigger received or a master bandgap or phone power fault occurred.

## PON\_POFF\_REASON1

Bits	Name	Description
7	KPDPWR_N	Triggered by KPDPWR_N 0x1: TRIGGER_RECEIVED
6	RESIN_N	Triggered by RESIN_N 0x1: TRIGGER_RECEIVED
5	KPDPWR_AND_RESIN	Triggered by simultaneous KPDPWR_N + RESIN_N 0x1: TRIGGER_RECEIVED
4	GP2	Triggered by Keypad_Reset2 0x1: TRIGGER_RECEIVED
3	GP1	Triggered by Keypad_Reset1 0x1: TRIGGER_RECEIVED
2	PMIC_WD	Triggered by PMIC Watchdog 0x1: TRIGGER_RECEIVED
1	PS_HOLD	Triggered by PS_HOLD 0x1: TRIGGER_RECEIVED
0	SOFT	Triggered by Software 0x1: TRIGGER_RECEIVED

## 0x0000080D PON\_POFF\_REASON2

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: raw\_xVdd\_rb

Reasons that the PMIC left the on state and commenced a shutdown sequence. All zeros mean that no trigger received or a master bandgap or phone power fault occurred.

#### PON\_POFF\_REASON2

Bits	Name	Description
7	STAGE3	Triggered by stage3 reset
		0x1: TRIGGER_RECEIVED
6	OTST3	Triggered by Overtemp
		0x1: TRIGGER_RECEIVED
5	UVLO	Triggered by UVLO
		0x1: TRIGGER_RECEIVED
4	AFP	Triggered by AFP
		0x1: TRIGGER_RECEIVED
3	CHARGER	Triggered by Charger (ENUM_TIMER, BOOT_DONE)
		0x1: TRIGGER_RECEIVED
2	AVDD_RB	Triggered by AVDD_RB
		0x1: TRIGGER_RECEIVED

# 0x0000080E PON\_SOFT\_RESET\_REASON1

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: raw xVdd rb

Reasons that the PMIC registers were reset. All zeros mean that no trigger received.

Clear both soft reason registers by writing to this register. This is a synchronized address so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.

#### PON\_SOFT\_RESET\_REASON1

Bits	Name	Description
7	KPDPWR_N	Triggered by KPDPWR_N 0x1: TRIGGER_RECEIVED
6	RESIN_N	Triggered by RESIN_N 0x1: TRIGGER_RECEIVED
5	KPDPWR_AND_RESIN	Triggered by simultaneous KPDPWR_N + RESIN_N 0x1: TRIGGER_RECEIVED
4	GP2	Triggered by Keypad_Reset2 0x1: TRIGGER_RECEIVED

#### PON\_SOFT\_RESET\_REASON1 (cont.)

Bits	Name	Description
3	GP1	Triggered by Keypad_Reset1
		0x1: TRIGGER_RECEIVED
2	PMIC_WD	Triggered by PMIC Watchdog
		0x1: TRIGGER_RECEIVED
1	PS_HOLD	Triggered by PS_HOLD
		0x1: TRIGGER_RECEIVED
0	SOFT	Triggered by Software
		0x1: TRIGGER_RECEIVED

### 0x0000080F PON\_SOFT\_RESET\_REASON2

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: raw xVdd rb

Reasons that the PMIC registers were reset. All zeros mean that no trigger received. Clear the soft reason registers by writing to the SOFT RESET REASON1 register

# PON\_SOFT\_RESET\_REASON2

Bits	Name	Description
4	AFP	Triggered AFP 0x1: TRIGGER_RECEIVED

### 0x00000810 PON\_INT\_RT\_STS

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

**Reset Name:** N/A

Interrupt Real Time Status Bits

#### PON\_INT\_RT\_STS

Bits	Name	Description
7	SOFT_RESET_OCCURED	warning that a reset event has been triggered by the PMIC Watchdog timer  0x0: INT_RT_STATUS_LOW  0x1: INT_RT_STATUS_HIGH

### PON\_INT\_RT\_STS (cont.)

Bits	Name	Description
6	PMIC_WD_BARK	warning that a reset event has been triggered by the PMIC Watchdog timer 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
5	K_R_BARK	warning that a reset event has been triggered by asserting RESIN_N and KPDPWR_N simultaneously 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
4	RESIN_BARK	warning that a reset event has been triggered by RESIN_N 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
3	KPDPWR_BARK	warning that a reset event has been triggered by KPDPWR_N 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
2	CBLPWR_ON	CBLPWR_N has been asserted for longer than his debounce timer 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
1	RESIN_ON	RESIN_N has been asserted for longer than his debounce timer 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
0	KPDPWR_ON	KPDPWR_N has been asserted for longer than his debounce timer 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH

# 0x00000811 PON\_INT\_SET\_TYPE

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: perph\_rb

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### PON\_INT\_SET\_TYPE

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: LEVEL
		0x1: EDGE
6	PMIC_WD_BARK	0x0: LEVEL
		0x1: EDGE

### PON\_INT\_SET\_TYPE (cont.)

Bits	Name	Description
5	K_R_BARK	0x0: LEVEL
		0x1: EDGE
4	RESIN_BARK	0x0: LEVEL
		0x1: EDGE
3	KPDPWR_BARK	0x0: LEVEL
		0x1: EDGE
2	CBLPWR_ON	0x0: LEVEL
		0x1: EDGE
1	RESIN_ON	0x0: LEVEL
		0x1: EDGE
0	KPDPWR_ON	0x0: LEVEL
		0x1: EDGE

# 0x00000812 PON\_INT\_POLARITY\_HIGH

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: perph\_rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

# PON\_INT\_POLARITY\_HIGH

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED
6	PMIC_WD_BARK	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED
5	K_R_BARK	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED
4	RESIN_BARK	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED
3	KPDPWR_BARK	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED
2	CBLPWR_ON	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED
1	RESIN_ON	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

### PON\_INT\_POLARITY\_HIGH (cont.)

Bits	Name	Description
0	KPDPWR_ON	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

### 0x00000813 PON\_INT\_POLARITY\_LOW

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: perph rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

# PON\_INT\_POLARITY\_LOW

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED
6	PMIC_WD_BARK	0x0: LOW_TRIGGER_DISABLED
	2,0	0x1: LOW_TRIGGER_ENABLED
5	K_R_BARK	0x0: LOW_TRIGGER_DISABLED
	3. Ornins	0x1: LOW_TRIGGER_ENABLED
4	RESIN_BARK	0x0: LOW_TRIGGER_DISABLED
	1	0x1: LOW_TRIGGER_ENABLED
3	KPDPWR_BARK	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED
2	CBLPWR_ON	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED
1	RESIN_ON	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED
0	KPDPWR_ON	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

# 0x00000814 PON\_INT\_LATCHED\_CLR

Type: W

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: perph\_rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### PON\_INT\_LATCHED\_CLR

Bits	Name	Description
7	SOFT_RESET_OCCURED	
6	PMIC_WD_BARK	
5	K_R_BARK	
4	RESIN_BARK	
3	KPDPWR_BARK	
2	CBLPWR_ON	2
1	RESIN_ON	
0	KPDPWR_ON	

# 0x00000815 PON\_INT\_EN\_SET

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### PON\_INT\_EN\_SET

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: INT_DISABLED
		0x1: INT_ENABLED
6	PMIC_WD_BARK	0x0: INT_DISABLED
		0x1: INT_ENABLED
5	K_R_BARK	0x0: INT_DISABLED
		0x1: INT_ENABLED
4	RESIN_BARK	0x0: INT_DISABLED
		0x1: INT_ENABLED
3	KPDPWR_BARK	0x0: INT_DISABLED
		0x1: INT_ENABLED
2	CBLPWR_ON	0x0: INT_DISABLED
		0x1: INT_ENABLED

### PON\_INT\_EN\_SET (cont.)

Bits	Name	Description
1	RESIN_ON	0x0: INT_DISABLED
		0x1: INT_ENABLED
0	KPDPWR_ON	0x0: INT_DISABLED
		0x1: INT_ENABLED

# 0x00000816 PON\_INT\_EN\_CLR

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### PON INT EN CLR

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: INT_DISABLED
	3. Chill.	0x1: INT_ENABLED
6	PMIC_WD_BARK	0x0: INT_DISABLED
		0x1: INT_ENABLED
5	K_R_BARK	0x0: INT_DISABLED
		0x1: INT_ENABLED
4	RESIN_BARK	0x0: INT_DISABLED
		0x1: INT_ENABLED
3	KPDPWR_BARK	0x0: INT_DISABLED
		0x1: INT_ENABLED
2	CBLPWR_ON	0x0: INT_DISABLED
		0x1: INT_ENABLED
1	RESIN_ON	0x0: INT_DISABLED
		0x1: INT_ENABLED
0	KPDPWR_ON	0x0: INT_DISABLED
		0x1: INT_ENABLED

# 0x00000818 PON\_INT\_LATCHED\_STS

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: N/A

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### PON\_INT\_LATCHED\_STS

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
6	PMIC_WD_BARK	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
5	K_R_BARK	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
4	RESIN_BARK	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
3	KPDPWR_BARK	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
2	CBLPWR_ON	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
1	RESIN_ON	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED
0	KPDPWR_ON	0x0: NO_INT_RECEIVED 0x1: INTERRUPT_RECEIVED

#### 0x00000819 PON\_INT\_PENDING\_STS

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### PON\_INT\_PENDING\_STS

Bits	Name	Description
7	SOFT_RESET_OCCURED	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

### PON\_INT\_PENDING\_STS (cont.)

Bits	Name	Description
6	PMIC_WD_BARK	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING
5	K_R_BARK	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING
4	RESIN_BARK	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING
3	KPDPWR_BARK	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING
2	CBLPWR_ON	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING
1	RESIN_ON	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING
0	KPDPWR_ON	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING

# 0x0000081A PON\_INT\_MID\_SEL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

### PON\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0
		0x1: MID1
		0x2: MID2
		0x3: MID3

## 0x0000081B PON\_INT\_PRIORITY

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: perph rb

#### PON\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR
		0x1: A

# 0x00000840 PON\_KPDPWR\_N\_RESET\_S1\_TIMER

Type: RW

Clock: pbus\_wrclk
Reset State: 0x0F

Reset Name: dVdd\_rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

# PON\_KPDPWR\_N\_RESET\_S1\_TIMER

	Description
3:0 S1_TIMER	Time that the debounced trigger must be held before bark is sent to MSM  This field can only be updated when block is disabled (i.e. 5 sleep clock cycles after writing 0 to S2_RESET_EN and PON_TRIGGER_EN:KPDPWR_N fields).  0x0: MS_0 0x1: MS_32 0x2: MS_56 0x3: MS_80 0x4: MS_128
	_

# 0x00000841 PON\_KPDPWR\_N\_RESET\_S2\_TIMER

Type: RW

Clock: pbus\_wrclk
Reset State: 0x07

Reset Name: dVdd rb

Stage 2 (bite) configuration

### PON\_KPDPWR\_N\_RESET\_S2\_TIMER

Bits	Name	Description
2:0	S2_TIMER	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s}
		This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field).  0x0: MS_0 0x1: MS_10 0x2: MS_50 0x3: MS_100 0x4: MS_250 0x5: MS_500 0x6: S_1 0x7: S_2

# 0x00000842 PON\_KPDPWR\_N\_RESET\_S2\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x04

Reset Name: dVdd rb

Stage 2 (bite) configuration

#### PON\_KPDPWR\_N\_RESET\_S2\_CTL

Bits	Name	Description
3:0	Name RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field).  0x0: RESERVED0  0x1: WARM_RESET  0x2: IMMEDIATE_XVDD_SHUTDOWN  0x3: RESERVED3  0x4: SHUTDOWN  0x5: DVDD_SHUTDOWN  0x6: XVDD_SHUTDOWN  0x7: HARD_RESET  0x8: DVDD_HARD_RESET  0x9: XVDD_HARD_RESET  0x9: XVDD_HARD_RESET  0xA: WARM_RESET_AND_DVDD_SHUTDOWN  0xB: WARM_RESET_AND_SHUTDOWN  0xC: WARM_RESET_AND_SHUTDOWN  0xC: WARM_RESET_THEN_HARD_RESET
	.0.	0xE: WARM_RESET_THEN_DVDD_HARD_RESET 0xF: WARM_RESET_THEN_XVDD_HARD_RESET

# 0x00000843 PON\_KPDPWR\_N\_RESET\_S2\_CTL2

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: dVdd rb

Stage 2 (bite) configuration

### PON\_KPDPWR\_N\_RESET\_S2\_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable Stage 2 reset
		Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles.  0x0: DISABLED  0x1: ENABLED

## 0x00000844 PON\_RESIN\_N\_RESET\_S1\_TIMER

Type: RW

Clock: pbus\_wrclk Reset State: 0x0F

Reset Name: dVdd rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

### PON\_RESIN\_N\_RESET\_S1\_TIMER

Bits	Name	Description
3:0	S1_TIMER	Time that the debounced trigger must be held before bark is sent to MSM
		This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field).
		0x0: MS_0
		0x1: MS_32
		0x2: MS_56
		0x3: MS_80
		0x4: MS_128
		0x5: MS_184
	- 5	0x6: MS_272
		0x7: MS_408
	2 2 18	0x8: MS_608
	2018-08-01111gt	0x9: MS_904
	7.8 " C.	0xA: MS_1352
	20 5	0xB: MS_2048
	1	0xC: MS_3072
		0xD: MS_4480
		0xE: MS_6720
		0xF: MS_10256

# 0x00000845 PON\_RESIN\_N\_RESET\_S2\_TIMER

Type: RW

Clock: pbus\_wrclk Reset State: 0x07

Reset Name: dVdd\_rb

Stage 2 (bite) configuration

### PON\_RESIN\_N\_RESET\_S2\_TIMER

Bits	Name	Description
2:0	S2_TIMER	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s}
		This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field).  0x0: MS 0
		0x1: MS_10
		0x2: MS_50 0x3: MS_100
		0x4: MS_250 0x5: MS_500
		0x6: S_1
		0x7: S_2

# 0x00000846 PON\_RESIN\_N\_RESET\_S2\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x04

Reset Name: dVdd rb

Stage 2 (bite) configuration

### PON\_RESIN\_N\_RESET\_S2\_CTL

Bits	Name	Description
3:0	RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field).
		0x0: RESERVED0
		0x1: WARM_RESET
		0x2: IMMEDIATE_XVDD_SHUTDOWN
		0x3: RESERVED3
		0x4: SHUTDOWN
		0x5: DVDD_SHUTDOWN
		0x6: XVDD_SHUTDOWN
		0x7: HARD_RESET
		0x8: DVDD_HARD_RESET
		0x9: XVDD_HARD_RESET
		0xA: WARM_RESET_AND_DVDD_SHUTDOWN
		0xB: WARM_RESET_AND_XVDD_SHUTDOWN
		0xC: WARM_RESET_AND_SHUTDOWN
		0xD: WARM_RESET_THEN_HARD_RESET
		0xE: WARM_RESET_THEN_DVDD_HARD_RESET
		0xF: WARM_RESET_THEN_XVDD_HARD_RESET

## 0x00000847 PON\_RESIN\_N\_RESET\_S2\_CTL2

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: dVdd rb

Stage 2 (bite) configuration

#### PON\_RESIN\_N\_RESET\_S2\_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable Stage 2 reset
		Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles.  0x0: DISABLED  0x1: ENABLED

# 0x00000848 PON\_RESIN\_AND\_KPDPWR\_RESET\_S1\_TIMER

Type: RW

Clock: pbus\_wrclk
Reset State: 0x0F

Reset Name: dVdd rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

#### PON\_RESIN\_AND\_KPDPWR\_RESET\_S1\_TIMER

Bits	Name	Description
3:0	S1_TIMER	Time that the debounced trigger must be held before bark is sent to MSM
		This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field).
		0x0: MS_0
		0x1: MS_32
		0x2: MS_56
		0x3: MS_80
		0x4: MS_128 0x5: MS_184
		0x6: MS_184 0x6: MS_272
		0x7: MS 408
		0x8: MS_608
		0x9: MS_904
		0xA: MS_1352
		0xB: MS_2048
		0xC: MS_3072
		0xD: MS_4480
	- 4	0xE: MS_6720
	27	0xF: MS_10256

# 0x00000849 PON\_RESIN\_AND\_KPDPWR\_RESET\_S2\_TIMER

Type: RW

Clock: pbus\_wrclk
Reset State: 0x07

Reset Name: dVdd\_rb

Stage 2 (bite) configuration

#### PON\_RESIN\_AND\_KPDPWR\_RESET\_S2\_TIMER

Bits	Name	Description
2:0	S2_TIMER	Time that debounced trigger must be held before S2 reset occurs {0ms, 10ms, 50ms, 100ms, 250ms, 500ms, 1s, 2s}
		This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field).  0x0: MS 0
		0x1: MS 10
		0x2: MS_50
		0x3: MS_100
		0x4: MS_250
		0x5: MS_500
		0x6: S_1
		0x7: S_2

# 0x0000084A PON\_RESIN\_AND\_KPDPWR\_RESET\_S2\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x04

Reset Name: dVdd rb

Stage 2 (bite) configuration

### PON\_RESIN\_AND\_KPDPWR\_RESET\_S2\_CTL

Bits	Name	Description
3:0	RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field).
		0x0: RESERVED0
		0x1: WARM_RESET
		0x2: RESERVED2
		0x3: RESERVED3
		0x4: RESERVED4
		0x5: RESERVED5
		0x6: RESERVED6
		0x7: HARD_RESET
		0x8: DVDD_HARD_RESET
		0x9: XVDD_HARD_RESET
		0xA: RESERVED10
		0xB: RESERVED11
		0xC: RESERVED12
		0xD: WARM_RESET_THEN_HARD_RESET
		0xE: WARM_RESET_THEN_DVDD_HARD_RESET
		0xF: WARM_RESET_THEN_XVDD_HARD_RESET

# 0x0000084B PON\_RESIN\_AND\_KPDPWR\_RESET\_S2\_CTL2

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: dVdd rb

Stage 2 (bite) configuration

### PON\_RESIN\_AND\_KPDPWR\_RESET\_S2\_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable Stage 2 reset
		Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles.  0x0: DISABLED  0x1: ENABLED

# 0x00000854 PON\_PMIC\_WD\_RESET\_S1\_TIMER

Type: RW

Clock: pbus\_wrclk
Reset State: 0x1F

Reset Name: dVdd rb

Stage 1 (Bark) Timer. Bark cannot be disabled, but interrupt can be disabled if necessary

# PON\_PMIC\_WD\_RESET\_S1\_TIMER

Bits	Name	Description
6:0	S1_TIMER	Time that the debounced trigger must be held before bark is sent to MSM (seconds) 0 - 127 seconds, default 31 seconds.  Program hex value of decimal count desired (not binary coded).
6.0	SI_IIIVIER	to MSM (seconds) 0 - 127 seconds, default 31 seconds.
		0x1C: SEC_28
		0x1D: SEC_29 0x1E: SEC_30
		0x1F: SEC_31
		0x20: SEC_32 0x21: SEC_33
		0x21: SEC_33 0x22: SEC_34
		0x23: SEC_35
		0x24: SEC_36
		0x25: SEC_37 0x26: SEC_38
		0.20. 020_00

# PON\_PMIC\_WD\_RESET\_S1\_TIMER (cont.)

Bits	Name	Description
		0x27: SEC_39
		0x28: SEC_40
		0x29: SEC_41
		0x2A: SEC_42
		0x2B: SEC_43
		0x2C: SEC_44
		0x2D: SEC_45
		0x2E: SEC_46
		0x2F: SEC_47
		0x30: SEC_48
		0x31: SEC_49
		0x32: SEC_50
		0x33: SEC_51
		0x34: SEC_52
		0x35: SEC_53
		0x36: SEC_54
		0x37: SEC_55
		0x38: SEC_56
		0x39: SEC_57
		0x3A: SEC_58
	0,	0x3B: SEC_59
	2,10	0x3C: SEC_60
	2018-08 William	0x3D: SEC_61
	18 Out	0x3E: SEC_62
	30 EM	0x3F: SEC_63
	1	0x40: SEC_64
		0x41: SEC_65 0x42: SEC_66
		0x42: SEC_60 0x43: SEC_67
		0x44: SEC_68
		0x45: SEC_69
		0x46: SEC 70
		0x47: SEC_71
		0x48: SEC_72
		0x49: SEC_73
		0x4A: SEC_74
		0x4B: SEC_75
		0x4C: SEC_76
		0x4D: SEC_77
		0x4E: SEC_78
		0x4F: SEC_79
		0x50: SEC_80
		0x51: SEC_81
		0x52: SEC_82
		0x53: SEC_83
		0x54: SEC_84
		0x55: SEC_85
		0x56: SEC_86
		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

# PON\_PMIC\_WD\_RESET\_S1\_TIMER (cont.)

Bits	Name	Description
		0x57: SEC_87
		0x58: SEC_88
		0x59: SEC_89
		0x5A: SEC_90
		0x5B: SEC_91
		0x5C: SEC_92
		0x5D: SEC_93
		0x5E: SEC_94
		0x5F: SEC_95
		0x60: SEC_96
		0x61: SEC_97
		0x62: SEC_98
		0x63: SEC_99
		0x64: SEC_100
		0x65: SEC_101
	10	0x66: SEC_102
		0x67: SEC_103
		0x68: SEC_104
		0x69: SEC_105
		0x6A: SEC_106
	, , , , ,	0x6B: SEC_107
	2 2	0x6C: SEC_108
	10° in 10°	0x6D: SEC_109
	18. 16. IL	0x6E: SEC_110 0x6F: SEC_111
	Cole on white	0x70: SEC_112
	1	0x71: SEC_113
		0x72: SEC_114
		0x73: SEC_115
		0x74: SEC 116
		0x75: SEC 117
		0x76: SEC_118
		0x77: SEC_119
		0x78: SEC_120
		0x79: SEC_121
		0x7A: SEC_122
		0x7B: SEC_123
		0x7C: SEC_124
		0x7D: SEC_125
		0x7E: SEC_126
		0x7F: SEC_127

#### 0x00000855 PON\_PMIC\_WD\_RESET\_S2\_TIMER

Type: RW

Clock: pbus wrclk Reset State: 0x01

Reset Name: dVdd rb

Stage 2 (bite) configuration



# PON\_PMIC\_WD\_RESET\_S2\_TIMER

Bits	Name	Description
6:0	Name S2_TIMER	Time that debounced trigger must be held before S2 reset occurs - 0 - 127 seconds (default = 32 seconds). Program hex value of decimal count desired (Not binary coded). Timer starts after WD bark expires  This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.  0x0: SEC_0 0x1: SEC_1 0x2: SEC_2 0x3: SEC_3 0x4: SEC_4 0x5: SEC_5 0x6: SEC_6 0x7: SEC_7 0x8: SEC_8
		0x9: SEC_9 0xA: SEC_10 0xB: SEC_11 0xC: SEC_12 0xD: SEC_13 0xE: SEC_14 0xF: SEC_15 0x10: SEC_16 0x11: SEC_17 0x12: SEC_18 0x13: SEC_19 0x14: SEC_20 0x15: SEC_21 0x16: SEC_22 0x17: SEC_23
		0x18: SEC_24 0x19: SEC_25 0x1A: SEC_26 0x1B: SEC_27 0x1C: SEC_28
		0x1D: SEC_29 0x1E: SEC_30 0x1F: SEC_31 0x20: SEC_32 0x21: SEC_33
		0x22: SEC_34 0x23: SEC_35 0x24: SEC_36

# PON\_PMIC\_WD\_RESET\_S2\_TIMER (cont.)

Bits	Name	Description
		0x25: SEC_37
		0x26: SEC_38
		0x27: SEC_39
		0x28: SEC_40
		0x29: SEC_41
		0x2A: SEC_42
		0x2B: SEC_43
		0x2C: SEC_44 0x2D: SEC_45
		0x2E: SEC_46
		0x2E: SEC_40 0x2F: SEC_47
		0x30: SEC_48
		0x31: SEC_49
		0x32: SEC 50
		0x33: SEC_51
		0x34: SEC 52
		0x35: SEC 53
		0x36: SEC_54
	. ( )	0x37: SEC_55
		0x38: SEC_56
	0)	0x39: SEC_57
	2,70	0x3A: SEC_58
	97,01	0x3B: SEC_59
	2018:09 winds	0x3C: SEC_60
	30, 24,	0x3D: SEC_61
	1	0x3E: SEC_62
		0x3F: SEC_63
		0x40: SEC_64
		0x41: SEC_65 0x42: SEC_66
		0x43: SEC_67
		0x44: SEC_68
		0x45: SEC_69
		0x46: SEC_70
		0x47: SEC_71
		0x48: SEC_72
		0x49: SEC_73
		0x4A: SEC_74
		0x4B: SEC_75
		0x4C: SEC_76
		0x4D: SEC_77
		0x4E: SEC_78
		0x4F: SEC_79
		0x50: SEC_80
		0x51: SEC_81
		0x52: SEC_82

# PON\_PMIC\_WD\_RESET\_S2\_TIMER (cont.)

Bits	Name	Description
		0x53: SEC_83
		0x54: SEC_84
		0x55: SEC_85
		0x56: SEC_86
		0x57: SEC_87
		0x58: SEC_88
		0x59: SEC_89
		0x5A: SEC_90
		0x5B: SEC_91
		0x5C: SEC_92 0x5D: SEC_93
		0x5E: SEC_94
		0x5F: SEC_95
		0x60: SEC 96
		0x61: SEC_97
		0x62: SEC 98
		0x63: SEC 99
		0x64: SEC_100
	. ( )	0x65: SEC_101
		0x66: SEC_102
	0)	0x67: SEC_103
	270	0x68: SEC_104
	9 ,01	0x69: SEC_105
	3. Only	0x6A: SEC_106
	2018-09 William	0x6B: SEC_107
	1	0x6C: SEC_108
		0x6D: SEC_109
		0x6E: SEC_110
		0x6F: SEC_111 0x70: SEC_112
		0x71: SEC_112
		0x72: SEC_114
		0x73: SEC_115
		0x74: SEC_116
		0x75: SEC 117
		0x76: SEC 118
		0x77: SEC_119
		0x78: SEC_120
		0x79: SEC_121
		0x7A: SEC_122
		0x7B: SEC_123
		0x7C: SEC_124
		0x7D: SEC_125
		0x7E: SEC_126
		0x7F: SEC_127

## 0x00000856 PON\_PMIC\_WD\_RESET\_S2\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x06

Reset Name: dVdd rb

Stage 2 (bite) configuration. This register can only be written when PMIC\_WD\_LOCK field is 0x0.

#### PON\_PMIC\_WD\_RESET\_S2\_CTL

Bits	Name	Description
3:0	RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field).
		0x0: RESERVED0
		0x1: WARM_RESET
		0x2: IMMEDIATE_XVDD_SHUTDOWN
		0x3: RESERVED3
		0x4: SHUTDOWN
		0x5: DVDD_SHUTDOWN
		0x6: XVDD_SHUTDOWN
	5	0x7: HARD_RESET
		0x8: DVDD_HARD_RESET
	0, 48	0x9: XVDD_HARD_RESET
	.O. ville	0xA: WARM_RESET_AND_DVDD_SHUTDOWN
	75 400	0xB: WARM_RESET_AND_XVDD_SHUTDOWN
	2.5	0xC: WARM_RESET_AND_SHUTDOWN
	1	0xD: WARM_RESET_THEN_HARD_RESET
		0xE: WARM_RESET_THEN_DVDD_HARD_RESET
		0xF: WARM_RESET_THEN_XVDD_HARD_RESET

### 0x00000857 PON\_PMIC\_WD\_RESET\_S2\_CTL2

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: dVdd rb

Stage 2 (bite) configuration. This register can only be written when PMIC\_WD\_LOCK field is

0x0.

#### PON\_PMIC\_WD\_RESET\_S2\_CTL2

Bits	Name	Description	
7	S2_RESET_EN	Enable Stage 2 reset	
		Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles.  0x0: DISABLED  0x1: ENABLED	
PON_PMIC_WD_RESET_PET			
Type: W Clock: pbus_wrclk Reset State: 0x00			
Reset I	Reset Name: dVdd_rb		
Stage 2 (bite) configuration			
PON_F	PON_PMIC_WD_RESET_PET		
Bits	Name	Description	

#### 0x00000858 PON\_PMIC\_WD\_RESET\_PET

#### PON\_PMIC\_WD\_RESET\_PET

Bits	Name	Description
0	WATCHDOG_PET	Writing '1' to this bit will clear the PMIC WD timer. Writing '0' has no effect.
	***	This is a synchronized field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.  0x1: PET_WD

# 0x0000085A PON\_PS\_HOLD\_RESET\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x04

Reset Name: dVdd\_rb

#### PON\_PS\_HOLD\_RESET\_CTL

Bits	Name	Description
3:0	RESET_TYPE	This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 8 sleep clock cycles.  0x0: RESERVED0 0x1: WARM_RESET 0x2: IMMEDIATE_XVDD_SHUTDOWN 0x3: RESERVED3 0x4: SHUTDOWN 0x5: DVDD_SHUTDOWN 0x6: XVDD_SHUTDOWN 0x7: HARD_RESET 0x8: DVDD_HARD_RESET 0x9: XVDD_HARD_RESET 0x9: XVDD_HARD_RESET 0x0: WARM_RESET_AND_DVDD_SHUTDOWN 0xC: WARM_RESET_AND_SHUTDOWN 0xC: WARM_RESET_AND_SHUTDOWN 0xC: WARM_RESET_THEN_HARD_RESET 0xE: WARM_RESET_THEN_DVDD_HARD_RESET 0xF: WARM_RESET_THEN_DVDD_HARD_RESET
		V 10

# 0x0000085B PON\_PS\_HOLD\_RESET\_CTL2

Type: RW

Clock: pbus\_wrclk
Reset State: 0x80

Reset Name: dVdd rb

### PON\_PS\_HOLD\_RESET\_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable reset  Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles.
		0x0: DISABLED
		0x1: ENABLED

# 0x00000862 PON\_SW\_RESET\_S2\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: dVdd rb

Software initiated shutdown (AFP)

### PON\_SW\_RESET\_S2\_CTL

Bits	Name	Description
3:0	RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to SW_RESET_EN field).
		0x0: SOFT_RESET
		0x1: WARM_RESET
		0x2: IMMEDIATE_XVDD_SHUTDOWN
		0x3: RESERVED3
		0x4: SHUTDOWN
		0x5: DVDD_SHUTDOWN
		0x6: XVDD_SHUTDOWN
		0x7: HARD_RESET
	200	0x8: DVDD_HARD_RESET
	2	0x9: XVDD_HARD_RESET
	a grade	0xA: WARM_RESET_AND_DVDD_SHUTDOWN
	C.O. willis	0xB: WARM_RESET_AND_XVDD_SHUTDOWN
	O. P. M. C.	0xC: WARM_RESET_AND_SHUTDOWN
	2,5	0xD: WARM_RESET_THEN_HARD_RESET
	1	0xE: WARM_RESET_THEN_DVDD_HARD_RESET
		0xF: WARM_RESET_THEN_XVDD_HARD_RESET

# 0x00000863 PON\_SW\_RESET\_S2\_CTL2

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: dVdd\_rb

Software initiated shutdown (AFP)

#### PON\_SW\_RESET\_S2\_CTL2

Bits	Name	Description
7	SW_RESET_EN	Enable SW reset
		Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles.  0x0: DISABLED  0x1: ENABLED

#### 0x00000864 PON\_SW\_RESET\_GO

Type: W

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: dVdd\_rb

Initiate SW Reset by writing 0xA5 to this register

#### PON\_SW\_RESET\_GO

Bits	Name	Description
7:0	SW_RESET_GO	Initiate SW Reset by writing 0xA5 to this register
	50, 2m	This is a synchronized field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.

### 0x00000866 PON\_OVERTEMP\_RESET\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x04

Reset Name: dVdd\_rb

Over temperature stage 3 plus charger FLCB stage 2 reset/shutdown control.

Note: For safety reasons, only shutdown and hard reset events are supported by the overtemp reset trigger.

# PON\_OVERTEMP\_RESET\_CTL

Bits	Name	Description
3:0	Name RESET_TYPE	This field can only be updated when block is disabled (i.e. 8 sleep clock cycles after writing 0 to S2_RESET_EN field).  0x0: RESERVED0  0x1: RESERVED1  0x2: IMMEDIATE_XVDD_SHUTDOWN  0x3: RESERVED3  0x4: SHUTDOWN  0x5: DVDD_SHUTDOWN  0x6: XVDD_SHUTDOWN  0x7: HARD_RESET  0x8: DVDD_HARD_RESET  0x9: XVDD_HARD_RESET  0x0: RESERVED10  0xB: RESERVED11  0xC: RESERVED12  0xD: RESERVED13
	,0,	0xE: RESERVED14 0xF: RESERVED15

# 0x00000867 PON\_OVERTEMP\_RESET\_CTL2

Type: RW

Clock: pbus\_wrclk
Reset State: 0x80

Reset Name: dVdd rb

Over temperature stage 3 plus charger FLCB stage 2 reset/shutdown control.

# PON\_OVERTEMP\_RESET\_CTL2

Bits	Name	Description
7	S2_RESET_EN	Enable stage 2 reset
		Field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles.  0x0: DISABLED  0x1: ENABLED

#### PON\_PULL\_CTL 0x00000870

Type: RW

Clock: pbus\_wrclk **Reset State:** 0x0F

**Reset Name:** soft\_dVdd\_rb

### PON\_PULL\_CTL

Bits	Name	Description
3	PON1_PD_EN	0x0: PD_DISABLED
		0x1: PD_ENABLED
2	CBLPWR_N_PU_EN	0x0: PD_DISABLED
		0x1: PD_ENABLED
1	KPDPWR_N_PU_EN	0x0: PD_DISABLED
		0x1: PD_ENABLED
0	RESIN_N_PU_EN	0x0: PD_DISABLED
		0x1: PD_ENABLED
PON_DEBOUNCE_CTL  Type: RW Clock: pbus_wrclk Reset State: 0x00  Reset Name: dVdd_rb		

#### 0x00000871

# PON\_DEBOUNCE\_CTL

Bits	Name	Description
5:3	WIPWR_DEBOUNCE	PON_1: Time delay for general purpose input de-bouncing during wireless charger power on sequences (i.e. PON_1 input signal and WIPWR_DEBOUNCE_DLY field asserted). Only signal assertion is de-bounced.
		if $X = 0$ then delay = 0, else delay = (1/1024) seconds * 2 ^(X-1) where $X = $ value of bits <2:0>
		This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.  0x0: IMMEDIATE 0x1: MSEC_0P98 0x2: MSEC_1P95 0x3: MSEC_3P91 0x4: MSEC_7P81 0x5: MSEC_15P63 0x6: MSEC_31P25 0x7: MSEC_62P5
2:0	DEBOUNCE	KPD/CBL/GP_DLY/RESIN/RESIN_AND_KPD/GP1/GP2: Time delay for KPD, CBL, General Purpose PON, RESIN, RESIN_AND_KPD, GP1 and GP2 state change interrupt and triggering. Delay = (1/1024)* 2^ (x+4)  This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.  0x0: MS_15P6 0x1: MS_31P2 0x2: MS_62P5 0x3: MS_125 0x4: MS_250 0x5: MS_500 0x6: MS_1000 0x7: MS_2000

# 0x00000874 PON\_RESET\_S3\_SRC

Type: RW

Clock: pbus\_wrclk
Reset State: 0x03

Reset Name: dVdd\_rb

Choose source for stage 3 (Full Complete Shutdown). This is a write once register.

PMIC\_WRITE\_ONCE

#### PON\_RESET\_S3\_SRC

Bits	Name	Description
1:0	RESET_S3_SOURCE	00=KPDPWR_N, 01=RESIN_N, 10=(KPDPWR_N and RESIN_N both need to be asserted, 11=either KPDPWR_N or RESIN_N)
		This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.
		For devices with dVdd_rb trim copy feature shadow register is loaded by writes to this or it's corresponding trim register field.
		0x0: KPDPWR_N
		0x1: RESIN_N
		0x2: KPDPWR_AND_RESIN
		0x3: KPDPWR_OR_RESIN

### 0x00000875 PON\_RESET\_S3\_TIMER

Type: RW

Clock: pbus\_wrclk
Reset State: 0x04

Reset Name: dVdd\_rb

Time trigger must be held before S3 reset occurs (seconds)

PMIC\_LOCKED=SEC\_ACCESS

#### PON\_RESET\_S3\_TIMER

Bits	Name	Description
2:0	S3_TIMER	Time trigger must be held before S3 reset occurs.
		000 = Instant, else 2 <sup>(x)</sup> seconds (2 to 128) for 50kHz LFRC
		F., 2011, 15D0
		For 32kHz LFRC
		0 = instant
		1 = 3.1s
		2 = 6.1s
		3 = 12.2s
		4 = 24.2s
		5 = 48.8s
		6 = 97.7s
		7 = 195.3s
		This is a shadowed field so, for reliable hardware operation, the
		minimum time allowed between write operations is 5 sleep clock
		cycles.
		0x0: IMMEDIATE
	. ( )	0x1: SEC_2
		0x2: SEC_4
	0	0x3: SEC_8
	25	0x4: SEC_16
	3° 10°	0x5: SEC_32
	O. O. William	0x6: SEC_64
	OFENE	0x7: SEC_128

# 0x00000880 PON\_PON\_TRIGGER\_EN

Type: RW

Clock: pbus\_wrclk Reset State: 0xFE

**Reset Name:** soft\_dVdd\_rb

Power on trigger enables.

Each field is synchronized by a 2-stage shift register so, for reliable hardware operation, the minimum time allowed between write operations is 3 sleep clock cycles.

### PON\_PON\_TRIGGER\_EN

Bits	Name	Description
7	KPDPWR_N	Enable PON trigger for new KPDPWR press 0x0: DISABLED 0x1: ENABLED

### PON\_PON\_TRIGGER\_EN (cont.)

Bits	Name	Description
6	CBLPWR_N	Enable PON trigger for CBL_PWR_N 0x0: DISABLED 0x1: ENABLED
5	PON1	Enable PON trigger for PON1 0x0: DISABLED 0x1: ENABLED
4	USB_CHG	Enable PON trigger for USB CHG 0x0: DISABLED 0x1: ENABLED
3	DC_CHG	Enable PON trigger for DC CHG 0x0: DISABLED 0x1: ENABLED
2	RTC	Enable PON trigger for RTC 0x0: DISABLED 0x1: ENABLED
1	SMPL	Enable PON trigger for SMPL 0x0: DISABLED 0x1: ENABLED

# 0x00000883 PON\_WATCHDOG\_LOCK

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: shutdown2\_rb

Write Once register that is reset at the end of the shutdown sequence

PMIC\_WRITE\_ONCE

### PON\_WATCHDOG\_LOCK

Bits	Name	Description
7	PMIC_WD_LOCK	This is a write once register. '1' then PMIC_WD_RESET_S2_CTL is locked and the contents can no longer be modified. If '0' the register is programmable.  0x0: WD_UNLOCKED  0x1: WD_LOCKED

#### PON\_UVLO 0x00000888

**Type:** RW

Clock: pbus\_wrclk Reset State: 0x1D

Reset Name: soft\_dVdd\_rb

**UVLO** Delay

## PON\_UVLO

Bits	Name	Description
5:3	WIPWR_UVLO_DLY	Time delay for UVLO detection de-bouncing during wireless charger power on sequences (i.e. PON_1 input signal and WIPWR_DEBOUNCE_DLY field asserted). Only signal assertion is de-bounced.
	(	if $X = 0$ then delay = 0, else delay = (1/1024) seconds * 2 ^(X-1) where $X = $ value of bits <2:0>
	(0)	This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.
		0x0: IMMEDIATE
	27	0x1: MSEC_0P98
	2018-09-22 THE SWEWINGTON	0x2: MSEC_1P95
	18, 16 m	0x3: MSEC_3P91 0x4: MSEC_7P81
	50, 24	0x5: MSEC_15P63
	1	0x6: MSEC 31P25
		0x7: MSEC_62P5
2:0	UVLO_DLY	Time delay for UVLO detection.
		if $X = 0$ then delay = 0, else delay = (1/1024) seconds * 2 ^(X-1) where $X = $ value of bits <2:0>
		This is a shadowed field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.
		0x0: IMMEDIATE
		0x1: MSEC_0P98
		0x2: MSEC_1P95
		0x3: MSEC_3P91
		0x4: MSEC_7P81 0x5: MSEC_15P63
		0x6: MSEC_15F65 0x6: MSEC_31P25
		0x7: MSEC_62P5

## 0x0000088A PON\_AVDD\_VPH

Type: RW

Clock: pbus\_wrclk
Reset State: 0x30

Reset Name: perph rb

Control for AVDD

## PON\_AVDD\_VPH

Bits	Name	Description
5	AVDD_HPM_EN	1' = Enable LDO HPM, '0' = LDO LPM
		0x0: LPM
		0x1: HPM
4	AVDD_REF_OVR	aVdd regulator Reference Adjust Override
	.\(	0 - aVdd regulator switches it's voltage reference to the PMIC MBG when MBG_OK = 1. If MBG_OK = 0, aVdd regulator uses the internal PON mini-bg as a voltage reference
	.0	1 - aVdd regulator always uses the internal PON mini-bg as a voltage reference
		0x0: AUTO
	.03	0x1: FORCE_MINI_BG

## 0x00000890 PON\_PON1\_INTERFACE

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: shutdown2\_rb

PON module interface signaling.

## PON\_PON1\_INTERFACE

Bits	Name	Description
7	PON_OUT	Field drives primary PMIC PON output buffer input.  0x0: LOW
		OXO. LOVV
		0x1: HIGH

## 0x00000891 PON\_PBS\_INTERFACE

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: shutdown2 rb

PON module interface signaling.

## PON\_PBS\_INTERFACE

Bits	Name	Description
6	ACK_NACK	write 0x01 to ACK the PON module, write 0x00 to NACK the PON module. A NACK will cause the PMIC to shutdown.
		This is a synchronized field so, for reliable hardware operation, the minimum time allowed between write operations is 5 sleep clock cycles.  0x0: NACK 0x1: ACK
	2018.09.21.01. 2018.5m@mirdte	OZ.Z.

# 7 Misc\_PM8937 Registers

## 0x00000900 MISC\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

## MISC\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00000901 MISC\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

## MISC\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x00000902 MISC\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### MISC\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00000903 MISC REVISION4

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### MISC\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00000904 MISC\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x14

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

## MISC\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	

## 0x00000905 MISC\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x22

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### MISC PERPH SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	02.0

## 0x0000094A MISC\_TX\_GTR\_THRES\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### MISC\_TX\_GTR\_THRES\_CTL

Bits	Name	Description
7	TX_GTR_THRES_REG	A signal sent by modem to indicate that a high power GSM transmit is about to happen (~100us before PA on ramp starts). It is de-asserted when the Tx transmit is over.  0x1: GSM_TRANSMIT  0x0: TRANSMIT_OVER

## 0x000009D0 MISC\_SEC\_ACCESS

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: dVdd rb

#### PMIC LOCKING

## MISC\_SEC\_ACCESS

Bits	Name	Description
7:0	SEC_UNLOCK	Unlock the Secure Registers by writing 0xA5 to this register. Lock is rearmed after the next write to the module.



# 8 Vref\_lpddr Registers

## 0x00000A00 VREFLPDDR\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

## VREFLPDDR\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00000A01 VREFLPDDR\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC\_CONSTANT

## VREFLPDDR\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x00000A02 VREFLPDDR\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [23:16]

#### VREFLPDDR\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00000A03 VREFLPDDR\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

## VREFLPDDR\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00000A04 VREFLPDDR\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x14

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

## VREFLPDDR\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0x14: MISC

## 0x00000A05 VREFLPDDR\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x06

Reset Name: N/A

Peripheral SubType

PMIC\_CONSTANT

## VREFLPDDR\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x6: VREF_LPDDR2

## 0x00000A08 VREFLPDDR\_STATUS1

Type: R

Clock: PBUS\_WRCLK

**Reset State:** 0x00

Reset Name: N/A

**Status Registers** 

## VREFLPDDR\_STATUS1

Bits	Name	Description
7	VREF_OK	0 = VREF_LPDDR2_PERPH_EN is low
		1 = VREF_LPDDR2_PERPH_EN is high
6	VREF_LPDDR_OK	0 = VREF is disabled
		1 = VREF is enabled
		(PERPH_EN & (REF_EN   (FWE2 & HE2)   (FWE1 & HE2)))

## 0x00000A44 VREFLPDDR\_VREF\_LPDDR2\_EN

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH RB

If any of the conditions below are true, the block is on provided that the PERPH EN is set

## VREFLPDDR\_VREF\_LPDDR2\_EN

Bits	Name	Description
7	REF_EN	Enable the reference.
1	FOLLOW_HW_EN2	Enable the reference if the external HW_EN is set (Typically connects to sleep_b)
0	FOLLOW_HW_EN1	Enable the reference if the external HW_EN is set (Typically connects to VREG_OK from LPDDR regulator)

## 0x00000A46 VREFLPDDR EN CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

## VREFLPDDR\_EN\_CTL1

Bits	Name	Description
7	PERPH_EN	LPDDR Reference Enable
		0 = Block is forcefully shut down
		1 = Reference state is controlled by individual enable controls

# 9 Bua\_ext\_charger Registers

## 0x00001C00 BUA\_EXT\_CHARGER\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

## BUA\_EXT\_CHARGER\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00001C01 BUA\_EXT\_CHARGER\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

#### BUA\_EXT\_CHARGER\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x00001C04 BUA\_EXT\_CHARGER\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x1E Reset Name: N/A

Peripheral Type

#### BUA\_EXT\_CHARGER\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0x1E: BATT_ALARM

## 0x00001C05 BUA\_EXT\_CHARGER\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x04
Reset Name: N/A
Peripheral SubType

## BUA\_EXT\_CHARGER\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x1: BUA
		0x2: BUA_NO_CHARGER
		0x3: BUA_4UICC
		0x4: BUA_EXT_CHARGER
		0x5: BUA_BATT_ALARM
		0x6: BUA_4UICC_DUAL_BATT_ALARM

## 0x00001C08 BUA\_EXT\_CHARGER\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Status Registers

## **BUA\_EXT\_CHARGER\_STATUS1**

Bits	Name	Description
7	BUA_OK	0 = BUA is disabled 1 = BUA is enabled
		0x1: BUA_ENABLED 0x0: BUA_DISABLED
6	BATT_GONE_DETECTED	0 = BATT_GONE is low 1 = BATT_GONE is high. External charger detected battery is gone. 0x1: BATT_GONE 0x0: BAT_PRESENT

## 0x00001C09 BUA\_EXT\_CHARGER\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Status Registers

## BUA\_EXT\_CHARGER\_STATUS2

Bits	Name	Description
3	UICC4_ALARM_DETECTED	0 = UICC4 Alarm Off 1 = UICC4 Alarm Received 0x1: ALARM_DETECTED 0x0: ALARM_NOT_DETECTED
2	UICC3_ALARM_DETECTED	0 = UICC3 Alarm Off 1 = UICC3 Alarm Received 0x1: ALARM_DETECTED 0x0: ALARM_NOT_DETECTED
1	UICC2_ALARM_DETECTED	0 = UICC2 Alarm Off 1 = UICC2Alarm Received 0x1: ALARM_DETECTED 0x0: ALARM_NOT_DETECTED
0	UICC1_ALARM_DETECTED	0 = UICC1 Alarm Off 1 = UICC1 Alarm Received 0x1: ALARM_DETECTED 0x0: ALARM_NOT_DETECTED

## 0x00001C10 BUA\_EXT\_CHARGER\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Interrupt Real Time Status Bits

## BUA\_EXT\_CHARGER\_INT\_RT\_STS

Bits	Name	Description
4	UICC4_ALARM_STS	0 = No Event 1 = UICC4 Alarm Received and LDO reset 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
3	UICC3_ALARM_STS	0 = No Event 1 = UICC3 Alarm Received and LDO reset 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
2	UICC2_ALARM_STS	0 = No Event 1 = UICC2 Alarm Received and LDO reset 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
1	UICC1_ALARM_STS	0 = No Event 1 = UICC1 Alarm Received and LDO reset 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH
0	BATT_ALARM_STS	0 = Battery Alarm Off 1 = Battery Alarm On (Battery has been removed) 0x0: INT_RT_STATUS_LOW 0x1: INT_RT_STATUS_HIGH

## 0x00001C11 BUA\_EXT\_CHARGER\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## BUA\_EXT\_CHARGER\_INT\_SET\_TYPE

Bits	Name	Description
4	UICC4_ALARM_TYPE	0x0: LEVEL
		0x1: EDGE
3	UICC3_ALARM_TYPE	0x0: LEVEL
		0x1: EDGE
2	UICC2_ALARM_TYPE	0x0: LEVEL
		0x1: EDGE
1	UICC1_ALARM_TYPE	0x0: LEVEL
		0x1: EDGE
0	BATT_ALARM_TYPE	0x0: LEVEL
		0x1: EDGE

## 0x00001C12 BUA\_EXT\_CHARGER\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

## BUA\_EXT\_CHARGER\_INT\_POLARITY\_HIGH

Bits	Name	Description
4	UICC4_ALARM_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED
3	UICC3_ALARM_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED
2	UICC2_ALARM_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED
1	UICC1_ALARM_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED
0	BATT_ALARM_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

## 0x00001C13 BUA\_EXT\_CHARGER\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

## BUA\_EXT\_CHARGER\_INT\_POLARITY\_LOW

Bits	Name	Description
4	UICC4_ALARM_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED
3	UICC3_ALARM_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED
2	UICC2_ALARM_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED
1	UICC1_ALARM_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED
0	BATT_ALARM_LOW	0x0: LOW_TRIGGER_DISABLED
	2,7	0x1: LOW_TRIGGER_ENABLED

## 0x00001C14 BUA\_EXT\_CHARGER\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

## BUA\_EXT\_CHARGER\_INT\_LATCHED\_CLR

Bits	Name	Description
4	UICC4_ALARM_LATCHED_ CLR	
3	UICC3_ALARM_LATCHED_ CLR	
2	UICC2_ALARM_LATCHED_ CLR	
1	UICC1_ALARM_LATCHED_ CLR	

#### BUA\_EXT\_CHARGER\_INT\_LATCHED\_CLR (cont.)

Bits	Name	Description
0	BATT_ALARM_LATCHED_C LR	

## 0x00001C15 BUA\_EXT\_CHARGER\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### **BUA EXT CHARGER INT EN SET**

Bits	Name	Description
4	UICC4_ALARM_EN_SET	0x0: INT_DISABLED
	2,0	0x1: INT_ENABLED
3	UICC3_ALARM_EN_SET	0x0: INT_DISABLED
	8. Orning	0x1: INT_ENABLED
2	UICC2_ALARM_EN_SET	0x0: INT_DISABLED
	1	0x1: INT_ENABLED
1	UICC1_ALARM_EN_SET	0x0: INT_DISABLED
		0x1: INT_ENABLED
0	BATT_ALARM_EN_SET	0x0: INT_DISABLED
		0x1: INT_ENABLED

## 0x00001C16 BUA\_EXT\_CHARGER\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

## BUA\_EXT\_CHARGER\_INT\_EN\_CLR

Bits	Name	Description
4	UICC4_ALARM_EN_CLR	0x0: INT_DISABLED
		0x1: INT_ENABLED
3	UICC3_ALARM_EN_CLR	0x0: INT_DISABLED
		0x1: INT_ENABLED
2	UICC2_ALARM_EN_CLR	0x0: INT_DISABLED
		0x1: INT_ENABLED
1	UICC1_ALARM_EN_CLR	0x0: INT_DISABLED
		0x1: INT_ENABLED
0	BATT_ALARM_EN_CLR	0x0: INT_DISABLED
		0x1: INT_ENABLED

## 0x00001C18 BUA EXT CHARGER INT LATCHED STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

## BUA\_EXT\_CHARGER\_INT\_LATCHED\_STS

Bits	Name	Description
4	UICC4_ALARM_LATCHED_ STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
3	UICC3_ALARM_LATCHED_ STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
2	UICC2_ALARM_LATCHED_ STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
1	UICC1_ALARM_LATCHED_ STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED
0	BATT_ALARM_LATCHED_S TS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

## 0x00001C19 BUA\_EXT\_CHARGER\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Pending is set if interrupt has been sent but not cleared.

## BUA\_EXT\_CHARGER\_INT\_PENDING\_STS

Bits	Name	Description
4	UICC4_ALARM_PENDING_ STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
3	UICC3_ALARM_PENDING_ STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
2	UICC2_ALARM_PENDING_ STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
1	UICC1_ALARM_PENDING_ STS	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING
0	BATT_ALARMPENDING_ST S	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

## 0x00001C1A BUA\_EXT\_CHARGER\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

## BUA\_EXT\_CHARGER\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0
		0x1: MID1
		0x2: MID2
		0x3: MID3

## 0x00001C1B BUA\_EXT\_CHARGER\_INT\_PRIORITY

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

SR=0 A=1

## BUA\_EXT\_CHARGER\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR 0x1: A

## 0x00001C40 BUA\_EXT\_CHARGER\_BUA\_CTL1

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x16

Reset Name: PERPH RB

**TBD** 

## BUA\_EXT\_CHARGER\_BUA\_CTL1

Bits	Name	Description
7	BAT_GONE_SEL	0' = Battery alarm from BATT_GONE (GPIO) pin; '1' = Battery alarm from bidirectional BUA (GPIO) pin,'FROM_BAT_GONE_GPIO=0,FROM_BUA_GPIO=1',RTL_RI FO=BUA_CTL1_BAT_GONE_SEL_rifo,'

## **BUA\_EXT\_CHARGER\_BUA\_CTL1** (cont.)

Bits	Name	Description
6:4	BATT_RMV_DEB	BAT_GONE debounce timer
		3'b000: 0-1 sclk
		3'b001: 1-2 sclk (default)
		3'b010: 2-3 sclk
		3'b011: 5-6 sclk
		3'b100: 8-9 sclk
		3'b101: 11-12 sclk
		3'b110: 15-16 sclk
		3'b111: 31-32 sclk
		0x0: SCLK_0_TO_1
		0x1: SCLK_1_TO_2
		0x2: SCLK_2_TO_3
		0x3: SCLK_5_TO_6
		0x4: SCLK_8_TO_9
		0x5: SCLK_11_TO_12
	<b>\</b> (	0x6: SCLK_15_TO_16
		0x7: SCLK_31_TO_32
2:0	LDO_SHUTDOWN_DELAY	Programmable delay between Battery removal and start of UICC LDO reset
		3b000 = 2.5 sclk (~76us)
	0,	3b001 = 3.5 sclk (~107us)
	2,0	3b010 = 4.5 sclk (~137us)
	2013:09 swindy	3b011 = 5.5 sclk (~168us)
	S. Out	3b100 = 7.5 sclk (~229us)
	30, 2M	3b101 = 8.5 sclk (~259us)
	1	3b110 = 9.5 sclk (~290us) (default)
		3b111 = 11.5 sclk (~351us)
		0x0: SCLK2P5
		0x1: SCLK3P5
		0x2: SCLK4P5
		0x3: SCLK5P5
		0x4: SCLK6P5
		0x5: SCLK8P5
		0x6: SCLK9P5
		0x7: SCLK11P5

## 0x00001C46 BUA\_EXT\_CHARGER\_EN\_CTL1

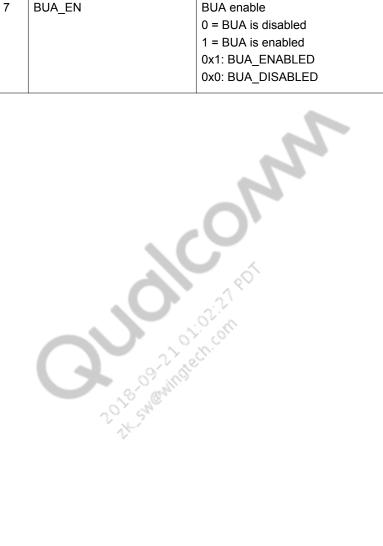
Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

## BUA\_EXT\_CHARGER\_EN\_CTL1

Bits	Name	Description
7	BUA_EN	BUA enable
		0 = BUA is disabled
		1 = BUA is enabled
		0x1: BUA_ENABLED
		0x0: BUA_DISABLED



# 10 Temp\_alarm Registers

## 0x00002400 TEMP\_ALARM\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

## TEMP\_ALARM\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00002401 TEMP\_ALARM\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

#### TEMP\_ALARM\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x00002402 TEMP\_ALARM\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### TEMP\_ALARM\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00002403 TEMP ALARM REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### TEMP\_ALARM\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00002404 TEMP\_ALARM\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x09

Reset Name: N/A

Peripheral Type

#### TEMP\_ALARM\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0x9: ALARM

## 0x00002405 TEMP\_ALARM\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x08

**Reset Name:** N/A

Peripheral SubType

## TEMP\_ALARM\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x8: TEMP_ALARM

## 0x00002408 TEMP\_ALARM\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Status Registers

## **TEMP ALARM STATUS1**

Bits	Name	Description
7	TEMP_ALARM_OK	1: TEMP ALARM enabled 0: TEMP ALARM disabled 0x0: TEMP_ALARM_DISABLED 0x1: TEMP_ALARM_ENABLED
3	ST3_SHUTDOWN_STS	Writing 1 to ST3_SHUTDOWN_CLR clears this bit 0x0: NO_EVENT 0x1: ST3_EVENT_OCCURRED
2	ST2_SHUTDOWN_STS	Writing 1 to ST2_SHUTDOWN_CLR clears this bit 0x0: NO_EVENT 0x1: ST2_EVENT_OCCURRED
1:0	TEMP_ALARM_FSM_STATE	TEMP_ALARM_FSM_STATE  0x0: STAGE_0  0x1: STAGE_1  0x2: STAGE_2  0x3: STAGE_3

## 0x00002410 TEMP\_ALARM\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

**Interrupt Real Time Status Bits** 

#### TEMP\_ALARM\_INT\_RT\_STS

Bits	Name	Description
0	TEMP_ALARM_RT_STS	0x0: INT_RT_STATUS_LOW
		0x1: INT_RT_STATUS_HIGH

## 0x00002411 TEMP ALARM INT SET TYPE

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### TEMP\_ALARM\_INT\_SET\_TYPE

Bits	Name	Description
0	TEMP_ALARM_TYPE	0x0: LEVEL
		0x1: EDGE

## 0x00002412 TEMP\_ALARM\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

## TEMP\_ALARM\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	TEMP_ALARM_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

## 0x00002413 TEMP\_ALARM\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

#### TEMP\_ALARM\_INT\_POLARITY\_LOW

E	Bits	Name	Description
	0	TEMP_ALARM_LOW	0x0: LOW_TRIGGER_DISABLED
			0x1: LOW_TRIGGER_ENABLED

## 0x00002414 TEMP\_ALARM\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

writing a 1 to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

## TEMP\_ALARM\_INT\_LATCHED\_CLR

Bits	Name	Description
0	TEMP_ALARM_LATCHED_ CLR	

## 0x00002415 TEMP\_ALARM\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing 0 to this register has no effect. Writing a 1 will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

## TEMP\_ALARM\_INT\_EN\_SET

Bits	Name	Description
0	TEMP_ALARM_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED

## 0x00002416 TEMP\_ALARM\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

writing 0 to this register has no effect. Writing a 1 will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### TEMP ALARM INT EN CLR

Bits	Name	Description
0	TEMP_ALARM_EN_CLR	0x0: INT_DISABLED
	97,018	0x1: INT_ENABLED

## 0x00002418 TEMP\_ALARM\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Debug: Latched (Sticky) Interrupt. 1 indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

## TEMP\_ALARM\_INT\_LATCHED\_STS

Bits	Name	Description
0	TEMP_ALARM_LATCHED_ STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

## 0x00002419 TEMP\_ALARM\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### TEMP\_ALARM\_INT\_PENDING\_STS

Bits	Name	Description
0		0x0: NO_INT_PENDING
	TS	0x1: INTERRUPT_PENDING

## 0x0000241A TEMP ALARM INT MID SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

## TEMP\_ALARM\_INT\_MID\_SEL

Name	Description
NT_MID_SEL	0x0: MID0
	0x1: MID1
	0x2: MID2
	0x3: MID3
V	· · V

## 0x0000241B TEMP\_ALARM\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

## TEMP\_ALARM\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR
		0x1: A

## 0x00002440 TEMP\_ALARM\_SHUTDOWN\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

## TEMP\_ALARM\_SHUTDOWN\_CTL1

Bits	Name	Description
7	OVRD_ST3_EN	OVRD_ST3_EN : Override automatic shutdown in stage 3 0x0: NO_OVERRIDE 0x1: OVERTEMP_SHUTDOWN_BLOCKED
6	OVRD_ST2_EN	OVRD_ST2_EN: Override partial automatic shutdown in stage 2 0x0: NO_OVERRIDE 0x1: OVERTEMP_SHUTDOWN_BLOCKED
1:0	TEMP_THRESH_CNTRL	TEMP_THRESH_CNTRL: THRESH_STAGE1_STAGE2_STAGE3 0x0: THRESH_105C_125C_145C 0x1: THRESH_110C_130C_150C 0x2: THRESH_115C_135C_155C 0x3: THRESH_120C_140C_160C

## 0x00002442 TEMP\_ALARM\_SHUTDOWN\_CTL2

Type: W

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

#### TEMP\_ALARM\_SHUTDOWN\_CTL2

Bits	Name	Description
7	ST3_SHUTDOWN_CLR	writing 1 clears ST3_SHUTDOWN_STS bit
6	ST2_SHUTDOWN_CLR	writing 1 clears ST2_SHUTDOWN_STS bit

## 0x00002446 TEMP\_ALARM\_EN\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

## TEMP\_ALARM\_EN\_CTL1

Bits	Name	Description
7	TEMP_ALARM_EN	0x0: TEMP_ALARM_DISABLED
		0x1: TEMP_ALARM_FORCED_ON
0	FOLLOW_TEMP_ALARM_H W_EN	0x0: TEMP_ALARM_DISABLED 0x1: TEMP_ALARM_FOLLOWS_HW_EN



# **Coincell Registers**

#### 0x00002800 COIN\_REVISION1

COIN	_REVISION1		
Clock: Reset S	Type: R Clock: PBUS_WRCLK Reset State: 0x01 Reset N/A		
HW Ve	HW Version Register [7:0]  COIN_REVISION1		
Bits	Name	Description	
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.	

#### 0x00002801 COIN\_REVISION2

Type: R

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

## COIN\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x00002802 COIN\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

## COIN\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

N

## COIN\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00002804 COIN\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: N/A

Peripheral Type

## COIN\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0x2: CHARGER

## 0x00002805 COIN\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x20

Reset Name: N/A

Peripheral SubType

## COIN\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	0x20: COINCELL

JUNE

## 0x00002808 COIN\_STATUS1

Type: R

Clock: PBUS WRCLK

Reset State: 0x00

Reset Name: N/A

Status Registers

## COIN\_STATUS1

Bits	Name	Description
7	COINCELL_OK	0 = coincell is disabled
		1 = coincell is enabled
		0x0: CC_DISABLED
		0x1: CC_ENABLED

## 0x00002844 COIN\_COIN\_CHG\_RSET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: soft xVdd rb

Set Coincell Charge Current

## COIN\_COIN\_CHG\_RSET

Bits	Name	Description
1:0	COIN_CHG_RSET	sets the coin cell charger current limiting resistor value
		0 = 2.1k ohm
		1 = 1.7k ohm
		2 = 1.2k ohm
		3 = 800 ohm
		0x0: CC_RSET_2K1
		0x1: CC_RSET_1K7
		0x2: CC_RSET_1K2
		0x3: CC_RSET_0K8

## 0x00002845 COIN\_COIN\_CHG\_VSET

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** soft\_xVdd\_rb Set Coincell Charge Voltage

## COIN\_COIN\_CHG\_VSET

Bits	Name	Description
1:0	COIN_CHG_VSET	sets the coin cell charging voltage  0 = 2.5V  1 = 3.2V  2 = 3.1V  3 = 3.0V  0x0: CC_VSET_2V5  0x1: CC_VSET_3V2  0x2: CC_VSET_3V1  0x3: CC_VSET_3V0

## 0x00002846 COIN\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** soft\_xVdd\_rb

#### COIN\_EN\_CTL

Bits	Name	Description
7	COINCELL_EN	1 = Enable the Coincell, 0 = Disable the coincell 0x0: CC_DISABLED 0x1: CC_ENABLED



# 12 Mbg\_dig Registers

### 0x00002C00 MBG1\_REVISION1

MBG1	MBG1_REVISION1			
Clock:	Type: R Clock: PBUS_WRCLK Reset State: 0x00			
Reset N	Name: n/a			
	HW Version Register [7:0]			
MBG1_	_REVISION1	100m		
Bits	Name	Description		
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.		

#### 0x00002C01 MBG1\_REVISION2

Type: R

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [15:8]

#### MBG1\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00002C02 MBG1\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: n/a

HW Version Register [23:16]

#### MBG1\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

### 0x00002C03 MBG1\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [31:24]

#### MBG1\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

### 0x00002C04 MBG1\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x0E

Reset Name: n/a

Peripheral Type

#### MBG1\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0xE: MBG

### 0x00002C05 MBG1\_PERPH\_SUBTYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: n/a

Peripheral SubType

#### MBG1\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	

#### 0x00002C08 MBG1\_STATUS1

#### **MBG1 STATUS1**

MBG1	MBG1_STATUS1			
Clock:	Type: R Clock: PBUS_WRCLK Reset State: Undefined			
Reset 1	Name: n/a	ign. Corn		
Status 1	Registers	i. S. Coliff		
	27	Egg.		
MBG1_	STATUS1			
Bits	Name	Description		
7	MBG_OK	1= MBG has started up and the Vref1p25 is charged up to at least		
		vbg_pon level 0x0: MBG_NOT_OK		
		0x1: MBG_OK		
		_		
1	NPM_TRUE	1 = MBG is on and in NPM		
		0x0: MBG_LPM		
1		0x1: MBG_NPM		

### 0x00002C44 MBG1\_MODE\_CTRL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x91

Reset Name: perph rb

#### MBG1\_MODE\_CTRL

Bits	Name	Description
7	FORCE_NPM	Force NPM whenever this bit is set 0x0: NO_FORCE_LPM 0x1: FORCE_NPM
4	NPM_FOLLOW_SLEEPB	1' = transition to NPM, whenever PMIC is awake, '0' = LPM (IPTAT_EN and IREF_EN must be set 0x0: NO_FOLLOW 0x1: FOLLOW_SLEEP_B
3	FORCE_FASTVBG	set this bit high will force fast charge mode always on instead of the auto mode controlled by the MBG_OK signal.  0x0: NORMAL_MODE  0x1: FORCE_FAST_VBG
2	FORCE_MBGCC_EN	set this bit high will force the curvature correction block on in both normal mode and sleep mode if Iref and Iptat is available 0x0: CC_DISABLED 0x1: CC_ENABLED
1	FORCE_IPTAT_EN	set this bit high will force the IPTAT block on in sleep mode 0x0: NO_FORCE_IPTAT 0x1: FORCE_IPTAT
0	FORCE_IREF_EN	set this bit high will force Iref block on in sleep mode 0x0: NO_FORCE_IREF 0x1: FORCE_IREF

### 0x00002C46 MBG1\_EN\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

### MBG1\_EN\_CTL

Bits	Name	Description
7	MBG_EN	this bit is one of the multiple MBG_EN signals that are from different
		sources and ORed together to control the ON/OFF of MBG block 0x0: MBG_DISABLED 0x1: MBG_ENABLED

# 13 Vadc Registers

## 0x00003100 VADC1\_LC\_USR\_REVISION1

Type: R

Clock: pbus\_wrclk Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### VADC1\_LC\_USR\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

### 0x00003101 VADC1\_LC\_USR\_REVISION2

Type: R

Clock: pbus\_wrclk Reset State: 0x04

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### VADC1\_LC\_USR\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00003102 VADC1\_LC\_USR\_REVISION3

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### VADC1\_LC\_USR\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

### 0x00003103 VADC1\_LC\_USR\_REVISION4

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### VADC1\_LC\_USR\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

### 0x00003104 VADC1\_LC\_USR\_PERPH\_TYPE

Type: R

Clock: pbus\_wrclk Reset State: 0x08

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

### VADC1\_LC\_USR\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	ADC

### 0x00003105 VADC1\_LC\_USR\_PERPH\_SUBTYPE

Type: R

Clock: pbus\_wrclk Reset State: 0x09

Reset Name: N/A

Peripheral SubType

#### VADC1\_LC\_USR\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	ADC sub type

## 0x00003108 VADC1\_LC\_USR\_STATUS1

Type: R

Clock: pbus\_wrclk Reset State: 0x01

Reset Name: N/A

Status Registers

#### VADC1\_LC\_USR\_STATUS1

Bits	Name	Description
4:3	OP_MODE	Selects basic mode of operation
		0x0: NORM_MODE
		0x1: CONV_SEQ_MODE
		0x2: MEAS_INT_MODE
2	MEAS_INTERVAL_EN_STS	Interval Mode
		0x0: INTERVAL_MODE_DISABLED
		0x1: INTERVAL_MODE_ENABLED
1	REQ_STS	REQ_STS mirrors the REQ bit. When REQ is asserted the arbiter stores a descriptor in the conversion request queue. Bit is cleared when ADC conversion is completed.
		0x0: REQ_NOT_IN_PROGRESS
		0x1: REQ_IN_PROGRESS

### VADC1\_LC\_USR\_STATUS1 (cont.)

Bits	Name	Description
0	EOC	End of conversion status flag. Bit is de-asserted when arbiter is servicing a conversion request and asserted when conversion is completed. After a conversion is requested, the EOC and REQ_STS bits can be polled to determine ADC conversion status as follows:  REQ_STS EOC Arbiter state  1 1 Waiting for ADC to complete another process's conversion request.  1 0 ADC conversion occurring.  0 1 ADC conversion completed.  0 0 Invalid  0x0: CONV_NOT_COMPLETE  0x1: CONV_COMPLETE

### 0x00003110 VADC1\_LC\_USR\_INT\_RT\_STS

Type: R

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Interrupt Real Time Status Bits

### VADC1\_LC\_USR\_INT\_RT\_STS

Bits	Name	Description
5	MIN_LOW_THR_INT_RT_S TS	ADC minimum output lower than low threshold. Active high signal. 0x0: MIN_LOW_THR_INT_FALSE 0x1: MIN_LOW_THR_INT_TRUE
4	LOW_THR_INT_RT_STS	ADC output lower than low threshold. Active high signal.  0x0: LOW_THR_INT_FALSE  0x1: LOW_THR_INT_TRUE
3	HIGH_THR_INT_RT_STS	ADC output higher than high threshold. Active high signal. 0x0: HIGH_THR_INT_FALSE 0x1: HIGH_THR_INT_TRUE
2	CONV_SEQ_TIMEOUT_INT _RT_STS	Indicates conversion sequencer conversion was triggered by SBI register field conversion request time out.  0x0: CONV_SEQ_TIMEOUT_FALSE  0x1: CONV_SEQ_TIMEOUT_TRUE
1	FIFO_NOT_EMPTY_INT_RT _STS	Indicates conversion sequencer request written to FIFO when it was not empty.  0x0: FIFO_NOT_EMPTY_INT_FALSE  0x1: FIFO_EMPTY_INT_TRUE

### VADC1\_LC\_USR\_INT\_RT\_STS (cont.)

Bits	Name	Description
0	EOC_INT_RT_STS	Secure process end of conversion interrupt. Active high signal two tcxo_clk cycles wide.  0x0: CONV_COMPLETE_INT_FALSE  0x1: CONV_COMPLETE_INT_TRUE

### 0x00003111 VADC1\_LC\_USR\_INT\_SET\_TYPE

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## VADC1\_LC\_USR\_INT\_SET\_TYPE

Bits	Name	Description
5	MIN_LOW_THR_INT_SET_T YPE	Minimum Low threshold interrupt set type 0x0: MIN_LOW_THR_INT_LEVEL 0x1: MIN_LOW_THR_INT_EDGE
4	LOW_THR_INT_SET_TYPE	Low threshold interrupt set type 0x0: LOW_THR_INT_LEVEL 0x1: LOW_THR_INT_EDGE
3	HIGH_THR_INT_SET_TYPE	High threshold interrupt set type 0x0: HIGH_THR_INT_LEVEL 0x1: HIGH_THR_INT_EDGE
2	CONV_SEQ_TIMEOUT_INT _SET_TYPE	Conversion sequencer timeout interrupt set type 0x0: CONV_SEQ_TIMEOUT_LEVEL 0x1: CONV_SEQ_TIMEOUT_EDGE
1	FIFO_NOT_EMPTY_INT_SE T_TYPE	FIFO not empty interrupt set type 0x0: FIFO_NOT_EMPTY_LEVEL 0x1: FIFO_NOT_EMPTY_EDGE
0	EOC_SET_INT_TYPE	EOC interrupt set type 0x0: EOC_LEVEL 0x1: EOC_EDGE

### 0x00003112 VADC1\_LC\_USR\_INT\_POLARITY\_HIGH

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### VADC1\_LC\_USR\_INT\_POLARITY\_HIGH

Bits	Name	Description
5	MIN_LOW_THR_INT_HIGH	Minimum Low threshold interrupt high polarity enabled 0x0: MIN_LOW_THR_INT_POL_HIGH_DISABLED 0x1: MIN_LOW_THR_INT_POL_HIGH_ENABLED
4	LOW_THR_INT_HIGH	Low threshold interrupt high polarity enabled 0x0: LOW_THR_INT_POL_HIGH_DISABLED 0x1: LOW_THR_INT_POL_HIGH_ENABLED
3	HIGH_THR_INT_HIGH	High threshold interrupt high polarity enabled 0x0: HIGH_THR_INT_POL_HIGH_DISABLED 0x1: HIGH_THR_INT_POL_HIGH_ENABLED
2	CONV_SEQ_TIMEOUT_INT _HIGH	Conversion sequencer interrupt high polarity enabled 0x0: CONV_SEQ_TIMEOUT_INT_POL_HIGH_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_POL_HIGH_ENABLED
1	FIFO_NOT_EMPTY_INT_HI GH	FIFO not empty interrupt high polarity enabled 0x0: FIFO_NOT_EMPTY_INT_POL_HIGH_DISABLED 0x1: FIFO_NOT_EMPTY_INT_POL_HIGH_ENABLED
0	EOC_INT_HIGH	EOC interrupt high polarity enabled 0x0: EOC_INT_POL_HIGH_DISABLED 0x1: EOC_INT_POL_HIGH_ENABLED

### 0x00003113 VADC1\_LC\_USR\_INT\_POLARITY\_LOW

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

### VADC1\_LC\_USR\_INT\_POLARITY\_LOW

Bits	Name	Description
5	MIN_LOW_THR_INT_HIGH	Minimum Low threshold interrupt low polarity enabled 0x0: MIN_LOW_THR_INT_POL_LOW_DISABLED 0x1: MIN_LOW_THR_INT_POL_LOW_ENABLED
4	LOW_THR_INT_HIGH	Low threshold interrupt low polarity enabled 0x0: LOW_THR_INT_POL_LOW_DISABLED 0x1: LOW_THR_INT_POL_LOW_ENABLED
3	HIGH_THR_INT_HIGH	High threshold interrupt low polarity enabled 0x0: HIGH_THR_INT_POL_LOW_DISABLED 0x1: HIGH_THR_INT_POL_LOW_ENABLED
2	CONV_SEQ_TIMEOUT_INT _LOW	Conversion sequencer interrupt low polarity enabled 0x0: CONV_SEQ_TIMEOUT_INT_POL_LOW_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_POL_LOW_ENABLED
1	FIFO_NOT_EMPTY_INT_LO W	FIFO not empty interrupt low polarity enabled 0x0: FIFO_NOT_EMPTY_INT_POL_LOW_DISABLED 0x1: FIFO_NOT_EMPTY_INT_POL_LOW_ENABLED
0	EOC_INT_LOW	EOC interrupt low polarity enabled 0x0: EOC_INT_POL_LOW_DISABLED 0x1: EOC_INT_POL_LOW_ENABLED

### 0x00003114 VADC1\_LC\_USR\_INT\_LATCHED\_CLR

Type: W

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Writing a '1' to a bit in this register will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### VADC1\_LC\_USR\_INT\_LATCHED\_CLR

Bits	Name	Description
5	MIN_LOW_THR_INT_LATC HED_CLR	Minimum Low threshold interrupt latched clear
4	LOW_THR_INT_LATCHED_ CLR	Low threshold interrupt latched clear
3	HIGH_THR_INT_LATCHED_ CLR	High threshold interrupt latched clear
2	CONV_SEQ_TIMEOUT_INT _LATCHED_CLR	Conversion sequencer interrupt latched clear

### VADC1\_LC\_USR\_INT\_LATCHED\_CLR (cont.)

Bits	Name	Description
1	FIFO_NOT_EMPTY_INT_LA TCHED_CLR	FIFO not empty interrupt latched clear
0	EOC_INT_LATCHED_CLR	EOC interrupt latched clear

### 0x00003115 VADC1\_LC\_USR\_INT\_EN\_SET

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Writing '0' to a bit in this register has no effect. Writing a '1' to a bit in this register will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### VADC1\_LC\_USR\_INT\_EN\_SET

Bits	Name	Description
5	MIN_LOW_THR_INT_EN_S ET	Minimum Low threshold interrupt enable set 0x0: LOW_THR_INT_DISABLED 0x1: LOW_THR_INT_ENBLED
4	LOW_THR_INT_EN_SET	Low threshold interrupt enable set  0x0: LOW_THR_INT_DISABLED  0x1: LOW_THR_INT_ENBLED
3	HIGH_THR_INT_EN_SET	High threshold interrupt enable set 0x0: HIGH_THR_INT_DISABLED 0x1: HIGH_THR_INT_ENBLED
2	CONV_SEQ_TIMEOUT_INT _EN_SET	Conversion sequencer interrupt enable set 0x0: CONV_SEQ_TIMEOUT_INT_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_ENBLED
1	FIFO_NOT_EMPTY_INT_EN _SET	FIFO not empty interrupt enable set  0x0: FIFO_NOT_EMPTY_INT_DISABLED  0x1: FIFO_NOT_EMPTY_INT_ENBLED
0	EOC_INT_EN_SET	EOC interrupt enable set 0x0: EOC_INT_DISABLED 0x1: EOC_INT_ENBLED

### 0x00003116 VADC1\_LC\_USR\_INT\_EN\_CLR

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Writing a '0' to a bit in this register has no effect. Writing a '1' to a bit in this register will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

### VADC1\_LC\_USR\_INT\_EN\_CLR

Bits	Name	Description
5	MIN_LOW_THR_INT_EN_C LR	Minimum Low threshold interrupt enable clear 0x0: MIN_LOW_THR_INT_DISABLED 0x1: MIN_LOW_THR_INT_ENBLED
4	LOW_THR_INT_EN_CLR	Low threshold interrupt enable clear 0x0: LOW_THR_INT_DISABLED 0x1: LOW_THR_INT_ENBLED
3	HIGH_THR_INT_EN_CLR	High threshold interrupt enable clear 0x0: HIGH_THR_INT_DISABLED 0x1: HIGH_THR_INT_ENBLED
2	CONV_SEQ_TIMEOUT_INT _EN_CLR	Conversion sequencer interrupt enable clear 0x0: CONV_SEQ_TIMEOUT_INT_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_ENBLED
1	FIFO_NOT_EMPTY_INT_EN _CLR	FIFO not empty interrupt enable clear 0x0: FIFO_NOT_EMPTY_INT_DISABLED 0x1: FIFO_NOT_EMPTY_INT_ENBLED
0	EOC_INT_EN_CLR	EOC interrupt enable clear 0x0: EOC_INT_DISABLED 0x1: EOC_INT_ENBLED

### 0x00003118 VADC1\_LC\_USR\_INT\_LATCHED\_STS

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

### VADC1\_LC\_USR\_INT\_LATCHED\_STS

Bits	Name	Description
5	MIN_LOW_THR_INT_LATC HED_STS	Minimum Low threshold interrupt latched 0x0: MIN_LOW_THR_INT_LATCHED_FALSE 0x1: MIN_LOW_THR_INT_LATCHED_TRUE
4	LOW_THR_INT_LATCHED_ STS	Low threshold interrupt latched 0x0: LOW_THR_INT_LATCHED_FALSE 0x1: LOW_THR_INT_LATCHED_TRUE
3	HIGH_THR_INT_LATCHED_ STS	High threshold interrupt latched 0x0: HIGH_THR_INT_LATCHED_FALSE 0x1: HIGH_THR_INT_LATCHED_TRUE
2	CONV_SEQ_TIMEOUT_INT _LATCHED_STS	Conversion sequencer interrupt latched  0x0: CONV_SEQ_TIMEOUT_INT_LATCHED_FALSE  0x1: CONV_SEQ_TIMEOUT_INT_LATCHED_TRUE
1	FIFO_NOT_EMPTY_INT_LA TCHED_STS	FIFO not empty interrupt latched  0x0: FIFO_NOT_EMPTY_INT_LATCHED_FALSE  0x1: FIFO_NOT_EMPTY_INT_LATCHED_TRUE
0	EOC_INT_LATCHED_STS	EOC interrupt latched 0x0: EOC_INT_LATCHED_FALSE 0x1: EOC_INT_LATCHED_TRUE

### 0x00003119 VADC1\_LC\_USR\_INT\_PENDING\_STS

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Debug: Pending is set if interrupt has been sent but not cleared.

### VADC1\_LC\_USR\_INT\_PENDING\_STS

Bits	Name	Description
5	MIN_LOW_THR_INT_PENDI NG_STS	Minimum Low threshold interrupt pending 0x0: MIN_LOW_THR_INT_PENDING_FALSE 0x1: MIN_LOW_THR_INT_PENDING_TRUE
4	LOW_THR_INT_PENDING_ STS	Low threshold interrupt pending 0x0: LOW_THR_INT_PENDING_FALSE 0x1: LOW_THR_INT_PENDING_TRUE
3	HIGH_THR_INT_PENDING_ STS	High threshold interrupt pending 0x0: HIGH_THR_INT_PENDING_FALSE 0x1: HIGH_THR_INT_PENDING_TRUE

### VADC1\_LC\_USR\_INT\_PENDING\_STS (cont.)

Bits	Name	Description
2	CONV_SEQ_TIMEOUT_INT _PENDING_STS	Conversion sequencer interrupt pending 0x0: CONV_SEQ_TIMEOUT_INT_PENDING_FALSE 0x1: CONV_SEQ_TIMEOUT_INT_PENDING_TRUE
1	FIFO_NOT_EMPTY_INT_PE NDING_STS	FIFO not empty interrupt pending 0x0: FIFO_NOT_EMPTY_INT_PENDING_FALSE 0x1: FIFO_NOT_EMPTY_INT_PENDING_TRUE
0	EOC_INT_PENDING_STS	EOC interrupt pending 0x0: EOC_INT_PENDING_FALSE 0x1: EOC_INT_PENDING_TRUE

## 0x0000311A VADC1\_LC\_USR\_INT\_MID\_SEL

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Selects the MID that will receive the interrupt

### VADC1\_LC\_USR\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	Selects the MID that will receive the interrupt

### 0x0000311B VADC1\_LC\_USR\_INT\_PRIORITY

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Selects the SPMI interrupt priority

#### VADC1\_LC\_USR\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	Selects the SPMI interrupt priority 0x0: SR 0x1: A

### 0x00003140 VADC1\_LC\_USR\_MODE\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x03

Reset Name: uvlo\_perph\_rb

Settings Common to Input and Output

### VADC1\_LC\_USR\_MODE\_CTL

Bits	Name	Description
4:3	OP_MODE	Selects basic mode of operation:
		00=Normal Mode - Single measurement
		01=Conversion Sequencer - Single measurement using conversion sequencer
		10=Measurement Interval - Single or Continuous measurements at specified delay/interval
		0x0: NORM_MODE
		0x1: CONV_SEQ_MODE
		0x2: MEAS_INT_MODE
2	VREF_XO_THM_FORCE	When cleared, VDD_REF is connected to XO thermistor in active mode, disconnected in sleep mode
	27,10	When set, force VDD_REF to be connected to the XO thermistor regardless the status of sleepb
	OS villes	0x0: VREF_XO_THM_FORCE_FALSE
	Old Wen	0x1: VREF_XO_THM_FORCE_TRUE
1	RESERVED	
0	ADC_TRIM_EN	Enable ADC trim
		0x0: ADC_TRIM_DISABLED
		0x1: ADC_TRIM_ENABLED

### 0x00003146 VADC1\_LC\_USR\_EN\_CTL1

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Enables ADC module.

### VADC1\_LC\_USR\_EN\_CTL1

Bits	Name	Description
7	ADC_EN	Enables ADC module.
		0x0: ADC_DISABLED
		0x1: ADC_ENABLED

## 0x00003148 VADC1\_LC\_USR\_ADC\_CH\_SEL\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x06

Reset Name: uvlo perph rb

ADC Channel selection. See device specification for channel descriptions.

### VADC1\_LC\_USR\_ADC\_CH\_SEL\_CTL

Bits	Name	Description
7:0	ADC_CH_SEL	ADC Channel selection. See device specification for channel descriptions.

### 0x00003150 VADC1\_LC\_USR\_ADC\_DIG\_PARAM

Type: RW

Clock: pbus\_wrclk Reset State: 0x04

Reset Name: uvlo perph rb

**ADC** Digital Parameters

#### VADC1\_LC\_USR\_ADC\_DIG\_PARAM

Bits	Name	Description
3:2	DEC_RATIO_SEL	Decimation ratio: 0x0: DECI_512 0x1: DECI_1K 0x2: DECI_2K 0x3: DECI_4K
1:0	CLK_SEL	Select ADC clock rate: 0x0: CLK_SEL_2P4MHZ 0x1: CLK_SEL_4P8MHZ 0x2: CLK_SEL_9P6MHZ 0x3: CLK_SEL_19P2MHZ

### 0x00003151 VADC1\_LC\_USR\_HW\_SETTLE\_DELAY

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Settle Delay

### VADC1\_LC\_USR\_HW\_SETTLE\_DELAY

Time between AMUX getting configured and the ADC starting conversion. Delay = 100us*(value) for value<11, and 2ms*(value- 10) otherwise 0x0: HW_SETTLE_DELAY_0US 0x1: HW_SETTLE_DELAY_100US 0x2: HW_SETTLE_DELAY_200US 0x3: HW_SETTLE_DELAY_300US 0x4: HW_SETTLE_DELAY_400US 0x5: HW_SETTLE_DELAY_500US 0x6: HW_SETTLE_DELAY_600US 0x7: HW_SETTLE_DELAY_700US 0x8: HW_SETTLE_DELAY_700US 0x8: HW_SETTLE_DELAY_800US 0x9: HW_SETTLE_DELAY_900US 0x4: HW_SETTLE_DELAY_900US 0x6: HW_SETTLE_DELAY_1MS	Bits	Name	Description
~ > 200			Time between AMUX getting configured and the ADC starting conversion. Delay = 100us*(value) for value<11, and 2ms*(value-10) otherwise  0x0: HW_SETTLE_DELAY_0US  0x1: HW_SETTLE_DELAY_100US  0x2: HW_SETTLE_DELAY_200US  0x3: HW_SETTLE_DELAY_300US  0x4: HW_SETTLE_DELAY_400US  0x5: HW_SETTLE_DELAY_500US  0x6: HW_SETTLE_DELAY_600US  0x7: HW_SETTLE_DELAY_700US  0x8: HW_SETTLE_DELAY_800US  0x9: HW_SETTLE_DELAY_900US  0x9: HW_SETTLE_DELAY_1MS  0xB: HW_SETTLE_DELAY_1MS
0xC: HW_SETTLE_DELAY_4MS 0xD: HW_SETTLE_DELAY_6MS		20, 34	
I DYB. HW. SELLLE DELAY 2MS		C 8.09 minute	0xA: HW_SETTLE_DELAY_1MS
			0xE: HW_SETTLE_DELAY_8MS 0xF: HW_SETTLE_DELAY_10MS

### 0x00003152 VADC1\_LC\_USR\_CONV\_REQ

Type: W

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: req\_rb

Conversion Request

#### VADC1\_LC\_USR\_CONV\_REQ

Bits	Name	Description
7	REQ	Conversion request strobe. When bit is asserted the arbiter stores a descriptor in the conversion request queue. Bit is cleared when ADC conversion is completed.  0x0: CONV_REQ_FALSE  0x1: CONV_REQ_TRUE

## 0x00003154 VADC1\_LC\_USR\_CONV\_SEQ\_CTL

**Type:** RW

Clock: pbus\_wrclk Reset State: 0x45

Reset Name: uvlo perph rb

**Conversion Sequencer Control** 

### VADC1\_LC\_USR\_CONV\_SEQ\_CTL

Bits	Name	Description
7:4	CONV_SEQ_HOLDOFF	Select delay from conversion trigger signal (i.e. adc_conv_seq_trig) transition to ADC enable. Delay = 25us*(value+1). Actual delay will be longer if request is stored in a non empty FIFO and/or conversion needs to wait for LDO OK handshake.
	2 5	0x0: SEQ_HOLD_25US
		0x1: SEQ_HOLD_50US
		0x2: SEQ_HOLD_75US
		0x3: SEQ_HOLD_100US
		0x4: SEQ_HOLD_125US
		0x5: SEQ_HOLD_150US
		0x6: SEQ_HOLD_175US
		0x7: SEQ_HOLD_200US
		0x8: SEQ_HOLD_225US
		0x9: SEQ_HOLD_250US
		0xA: SEQ_HOLD_275US
		0xB: SEQ_HOLD_300US
		0xC: SEQ_HOLD_325US
		0xD: SEQ_HOLD_350US
		0xE: SEQ_HOLD_375US
		0xF: SEQ_HOLD_400US

### VADC1\_LC\_USR\_CONV\_SEQ\_CTL (cont.)

Bits	Name	Description
3:0	CONV_SEQ_TIMEOUT	Select delay (0 to 15ms) from conversion request to triggering conversion sequencer hold off timer.
		0x0: SEQ_TIMEOUT_0MS
		0x1: SEQ_TIMEOUT_1MS
		0x2: SEQ_TIMEOUT_2MS
		0x3: SEQ_TIMEOUT_3MS
		0x4: SEQ_TIMEOUT_4MS
		0x5: SEQ_TIMEOUT_5MS
		0x6: SEQ_TIMEOUT_6MS
		0x7: SEQ_TIMEOUT_7MS
		0x8: SEQ_TIMEOUT_8MS
		0x9: SEQ_TIMEOUT_9MS
		0xA: SEQ_TIMEOUT_10MS
		0xB: SEQ_TIMEOUT_11MS
		0xC: SEQ_TIMEOUT_12MS
		0xD: SEQ_TIMEOUT_13MS
		0xE: SEQ_TIMEOUT_14MS
		0xF: SEQ_TIMEOUT_15MS

### 0x00003155 VADC1\_LC\_USR\_CONV\_SEQ\_TRIG\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Conversion Sequencer Trigger Select

### VADC1\_LC\_USR\_CONV\_SEQ\_TRIG\_CTL

Bits	Name	Description
7	CONV_SEQ_TRIG_COND	Select conversion trigger condition(s) that starts ADC conversion hold off timer.  0x0 - Falling edge  0x1 - Rising edge  0x0: FALLING_EDGE  0x1: RISING_EDGE
1:0	CONV_SEQ_TRIG_SEL	Select conversion sequencer trigger input signal.  0x0: ADC_TRIG0  0x1: ADC_TRIG1  0x2: ADC_TRIG2  0x3: ADC_TRIG3

### 0x00003157 VADC1\_LC\_USR\_MEAS\_INTERVAL\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Interval Mode Control

### VADC1\_LC\_USR\_MEAS\_INTERVAL\_CTL

Bits	Name	Description
3:0	Name  MEAS_INTERVAL_TIME	Description  Select measurement interval time (i.e., If value=0, use 0ms, else use 2^(value+4)/32768).  0x0: MEAS_INTERVAL_0MS  0x1: MEAS_INTERVAL_1P0MS  0x2: MEAS_INTERVAL_2P0MS  0x3: MEAS_INTERVAL_3P9MS  0x4: MEAS_INTERVAL_7P8MS  0x5: MEAS_INTERVAL_1P0MS
	2018.09.2101 2018.5m@minds	0x6: MEAS_INTERVAL_31P3MS 0x7: MEAS_INTERVAL_62P5MS 0x8: MEAS_INTERVAL_125MS 0x9: MEAS_INTERVAL_250MS 0xA: MEAS_INTERVAL_500MS 0xB: MEAS_INTERVAL_1S 0xC: MEAS_INTERVAL_2S 0xD: MEAS_INTERVAL_4S 0xE: MEAS_INTERVAL_4S 0xF: MEAS_INTERVAL_16S

### 0x00003159 VADC1\_LC\_USR\_MEAS\_INTERVAL\_OP\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Interval mode select

### VADC1\_LC\_USR\_MEAS\_INTERVAL\_OP\_CTL

Bits	Name	Description
7	MEAS_INTERVAL_OP	Interval mode select 0x0: INTERVAL_MODE_DISABLED 0x1: INTERVAL_MODE_ENABLED

### 0x0000315A VADC1\_LC\_USR\_FAST\_AVG\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Fast Average Control

### VADC1\_LC\_USR\_FAST\_AVG\_CTL

Bits	Name	Description
3:0	FAST_AVG_SAMPLES	Select number of samples for use in fast average mode (i.e.
		2^(value).
		0x0: AVG_1_SAMPLE
		0x1: AVG_2_SAMPLES
		0x2: AVG_4_SAMPLES
		0x3: AVG_8_SAMPLES
		0x4: AVG_16_SAMPLES
		0x5: AVG_32_SAMPLES
		0x6: AVG_64_SAMPLES
		0x7: AVG_128_SAMPLES
		0x8: AVG_256_SAMPLES
	27	0x9: AVG_512_SAMPLES

## 0x0000315B VADC1\_LC\_USR\_FAST\_AVG\_EN

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Fast Average Enable

### VADC1\_LC\_USR\_FAST\_AVG\_EN

Bits	Name	Description
7	FAST_AVG_EN	Select low latency for multiple conversions
		0x0: FAST_AVG_DISABLED
		0x1: FAST_AVG_ENABLED

### 0x0000315C VADC1\_LC\_USR\_LOW\_THR0

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Low Threshold Byte 0

#### VADC1\_LC\_USR\_LOW\_THR0

Bits	Name	Description
7:0	LOW_THR_7_0	Low byte of low threshold detector

### 0x0000315D VADC1\_LC\_USR\_LOW\_THR1

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Low Threshold Byte 1

### VADC1\_LC\_USR\_LOW\_THR1

Bits	Name	Description
7:0	LOW_THR_15_8	High byte of low threshold detector

### 0x0000315E VADC1\_LC\_USR\_HIGH\_THR0

Type: RW

Clock: pbus\_wrclk
Reset State: 0xFF

Reset Name: uvlo perph rb

High Threshold Byte 0

### VADC1\_LC\_USR\_HIGH\_THR0

Bits	Name	Description
7:0	HIGH_THR_7_0	Low byte of high threshold detector

### 0x0000315F VADC1\_LC\_USR\_HIGH\_THR1

Type: RW

Clock: pbus\_wrclk Reset State: 0xFF

Reset Name: uvlo perph rb

High Threshold Byte 1

#### VADC1\_LC\_USR\_HIGH\_THR1

Bits	Name	Description
7:0	HIGH_THR_15_8	High byte of high threshold detector

#### 

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: uvlo perph rb

ADC Sample Byte 0

### VADC1\_LC\_USR\_DATA0

Bits	Name	Description
7:0	DATA_7_0	Low byte of ADC output

#### 

**Type:** R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: uvlo\_perph\_rb

ADC Sample Byte 1

### VADC1\_LC\_USR\_DATA1

Bits	Name	Description
7:0	DATA_15_8	High byte of ADC output

### 0x00003162 VADC1\_LC\_USR\_MIN\_LOW\_THR0

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Minimum Low Threshold Byte 0

#### VADC1\_LC\_USR\_MIN\_LOW\_THR0

Bits	Name	Description
7:0	MIN_LOW_THR_7_0	Low byte of minimum low threshold detector

### 0x00003163 VADC1\_LC\_USR\_MIN\_LOW\_THR1

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Minimum Low Threshold Byte 1

#### VADC1\_LC\_USR\_MIN\_LOW\_THR1

Bits	Name	Description
7:0	MIN_LOW_THR_15_8	High byte of minimum low threshold detector

### 0x00003166 VADC1\_LC\_USR\_MIN\_DATA0

**Type:** R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: uvlo perph rb

Minimum ADC Sample Byte 0

### VADC1\_LC\_USR\_MIN\_DATA0

Bits	Name	Description
7:0	MIN_DATA_7_0	Low byte of minimum ADC output

### 0x00003167 VADC1\_LC\_USR\_MIN\_DATA1

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: uvlo perph rb

Minimum ADC Sample Byte 1

#### VADC1\_LC\_USR\_MIN\_DATA1

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E	Bits	Name	Description
	7:0	MIN_DATA_15_8	High byte of minimum ADC output

# 14 Vadc\_adj Registers

### 0x00003200 VADC3\_LC\_MDM\_REVISION1

Type: R

Clock: pbus\_wrclk Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

### VADC3\_LC\_MDM\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

### 0x00003201 VADC3\_LC\_MDM\_REVISION2

Type: R

Clock: pbus\_wrclk Reset State: 0x04

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### VADC3\_LC\_MDM\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00003202 VADC3\_LC\_MDM\_REVISION3

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

### VADC3\_LC\_MDM\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

### 0x00003203 VADC3\_LC\_MDM\_REVISION4

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### VADC3\_LC\_MDM\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

### 0x00003204 VADC3\_LC\_MDM\_PERPH\_TYPE

Type: R

Clock: pbus\_wrclk Reset State: 0x08

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

### VADC3\_LC\_MDM\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	ADC

### 0x00003205 VADC3\_LC\_MDM\_PERPH\_SUBTYPE

Type: R

Clock: pbus\_wrclk Reset State: 0x0B

**Reset Name:** N/A Peripheral SubType

#### VADC3\_LC\_MDM\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	VADC1

## 0x00003208 VADC3\_LC\_MDM\_STATUS1

Type: R

Clock: pbus\_wrclk
Reset State: 0x01

Reset Name: N/A

Status Registers

### VADC3\_LC\_MDM\_STATUS1

Bits	Name	Description
4:3	OP_MODE	Selects basic mode of operation
		0x0: NORM_MODE
		0x1: CONV_SEQ_MODE
		0x2: MEAS_INT_MODE
2	MEAS_INTERVAL_EN_STS	Interval Mode
		0x0: INTERVAL_MODE_DISABLED
		0x1: INTERVAL_MODE_ENABLED
1	REQ_STS	REQ_STS mirrors the REQ bit. When REQ is asserted the arbiter stores a descriptor in the conversion request queue. Bit is cleared when ADC conversion is completed.
		0x0: REQ_NOT_IN_PROGRESS
		0x1: REQ_IN_PROGRESS

### VADC3\_LC\_MDM\_STATUS1 (cont.)

Bits	Name	Description
0	EOC	End of conversion status flag. Bit is de-asserted when arbiter is servicing a conversion request and asserted when conversion is completed. After a conversion is requested, the EOC and REQ_STS bits can be polled to determine ADC conversion status as follows:  REQ_STS EOC Arbiter state  1 1 Waiting for ADC to complete another process's conversion request.  1 0 ADC conversion occurring.  0 1 ADC conversion completed.  0 0 Invalid  0x0: CONV_NOT_COMPLETE  0x1: CONV_COMPLETE

### 0x00003210 VADC3 LC MDM INT RT STS

Type: R

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Interrupt Real Time Status Bits

### VADC3\_LC\_MDM\_INT\_RT\_STS

Bits	Name	Description
5	MIN_LOW_THR_INT_RT_S TS	ADC minimum output lower than low threshold. Active high signal. 0x0: MIN_LOW_THR_INT_FALSE 0x1: MIN_LOW_THR_INT_TRUE
4	LOW_THR_INT_RT_STS	ADC output lower than low threshold. Active high signal.  0x0: LOW_THR_INT_FALSE  0x1: LOW_THR_INT_TRUE
3	HIGH_THR_INT_RT_STS	ADC output higher than high threshold. Active high signal. 0x0: HIGH_THR_INT_FALSE 0x1: HIGH_THR_INT_TRUE
2	CONV_SEQ_TIMEOUT_INT _RT_STS	Indicates conversion sequencer conversion was triggered by SBI register field conversion request time out.  0x0: CONV_SEQ_TIMEOUT_FALSE  0x1: CONV_SEQ_TIMEOUT_TRUE
1	FIFO_NOT_EMPTY_INT_RT _STS	Indicates conversion sequencer request written to FIFO when it was not empty.  0x0: FIFO_NOT_EMPTY_INT_FALSE  0x1: FIFO_EMPTY_INT_TRUE

### VADC3\_LC\_MDM\_INT\_RT\_STS (cont.)

Bits	Name	Description
0	EOC_INT_RT_STS	Secure process end of conversion interrupt. Active high signal two tcxo_clk cycles wide.  0x0: CONV_COMPLETE_INT_FALSE  0x1: CONV_COMPLETE_INT_TRUE

### 0x00003211 VADC3\_LC\_MDM\_INT\_SET\_TYPE

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

0 =use level trigger interrupts, 1 =use edge trigger interrupts

### VADC3\_LC\_MDM\_INT\_SET\_TYPE

Bits	Name	Description
5	MIN_LOW_THR_INT_SET_T YPE	Minimum Low threshold interrupt set type 0x0: MIN_LOW_THR_INT_LEVEL 0x1: MIN_LOW_THR_INT_EDGE
4	LOW_THR_INT_SET_TYPE	Low threshold interrupt set type 0x0: LOW_THR_INT_LEVEL 0x1: LOW_THR_INT_EDGE
3	HIGH_THR_INT_SET_TYPE	High threshold interrupt set type 0x0: HIGH_THR_INT_LEVEL 0x1: HIGH_THR_INT_EDGE
2	CONV_SEQ_TIMEOUT_INT _SET_TYPE	Conversion sequencer timeout interrupt set type 0x0: CONV_SEQ_TIMEOUT_LEVEL 0x1: CONV_SEQ_TIMEOUT_EDGE
1	FIFO_NOT_EMPTY_INT_SE T_TYPE	FIFO not empty interrupt set type 0x0: FIFO_NOT_EMPTY_LEVEL 0x1: FIFO_NOT_EMPTY_EDGE
0	EOC_SET_INT_TYPE	EOC interrupt set type 0x0: EOC_LEVEL 0x1: EOC_EDGE

### 0x00003212 VADC3\_LC\_MDM\_INT\_POLARITY\_HIGH

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

### VADC3\_LC\_MDM\_INT\_POLARITY\_HIGH

Bits	Name	Description
5	MIN_LOW_THR_INT_HIGH	Minimum Low threshold interrupt high polarity enabled 0x0: MIN_LOW_THR_INT_POL_HIGH_DISABLED 0x1: MIN_LOW_THR_INT_POL_HIGH_ENABLED
4	LOW_THR_INT_HIGH	Low threshold interrupt high polarity enabled 0x0: LOW_THR_INT_POL_HIGH_DISABLED 0x1: LOW_THR_INT_POL_HIGH_ENABLED
3	HIGH_THR_INT_HIGH	High threshold interrupt high polarity enabled 0x0: HIGH_THR_INT_POL_HIGH_DISABLED 0x1: HIGH_THR_INT_POL_HIGH_ENABLED
2	CONV_SEQ_TIMEOUT_INT _HIGH	Conversion sequencer interrupt high polarity enabled 0x0: CONV_SEQ_TIMEOUT_INT_POL_HIGH_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_POL_HIGH_ENABLED
1	FIFO_NOT_EMPTY_INT_HI GH	FIFO not empty interrupt high polarity enabled 0x0: FIFO_NOT_EMPTY_INT_POL_HIGH_DISABLED 0x1: FIFO_NOT_EMPTY_INT_POL_HIGH_ENABLED
0	EOC_INT_HIGH	EOC interrupt high polarity enabled 0x0: EOC_INT_POL_HIGH_DISABLED 0x1: EOC_INT_POL_HIGH_ENABLED

### 0x00003213 VADC3\_LC\_MDM\_INT\_POLARITY\_LOW

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

### VADC3\_LC\_MDM\_INT\_POLARITY\_LOW

Bits	Name	Description
5	MIN_LOW_THR_INT_HIGH	Minimum Low threshold interrupt low polarity enabled 0x0: MIN_LOW_THR_INT_POL_LOW_DISABLED 0x1: MIN_LOW_THR_INT_POL_LOW_ENABLED
4	LOW_THR_INT_HIGH	Low threshold interrupt low polarity enabled 0x0: LOW_THR_INT_POL_LOW_DISABLED 0x1: LOW_THR_INT_POL_LOW_ENABLED
3	HIGH_THR_INT_HIGH	High threshold interrupt low polarity enabled 0x0: HIGH_THR_INT_POL_LOW_DISABLED 0x1: HIGH_THR_INT_POL_LOW_ENABLED
2	CONV_SEQ_TIMEOUT_INT _LOW	Conversion sequencer interrupt low polarity enabled 0x0: CONV_SEQ_TIMEOUT_INT_POL_LOW_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_POL_LOW_ENABLED
1	FIFO_NOT_EMPTY_INT_LO W	FIFO not empty interrupt low polarity enabled 0x0: FIFO_NOT_EMPTY_INT_POL_LOW_DISABLED 0x1: FIFO_NOT_EMPTY_INT_POL_LOW_ENABLED
0	EOC_INT_LOW	EOC interrupt low polarity enabled 0x0: EOC_INT_POL_LOW_DISABLED 0x1: EOC_INT_POL_LOW_ENABLED

### 0x00003214 VADC3\_LC\_MDM\_INT\_LATCHED\_CLR

Type: W

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Writing a '1' to a bit in this register will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

### VADC3\_LC\_MDM\_INT\_LATCHED\_CLR

Bits	Name	Description
5	MIN_LOW_THR_INT_LATC HED_CLR	Minimum Low threshold interrupt latched clear
4	LOW_THR_INT_LATCHED_ CLR	Low threshold interrupt latched clear
3	HIGH_THR_INT_LATCHED_ CLR	High threshold interrupt latched clear
2	CONV_SEQ_TIMEOUT_INT _LATCHED_CLR	Conversion sequencer interrupt latched clear

### VADC3\_LC\_MDM\_INT\_LATCHED\_CLR (cont.)

Bits	Name	Description
1	FIFO_NOT_EMPTY_INT_LA TCHED_CLR	FIFO not empty interrupt latched clear
0	EOC_INT_LATCHED_CLR	EOC interrupt latched clear

### 0x00003215 VADC3\_LC\_MDM\_INT\_EN\_SET

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Writing '0' to a bit in this register has no effect. Writing a '1' to a bit in this register will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### VADC3\_LC\_MDM\_INT\_EN\_SET

Bits	Name	Description
5	MIN_LOW_THR_INT_EN_S ET	Minimum Low threshold interrupt enable set 0x0: MIN_LOW_THR_INT_DISABLED 0x1: MIN_LOW_THR_INT_ENBLED
4	LOW_THR_INT_EN_SET	Low threshold interrupt enable set 0x0: LOW_THR_INT_DISABLED 0x1: LOW_THR_INT_ENBLED
3	HIGH_THR_INT_EN_SET	High threshold interrupt enable set 0x0: HIGH_THR_INT_DISABLED 0x1: HIGH_THR_INT_ENBLED
2	CONV_SEQ_TIMEOUT_INT _EN_SET	Conversion sequencer interrupt enable set 0x0: CONV_SEQ_TIMEOUT_INT_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_ENBLED
1	FIFO_NOT_EMPTY_INT_EN _SET	FIFO not empty interrupt enable set  0x0: FIFO_NOT_EMPTY_INT_DISABLED  0x1: FIFO_NOT_EMPTY_INT_ENBLED
0	EOC_INT_EN_SET	EOC interrupt enable set 0x0: EOC_INT_DISABLED 0x1: EOC_INT_ENBLED

### 0x00003216 VADC3\_LC\_MDM\_INT\_EN\_CLR

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Writing a '0' to a bit in this register has no effect. Writing a '1' to a bit in this register will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### VADC3 LC MDM INT EN CLR

Bits	Name	Description
5	MIN_LOW_THR_INT_EN_C LR	Minimum Low threshold interrupt enable clear 0x0: MIN_LOW_THR_INT_DISABLED 0x1: MIN_LOW_THR_INT_ENBLED
4	LOW_THR_INT_EN_CLR	Low threshold interrupt enable clear 0x0: LOW_THR_INT_DISABLED 0x1: LOW_THR_INT_ENBLED
3	HIGH_THR_INT_EN_CLR	High threshold interrupt enable clear 0x0: HIGH_THR_INT_DISABLED 0x1: HIGH_THR_INT_ENBLED
2	CONV_SEQ_TIMEOUT_INT _EN_CLR	Conversion sequencer interrupt enable clear 0x0: CONV_SEQ_TIMEOUT_INT_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_ENBLED
1	FIFO_NOT_EMPTY_INT_EN _CLR	FIFO not empty interrupt enable clear 0x0: FIFO_NOT_EMPTY_INT_DISABLED 0x1: FIFO_NOT_EMPTY_INT_ENBLED
0	EOC_INT_EN_CLR	EOC interrupt enable clear 0x0: EOC_INT_DISABLED 0x1: EOC_INT_ENBLED

### 0x00003218 VADC3\_LC\_MDM\_INT\_LATCHED\_STS

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

# VADC3\_LC\_MDM\_INT\_LATCHED\_STS

Bits	Name	Description
5	MIN_LOW_THR_INT_LATC HED_STS	Minimum Low threshold interrupt latched 0x0: MIN_LOW_THR_INT_LATCHED_FALSE 0x1: MIN_LOW_THR_INT_LATCHED_TRUE
4	LOW_THR_INT_LATCHED_ STS	Low threshold interrupt latched 0x0: LOW_THR_INT_LATCHED_FALSE 0x1: LOW_THR_INT_LATCHED_TRUE
3	HIGH_THR_INT_LATCHED_ STS	High threshold interrupt latched 0x0: HIGH_THR_INT_LATCHED_FALSE 0x1: HIGH_THR_INT_LATCHED_TRUE
2	CONV_SEQ_TIMEOUT_INT _LATCHED_STS	Conversion sequencer interrupt latched 0x0: CONV_SEQ_TIMEOUT_INT_LATCHED_FALSE 0x1: CONV_SEQ_TIMEOUT_INT_LATCHED_TRUE
1	FIFO_NOT_EMPTY_INT_LA TCHED_STS	FIFO not empty interrupt latched  0x0: FIFO_NOT_EMPTY_INT_LATCHED_FALSE  0x1: FIFO_NOT_EMPTY_INT_LATCHED_TRUE
0	EOC_INT_LATCHED_STS	EOC interrupt latched 0x0: EOC_INT_LATCHED_FALSE 0x1: EOC_INT_LATCHED_TRUE

# 0x00003219 VADC3\_LC\_MDM\_INT\_PENDING\_STS

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Debug: Pending is set if interrupt has been sent but not cleared.

# VADC3\_LC\_MDM\_INT\_PENDING\_STS

Bits	Name	Description
5	MIN_LOW_THR_INT_PENDI NG_STS	Minimum Low threshold interrupt pending 0x0: MIN_LOW_THR_INT_PENDING_FALSE 0x1: MIN_LOW_THR_INT_PENDING_TRUE
4	LOW_THR_INT_PENDING_ STS	Low threshold interrupt pending 0x0: LOW_THR_INT_PENDING_FALSE 0x1: LOW_THR_INT_PENDING_TRUE
3	HIGH_THR_INT_PENDING_ STS	High threshold interrupt pending 0x0: HIGH_THR_INT_PENDING_FALSE 0x1: HIGH_THR_INT_PENDING_TRUE

# VADC3\_LC\_MDM\_INT\_PENDING\_STS (cont.)

Bits	Name	Description
2	CONV_SEQ_TIMEOUT_INT _PENDING_STS	Conversion sequencer interrupt pending 0x0: CONV_SEQ_TIMEOUT_INT_PENDING_FALSE 0x1: CONV_SEQ_TIMEOUT_INT_PENDING_TRUE
1	FIFO_NOT_EMPTY_INT_PE NDING_STS	FIFO not empty interrupt pending 0x0: FIFO_NOT_EMPTY_INT_PENDING_FALSE 0x1: FIFO_NOT_EMPTY_INT_PENDING_TRUE
0	EOC_INT_PENDING_STS	EOC interrupt pending 0x0: EOC_INT_PENDING_FALSE 0x1: EOC_INT_PENDING_TRUE

# 0x0000321A VADC3\_LC\_MDM\_INT\_MID\_SEL

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Selects the MID that will receive the interrupt

# VADC3\_LC\_MDM\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	Selects the MID that will receive the interrupt

# 0x0000321B VADC3\_LC\_MDM\_INT\_PRIORITY

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Selects the SPMI interrupt priority

# VADC3\_LC\_MDM\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	Selects the SPMI interrupt priority 0x0: SR 0x1: A

# 0x00003240 VADC3\_LC\_MDM\_MODE\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x03

Reset Name: uvlo\_perph\_rb

Settings Common to Input and Output

# VADC3\_LC\_MDM\_MODE\_CTL

Bits	Name	Description
4:3	OP_MODE	Selects basic mode of operation:
		00=Normal Mode - Single measurement
		01=Conversion Sequencer - Single measurement using conversion sequencer
		10=Measurement Interval - Single or Continuous measurements at specified delay/interval
		0x0: NORM_MODE
		0x1: CONV_SEQ_MODE
	. ()	0x2: MEAS_INT_MODE
2	VREF_XO_THM_FORCE	When cleared, VDD_REF is connected to XO thermistor in active mode, disconnected in sleep mode
	27,10	When set, force VDD_REF to be connected to the XO thermistor regardless the status of sleepb
	O'S willis	0x0: VREF_XO_THM_FORCE_FALSE
	OJS WEN	0x1: VREF_XO_THM_FORCE_TRUE
1	RESERVED	
0	ADC_TRIM_EN	Enable ADC trim
		0x0: ADC_TRIM_DISABLED
		0x1: ADC_TRIM_ENABLED

Go.

# 0x00003246 VADC3\_LC\_MDM\_EN\_CTL1

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Enables ADC module.

# VADC3\_LC\_MDM\_EN\_CTL1

Bits	Name	Description
7	ADC_EN	Enables ADC module.
		0x0: ADC_DISABLED
		0x1: ADC_ENABLED

# 0x00003248 VADC3\_LC\_MDM\_ADC\_CH\_SEL\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x06

Reset Name: uvlo perph rb

ADC Channel selection. See device specification for channel descriptions.

# VADC3\_LC\_MDM\_ADC\_CH\_SEL\_CTL

Bits	Name	Description
7:0	ADC_CH_SEL	ADC Channel selection. See device specification for channel descriptions.

# 0x00003250 VADC3\_LC\_MDM\_ADC\_DIG\_PARAM

Type: RW

Clock: pbus\_wrclk Reset State: 0x04

Reset Name: uvlo perph rb

**ADC** Digital Parameters

# VADC3\_LC\_MDM\_ADC\_DIG\_PARAM

Bits	Name	Description
3:2	DEC_RATIO_SEL	Decimation ratio: 0x0: DECI_512 0x1: DECI_1K 0x2: DECI_2K 0x3: DECI_4K
1:0	CLK_SEL	Select ADC clock rate:  0x0: CLK_SEL_2P4MHZ  0x1: CLK_SEL_4P8MHZ  0x2: CLK_SEL_9P6MHZ  0x3: CLK_SEL_19P2MHZ

# 0x00003251 VADC3\_LC\_MDM\_HW\_SETTLE\_DELAY

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Settle Delay

# VADC3\_LC\_MDM\_HW\_SETTLE\_DELAY

Bits	Name	Description
3:0	Name  HW_SETTLE_DELAY	Description  Time between AMUX getting configured and the ADC starting conversion. Delay = 100us*(value) for value<11, and 2ms*(value-10) otherwise  0x0: HW_SETTLE_DELAY_0US  0x1: HW_SETTLE_DELAY_100US  0x2: HW_SETTLE_DELAY_200US  0x3: HW_SETTLE_DELAY_300US  0x4: HW_SETTLE_DELAY_400US  0x5: HW_SETTLE_DELAY_500US  0x6: HW_SETTLE_DELAY_600US  0x7: HW_SETTLE_DELAY_700US  0x8: HW_SETTLE_DELAY_800US  0x9: HW_SETTLE_DELAY_900US  0xA: HW_SETTLE_DELAY_1MS  0xB: HW_SETTLE_DELAY_1MS  0xC: HW_SETTLE_DELAY_4MS  0xD: HW_SETTLE_DELAY_4MS
		0xE: HW_SETTLE_DELAY_8MS 0xF: HW_SETTLE_DELAY_10MS

# 0x00003252 VADC3\_LC\_MDM\_CONV\_REQ

Type: W

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: req\_rb

Conversion Request

# VADC3\_LC\_MDM\_CONV\_REQ

Bits	Name	Description
7	REQ	Conversion request strobe. When bit is asserted the arbiter stores a descriptor in the conversion request queue. Bit is cleared when ADC conversion is completed.  0x0: CONV_REQ_FALSE  0x1: CONV_REQ_TRUE

# 0x00003254 VADC3\_LC\_MDM\_CONV\_SEQ\_CTL

**Type:** RW

Clock: pbus\_wrclk
Reset State: 0x45

Reset Name: uvlo perph rb

**Conversion Sequencer Control** 

# VADC3\_LC\_MDM\_CONV\_SEQ\_CTL

Bits	Name	Description
7:4	CONV_SEQ_HOLDOFF	Select delay from conversion trigger signal (i.e. adc_conv_seq_trig) transition to ADC enable. Delay = 25us*(value+1). Actual delay will be longer if request is stored in a non empty FIFO and/or conversion needs to wait for LDO OK handshake.  0x0: SEQ_HOLD_25US 0x1: SEQ_HOLD_50US 0x2: SEQ_HOLD_75US 0x3: SEQ_HOLD_100US 0x4: SEQ_HOLD_125US 0x5: SEQ_HOLD_125US 0x6: SEQ_HOLD_175US 0x7: SEQ_HOLD_200US 0x8: SEQ_HOLD_225US 0x9: SEQ_HOLD_250US 0x9: SEQ_HOLD_250US 0xA: SEQ_HOLD_350US 0xC: SEQ_HOLD_325US 0xC: SEQ_HOLD_355US 0xC: SEQ_HOLD_355US
		0xF: SEQ_HOLD_400US

# VADC3\_LC\_MDM\_CONV\_SEQ\_CTL (cont.)

Bits	Name	Description
3:0	CONV_SEQ_TIMEOUT	Select delay (0 to 15ms) from conversion request to triggering conversion sequencer hold off timer.
		0x0: SEQ_TIMEOUT_0MS
		0x1: SEQ_TIMEOUT_1MS
		0x2: SEQ_TIMEOUT_2MS
		0x3: SEQ_TIMEOUT_3MS
		0x4: SEQ_TIMEOUT_4MS
		0x5: SEQ_TIMEOUT_5MS
		0x6: SEQ_TIMEOUT_6MS
		0x7: SEQ_TIMEOUT_7MS
		0x8: SEQ_TIMEOUT_8MS
		0x9: SEQ_TIMEOUT_9MS
		0xA: SEQ_TIMEOUT_10MS
		0xB: SEQ_TIMEOUT_11MS
		0xC: SEQ_TIMEOUT_12MS
	<b>~</b> (	0xD: SEQ_TIMEOUT_13MS
		0xE: SEQ_TIMEOUT_14MS
		0xF: SEQ_TIMEOUT_15MS

# 0x00003255 VADC3\_LC\_MDM\_CONV\_SEQ\_TRIG\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Conversion Sequencer Trigger Select

# VADC3\_LC\_MDM\_CONV\_SEQ\_TRIG\_CTL

Bits	Name	Description
7	CONV_SEQ_TRIG_COND	Select conversion trigger condition(s) that starts ADC conversion hold off timer.  0x0 - Falling edge  0x1 - Rising edge  0x0: FALLING_EDGE  0x1: RISING_EDGE
1:0	CONV_SEQ_TRIG_SEL	Select conversion sequencer trigger input signal.  0x0: ADC_TRIG0  0x1: ADC_TRIG1  0x2: ADC_TRIG2  0x3: ADC_TRIG3

# 0x00003257 VADC3\_LC\_MDM\_MEAS\_INTERVAL\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo perph rb

Interval Mode Control

# VADC3\_LC\_MDM\_MEAS\_INTERVAL\_CTL

3:0 MEAS_INTERVAL_TIME  Select measurement interval time (i.e., If value=0, use 0ms, else use 2^(value+4)/32768).  0x0: MEAS_INTERVAL_0MS  0x1: MEAS_INTERVAL_1P0MS  0x2: MEAS_INTERVAL_2P0MS  0x3: MEAS_INTERVAL_3P9MS  0x4: MEAS_INTERVAL_7P8MS  0x5: MEAS_INTERVAL_15P6MS  0x6: MEAS_INTERVAL_31P3MS  0x7: MEAS_INTERVAL_62P5MS  0x8: MEAS_INTERVAL_125MS	Bits	Name	Description
0x9: MEAS_INTERVAL_250MS 0xA: MEAS_INTERVAL_500MS 0xB: MEAS_INTERVAL_1S 0xC: MEAS_INTERVAL_2S 0xD: MEAS_INTERVAL_4S 0xE: MEAS_INTERVAL_8S 0xF: MEAS_INTERVAL_16S			Select measurement interval time (i.e., If value=0, use 0ms, else use 2^(value+4)/32768).  0x0: MEAS_INTERVAL_0MS  0x1: MEAS_INTERVAL_1P0MS  0x2: MEAS_INTERVAL_2P0MS  0x3: MEAS_INTERVAL_3P9MS  0x4: MEAS_INTERVAL_7P8MS  0x5: MEAS_INTERVAL_15P6MS  0x6: MEAS_INTERVAL_31P3MS  0x7: MEAS_INTERVAL_62P5MS  0x8: MEAS_INTERVAL_125MS  0x9: MEAS_INTERVAL_250MS  0x9: MEAS_INTERVAL_500MS  0xA: MEAS_INTERVAL_1S  0xC: MEAS_INTERVAL_1S  0xC: MEAS_INTERVAL_2S  0xD: MEAS_INTERVAL_4S  0xE: MEAS_INTERVAL_4S

# 0x00003259 VADC3\_LC\_MDM\_MEAS\_INTERVAL\_OP\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Interval mode select

# VADC3\_LC\_MDM\_MEAS\_INTERVAL\_OP\_CTL

Bits	Name	Description
7	MEAS_INTERVAL_OP	Interval mode select 0x0: INTERVAL_MODE_DISABLED 0x1: INTERVAL_MODE_ENABLED

# 0x0000325A VADC3\_LC\_MDM\_FAST\_AVG\_CTL

**Type:** RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Fast Average Control

# VADC3\_LC\_MDM\_FAST\_AVG\_CTL

Bits	Name	Description
3:0	FAST_AVG_SAMPLES	Select number of samples for use in fast average mode (i.e. 2^(value).
		0x0: AVG_1_SAMPLE
		0x1: AVG_2_SAMPLES
		0x2: AVG_4_SAMPLES
	× (	0x3: AVG_8_SAMPLES
		0x4: AVG_16_SAMPLES
		0x5: AVG_32_SAMPLES
		0x6: AVG_64_SAMPLES
		0x7: AVG_128_SAMPLES
		0x8: AVG_256_SAMPLES
	25	0x9: AVG_512_SAMPLES

# 0x0000325B VADC3\_LC\_MDM\_FAST\_AVG\_EN

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Fast Average Enable

# VADC3\_LC\_MDM\_FAST\_AVG\_EN

Bits	Name	Description
7	FAST_AVG_EN	Select low latency for multiple conversions 0x0: FAST_AVG_DISABLED 0x1: FAST_AVG_ENABLED

# 0x0000325C VADC3\_LC\_MDM\_LOW\_THR0

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Low Threshold Byte 0

#### VADC3\_LC\_MDM\_LOW\_THR0

Bits	Name	Description
7:0	LOW_THR_7_0	Low byte of low threshold detector

# 0x0000325D VADC3\_LC\_MDM\_LOW\_THR1

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Low Threshold Byte 1

# VADC3\_LC\_MDM\_LOW\_THR1

Bits	Name	Description
7:0	LOW_THR_15_8	High byte of low threshold detector

# 0x0000325E VADC3\_LC\_MDM\_HIGH\_THR0

Type: RW

Clock: pbus\_wrclk
Reset State: 0xFF

Reset Name: uvlo\_perph\_rb

High Threshold Byte 0

# VADC3\_LC\_MDM\_HIGH\_THR0

Bits	Name	Description
7:0	HIGH_THR_7_0	Low byte of high threshold detector

# 0x0000325F VADC3\_LC\_MDM\_HIGH\_THR1

Type: RW

Clock: pbus\_wrclk Reset State: 0xFF

Reset Name: uvlo perph rb

High Threshold Byte 1

#### VADC3\_LC\_MDM\_HIGH\_THR1

Bits	Name	Description
7:0	HIGH_THR_15_8	High byte of high threshold detector

#### 

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: uvlo perph rb

ADC Sample Byte 0

# VADC3\_LC\_MDM\_DATA0

Bits	Name	Description
7:0	DATA_7_0	Low byte of ADC output

#### 

**Type:** R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: uvlo\_perph\_rb

ADC Sample Byte 1

# VADC3\_LC\_MDM\_DATA1

Bits	Name	Description
7:0	DATA_15_8	High byte of ADC output

# 0x00003262 VADC3\_LC\_MDM\_MIN\_LOW\_THR0

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Minimum Low Threshold Byte 0

#### VADC3\_LC\_MDM\_MIN\_LOW\_THR0

Bits	Name	Description
7:0	MIN_LOW_THR_7_0	Low byte of minimum low threshold detector

# 0x00003263 VADC3\_LC\_MDM\_MIN\_LOW\_THR1

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Minimum Low Threshold Byte 1

# VADC3\_LC\_MDM\_MIN\_LOW\_THR1

Bits	Name	Description
7:0	MIN_LOW_THR_15_8	High byte of minimum low threshold detector

# 0x00003266 VADC3\_LC\_MDM\_MIN\_DATA0

**Type:** R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: uvlo perph rb

Minimum ADC Sample Byte 0

#### VADC3\_LC\_MDM\_MIN\_DATA0

Bits	Name	Description
7:0	MIN_DATA_7_0	Low byte of minimum ADC output

# 0x00003267 VADC3\_LC\_MDM\_MIN\_DATA1

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: uvlo perph rb

Minimum ADC Sample Byte 1

# VADC3\_LC\_MDM\_MIN\_DATA1

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E	Bits	Name	Description
	7:0	MIN_DATA_15_8	High byte of minimum ADC output

# 15 Vadc\_btm2 Registers

# 0x00003400 VADC2\_LC\_BTM\_2\_REVISION1

Type: R

Clock: pbus\_wrclk Reset State: 0x02

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

# VADC2\_LC\_BTM\_2\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00003401 VADC2\_LC\_BTM\_2\_REVISION2

Type: R

Clock: pbus\_wrclk Reset State: 0x02

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

# VADC2\_LC\_BTM\_2\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

# 0x00003402 VADC2\_LC\_BTM\_2\_REVISION3

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### VADC2\_LC\_BTM\_2\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00003403 VADC2\_LC\_BTM\_2\_REVISION4

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

# VADC2\_LC\_BTM\_2\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

# 0x00003404 VADC2\_LC\_BTM\_2\_PERPH\_TYPE

Type: R

Clock: pbus\_wrclk Reset State: 0x08

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

# VADC2\_LC\_BTM\_2\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	ADC

# 0x00003405 VADC2\_LC\_BTM\_2\_PERPH\_SUBTYPE

Type: R

Clock: pbus\_wrclk Reset State: 0x22

Reset Name: N/A

Peripheral SubType

# VADC2\_LC\_BTM\_2\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	ADC sub type

#### 

Type: R

Clock: pbus\_wrclk Reset State: 0x01

Reset Name: N/A

Status Registers

# VADC2\_LC\_BTM\_2\_STATUS1

Bits	Name	Description
4:3	OP_MODE	Selects basic mode of operation
		0x0: NORM_MODE
		0x1: CONV_SEQ_MODE
		0x2: MEAS_INT_MODE
2	MEAS_INTERVAL_EN_STS	Interval Mode
		0x0: INTERVAL_MODE_DISABLED
		0x1: INTERVAL_MODE_ENABLED
1	REQ_STS	REQ_STS mirrors the REQ bit. When REQ is asserted the arbiter stores a descriptor in the conversion request queue. Bit is cleared when ADC conversion is completed.
		0x0: REQ_NOT_IN_PROGRESS
		0x1: REQ_IN_PROGRESS

# VADC2\_LC\_BTM\_2\_STATUS1 (cont.)

Bits	Name	Description
0	EOC	End of conversion status flag. Bit is de-asserted when arbiter is servicing a conversion request and asserted when conversion is completed. After a conversion is requested, the EOC and REQ_STS bits can be polled to determine ADC conversion status as follows:  REQ_STS EOC Arbiter state  1 1 Waiting for ADC to complete another process's conversion request.  1 0 ADC conversion occurring.  0 1 ADC conversion completed.  0 0 Invalid  0x0: CONV_NOT_COMPLETE  0x1: CONV_COMPLETE

# 0x0000340A VADC2\_LC\_BTM\_2\_STATUS\_LOW

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

Indicates measurement(s) where VADC read is less than low threshold.

# VADC2\_LC\_BTM\_2\_STATUS\_LOW

Bits	Name	Description
1	M1_LOW	M1 measurement under low threshold 0x0: M1_LOW_FALSE 0x1: M1_LOW_TRUE
0	M0_LOW	M0 measurement under low threshold 0x0: M0_LOW_FALSE 0x1: M0_LOW_TRUE

# 0x0000340B VADC2\_LC\_BTM\_2\_STATUS\_HIGH

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

Indicates measurement(s) where VADC read is greater than high threshold.

# VADC2\_LC\_BTM\_2\_STATUS\_HIGH

Bits	Name	Description
1	M1_HIGH	M1 measurement above high threshold 0x0: M1_HIGH_FALSE 0x1: M1_HIGH_TRUE
0	M0_HIGH	M0 measurement above high threshold 0x0: M0_HIGH_FALSE 0x1: M0_HIGH_TRUE

# 0x00003410 VADC2\_LC\_BTM\_2\_INT\_RT\_STS

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

0 =use level trigger interrupts, 1 =use edge trigger interrupts

# VADC2\_LC\_BTM\_2\_INT\_RT\_STS

Bits	Name	Description
4	LOW_THR_INT_RT_STS	Low threshold interrupt set type 0x0: LOW_THR_INT_LEVEL 0x1: LOW_THR_INT_EDGE
3	HIGH_THR_INT_RT_STS	High threshold interrupt set type 0x0: HIGH_THR_INT_LEVEL 0x1: HIGH_THR_INT_EDGE
2	CONV_SEQ_TIMEOUT_INT _RT_STS	Conversion sequencer timeout interrupt set type 0x0: CONV_SEQ_TIMEOUT_LEVEL 0x1: CONV_SEQ_TIMEOUT_EDGE
1	FIFO_NOT_EMPTY_INT_RT _STS	FIFO not empty interrupt set type 0x0: FIFO_NOT_EMPTY_LEVEL 0x1: FIFO_NOT_EMPTY_EDGE
0	EOC_INT_RT_STS	EOC interrupt set type 0x0: EOC_LEVEL 0x1: EOC_EDGE

# 0x00003411 VADC2\_LC\_BTM\_2\_INT\_SET\_TYPE

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

# VADC2\_LC\_BTM\_2\_INT\_SET\_TYPE

Bits	Name	Description
4	LOW_THR_INT_SET_TYPE	Low threshold interrupt high polarity enabled 0x0: LOW_THR_INT_POL_HIGH_DISABLED 0x1: LOW_THR_INT_POL_HIGH_ENABLED
3	HIGH_THR_INT_SET_TYPE	High threshold interrupt high polarity enabled 0x0: HIGH_THR_INT_POL_HIGH_DISABLED 0x1: HIGH_THR_INT_POL_HIGH_ENABLED
2	CONV_SEQ_TIMEOUT_INT _SET_TYPE	Conversion sequencer interrupt high polarity enabled 0x0: CONV_SEQ_TIMEOUT_INT_POL_HIGH_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_POL_HIGH_ENABLED
1	FIFO_NOT_EMPTY_INT_SE T_TYPE	FIFO not empty interrupt high polarity enabled 0x0: FIFO_NOT_EMPTY_INT_POL_HIGH_DISABLED 0x1: FIFO_NOT_EMPTY_INT_POL_HIGH_ENABLED
0	EOC_SET_INT_TYPE	EOC interrupt high polarity enabled  0x0: EOC_INT_POL_HIGH_DISABLED  0x1: EOC_INT_POL_HIGH_ENABLED

# 0x00003412 VADC2\_LC\_BTM\_2\_INT\_POLARITY\_HIGH

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

# VADC2\_LC\_BTM\_2\_INT\_POLARITY\_HIGH

Bits	Name	Description
4	LOW_THR_INT_HIGH	Low threshold interrupt low polarity enabled  0x0: LOW_THR_INT_POL_LOW_DISABLED  0x1: LOW_THR_INT_POL_LOW_ENABLED

# VADC2\_LC\_BTM\_2\_INT\_POLARITY\_HIGH (cont.)

Bits	Name	Description
3	HIGH_THR_INT_HIGH	High threshold interrupt low polarity enabled 0x0: HIGH_THR_INT_POL_LOW_DISABLED 0x1: HIGH_THR_INT_POL_LOW_ENABLED
2	CONV_SEQ_TIMEOUT_INT _HIGH	Conversion sequencer interrupt low polarity enabled 0x0: CONV_SEQ_TIMEOUT_INT_POL_LOW_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_POL_LOW_ENABLED
1	FIFO_NOT_EMPTY_INT_HI GH	FIFO not empty interrupt low polarity enabled 0x0: FIFO_NOT_EMPTY_INT_POL_LOW_DISABLED 0x1: FIFO_NOT_EMPTY_INT_POL_LOW_ENABLED
0	EOC_INT_HIGH	EOC interrupt low polarity enabled  0x0: EOC_INT_POL_LOW_DISABLED  0x1: EOC_INT_POL_LOW_ENABLED

# 0x00003413 VADC2\_LC\_BTM\_2\_INT\_POLARITY\_LOW

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

# VADC2\_LC\_BTM\_2\_INT\_POLARITY\_LOW

Bits	Name	Description
4	LOW_THR_INT_HIGH	Low threshold interrupt low polarity enabled 0x0: LOW_THR_INT_POL_LOW_DISABLED 0x1: LOW_THR_INT_POL_LOW_ENABLED
3	HIGH_THR_INT_HIGH	High threshold interrupt low polarity enabled 0x0: HIGH_THR_INT_POL_LOW_DISABLED 0x1: HIGH_THR_INT_POL_LOW_ENABLED
2	CONV_SEQ_TIMEOUT_INT _LOW	Conversion sequencer interrupt low polarity enabled 0x0: CONV_SEQ_TIMEOUT_INT_POL_LOW_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_POL_LOW_ENABLED
1	FIFO_NOT_EMPTY_INT_LO W	FIFO not empty interrupt low polarity enabled 0x0: FIFO_NOT_EMPTY_INT_POL_LOW_DISABLED 0x1: FIFO_NOT_EMPTY_INT_POL_LOW_ENABLED
0	EOC_INT_LOW	EOC interrupt low polarity enabled 0x0: EOC_INT_POL_LOW_DISABLED 0x1: EOC_INT_POL_LOW_ENABLED

# 0x00003414 VADC2\_LC\_BTM\_2\_INT\_LATCHED\_CLR

Type: W

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Writing a '1' to a bit in this register will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

# VADC2\_LC\_BTM\_2\_INT\_LATCHED\_CLR

Bits	Name	Description
4	LOW_THR_INT_LATCHED_ CLR	Low threshold interrupt latched clear
3	HIGH_THR_INT_LATCHED_ CLR	High threshold interrupt latched clear
2	CONV_SEQ_TIMEOUT_INT _LATCHED_CLR	Conversion sequencer interrupt latched clear
1	FIFO_NOT_EMPTY_INT_LA TCHED_CLR	FIFO not empty interrupt latched clear
0	EOC_INT_LATCHED_CLR	EOC interrupt latched clear

# 0x00003415 VADC2\_LC\_BTM\_2\_INT\_EN\_SET

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Writing '0' to a bit in this register has no effect. Writing a '1' to a bit in this register will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

# VADC2\_LC\_BTM\_2\_INT\_EN\_SET

Bits	Name	Description
4	LOW_THR_INT_EN_SET	Low threshold interrupt enable set  0x0: LOW_THR_INT_DISABLED  0x1: LOW_THR_INT_ENBLED
3	HIGH_THR_INT_EN_SET	High threshold interrupt enable set 0x0: HIGH_THR_INT_DISABLED 0x1: HIGH_THR_INT_ENBLED

# VADC2\_LC\_BTM\_2\_INT\_EN\_SET (cont.)

Bits	Name	Description
2	CONV_SEQ_TIMEOUT_INT _EN_SET	Conversion sequencer interrupt enable set 0x0: CONV_SEQ_TIMEOUT_INT_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_ENBLED
1	FIFO_NOT_EMPTY_INT_EN _SET	FIFO not empty interrupt enable set  0x0: FIFO_NOT_EMPTY_INT_DISABLED  0x1: FIFO_NOT_EMPTY_INT_ENBLED
0	EOC_INT_EN_SET	EOC interrupt enable set 0x0: EOC_INT_DISABLED 0x1: EOC_INT_ENBLED

# 0x00003416 VADC2\_LC\_BTM\_2\_INT\_EN\_CLR

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Writing a '0' to a bit in this register has no effect. Writing a '1' to a bit in this register will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

# VADC2\_LC\_BTM\_2\_INT\_EN\_CLR

Bits	Name	Description
4	LOW_THR_INT_EN_CLR	Low threshold interrupt enable clear 0x0: LOW_THR_INT_DISABLED 0x1: LOW_THR_INT_ENBLED
3	HIGH_THR_INT_EN_CLR	High threshold interrupt enable clear 0x0: HIGH_THR_INT_DISABLED 0x1: HIGH_THR_INT_ENBLED
2	CONV_SEQ_TIMEOUT_INT _EN_CLR	Conversion sequencer interrupt enable clear 0x0: CONV_SEQ_TIMEOUT_INT_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_ENBLED
1	FIFO_NOT_EMPTY_INT_EN _CLR	FIFO not empty interrupt enable clear 0x0: FIFO_NOT_EMPTY_INT_DISABLED 0x1: FIFO_NOT_EMPTY_INT_ENBLED
0	EOC_INT_EN_CLR	EOC interrupt enable clear 0x0: EOC_INT_DISABLED 0x1: EOC_INT_ENBLED

# 0x00003418 VADC2\_LC\_BTM\_2\_INT\_LATCHED\_STS

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

# VADC2\_LC\_BTM\_2\_INT\_LATCHED\_STS

Bits	Name	Description
4	LOW_THR_INT_LATCHED_ STS	Low threshold interrupt latched 0x0: LOW_THR_INT_LATCHED_FALSE 0x1: LOW_THR_INT_LATCHED_TRUE
3	HIGH_THR_INT_LATCHED_ STS	High threshold interrupt latched 0x0: HIGH_THR_INT_LATCHED_FALSE 0x1: HIGH_THR_INT_LATCHED_TRUE
2	CONV_SEQ_TIMEOUT_INT _LATCHED_STS	Conversion sequencer interrupt latched  0x0: CONV_SEQ_TIMEOUT_INT_LATCHED_FALSE  0x1: CONV_SEQ_TIMEOUT_INT_LATCHED_TRUE
1	FIFO_NOT_EMPTY_INT_LA TCHED_STS	FIFO not empty interrupt latched  0x0: FIFO_NOT_EMPTY_INT_LATCHED_FALSE  0x1: FIFO_NOT_EMPTY_INT_LATCHED_TRUE
0	EOC_INT_LATCHED_STS	EOC interrupt latched 0x0: EOC_INT_LATCHED_FALSE 0x1: EOC_INT_LATCHED_TRUE

# 0x00003419 VADC2\_LC\_BTM\_2\_INT\_PENDING\_STS

**Type:** R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

# VADC2\_LC\_BTM\_2\_INT\_PENDING\_STS

Bits	Name	Description
4	LOW_THR_INT_PENDING_ STS	Low threshold interrupt pending 0x0: LOW_THR_INT_PENDING_FALSE 0x1: LOW_THR_INT_PENDING_TRUE

# VADC2\_LC\_BTM\_2\_INT\_PENDING\_STS (cont.)

Bits	Name	Description
3	HIGH_THR_INT_PENDING_ STS	High threshold interrupt pending 0x0: HIGH_THR_INT_PENDING_FALSE 0x1: HIGH_THR_INT_PENDING_TRUE
2	CONV_SEQ_TIMEOUT_INT _PENDING_STS	Conversion sequencer interrupt pending 0x0: CONV_SEQ_TIMEOUT_INT_PENDING_FALSE 0x1: CONV_SEQ_TIMEOUT_INT_PENDING_TRUE
1	FIFO_NOT_EMPTY_INT_PE NDING_STS	FIFO not empty interrupt pending 0x0: FIFO_NOT_EMPTY_INT_PENDING_FALSE 0x1: FIFO_NOT_EMPTY_INT_PENDING_TRUE
0	EOC_INT_PENDING_STS	EOC interrupt pending 0x0: EOC_INT_PENDING_FALSE 0x1: EOC_INT_PENDING_TRUE

# 0x0000341A VADC2\_LC\_BTM\_2\_INT\_MID\_SEL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo perph rb

Selects the MID that will receive the interrupt

# VADC2\_LC\_BTM\_2\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	Selects the MID that will receive the interrupt

# 0x0000341B VADC2\_LC\_BTM\_2\_INT\_PRIORITY

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Selects the SPMI interrupt priority

# VADC2\_LC\_BTM\_2\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	Selects the SPMI interrupt priority 0x0: SR 0x1: A

# 0x00003440 VADC2\_LC\_BTM\_2\_MODE\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x03

Reset Name: uvlo perph rb

Settings Common to Input and Output

# VADC2\_LC\_BTM\_2\_MODE\_CTL

Bits	Name	Description
4:3	OP_MODE	Selects basic mode of operation:  00=Normal Mode - Single measurement  01=Conversion Sequencer - Single measurement using conversion sequencer  10=Measurement Interval - Single or Continuous measurements at specified delay/interval  0x0: NORM_MODE  0x1: CONV_SEQ_MODE  0x2: MEAS_INT_MODE
2	VREF_XO_THM_FORCE	When cleared, VDD_REF is connected to XO thermistor in active mode, disconnected in sleep mode When set, force VDD_REF to be connected to the XO thermistor regardless the status of sleepb 0x0: VREF_XO_THM_FORCE_FALSE 0x1: VREF_XO_THM_FORCE_TRUE
1	RESERVED	
0	ADC_TRIM_EN	Enable ADC trim 0x0: ADC_TRIM_DISABLED 0x1: ADC_TRIM_ENABLED

# 0x00003441 VADC2\_LC\_BTM\_2\_MULTI\_MEAS\_EN

Type: RW

Clock: pbus\_wrclk Reset State: 0x01

Reset Name: uvlo perph rb

Measurement enabled when bit is high

#### VADC2\_LC\_BTM\_2\_MULTI\_MEAS\_EN

Bits	Name	Description
1	M1_MEAS_EN	Enables measurement M1 in auto-sequence
		0x0: M1_MEAS_DISABLE
		0x1: M1_MEAS_ENABLE
0	M0_MEAS_EN	Enables measurement M0 in auto-sequence
		0x0: M0_MEAS_DISABLE
		0x1: M0_MEAS_ENABLE

# 0x00003442 VADC2\_LC\_BTM\_2\_LOW\_THR\_INT\_EN

Type: RW

Clock: pbus\_wrclk Reset State: 0x01

Reset Name: uvlo perph rb

Measurement's low threshold is used to trigger threshold interrupt when bit is high,,,,'

#### VADC2\_LC\_BTM\_2\_LOW\_THR\_INT\_EN

Bits	Name	Description
1	M1_LOW_THR_INT_EN	Enables M1 low threshold for interrupt
		0x0: M1_LOW_THR_INT_DISABLED
		0x1: M1_LOW_THR_INT_ENABLED
0	M0_LOW_THR_INT_EN	Enables M0 low threshold for interrupt
		0x0: M0_LOW_THR_INT_DISABLED
		0x1: M0_LOW_THR_INT_ENABLED

# 0x00003443 VADC2\_LC\_BTM\_2\_HIGH\_THR\_INT\_EN

Type: RW

Clock: pbus\_wrclk Reset State: 0x01

Reset Name: uvlo perph rb

Measurement's high threshold is used to trigger threshold interrupt when bit is high,,,,,'

# VADC2\_LC\_BTM\_2\_HIGH\_THR\_INT\_EN

Bits	Name	Description
1	M1_HIGH_THR_INT_EN	Enables M1 high threshold for interrupt
		0x0: M1_HIGH_THR_INT_DISABLED
		0x1: M1_HIGH_THR_INT_ENABLED
0	M0_HIGH_THR_INT_EN	Enables M0 high threshold for interrupt
		0x0: M0_HIGH_THR_INT_DISABLED
		0x1: M0_HIGH_THR_INT_ENABLED

#### 

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Enables ADC module.

#### VADC2 LC BTM 2 EN CTL1

Bits		Name	Description
7	ADC_EN	JOJ SWE	Enables ADC module. 0x0: ADC_DISABLED 0x1: ADC_ENABLED

# 0x00003448 VADC2\_LC\_BTM\_2\_M0\_ADC\_CH\_SEL\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0xFF

Reset Name: uvlo perph rb

M0 ADC Channel selection. See device specification for channel descriptions.

# VADC2\_LC\_BTM\_2\_M0\_ADC\_CH\_SEL\_CTL

Bits	Name	Description
7:0	ADC_CH_SEL	M0 ADC Channel selection. See device specification for channel descriptions.

# 0x00003450 VADC2\_LC\_BTM\_2\_ADC\_DIG\_PARAM

Type: RW

Clock: pbus\_wrclk
Reset State: 0x04

Reset Name: uvlo\_perph\_rb

**ADC Digital Parameters** 

# VADC2\_LC\_BTM\_2\_ADC\_DIG\_PARAM

Bits	Name	Description
3:2	DEC_RATIO_SEL	Decimation ratio: 0x0: DECI_512 0x1: DECI_1K 0x2: DECI_2K
1:0	CLK_SEL	0x3: DECI_4K  Select ADC clock rate: 0x0: CLK_SEL_2P4MHZ 0x1: CLK_SEL_4P8MHZ 0x2: CLK_SEL_9P6MHZ 0x3: CLK_SEL_19P2MHZ

# 0x00003451 VADC2\_LC\_BTM\_2\_HW\_SETTLE\_DELAY

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Settle Delay

# VADC2\_LC\_BTM\_2\_HW\_SETTLE\_DELAY

Bits	Name	Description
3:0	HW_SETTLE_DELAY	Time between AMUX getting configured and the ADC starting conversion. Delay = 100us*(value) for value<11, and 2ms*(value-10) otherwise
		0x0: HW_SETTLE_DELAY_0US
		0x1: HW_SETTLE_DELAY_100US
		0x2: HW_SETTLE_DELAY_200US
		0x3: HW_SETTLE_DELAY_300US
		0x4: HW_SETTLE_DELAY_400US
		0x5: HW_SETTLE_DELAY_500US
		0x6: HW_SETTLE_DELAY_600US
		0x7: HW_SETTLE_DELAY_700US
		0x8: HW_SETTLE_DELAY_800US
		0x9: HW_SETTLE_DELAY_900US
		0xA: HW_SETTLE_DELAY_1MS
		0xB: HW_SETTLE_DELAY_2MS
		0xC: HW_SETTLE_DELAY_4MS
		0xD: HW_SETTLE_DELAY_6MS
		0xE: HW_SETTLE_DELAY_8MS
		0xF: HW_SETTLE_DELAY_10MS

# 0x00003452 VADC2\_LC\_BTM\_2\_CONV\_REQ

Type: W

Clock: pbus\_wrclk Reset State: 0x00

**Reset Name:** req\_rb

Conversion Request

# VADC2\_LC\_BTM\_2\_CONV\_REQ

Bits	Name	Description
7	REQ	Conversion request strobe. When bit is asserted the arbiter stores a descriptor in the conversion request queue. Bit is cleared when ADC conversion is completed.  0x0: CONV_REQ_FALSE  0x1: CONV_REQ_TRUE

# 0x00003454 VADC2\_LC\_BTM\_2\_CONV\_SEQ\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x45

Reset Name: uvlo\_perph\_rb

Conversion Sequencer Control

# VADC2\_LC\_BTM\_2\_CONV\_SEQ\_CTL

Bits	Name	Description
7:4	CONV_SEQ_HOLDOFF	Select delay from conversion trigger signal (i.e. adc_conv_seq_trig) transition to ADC enable. Delay = 25us*(value+1). Actual delay will be longer if request is stored in a non empty FIFO and/or conversion needs to wait for LDO OK handshake.  0x0: SEQ_HOLD_25US 0x1: SEQ_HOLD_50US 0x2: SEQ_HOLD_75US 0x3: SEQ_HOLD_100US 0x4: SEQ_HOLD_125US 0x5: SEQ_HOLD_150US 0x6: SEQ_HOLD_155US 0x7: SEQ_HOLD_175US 0x7: SEQ_HOLD_200US 0x8: SEQ_HOLD_225US 0x9: SEQ_HOLD_255US 0x9: SEQ_HOLD_255US 0xA: SEQ_HOLD_300US 0xC: SEQ_HOLD_300US 0xC: SEQ_HOLD_355US 0xD: SEQ_HOLD_355US 0xF: SEQ_HOLD_375US 0xF: SEQ_HOLD_400US

# VADC2\_LC\_BTM\_2\_CONV\_SEQ\_CTL (cont.)

Bits	Name	Description
3:0	CONV_SEQ_TIMEOUT	Select delay (0 to 15ms) from conversion request to triggering conversion sequencer hold off timer.
		0x0: SEQ_TIMEOUT_0MS
		0x1: SEQ_TIMEOUT_1MS
		0x2: SEQ_TIMEOUT_2MS
		0x3: SEQ_TIMEOUT_3MS
		0x4: SEQ_TIMEOUT_4MS
		0x5: SEQ_TIMEOUT_5MS
		0x6: SEQ_TIMEOUT_6MS
		0x7: SEQ_TIMEOUT_7MS
		0x8: SEQ_TIMEOUT_8MS
		0x9: SEQ_TIMEOUT_9MS
		0xA: SEQ_TIMEOUT_10MS
		0xB: SEQ_TIMEOUT_11MS
		0xC: SEQ_TIMEOUT_12MS
	<b>~</b> (	0xD: SEQ_TIMEOUT_13MS
		0xE: SEQ_TIMEOUT_14MS
		0xF: SEQ_TIMEOUT_15MS

# 0x00003455 VADC2\_LC\_BTM\_2\_CONV\_SEQ\_TRIG\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Conversion Sequencer Trigger Select

# VADC2\_LC\_BTM\_2\_CONV\_SEQ\_TRIG\_CTL

Bits	Name	Description
7	CONV_SEQ_TRIG_COND	Select conversion trigger condition(s) that starts ADC conversion hold off timer.  0x0: FALLING_EDGE  0x1: RISING_EDGE
1:0	CONV_SEQ_TRIG_SEL	Select conversion sequencer trigger input signal.  0x0: ADC_TRIG0  0x1: ADC_TRIG1  0x2: ADC_TRIG2  0x3: ADC_TRIG3

# 0x00003457 VADC2\_LC\_BTM\_2\_MEAS\_INTERVAL\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo perph rb

Interval Mode Control

# VADC2\_LC\_BTM\_2\_MEAS\_INTERVAL\_CTL

Bits	Name	Description
3:0	MEAS_INTERVAL_TIME1	Select measurement interval time (i.e., If value=0, use 0ms, else use 2^(value+4)/32768).  0x0: MEAS_INTERVAL1_0MS  0x1: MEAS_INTERVAL1_1P0MS  0x2: MEAS_INTERVAL1_2P0MS  0x3: MEAS_INTERVAL1_3P9MS  0x4: MEAS_INTERVAL1_3P9MS  0x5: MEAS_INTERVAL1_15P6MS  0x6: MEAS_INTERVAL1_31P3MS  0x7: MEAS_INTERVAL1_31P3MS  0x7: MEAS_INTERVAL1_62P5MS  0x8: MEAS_INTERVAL1_125MS  0x9: MEAS_INTERVAL1_250MS  0x0: MEAS_INTERVAL1_1500MS  0xA: MEAS_INTERVAL1_1S  0xC: MEAS_INTERVAL1_1S  0xC: MEAS_INTERVAL1_1S  0xC: MEAS_INTERVAL1_1S  0xC: MEAS_INTERVAL1_1AS  0xE: MEAS_INTERVAL1_1AS  0xF: MEAS_INTERVAL1_1AS

# 0x00003458 VADC2\_LC\_BTM\_2\_MEAS\_INTERVAL\_CTL2

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

# VADC2\_LC\_BTM\_2\_MEAS\_INTERVAL\_CTL2

Bits	Name	Description
7:4	MEAS_INTERVAL_TIME2	Small timer: Select measurement interval time in 100ms
		increments.
		0x0: MEAS_INTERVAL2_0MS
		0x1: MEAS_INTERVAL2_100MS
		0x2: MEAS_INTERVAL2_200MS
		0x3: MEAS_INTERVAL2_300MS
		0x4: MEAS_INTERVAL2_400MS
		0x5: MEAS_INTERVAL2_500MS
		0x6: MEAS_INTERVAL2_600MS
		0x7: MEAS_INTERVAL2_700MS
		0x8: MEAS_INTERVAL2_800MS
		0x9: MEAS_INTERVAL2_900MS
		0xA: MEAS_INTERVAL2_1000MS
		0xB: MEAS_INTERVAL2_1100MS
		0xC: MEAS_INTERVAL2_1200MS
		0xD: MEAS_INTERVAL2_1300MS
		0xE: MEAS_INTERVAL2_1400MS
		0xF: MEAS_INTERVAL2_1500MS
3:0	MEAS_INTERVAL_TIME3	Large timer: Select measurement interval time in seconds.
	, 0,	0x0: MEAS_INTERVAL3_0S
	2,10	0x1: MEAS_INTERVAL3_1S
	OS indi	0x2: MEAS_INTERVAL3_2S
	S. On	0x3: MEAS_INTERVAL3_3S
	30 2 2 M	0x4: MEAS_INTERVAL3_4S
	1	0x5: MEAS_INTERVAL3_5S
		0x6: MEAS_INTERVAL3_6S
		0x7: MEAS_INTERVAL3_7S
		0x8: MEAS_INTERVAL3_8S
		0x9: MEAS_INTERVAL3_9S
		0xA: MEAS_INTERVAL3_10S
		0xB: MEAS_INTERVAL3_11S
		0xC: MEAS_INTERVAL3_12S
		0xD: MEAS_INTERVAL3_13S
		0xE: MEAS_INTERVAL3_14S
		0xF: MEAS_INTERVAL3_15S
	L	

# 0x00003459 VADC2\_LC\_BTM\_2\_MEAS\_INTERVAL\_OP\_CTL

**Type:** RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo perph rb

Interval mode select

# VADC2\_LC\_BTM\_2\_MEAS\_INTERVAL\_OP\_CTL

Bits	Name	Description
7	MEAS_INTERVAL_OP	Interval mode select
		0x0: INTERVAL_MODE_DISABLED
		0x1: INTERVAL_MODE_ENABLED
1:0	M0_MEAS_INTERVAL_TIME	Select which interval timer to use
		0x0: M0_USING_TIMER1
		0x1: M0_USING_TIMER2
		0x2: M0_USING_TIMER3

# 0x0000345A VADC2\_LC\_BTM\_2\_FAST\_AVG\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Fast Average Control

# VADC2\_LC\_BTM\_2\_FAST\_AVG\_CTI

Bits	Name	Description
3:0	FAST_AVG_SAMPLES	Select number of samples for use in fast average mode (i.e. 2^(value).  0x0: AVG_1_SAMPLE  0x1: AVG_2_SAMPLES  0x2: AVG_4_SAMPLES  0x3: AVG_8_SAMPLES  0x4: AVG_16_SAMPLES  0x5: AVG_32_SAMPLES  0x6: AVG_64_SAMPLES  0x7: AVG_128_SAMPLES  0x8: AVG_128_SAMPLES
		0x9: AVG_512_SAMPLES

# 0x0000345B VADC2\_LC\_BTM\_2\_FAST\_AVG\_EN

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Fast Average Enable

# VADC2\_LC\_BTM\_2\_FAST\_AVG\_EN

Bits	Name	Description
7	FAST_AVG_EN	Select low latency for multiple conversions 0x0: FAST_AVG_DISABLED 0x1: FAST_AVG_ENABLED

# 0x0000345C VADC2\_LC\_BTM\_2\_M0\_LOW\_THR0

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

M0 Low Threshold Byte 0

#### VADC2\_LC\_BTM\_2\_M0\_LOW\_THR0

Bits	Name	Description
7:0	LOW_THR_7_0	M0 Low byte of low threshold detector

# 

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

M0 Low Threshold Byte 1

#### VADC2\_LC\_BTM\_2\_M0\_LOW\_THR1

Bits	Name	Description
7:0	LOW_THR_15_8	M0 High byte of low threshold detector

# 0x0000345E VADC2\_LC\_BTM\_2\_M0\_HIGH\_THR0

Type: RW

Clock: pbus\_wrclk
Reset State: 0xFF

Reset Name: uvlo\_perph\_rb

M0 High Threshold Byte 0

# VADC2\_LC\_BTM\_2\_M0\_HIGH\_THR0

Bits	Name	Description
7:0	HIGH_THR_7_0	M0 Low byte of high threshold detector

# 0x0000345F VADC2\_LC\_BTM\_2\_M0\_HIGH\_THR1

Type: RW

Clock: pbus\_wrclk
Reset State: 0xFF

**Reset Name:** uvlo\_perph\_rb

M0 High Threshold Byte 1

# VADC2\_LC\_BTM\_2\_M0\_HIGH\_THR1

Bits	Name	Description
7:0	HIGH_THR_15_8	M0 High byte of high threshold detector

#### 

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

M0 ADC Sample Byte 0

# VADC2\_LC\_BTM\_2\_M0\_DATA0

Bits	Name	Description
7:0	DATA_7_0	M0 Low byte of ADC output

#### 

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

M0 ADC Sample Byte 1

#### VADC2\_LC\_BTM\_2\_M0\_DATA1

Bits	Name	Description
7:0	DATA_15_8	M0 High byte of ADC output

# 0x00003468 VADC2\_LC\_BTM\_2\_M1\_ADC\_CH\_SEL\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo perph rb

M1 ADC Channel selection. See device specification for channel descriptions.

#### VADC2\_LC\_BTM\_2\_M1\_ADC\_CH\_SEL\_CTL

Bits	Name	Description
7:0	ADC_CH_SEL	M1 ADC Channel selection. See device specification for channel descriptions.

#### 

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

**Reset Name:** uvlo\_perph\_rb M1 Low Threshold Byte 0

#### VADC2\_LC\_BTM\_2\_M1\_LOW\_THR0

Bits	Name	Description
7:0	LOW_THR_7_0	M1 Low byte of low threshold detector

#### 0x0000346A VADC2\_LC\_BTM\_2\_M1\_LOW\_THR1

**Type:** RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

M1 Low Threshold Byte 1

#### VADC2\_LC\_BTM\_2\_M1\_LOW\_THR1

Bits	Name	Description
7:0	LOW_THR_15_8	M1 High byte of low threshold detector

# 0x0000346B VADC2\_LC\_BTM\_2\_M1\_HIGH\_THR0

Type: RW

Clock: pbus\_wrclk
Reset State: 0xFF

**Reset Name:** uvlo\_perph\_rb M1 High Threshold Byte 0

#### VADC2\_LC\_BTM\_2\_M1\_HIGH\_THR0

Bits	Name	Description
7:0	HIGH_THR_7_0	M1 Low byte of high threshold detector

# 0x0000346C VADC2\_LC\_BTM\_2\_M1\_HIGH\_THR1

Type: RW

Clock: pbus\_wrclk
Reset State: 0xFF

**Reset Name:** uvlo\_perph\_rb

M1 High Threshold Byte 1

#### VADC2\_LC\_BTM\_2\_M1\_HIGH\_THR1

Bits	Name	Description
7:0	HIGH_THR_15_8	M1 High byte of high threshold detector

# 0x0000346D VADC2\_LC\_BTM\_2\_M1\_MEAS\_INTERVAL\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

#### VADC2\_LC\_BTM\_2\_M1\_MEAS\_INTERVAL\_CTL

Bits	Name	Description
1:0	M1_MEAS_INTERVAL_TIME	M1 Select which interval timer to use
		0x0: M1_USING_TIMER1
		0x1: M1_USING_TIMER2
		0x2: M1_USING_TIMER3

# 

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

M1 ADC Sample Byte 0

#### VADC2\_LC\_BTM\_2\_M1\_DATA0

Bits	Name	Description
7:0	DATA_7_0	M1 Low byte of ADC output

# 

Type: R

Clock: pbus\_wrclk Reset State: 0x00

**Reset Name:** N/A

M1 ADC Sample Byte 1

#### VADC2\_LC\_BTM\_2\_M1\_DATA1

Bits	Name	Description
7:0	DATA_15_8	M1 High byte of ADC output

# 16 Vadc\_adj Registers

# 0x00003500 VADC4\_LC\_VBAT\_REVISION1

Type: R

Clock: pbus\_wrclk Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

# VADC4\_LC\_VBAT\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00003501 VADC4\_LC\_VBAT\_REVISION2

Type: R

Clock: pbus\_wrclk
Reset State: 0x04

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### VADC4\_LC\_VBAT\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00003502 VADC4\_LC\_VBAT\_REVISION3

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### VADC4\_LC\_VBAT\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00003503 VADC4\_LC\_VBAT\_REVISION4

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### VADC4\_LC\_VBAT\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

# 0x00003504 VADC4\_LC\_VBAT\_PERPH\_TYPE

Type: R

Clock: pbus\_wrclk Reset State: 0x08

**Reset Name:** N/A

Peripheral Type

PMIC CONSTANT

#### VADC4\_LC\_VBAT\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	ADC

# 0x00003505 VADC4\_LC\_VBAT\_PERPH\_SUBTYPE

Type: R

Clock: pbus\_wrclk Reset State: 0x0C Reset Name: N/A

Peripheral SubType

#### VADC4\_LC\_VBAT\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	VADC1

# 0x00003508 VADC4\_LC\_VBAT\_STATUS1

Type: R

Clock: pbus\_wrclk
Reset State: 0x01

Reset Name: N/A

Status Registers

#### VADC4\_LC\_VBAT\_STATUS1

Bits	Name	Description
4:3	OP_MODE	Selects basic mode of operation
		0x0: NORM_MODE
		0x1: CONV_SEQ_MODE
		0x2: MEAS_INT_MODE
2	MEAS_INTERVAL_EN_STS	Interval Mode
		0x0: INTERVAL_MODE_DISABLED
		0x1: INTERVAL_MODE_ENABLED
1	REQ_STS	REQ_STS mirrors the REQ bit. When REQ is asserted the arbiter stores a descriptor in the conversion request queue. Bit is cleared when ADC conversion is completed.
		0x0: REQ_NOT_IN_PROGRESS
		0x1: REQ_IN_PROGRESS

# VADC4\_LC\_VBAT\_STATUS1 (cont.)

Bits	Name	Description
0	EOC	End of conversion status flag. Bit is de-asserted when arbiter is servicing a conversion request and asserted when conversion is completed. After a conversion is requested, the EOC and REQ_STS bits can be polled to determine ADC conversion status as follows:  REQ_STS EOC Arbiter state  1 1 Waiting for ADC to complete another process's conversion request.  1 0 ADC conversion occurring.  0 1 ADC conversion completed.  0 0 Invalid  0x0: CONV_NOT_COMPLETE  0x1: CONV_COMPLETE

# 0x00003510 VADC4\_LC\_VBAT\_INT\_RT\_STS

Type: R

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Interrupt Real Time Status Bits

# VADC4\_LC\_VBAT\_INT\_RT\_STS

Bits	Name	Description
5	MIN_LOW_THR_INT_RT_S TS	ADC minimum output lower than low threshold. Active high signal. 0x0: MIN_LOW_THR_INT_FALSE 0x1: MIN_LOW_THR_INT_TRUE
4	LOW_THR_INT_RT_STS	ADC output lower than low threshold. Active high signal.  0x0: LOW_THR_INT_FALSE  0x1: LOW_THR_INT_TRUE
3	HIGH_THR_INT_RT_STS	ADC output higher than high threshold. Active high signal. 0x0: HIGH_THR_INT_FALSE 0x1: HIGH_THR_INT_TRUE
2	CONV_SEQ_TIMEOUT_INT _RT_STS	Indicates conversion sequencer conversion was triggered by SBI register field conversion request time out.  0x0: CONV_SEQ_TIMEOUT_FALSE  0x1: CONV_SEQ_TIMEOUT_TRUE
1	FIFO_NOT_EMPTY_INT_RT _STS	Indicates conversion sequencer request written to FIFO when it was not empty.  0x0: FIFO_NOT_EMPTY_INT_FALSE  0x1: FIFO_EMPTY_INT_TRUE

# VADC4\_LC\_VBAT\_INT\_RT\_STS (cont.)

Bits	Name	Description
0	EOC_INT_RT_STS	Secure process end of conversion interrupt. Active high signal two tcxo_clk cycles wide.  0x0: CONV_COMPLETE_INT_FALSE  0x1: CONV_COMPLETE_INT_TRUE

# 0x00003511 VADC4\_LC\_VBAT\_INT\_SET\_TYPE

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

0 =use level trigger interrupts, 1 =use edge trigger interrupts

# VADC4\_LC\_VBAT\_INT\_SET\_TYPE

Bits	Name	Description
5	MIN_LOW_THR_INT_SET_T YPE	Minimum Low threshold interrupt set type 0x0: MIN_LOW_THR_INT_LEVEL 0x1: MIN_LOW_THR_INT_EDGE
4	LOW_THR_INT_SET_TYPE	Low threshold interrupt set type 0x0: LOW_THR_INT_LEVEL 0x1: LOW_THR_INT_EDGE
3	HIGH_THR_INT_SET_TYPE	High threshold interrupt set type 0x0: HIGH_THR_INT_LEVEL 0x1: HIGH_THR_INT_EDGE
2	CONV_SEQ_TIMEOUT_INT _SET_TYPE	Conversion sequencer timeout interrupt set type 0x0: CONV_SEQ_TIMEOUT_LEVEL 0x1: CONV_SEQ_TIMEOUT_EDGE
1	FIFO_NOT_EMPTY_INT_SE T_TYPE	FIFO not empty interrupt set type 0x0: FIFO_NOT_EMPTY_LEVEL 0x1: FIFO_NOT_EMPTY_EDGE
0	EOC_SET_INT_TYPE	EOC interrupt set type 0x0: EOC_LEVEL 0x1: EOC_EDGE

# 0x00003512 VADC4\_LC\_VBAT\_INT\_POLARITY\_HIGH

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### VADC4\_LC\_VBAT\_INT\_POLARITY\_HIGH

Bits	Name	Description
5	MIN_LOW_THR_INT_HIGH	Minimum Low threshold interrupt high polarity enabled 0x0: MIN_LOW_THR_INT_POL_HIGH_DISABLED 0x1: MIN_LOW_THR_INT_POL_HIGH_ENABLED
4	LOW_THR_INT_HIGH	Low threshold interrupt high polarity enabled 0x0: LOW_THR_INT_POL_HIGH_DISABLED 0x1: LOW_THR_INT_POL_HIGH_ENABLED
3	HIGH_THR_INT_HIGH	High threshold interrupt high polarity enabled 0x0: HIGH_THR_INT_POL_HIGH_DISABLED 0x1: HIGH_THR_INT_POL_HIGH_ENABLED
2	CONV_SEQ_TIMEOUT_INT _HIGH	Conversion sequencer interrupt high polarity enabled 0x0: CONV_SEQ_TIMEOUT_INT_POL_HIGH_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_POL_HIGH_ENABLED
1	FIFO_NOT_EMPTY_INT_HI GH	FIFO not empty interrupt high polarity enabled 0x0: FIFO_NOT_EMPTY_INT_POL_HIGH_DISABLED 0x1: FIFO_NOT_EMPTY_INT_POL_HIGH_ENABLED
0	EOC_INT_HIGH	EOC interrupt high polarity enabled  0x0: EOC_INT_POL_HIGH_DISABLED  0x1: EOC_INT_POL_HIGH_ENABLED

# 0x00003513 VADC4\_LC\_VBAT\_INT\_POLARITY\_LOW

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### VADC4\_LC\_VBAT\_INT\_POLARITY\_LOW

Bits	Name	Description
5	MIN_LOW_THR_INT_HIGH	Minimum Low threshold interrupt low polarity enabled 0x0: MIN_LOW_THR_INT_POL_LOW_DISABLED 0x1: MIN_LOW_THR_INT_POL_LOW_ENABLED
4	LOW_THR_INT_HIGH	Low threshold interrupt low polarity enabled 0x0: LOW_THR_INT_POL_LOW_DISABLED 0x1: LOW_THR_INT_POL_LOW_ENABLED
3	HIGH_THR_INT_HIGH	High threshold interrupt low polarity enabled 0x0: HIGH_THR_INT_POL_LOW_DISABLED 0x1: HIGH_THR_INT_POL_LOW_ENABLED
2	CONV_SEQ_TIMEOUT_INT _LOW	Conversion sequencer interrupt low polarity enabled 0x0: CONV_SEQ_TIMEOUT_INT_POL_LOW_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_POL_LOW_ENABLED
1	FIFO_NOT_EMPTY_INT_LO W	FIFO not empty interrupt low polarity enabled 0x0: FIFO_NOT_EMPTY_INT_POL_LOW_DISABLED 0x1: FIFO_NOT_EMPTY_INT_POL_LOW_ENABLED
0	EOC_INT_LOW	EOC interrupt low polarity enabled 0x0: EOC_INT_POL_LOW_DISABLED 0x1: EOC_INT_POL_LOW_ENABLED

# 0x00003514 VADC4\_LC\_VBAT\_INT\_LATCHED\_CLR

Type: W

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Writing a '1' to a bit in this register will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

# VADC4\_LC\_VBAT\_INT\_LATCHED\_CLR

Bits	Name	Description
5	MIN_LOW_THR_INT_LATC HED_CLR	Minimum Low threshold interrupt latched clear
4	LOW_THR_INT_LATCHED_ CLR	Low threshold interrupt latched clear
3	HIGH_THR_INT_LATCHED_ CLR	High threshold interrupt latched clear
2	CONV_SEQ_TIMEOUT_INT _LATCHED_CLR	Conversion sequencer interrupt latched clear

# VADC4\_LC\_VBAT\_INT\_LATCHED\_CLR (cont.)

Bits	Name	Description
1	FIFO_NOT_EMPTY_INT_LA TCHED_CLR	FIFO not empty interrupt latched clear
0	EOC_INT_LATCHED_CLR	EOC interrupt latched clear

# 0x00003515 VADC4\_LC\_VBAT\_INT\_EN\_SET

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Writing '0' to a bit in this register has no effect. Writing a '1' to a bit in this register will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### VADC4\_LC\_VBAT\_INT\_EN\_SET

Bits	Name	Description
5	MIN_LOW_THR_INT_EN_S ET	Minimum Low threshold interrupt enable set 0x0: MIN_LOW_THR_INT_DISABLED 0x1: MIN_LOW_THR_INT_ENBLED
4	LOW_THR_INT_EN_SET	Low threshold interrupt enable set 0x0: LOW_THR_INT_DISABLED 0x1: LOW_THR_INT_ENBLED
3	HIGH_THR_INT_EN_SET	High threshold interrupt enable set 0x0: HIGH_THR_INT_DISABLED 0x1: HIGH_THR_INT_ENBLED
2	CONV_SEQ_TIMEOUT_INT _EN_SET	Conversion sequencer interrupt enable set 0x0: CONV_SEQ_TIMEOUT_INT_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_ENBLED
1	FIFO_NOT_EMPTY_INT_EN _SET	FIFO not empty interrupt enable set  0x0: FIFO_NOT_EMPTY_INT_DISABLED  0x1: FIFO_NOT_EMPTY_INT_ENBLED
0	EOC_INT_EN_SET	EOC interrupt enable set 0x0: EOC_INT_DISABLED 0x1: EOC_INT_ENBLED

#### 0x00003516 VADC4\_LC\_VBAT\_INT\_EN\_CLR

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Writing a '0' to a bit in this register has no effect. Writing a '1' to a bit in this register will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### VADC4 LC VBAT INT EN CLR

Bits	Name	Description
5	MIN_LOW_THR_INT_EN_C LR	Minimum Low threshold interrupt enable clear 0x0: MIN_LOW_THR_INT_DISABLED 0x1: MIN_LOW_THR_INT_ENBLED
4	LOW_THR_INT_EN_CLR	Low threshold interrupt enable clear 0x0: LOW_THR_INT_DISABLED 0x1: LOW_THR_INT_ENBLED
3	HIGH_THR_INT_EN_CLR	High threshold interrupt enable clear 0x0: HIGH_THR_INT_DISABLED 0x1: HIGH_THR_INT_ENBLED
2	CONV_SEQ_TIMEOUT_INT _EN_CLR	Conversion sequencer interrupt enable clear 0x0: CONV_SEQ_TIMEOUT_INT_DISABLED 0x1: CONV_SEQ_TIMEOUT_INT_ENBLED
1	FIFO_NOT_EMPTY_INT_EN _CLR	FIFO not empty interrupt enable clear 0x0: FIFO_NOT_EMPTY_INT_DISABLED 0x1: FIFO_NOT_EMPTY_INT_ENBLED
0	EOC_INT_EN_CLR	EOC interrupt enable clear 0x0: EOC_INT_DISABLED 0x1: EOC_INT_ENBLED

# 0x00003518 VADC4\_LC\_VBAT\_INT\_LATCHED\_STS

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

# VADC4\_LC\_VBAT\_INT\_LATCHED\_STS

Bits	Name	Description
5	MIN_LOW_THR_INT_LATC HED_STS	Minimum Low threshold interrupt latched 0x0: MIN_LOW_THR_INT_LATCHED_FALSE 0x1: MIN_LOW_THR_INT_LATCHED_TRUE
4	LOW_THR_INT_LATCHED_ STS	Low threshold interrupt latched 0x0: LOW_THR_INT_LATCHED_FALSE 0x1: LOW_THR_INT_LATCHED_TRUE
3	HIGH_THR_INT_LATCHED_ STS	High threshold interrupt latched 0x0: HIGH_THR_INT_LATCHED_FALSE 0x1: HIGH_THR_INT_LATCHED_TRUE
2	CONV_SEQ_TIMEOUT_INT _LATCHED_STS	Conversion sequencer interrupt latched 0x0: CONV_SEQ_TIMEOUT_INT_LATCHED_FALSE 0x1: CONV_SEQ_TIMEOUT_INT_LATCHED_TRUE
1	FIFO_NOT_EMPTY_INT_LA TCHED_STS	FIFO not empty interrupt latched  0x0: FIFO_NOT_EMPTY_INT_LATCHED_FALSE  0x1: FIFO_NOT_EMPTY_INT_LATCHED_TRUE
0	EOC_INT_LATCHED_STS	EOC interrupt latched 0x0: EOC_INT_LATCHED_FALSE 0x1: EOC_INT_LATCHED_TRUE

# 0x00003519 VADC4\_LC\_VBAT\_INT\_PENDING\_STS

Type: R

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Debug: Pending is set if interrupt has been sent but not cleared.

# VADC4\_LC\_VBAT\_INT\_PENDING\_STS

Bits	Name	Description
5	MIN_LOW_THR_INT_PENDI NG_STS	Minimum Low threshold interrupt pending 0x0: MIN_LOW_THR_INT_PENDING_FALSE 0x1: MIN_LOW_THR_INT_PENDING_TRUE
4	LOW_THR_INT_PENDING_ STS	Low threshold interrupt pending 0x0: LOW_THR_INT_PENDING_FALSE 0x1: LOW_THR_INT_PENDING_TRUE
3	HIGH_THR_INT_PENDING_ STS	High threshold interrupt pending 0x0: HIGH_THR_INT_PENDING_FALSE 0x1: HIGH_THR_INT_PENDING_TRUE

#### VADC4\_LC\_VBAT\_INT\_PENDING\_STS (cont.)

Bits	Name	Description
2	CONV_SEQ_TIMEOUT_INT _PENDING_STS	Conversion sequencer interrupt pending 0x0: CONV_SEQ_TIMEOUT_INT_PENDING_FALSE 0x1: CONV_SEQ_TIMEOUT_INT_PENDING_TRUE
1	FIFO_NOT_EMPTY_INT_PE NDING_STS	FIFO not empty interrupt pending 0x0: FIFO_NOT_EMPTY_INT_PENDING_FALSE 0x1: FIFO_NOT_EMPTY_INT_PENDING_TRUE
0	EOC_INT_PENDING_STS	EOC interrupt pending 0x0: EOC_INT_PENDING_FALSE 0x1: EOC_INT_PENDING_TRUE

# 0x0000351A VADC4\_LC\_VBAT\_INT\_MID\_SEL

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Selects the MID that will receive the interrupt

# VADC4\_LC\_VBAT\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	Selects the MID that will receive the interrupt

# 0x0000351B VADC4\_LC\_VBAT\_INT\_PRIORITY

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Selects the SPMI interrupt priority

#### VADC4\_LC\_VBAT\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	Selects the SPMI interrupt priority 0x0: SR 0x1: A

# 0x00003540 VADC4\_LC\_VBAT\_MODE\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x03

Reset Name: uvlo\_perph\_rb

Settings Common to Input and Output

# VADC4\_LC\_VBAT\_MODE\_CTL

Bits	Name	Description
4:3	OP_MODE	Selects basic mode of operation:
		00=Normal Mode - Single measurement
		01=Conversion Sequencer - Single measurement using conversion sequencer
		10=Measurement Interval - Single or Continuous measurements at specified delay/interval
		0x0: NORM_MODE
		0x1: CONV_SEQ_MODE
	. ()	0x2: MEAS_INT_MODE
2	VREF_XO_THM_FORCE	When cleared, VDD_REF is connected to XO thermistor in active mode, disconnected in sleep mode
	27,10	When set, force VDD_REF to be connected to the XO thermistor regardless the status of sleepb
	O'S willis	0x0: VREF_XO_THM_FORCE_FALSE
	Old Wen	0x1: VREF_XO_THM_FORCE_TRUE
1	RESERVED	
0	ADC_TRIM_EN	Enable ADC trim
		0x0: ADC_TRIM_DISABLED
		0x1: ADC_TRIM_ENABLED

Go.

# 0x00003546 VADC4\_LC\_VBAT\_EN\_CTL1

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Enables ADC module.

#### VADC4\_LC\_VBAT\_EN\_CTL1

Bits	Name	Description
7	ADC_EN	Enables ADC module.
		0x0: ADC_DISABLED
		0x1: ADC_ENABLED

# 0x00003548 VADC4\_LC\_VBAT\_ADC\_CH\_SEL\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x06

Reset Name: uvlo perph rb

ADC Channel selection. See device specification for channel descriptions.

#### VADC4\_LC\_VBAT\_ADC\_CH\_SEL\_CTL

Bits	Name	Description
7:0	ADC_CH_SEL	ADC Channel selection. See device specification for channel descriptions.

# 0x00003550 VADC4\_LC\_VBAT\_ADC\_DIG\_PARAM

Type: RW

Clock: pbus\_wrclk Reset State: 0x04

Reset Name: uvlo perph rb

**ADC** Digital Parameters

#### VADC4\_LC\_VBAT\_ADC\_DIG\_PARAM

Bits	Name	Description
3:2	DEC_RATIO_SEL	Decimation ratio: 0x0: DECI_512 0x1: DECI_1K 0x2: DECI_2K 0x3: DECI_4K
1:0	CLK_SEL	Select ADC clock rate: 0x0: CLK_SEL_2P4MHZ 0x1: CLK_SEL_4P8MHZ 0x2: CLK_SEL_9P6MHZ 0x3: CLK_SEL_19P2MHZ

# 0x00003551 VADC4\_LC\_VBAT\_HW\_SETTLE\_DELAY

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Settle Delay

# VADC4\_LC\_VBAT\_HW\_SETTLE\_DELAY

Bits	Name	Description
3:0	HW_SETTLE_DELAY	Time between AMUX getting configured and the ADC starting conversion. Delay = 100us*(value) for value<11, and 2ms*(value-10) otherwise  0x0: HW_SETTLE_DELAY_0US  0x1: HW_SETTLE_DELAY_100US  0x2: HW_SETTLE_DELAY_200US  0x3: HW_SETTLE_DELAY_300US  0x4: HW_SETTLE_DELAY_400US  0x5: HW_SETTLE_DELAY_500US  0x6: HW_SETTLE_DELAY_600US  0x7: HW_SETTLE_DELAY_700US  0x8: HW_SETTLE_DELAY_800US  0x9: HW_SETTLE_DELAY_900US  0x0: HW_SETTLE_DELAY_900US  0xA: HW_SETTLE_DELAY_1MS  0xB: HW_SETTLE_DELAY_2MS  0xC: HW_SETTLE_DELAY_4MS  0xD: HW_SETTLE_DELAY_6MS  0xE: HW_SETTLE_DELAY_8MS  0xF: HW_SETTLE_DELAY_10MS

# 0x00003552 VADC4\_LC\_VBAT\_CONV\_REQ

Type: W

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: req\_rb

Conversion Request

#### VADC4\_LC\_VBAT\_CONV\_REQ

Bits	Name	Description
7	REQ	Conversion request strobe. When bit is asserted the arbiter stores a descriptor in the conversion request queue. Bit is cleared when ADC conversion is completed.
		0x0: CONV_REQ_FALSE 0x1: CONV_REQ_TRUE

# 0x00003554 VADC4\_LC\_VBAT\_CONV\_SEQ\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x45

Reset Name: uvlo perph rb

Conversion Sequencer Control

# VADC4\_LC\_VBAT\_CONV\_SEQ\_CTL

Bits	Name	Description
7:4	Name CONV_SEQ_HOLDOFF	Select delay from conversion trigger signal (i.e. adc_conv_seq_trig) transition to ADC enable. Delay = 25us*(value+1). Actual delay will be longer if request is stored in a non empty FIFO and/or conversion needs to wait for LDO OK handshake.  0x0: SEQ_HOLD_25US 0x1: SEQ_HOLD_50US 0x2: SEQ_HOLD_75US 0x3: SEQ_HOLD_100US 0x4: SEQ_HOLD_125US 0x5: SEQ_HOLD_15US 0x6: SEQ_HOLD_15US 0x7: SEQ_HOLD_175US
		0x8: SEQ_HOLD_225US 0x9: SEQ_HOLD_250US
		0xA: SEQ_HOLD_275US
		0xB: SEQ_HOLD_300US
		0xC: SEQ_HOLD_325US
		0xD: SEQ_HOLD_350US
		0xE: SEQ_HOLD_375US
		0xF: SEQ_HOLD_400US

# VADC4\_LC\_VBAT\_CONV\_SEQ\_CTL (cont.)

Bits	Name	Description
3:0	CONV_SEQ_TIMEOUT	Select delay (0 to 15ms) from conversion request to triggering conversion sequencer hold off timer.
		0x0: SEQ_TIMEOUT_0MS
		0x1: SEQ_TIMEOUT_1MS
		0x2: SEQ_TIMEOUT_2MS
		0x3: SEQ_TIMEOUT_3MS
		0x4: SEQ_TIMEOUT_4MS
		0x5: SEQ_TIMEOUT_5MS
		0x6: SEQ_TIMEOUT_6MS
		0x7: SEQ_TIMEOUT_7MS
		0x8: SEQ_TIMEOUT_8MS
		0x9: SEQ_TIMEOUT_9MS
		0xA: SEQ_TIMEOUT_10MS
		0xB: SEQ_TIMEOUT_11MS
		0xC: SEQ_TIMEOUT_12MS
	\ (	0xD: SEQ_TIMEOUT_13MS
		0xE: SEQ_TIMEOUT_14MS
		0xF: SEQ_TIMEOUT_15MS

# 0x00003555 VADC4\_LC\_VBAT\_CONV\_SEQ\_TRIG\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Conversion Sequencer Trigger Select

# VADC4\_LC\_VBAT\_CONV\_SEQ\_TRIG\_CTL

Bits	Name	Description
7	CONV_SEQ_TRIG_COND	Select conversion trigger condition(s) that starts ADC conversion hold off timer.  0x0 - Falling edge  0x1 - Rising edge  0x0: FALLING_EDGE  0x1: RISING_EDGE
1:0	CONV_SEQ_TRIG_SEL	Select conversion sequencer trigger input signal. 0x0: ADC_TRIG0 0x1: ADC_TRIG1 0x2: ADC_TRIG2 0x3: ADC_TRIG3

# 0x00003557 VADC4\_LC\_VBAT\_MEAS\_INTERVAL\_CTL

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Interval Mode Control

# VADC4\_LC\_VBAT\_MEAS\_INTERVAL\_CTL

Bits	Name	Description
3:0	Name  MEAS_INTERVAL_TIME	Description  Select measurement interval time (i.e., If value=0, use 0ms, else use 2^(value+4)/32768).  0x0: MEAS_INTERVAL_0MS  0x1: MEAS_INTERVAL_1P0MS  0x2: MEAS_INTERVAL_2P0MS  0x3: MEAS_INTERVAL_3P9MS  0x4: MEAS_INTERVAL_7P8MS  0x5: MEAS_INTERVAL_15P6MS  0x6: MEAS_INTERVAL_31P3MS  0x7: MEAS_INTERVAL_62P5MS  0x8: MEAS_INTERVAL_125MS  0x9: MEAS_INTERVAL_125MS  0x9: MEAS_INTERVAL_500MS  0xA: MEAS_INTERVAL_500MS  0xA: MEAS_INTERVAL_1S
	2018 3464	0xC: MEAS_INTERVAL_2S 0xD: MEAS_INTERVAL_4S 0xE: MEAS_INTERVAL_8S 0xF: MEAS_INTERVAL_16S

# 0x00003559 VADC4\_LC\_VBAT\_MEAS\_INTERVAL\_OP\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Interval mode select

# VADC4\_LC\_VBAT\_MEAS\_INTERVAL\_OP\_CTL

Bits	Name	Description
7	MEAS_INTERVAL_OP	Interval mode select 0x0: INTERVAL_MODE_DISABLED 0x1: INTERVAL_MODE_ENABLED

# 0x0000355A VADC4\_LC\_VBAT\_FAST\_AVG\_CTL

Type: RW

Clock: pbus\_wrclk
Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Fast Average Control

# VADC4\_LC\_VBAT\_FAST\_AVG\_CTL

Bits	Name	Description
3:0	FAST_AVG_SAMPLES	Select number of samples for use in fast average mode (i.e. 2^(value).
		0x0: AVG_1_SAMPLE
		0x1: AVG_2_SAMPLES
		0x2: AVG_4_SAMPLES
		0x3: AVG_8_SAMPLES
		0x4: AVG_16_SAMPLES
		0x5: AVG_32_SAMPLES
		0x6: AVG_64_SAMPLES
		0x7: AVG_128_SAMPLES
		0x8: AVG_256_SAMPLES
	12	0x9: AVG_512_SAMPLES

# 0x0000355B VADC4\_LC\_VBAT\_FAST\_AVG\_EN

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo\_perph\_rb

Fast Average Enable

# VADC4\_LC\_VBAT\_FAST\_AVG\_EN

Bits	Name	Description
7	FAST_AVG_EN	Select low latency for multiple conversions 0x0: FAST_AVG_DISABLED 0x1: FAST_AVG_ENABLED

#### 0x0000355C VADC4\_LC\_VBAT\_LOW\_THR0

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Low Threshold Byte 0

#### VADC4\_LC\_VBAT\_LOW\_THR0

Bits	Name	Description
7:0	LOW_THR_7_0	Low byte of low threshold detector

# 0x0000355D VADC4\_LC\_VBAT\_LOW\_THR1

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Low Threshold Byte 1

### VADC4\_LC\_VBAT\_LOW\_THR1

Bits	Name	Description
7:0	LOW_THR_15_8	High byte of low threshold detector

#### 0x0000355E VADC4\_LC\_VBAT\_HIGH\_THR0

Type: RW

Clock: pbus\_wrclk
Reset State: 0xFF

Reset Name: uvlo\_perph\_rb

High Threshold Byte 0

### VADC4\_LC\_VBAT\_HIGH\_THR0

Bits	Name	Description
7:0	HIGH_THR_7_0	Low byte of high threshold detector

# 0x0000355F VADC4\_LC\_VBAT\_HIGH\_THR1

Type: RW

Clock: pbus\_wrclk Reset State: 0xFF

Reset Name: uvlo perph rb

High Threshold Byte 1

#### VADC4\_LC\_VBAT\_HIGH\_THR1

Bits	Name	Description
7:0	HIGH_THR_15_8	High byte of high threshold detector

### 0x00003560 VADC4\_LC\_VBAT\_DATA0

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: uvlo perph rb

ADC Sample Byte 0

#### VADC4\_LC\_VBAT\_DATA0

Bits	Name	Description
7:0	DATA_7_0	Low byte of ADC output

# 0x00003561 VADC4\_LC\_VBAT\_DATA1

**Type:** R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: uvlo perph rb

ADC Sample Byte 1

# VADC4\_LC\_VBAT\_DATA1

Bits	Name	Description
7:0	DATA_15_8	High byte of ADC output

#### 0x00003562 VADC4\_LC\_VBAT\_MIN\_LOW\_THR0

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Minimum Low Threshold Byte 0

#### VADC4\_LC\_VBAT\_MIN\_LOW\_THR0

Bits	Name	Description
7:0	MIN_LOW_THR_7_0	Low byte of minimum low threshold detector

# 0x00003563 VADC4\_LC\_VBAT\_MIN\_LOW\_THR1

Type: RW

Clock: pbus\_wrclk Reset State: 0x00

Reset Name: uvlo perph rb

Minimum Low Threshold Byte 1

# VADC4\_LC\_VBAT\_MIN\_LOW\_THR1

Bits	Name	Description
7:0	MIN_LOW_THR_15_8	High byte of minimum low threshold detector

#### 0x00003566 VADC4\_LC\_VBAT\_MIN\_DATA0

**Type:** R

Clock: pbus\_wrclk
Reset State: Undefined

Reset Name: uvlo perph rb

Minimum ADC Sample Byte 0

#### VADC4\_LC\_VBAT\_MIN\_DATA0

Bits	Name	Description
7:0	MIN_DATA_7_0	Low byte of minimum ADC output

# 0x00003567 VADC4\_LC\_VBAT\_MIN\_DATA1

Type: R

Clock: pbus\_wrclk
Reset State: Undefined

**Reset Name:** uvlo\_perph\_rb

Minimum ADC Sample Byte 1

#### VADC4\_LC\_VBAT\_MIN\_DATA1

2018-09-21 oli 02:27 bpf

Bits	Name	Description
7:0	MIN_DATA_15_8	High byte of minimum ADC output

# 17 Bbclk Registers

# 0x00005100 BB\_CLK1\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### BB\_CLK1\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00005101 BB\_CLK1\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

# BB\_CLK1\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

# 0x00005102 BB\_CLK1\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### BB\_CLK1\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00005103 BB\_CLK1\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [31:24]

#### BB\_CLK1\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

# 0x00005104 BB\_CLK1\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x06

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### BB\_CLK1\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	Clock 0x6: CLOCK

# 0x00005105 BB\_CLK1\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

### BB\_CLK1\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	BB clock
	250	0x8: BB_CLK

# 0x00005108 BB\_CLK1\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

**Status Registers** 

#### BB\_CLK1\_STATUS1

Bits	Name	Description
7	CLK_OK	Indicates Hardware or Software enable and includes warm-up delay 0x0: BBCLK_OFF 0x1: BBCLK_ON

# 0x00005143 BB\_CLK1\_EDGE\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x06

Reset Name: PERPH RB

#### BB\_CLK1\_EDGE\_CTL1

Bits	Name	Description
3:0	OUT_EDGE	Edge Rate Control:
		0000 - Invalid
		0001 - Slowest
		1111 - Fastest

# 0x00005144 BB\_CLK1\_DRV\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: PERPH RB

#### BB\_CLK1\_DRV\_CTL1

Bits	Name	Description
1:0	OUT_DRV	Drive Strength Control
	2,72	0x0: ONE_X
	V	0x1: TWO_X
		0x2: THREE_X
		0x3: FOUR_X

#### 0x00005146 BB\_CLK1\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

#### BB\_CLK1\_EN\_CTL

Bits	Name	Description
7	CLK_EN	0x0: BBCLK_NOT_FORCE 0x1: BBCLK_FORCE_EN
1	PC_POLARITY	0x0: POS_PINCONTROL_POLARITY 0x1: NEG_PINCONTROL_POLARITY

#### BB\_CLK1\_EN\_CTL (cont.)

Bits	Name	Description
0	FOLLOW_PC_EN	When set, clock can be enabled from an external signal.  0x0: NOT_FOLLOW_PIN  0x1: FOLLOW_PIN



# 18 Bbclk Registers

# 0x00005200 BB\_CLK2\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### BB\_CLK2\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00005201 BB\_CLK2\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

# BB\_CLK2\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

# 0x00005202 BB\_CLK2\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### BB\_CLK2\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00005203 BB\_CLK2\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [31:24]

#### BB\_CLK2\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

# 0x00005204 BB\_CLK2\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x06

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### BB\_CLK2\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	Clock 0x6: CLOCK

# 0x00005205 BB\_CLK2\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### BB\_CLK2\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	BB clock
	250	0x8: BB_CLK

# 0x00005208 BB\_CLK2\_STATUS1

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

**Status Registers** 

#### BB\_CLK2\_STATUS1

Bits	Name	Description
7	CLK_OK	Indicates Hardware or Software enable and includes warm-up delay 0x0: BBCLK_OFF 0x1: BBCLK_ON

# 0x00005243 BB\_CLK2\_EDGE\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x06

Reset Name: PERPH RB

#### BB\_CLK2\_EDGE\_CTL1

Name	Description
OUT_EDGE	Edge Rate Control:
	0000 - Invalid
	0001 - Slowest
	1111 - Fastest
(	

# 0x00005244 BB\_CLK2\_DRV\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: PERPH RB

#### BB\_CLK2\_DRV\_CTL1

Bits	Name	Description
1:0	OUT_DRV	Drive Strength Control
	2,72	0x0: ONE_X
	V	0x1: TWO_X
		0x2: THREE_X
		0x3: FOUR_X

#### 0x00005246 BB\_CLK2\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### BB\_CLK2\_EN\_CTL

Bits	Name	Description
7	CLK_EN	0x0: BBCLK_NOT_FORCE 0x1: BBCLK_FORCE_EN
1	PC_POLARITY	0x0: POS_PINCONTROL_POLARITY 0x1: NEG_PINCONTROL_POLARITY

#### BB\_CLK2\_EN\_CTL (cont.)

Bits	Name	Description
0	FOLLOW_PC_EN	When set, clock can be enabled from an external signal.  0x0: NOT_FOLLOW_PIN  0x1: FOLLOW_PIN



# 19 Rfclk Registers

# 0x00005400 RF\_CLK1\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### RF\_CLK1\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00005401 RF\_CLK1\_REVISION2

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

# RF\_CLK1\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00005402 RF\_CLK1\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### **RF\_CLK1\_REVISION3**

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

### 0x00005403 RF\_CLK1\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [31:24]

#### RF\_CLK1\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00005404 RF\_CLK1\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x06

Reset Name: N/A

Peripheral Type

PMIC\_CONSTANT

#### RF\_CLK1\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	Clock 0x6: CLOCK

#### 0x00005405 RF\_CLK1\_PERPH\_SUBTYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x09

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### RF\_CLK1\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	RF clock
	25	0x9: RF_CLK

## 0x00005408 RF\_CLK1\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

**Status Registers** 

#### RF\_CLK1\_STATUS1

Bits	Name	Description
7	CLK_OK	0 = Clock is off
		1 =Clock is on. Indicates HW or SW enable
		0x0: RFCLK_OFF
		0x1: RFCLK_ON

#### 0x00005443 RF\_CLK1\_EDGE\_CTL1

Type: RW

Clock: PBUS\_WRCLK **Reset State:** 0x0F

Reset Name: PERPH RB

#### RF\_CLK1\_EDGE\_CTL1

Bits	Name	Description
3:0	OUT_EDGE	Edge Rate Control:
		0000 - Invalid
		0001 - Slowest
		1111 - Fastest

#### RF\_CLK1\_DRV\_CTL1 0x00005444

## RF\_CLK1\_DRV\_CTL1

RF_C	RF_CLK1_DRV_CTL1			
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x02			
Reset N	Name: PERPH_RB	OT COM		
RF_CLK1_DRV_CTL1				
RF_CL	KI_DRV_CILI	XX <sup>C</sup> C.		
RF_CL Bits	Name	Description		
_		Description  Drive Strength Control		
Bits	Name			
Bits	Name	Drive Strength Control		
Bits	Name	Drive Strength Control 0x0: ONE_X		

#### 0x00005446 RF\_CLK1\_EN\_CTL

Type: RW

Clock: PBUS WRCLK **Reset State:** 0x00

Reset Name: PERPH\_RB

#### RF\_CLK1\_EN\_CTL

Bits	Name	Description
7	CLK_EN	0x0: RFCLK_NOT_FORCE 0x1: RFCLK_FORCE_EN
1	PC_POLARITY	0x0: POS_PINCONTROL_POLARITY 0x1: NEG_PINCONTROL_POLARITY

#### RF\_CLK1\_EN\_CTL (cont.)

Bits	Name	Description
0	FOLLOW_PC_EN	When set, clock can be enabled fRm an external signal. 0x0: NOT_FOLLOW_PIN 0x1: FOLLOW_PIN



# 20 Rfclk Registers

### 0x00005500 RF\_CLK2\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### RF\_CLK2\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00005501 RF\_CLK2\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC\_CONSTANT

## RF\_CLK2\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00005502 RF\_CLK2\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### RF\_CLK2\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

### 0x00005503 RF\_CLK2\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [31:24]

#### RF\_CLK2\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00005504 RF\_CLK2\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x06

Reset Name: N/A

Peripheral Type

PMIC\_CONSTANT

#### RF\_CLK2\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	Clock 0x6: CLOCK

#### 0x00005505 RF\_CLK2\_PERPH\_SUBTYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x09

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### RF\_CLK2\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	RF clock
	250	0x9: RF_CLK

#### 0x00005508 RF\_CLK2\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

**Status Registers** 

#### RF\_CLK2\_STATUS1

Bits	Name	Description
7	CLK_OK	0 = Clock is off
		1 =Clock is on. Indicates HW or SW enable
		0x0: RFCLK_OFF
		0x1: RFCLK_ON

### 0x00005543 RF\_CLK2\_EDGE\_CTL1

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x0F

Reset Name: PERPH RB

#### RF\_CLK2\_EDGE\_CTL1

Name	Description
T_EDGE	Edge Rate Control:
	0000 - Invalid
	0001 - Slowest
	1111 - Fastest
T	r_EDGE

## 0x00005544 RF\_CLK2\_DRV\_CTL1

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x02

Reset Name: PERPH RB

#### RF\_CLK2\_DRV\_CTL1

Bits	Name	Description
1:0	OUT_DRV	Drive Strength Control
	2,73	0x0: ONE_X
	V	0x1: TWO_X
		0x2: THREE_X
		0x3: FOUR_X

#### 0x00005546 RF\_CLK2\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

#### RF\_CLK2\_EN\_CTL

Bits	Name	Description
7	CLK_EN	0x0: RFCLK_NOT_FORCE 0x1: RFCLK_FORCE_EN
1	PC_POLARITY	0x0: POS_PINCONTROL_POLARITY 0x1: NEG_PINCONTROL_POLARITY

#### RF\_CLK2\_EN\_CTL (cont.)

Bits	Name	Description
0	FOLLOW_PC_EN	When set, clock can be enabled fRm an external signal. 0x0: NOT_FOLLOW_PIN 0x1: FOLLOW_PIN



## 21 Bbclk Registers

### 0x00005800 LN\_BB\_CLK\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### LN\_BB\_CLK\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00005801 LN\_BB\_CLK\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### LN\_BB\_CLK\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00005802 LN\_BB\_CLK\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### LN\_BB\_CLK\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00005803 LN\_BB\_CLK\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [31:24]

#### LN\_BB\_CLK\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 0x00005804 LN\_BB\_CLK\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x06

Reset Name: N/A

Peripheral Type

PMIC\_CONSTANT

#### LN\_BB\_CLK\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	Clock 0x6: CLOCK

#### 0x00005805 LN\_BB\_CLK\_PERPH\_SUBTYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

## LN\_BB\_CLK\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	BB clock
	27	0x8: BB_CLK

#### 0x00005808 LN\_BB\_CLK\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Status Registers

#### LN\_BB\_CLK\_STATUS1

Bits	Name	Description
7	CLK_OK	Indicates Hardware or Software enable and includes warm-up delay 0x0: BBCLK_OFF 0x1: BBCLK_ON

### 0x00005843 LN\_BB\_CLK\_EDGE\_CTL1

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x06

Reset Name: PERPH RB

#### LN\_BB\_CLK\_EDGE\_CTL1

Bits	Name	Description
3:0	OUT_EDGE	Edge Rate Control:
		0000 - Invalid
		0001 - Slowest
		1111 - Fastest

## 0x00005844 LN\_BB\_CLK\_DRV\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: PERPH RB

#### LN\_BB\_CLK\_DRV\_CTL1

Bits	Name	Description
1:0	OUT_DRV	Drive Strength Control
	2,75	0x0: ONE_X
	V	0x1: TWO_X
		0x2: THREE_X
		0x3: FOUR_X

## 0x00005846 LN\_BB\_CLK\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### LN\_BB\_CLK\_EN\_CTL

Bits	Name	Description
7	CLK_EN	0x0: BBCLK_NOT_FORCE 0x1: BBCLK_FORCE_EN
1	PC_POLARITY	0x0: POS_PINCONTROL_POLARITY 0x1: NEG_PINCONTROL_POLARITY

#### LN\_BB\_CLK\_EN\_CTL (cont.)

Bits	Name	Description
0	FOLLOW_PC_EN	When set, clock can be enabled from an external signal.  0x0: NOT_FOLLOW_PIN  0x1: FOLLOW_PIN



## 22 Slpclk Registers

## 0x00005A00 SLEEP\_CLK1\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x04

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### SLEEP\_CLK1\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00005A01 SLEEP\_CLK1\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

## SLEEP\_CLK1\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00005A04 SLEEP\_CLK1\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x06

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### SLEEP\_CLK1\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	Clock
		0x6: CLOCK

#### 0x00005A05 SLEEP\_CLK1\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x0C

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### SLEEP\_CLK1\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	Sleep Clock 0xC: SLP_CLK

#### 0x00005A46 SLEEP\_CLK1\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK **Reset State:** 0x00

Reset Name: PERPH\_RB

#### SLEEP\_CLK1\_EN\_CTL

Name	Description
SLP_CLK_PAD_EN	Enable Sleep Clock Driver
	0x0: SLP_CLK_BUF_DISABLED
	0x1: SLP_CLK_BUF_ENABLED

## 0x00005A48 SLEEP\_CLK1\_SMPL\_CTL1

#### SLEEP\_CLK1\_SMPL\_CTL1

SLEEP_CLK1_SMPL_CTL1		
Reset S Reset N	RW PBUS_WRCLK State: 0x00 Name: soft_xvdd_rbCLK1_SMPL_CTL1	
Bits	Name	Description
7	SMPL_EN	Enable SMPL timer
		0x0: SMPL_DISABLE
		0x1: SMPL_ENABLED
6	RESERVED	Not used. Used to be TRIGGER_SEL
	27.0	0x1: PON_RB_TRIGGER
	S OS INDIE	0x0: SHUTDOWN2_RB_TRIGGER
1:0	SMPL_DELAY	0x0: HALF_SEC
	20 3h	0x1: ONE_SEC
	1	0x2: ONEANDHALF_SEC
		0x3: TWO_SEC

## 0x00005A5A SLEEP\_CLK1\_CAL\_RC3

Type: RW

Clock: PBUS\_WRCLK **Reset State:** 0x01

Reset Name: soft dvdd rb

#### SLEEP\_CLK1\_CAL\_RC3

	Bits	Name	Description
	0	LFRC_DRIFT_DET_EN_BAT	Ifrc drift detector enabled when battery is present
		Т	0x0: DRIFT_DET_DISABLED
			0x1: DRIFT_DET_ENABLED
L			

## 0x00005A5B SLEEP\_CLK1\_CAL\_RC4

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: soft\_xvdd\_rb

## SLEEP\_CLK1\_CAL\_RC4

Bits	Name	Description
7	CALRC_EN	CalRC enable 0x0: CALRC_DISABLED 0x1: CALRC_ENABLED
6	COINCELL_GOOD	COINCELL_GOOD Indicate whether a qualified coin cell is installed 0x0: WEAK_COINCAP 0x1: STRONG_COINCAP
4	LFRC_DRIFT_DET_EN_COI	Ifrc drift detector enabled when coin cell/cap is present 0x0: DRIFT_DET_DISABLED 0x1: DRIFT_DET_ENABLED
0	CALRC_DTEST_EN	CALRC_DTEST_EN When High {DTEST3,DTEST2,DTEST1} = CalRC FSM state[2:0] 0x0: NORMAL 0x1: CALRC_STATE_ON_DTEST
	2018 24 CM	

# 23 Divclk Registers

### 0x00005B00 DIV\_CLK1\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### **DIV\_CLK1\_REVISION1**

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00005B01 DIV\_CLK1\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### DIV\_CLK1\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00005B04 DIV\_CLK1\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x06

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### DIV\_CLK1\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	Clock
		0x6: CLOCK

#### 0x00005B05 DIV\_CLK1\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x0B

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### DIV\_CLK1\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	DIV_CLK 0xB: DIV_CLK

#### 0x00005B08 DIV\_CLK1\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Status Registers

#### DIV\_CLK1\_STATUS1

Bits	Name	Description
7	DIVCLK_OK	0 = DIVCLK is off
		1 = DIVCLK is on
		0x0: DIVIDER_OFF
		0x1: DIVIDER_ON

## 0x00005B43 DIV\_CLK1\_DIV\_CTL1

#### DIV\_CLK1\_DIV\_CTL1

DIV_CLK1_DIV_CTL1  Type: RW Clock: PBUS_WRCLK Reset State: 0x00  Reset Name: PERPH_RB  DIV_CLK1_DIV_CTL1		
Bits	Name	Description
2:0	DIV_FACTOR	Low power divided clock output to GPIO divide ratio  000 = XO / 1  001 = XO / 1  010 = XO / 2  011 = XO / 4  100 = XO / 8  101 = XO / 16  110 = XO / 32  111 = XO / 64  0x0: XO_DIV1_0  0x1: XO_DIV1  0x2: XO_DIV2  0x3: XO_DIV4  0x4: XO_DIV8  0x5: XO_DIV16  0x6: XO_DIV32  0x7: XO_DIV64

## 0x00005B46 DIV\_CLK1\_EN\_CTL

Type: RW

Clock: PBUS WRCLK **Reset State:** 0x00

Reset Name: PERPH RB

#### DIV\_CLK1\_EN\_CTL

Bits	Name	Description
7	DIVCLK_EN	1 = DIVCLK is on, 0 = DIVCLK is disabled 0x0: DIVCLK_DIS 0x1: DIVCLK_EN
0	FOLLOW_PC_EN	When set, clock can be enabled from an external signal.  0x0: NOT_FOLLOW_PIN  0x1: FOLLOW_PIN
	2018-09-21-01	OZZ POT DOTON

# 24 Divclk Registers

### 0x00005C00 DIV\_CLK2\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### DIV\_CLK2\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00005C01 DIV\_CLK2\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### DIV\_CLK2\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00005C04 DIV\_CLK2\_PERPH\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x06

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### DIV\_CLK2\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	Clock
		0x6: CLOCK

#### 0x00005C05 DIV\_CLK2\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x0B

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### DIV\_CLK2\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	DIV_CLK 0xB: DIV_CLK

#### 0x00005C08 DIV\_CLK2\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Status Registers

#### DIV\_CLK2\_STATUS1

Bits	Name	Description
7	DIVCLK_OK	0 = DIVCLK is off
		1 = DIVCLK is on
		0x0: DIVIDER_OFF
		0x1: DIVIDER_ON

## 0x00005C43 DIV\_CLK2\_DIV\_CTL1

### DIV\_CLK2\_DIV\_CTL1

DIV_CLK2_DIV_CTL1  Type: RW Clock: PBUS_WRCLK Reset State: 0x00  Reset Name: PERPH_RB  DIV_CLK2_DIV_CTL1		
Bits	Name	Description
2:0	DIV_FACTOR	Low power divided clock output to GPIO divide ratio  000 = XO / 1  001 = XO / 1  010 = XO / 2  011 = XO / 4  100 = XO / 8  101 = XO / 16  110 = XO / 32  111 = XO / 64  0x0: XO_DIV1_0  0x1: XO_DIV1  0x2: XO_DIV2  0x3: XO_DIV4  0x4: XO_DIV8  0x5: XO_DIV16  0x6: XO_DIV32  0x7: XO_DIV64

## 0x00005C46 DIV\_CLK2\_EN\_CTL

Type: RW

Clock: PBUS WRCLK **Reset State:** 0x00

Reset Name: PERPH RB

#### DIV\_CLK2\_EN\_CTL

Bits	Name	Description
7	DIVCLK_EN	1 = DIVCLK is on, 0 = DIVCLK is disabled 0x0: DIVCLK_DIS 0x1: DIVCLK_EN
0	FOLLOW_PC_EN	When set, clock can be enabled from an external signal.  0x0: NOT_FOLLOW_PIN  0x1: FOLLOW_PIN
	2018 Swamington	OZZA RUÍ JAN. ZOM

# 25 Divclk Registers

### 0x00005D00 DIV\_CLK3\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### **DIV\_CLK3\_REVISION1**

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00005D01 DIV\_CLK3\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC\_CONSTANT

#### DIV\_CLK3\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00005D04 DIV\_CLK3\_PERPH\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x06

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### DIV\_CLK3\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	Clock
		0x6: CLOCK

#### 0x00005D05 DIV\_CLK3\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x0B

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### DIV\_CLK3\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	DIV_CLK 0xB: DIV_CLK

#### 0x00005D08 DIV\_CLK3\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Status Registers

#### DIV\_CLK3\_STATUS1

Bits	Name	Description
7	DIVCLK_OK	0 = DIVCLK is off
		1 = DIVCLK is on
		0x0: DIVIDER_OFF
		0x1: DIVIDER_ON

## 0x00005D43 DIV\_CLK3\_DIV\_CTL1

#### DIV\_CLK3\_DIV\_CTL1

DIV_CLK3_DIV_CTL1  Type: RW Clock: PBUS_WRCLK Reset State: 0x00  Reset Name: PERPH_RB  DIV_CLK3_DIV_CTL1		
Bits	Name	Description
2:0	DIV_FACTOR	Low power divided clock output to GPIO divide ratio  000 = XO / 1  001 = XO / 1  010 = XO / 2  011 = XO / 4  100 = XO / 8  101 = XO / 16  110 = XO / 32  111 = XO / 64  0x0: XO_DIV1_0  0x1: XO_DIV1  0x2: XO_DIV2  0x3: XO_DIV4  0x4: XO_DIV8  0x5: XO_DIV16  0x6: XO_DIV32  0x7: XO_DIV64

## 0x00005D46 DIV\_CLK3\_EN\_CTL

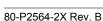
Type: RW

Clock: PBUS WRCLK **Reset State:** 0x00

Reset Name: PERPH RB

#### DIV\_CLK3\_EN\_CTL

Bits	Name	Description
7	DIVCLK_EN	1 = DIVCLK is on, 0 = DIVCLK is disabled 0x0: DIVCLK_DIS 0x1: DIVCLK_EN
0	FOLLOW_PC_EN	When set, clock can be enabled from an external signal. 0x0: NOT_FOLLOW_PIN 0x1: FOLLOW_PIN
	2018-09-21018 2018-09-21018	A. C.



# 26 Rtc\_rw Registers

### 0x00006000 RTC\_RW\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### RTC\_RW\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00006001 RTC\_RW\_REVISION2

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### RTC\_RW\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00006004 RTC\_RW\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x07

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### RTC\_RW\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	RTC
		0x7: RTC

#### 0x00006005 RTC\_RW\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### RTC\_RW\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	RTC RW
		0x1: RTC_RW

#### 0x00006008 RTC\_RW\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Status Registers

#### RTC\_RW\_STATUS1

Bits	Name	Description
7	RTC_OK	0 = RTC is disabled
		1 = RTC is enabled
		0x0: RTC_OFF
		0x1: RTC_ON

#### 0x00006046 RTC\_RW\_EN\_CTL1

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: soft xVdd rb

#### RTC\_RW\_EN\_CTL1

Bits	Name		Description	
7	RTC_EN	7	RTC_EN - enables the real-time clock	
			0x1: RTC_COUNTER_EN	
		20,	0x0: RTC_COUNTER_DIS	

#### 0x00006048 RTC RW RDATA0

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: xVdd rb

#### RTC\_RW\_RDATA0

Bits	Name	Description
7:0	RTC_RDATA0	RTC 32-bit counter [7:0] value

#### 0x00006049 RTC\_RW\_RDATA1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** xVdd\_rb

#### RTC\_RW\_RDATA1

Bits	Name	Description
7:0	RTC_RDATA1	RTC 32-bit counter [15:8] value

#### 0x0000604A RTC\_RW\_RDATA2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: xVdd\_rb

### RTC\_RW\_RDATA2

Bits	Name	Description
7:0	RTC_RDATA2	RTC 32-bit counter [23:16] value

## 0x0000604B RTC\_RW\_RDATA3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: xVdd\_rb

## RTC\_RW\_RDATA3

Bit	Name	Description
7:0	RTC_RDATA3	RTC 32-bit counter [31:24] value

# 27 Rtc\_alarm Registers

## 0x00006100 RTC\_ALARM\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### RTC\_ALARM\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00006101 RTC\_ALARM\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### RTC\_ALARM\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00006104 RTC\_ALARM\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x07

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### RTC\_ALARM\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	RTC
		0x7: RTC

#### 0x00006105 RTC\_ALARM\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x03

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### RTC\_ALARM\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	RTC_ALARM 0x3: RTC_ALARM

#### 0x00006108 RTC\_ALARM\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Status Registers

#### RTC\_ALARM\_STATUS1

Bits	Name	Description
7	RTC_ALARM_OK	0 = ALARM is not enabled
		1 = ALARM is enabled
		0x0: RTC_ALARM_DIS
		0x1: RTC_ALARM_EN

#### 0x00006110 RTC\_ALARM\_INT\_RT\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Interrupt Real Time Status Bits

## RTC\_ALARM\_INT\_RT\_STS

Bits	Name	Description
1	RTC_ALARM	0x0: RTC_ALARM_NOT_EXPIRED
	27.0	0x1: RTC_ALARM_EXPIRED

## 0x00006111 RTC\_ALARM\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### RTC\_ALARM\_INT\_SET\_TYPE

Bits	Name	Description
1	RTC_ALARM	0x0: LEVEL
		0x1: EDGE

#### 0x00006112 RTC\_ALARM\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### RTC\_ALARM\_INT\_POLARITY\_HIGH

Bits	Name	Description
1	RTC_ALARM	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

#### 0x00006113 RTC\_ALARM\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### RTC ALARM INT POLARITY LOW

Bits	Name	Description
1	RTC_ALARM	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

#### 0x00006114 RTC\_ALARM\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK

Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### RTC\_ALARM\_INT\_LATCHED\_CLR

Bits	Name	Description
1	RTC_ALARM	

#### 0x00006115 RTC\_ALARM\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_SET\_MASK

#### RTC\_ALARM\_INT\_EN\_SET

Bits	Name	Description
1	RTC_ALARM	0x0: INT_DISABLED
		0x1: INT_ENABLED

#### 0x00006116 RTC\_ALARM\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC CLR MASK=INT EN SET

## RTC\_ALARM\_INT\_EN\_CLR

Bits	Name	Description
1	RTC_ALARM	2.27

## 0x00006118 RTC\_ALARM\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### RTC\_ALARM\_INT\_LATCHED\_STS

Bits	Name	Description
1	RTC_ALARM	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

#### 0x00006119 RTC\_ALARM\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### RTC\_ALARM\_INT\_PENDING\_STS

Bits	Name	Description
1	RTC_ALARM	0x0: NO_INT_PENDING 0x1: INTERRUPT_PENDING

#### 0x0000611A RTC\_ALARM\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

#### RTC\_ALARM\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0
		0x1: MID1
		0x2: MID2
	27.0	0x3: MID3

## 0x0000611B RTC\_ALARM\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

#### RTC\_ALARM\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR
		0x1: A

#### 0x00006140 RTC\_ALARM\_ALARM\_DATA0

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: soft xVdd rb

#### RTC ALARM ALARM DATA0

Bits	Name	Description
7:0	RTC_ALARM_DATA0	RTC_ALARM_DATA0 - Real time alarm value [7:0].

## 0x00006141 RTC\_ALARM\_ALARM\_DATA1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** soft\_xVdd\_rb

#### RTC\_ALARM\_ALARM\_DATA1

Bits	Name	Description
7:0	RTC_ALARM_DATA1	RTC_ALARM_DATA1 - Real time alarm value [15:8].

#### 0x00006142 RTC\_ALARM\_ALARM\_DATA2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: soft xVdd rb

#### RTC\_ALARM\_ALARM\_DATA2

Bits	Name	Description
7:0	RTC_ALARM_DATA2	RTC_ALARM_DATA2 - Real time alarm value [23:16].

#### 0x00006143 RTC\_ALARM\_ALARM\_DATA3

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** soft\_xVdd\_rb

#### RTC\_ALARM\_ALARM\_DATA3

Bits	Name	Description
7:0	RTC_ALARM_DATA3	RTC_ALARM_DATA3 - Real time alarm value [31:24].

#### 0x00006146 RTC\_ALARM\_EN\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** soft\_xVdd\_rb

#### RTC\_ALARM\_EN\_CTL1

Bits	Name	Description
7	ALARM_EN	ALARM_EN - enables the real-time clock alarm
		0x0: RTC_ALARM_DIS
		0x1: RTC_ALARM_EN
0	ABORT_EN	ABORT_EN - Enable the abort on PERPH_RB feature. If the PMIC fails to power up within 4 seconds, the alarm will be masked to stop repeated power cycling.
	70	0x0: RTC_STARTUP_DOESNT_ABORT
	97,018	0x1: RTC_STARTUP_ABORT_EN

## 0x00006148 RTC\_ALARM\_ALARM\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: soft\_xVdd\_rb

#### RTC\_ALARM\_ALARM\_CLR

Bits	Name	Description
0	ALARM_CLR	RTC alarm cleared by writing 1

# 28 Mpp\_ult Registers

### 0x0000A000 MPP1\_REVISION1

#### MPP1 REVISION1

Type: Clock:	MPP1_REVISION1  Type: R Clock: PBUS_WRCLK Reset State: 0x01		
Reset I	Name: N/A		
HW Ve	ersion Register [7:0]		
PMIC_	PMIC_CONSTANT		
_	REVISION1	in com	
Bits	Name	Description	
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.	

## 0x0000A001 MPP1\_REVISION2

Type: R

Clock: PBUS WRCLK **Reset State:** 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### MPP1\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x0000A002 MPP1\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### MPP1\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x0000A003 MPP1 REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### MPP1\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x0000A004 MPP1\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x11

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### MPP1\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0x11: MPP

#### 0x0000A005 MPP1\_PERPH\_SUBTYPE

Type: R

#### MPP1\_PERPH\_SUBTYPE

	PBUS_WRCLK State: 0x06	
Reset Name: N/A		
Peripheral SubType		
MPP1_	PERPH_SUBTYPE	·O,
Bits	Name	Description
7:0	SUBTYPE	0x3: MPP_4CH_SINK
	. ( )	0x4: ULT_MPP_4CH_SINK
		0x5: MPP_4CH_AOUT
		0x6: ULT_MPP_4CH_AOUT
	25.0	0x7: MPP_4CH_AOUT_SINK
	29 201	0xB: MPP_8CH_SINK
		OVD, MDD OCH ACHT
	C' CULI	0xD: MPP_8CH_AOUT 0xF: MPP_8CH_AOUT_SINK

#### 800A000x0 MPP1\_STATUS1

**Type:** R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: N/A

Status Registers

#### MPP1\_STATUS1

Bits	Name	Description
7	MPP_OK	0 = MPP is disabled
		1 = MPP is enabled
		0x0: MPP_DISABLED
		0x1: MPP_ENABLED

#### MPP1\_STATUS1 (cont.)

Bits	Name	Description
0	MPP_VAL	Value read by the input buffer, if enabled 0x0: MPP_INPUT_LOW 0x1: MPP_INPUT_HIGH

## 0x0000A010 MPP1\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Interrupt Real Time Status Bits

#### MPP1\_INT\_RT\_STS

Bits	Name	Description
0	MPP_IN_STS	0x0: INT_RT_STATUS_LOW
		0x1: INT_RT_STATUS_HIGH

#### 0x0000A011 MPP1 INT SET TYPE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### MPP1\_INT\_SET\_TYPE

Bits	Name	Description
0	MPP_IN_TYPE	0x0: LEVEL
		0x1: EDGE

#### 0x0000A012 MPP1\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### MPP1\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	MPP_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

#### 0x0000A013 MPP1\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### MPP1\_INT\_POLARITY\_LOW

Bits	Name	Description
0	MPP_IN_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

## 0x0000A014 MPP1\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### MPP1\_INT\_LATCHED\_CLR

Bits	Name	Description
0	MPP_IN_LATCHED_CLR	

#### 0x0000A015 MPP1\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### MPP1\_INT\_EN\_SET

Bit	Name	Description
0	MPP_IN_EN_SET	0x0: INT_DISABLED
		0x1: INT_ENABLED

#### 0x0000A016 MPP1\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### MPP1 INT EN CLR

Bits	Name	Description
0	MPP_IN_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

#### 0x0000A018 MPP1\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### MPP1\_INT\_LATCHED\_STS

Bits	Name	Description
0	MPP_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

#### 0x0000A019 MPP1\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### MPP1\_INT\_PENDING\_STS

Bits	Name	Description
0	MPP_IN_PENDING_STS	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING

#### 0x0000A01A MPP1\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### MPP1\_INT\_MID\_SEL

Name	Description
NT_MID_SEL	0x0: MID0
	0x1: MID1
	0x2: MID2
	0x3: MID3
V	· · V

## 0x0000A01B MPP1\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### MPP1\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR
		0x1: A

## 0x0000A040 MPP1\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

#### MPP1\_MODE\_CTL

Bits	Name	Description
6:4	MODE	MPP Type:
		0x0: DIGITAL_INPUT
		0x1: DIGITAL_OUTPUT
		0x2: DIGITAL_IN_AND_OUT
		0x3: RESERVED3
		0x4: ANALOG_INPUT
		0x5: ANALOG_OUTPUT
		0x6: CURRENT_SINK
	. ( )	0x7: RESERVED7
	2018-09-21-01-02-01-01-01-01-01-01-01-01-01-01-01-01-01-	

## MPP1\_MODE\_CTL (cont.)

Bits	Name	Description
3:0	EN_AND_SOURCE_SEL	When configured as a digital output Source select:
		0000 = 0
		0001 = 1
		0010 = paired MPP
		0011 = inverted paired MPP 0100 = Reserved
		0101 = Reserved
		0110 = Reserved
		0111 = Reserved
		1000 = DTEST1
		1001 = inverted DTEST1
		1010 = DTEST2
		1011 = inverted DTEST2
		1100 = DTEST3
		1101 = inverted DTEST3
		1110 = DTEST4
		1111 = inverted DTEST4
		1 P
		Enable control when configured as AOUT, or Current Sink. MPP is
		enable whenever the selected condition is true.
	, 0,	0000 = 0 (mpp is always disabled) 0001 = 1 (mpp is always Enabled)
	2 2	0010 = paired MPP
	09, 1110	0011 = inverted paired MPP
	J. 8. 16.1.	0100 = Reserved
	College Williams	0101 = Reserved
	1	0110 = Reserved
		0111 = Reserved
		1000 = DTEST1
		1001 = inverted DTEST1
		1010 = DTEST2
		1011 = inverted DTEST2
		1100 = DTEST3
		1101 = inverted DTEST3 1110 = DTEST4
		1111 = inverted DTEST4 0x0: LOW
		0x1: HIGH
		0x2: PAIRED MPP
		0x3: NOT_PAIRED_MPP
		0x4: RESERVED4
		0x5: RESERVED5
		0x6: RESERVED6
		0x7: RESERVED7
		0x8: DTEST1
		0x9: NOT_DTEST1

#### MPP1\_MODE\_CTL (cont.)

Bits	Name	Description
		0xA: DTEST2
		0xB: NOT_DTEST2
		0xC: DTEST3
		0xD: NOT_DTEST3
		0xE: DTEST4
		0xF: NOT_DTEST4

#### 0x0000A041 MPP1\_DIG\_VIN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### MPP1\_DIG\_VIN\_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source: (refer to the device specification for the definition of VINx) 0x0: VIN0 0x1: VIN1
	O 18:08 mills	0x2: VIN2 0x3: VIN3

#### 0x0000A043 MPP1\_DIG\_IN\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

**Enable DTEST buffers** 

#### MPP1\_DIG\_IN\_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4  0x0: DTEST_DISABLED  0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3  0x0: DTEST_DISABLED  0x1: DTEST_ENABLED

#### MPP1\_DIG\_IN\_CTL (cont.)

Bits	Name	Description
1	DTEST2	Route to DTEST2 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED

## 0x0000A046 MPP1\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### MPP1\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	MPP Master enable
		0 = puts MPP_PAD at high Z and disables the block
	27	1 = MPP is enabled
	29 00	0x0: MPP_DISABLED
	18.00 mills	0x1: MPP_ENABLED

#### 0x0000A048 MPP1\_ANA\_OUT\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### MPP1\_ANA\_OUT\_CTL

Bits	Name	Description
2:0	RESERVED	

#### 0x0000A04A MPP1\_ANA\_IN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### MPP1\_ANA\_IN\_CTL

Bits	Name	Description
2:0	ROUTE_SEL	AMUX Channel Control
		0: Route to hkadc5
		1: Route to hkadc6
		2: Route to hkadc7
		3: Route to hkadc8
		4: Reserved
		5: Reserved
		6: Reserved
		7: Reserved
		0x0: HKADC5
		0x1: HKADC6
		0x2: HKADC7
		0x3: HKADC8
		0x4: Reserved
	\ (	0x5: Reserved
		0x6: Reserved
		0x7: Reserved

## 0x0000A04C MPP1\_SINK\_CTL

Type: RW

Clock: PBUS\_WRCLK

Reset State: 0x00

Reset Name: PERPH\_RB

#### MPP1\_SINK\_CTL

Bits	Name	Description
2:0	CURRENT_SEL	Current Sink Output Control
		0x0: CURRENT_5MA
		0x1: CURRENT_10MA
		0x2: CURRENT_15MA
		0x3: CURRENT_20MA
		0x4: CURRENT_25MA
		0x5: CURRENT_30MA
		0x6: CURRENT_35MA
		0x7: CURRENT_40MA

# 29 Mpp\_ult Registers

### 0x0000A100 MPP2\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### MPP2\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x0000A101 MPP2\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### MPP2\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x0000A102 MPP2\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### MPP2\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x0000A103 MPP2 REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### MPP2\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x0000A104 MPP2\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x11

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### MPP2\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0x11: MPP

#### 0x0000A105 MPP2\_PERPH\_SUBTYPE

Type: R

#### MPP2\_PERPH\_SUBTYPE

	PBUS_WRCLK State: 0x04	
Reset Name: N/A		
Periphe	eral SubType	
MDD2	DEDDU GUDTVDE	
	PERPH_SUBTYPE	
Bits	Name	Description
7:0	SUBTYPE	0x3: MPP_4CH_SINK
	. ( )	0x4: ULT_MPP_4CH_SINK
		0x5: MPP 4CH AOUT
1		0X5. MFF_4CH_AOUT
	65	0x6: ULT_MPP_4CH_AOUT
	210	V 20 = =
	29-21 de	0x6: ULT_MPP_4CH_AOUT
	G 1.09-21.03	0x6: ULT_MPP_4CH_AOUT 0x7: MPP_4CH_AOUT_SINK

#### 0x0000A108 MPP2\_STATUS1

**Type:** R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: N/A

Status Registers

#### MPP2\_STATUS1

Bits	Name	Description
7	MPP_OK	0 = MPP is disabled
		1 = MPP is enabled
		0x0: MPP_DISABLED
		0x1: MPP_ENABLED

#### MPP2\_STATUS1 (cont.)

Bits	Name	Description
0	MPP_VAL	Value read by the input buffer, if enabled 0x0: MPP_INPUT_LOW 0x1: MPP_INPUT_HIGH

#### 0x0000A110 MPP2\_INT\_RT\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Interrupt Real Time Status Bits

#### MPP2\_INT\_RT\_STS

Bits	Name	Description
0	MPP_IN_STS	0x0: INT_RT_STATUS_LOW
		0x1: INT_RT_STATUS_HIGH

#### 0x0000A111 MPP2 INT SET TYPE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### MPP2\_INT\_SET\_TYPE

Bits	Name	Description
0	MPP_IN_TYPE	0x0: LEVEL
		0x1: EDGE

#### 0x0000A112 MPP2\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### MPP2\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	MPP_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

#### 0x0000A113 MPP2\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### MPP2\_INT\_POLARITY\_LOW

Bits	Name	Description
0	MPP_IN_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

## 0x0000A114 MPP2\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### MPP2\_INT\_LATCHED\_CLR

Bits	Name	Description
0	MPP_IN_LATCHED_CLR	

#### 0x0000A115 MPP2\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### MPP2\_INT\_EN\_SET

Bits	Name	Description
0	MPP_IN_EN_SET	0x0: INT_DISABLED
		0x1: INT_ENABLED

#### 0x0000A116 MPP2\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### MPP2 INT EN CLR

Bits	Name	Description
0	MPP_IN_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

#### 0x0000A118 MPP2\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### MPP2\_INT\_LATCHED\_STS

Bits	Name	Description
0	MPP_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

#### 0x0000A119 MPP2\_INT\_PENDING\_STS

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### MPP2\_INT\_PENDING\_STS

Bits	Name	Description
0	MPP_IN_PENDING_STS	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING

#### 0x0000A11A MPP2\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### MPP2\_INT\_MID\_SEL

Name	Description
NT_MID_SEL	0x0: MID0
	0x1: MID1
	0x2: MID2
	0x3: MID3
V	· · V

## 0x0000A11B MPP2\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### MPP2\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR
		0x1: A

## 0x0000A140 MPP2\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

#### MPP2\_MODE\_CTL

Bits	Name	Description
6:4	MODE	MPP Type:
		0x0: DIGITAL_INPUT
		0x1: DIGITAL_OUTPUT
		0x2: DIGITAL_IN_AND_OUT
		0x3: RESERVED3
		0x4: ANALOG_INPUT
		0x5: ANALOG_OUTPUT
		0x6: CURRENT_SINK
	. ( )	0x7: RESERVED7
2012 Swamingtern.com		

## MPP2\_MODE\_CTL (cont.)

Bits	Name	Description
3:0	EN_AND_SOURCE_SEL	When configured as a digital output Source select:
		0000 = 0
		0001 = 1
		0010 = paired MPP
		0011 = inverted paired MPP 0100 = Reserved
		0101 = Reserved
		0110 = Reserved
		0111 = Reserved
		1000 = DTEST1
		1001 = inverted DTEST1
		1010 = DTEST2
		1011 = inverted DTEST2
		1100 = DTEST3
		1101 = inverted DTEST3
		1110 = DTEST4
		1111 = inverted DTEST4
		1 P
		Enable control when configured as AOUT, or Current Sink. MPP is
		enable whenever the selected condition is true.
	, 0,	0000 = 0 (mpp is always disabled) 0001 = 1 (mpp is always Enabled)
	2 2	0010 = paired MPP
	09, 1110	0011 = inverted paired MPP
	J. 8. 16.1.	0100 = Reserved
	Cole of thirth	0101 = Reserved
	1	0110 = Reserved
		0111 = Reserved
		1000 = DTEST1
		1001 = inverted DTEST1
		1010 = DTEST2
		1011 = inverted DTEST2
		1100 = DTEST3
		1101 = inverted DTEST3 1110 = DTEST4
		1111 = inverted DTEST4 0x0: LOW
		0x1: HIGH
		0x2: PAIRED MPP
		0x3: NOT_PAIRED_MPP
		0x4: RESERVED4
		0x5: RESERVED5
		0x6: RESERVED6
		0x7: RESERVED7
		0x8: DTEST1
		0x9: NOT_DTEST1

#### MPP2\_MODE\_CTL (cont.)

Bits	Name	Description
		0xA: DTEST2
		0xB: NOT_DTEST2
		0xC: DTEST3
		0xD: NOT_DTEST3
		0xE: DTEST4
		0xF: NOT_DTEST4

#### 0x0000A141 MPP2\_DIG\_VIN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

## MPP2\_DIG\_VIN\_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source:
		(refer to the device specification for the definition of VINx)
	, , , ,	0x0: VIN0
	2 2	0x1: VIN1
	, OS , if OS	0x2: VIN2
	OJS NEW	0x3: VIN3

#### 0x0000A143 MPP2\_DIG\_IN\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

**Enable DTEST buffers** 

#### MPP2\_DIG\_IN\_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4  0x0: DTEST_DISABLED  0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED

#### MPP2\_DIG\_IN\_CTL (cont.)

Bits	Name	Description
1	DTEST2	Route to DTEST2 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED

## 0x0000A146 MPP2\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### MPP2\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	MPP Master enable
		0 = puts MPP_PAD at high Z and disables the block
	27	1 = MPP is enabled
	20 00	0x0: MPP_DISABLED
	18. Onlin	0x1: MPP_ENABLED

#### 0x0000A148 MPP2\_ANA\_OUT\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### MPP2\_ANA\_OUT\_CTL

Bits	Name	Description
2:0	RESERVED	

## 0x0000A14A MPP2\_ANA\_IN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

#### MPP2\_ANA\_IN\_CTL

Bits	Name	Description
2:0	ROUTE_SEL	AMUX Channel Control
		0: Route to hkadc5
		1: Route to hkadc6
		2: Route to hkadc7
		3: Route to hkadc8
		4: Reserved
		5: Reserved
		6: Reserved
		7: Reserved
		0x0: HKADC5
		0x1: HKADC6
		0x2: HKADC7
		0x3: HKADC8
		0x4: Reserved
	\ (	0x5: Reserved
		0x6: Reserved
		0x7: Reserved

## 0x0000A14C MPP2\_SINK\_CTL

Type: RW

Clock: PBUS\_WRCLK

Reset State: 0x00

Reset Name: PERPH\_RB

#### MPP2\_SINK\_CTL

Bits	Name	Description
2:0	CURRENT_SEL	Current Sink Output Control
		0x0: CURRENT_5MA
		0x1: CURRENT_10MA
		0x2: CURRENT_15MA
		0x3: CURRENT_20MA
		0x4: CURRENT_25MA
		0x5: CURRENT_30MA
		0x6: CURRENT_35MA
		0x7: CURRENT_40MA

# 30 Mpp\_ult Registers

### 0x0000A200 MPP3\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### MPP3\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x0000A201 MPP3\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### MPP3\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x0000A202 MPP3\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### MPP3\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x0000A203 MPP3 REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### MPP3\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x0000A204 MPP3\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x11

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### MPP3\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0x11: MPP

## 0x0000A205 MPP3\_PERPH\_SUBTYPE

Type: R

#### MPP3\_PERPH\_SUBTYPE

	PBUS_WRCLK State: 0x06	
Reset Name: N/A		
Periphe	eral SubType	
MPP3_	PERPH_SUBTYPE	·O,
Bits	Name	Description
7:0	SUBTYPE	0x3: MPP_4CH_SINK
	. ( )	0x4: ULT_MPP_4CH_SINK
		0x5: MPP_4CH_AOUT
		0x6: ULT_MPP_4CH_AOUT
	27	0x7: MPP_4CH_AOUT_SINK
	39 alie	0xB: MPP_8CH_SINK
	C. C. Mills	0xD: MPP_8CH_AOUT
	V V (O)	0xF: MPP 8CH AOUT SINK

#### 0x0000A208 MPP3\_STATUS1

**Type:** R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: N/A

Status Registers

#### MPP3\_STATUS1

Bits	Name	Description
7	MPP_OK	0 = MPP is disabled
		1 = MPP is enabled
		0x0: MPP_DISABLED
		0x1: MPP_ENABLED

#### MPP3\_STATUS1 (cont.)

Bits	Name	Description
0	MPP_VAL	Value read by the input buffer, if enabled 0x0: MPP_INPUT_LOW 0x1: MPP_INPUT_HIGH

## 0x0000A210 MPP3\_INT\_RT\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Interrupt Real Time Status Bits

#### MPP3\_INT\_RT\_STS

Bits	Name	Description
0	MPP_IN_STS	0x0: INT_RT_STATUS_LOW
		0x1: INT_RT_STATUS_HIGH

## 0x0000A211 MPP3\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### MPP3\_INT\_SET\_TYPE

Bits	Name	Description
0	MPP_IN_TYPE	0x0: LEVEL
		0x1: EDGE

#### 0x0000A212 MPP3\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### MPP3\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	MPP_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

#### 0x0000A213 MPP3\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### MPP3\_INT\_POLARITY\_LOW

Bits	Name	Description
0	MPP_IN_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

## 0x0000A214 MPP3\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### MPP3\_INT\_LATCHED\_CLR

Bits	Name	Description
0	MPP_IN_LATCHED_CLR	

#### 0x0000A215 MPP3\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### MPP3\_INT\_EN\_SET

Bits	Name	Description
0	MPP_IN_EN_SET	0x0: INT_DISABLED
		0x1: INT_ENABLED

#### 0x0000A216 MPP3\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### MPP3 INT EN CLR

Bits	Name	Description
0	MPP_IN_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

#### 0x0000A218 MPP3\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### MPP3\_INT\_LATCHED\_STS

Bits	Name	Description
0	MPP_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

#### 0x0000A219 MPP3\_INT\_PENDING\_STS

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### MPP3\_INT\_PENDING\_STS

Bits	Name	Description
0	MPP_IN_PENDING_STS	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING

#### 0x0000A21A MPP3\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### MPP3\_INT\_MID\_SEL

Name	Description
NT_MID_SEL	0x0: MID0
	0x1: MID1
	0x2: MID2
	0x3: MID3
V	· · V

### 0x0000A21B MPP3\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### MPP3\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR
		0x1: A

## 0x0000A240 MPP3\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

#### MPP3\_MODE\_CTL

Bits	Name	Description	
6:4	MODE	MPP Type:	
		0x0: DIGITAL_INPUT	
		0x1: DIGITAL_OUTPUT	
		0x2: DIGITAL_IN_AND_OUT	
		0x3: RESERVED3	
		0x4: ANALOG_INPUT	
		0x5: ANALOG_OUTPUT	
		0x6: CURRENT_SINK	
	. ( )	0x7: RESERVED7	
	2018-09-21 of October 2018 Shieming Echicom		

## MPP3\_MODE\_CTL (cont.)

Bits	Name	Description
3:0	EN_AND_SOURCE_SEL	When configured as a digital output Source select:
		0000 = 0
		0001 = 1
		0010 = paired MPP
		0011 = inverted paired MPP 0100 = Reserved
		0101 = Reserved
		0110 = Reserved
		0111 = Reserved
		1000 = DTEST1
		1001 = inverted DTEST1
		1010 = DTEST2
		1011 = inverted DTEST2
		1100 = DTEST3
		1101 = inverted DTEST3
		1110 = DTEST4
		1111 = inverted DTEST4
		1 P
		Enable control when configured as AOUT, or Current Sink. MPP is
		enable whenever the selected condition is true.
	, 0,	0000 = 0 (mpp is always disabled) 0001 = 1 (mpp is always Enabled)
	2 2	0010 = paired MPP
	09, 1119	0011 = inverted paired MPP
	J. 8. 16.1.	0100 = Reserved
	Cole of thirth	0101 = Reserved
	1	0110 = Reserved
		0111 = Reserved
		1000 = DTEST1
		1001 = inverted DTEST1
		1010 = DTEST2
		1011 = inverted DTEST2
		1100 = DTEST3
		1101 = inverted DTEST3 1110 = DTEST4
		1111 = inverted DTEST4 0x0: LOW
		0x1: HIGH
		0x2: PAIRED MPP
		0x3: NOT_PAIRED_MPP
		0x4: RESERVED4
		0x5: RESERVED5
		0x6: RESERVED6
		0x7: RESERVED7
		0x8: DTEST1
		0x9: NOT_DTEST1

#### MPP3\_MODE\_CTL (cont.)

Bits	Name	Description
		0xA: DTEST2
		0xB: NOT_DTEST2
		0xC: DTEST3
		0xD: NOT_DTEST3
		0xE: DTEST4
		0xF: NOT_DTEST4

### 0x0000A241 MPP3\_DIG\_VIN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

## MPP3\_DIG\_VIN\_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source: (refer to the device specification for the definition of VINx) 0x0: VIN0
	C 18.09. Ningte	0x1: VIN1 0x2: VIN2 0x3: VIN3

#### 0x0000A243 MPP3\_DIG\_IN\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

**Enable DTEST buffers** 

#### MPP3\_DIG\_IN\_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4  0x0: DTEST_DISABLED  0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED

#### MPP3\_DIG\_IN\_CTL (cont.)

Bits	Name	Description
1	DTEST2	Route to DTEST2 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED

#### 0x0000A246 MPP3\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### MPP3\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	MPP Master enable
		0 = puts MPP_PAD at high Z and disables the block
	27	1 = MPP is enabled
	29 201	0x0: MPP_DISABLED
	18. Onlin	0x1: MPP_ENABLED

#### 0x0000A248 MPP3 ANA OUT CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### MPP3\_ANA\_OUT\_CTL

Bits	Name	Description
2:0	RESERVED	

## 0x0000A24A MPP3\_ANA\_IN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### MPP3\_ANA\_IN\_CTL

Bits	Name	Description
2:0	ROUTE_SEL	AMUX Channel Control
		0: Route to hkadc5
		1: Route to hkadc6
		2: Route to hkadc7
		3: Route to hkadc8
		4: Reserved
		5: Reserved
		6: Reserved
		7: Reserved
		0x0: HKADC5
		0x1: HKADC6
		0x2: HKADC7
		0x3: HKADC8
		0x4: Reserved
	\ (	0x5: Reserved
		0x6: Reserved
		0x7: Reserved

## 0x0000A24C MPP3\_SINK\_CTL

Type: RW

Clock: PBUS\_WRCLK

Reset State: 0x00

Reset Name: PERPH\_RB

#### MPP3\_SINK\_CTL

Bits	Name	Description
2:0	CURRENT_SEL	Current Sink Output Control
		0x0: CURRENT_5MA
		0x1: CURRENT_10MA
		0x2: CURRENT_15MA
		0x3: CURRENT_20MA
		0x4: CURRENT_25MA
		0x5: CURRENT_30MA
		0x6: CURRENT_35MA
		0x7: CURRENT_40MA

# Mpp\_ult Registers

#### 0x0000A300 MPP4\_REVISION1

#### MPP4 REVISION1

MPP4	_REVISION1		
Clock:	Type: R Clock: PBUS_WRCLK Reset State: 0x01		
Reset I	Name: N/A		
HW Ve	ersion Register [7:0]	0.05	
PMIC_	CONSTANT	2.21	
MPP4_	MPP4_REVISION1		
Bits	Name Name	Description	
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.	

## 0x0000A301 MPP4\_REVISION2

**Type:** R

Clock: PBUS WRCLK **Reset State:** 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### MPP4\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x0000A302 MPP4\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### MPP4\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x0000A303 MPP4 REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### MPP4\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x0000A304 MPP4\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x11

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### MPP4\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0x11: MPP

#### 0x0000A305 MPP4\_PERPH\_SUBTYPE

Type: R

#### MPP4\_PERPH\_SUBTYPE

Clock: PBUS_WRCLK Reset State: 0x04		
Reset Name: N/A		
Periphe	eral SubType	N
MPP4_	PERPH_SUBTYPE	
Bits	Name	Description
7:0	SUBTYPE	0x3: MPP_4CH_SINK
	. ( )	0x4: ULT_MPP_4CH_SINK
		0x5: MPP_4CH_AOUT
		0x6: ULT_MPP_4CH_AOUT
	7,0	0x6: ULT_MPP_4CH_AOUT 0x7: MPP_4CH_AOUT_SINK
	37.70	V
	G 1.09.21.01	0x7: MPP_4CH_AOUT_SINK

#### 0x0000A308 MPP4\_STATUS1

**Type:** R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: N/A

Status Registers

#### MPP4\_STATUS1

Bits	Name	Description
7	MPP_OK	0 = MPP is disabled
		1 = MPP is enabled
		0x0: MPP_DISABLED
		0x1: MPP_ENABLED

#### MPP4\_STATUS1 (cont.)

Bits	Name	Description
0	MPP_VAL	Value read by the input buffer, if enabled 0x0: MPP_INPUT_LOW 0x1: MPP_INPUT_HIGH

## 0x0000A310 MPP4\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Interrupt Real Time Status Bits

#### MPP4\_INT\_RT\_STS

Bits	Name	Description
0	MPP_IN_STS	0x0: INT_RT_STATUS_LOW
		0x1: INT_RT_STATUS_HIGH

### 0x0000A311 MPP4\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### MPP4\_INT\_SET\_TYPE

Bits	Name	Description
0	MPP_IN_TYPE	0x0: LEVEL
		0x1: EDGE

#### 0x0000A312 MPP4\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### MPP4\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	MPP_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

#### 0x0000A313 MPP4\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### MPP4\_INT\_POLARITY\_LOW

Bits	Name	Description
0	MPP_IN_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

### 0x0000A314 MPP4\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### MPP4\_INT\_LATCHED\_CLR

Bits	Name	Description
0	MPP_IN_LATCHED_CLR	

#### 0x0000A315 MPP4\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### MPP4\_INT\_EN\_SET

Bits	Name	Description
0	MPP_IN_EN_SET	0x0: INT_DISABLED
		0x1: INT_ENABLED

#### 0x0000A316 MPP4\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### MPP4 INT EN CLR

Bits	Name	Description
0	MPP_IN_EN_CLR	0x0: INT_DISABLED 0x1: INT_ENABLED

#### 0x0000A318 MPP4\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### MPP4\_INT\_LATCHED\_STS

Bits	Name	Description
0	MPP_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

#### 0x0000A319 MPP4\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### MPP4\_INT\_PENDING\_STS

Bits	Name	Description
0	MPP_IN_PENDING_STS	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING

#### 0x0000A31A MPP4\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### MPP4\_INT\_MID\_SEL

Name	Description
NT_MID_SEL	0x0: MID0
	0x1: MID1
	0x2: MID2
	0x3: MID3
V	· · V

## 0x0000A31B MPP4\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### MPP4\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR
		0x1: A

## 0x0000A340 MPP4\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

MPP Mode allows you to switch from one mode to another mode in a single register write.

#### MPP4\_MODE\_CTL

Bits	Name	Description
6:4	MODE	MPP Type:
		0x0: DIGITAL_INPUT
		0x1: DIGITAL_OUTPUT
		0x2: DIGITAL_IN_AND_OUT
		0x3: RESERVED3
		0x4: ANALOG_INPUT
		0x5: ANALOG_OUTPUT
		0x6: CURRENT_SINK
	. ( )	0x7: RESERVED7
2018:09:22101:02in 2018:5m@minife.in.com		

## MPP4\_MODE\_CTL (cont.)

Bits	Name	Description
3:0	EN_AND_SOURCE_SEL	When configured as a digital output Source select:
		0000 = 0
		0001 = 1
		0010 = paired MPP
		0011 = inverted paired MPP 0100 = Reserved
		0101 = Reserved
		0110 = Reserved
		0111 = Reserved
		1000 = DTEST1
		1001 = inverted DTEST1
		1010 = DTEST2
		1011 = inverted DTEST2
		1100 = DTEST3
		1101 = inverted DTEST3
	<b>\</b> (	1110 = DTEST4
		1111 = inverted DTEST4
		1 P
		Enable control when configured as AOUT, or Current Sink. MPP is
		enable whenever the selected condition is true.
	, 0,	0000 = 0 (mpp is always disabled) 0001 = 1 (mpp is always Enabled)
	2 2	0010 = paired MPP
	09, 1110	0011 = inverted paired MPP
	J. 8. 16.1.	0100 = Reserved
	Cole of thirth	0101 = Reserved
	1	0110 = Reserved
		0111 = Reserved
		1000 = DTEST1
		1001 = inverted DTEST1
		1010 = DTEST2
		1011 = inverted DTEST2
		1100 = DTEST3
		1101 = inverted DTEST3 1110 = DTEST4
		1111 = inverted DTEST4 0x0: LOW
		0x1: HIGH
		0x2: PAIRED MPP
		0x3: NOT_PAIRED_MPP
		0x4: RESERVED4
		0x5: RESERVED5
		0x6: RESERVED6
		0x7: RESERVED7
		0x8: DTEST1
		0x9: NOT_DTEST1

#### MPP4\_MODE\_CTL (cont.)

Bits	Name	Description
		0xA: DTEST2
		0xB: NOT_DTEST2
		0xC: DTEST3
		0xD: NOT_DTEST3
		0xE: DTEST4
		0xF: NOT_DTEST4

#### 0x0000A341 MPP4\_DIG\_VIN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

## MPP4\_DIG\_VIN\_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source:
		(refer to the device specification for the definition of VINx)
	, , , ,	0x0: VIN0
	2 2	0x1: VIN1
	, OS , if OS	0x2: VIN2
	OJS NEW	0x3: VIN3

#### 0x0000A343 MPP4\_DIG\_IN\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

**Enable DTEST buffers** 

#### MPP4\_DIG\_IN\_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4  0x0: DTEST_DISABLED  0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3  0x0: DTEST_DISABLED  0x1: DTEST_ENABLED

#### MPP4\_DIG\_IN\_CTL (cont.)

Bits	Name	Description
1	DTEST2	Route to DTEST2 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1 0x0: DTEST_DISABLED 0x1: DTEST_ENABLED

#### 0x0000A346 MPP4\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### MPP4\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	MPP Master enable
		0 = puts MPP_PAD at high Z and disables the block
	27	1 = MPP is enabled
	29 201	0x0: MPP_DISABLED
	18. Onlin	0x1: MPP_ENABLED

#### 0x0000A348 MPP4\_ANA\_OUT\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### MPP4\_ANA\_OUT\_CTL

Bits	Name	Description
2:0	RESERVED	

#### 0x0000A34A MPP4\_ANA\_IN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### MPP4\_ANA\_IN\_CTL

Bits	Name	Description
2:0	ROUTE_SEL	AMUX Channel Control
		0: Route to hkadc5
		1: Route to hkadc6
		2: Route to hkadc7
		3: Route to hkadc8
		4: Reserved
		5: Reserved
		6: Reserved
		7: Reserved
		0x0: HKADC5
		0x1: HKADC6
		0x2: HKADC7
		0x3: HKADC8
		0x4: Reserved
	\ (	0x5: Reserved
		0x6: Reserved
		0x7: Reserved

## 0x0000A34C MPP4\_SINK\_CTL

Type: RW

Clock: PBUS\_WRCLK

Reset State: 0x00

Reset Name: PERPH\_RB

#### MPP4\_SINK\_CTL

Bits	Name	Description
2:0	CURRENT_SEL	Current Sink Output Control
		0x0: CURRENT_5MA
		0x1: CURRENT_10MA
		0x2: CURRENT_15MA
		0x3: CURRENT_20MA
		0x4: CURRENT_25MA
		0x5: CURRENT_30MA
		0x6: CURRENT_35MA
		0x7: CURRENT_40MA

# 32 Gpio Registers

#### 0x0000C000 GPIO1\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### **GPIO1\_REVISION1**

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x0000C001 GPIO1\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC\_CONSTANT

#### **GPIO1\_REVISION2**

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x0000C002 GPIO1\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### **GPIO1\_REVISION3**

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x0000C003 GPIO1\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### **GPIO1\_REVISION4**

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 0x0000C004 GPIO1\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x10

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### **GPIO1\_PERPH\_TYPE**

Bits	Name	Description
7:0	TYPE	0x10: GPIO

#### 0x0000C005 GPIO1\_PERPH\_SUBTYPE

Type: R

#### **GPIO1\_PERPH\_SUBTYPE**

	PBUS_WRCLK State: 0x05	
Reset N	Name: N/A	
Periphe	eral SubType	
GPIO1	_PERPH_SUBTYPE	
GPIO1_ Bits	_PERPH_SUBTYPE  Name	Description
		Description  0x1: GPIO_4CH
Bits	Name	
Bits	Name	0x1: GPIO_4CH

#### 0x0000C008 **GPIO1\_STATUS1**

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: N/A

**Status Registers** 

#### **GPIO1\_STATUS1**

Bits	Name	Description
7	GPIO_OK	0x0: GPIO_DISABLED
		0x1: GPIO_ENABLED
0	GPIO_VAL	Value read by the input buffer, if enabled
		0x0: GPIO_INPUT_LOW
		0x1: GPIO_INPUT_HIGH

#### 0x0000C010 GPIO1\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Interrupt Real Time Status Bits

#### GPIO1\_INT\_RT\_STS

Bits	Name	Description
0	GPIO_IN_STS	0x0: INT_RT_STATUS_LOW
		0x1: INT_RT_STATUS_HIGH

#### 0x0000C011 GPIO1\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### GPIO1\_INT\_SET\_TYPE

Bits	Name	Description
0	GPIO_IN_TYPE	0x0: LEVEL
		0x1: EDGE

## 0x0000C012 GPIO1\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### **GPIO1\_INT\_POLARITY\_HIGH**

Bits	Name	Description
0	GPIO_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

#### 0x0000C013 GPIO1\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

#### **GPIO1\_INT\_POLARITY\_LOW**

Bits	Name	Description
0	GPIO_IN_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

#### 0x0000C014 GPIO1 INT LATCHED CLR

Type: W

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

writing a 1 to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### GPIO1\_INT\_LATCHED\_CLR

Bits	Name	Description
0	GPIO_IN_LATCHED_CLR	

#### 0x0000C015 GPIO1\_INT\_EN\_SET

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing 0 to this register has no effect. Writing a 1 will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### GPIO1\_INT\_EN\_SET

Bits	Name	Description
0	GPIO_IN_EN_SET	0x0: INT_DISABLED
		0x1: INT_ENABLED

#### 0x0000C016 GPIO1\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

writing 0 to this register has no effect. Writing a 1 will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### **GPIO1 INT EN CLR**

Bits	Name	Description
0	GPIO_IN_EN_CLR	0x0: INT_DISABLED
	9,019	0x1: INT_ENABLED

## 0x0000C018 GPIO1\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

**Reset Name:** N/A

Debug: Latched (Sticky) Interrupt. 1 indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### GPIO1\_INT\_LATCHED\_STS

Bits	Name	Description
0	GPIO_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

## 0x0000C019 GPIO1\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### GPIO1\_INT\_PENDING\_STS

Bits	Name	Description
0	GPIO_IN_PENDING_STS	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING

## 0x0000C01A GPIO1\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### GPIO1\_INT\_MID\_SEL

Name	Description
NT_MID_SEL	0x0: MID0
	0x1: MID1
	0x2: MID2
	0x3: MID3
V	· · V

#### 0x0000C01B GPIO1\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

#### **GPIO1\_INT\_PRIORITY**

Bits	Name	Description
0	INT_PRIORITY	0x0: SR 0x1: A

## 0x0000C040 GPIO1\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

GPIO Mode allows you to switch from one mode to another mode in a single register write.

## GPIO1\_MODE\_CTL

Bits	Name	Description
6:4	MODE	GPIO Mode:
		0x0: DIGITAL_INPUT
		0x1: DIGITAL_OUTPUT
	27.0	0x2: DIGITAL_IN_AND_OUT
	O' indie	0x3: RESERVED
3:0	EN_AND_SOURCE_SEL	Output Source select:
	30, 2M	(Note: bit zero is effectively an invert bit (every odd entry is
	14	inverted)
		0x0: LOW
		0x1: HIGH
		0x2: PAIRED_GPIO
		0x3: NOT_PAIRED_GPIO
		0x4: SPECIAL_FUNCTION1
		0x5: NOT_SPECIAL_FUNCTION1
		0x6: SPECIAL_FUNCTION2
		0x7: NOT_SPECIAL_FUNCTION2
		0x8: DTEST1
		0x9: NOT_DTEST1
		0xA: DTEST2
		0xB: NOT_DTEST2
		0xC: DTEST3
		0xD: NOT_DTEST3
		0xE: DTEST4
		0xF: NOT_DTEST4

## 0x0000C041 GPIO1\_DIG\_VIN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### GPIO1\_DIG\_VIN\_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source: (refer to the device specification for the definition of VINx)
		0x0: VIN0 0x1: VIN1 0x2: VIN2 0x3: VIN3 0x4: RESERVED4 0x5: RESERVED5 0x6: RESERVED6 0x7: RESERVED7

## 0x0000C042 GPIO1\_DIG\_PULL\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x04

0

Reset Name: PERPH\_RB

#### GPIO1\_DIG\_PULL\_CTL

Bits	Name	Description
2:0	PULLUP_SEL	Current source pulls:
		(Note: HW disables pulls for modes other than input and open- drain output)
		0x0: PULLUP_30UA
		0x1: PULLUP_1P5UA
		0x2: PULLUP_31P5UA
		0x3: PULLUP_1P5UA_30UA_BOOST
		0x4: PULLDOWN_10UA
		0x5: NO_PULL
		0x6: RESERVED6
		0x7: RESERVED7

## 0x0000C043 GPIO1\_DIG\_IN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

**Enable DTEST buffers** 

#### GPIO1\_DIG\_IN\_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
1	DTEST2	Route to DTEST2
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1
	27.0	0x0: DTEST_DISABLED
	09 indi	0x1: DTEST_ENABLED

### 0x0000C045 GPIO1\_DIG\_OUT\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

#### GPIO1\_DIG\_OUT\_CTL

Bits	Name	Description
5:4	OUTPUT_TYPE	Output buffer configuration 10= open drain PMOS (only drive high) 01=open drain NMOS (only drive low, i.e. I2C) 00=CMOS (drive high and low)  Open drain not supported in GPIOC flavor 0x0: CMOS
		0x1: OPEN_HIGH 0x2: OPEN_LOW

#### **GPIO1\_DIG\_OUT\_CTL** (cont.)

Bits	Name	Description
1:0	OUTPUT_DRV_SEL	Output buffer drive strength:
		0x0: RESERVED
		0x1: LOW
		0x2: MED
		0x3: HIGH

## 0x0000C046 GPIO1\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH RB

#### GPIO1\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	GPIO Master Enable
		0 = puts GPIO_PAD at high Z and disables the block
		1 = GPIO is enabled
	,0	0x0: GPIO_DISABLED
	20 7 de	0x1: GPIO_ENABLED

ONN

# 33 Gpio Registers

#### 0x0000C100 GPIO2\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### **GPIO2\_REVISION1**

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x0000C101 GPIO2\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC\_CONSTANT

#### GPIO2\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x0000C102 GPIO2\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### **GPIO2\_REVISION3**

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x0000C103 GPIO2 REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### GPIO2\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x0000C104 GPIO2\_PERPH\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x10

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### GPIO2\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0x10: GPIO

#### 0x0000C105 GPIO2\_PERPH\_SUBTYPE

**Type:** R

#### GPIO2\_PERPH\_SUBTYPE

	PBUS_WRCLK State: 0x05	
Reset N	Name: N/A	
Periphe	eral SubType	N
	_PERPH_SUBTYPE	·O,
GPIO2	_PERPH_SUBTYPE  Name	Description
		Description 0x1: GPIO_4CH
Bits	Name	
Bits	Name	0x1: GPIO_4CH

#### 0x0000C108 GPIO2\_STATUS1

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: N/A

**Status Registers** 

#### GPIO2\_STATUS1

Bits	Name	Description
7	GPIO_OK	0x0: GPIO_DISABLED
		0x1: GPIO_ENABLED
0	GPIO_VAL	Value read by the input buffer, if enabled
		0x0: GPIO_INPUT_LOW
		0x1: GPIO_INPUT_HIGH

#### 0x0000C110 GPIO2\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Interrupt Real Time Status Bits

#### GPIO2\_INT\_RT\_STS

Bits	Name	Description
0	GPIO_IN_STS	0x0: INT_RT_STATUS_LOW
		0x1: INT_RT_STATUS_HIGH

#### 0x0000C111 GPIO2\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### GPIO2\_INT\_SET\_TYPE

Bits	Name	Description
0	GPIO_IN_TYPE	0x0: LEVEL
		0x1: EDGE

#### 0x0000C112 GPIO2\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### GPIO2\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	GPIO_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

#### 0x0000C113 GPIO2\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

#### GPIO2\_INT\_POLARITY\_LOW

Bits	Name	Description
0	GPIO_IN_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

#### 0x0000C114 GPIO2 INT LATCHED CLR

Type: W

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

writing a 1 to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### GPIO2\_INT\_LATCHED\_CLR

Bits	Name	Description
0	GPIO_IN_LATCHED_CLR	

#### 0x0000C115 GPIO2\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing 0 to this register has no effect. Writing a 1 will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### GPIO2\_INT\_EN\_SET

Bits	Name	Description
0	GPIO_IN_EN_SET	0x0: INT_DISABLED
		0x1: INT_ENABLED

#### 0x0000C116 GPIO2\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing 0 to this register has no effect. Writing a 1 will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### **GPIO2 INT EN CLR**

Bits	Name	Description
0	GPIO_IN_EN_CLR	0x0: INT_DISABLED
	9,019	0x1: INT_ENABLED

#### 0x0000C118 GPIO2\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Debug: Latched (Sticky) Interrupt. 1 indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### GPIO2\_INT\_LATCHED\_STS

Bits	Name	Description
0	GPIO_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

#### 0x0000C119 GPIO2\_INT\_PENDING\_STS

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### GPIO2\_INT\_PENDING\_STS

Bits	Name	Description
0	GPIO_IN_PENDING_STS	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING

## 0x0000C11A GPIO2\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### GPIO2\_INT\_MID\_SEL

Name	Description
NT_MID_SEL	0x0: MID0
	0x1: MID1
	0x2: MID2
	0x3: MID3
V	· · V

### 0x0000C11B GPIO2\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

#### **GPIO2\_INT\_PRIORITY**

Е	Bits	Name	Description
	0	INT_PRIORITY	0x0: SR 0x1: A

## 0x0000C140 GPIO2\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

GPIO Mode allows you to switch from one mode to another mode in a single register write.

## GPIO2\_MODE\_CTL

Bits	Name	Description
6:4	MODE	GPIO Mode:
		0x0: DIGITAL_INPUT
		0x1: DIGITAL_OUTPUT
	27	0x2: DIGITAL_IN_AND_OUT
	9' "19"	0x3: RESERVED
3:0	EN_AND_SOURCE_SEL	Output Source select:
	20, 24	(Note: bit zero is effectively an invert bit (every odd entry is
	1	inverted)
		0x0: LOW
		0x1: HIGH
		0x2: PAIRED_GPIO
		0x3: NOT_PAIRED_GPIO
		0x4: SPECIAL_FUNCTION1
		0x5: NOT_SPECIAL_FUNCTION1
		0x6: SPECIAL_FUNCTION2
		0x7: NOT_SPECIAL_FUNCTION2
		0x8: DTEST1
		0x9: NOT_DTEST1
		0xA: DTEST2
		0xB: NOT_DTEST2
		0xC: DTEST3
		0xD: NOT_DTEST3
		0xE: DTEST4
		0xF: NOT_DTEST4

## 0x0000C141 GPIO2\_DIG\_VIN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### GPIO2\_DIG\_VIN\_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source:
		(refer to the device specification for the definition of VINx)
		0x0: VIN0
		0x1: VIN1
		0x2: VIN2
		0x3: VIN3
		0x4: RESERVED4
		0x5: RESERVED5
	10	0x6: RESERVED6
		0x7: RESERVED7
		. **

## 0x0000C142 GPIO2\_DIG\_PULL\_CTL

Type: RW

Clock: PBUS\_WRCLK

**Reset State:** 0x04

Reset Name: PERPH\_RB

#### GPIO2\_DIG\_PULL\_CTL

Bits	Name	Description
2:0	PULLUP_SEL	Current source pulls:
		(Note: HW disables pulls for modes other than input and open- drain output)
		0x0: PULLUP_30UA
		0x1: PULLUP_1P5UA
		0x2: PULLUP_31P5UA
		0x3: PULLUP_1P5UA_30UA_BOOST
		0x4: PULLDOWN_10UA
		0x5: NO_PULL
		0x6: RESERVED6
		0x7: RESERVED7

## 0x0000C143 GPIO2\_DIG\_IN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

**Enable DTEST buffers** 

#### GPIO2\_DIG\_IN\_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
1	DTEST2	Route to DTEST2
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1
	27.0	0x0: DTEST_DISABLED
	S OS MIND	0x1: DTEST_ENABLED

#### 0x0000C145 GPIO2\_DIG\_OUT\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

#### GPIO2\_DIG\_OUT\_CTL

Bits	Name	Description
5:4	OUTPUT_TYPE	Output buffer configuration 10= open drain PMOS (only drive high) 01=open drain NMOS (only drive low, i.e. I2C) 00=CMOS (drive high and low)  Open drain not supported in GPIOC flavor 0x0: CMOS
		0x1: OPEN_HIGH 0x2: OPEN_LOW

#### **GPIO2\_DIG\_OUT\_CTL** (cont.)

Bits	Name	Description
1:0	OUTPUT_DRV_SEL	Output buffer drive strength:
		0x0: RESERVED
		0x1: LOW
		0x2: MED
		0x3: HIGH

## 0x0000C146 GPIO2\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

#### GPIO2\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	GPIO Master Enable
		0 = puts GPIO_PAD at high Z and disables the block 1 = GPIO is enabled
	,0	0x0: GPIO_DISABLED
	92 45	0x1: GPIO_ENABLED

# **Gpio Registers**

### 0x0000C200 GPIO3\_REVISION1

#### **GPIO3\_REVISION1**

GPIO:	GPIO3_REVISION1			
Clock:	Type: R Clock: PBUS_WRCLK Reset State: 0x01			
Reset N	Name: N/A			
HW Ve	ersion Register [7:0]			
PMIC_	CONSTANT			
GPIO3	GPIO3_REVISION1			
Bits	Name O Name	Description		
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.		

## 0x0000C201 GPIO3\_REVISION2

Type: R

Clock: PBUS WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### GPIO3\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x0000C202 GPIO3\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### **GPIO3\_REVISION3**

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x0000C203 GPIO3\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### **GPIO3\_REVISION4**

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x0000C204 GPIO3\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x10

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### **GPIO3\_PERPH\_TYPE**

Bits	Name	Description
7:0	TYPE	0x10: GPIO

#### 0x0000C205 GPIO3\_PERPH\_SUBTYPE

Type: R

#### **GPIO3\_PERPH\_SUBTYPE**

	PBUS_WRCLK State: 0x01	
Reset Name: N/A		
Periphe	eral SubType	N
	_PERPH_SUBTYPE	·O,
GPIO3	_PERPH_SUBTYPE  Name	Description
		Description  0x1: GPIO_4CH
Bits	Name	
Bits	Name	0x1: GPIO_4CH

#### 0x0000C208 **GPIO3\_STATUS1**

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: N/A

**Status Registers** 

#### **GPIO3\_STATUS1**

Bits	Name	Description
7	GPIO_OK	0x0: GPIO_DISABLED 0x1: GPIO_ENABLED
0	GPIO_VAL	Value read by the input buffer, if enabled 0x0: GPIO_INPUT_LOW 0x1: GPIO_INPUT_HIGH

### 0x0000C210 GPIO3\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Interrupt Real Time Status Bits

#### GPIO3\_INT\_RT\_STS

Bits	Name	Description
0	GPIO_IN_STS	0x0: INT_RT_STATUS_LOW
		0x1: INT_RT_STATUS_HIGH

#### 0x0000C211 GPIO3\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### GPIO3\_INT\_SET\_TYPE

Bits	Name	Description
0	GPIO_IN_TYPE	0x0: LEVEL
		0x1: EDGE

#### 0x0000C212 GPIO3\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### **GPIO3\_INT\_POLARITY\_HIGH**

Bits	Name	Description
0	GPIO_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

#### 0x0000C213 GPIO3\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

#### **GPIO3\_INT\_POLARITY\_LOW**

Bits	Name	Description
0	GPIO_IN_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

### 0x0000C214 GPIO3 INT LATCHED CLR

Type: W

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

writing a 1 to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### GPIO3\_INT\_LATCHED\_CLR

Bits	Name	Description
0	GPIO_IN_LATCHED_CLR	

#### 0x0000C215 GPIO3\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing 0 to this register has no effect. Writing a 1 will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### GPIO3\_INT\_EN\_SET

Bits	Name	Description
0	GPIO_IN_EN_SET	0x0: INT_DISABLED 0x1: INT_ENABLED

#### 0x0000C216 GPIO3\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

writing 0 to this register has no effect. Writing a 1 will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### **GPIO3 INT EN CLR**

Bits	Name	Description
0	GPIO_IN_EN_CLR	0x0: INT_DISABLED
	97 018	0x1: INT_ENABLED

## 0x0000C218 GPIO3\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Debug: Latched (Sticky) Interrupt. 1 indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### GPIO3\_INT\_LATCHED\_STS

Bits	Name	Description
0	GPIO_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

#### 0x0000C219 GPIO3\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### GPIO3\_INT\_PENDING\_STS

Bits	Name	Description
0	GPIO_IN_PENDING_STS	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING

## 0x0000C21A GPIO3\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### GPIO3\_INT\_MID\_SEL

Name	Description
NT_MID_SEL	0x0: MID0
	0x1: MID1
	0x2: MID2
	0x3: MID3
V	· · V

#### 0x0000C21B GPIO3\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

#### **GPIO3\_INT\_PRIORITY**

Е	Bits	Name	Description
	0	INT_PRIORITY	0x0: SR 0x1: A

## 0x0000C240 GPIO3\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

GPIO Mode allows you to switch from one mode to another mode in a single register write.

#### GPIO3\_MODE\_CTL

Bits	Name	Description
6:4	MODE	GPIO Mode:
		0x0: DIGITAL_INPUT
		0x1: DIGITAL_OUTPUT
	25	0x2: DIGITAL_IN_AND_OUT
	09' indi	0x3: RESERVED
3:0	EN_AND_SOURCE_SEL	Output Source select:
	50x 34	(Note: bit zero is effectively an invert bit (every odd entry is inverted)
	V	0x0: LOW
		0x1: HIGH
		0x2: PAIRED_GPIO
		0x3: NOT_PAIRED_GPIO
		0x4: SPECIAL_FUNCTION1
		0x5: NOT_SPECIAL_FUNCTION1
		0x6: SPECIAL_FUNCTION2
		0x7: NOT_SPECIAL_FUNCTION2
		0x8: DTEST1
		0x9: NOT_DTEST1
		0xA: DTEST2
		0xB: NOT_DTEST2
		0xC: DTEST3
		0xD: NOT_DTEST3
		0xE: DTEST4
		0xF: NOT_DTEST4

## 0x0000C241 GPIO3\_DIG\_VIN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### GPIO3\_DIG\_VIN\_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source:
		(refer to the device specification for the definition of VINx)
		0x0: VIN0
		0x1: VIN1
		0x2: VIN2
		0x3: VIN3
		0x4: RESERVED4
		0x5: RESERVED5
		0x6: RESERVED6
		0x7: RESERVED7

## 0x0000C242 GPIO3\_DIG\_PULL\_CTL

Type: RW

Clock: PBUS\_WRCLK

**Reset State:** 0x04

Reset Name: PERPH\_RB

#### GPIO3\_DIG\_PULL\_CTL

Bits	Name	Description
2:0	PULLUP_SEL	Current source pulls:
		(Note: HW disables pulls for modes other than input and open- drain output)
		0x0: PULLUP_30UA
		0x1: PULLUP_1P5UA
		0x2: PULLUP_31P5UA
		0x3: PULLUP_1P5UA_30UA_BOOST
		0x4: PULLDOWN_10UA
		0x5: NO_PULL
		0x6: RESERVED6
		0x7: RESERVED7

## 0x0000C243 GPIO3\_DIG\_IN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

**Enable DTEST buffers** 

#### GPIO3\_DIG\_IN\_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
1	DTEST2	Route to DTEST2
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1
	27.0	0x0: DTEST_DISABLED
	5 .09 indi	0x1: DTEST_ENABLED

## 0x0000C245 GPIO3\_DIG\_OUT\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

#### GPIO3\_DIG\_OUT\_CTL

Bits	Name	Description
5:4	OUTPUT_TYPE	Output buffer configuration 10= open drain PMOS (only drive high) 01=open drain NMOS (only drive low, i.e. I2C) 00=CMOS (drive high and low)
		Open drain not supported in GPIOC flavor 0x0: CMOS 0x1: OPEN_HIGH 0x2: OPEN_LOW

#### GPIO3\_DIG\_OUT\_CTL (cont.)

Bits	Name	Description
1:0	OUTPUT_DRV_SEL	Output buffer drive strength:
		0x0: RESERVED
		0x1: LOW
		0x2: MED
		0x3: HIGH

## 0x0000C246 GPIO3\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

#### GPIO3\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	GPIO Master Enable
		0 = puts GPIO_PAD at high Z and disables the block
		1 = GPIO is enabled
	,0	0x0: GPIO_DISABLED
	3 7 die	0x1: GPIO_ENABLED

# 35 Gpio Registers

#### 0x0000C300 GPIO4\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### **GPIO4\_REVISION1**

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x0000C301 GPIO4\_REVISION2

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC\_CONSTANT

#### GPIO4\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x0000C302 GPIO4\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### **GPIO4\_REVISION3**

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x0000C303 GPIO4\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### **GPIO4\_REVISION4**

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 0x0000C304 GPIO4\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x10

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### **GPIO4\_PERPH\_TYPE**

Bits	Name	Description
7:0	TYPE	0x10: GPIO

#### 0x0000C305 GPIO4\_PERPH\_SUBTYPE

Type: R

#### **GPIO4\_PERPH\_SUBTYPE**

	PBUS_WRCLK State: 0x01	
Reset N	Name: N/A	
Periphe	eral SubType	N
GPIO4	_PERPH_SUBTYPE	·O,
GPIO4	_PERPH_SUBTYPE	Description
		Description  0x1: GPIO_4CH
Bits	Name	
Bits	Name	0x1: GPIO_4CH

#### 0x0000C308 GPIO4\_STATUS1

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: N/A

**Status Registers** 

#### **GPIO4\_STATUS1**

Bits	Name	Description
7	GPIO_OK	0x0: GPIO_DISABLED 0x1: GPIO_ENABLED
0	GPIO_VAL	Value read by the input buffer, if enabled 0x0: GPIO_INPUT_LOW 0x1: GPIO_INPUT_HIGH

#### 0x0000C310 GPIO4\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Interrupt Real Time Status Bits

#### GPIO4\_INT\_RT\_STS

Bits	Name	Description
0	GPIO_IN_STS	0x0: INT_RT_STATUS_LOW
		0x1: INT_RT_STATUS_HIGH

#### 0x0000C311 GPIO4 INT SET TYPE

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### GPIO4\_INT\_SET\_TYPE

Bits	Name	Description
0	GPIO_IN_TYPE	0x0: LEVEL
		0x1: EDGE

#### 0x0000C312 GPIO4\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### GPIO4\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	GPIO_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

#### 0x0000C313 GPIO4\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

#### GPIO4\_INT\_POLARITY\_LOW

Bits	Name	Description
0	GPIO_IN_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

### 0x0000C314 GPIO4 INT LATCHED CLR

Type: W

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

writing a 1 to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### GPIO4\_INT\_LATCHED\_CLR

Bits	Name	Description
0	GPIO_IN_LATCHED_CLR	

#### 0x0000C315 GPIO4\_INT\_EN\_SET

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing 0 to this register has no effect. Writing a 1 will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### GPIO4\_INT\_EN\_SET

Bits	Name	Description
0	GPIO_IN_EN_SET	0x0: INT_DISABLED
		0x1: INT_ENABLED

#### 0x0000C316 GPIO4\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

writing 0 to this register has no effect. Writing a 1 will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### **GPIO4 INT EN CLR**

Bits	Name	Description
0	GPIO_IN_EN_CLR	0x0: INT_DISABLED
	and the	0x1: INT_ENABLED

#### 0x0000C318 GPIO4\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

**Reset Name:** N/A

Debug: Latched (Sticky) Interrupt. 1 indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### GPIO4\_INT\_LATCHED\_STS

Bits	Name	Description
0	GPIO_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

#### 0x0000C319 GPIO4\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### GPIO4\_INT\_PENDING\_STS

Bits	Name	Description
0	GPIO_IN_PENDING_STS	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING

#### 0x0000C31A GPIO4\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### GPIO4\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0
		0x1: MID1
		0x2: MID2
		0x3: MID3

## 0x0000C31B GPIO4\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

#### **GPIO4\_INT\_PRIORITY**

Bits	Name	Description
0	INT_PRIORITY	0x0: SR
		0x1: A

## 0x0000C340 GPIO4\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

GPIO Mode allows you to switch from one mode to another mode in a single register write.

#### GPIO4\_MODE\_CTL

Bits	Name	Description
6:4	MODE	GPIO Mode:
		0x0: DIGITAL_INPUT
		0x1: DIGITAL_OUTPUT
	25	0x2: DIGITAL_IN_AND_OUT
	09' indi	0x3: RESERVED
3:0	EN_AND_SOURCE_SEL	Output Source select:
	50x 34	(Note: bit zero is effectively an invert bit (every odd entry is inverted)
	V	0x0: LOW
		0x1: HIGH
		0x2: PAIRED_GPIO
		0x3: NOT_PAIRED_GPIO
		0x4: SPECIAL_FUNCTION1
		0x5: NOT_SPECIAL_FUNCTION1
		0x6: SPECIAL_FUNCTION2
		0x7: NOT_SPECIAL_FUNCTION2
		0x8: DTEST1
		0x9: NOT_DTEST1
		0xA: DTEST2
		0xB: NOT_DTEST2
		0xC: DTEST3
		0xD: NOT_DTEST3
		0xE: DTEST4
		0xF: NOT_DTEST4

## 0x0000C341 GPIO4\_DIG\_VIN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### GPIO4\_DIG\_VIN\_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source:
		(refer to the device specification for the definition of VINx)
		0x0: VIN0
		0x1: VIN1
		0x2: VIN2
		0x3: VIN3
		0x4: RESERVED4
		0x5: RESERVED5
		0x6: RESERVED6
		0x7: RESERVED7

## 0x0000C342 GPIO4\_DIG\_PULL\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x04

Reset State. UAU4

Reset Name: PERPH\_RB

#### GPIO4\_DIG\_PULL\_CTL

Bits	Name	Description
2:0	PULLUP_SEL	Current source pulls:
		(Note: HW disables pulls for modes other than input and open-drain output)
		0x0: PULLUP_30UA
		0x1: PULLUP_1P5UA
		0x2: PULLUP_31P5UA
		0x3: PULLUP_1P5UA_30UA_BOOST
		0x4: PULLDOWN_10UA
		0x5: NO_PULL
		0x6: RESERVED6
		0x7: RESERVED7

## 0x0000C343 GPIO4\_DIG\_IN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

**Enable DTEST buffers** 

#### GPIO4\_DIG\_IN\_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
1	DTEST2	Route to DTEST2
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1
	27.0	0x0: DTEST_DISABLED
	5 .09 indi	0x1: DTEST_ENABLED

### 0x0000C345 GPIO4\_DIG\_OUT\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

#### GPIO4\_DIG\_OUT\_CTL

Bits	Name	Description
5:4	OUTPUT_TYPE	Output buffer configuration 10= open drain PMOS (only drive high) 01=open drain NMOS (only drive low, i.e. I2C) 00=CMOS (drive high and low)  Open drain not supported in GPIOC flavor 0x0: CMOS
		0x1: OPEN_HIGH 0x2: OPEN_LOW

#### **GPIO4\_DIG\_OUT\_CTL** (cont.)

Bits	Name	Description
1:0	OUTPUT_DRV_SEL	Output buffer drive strength:
		0x0: RESERVED
		0x1: LOW
		0x2: MED
		0x3: HIGH

## 0x0000C346 GPIO4\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

#### GPIO4\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	GPIO Master Enable
		0 = puts GPIO_PAD at high Z and disables the block 1 = GPIO is enabled
	,0	0x0: GPIO_DISABLED
	92 45	0x1: GPIO_ENABLED

# 36 Gpio Registers

### 0x0000C400 GPIO5\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### **GPIO5\_REVISION1**

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x0000C401 GPIO5\_REVISION2

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### GPIO5\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x0000C402 GPIO5\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### **GPIO5\_REVISION3**

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x0000C403 GPIO5\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### GPIO5\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x0000C404 GPIO5\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x10

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### **GPIO5\_PERPH\_TYPE**

Bits	Name	Description
7:0	TYPE	0x10: GPIO

#### 0x0000C405 GPIO5\_PERPH\_SUBTYPE

Type: R

#### **GPIO5\_PERPH\_SUBTYPE**

Clock: PBUS_WRCLK Reset State: 0x01 Reset Name: N/A		
Periphe	eral SubType	
GPIO5	_PERPH_SUBTYPE	·O,
GPIO5	_PERPH_SUBTYPE  Name	Description
		Description 0x1: GPIO_4CH
Bits	Name	
Bits	Name	0x1: GPIO_4CH

#### GPIO5\_STATUS1 0x0000C408

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: N/A

**Status Registers** 

#### GPIO5\_STATUS1

Bits	Name	Description
7	GPIO_OK	0x0: GPIO_DISABLED
		0x1: GPIO_ENABLED
0	GPIO_VAL	Value read by the input buffer, if enabled
		0x0: GPIO_INPUT_LOW
		0x1: GPIO_INPUT_HIGH

### 0x0000C410 GPIO5\_INT\_RT\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Interrupt Real Time Status Bits

#### GPIO5\_INT\_RT\_STS

Bits	Name	Description
0	GPIO_IN_STS	0x0: INT_RT_STATUS_LOW
		0x1: INT_RT_STATUS_HIGH

#### 0x0000C411 GPIO5\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### GPIO5\_INT\_SET\_TYPE

Bits	Name	Description
0	GPIO_IN_TYPE	0x0: LEVEL
		0x1: EDGE

## 0x0000C412 GPIO5\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### **GPIO5\_INT\_POLARITY\_HIGH**

Bits	Name	Description
0	GPIO_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

#### 0x0000C413 GPIO5\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

#### GPIO5\_INT\_POLARITY\_LOW

Bits	Name	Description
0	GPIO_IN_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

### 0x0000C414 GPIO5 INT LATCHED CLR

Type: W

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

writing a 1 to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### GPIO5\_INT\_LATCHED\_CLR

Bits	Name	Description
0	GPIO_IN_LATCHED_CLR	

#### 0x0000C415 GPIO5\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing 0 to this register has no effect. Writing a 1 will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### GPIO5\_INT\_EN\_SET

Bits	Name	Description
0	GPIO_IN_EN_SET	0x0: INT_DISABLED
		0x1: INT_ENABLED

#### 0x0000C416 GPIO5\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

writing 0 to this register has no effect. Writing a 1 will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### **GPIO5 INT EN CLR**

Bits	Name	Description
0	GPIO_IN_EN_CLR	0x0: INT_DISABLED
	and the	0x1: INT_ENABLED

### 0x0000C418 GPIO5\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Debug: Latched (Sticky) Interrupt. 1 indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### **GPIO5\_INT\_LATCHED\_STS**

Bits	Name	Description
0	GPIO_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

#### 0x0000C419 GPIO5\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

#### GPIO5\_INT\_PENDING\_STS

Bits	Name	Description
0	GPIO_IN_PENDING_STS	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING

## 0x0000C41A GPIO5\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### GPIO5\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0
		0x1: MID1
		0x2: MID2
		0x3: MID3

## 0x0000C41B GPIO5\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

#### **GPIO5\_INT\_PRIORITY**

Bits	Name	Description
0	INT_PRIORITY	0x0: SR
		0x1: A

## 0x0000C440 GPIO5\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

GPIO Mode allows you to switch from one mode to another mode in a single register write.

#### GPIO5\_MODE\_CTL

Bits	Name	Description
6:4	MODE	GPIO Mode:
		0x0: DIGITAL_INPUT
		0x1: DIGITAL_OUTPUT
	27.	0x2: DIGITAL_IN_AND_OUT
	9 ingle	0x3: RESERVED
3:0	EN_AND_SOURCE_SEL	Output Source select:
	50x 3m	(Note: bit zero is effectively an invert bit (every odd entry is inverted)
	V	0x0: LOW
		0x1: HIGH
		0x2: PAIRED_GPIO
		0x3: NOT_PAIRED_GPIO
		0x4: SPECIAL_FUNCTION1
		0x5: NOT_SPECIAL_FUNCTION1
		0x6: SPECIAL_FUNCTION2
		0x7: NOT_SPECIAL_FUNCTION2
		0x8: DTEST1
		0x9: NOT_DTEST1
		0xA: DTEST2
		0xB: NOT_DTEST2
		0xC: DTEST3
		0xD: NOT_DTEST3
		0xE: DTEST4
		0xF: NOT_DTEST4

## 0x0000C441 GPIO5\_DIG\_VIN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### GPIO5\_DIG\_VIN\_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source: (refer to the device specification for the definition of VINx)
		0x0: VIN0 0x1: VIN1 0x2: VIN2 0x3: VIN3 0x4: RESERVED4 0x5: RESERVED5 0x6: RESERVED6 0x7: RESERVED7

## 0x0000C442 GPIO5\_DIG\_PULL\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x04

Reset Name: PERPH\_RB

#### GPIO5\_DIG\_PULL\_CTL

Bits	Name	Description
2:0	PULLUP_SEL	Current source pulls:
		(Note: HW disables pulls for modes other than input and open-drain output)
		0x0: PULLUP_30UA
		0x1: PULLUP_1P5UA
		0x2: PULLUP_31P5UA
		0x3: PULLUP_1P5UA_30UA_BOOST
		0x4: PULLDOWN_10UA
		0x5: NO_PULL
		0x6: RESERVED6
		0x7: RESERVED7

### 0x0000C443 GPIO5\_DIG\_IN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

**Enable DTEST buffers** 

#### GPIO5\_DIG\_IN\_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
1	DTEST2	Route to DTEST2
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1
	27.0	0x0: DTEST_DISABLED
	5 .09 indi	0x1: DTEST_ENABLED

### 0x0000C445 GPIO5\_DIG\_OUT\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

#### GPIO5\_DIG\_OUT\_CTL

Bits	Name	Description
5:4	OUTPUT_TYPE	Output buffer configuration 10= open drain PMOS (only drive high) 01=open drain NMOS (only drive low, i.e. I2C) 00=CMOS (drive high and low)
		Open drain not supported in GPIOC flavor 0x0: CMOS 0x1: OPEN_HIGH 0x2: OPEN_LOW

## **GPIO5\_DIG\_OUT\_CTL** (cont.)

Bits	Name	Description
1:0	OUTPUT_DRV_SEL	Output buffer drive strength:
		0x0: RESERVED
		0x1: LOW
		0x2: MED
		0x3: HIGH

# 0x0000C446 GPIO5\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

## GPIO5\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	GPIO Master Enable
		0 = puts GPIO_PAD at high Z and disables the block
		1 = GPIO is enabled
	,0	0x0: GPIO_DISABLED
	3 7 die	0x1: GPIO_ENABLED

# 37 Gpio Registers

## 0x0000C500 GPIO6\_REVISION1

## **GPIO6\_REVISION1**

GPIO	6_REVISION1	
	R PBUS_WRCLK State: 0x01	
Reset N	Name: N/A	
HW Ve	ersion Register [7:0]	0.05
PMIC_	CONSTANT	
GPIO6	GPIO6_REVISION1	
Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x0000C501 GPIO6\_REVISION2

**Type:** R

Clock: PBUS WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

## GPIO6\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x0000C502 GPIO6\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### **GPIO6\_REVISION3**

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x0000C503 GPIO6\_REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

## GPIO6\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x0000C504 GPIO6\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x10

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

## GPIO6\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0x10: GPIO

## 0x0000C505 GPIO6\_PERPH\_SUBTYPE

Type: R

## GPIO6\_PERPH\_SUBTYPE

	PBUS_WRCLK State: 0x01	
Reset N	Name: N/A	
Periphe	eral SubType	N
GPIO6	_PERPH_SUBTYPE	·O,
GPIO6	_PERPH_SUBTYPE	Description
		Description  0x1: GPIO_4CH
Bits	Name	
Bits	Name	0x1: GPIO_4CH

#### GPIO6\_STATUS1 0x0000C508

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: N/A

**Status Registers** 

## GPIO6\_STATUS1

Bits	Name	Description
7	GPIO_OK	0x0: GPIO_DISABLED
		0x1: GPIO_ENABLED
0	GPIO_VAL	Value read by the input buffer, if enabled
		0x0: GPIO_INPUT_LOW
		0x1: GPIO_INPUT_HIGH

## 0x0000C510 GPIO6\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

Interrupt Real Time Status Bits

## GPIO6\_INT\_RT\_STS

Bits	Name	Description
0	GPIO_IN_STS	0x0: INT_RT_STATUS_LOW
		0x1: INT_RT_STATUS_HIGH

## 0x0000C511 GPIO6\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## GPIO6\_INT\_SET\_TYPE

Bits	Name	Description
0	GPIO_IN_TYPE	0x0: LEVEL
		0x1: EDGE

## 0x0000C512 GPIO6\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

## GPIO6\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	GPIO_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

## 0x0000C513 GPIO6\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

#### GPIO6\_INT\_POLARITY\_LOW

Bits	Name	Description
0	GPIO_IN_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

## 0x0000C514 GPIO6 INT LATCHED CLR

Type: W

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

writing a 1 to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

## GPIO6\_INT\_LATCHED\_CLR

Bits	Name	Description
0	GPIO_IN_LATCHED_CLR	

## 0x0000C515 GPIO6\_INT\_EN\_SET

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing 0 to this register has no effect. Writing a 1 will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

## GPIO6\_INT\_EN\_SET

Bits	Name	Description
0	GPIO_IN_EN_SET	0x0: INT_DISABLED
		0x1: INT_ENABLED

## 0x0000C516 GPIO6\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

writing 0 to this register has no effect. Writing a 1 will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

## GPIO6\_INT\_EN\_CLR

Bits	Name	Description
0	GPIO_IN_EN_CLR	0x0: INT_DISABLED
	and the	0x1: INT_ENABLED

## 0x0000C518 GPIO6\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Debug: Latched (Sticky) Interrupt. 1 indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

## GPIO6\_INT\_LATCHED\_STS

Bits	Name	Description
0	GPIO_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

## 0x0000C519 GPIO6\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

## GPIO6\_INT\_PENDING\_STS

Bits	Name	Description
0	GPIO_IN_PENDING_STS	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING

## 0x0000C51A GPIO6\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

## GPIO6\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: MID0
		0x1: MID1
		0x2: MID2
		0x3: MID3

## 0x0000C51B GPIO6\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

## GPIO6\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x0: SR
		0x1: A

## 0x0000C540 GPIO6\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

GPIO Mode allows you to switch from one mode to another mode in a single register write.

# GPIO6\_MODE\_CTL

Bits	Name	Description
6:4	MODE	GPIO Mode:
		0x0: DIGITAL_INPUT
		0x1: DIGITAL_OUTPUT
	27.0	0x2: DIGITAL_IN_AND_OUT
	O' indie	0x3: RESERVED
3:0	EN_AND_SOURCE_SEL	Output Source select:
	30, 2M	(Note: bit zero is effectively an invert bit (every odd entry is
	14	inverted)
		0x0: LOW
		0x1: HIGH
		0x2: PAIRED_GPIO
		0x3: NOT_PAIRED_GPIO
		0x4: SPECIAL_FUNCTION1
		0x5: NOT_SPECIAL_FUNCTION1
		0x6: SPECIAL_FUNCTION2
		0x7: NOT_SPECIAL_FUNCTION2
		0x8: DTEST1
		0x9: NOT_DTEST1
		0xA: DTEST2
		0xB: NOT_DTEST2
		0xC: DTEST3
		0xD: NOT_DTEST3
		0xE: DTEST4
		0xF: NOT_DTEST4

## 0x0000C541 GPIO6\_DIG\_VIN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

## GPIO6\_DIG\_VIN\_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source: (refer to the device specification for the definition of VINx)
		0x0: VIN0 0x1: VIN1 0x2: VIN2 0x3: VIN3 0x4: RESERVED4 0x5: RESERVED5 0x6: RESERVED6 0x7: RESERVED7

# 0x0000C542 GPIO6\_DIG\_PULL\_CTL

Type: RW

Clock: PBUS\_WRCLK

Reset State: 0x04

Reset Name: PERPH\_RB

## GPIO6\_DIG\_PULL\_CTL

Bits	Name	Description
2:0	PULLUP_SEL	Current source pulls:
		(Note: HW disables pulls for modes other than input and open-drain output)
		0x0: PULLUP_30UA
		0x1: PULLUP_1P5UA
		0x2: PULLUP_31P5UA
		0x3: PULLUP_1P5UA_30UA_BOOST
		0x4: PULLDOWN_10UA
		0x5: NO_PULL
		0x6: RESERVED6
		0x7: RESERVED7

# 0x0000C543 GPIO6\_DIG\_IN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

**Enable DTEST buffers** 

## GPIO6\_DIG\_IN\_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
1	DTEST2	Route to DTEST2
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1
	2.0	0x0: DTEST_DISABLED
	S OS MINDE	0x1: DTEST_ENABLED

## 0x0000C545 GPIO6\_DIG\_OUT\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

## GPIO6\_DIG\_OUT\_CTL

Bits	Name	Description
5:4	OUTPUT_TYPE	Output buffer configuration 10= open drain PMOS (only drive high) 01=open drain NMOS (only drive low, i.e. I2C) 00=CMOS (drive high and low)
		Open drain not supported in GPIOC flavor 0x0: CMOS 0x1: OPEN_HIGH 0x2: OPEN_LOW

## **GPIO6\_DIG\_OUT\_CTL** (cont.)

Bits	Name	Description
1:0	OUTPUT_DRV_SEL	Output buffer drive strength:
		0x0: RESERVED
		0x1: LOW
		0x2: MED
		0x3: HIGH

# 0x0000C546 GPIO6\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

## GPIO6\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	GPIO Master Enable
		0 = puts GPIO_PAD at high Z and disables the block 1 = GPIO is enabled
	,0	0x0: GPIO_DISABLED
	92 45	0x1: GPIO_ENABLED

# 38 Gpio Registers

## 0x0000C600 GPIO7\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

## **GPIO7\_REVISION1**

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x0000C601 GPIO7\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC\_CONSTANT

#### **GPIO7\_REVISION2**

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x0000C602 GPIO7\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### **GPIO7\_REVISION3**

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x0000C603 GPIO7 REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

## **GPIO7\_REVISION4**

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x0000C604 GPIO7\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x10

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

## **GPIO7\_PERPH\_TYPE**

Bits	Name	Description
7:0	TYPE	0x10: GPIO

## 0x0000C605 GPIO7\_PERPH\_SUBTYPE

Type: R

## **GPIO7\_PERPH\_SUBTYPE**

	PBUS_WRCLK State: 0x01	
Reset N	Name: N/A	
Periphe	eral SubType	N
GPIO7	_PERPH_SUBTYPE	-O,
GPIO7	_PERPH_SUBTYPE	Description
		Description  0x1: GPIO_4CH
Bits	Name	
Bits	Name	0x1: GPIO_4CH

#### GPIO7\_STATUS1 0x0000C608

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: N/A

**Status Registers** 

## **GPIO7\_STATUS1**

Bits	Name	Description
7	GPIO_OK	0x0: GPIO_DISABLED
		0x1: GPIO_ENABLED
0	GPIO_VAL	Value read by the input buffer, if enabled
		0x0: GPIO_INPUT_LOW
		0x1: GPIO_INPUT_HIGH

## 0x0000C610 GPIO7\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Interrupt Real Time Status Bits

#### GPIO7\_INT\_RT\_STS

Bits	Name	Description
0	GPIO_IN_STS	0x0: INT_RT_STATUS_LOW
		0x1: INT_RT_STATUS_HIGH

## 0x0000C611 GPIO7\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## GPIO7\_INT\_SET\_TYPE

Bits	Name	Description
0	GPIO_IN_TYPE	0x0: LEVEL
		0x1: EDGE

## 0x0000C612 GPIO7\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

## **GPIO7\_INT\_POLARITY\_HIGH**

Bits	Name	Description
0	GPIO_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

## 0x0000C613 GPIO7\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

#### **GPIO7\_INT\_POLARITY\_LOW**

Bits	Name	Description
0	GPIO_IN_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

## 0x0000C614 GPIO7 INT LATCHED CLR

Type: W

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

writing a 1 to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

## GPIO7\_INT\_LATCHED\_CLR

Bits	Name	Description
0	GPIO_IN_LATCHED_CLR	

## 0x0000C615 GPIO7\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing 0 to this register has no effect. Writing a 1 will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

## GPIO7\_INT\_EN\_SET

Bits	Name	Description
0	GPIO_IN_EN_SET	0x0: INT_DISABLED
		0x1: INT_ENABLED

## 0x0000C616 GPIO7\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

writing 0 to this register has no effect. Writing a 1 will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

## **GPIO7 INT EN CLR**

Bits	Name	Description
0	GPIO_IN_EN_CLR	0x0: INT_DISABLED
	97 018	0x1: INT_ENABLED

## 0x0000C618 GPIO7\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Debug: Latched (Sticky) Interrupt. 1 indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

## GPIO7\_INT\_LATCHED\_STS

Bits	Name	Description
0	GPIO_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

## 0x0000C619 GPIO7\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

## GPIO7\_INT\_PENDING\_STS

Bits	Name	Description
0	GPIO_IN_PENDING_STS	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING

## 0x0000C61A GPIO7\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

## GPIO7\_INT\_MID\_SEL

Name	Description
NT_MID_SEL	0x0: MID0
	0x1: MID1
	0x2: MID2
	0x3: MID3
V	· · V

## 0x0000C61B GPIO7\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

## **GPIO7\_INT\_PRIORITY**

Bits	Name	Description
0	INT_PRIORITY	0x0: SR
		0x1: A

## 0x0000C640 GPIO7\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

GPIO Mode allows you to switch from one mode to another mode in a single register write.

## GPIO7\_MODE\_CTL

Bits	Name	Description
6:4	MODE	GPIO Mode:
		0x0: DIGITAL_INPUT
		0x1: DIGITAL_OUTPUT
	27.	0x2: DIGITAL_IN_AND_OUT
	9 ingile	0x3: RESERVED
3:0	EN_AND_SOURCE_SEL	Output Source select:
	50x 34	(Note: bit zero is effectively an invert bit (every odd entry is inverted)
	V	0x0: LOW
		0x1: HIGH
		0x2: PAIRED_GPIO
		0x3: NOT_PAIRED_GPIO
		0x4: SPECIAL_FUNCTION1
		0x5: NOT_SPECIAL_FUNCTION1
		0x6: SPECIAL_FUNCTION2
		0x7: NOT_SPECIAL_FUNCTION2
		0x8: DTEST1
		0x9: NOT_DTEST1
		0xA: DTEST2
		0xB: NOT_DTEST2
		0xC: DTEST3
		0xD: NOT_DTEST3
		0xE: DTEST4
		0xF: NOT_DTEST4

# 0x0000C641 GPIO7\_DIG\_VIN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

## GPIO7\_DIG\_VIN\_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source: (refer to the device specification for the definition of VINx)
		0x0: VIN0 0x1: VIN1 0x2: VIN2 0x3: VIN3 0x4: RESERVED4 0x5: RESERVED5 0x6: RESERVED6 0x7: RESERVED7

# 0x0000C642 GPIO7\_DIG\_PULL\_CTL

Type: RW

Clock: PBUS\_WRCLK

**Reset State:** 0x04

Reset Name: PERPH\_RB

## GPIO7\_DIG\_PULL\_CTL

Bits	Name	Description
2:0	PULLUP_SEL	Current source pulls:
		(Note: HW disables pulls for modes other than input and open- drain output)
		0x0: PULLUP_30UA
		0x1: PULLUP_1P5UA
		0x2: PULLUP_31P5UA
		0x3: PULLUP_1P5UA_30UA_BOOST
		0x4: PULLDOWN_10UA
		0x5: NO_PULL
		0x6: RESERVED6
		0x7: RESERVED7

## 0x0000C643 GPIO7\_DIG\_IN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

**Enable DTEST buffers** 

## GPIO7\_DIG\_IN\_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
1	DTEST2	Route to DTEST2
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1
	27.0	0x0: DTEST_DISABLED
	5 .09 indi	0x1: DTEST_ENABLED

## 0x0000C645 GPIO7\_DIG\_OUT\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

## GPIO7\_DIG\_OUT\_CTL

Bits	Name	Description
5:4	OUTPUT_TYPE	Output buffer configuration 10= open drain PMOS (only drive high) 01=open drain NMOS (only drive low, i.e. I2C) 00=CMOS (drive high and low)
		Open drain not supported in GPIOC flavor 0x0: CMOS 0x1: OPEN_HIGH 0x2: OPEN_LOW

## **GPIO7\_DIG\_OUT\_CTL** (cont.)

Bits	Name	Description
1:0	OUTPUT_DRV_SEL	Output buffer drive strength:
		0x0: RESERVED
		0x1: LOW
		0x2: MED
		0x3: HIGH

# 0x0000C646 GPIO7\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

## GPIO7\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	GPIO Master Enable
		0 = puts GPIO_PAD at high Z and disables the block 1 = GPIO is enabled
	,0	0x0: GPIO_DISABLED
	92 45	0x1: GPIO_ENABLED

# 39 Gpio Registers

## 0x0000C700 GPIO8\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

## **GPIO8\_REVISION1**

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x0000C701 GPIO8\_REVISION2

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC\_CONSTANT

## **GPIO8\_REVISION2**

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x0000C702 GPIO8\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

## **GPIO8\_REVISION3**

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x0000C703 GPIO8 REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

## **GPIO8\_REVISION4**

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x0000C704 GPIO8\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x10

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

## GPIO8\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	0x10: GPIO

## 0x0000C705 GPIO8\_PERPH\_SUBTYPE

Type: R

## GPIO8\_PERPH\_SUBTYPE

	PBUS_WRCLK State: 0x01	
Reset N	Name: N/A	
Periphe	eral SubType	N
	_PERPH_SUBTYPE	·O,
GPIO8	_PERPH_SUBTYPE  Name	Description
		Description 0x1: GPIO_4CH
Bits	Name	
Bits	Name	0x1: GPIO_4CH

#### GPIO8\_STATUS1 0x0000C708

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: N/A

**Status Registers** 

## GPIO8\_STATUS1

Bits	Name	Description
7	GPIO_OK	0x0: GPIO_DISABLED
		0x1: GPIO_ENABLED
0	GPIO_VAL	Value read by the input buffer, if enabled
		0x0: GPIO_INPUT_LOW
		0x1: GPIO_INPUT_HIGH

## 0x0000C710 GPIO8\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Interrupt Real Time Status Bits

## GPIO8\_INT\_RT\_STS

Bits	Name	Description
0	GPIO_IN_STS	0x0: INT_RT_STATUS_LOW
		0x1: INT_RT_STATUS_HIGH

## 0x0000C711 GPIO8\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## GPIO8\_INT\_SET\_TYPE

Bits	Name	Description
0	GPIO_IN_TYPE	0x0: LEVEL
		0x1: EDGE

## 0x0000C712 GPIO8\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

## GPIO8\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	GPIO_IN_HIGH	0x0: HIGH_TRIGGER_DISABLED
		0x1: HIGH_TRIGGER_ENABLED

## 0x0000C713 GPIO8\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

## GPIO8\_INT\_POLARITY\_LOW

Bits	Name	Description
0	GPIO_IN_LOW	0x0: LOW_TRIGGER_DISABLED
		0x1: LOW_TRIGGER_ENABLED

## 0x0000C714 GPIO8\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

writing a 1 to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

## GPIO8\_INT\_LATCHED\_CLR

Bits	Name	Description
0	GPIO_IN_LATCHED_CLR	

## 0x0000C715 GPIO8\_INT\_EN\_SET

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing 0 to this register has no effect. Writing a 1 will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

## GPIO8\_INT\_EN\_SET

Bits	Name	Description
0	GPIO_IN_EN_SET	0x0: INT_DISABLED
		0x1: INT_ENABLED

## 0x0000C716 GPIO8\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

writing 0 to this register has no effect. Writing a 1 will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### **GPIO8 INT EN CLR**

Bits	Name	Description
0	GPIO_IN_EN_CLR	0x0: INT_DISABLED
	and the	0x1: INT_ENABLED

## 0x0000C718 GPIO8\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

Debug: Latched (Sticky) Interrupt. 1 indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

## GPIO8\_INT\_LATCHED\_STS

Bits	Name	Description
0	GPIO_IN_LATCHED_STS	0x0: NO_INT_LATCHED 0x1: INTERRUPT_LATCHED

## 0x0000C719 GPIO8\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

Debug: Pending is set if interrupt has been sent but not cleared.

## GPIO8\_INT\_PENDING\_STS

Bits	Name	Description
0	GPIO_IN_PENDING_STS	0x0: NO_INT_PENDING
		0x1: INTERRUPT_PENDING

## 0x0000C71A GPIO8\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

## GPIO8\_INT\_MID\_SEL

Name	Description
NT_MID_SEL	0x0: MID0
	0x1: MID1
	0x2: MID2
	0x3: MID3
V	· · V

## 0x0000C71B GPIO8\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

## **GPIO8\_INT\_PRIORITY**

Bits	Name	Description
0	INT_PRIORITY	0x0: SR 0x1: A

## 0x0000C740 GPIO8\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

GPIO Mode allows you to switch from one mode to another mode in a single register write.

## GPIO8\_MODE\_CTL

Bits	Name	Description
6:4	MODE	GPIO Mode:
		0x0: DIGITAL_INPUT
		0x1: DIGITAL_OUTPUT
	27.	0x2: DIGITAL_IN_AND_OUT
	9 ingile	0x3: RESERVED
3:0	EN_AND_SOURCE_SEL	Output Source select:
	50x 34	(Note: bit zero is effectively an invert bit (every odd entry is inverted)
	V	0x0: LOW
		0x1: HIGH
		0x2: PAIRED_GPIO
		0x3: NOT_PAIRED_GPIO
		0x4: SPECIAL_FUNCTION1
		0x5: NOT_SPECIAL_FUNCTION1
		0x6: SPECIAL_FUNCTION2
		0x7: NOT_SPECIAL_FUNCTION2
		0x8: DTEST1
		0x9: NOT_DTEST1
		0xA: DTEST2
		0xB: NOT_DTEST2
		0xC: DTEST3
		0xD: NOT_DTEST3
		0xE: DTEST4
		0xF: NOT_DTEST4

## 0x0000C741 GPIO8\_DIG\_VIN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

## GPIO8\_DIG\_VIN\_CTL

Bits	Name	Description
2:0	VOLTAGE_SEL	Select Voltage source: (refer to the device specification for the definition of VINx)
		0x0: VIN0 0x1: VIN1 0x2: VIN2 0x3: VIN3 0x4: RESERVED4 0x5: RESERVED5 0x6: RESERVED6 0x7: RESERVED7

# 0x0000C742 GPIO8\_DIG\_PULL\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x04

Reset Name: PERPH\_RB

## GPIO8\_DIG\_PULL\_CTL

Bits	Name	Description
2:0	PULLUP_SEL	Current source pulls:
		(Note: HW disables pulls for modes other than input and open- drain output)
		0x0: PULLUP_30UA
		0x1: PULLUP_1P5UA
		0x2: PULLUP_31P5UA
		0x3: PULLUP_1P5UA_30UA_BOOST
		0x4: PULLDOWN_10UA
		0x5: NO_PULL
		0x6: RESERVED6
		0x7: RESERVED7

# 0x0000C743 GPIO8\_DIG\_IN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

**Enable DTEST buffers** 

## GPIO8\_DIG\_IN\_CTL

Bits	Name	Description
3	DTEST4	Route to DTEST4
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
2	DTEST3	Route to DTEST3
		0x0: DTEST_DISABLED
	10	0x1: DTEST_ENABLED
1	DTEST2	Route to DTEST2
		0x0: DTEST_DISABLED
		0x1: DTEST_ENABLED
0	DTEST1	Route to DTEST1
	27.0	0x0: DTEST_DISABLED
	5 .09 indi	0x1: DTEST_ENABLED

## 0x0000C745 GPIO8\_DIG\_OUT\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

## GPIO8\_DIG\_OUT\_CTL

Bits	Name	Description
5:4	OUTPUT_TYPE	Output buffer configuration 10= open drain PMOS (only drive high) 01=open drain NMOS (only drive low, i.e. I2C) 00=CMOS (drive high and low)  Open drain not supported in GPIOC flavor 0x0: CMOS
		0x1: OPEN_HIGH 0x2: OPEN_LOW

## **GPIO8\_DIG\_OUT\_CTL** (cont.)

Bits	Name	Description
1:0	OUTPUT_DRV_SEL	Output buffer drive strength:
		0x0: RESERVED
		0x1: LOW
		0x2: MED
		0x3: HIGH

# 0x0000C746 GPIO8\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

## GPIO8\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	GPIO Master Enable
		0 = puts GPIO_PAD at high Z and disables the block 1 = GPIO is enabled
	,0	0x0: GPIO_DISABLED
	92 45	0x1: GPIO_ENABLED

# 40 Bclk\_gen\_main Registers

## 0x00011000 BCLK\_GEN\_MAIN\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

## BCLK\_GEN\_MAIN\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

## 0x00011001 BCLK\_GEN\_MAIN\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

## BCLK\_GEN\_MAIN\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x00011002 BCLK\_GEN\_MAIN\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** N/A

HW Version Register [23:16]

#### **BCLK\_GEN\_MAIN\_REVISION3**

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

## 0x00011003 BCLK GEN MAIN REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [31:24]

## **BCLK\_GEN\_MAIN\_REVISION4**

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00011004 BCLK\_GEN\_MAIN\_PERPH\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x1D

Reset Name: N/A

Peripheral Type

## BCLK\_GEN\_MAIN\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	BCLK GEN

#### 0x00011005 BCLK\_GEN\_MAIN\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: N/A

Peripheral SubType

#### BCLK\_GEN\_MAIN\_PERPH\_SUBTYPE

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Bits	Name	Description
7:0	SUBTYPE	BCLK GEN MAIN

# 41 Hfbuck2\_ctrl Registers

### 0x00011400 S1\_CTRL\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### S1\_CTRL\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	Indicates a change in the HW which is not intended to impact SW compatibility.

#### 

Type: R

Clock: PBUS\_WRCLK Reset State: 0x03

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### S1\_CTRL\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	Indicates a change in the HW which is not intended to impact SW compatibility.

## 0x00011402 S1\_CTRL\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

**Reset Name:** N/A

HW Version Register [23:16]

#### S1\_CTRL\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	Indicates expanded functionality. Minor version adds functionality while being backward compatibility for existing features.

## 0x00011403 S1\_CTRL\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x03

Reset Name: N/A

HW Version Register [31:24]

#### S1 CTRL REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	Indicates different interface version. Major version changes are not backward compatible.

#### 0x00011404 S1\_CTRL\_PERPH\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x03

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

### S1\_CTRL\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	SMPS 0x3: SMPS

## 0x00011405 S1\_CTRL\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: N/A

Peripheral SubType

#### S1\_CTRL\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	HFBUCK2 General Purpose Controller
		0x8: GENERAL_PURPOSE_CONTROLLER

#### 0x00011408 S1\_CTRL\_STATUS

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: N/A

Status Registers

#### S1\_CTRL\_STATUS

Bits	Name	Description
7	VREG_OK	0 = VREG output voltage is below VREG_OK threshold,,,, 1 = VREG output voltage is above VREG_OK threshold 0x0: VREG_OK_FALSE 0x1: VREG_OK_TRUE
5	ILS	Illegal Limit Stop. This is triggered when UL_Voltage < LL_Voltage. For more details look at HW/SW document 0x0: ILEGAL_LIMIT_STOP_FALSE 0x1: ILEGAL_LIMIT_STOP_TRUE
4	UL_VOLTAGE	Last voltage set was above UL_Voltage 0x0: UL_INT_FALSE 0x1: UL_INT_TRUE
3	LL_VOLTAGE	Last voltage set was below LL_Voltage 0x0: LL_INT_FALSE 0x1: LL_INT_TRUE
2	PS_TRUE	0 = buck is not pulse skipping,,,, 1 = buck is pulse skipping 0x0: PS_FALSE 0x1: PS_TRUE

#### S1\_CTRL\_STATUS (cont.)

Bits	Name	Description
1	NPM_TRUE	1 = VREG_OK and BUCK is in NPM 0x0: NPM_VREGOK_FALSE 0x1: NPM_VREGOK_TRUE
0	STEPPER_DONE	1 = stepper is done 0x0: STEPPER_DONE_FALSE 0x1: STEPPER_DONE_TRUE

#### 0x00011410 S1\_CTRL\_INT\_RT\_STS

#### S1\_CTRL\_INT\_RT\_STS

		0x0: STEPPER_DONE_FALSE 0x1: STEPPER_DONE_TRUE		
Type: Clock: Reset S Reset M	S1_CTRL_INT_RT_STS  Type: R Clock: PBUS_WRCLK Reset State: 0x00  Reset Name: PERPH_RB  Interrupt Real Time Status Bits  S1_CTRL_INT_RT_STS			
Bits	Name	Description		
1	VREG_FAULT_INT	OCP event has occurred 0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE		
0	VREG_OK_INT	Regulator has been successfully enabled 0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE		

#### 0x00011411 S1\_CTRL\_INT\_SET\_TYPE

Type: RW

Clock: PBUS WRCLK **Reset State:** 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## S1\_CTRL\_INT\_SET\_TYPE

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE

#### S1\_CTRL\_INT\_SET\_TYPE (cont.)

Bits	Name	Description
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

## 0x00011412 S1\_CTRL\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

## S1\_CTRL\_INT\_POLARITY\_HIGH

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
	20,	0x1: VREG_OK_INT_TRUE

#### 0x00011413 S1 CTRL INT POLARITY LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### S1\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

#### 0x00011414 S1\_CTRL\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### S1\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

### 0x00011415 S1\_CTRL\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### S1 CTRL INT EN SET

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

#### 

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### S1\_CTRL\_INT\_EN\_CLR

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

## 0x00011418 S1\_CTRL\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### S1 CTRL INT LATCHED STS

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

## 0x00011419 S1\_CTRL\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### S1\_CTRL\_INT\_PENDING\_STS

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

## 0x0001141A S1\_CTRL\_INT\_MID\_SEL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

#### S1\_CTRL\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: INT_MID_FALSE
	27,10	0x1: INT_MID_TRUE

## 0x0001141B S1\_CTRL\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### S1\_CTRL\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	SR=0 A=1
		0x0: INT_PRIORITY_FALSE
		0x1: INT_PRIORITY_TRUE

## 0x00011440 S1\_CTRL\_VOLTAGE\_CTL1

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

## PMIC\_LATCHED\_WRITE=VOLTAGE\_CTL2

#### S1\_CTRL\_VOLTAGE\_CTL1

Description
/ at steps of 12.5 mV (Vmin = 0.375 V, Vstep =
/ at steps of 25.0 mV (Vmin = 1.550 V, Vstep =
ALSE
RUE

## 0x00011441 S1\_CTRL\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x44

Reset Name: PERPH\_RB

#### S1\_CTRL\_VOLTAGE\_CTL2

Bits	Na	me	Description
6:0	V_SET	27.0	Voltage = Vmin + VSET*(Vstep)

#### 0x00011444 S1 CTRL PFM CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x85

Reset Name: PERPH\_RB

#### S1\_CTRL\_PFM\_CTL

Bits	Name	Description
7	PFM_VOLT_CTL	1=PFM voltage 1% over PWM voltage; 0=PFM voltage same as PWM voltage
		0x0: PFM_VOLT_BOOST_FALSE
		0x1: PFM_VOLT_BOOST_TRUE
6	PFM_IBOOST	1=Boost PFM Comparator bias current to 2uA; 0=bias current is 0.5uA 0x0: PFM_IBOOST_FALSE 0x1: PFM_IBOOST_TRUE

#### S1\_CTRL\_PFM\_CTL (cont.)

Bits	Name	Description
5	PFM_TYPE_I	1= Legacy PFM mode 0=Advanced PFM mode
		0x0: PFM_ADVANCED
		0x1: PFM_LEGACY
4	RESERVED	
3	RESERVED	
2	PFM_IPLIM_CTRL	0:Vdip_comp does not control IPLIM
		1:Set IPLIM same as PWM mode when Vdip_comp=1
		0x0: PFM_IPLIM_CTRL_FALSE
		0x1: PFM_IPLIM_CTRL_TRUE
1:0	PFM_IPLIM_DLY	00:Delay=75ns
		01:Delay=150ns
		10:Delay=300ns
		11:Delay=600ns
		0x0: PFM_IPLIM_CTRL_75NS
		0x1: PFM_IPLIMI_CTRL_150NS
		0x2: PFM_IPLIM_CTRL_300NS
		0x3: PFM_IPLIM_CTRL_600NS

## 0x00011445 S1\_CTRL\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK

**Reset State:** 0x80

Reset Name: PERPH\_RB

Define Buck Mode Transitions

#### S1\_CTRL\_MODE\_CTL

Bits	Name	Description
7	PWM	Force PWM  0x0: PWM_NO_FORCE
-	ALITO MODE	0x1: PWM_FORCE
6	AUTO_MODE	1=Automatically enter NPM based on current 0x0: AUTO_FALSE 0x1: AUTO_TRUE
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B) = '1' 0x0: FOLLOW_PMIC_AWAKE_FALSE 0x1: FOLLOW_PMIC_AWAKE_TRUE

#### S1\_CTRL\_MODE\_CTL (cont.)

Bits	Name	Description
3	FOLLOW_HWEN3	1' BUCK is in NPM when HWEN3 ='1', '0'= ignore HWEN3 0x0: FOLLOW_HWEN3_FALSE 0x1: FOLLOW_HWEN3_TRUE
2	FOLLOW_HWEN2	1' BUCK is in NPM when HWEN2 ='1', '0'= ignore HWEN2 0x0: FOLLOW_HWEN2_FALSE 0x1: FOLLOW_HWEN2_TRUE
1	FOLLOW_HWEN1	1' BUCK is in NPM when HWEN1 ='1', '0'= ignore HWEN1 0x0: FOLLOW_HWEN1_FALSE 0x1: FOLLOW_HWEN1_TRUE
0	FOLLOW_HWEN0	1' BUCK is in NPM when HWEN0 ='1', '0'= ignore HWEN0 0x0: FOLLOW_HWEN0_FALSE 0x1: FOLLOW_HWEN0_TRUE

## 0x00011446 S1\_CTRL\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

## S1\_CTRL\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	1' = Enable the BUCK, '0' = do not force BUCK on 0x0: BUCK_ENABLE_FALSE 0x1: BUCK_ENABLE_TRUE
3	FOLLOW_HWEN3	1' BUCK is enabled when HWEN3 ='1', '0'= ignore HWEN3 0x0: FOLLOW_HWEN3_FALSE 0x1: FOLLOW_HWEN3_TRUE
2	FOLLOW_HWEN2	1' BUCK is enabled when HWEN2 ='1', '0'= ignore HWEN2 0x0: FOLLOW_HWEN2_FALSE 0x1: FOLLOW_HWEN2_TRUE
1	FOLLOW_HWEN1	1' BUCK is enabled when HWEN1 ='1', '0'= ignore HWEN1 0x0: FOLLOW_HWEN1_FALSE 0x1: FOLLOW_HWEN1_TRUE
0	FOLLOW_HWEN0	1' BUCK is enabled when HWEN0 ='1', '0'= ignore HWEN0 0x0: FOLLOW_HWEN0_FALSE 0x1: FOLLOW_HWEN0_TRUE

## 0x00011448 S1\_CTRL\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH RB

#### S1\_CTRL\_PD\_CTL

Bits	Name	Description
7	PD_EN	1' = Enable the pull-down when the regulator is disabled, '0' = pull-down is always disabled. Preset by trim register CTL_TRIM4
		0x0: PD_ENABLE_FALSE
		0x1: PD_ENABLE_TRUE

## 0x00011468 S1\_CTRL\_UL\_LL\_CTRL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S1\_CTRL\_UL\_LL\_CTRL

Bits	Name	Description
7	UL_INT_EN	0 = Disable upper limit stop 1 = Enable upper limit stop 0x0: UL_INT_EN_FALSE 0x1: UL_INT_EN_TRUE
6	LL_INT_EN	0 = Disable lower limit stop 1 = Enable lower limit stop 0x0: LL_INT_EN_FALSE 0x1: LL_INT_EN_TRUE

### 0x00011469 S1\_CTRL\_UL\_VOLTAGE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x7F

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S1\_CTRL\_UL\_VOLTAGE

Bits	Name	Description
6:0	V_SET	Sets upper limit for the allowed output voltage range if LIMIT_LO_EN is asserted.
		For EXT_RANGE = 0:
		VLIMIT_STOP_LO = 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV), where m = <6:0>
		For EXT_RANGE = 1:
		VLIMIT_STOP_LO =1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV), where m = <6:0>

## 0x0001146B S1\_CTRL\_LL\_VOLTAGE

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_LOCKED=SEC ACCESS

#### S1\_CTRL\_LL\_VOLTAGE

Bits	Name	Description
6:0	V_SET	Sets lower limit for the allowed output voltage range if LIMIT_LO_EN is asserted.
		For EXT_RANGE = 0:
		VLIMIT_STOP_LO = 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV), where m = <6:0>
		For EXT_RANGE = 1:
		VLIMIT_STOP_LO =1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV), where m = <6:0>

### 0x0001147A S1\_CTRL\_CTLR\_MISC

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### S1\_CTRL\_CTLR\_MISC

Bits	Name	Description
7	SPARE_7	
6	SPARE_6	

#### S1\_CTRL\_CTLR\_MISC (cont.)

Bits	Name	Description
5	SPARE_5	
4	SPARE_4	
3	SPARE_3	
2	SPARE_2	1=OCP is reset when perph_en, en_ext, and when are all low, 0=OCP is reset by perph_en rising edge 0x1: SPARE_2_TRUE 0x0: SPARE_2_FALSE
1	SPARE_1	1=enable buck, 0=normal mode 0x1: SPARE_1_TRUE 0x0: SPARE_1_FALSE
0	SPARE_0	disable_ps_timeout 1=pulse skip timeout feature is disabled, 0=pulse skip timeout feature is enabled 0x1: SPARE_0_TRUE 0x0: SPARE_0_FALSE
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# 42 Ultbuck\_hc\_ps\_dig Registers

### 0x00011500 S1\_PS\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### S1\_PS\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	Indicates a change in the HW which is not intended to impact SW compatibility.

#### 0x00011501 S1\_PS\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### S1\_PS\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	Indicates a change in the HW which is not intended to impact SW compatibility.

#### 0x00011502 S1\_PS\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### S1\_PS\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	Indicates expanded functionality. Minor version adds functionality while being backward compatibility for existing features.

## 0x00011503 S1\_PS\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

**Reset Name:** N/A

HW Version Register [31:24]

## S1\_PS\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	Indicates different interface version. Major version changes are not backward compatible. There will be a new Programming Guide document per major revision.

## 0x00011504 S1\_PS\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x22

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### S1\_PS\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	SMPS
		0x16: SMPS

ONN

## 0x00011505 S1\_PS\_PERPH\_SUBTYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x06

**Reset Name:** N/A

Peripheral SubType

#### S1\_PS\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	1 PS_LV2p5A: ultbuck power stage
		2 PS_LV3p0A: ultbuck power stage
		3 PS_LV1p8A: ultbuck power stage
	25	4 PS_MV1p5A: ultbuck power stage
	ag atte	5 PS_MV2p5A: ultbuck power stage
	C. Capilles	6 PS2_LV3p0A: ultbuck power stage
	O'TO WE	7 PS2_MV2p5A: ultbuck power stage
	77.5	0x1: PS_LV2P5A
	V	0x2: PS_LV3P0A
		0x3: PS_LV1P8A
		0x4: PS_MV1P5A
		0x5: PS_MV2P5A
		0x6: PS2_LV3P0A
		0x7: PS2_MV2P5A

### 0x00011510 S1\_PS\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

Interrupt Real Time Status Bits

#### S1\_PS\_INT\_RT\_STS

Bits	Name	Description
1	HIGH_CURRENT_INT2	Buck current exceeds set level 2 0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	Buck current exceeds set level 1 0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### S1\_PS\_INT\_SET\_TYPE

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 0x00011512 S1\_PS\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### S1\_PS\_INT\_POLARITY\_HIGH

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 0x00011513 S1\_PS\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### S1\_PS\_INT\_POLARITY\_LOW

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

## 0x00011514 S1\_PS\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### S1\_PS\_INT\_LATCHED\_CLR

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 0x00011515 S1\_PS\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### S1\_PS\_INT\_EN\_SET

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

## 0x00011516 S1\_PS\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### S1\_PS\_INT\_EN\_CLR

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

## 0x00011518 S1\_PS\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### S1\_PS\_INT\_LATCHED\_STS

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

## 0x00011519 S1\_PS\_INT\_PENDING\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### S1\_PS\_INT\_PENDING\_STS

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE
	27 118	0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE
	201, Che	0x1: HIGH_CURRENT_INT1_TRUE

#### 0x0001151A S1\_PS\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### S1\_PS\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: INT_MID_FALSE
		0x1: INT_MID_TRUE

#### 0x0001151B S1\_PS\_INT\_PRIORITY

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### S1\_PS\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	SR=0 A=1
		0x0: INT_PRIORITY_FALSE
		0x1: INT_PRIORITY_TRUE

## 0x0001154A S1\_PS\_PWM\_CURRENT\_LIM\_CTL

**Type:** RW

Clock: PBUS\_WRCLK
Reset State: 0xB4

Reset Name: PERPH RB

#### S1\_PS\_PWM\_CURRENT\_LIM\_CTL

Bits	Name	Description
7	CURRENT_LIM_EN	0 = disable 1 = enable 0x0: CURRENT_LIM_EN_FALSE 0x1: CURRENT_LIM_EN_TRUE
5:3	CURRENT_LIM_AUTOINT_ SEL	These 3 bits are used to control the intermediate (hot PFM), current limit threshold whenever there is a mode transition between PFM and PWM mode under Auto-mode operation.  Iplimit threshold depends on selected current rating of the power stage:  HC (PS_LV2P5A, PS_LV3P0A, PS_MV2P5A, PS2_LV3P0A, PS2_MV2P5A)> Iplimit = 4400 mA - m*530 mA  LC (PS_LV1P8A, PS_MV1P5A)> Iplimit = 2700 mA - m*320 mA where m is the bit value of bit<5:3>  Note: The preset value of these bits is set to around 1A. The final values are device specific and listed in the device SBI table.  0x0: CURRENT_LIM_AUTOINT_SEL_LC_2700MA_HC_4400MA 0x1: CURRENT_LIM_AUTOINT_SEL_LC_2380MA_HC_3870MA 0x2: CURRENT_LIM_AUTOINT_SEL_LC_2060MA_HC_3340MA 0x3: CURRENT_LIM_AUTOINT_SEL_LC_1740MA_HC_2810MA 0x4: CURRENT_LIM_AUTOINT_SEL_LC_11420MA_HC_2280MA 0x5: CURRENT_LIM_AUTOINT_SEL_LC_1100MA_HC_1750MA 0x6: CURRENT_LIM_AUTOINT_SEL_LC_1100MA_HC_1750MA 0x6: CURRENT_LIM_AUTOINT_SEL_LC_780MA_HC_1220MA 0x7: CURRENT_LIM_AUTOINT_SEL_LC_780MA_HC_1220MA

#### S1\_PS\_PWM\_CURRENT\_LIM\_CTL (cont.)

Bits	Name	Description
2:0	CURRENT_LIM_PWM_SEL	These 3 bits are for current limit threshold programming when operating in PWM mode.
		Iplimit threshold depends on selected current rating of the power stage:
		HC (PS_LV2P5A, PS_LV3P0A, PS_MV2P5A, PS2_LV3P0A, PS2_MV2P5A)> Iplimit = 4400 mA - m*530 mA
		LC (PS_LV1P8A, PS_MV1P5A)> Iplimit = 2700 mA - m*320 mA
		where m is the bit value of bit<2:0>
		Note: The preset value of these bits is set by using Trim. Please refer to IPLIM_TRIM_OPT and Recommended defaults; however, the final values are device specific and listed in the
		device SBI table.
		0x0: CURRENT_LIM_PWM_SEL_LC_2700MA_HC_4400MA
		0x1: CURRENT_LIM_PWM_SEL_LC_2380MA_HC_3870MA
		0x2: CURRENT_LIM_PWM_SEL_LC_2060MA_HC_3340MA
		0x3: CURRENT_LIM_PWM_SEL_LC_1740MA_HC_2810MA
		0x4: CURRENT_LIM_PWM_SEL_LC_1420MA_HC_2280MA
		0x5: CURRENT_LIM_PWM_SEL_LC_1100MA_HC_1750MA
		0x6: CURRENT_LIM_PWM_SEL_LC_780MA_HC_1220MA
		0x7: CURRENT_LIM_PWM_SEL_LC_460MA_HC_690MA

## 0x0001154B S1\_PS\_PFM\_CURRENT\_LIM\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x84

Reset Name: PERPH RB

#### S1\_PS\_PFM\_CURRENT\_LIM\_CTL

Bits	Name	Description
7	CURRENT_LIM_EN	0 = disable
		1 = enable
		0x0: CURRENT_LIM_EN_FALSE
		0x1: CURRENT_LIM_EN_TRUE

#### S1\_PS\_PFM\_CURRENT\_LIM\_CTL (cont.)

Bits	Name	Description
2:0	CURRENT_LIM_SEL	Iplimit_sel<2:0> for current limit threshold programming when operating in PFM mode.
		Iplimit = 800 mA - m * 100 mA
		where m is the bit value of iplimit_sel<2:0>
		Note: The preset value and the final values of these bits are device specific and listed in the device SBI table.
		0x0: CURRENT_LIM_SEL_800MA
		0x1: CURRENT_LIM_SEL_700MA
		0x2: CURRENT_LIM_SEL_600MA
		0x3: CURRENT_LIM_SEL_500MA
		0x4: CURRENT_LIM_SEL_400MA
		0x5: CURRENT_LIM_SEL_300MA
		0x6: CURRENT_LIM_SEL_200MA
		0x7: CURRENT_LIM_SEL_100MA

## 0x00011580 S1\_PS\_HCINT\_EN

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

## S1\_PS\_HCINT\_EN

Bits	Name	Description
7	HCINT_EN	0 = INT disable
		1 = INT enable
		0x0: INT_DISABLE
		0x1: INT_ENABLE

## 0x00011581 S1\_PS\_HCINT\_CONTROL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

## S1\_PS\_HCINT\_CONTROL

Bits	Name	Description
5	SET_WINDOW_WIDTH	This bit controls the deglitch window to set interrupt based on no. of cycles of 32KHz clock 0 = 2cycles to set 1 = 16cycles to set 0x0: CYCLES2 0x1: CYCLES16
4	RESET_WINDOW_WIDTH	This bit controls the deglitch window to reset interrupt based on no. of cycles of 32KHz clock 0 = 2cycles to reset 1 = 16cycles to reset 0x0: CYCLESRESET2 0x1: CYCLESRESET16
3:2	INT2_CUR_THRESHOLD	rated current - 10%*(m+1) 0x0: RATED_CURRENT_90PCT 0x1: RATED_CURRENT_80PCT 0x2: RATED_CURRENT_70PCT 0x3: RATED_CURRENT_60PCT
1:0	INT1_CUR_THRESHOLD	rated current - 10%*(m+3) 0x0: RATED_CURRENT_70PCT 0x1: RATED_CURRENT_60PCT 0x2: RATED_CURRENT_50PCT 0x3: RATED_CURRENT_40PCT

# 43 Bclk\_gen\_clk Registers

### 0x00011600 S1\_FREQ\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

# S1\_FREQ\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

#### 0x00011601 S1\_FREQ\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: N/A

HW Version Register [15:8]

#### S1\_FREQ\_REVISION2

Bit	S Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00011604 S1\_FREQ\_PERPH\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x1D

Reset Name: N/A

Peripheral Type

#### S1\_FREQ\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	BCLK GEN

### 0x00011605 S1\_FREQ\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x19

Reset Name: N/A

Peripheral SubType

## S1\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	BCLK GEN CLK

## 0x00011646 S1\_FREQ\_CLK\_ENABLE

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH\_RB

PMIC\_LOCKED=SEC\_ACCESS

### S1\_FREQ\_CLK\_ENABLE

Bits	Name	Description
7	EN_CLK_INT	0 = do not force the clock on
		1 = enable the clock
		0x0: FORCE_EN_DISABLED
		0x1: FORCE_EN_ENABLED

#### S1\_FREQ\_CLK\_ENABLE (cont.)

Bits	Name	Description
0	FOLLOW_CLK_SX_REQ	0 = ignore smps_clk_req <x></x>
		1 = clock is enabled when the clocks request is high smps_clk_req <x>='1'</x>
		0x0: FALLOW_CLK_REQ_DISABLED
		0x1: FALLOW_CLK_REQ_ENABLED

## 0x00011650 S1\_FREQ\_CLK\_DIV

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x05

Reset Name: PERPH\_RB

PMIC LOCKED=SEC ACCESS, PMIC GANGED

## S1\_FREQ\_CLK\_DIV

Bits	Name	Description
3:0	CLK_DIV	clock_ frequency = 19.2MHz / (CLK_DIV + 1)
		FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz
	0,1 1,5	HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz
	.O. ville	CLK_DIV = 0 is not supported, it will generate 9.6 MHz
	2018. 24 Chillip	0x0: FREQ_9M6HZ_0
	2.5	0x1: FREQ_9M6HZ
	1	0x2: FREQ_6M4HZ
		0x3: FREQ_4M8HZ
		0x4: FREQ_3M8HZ
		0x5: FREQ_3M2HZ
		0x6: FREQ_2M7HZ
		0x7: FREQ_2M4HZ
		0x8: FREQ_2M1HZ
		0x9: FREQ_1M9HZ
		0xA: FREQ_1M7HZ
		0xB: FREQ_1M6HZ
		0xC: FREQ_1M5HZ
		0xD: FREQ_1M4HZ
		0xE: FREQ_1M3HZ
		0xF: FREQ_1M2HZ

### 0x00011651 S1\_FREQ\_CLK\_PHASE

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x07

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S1\_FREQ\_CLK\_PHASE

Bits	Name	Description
3:0	CLK_PHASE	Distributed clock phase select:
		clock phase delay = clock period * (CLK_PHASE / 16)

## 0x000116C0 S1\_FREQ\_GANG\_CTL1

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S1\_FREQ\_GANG\_CTL1

Bits	Name	Description
7:0	GANG_LEADER_PID	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

## 0x000116C1 S1\_FREQ\_GANG\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

#### S1\_FREQ\_GANG\_CTL2

Bits	Name	Description
7	GANG_EN	0 = disable
		1 = enable
		When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral
		0x0: GANGING_DISABLED
		0x1: GANGING_ENABLED



# 44 Hfbuck2\_ctrl Registers

### 0x00011700 S2\_CTRL\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### S2\_CTRL\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	Indicates a change in the HW which is not intended to impact SW compatibility.

### 0x00011701 S2\_CTRL\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x03

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### S2\_CTRL\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	Indicates a change in the HW which is not intended to impact SW compatibility.

### 0x00011702 S2\_CTRL\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [23:16]

#### S2\_CTRL\_REVISION3

	on
7:0 ANA_MINOR Indicates expanded functionality. Mir while being backward compatibility for	,

## 0x00011703 S2\_CTRL\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x03

Reset Name: N/A

HW Version Register [31:24]

#### S2 CTRL REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	Indicates different interface version. Major version changes are not backward compatible. There will be a new Programming Guide document per major revision

## 0x00011704 S2\_CTRL\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x03

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### S2\_CTRL\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	SMPS
		0x3: SMPS

#### 0x00011705 S2\_CTRL\_PERPH\_SUBTYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x08

**Reset Name:** N/A

Peripheral SubType

#### S2\_CTRL\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	HFBUCK2 General Purpose Controller
		0x8: GENERAL_PURPOSE_CONTROLLER

#### 0x00011708 S2\_CTRL\_STATUS

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

**Reset Name:** N/A

Status Registers

#### S2\_CTRL\_STATUS

Bits	Name	Description
7	VREG_OK	0 = VREG output voltage is below VREG_OK threshold,,,,
		1 = VREG output voltage is above VREG_OK threshold
		0x0: VREG_OK_FALSE
		0x1: VREG_OK_TRUE
5	ILS	Illegal Limit Stop. This is triggered when UL_Voltage < LL_Voltage.
		For more details look at HW/SW document
		0x0: ILEGAL_LIMIT_STOP_FALSE
		0x1: ILEGAL_LIMIT_STOP_TRUE
4	UL_VOLTAGE	Last voltage set was above UL_Voltage
		0x0: UL_INT_FALSE
		0x1: UL_INT_TRUE

#### S2\_CTRL\_STATUS (cont.)

Bits	Name	Description
3	LL_VOLTAGE	Last voltage set was below LL_Voltage
		0x0: LL_INT_FALSE
		0x1: LL_INT_TRUE
2	PS_TRUE	0 = buck is not pulse skipping,,,,
		1 = buck is pulse skipping
		0x0: PS_FALSE
		0x1: PS_TRUE
1	NPM_TRUE	1 = VREG_OK and BUCK is in NPM
		0x0: NPM_VREGOK_FALSE
		0x1: NPM_VREGOK_TRUE
0	STEPPER_DONE	1 = stepper is done
		0x0: STEPPER_DONE_FALSE
		0x1: STEPPER_DONE_TRUE

## 0x00011710 S2\_CTRL\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

Interrupt Real Time Status Bits

#### S2\_CTRL\_INT\_RT\_STS

Bits	Name	Description
1	VREG_FAULT_INT	OCP event has occurred 0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	Regulator has been successfully enabled 0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

#### 0x00011711 S2\_CTRL\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### S2\_CTRL\_INT\_SET\_TYPE

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

## 0x00011712 S2\_CTRL\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### **S2 CTRL INT POLARITY HIGH**

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
	027	0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
	201, CME	0x1: VREG_OK_INT_TRUE

#### 0x00011713 S2\_CTRL\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### S2\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

#### 0x00011714 S2\_CTRL\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### S2\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

#### 0x00011715 S2\_CTRL\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### S2 CTRL INT EN SET

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

#### 

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### S2\_CTRL\_INT\_EN\_CLR

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

# 0x00011718 S2 CTRL INT LATCHED STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### S2 CTRL INT LATCHED STS

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

# 0x00011719 S2\_CTRL\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### S2\_CTRL\_INT\_PENDING\_STS

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

# 0x0001171A S2\_CTRL\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

#### S2\_CTRL\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: INT_MID_FALSE
	02 119	0x1: INT_MID_TRUE

## 0x0001171B S2\_CTRL\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### S2\_CTRL\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	SR=0 A=1
		0x0: INT_PRIORITY_FALSE
		0x1: INT_PRIORITY_TRUE

#### 0x00011740 S2\_CTRL\_VOLTAGE\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

# PMIC\_LATCHED\_WRITE=VOLTAGE\_CTL2

#### S2\_CTRL\_VOLTAGE\_CTL1

Bits	Name	Description
0	RANGE	0 : 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV)
		1 : 1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV)
		0x0: RANGE_HV_FALSE
		0x1: RANGE_HV_TRUE

# 0x00011741 S2\_CTRL\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x44

Reset Name: PERPH RB

#### S2\_CTRL\_VOLTAGE\_CTL2

Bits		Name	0	Description
6:0	V_SET		2.0	Voltage = Vmin + VSET*(Vstep)

# 0x00011744 S2\_CTRL\_PFM\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x85

Reset Name: PERPH RB

#### S2\_CTRL\_PFM\_CTL

Bits	Name	Description
7	PFM_VOLT_CTL	1=PFM voltage 1% over PWM voltage; 0=PFM voltage same as PWM voltage
		0x0: PFM_VOLT_BOOST_FALSE
		0x1: PFM_VOLT_BOOST_TRUE
6	PFM_IBOOST	1=Boost PFM Comparator bias current to 2uA; 0=bias current is 0.5uA 0x0: PFM_IBOOST_FALSE 0x1: PFM_IBOOST_TRUE

#### S2\_CTRL\_PFM\_CTL (cont.)

Bits	Name	Description
5	PFM_TYPE_I	1= Legacy PFM mode
		0=Advanced PFM mode
		0x0: PFM_ADVANCED
		0x1: PFM_LEGACY
4	RESERVED	
3	RESERVED	
2	PFM_IPLIM_CTRL	0:Vdip_comp does not control IPLIM
		1:Set IPLIM same as PWM mode when Vdip_comp=1
		0x0: PFM_IPLIM_CTRL_FALSE
		0x1: PFM_IPLIM_CTRL_TRUE
1:0	PFM_IPLIM_DLY	00:Delay=75ns
		01:Delay=150ns
		10:Delay=300ns
	\ (	11:Delay=600ns
		0x0: PFM_IPLIM_CTRL_75NS
		0x1: PFM_IPLIMI_CTRL_150NS
	. ( )	0x2: PFM_IPLIM_CTRL_300NS
		0x3: PFM_IPLIM_CTRL_600NS

#### S2\_CTRL\_MODE\_CTL 0x00011745

Type: RW

Clock: PBUS WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

Define Buck Mode Transitions

#### S2\_CTRL\_MODE\_CTL

Bits	Name	Description
7	PWM	Force PWM
		0x0: PWM_NO_FORCE
		0x1: PWM_FORCE
6	AUTO_MODE	1=Automatically enter NPM based on current
		0x0: AUTO_FALSE
		0x1: AUTO_TRUE
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B) = '1'
		0x0: FOLLOW_PMIC_AWAKE_FALSE
		0x1: FOLLOW_PMIC_AWAKE_TRUE

#### S2\_CTRL\_MODE\_CTL (cont.)

Bits	Name	Description
3	FOLLOW_HWEN3	1' BUCK is in NPM when HWEN3 ='1', '0'= ignore HWEN3
		0x0: FOLLOW_HWEN3_FALSE
		0x1: FOLLOW_HWEN3_TRUE
2	FOLLOW_HWEN2	1' BUCK is in NPM when HWEN2 ='1', '0'= ignore HWEN2
		0x0: FOLLOW_HWEN2_FALSE
		0x1: FOLLOW_HWEN2_TRUE
1	FOLLOW_HWEN1	1' BUCK is in NPM when HWEN1 ='1', '0'= ignore HWEN1
		0x0: FOLLOW_HWEN1_FALSE
		0x1: FOLLOW_HWEN1_TRUE
0	FOLLOW_HWEN0	1' BUCK is in NPM when HWEN0 ='1', '0'= ignore HWEN0
		0x0: FOLLOW_HWEN0_FALSE
		0x1: FOLLOW_HWEN0_TRUE

# 0x00011746 S2\_CTRL\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

# S2\_CTRL\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	1' = Enable the BUCK, '0' = do not force BUCK on 0x0: BUCK_ENABLE_FALSE 0x1: BUCK_ENABLE_TRUE
3	FOLLOW_HWEN3	1' BUCK is enabled when HWEN3 ='1', '0'= ignore HWEN3 0x0: FOLLOW_HWEN3_FALSE 0x1: FOLLOW_HWEN3_TRUE
2	FOLLOW_HWEN2	1' BUCK is enabled when HWEN2 ='1', '0'= ignore HWEN2 0x0: FOLLOW_HWEN2_FALSE 0x1: FOLLOW_HWEN2_TRUE
1	FOLLOW_HWEN1	1' BUCK is enabled when HWEN1 ='1', '0'= ignore HWEN1 0x0: FOLLOW_HWEN1_FALSE 0x1: FOLLOW_HWEN1_TRUE
0	FOLLOW_HWEN0	1' BUCK is enabled when HWEN0 ='1', '0'= ignore HWEN0 0x0: FOLLOW_HWEN0_FALSE 0x1: FOLLOW_HWEN0_TRUE

#### 0x00011748 S2\_CTRL\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH RB

#### S2\_CTRL\_PD\_CTL

Bits	Name	Description
7	PD_EN	1' = Enable the pull-down when the regulator is disabled, '0' = pull-down is always disabled. Preset by trim register CTL_TRIM4
		0x0: PD_ENABLE_FALSE
		0x1: PD_ENABLE_TRUE

# 0x00011768 S2\_CTRL\_UL\_LL\_CTRL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S2\_CTRL\_UL\_LL\_CTRL

Bits	Name	Description
7	UL_INT_EN	0 = Disable upper limit stop 1 = Enable upper limit stop 0x0: UL_INT_EN_FALSE 0x1: UL_INT_EN_TRUE
6	LL_INT_EN	0 = Disable lower limit stop 1 = Enable lower limit stop 0x0: LL_INT_EN_FALSE 0x1: LL_INT_EN_TRUE

#### 0x00011769 S2\_CTRL\_UL\_VOLTAGE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x7F

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S2\_CTRL\_UL\_VOLTAGE

Bits	Name	Description
6:0	V_SET	Sets upper limit for the allowed output voltage range if LIMIT_LO_EN is asserted.
		For EXT_RANGE = 0:
		VLIMIT_STOP_LO = 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV), where m = <6:0>
		For EXT_RANGE = 1:
		VLIMIT_STOP_LO =1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV), where m = <6:0>

# 0x0001176B S2\_CTRL\_LL\_VOLTAGE

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_LOCKED=SEC ACCESS

#### S2\_CTRL\_LL\_VOLTAGE

Bits	Name	Description
6:0	V_SET	Sets lower limit for the allowed output voltage range if LIMIT_LO_EN is asserted.
		For EXT_RANGE = 0:
		VLIMIT_STOP_LO = 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV), where m = <6:0>
		For EXT_RANGE = 1:
		VLIMIT_STOP_LO =1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV), where m = <6:0>

#### 0x0001177A S2\_CTRL\_CTLR\_MISC

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### S2\_CTRL\_CTLR\_MISC

Bits	Name	Description
7	SPARE_7	
6	SPARE_6	

#### S2\_CTRL\_CTLR\_MISC (cont.)

Bits	Name	Description
5	SPARE_5	
4	SPARE_4	
3	SPARE_3	
2	SPARE_2	1=OCP is reset when perph_en, en_ext, and when are all low, 0=OCP is reset by perph_en rising edge 0x1: SPARE_2_TRUE 0x0: SPARE_2_FALSE
1	SPARE_1	1=enable buck, 0=normal mode 0x1: SPARE_1_TRUE 0x0: SPARE_1_FALSE
0	SPARE_0	disable_ps_timeout 1=pulse skip timeout feature is disabled, 0=pulse skip timeout feature is enabled 0x1: SPARE_0_TRUE 0x0: SPARE_0_FALSE
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# 45 Ultbuck\_hc\_ps\_dig Registers

# 0x00011800 S2\_PS\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### S2\_PS\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	Indicates a change in the HW which is not intended to impact SW compatibility.

#### 0x00011801 S2\_PS\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### S2\_PS\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	Indicates a change in the HW which is not intended to impact SW compatibility.

#### 0x00011802 S2\_PS\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### S2\_PS\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	Indicates expanded functionality. Minor version adds functionality while being backward compatibility for existing features.

# 0x00011803 S2\_PS\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### S2 PS REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	Indicates different interface version. Major version changes are not backward compatible. There will be a new Programming Guide document per major revision.

# 0x00011804 S2\_PS\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x22

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### S2\_PS\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	SMPS
		0x16: SMPS

ONN

#### 0x00011805 S2\_PS\_PERPH\_SUBTYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x06

**Reset Name:** N/A

Peripheral SubType

#### S2\_PS\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	1 PS_LV2p5A: ultbuck power stage
		2 PS_LV3p0A: ultbuck power stage
		3 PS_LV1p8A: ultbuck power stage
	25	4 PS_MV1p5A: ultbuck power stage
	9 01° 01°	5 PS_MV2p5A: ultbuck power stage
	C. Capilles	6 PS2_LV3p0A: ultbuck power stage
	O'TO ME	7 PS2_MV2p5A: ultbuck power stage
	25	0x1: PS_LV2P5A
	V	0x2: PS_LV3P0A
		0x3: PS_LV1P8A
		0x4: PS_MV1P5A
		0x5: PS_MV2P5A
		0x6: PS2_LV3P0A
		0x7: PS2_MV2P5A

#### 0x00011810 S2\_PS\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

Interrupt Real Time Status Bits

#### S2\_PS\_INT\_RT\_STS

Bits	Name	Description
1	HIGH_CURRENT_INT2	Buck current exceeds set level 2 0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	Buck current exceeds set level 1 0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### S2\_PS\_INT\_SET\_TYPE

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 0x00011812 S2\_PS\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

# S2\_PS\_INT\_POLARITY\_HIGH

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 0x00011813 S2\_PS\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### S2\_PS\_INT\_POLARITY\_LOW

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

# 0x00011814 S2\_PS\_INT\_LATCHED\_CLR

**Type:** W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### S2\_PS\_INT\_LATCHED\_CLR

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 0x00011815 S2\_PS\_INT\_EN\_SET

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### S2\_PS\_INT\_EN\_SET

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE
		0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE
		0x1: HIGH_CURRENT_INT1_TRUE

## 0x00011816 S2\_PS\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### S2\_PS\_INT\_EN\_CLR

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 0x00011818 S2\_PS\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### S2\_PS\_INT\_LATCHED\_STS

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

# 0x00011819 S2\_PS\_INT\_PENDING\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### S2\_PS\_INT\_PENDING\_STS

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE
	27 118	0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE
	201, Che	0x1: HIGH_CURRENT_INT1_TRUE

# 0x0001181A S2\_PS\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### S2\_PS\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: INT_MID_FALSE
		0x1: INT_MID_TRUE

#### 0x0001181B S2\_PS\_INT\_PRIORITY

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### S2\_PS\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	SR=0 A=1
		0x0: INT_PRIORITY_FALSE
		0x1: INT_PRIORITY_TRUE

# 0x0001184A S2\_PS\_PWM\_CURRENT\_LIM\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0xB4

Reset Name: PERPH RB

#### S2\_PS\_PWM\_CURRENT\_LIM\_CTL

Bits	Name	Description
7	CURRENT_LIM_EN	0 = disable 1 = enable 0x0: CURRENT_LIM_EN_FALSE 0x1: CURRENT_LIM_EN_TRUE
5:3	CURRENT_LIM_AUTOINT_ SEL	These 3 bits are used to control the intermediate (hot PFM), current limit threshold whenever there is a mode transition between PFM and PWM mode under Auto-mode operation.  Iplimit threshold depends on selected current rating of the power stage:  HC (PS_LV2P5A, PS_LV3P0A, PS_MV2P5A, PS2_LV3P0A, PS2_MV2P5A)> Iplimit = 4400 mA - m*530 mA  LC (PS_LV1P8A, PS_MV1P5A)> Iplimit = 2700 mA - m*320 mA where m is the bit value of bit<5:3>  Note: The preset value of these bits is set to around 1A. The final values are device specific and listed in the device SBI table.  0x0: CURRENT_LIM_AUTOINT_SEL_LC_2700MA_HC_4400MA 0x1: CURRENT_LIM_AUTOINT_SEL_LC_2380MA_HC_3870MA 0x2: CURRENT_LIM_AUTOINT_SEL_LC_2060MA_HC_3340MA 0x3: CURRENT_LIM_AUTOINT_SEL_LC_1740MA_HC_2810MA 0x4: CURRENT_LIM_AUTOINT_SEL_LC_1740MA_HC_2280MA 0x5: CURRENT_LIM_AUTOINT_SEL_LC_1100MA_HC_2280MA 0x6: CURRENT_LIM_AUTOINT_SEL_LC_1100MA_HC_1750MA 0x6: CURRENT_LIM_AUTOINT_SEL_LC_780MA_HC_1220MA 0x7: CURRENT_LIM_AUTOINT_SEL_LC_780MA_HC_1220MA

#### S2\_PS\_PWM\_CURRENT\_LIM\_CTL (cont.)

Bits	Name	Description
2:0	CURRENT_LIM_PWM_SEL	These 3 bits are for current limit threshold programming when operating in PWM mode.
		Iplimit threshold depends on selected current rating of the power stage:
		HC (PS_LV2P5A, PS_LV3P0A, PS_MV2P5A, PS2_LV3P0A, PS2_MV2P5A)> Iplimit = 4400 mA - m*530 mA
		LC (PS_LV1P8A, PS_MV1P5A)> Iplimit = 2700 mA - m*320 mA
		where m is the bit value of bit<2:0>
		Note: The preset value of these bits is set by using Trim. Please refer to IPLIM_TRIM_OPT and Recommended defaults; however, the final values are device specific and listed in the
		device SBI table.
		0x0: CURRENT_LIM_PWM_SEL_LC_2700MA_HC_4400MA
		0x1: CURRENT_LIM_PWM_SEL_LC_2380MA_HC_3870MA
		0x2: CURRENT_LIM_PWM_SEL_LC_2060MA_HC_3340MA
		0x3: CURRENT_LIM_PWM_SEL_LC_1740MA_HC_2810MA
		0x4: CURRENT_LIM_PWM_SEL_LC_1420MA_HC_2280MA
		0x5: CURRENT_LIM_PWM_SEL_LC_1100MA_HC_1750MA
		0x6: CURRENT_LIM_PWM_SEL_LC_780MA_HC_1220MA
		0x7: CURRENT_LIM_PWM_SEL_LC_460MA_HC_690MA

# 0x0001184B S2\_PS\_PFM\_CURRENT\_LIM\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x84

Reset Name: PERPH RB

#### S2\_PS\_PFM\_CURRENT\_LIM\_CTL

Bits	Name	Description
7	CURRENT_LIM_EN	0 = disable
		1 = enable
		0x0: CURRENT_LIM_EN_FALSE
		0x1: CURRENT_LIM_EN_TRUE

#### S2\_PS\_PFM\_CURRENT\_LIM\_CTL (cont.)

Bits	Name	Description
2:0	CURRENT_LIM_SEL	Iplimit_sel<2:0> for current limit threshold programming when operating in PFM mode.
		Iplimit = 800 mA - m * 100 mA
		where m is the bit value of iplimit_sel<2:0>
		Note: The preset value and the final values of these bits are device specific and listed in the device SBI table.
		0x0: CURRENT_LIM_SEL_800MA
		0x1: CURRENT_LIM_SEL_700MA
		0x2: CURRENT_LIM_SEL_600MA
		0x3: CURRENT_LIM_SEL_500MA
		0x4: CURRENT_LIM_SEL_400MA
		0x5: CURRENT_LIM_SEL_300MA
		0x6: CURRENT_LIM_SEL_200MA
		0x7: CURRENT_LIM_SEL_100MA

#### 0x00011880 S2\_PS\_HCINT\_EN

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

# S2\_PS\_HCINT\_EN

Bits	Name	Description
7	HCINT_EN	0 = INT disable
		1 = INT enable
		0x0: INT_DISABLE
		0x1: INT_ENABLE

# 0x00011881 S2\_PS\_HCINT\_CONTROL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

# S2\_PS\_HCINT\_CONTROL

Bits	Name	Description
5	SET_WINDOW_WIDTH	This bit controls the deglitch window to set interrupt based on no. of cycles of 32KHz clock 0 = 2cycles to set 1 = 16cycles to set 0x0: CYCLES2 0x1: CYCLES16
4	RESET_WINDOW_WIDTH	This bit controls the deglitch window to reset interrupt based on no. of cycles of 32KHz clock 0 = 2cycles to reset 1 = 16cycles to reset 0x0: CYCLESRESET2 0x1: CYCLESRESET16
3:2	INT2_CUR_THRESHOLD	rated current - 10%*(m+1) 0x0: RATED_CURRENT_90PCT 0x1: RATED_CURRENT_80PCT 0x2: RATED_CURRENT_70PCT 0x3: RATED_CURRENT_60PCT
1:0	INT1_CUR_THRESHOLD	rated current - 10%*(m+3) 0x0: RATED_CURRENT_70PCT 0x1: RATED_CURRENT_60PCT 0x2: RATED_CURRENT_50PCT 0x3: RATED_CURRENT_40PCT

# 46 Bclk\_gen\_clk Registers

#### 0x00011900 S2\_FREQ\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

#### S2\_FREQ\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

#### 

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: N/A

HW Version Register [15:8]

#### S2\_FREQ\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00011904 S2\_FREQ\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x1D

Reset Name: N/A

Peripheral Type

#### S2\_FREQ\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	BCLK GEN

#### 0x00011905 S2\_FREQ\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x19

Reset Name: N/A

Peripheral SubType

## S2\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	BCLK GEN CLK

# 0x00011946 S2\_FREQ\_CLK\_ENABLE

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

#### S2\_FREQ\_CLK\_ENABLE

Bits	Name	Description
7	EN_CLK_INT	0 = do not force the clock on
		1 = enable the clock
		0x0: FORCE_EN_DISABLED
		0x1: FORCE_EN_ENABLED

#### S2\_FREQ\_CLK\_ENABLE (cont.)

Bits	Name	Description
0	FOLLOW_CLK_SX_REQ	0 = ignore smps_clk_req <x></x>
		1 = clock is enabled when the clocks request is high smps_clk_req <x>='1'</x>
		0x0: FALLOW_CLK_REQ_DISABLED
		0x1: FALLOW_CLK_REQ_ENABLED

# 0x00011950 S2\_FREQ\_CLK\_DIV

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x05

Reset Name: PERPH\_RB

PMIC LOCKED=SEC ACCESS, PMIC GANGED

# S2\_FREQ\_CLK\_DIV

Bits	Name	Description
3:0	CLK_DIV	clock_ frequency = 19.2MHz / (CLK_DIV + 1)
		FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz
	0,100	HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz
	o dille	CLK_DIV = 0 is not supported, it will generate 9.6 MHz
	750 110	0x0: FREQ_9M6HZ_0
	2018-24 Chillip	0x1: FREQ_9M6HZ
	1	0x2: FREQ_6M4HZ
		0x3: FREQ_4M8HZ
		0x4: FREQ_3M8HZ
		0x5: FREQ_3M2HZ
		0x6: FREQ_2M7HZ
		0x7: FREQ_2M4HZ
		0x8: FREQ_2M1HZ
		0x9: FREQ_1M9HZ
		0xA: FREQ_1M7HZ
		0xB: FREQ_1M6HZ
		0xC: FREQ_1M5HZ
		0xD: FREQ_1M4HZ
		0xE: FREQ_1M3HZ
		0xF: FREQ_1M2HZ

#### 0x00011951 S2\_FREQ\_CLK\_PHASE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x0F

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S2\_FREQ\_CLK\_PHASE

Bits	Name	Description
3:0	CLK_PHASE	Distributed clock phase select:
		clock phase delay = clock period * (CLK_PHASE / 16)

# 0x000119C0 S2\_FREQ\_GANG\_CTL1

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S2\_FREQ\_GANG\_CTL1

Bits	Name	Description
7:0	GANG_LEADER_PID	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

# 0x000119C1 S2\_FREQ\_GANG\_CTL2

Type: RW

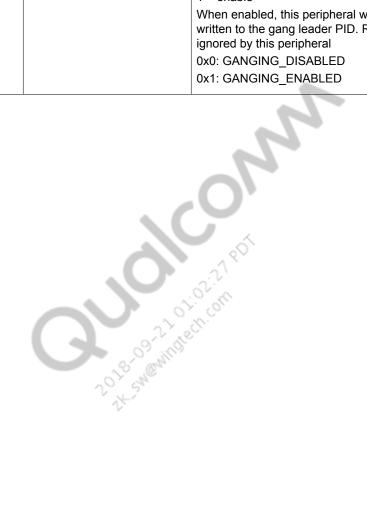
Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

#### S2\_FREQ\_GANG\_CTL2

Bits	Name	Description
7	GANG_EN	0 = disable
		1 = enable
		When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral
		0x0: GANGING_DISABLED
		0x1: GANGING_ENABLED



# 47 Hfbuck2\_ctrl Registers

#### 0x00011A00 S3\_CTRL\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### S3\_CTRL\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	Indicates a change in the HW which is not intended to impact SW compatibility.

#### 0x00011A01 S3\_CTRL\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x03

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### S3\_CTRL\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	Indicates a change in the HW which is not intended to impact SW compatibility.

# 0x00011A02 S3\_CTRL\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [23:16]

#### S3\_CTRL\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	Indicates expanded functionality. Minor version adds functionality while being backward compatibility for existing features.

# 0x00011A03 S3\_CTRL\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x03

Reset Name: N/A

HW Version Register [31:24]

#### S3 CTRL REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	Indicates different interface version. Major version changes are not backward compatible. There will be a new Programming Guide document per major revision

#### 0x00011A04 S3\_CTRL\_PERPH\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x03

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### S3\_CTRL\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	SMPS
		0x3: SMPS

#### 0x00011A05 S3\_CTRL\_PERPH\_SUBTYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: N/A

Peripheral SubType

#### S3\_CTRL\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	HFBUCK2 General Purpose Controller
		0x8: GENERAL_PURPOSE_CONTROLLER

#### 0x00011A08 S3\_CTRL\_STATUS

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: N/A

Status Registers

#### S3\_CTRL\_STATUS

Bits	Name	Description
7	VREG_OK	0 = VREG output voltage is below VREG_OK threshold,,,,
		1 = VREG output voltage is above VREG_OK threshold
		0x0: VREG_OK_FALSE
		0x1: VREG_OK_TRUE
5	ILS	Illegal Limit Stop. This is triggered when UL_Voltage < LL_Voltage.
		For more details look at HW/SW document
		0x0: ILEGAL_LIMIT_STOP_FALSE
		0x1: ILEGAL_LIMIT_STOP_TRUE
4	UL_VOLTAGE	Last voltage set was above UL_Voltage
		0x0: UL_INT_FALSE
		0x1: UL_INT_TRUE

#### S3\_CTRL\_STATUS (cont.)

Bits	Name	Description
3	LL_VOLTAGE	Last voltage set was below LL_Voltage
		0x0: LL_INT_FALSE
		0x1: LL_INT_TRUE
2	PS_TRUE	0 = buck is not pulse skipping,,,,
		1 = buck is pulse skipping
		0x0: PS_FALSE
		0x1: PS_TRUE
1	NPM_TRUE	1 = VREG_OK and BUCK is in NPM
		0x0: NPM_VREGOK_FALSE
		0x1: NPM_VREGOK_TRUE
0	STEPPER_DONE	1 = stepper is done
		0x0: STEPPER_DONE_FALSE
		0x1: STEPPER_DONE_TRUE

# 0x00011A10 S3\_CTRL\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

Interrupt Real Time Status Bits

#### S3\_CTRL\_INT\_RT\_STS

Bits	Name	Description
1	VREG_FAULT_INT	OCP event has occurred 0x0: VREG FAULT INT FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	Regulator has been successfully enabled 0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

#### 0x00011A11 S3\_CTRL\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### S3\_CTRL\_INT\_SET\_TYPE

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

# 0x00011A12 S3\_CTRL\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### S3\_CTRL\_INT\_POLARITY\_HIGH

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
	027	0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
	201, CME	0x1: VREG_OK_INT_TRUE

# 0x00011A13 S3\_CTRL\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### S3\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

#### 0x00011A14 S3\_CTRL\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### S3\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

#### 0x00011A15 S3\_CTRL\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### S3 CTRL INT EN SET

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

# 0x00011A16 S3\_CTRL\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### S3\_CTRL\_INT\_EN\_CLR

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

# 0x00011A18 S3 CTRL INT LATCHED STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### S3 CTRL INT LATCHED STS

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

# 0x00011A19 S3\_CTRL\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### S3\_CTRL\_INT\_PENDING\_STS

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

#### 0x00011A1A S3\_CTRL\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

Selects the MID that will receive the interrupt

#### S3\_CTRL\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: INT_MID_FALSE
	27,10	0x1: INT_MID_TRUE

# 0x00011A1B S3\_CTRL\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### S3\_CTRL\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	SR=0 A=1
		0x0: INT_PRIORITY_FALSE
		0x1: INT_PRIORITY_TRUE

#### 0x00011A40 S3\_CTRL\_VOLTAGE\_CTL1

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

# PMIC\_LATCHED\_WRITE=VOLTAGE\_CTL2

#### S3\_CTRL\_VOLTAGE\_CTL1

Bits	Name	Description
0	RANGE	0 : 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV)
		1 : 1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV)
		0x0: RANGE_HV_FALSE
		0x1: RANGE_HV_TRUE

# 0x00011A41 S3\_CTRL\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x49

Reset Name: PERPH\_RB

#### S3\_CTRL\_VOLTAGE\_CTL2

Bits	Name		Description
6:0	V_SET	27.0	Voltage = Vmin + VSET*(Vstep)

# 0x00011A44 S3\_CTRL\_PFM\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x85

Reset Name: PERPH\_RB

#### S3\_CTRL\_PFM\_CTL

Bits	Name	Description
7	PFM_VOLT_CTL	1=PFM voltage 1% over PWM voltage; 0=PFM voltage same as PWM voltage
		0x0: PFM_VOLT_BOOST_FALSE
		0x1: PFM_VOLT_BOOST_TRUE
6	PFM_IBOOST	1=Boost PFM Comparator bias current to 2uA; 0=bias current is 0.5uA 0x0: PFM_IBOOST_FALSE 0x1: PFM_IBOOST_TRUE

#### S3\_CTRL\_PFM\_CTL (cont.)

Bits	Name	Description
5	PFM_TYPE_I	1= Legacy PFM mode
		0=Advanced PFM mode
		0x0: PFM_ADVANCED
		0x1: PFM_LEGACY
4	RESERVED	
3	RESERVED	
2	PFM_IPLIM_CTRL	0:Vdip_comp does not control IPLIM
		1:Set IPLIM same as PWM mode when Vdip_comp=1
		0x0: PFM_IPLIM_CTRL_FALSE
		0x1: PFM_IPLIM_CTRL_TRUE
1:0	PFM_IPLIM_DLY	00:Delay=75ns
		01:Delay=150ns
		10:Delay=300ns
		11:Delay=600ns
		0x0: PFM_IPLIM_CTRL_75NS
		0x1: PFM_IPLIMI_CTRL_150NS
	. ( )	0x2: PFM_IPLIM_CTRL_300NS
		0x3: PFM_IPLIM_CTRL_600NS

# 0x00011A45 S3\_CTRL\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK

**Reset State:** 0x80

Reset Name: PERPH\_RB

Define Buck Mode Transitions

#### S3\_CTRL\_MODE\_CTL

Bits	Name	Description
7	PWM	Force PWM
		0x0: PWM_NO_FORCE
		0x1: PWM_FORCE
6	AUTO_MODE	1=Automatically enter NPM based on current
		0x0: AUTO_FALSE
		0x1: AUTO_TRUE
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B) = '1'
		0x0: FOLLOW_PMIC_AWAKE_FALSE
		0x1: FOLLOW_PMIC_AWAKE_TRUE

#### S3\_CTRL\_MODE\_CTL (cont.)

Bits	Name	Description
3	FOLLOW_HWEN3	1' BUCK is in NPM when HWEN3 ='1', '0'= ignore HWEN3
		0x0: FOLLOW_HWEN3_FALSE
		0x1: FOLLOW_HWEN3_TRUE
2	FOLLOW_HWEN2	1' BUCK is in NPM when HWEN2 ='1', '0'= ignore HWEN2
		0x0: FOLLOW_HWEN2_FALSE
		0x1: FOLLOW_HWEN2_TRUE
1	FOLLOW_HWEN1	1' BUCK is in NPM when HWEN1 ='1', '0'= ignore HWEN1
		0x0: FOLLOW_HWEN1_FALSE
		0x1: FOLLOW_HWEN1_TRUE
0	FOLLOW_HWEN0	1' BUCK is in NPM when HWEN0 ='1', '0'= ignore HWEN0
		0x0: FOLLOW_HWEN0_FALSE
		0x1: FOLLOW_HWEN0_TRUE

# 0x00011A46 S3\_CTRL\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

# S3\_CTRL\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	1' = Enable the BUCK, '0' = do not force BUCK on 0x0: BUCK_ENABLE_FALSE 0x1: BUCK_ENABLE_TRUE
3	FOLLOW_HWEN3	1' BUCK is enabled when HWEN3 ='1', '0'= ignore HWEN3 0x0: FOLLOW_HWEN3_FALSE 0x1: FOLLOW_HWEN3_TRUE
2	FOLLOW_HWEN2	1' BUCK is enabled when HWEN2 ='1', '0'= ignore HWEN2 0x0: FOLLOW_HWEN2_FALSE 0x1: FOLLOW_HWEN2_TRUE
1	FOLLOW_HWEN1	1' BUCK is enabled when HWEN1 ='1', '0'= ignore HWEN1 0x0: FOLLOW_HWEN1_FALSE 0x1: FOLLOW_HWEN1_TRUE
0	FOLLOW_HWEN0	1' BUCK is enabled when HWEN0 ='1', '0'= ignore HWEN0 0x0: FOLLOW_HWEN0_FALSE 0x1: FOLLOW_HWEN0_TRUE

## 0x00011A48 S3\_CTRL\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH RB

#### S3\_CTRL\_PD\_CTL

Bits	Name	Description
7	PD_EN	1' = Enable the pull-down when the regulator is disabled, '0' = pull-down is always disabled. Preset by trim register CTL_TRIM4
		0x0: PD_ENABLE_FALSE
		0x1: PD_ENABLE_TRUE

# 0x00011A68 S3\_CTRL\_UL\_LL\_CTRL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

## S3\_CTRL\_UL\_LL\_CTRL

Bits	Name	Description
7	UL_INT_EN	0 = Disable upper limit stop 1 = Enable upper limit stop 0x0: UL_INT_EN_FALSE 0x1: UL_INT_EN_TRUE
6	LL_INT_EN	0 = Disable lower limit stop 1 = Enable lower limit stop 0x0: LL_INT_EN_FALSE 0x1: LL_INT_EN_TRUE

#### 0x00011A69 S3\_CTRL\_UL\_VOLTAGE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x7F

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S3\_CTRL\_UL\_VOLTAGE

Bits	Name	Description
6:0	V_SET	Sets upper limit for the allowed output voltage range if LIMIT_LO_EN is asserted.
		For EXT_RANGE = 0:
		VLIMIT_STOP_LO = 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV), where m = <6:0>
		For EXT_RANGE = 1:
		VLIMIT_STOP_LO =1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV), where m = <6:0>

# 0x00011A6B S3\_CTRL\_LL\_VOLTAGE

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S3\_CTRL\_LL\_VOLTAGE

Bits	Name	Description
6:0	V_SET	Sets lower limit for the allowed output voltage range if LIMIT_LO_EN is asserted.
		For EXT_RANGE = 0:
		VLIMIT_STOP_LO = 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV), where m = <6:0>
		For EXT_RANGE = 1:
		VLIMIT_STOP_LO =1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV), where m = <6:0>

#### 0x00011A7A S3\_CTRL\_CTLR\_MISC

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

#### S3\_CTRL\_CTLR\_MISC

Bits	Name	Description
7	SPARE_7	
6	SPARE_6	

#### S3\_CTRL\_CTLR\_MISC (cont.)

Bits	Name	Description
5	SPARE_5	
4	SPARE_4	
3	SPARE_3	
2	SPARE_2	1=OCP is reset when perph_en, en_ext, and when are all low, 0=OCP is reset by perph_en rising edge 0x1: SPARE_2_TRUE 0x0: SPARE_2_FALSE
1	SPARE_1	1=enable buck, 0=normal mode 0x1: SPARE_1_TRUE 0x0: SPARE_1_FALSE
0	SPARE_0	disable_ps_timeout 1=pulse skip timeout feature is disabled, 0=pulse skip timeout feature is enabled 0x1: SPARE_0_TRUE 0x0: SPARE_0_FALSE
2018-09-21 OILOUR 2018-09-21 PDT		

# 48 Hfbuck2\_ps Registers

#### 0x00011B00 S3\_PS\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

HW Version Register [7:0]

PMIC CONSTANT

#### S3\_PS\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	Indicates a change in the HW which is not intended to impact SW compatibility.

#### 0x00011B01 S3\_PS\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

HW Version Register [15:8]

PMIC CONSTANT

#### S3\_PS\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	Indicates a change in the HW which is not intended to impact SW compatibility.

#### 0x00011B02 S3\_PS\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

HW Version Register [23:16]

#### S3\_PS\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	Indicates expanded functionality. Minor version adds functionality while being backward compatibility for existing features.

#### 0x00011B03 S3\_PS\_REVISION4

#### S3\_PS\_REVISION4

S3_P	S3_PS_REVISION4			
Type: R Clock: PBUS_WRCLK Reset State: 0x01				
HW Version Register [31:24]				
S3_PS	S3_PS_REVISION4			
Bits	Name	Description		
7:0	ANA_MAJOR	Indicates different interface version. Major version changes are not backward compatible. There will be a new Programming Guide document per major revision.		

#### 0x00011B04 S3\_PS\_PERPH\_TYPE

Type: R

Clock: PBUS WRCLK Reset State: 0x03

Peripheral Type

PMIC CONSTANT

#### S3\_PS\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	SMPS 0x3: SMPS

# 0x00011B05 S3\_PS\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x03

Peripheral SubType

#### S3\_PS\_PERPH\_SUBTYPE

В	Bits	Name	Description
7	7:0	SUBTYPE	1 1X HFBUCK2 Power Stage 2 2X HFBUCK2 Power Stage (up to 1.5A)
			3 3X HFBUCK2 Power Stage (up to 2.5A)
			0x1: POWERSTAGE_1X
			0x2: POWERSTAGE_2X 0x3: POWERSTAGE_3X
		2018-09-21-018 2018-54@minds	CO.27 RDT

# 49 Bclk\_gen\_clk Registers

#### 0x00011C00 S3\_FREQ\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

#### S3\_FREQ\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

#### 0x00011C01 S3\_FREQ\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: N/A

HW Version Register [15:8]

#### S3\_FREQ\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00011C04 S3\_FREQ\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x1D

Reset Name: N/A

Peripheral Type

#### S3\_FREQ\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	BCLK GEN

#### 0x00011C05 S3\_FREQ\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x19 Reset Name: N/A

Peripheral SubType

#### S3\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	BCLK GEN CLK

# 0x00011C46 S3\_FREQ\_CLK\_ENABLE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH\_RB

PMIC\_LOCKED=SEC\_ACCESS

#### S3\_FREQ\_CLK\_ENABLE

Bits	Name	Description
7	EN_CLK_INT	0 = do not force the clock on
		1 = enable the clock
		0x0: FORCE_EN_DISABLED
		0x1: FORCE_EN_ENABLED

#### S3\_FREQ\_CLK\_ENABLE (cont.)

Bits	Name	Description
0	FOLLOW_CLK_SX_REQ	0 = ignore smps_clk_req <x></x>
		1 = clock is enabled when the clocks request is high smps_clk_req <x>='1'</x>
		0x0: FALLOW_CLK_REQ_DISABLED
		0x1: FALLOW_CLK_REQ_ENABLED

# 0x00011C50 S3\_FREQ\_CLK\_DIV

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x0B

Reset Name: PERPH\_RB

PMIC LOCKED=SEC ACCESS, PMIC GANGED

# S3\_FREQ\_CLK\_DIV

Bits	Name	Description
3:0	CLK_DIV	clock_ frequency = 19.2MHz / (CLK_DIV + 1)
		FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz
	0,1 1,5	HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz
	.O. ville	CLK_DIV = 0 is not supported, it will generate 9.6 MHz
	2018. 24 Chillip	0x0: FREQ_9M6HZ_0
	2.5	0x1: FREQ_9M6HZ
	1	0x2: FREQ_6M4HZ
		0x3: FREQ_4M8HZ
		0x4: FREQ_3M8HZ
		0x5: FREQ_3M2HZ
		0x6: FREQ_2M7HZ
		0x7: FREQ_2M4HZ
		0x8: FREQ_2M1HZ
		0x9: FREQ_1M9HZ
		0xA: FREQ_1M7HZ
		0xB: FREQ_1M6HZ
		0xC: FREQ_1M5HZ
		0xD: FREQ_1M4HZ
		0xE: FREQ_1M3HZ
		0xF: FREQ_1M2HZ

#### 0x00011C51 S3\_FREQ\_CLK\_PHASE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x06

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S3\_FREQ\_CLK\_PHASE

Bits	Name	Description
3:0	CLK_PHASE	Distributed clock phase select:
		clock phase delay = clock period * (CLK_PHASE / 16)

# 0x00011CC0 S3\_FREQ\_GANG\_CTL1

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S3\_FREQ\_GANG\_CTL1

Bits	Name	Description
7:0	GANG_LEADER_PID	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

#### 0x00011CC1 S3\_FREQ\_GANG\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

#### S3\_FREQ\_GANG\_CTL2

Bits	Name	Description
7	GANG_EN	0 = disable
		1 = enable
		When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral
		0x0: GANGING_DISABLED
		0x1: GANGING_ENABLED



# 50 Hfbuck2\_ctrl Registers

#### 0x00011D00 S4\_CTRL\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### S4\_CTRL\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	Indicates a change in the HW which is not intended to impact SW compatibility.

#### 0x00011D01 S4\_CTRL\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x03

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### S4\_CTRL\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	Indicates a change in the HW which is not intended to impact SW compatibility.

#### 0x00011D02 S4\_CTRL\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [23:16]

#### S4\_CTRL\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	Indicates expanded functionality. Minor version adds functionality while being backward compatibility for existing features.

## 0x00011D03 S4\_CTRL\_REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x03

Reset Name: N/A

HW Version Register [31:24]

#### **S4 CTRL REVISION4**

Bits	Name	Description
7:0	ANA_MAJOR	Indicates different interface version. Major version changes are not backward compatible. There will be a new Programming Guide document per major revision

#### 0x00011D04 S4\_CTRL\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x03

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### S4\_CTRL\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	SMPS
		0x3: SMPS

#### 0x00011D05 S4\_CTRL\_PERPH\_SUBTYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x08

**Reset Name:** N/A

Peripheral SubType

#### S4\_CTRL\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	HFBUCK2 General Purpose Controller
		0x8: GENERAL_PURPOSE_CONTROLLER

#### 0x00011D08 S4\_CTRL\_STATUS

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: N/A

Status Registers

#### S4\_CTRL\_STATUS

Bits	Name	Description
7	VREG_OK	0 = VREG output voltage is below VREG_OK threshold,,,,
		1 = VREG output voltage is above VREG_OK threshold
		0x0: VREG_OK_FALSE
		0x1: VREG_OK_TRUE
5	ILS	Illegal Limit Stop. This is triggered when UL_Voltage < LL_Voltage.
		For more details look at HW/SW document
		0x0: ILEGAL_LIMIT_STOP_FALSE
		0x1: ILEGAL_LIMIT_STOP_TRUE
4	UL_VOLTAGE	Last voltage set was above UL_Voltage
		0x0: UL_INT_FALSE
		0x1: UL_INT_TRUE

#### S4\_CTRL\_STATUS (cont.)

Bits	Name	Description
3	LL_VOLTAGE	Last voltage set was below LL_Voltage
		0x0: LL_INT_FALSE
		0x1: LL_INT_TRUE
2	PS_TRUE	0 = buck is not pulse skipping,,,,
		1 = buck is pulse skipping
		0x0: PS_FALSE
		0x1: PS_TRUE
1	NPM_TRUE	1 = VREG_OK and BUCK is in NPM
		0x0: NPM_VREGOK_FALSE
		0x1: NPM_VREGOK_TRUE
0	STEPPER_DONE	1 = stepper is done
		0x0: STEPPER_DONE_FALSE
		0x1: STEPPER_DONE_TRUE

# 0x00011D10 S4\_CTRL\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

Interrupt Real Time Status Bits

#### S4\_CTRL\_INT\_RT\_STS

Bits	Name	Description
1	VREG_FAULT_INT	OCP event has occurred 0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	Regulator has been successfully enabled 0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

#### 0x00011D11 S4\_CTRL\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### S4\_CTRL\_INT\_SET\_TYPE

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

## 0x00011D12 S4\_CTRL\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### S4\_CTRL\_INT\_POLARITY\_HIGH

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
	27 118	0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
	2010 CHE	0x1: VREG_OK_INT_TRUE

## 0x00011D13 S4\_CTRL\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### S4\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

#### 0x00011D14 S4\_CTRL\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### S4\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

#### 0x00011D15 S4\_CTRL\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### S4 CTRL INT EN SET

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE 0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE 0x1: VREG_OK_INT_TRUE

#### 0x00011D16 S4\_CTRL\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### S4\_CTRL\_INT\_EN\_CLR

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

## 0x00011D18 S4 CTRL INT LATCHED STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### S4 CTRL INT LATCHED STS

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

## 0x00011D19 S4\_CTRL\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### S4\_CTRL\_INT\_PENDING\_STS

Bits	Name	Description
1	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALSE
		0x1: VREG_FAULT_INT_TRUE
0	VREG_OK_INT	0x0: VREG_OK_INT_FALSE
		0x1: VREG_OK_INT_TRUE

#### 0x00011D1A S4\_CTRL\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### S4\_CTRL\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: INT_MID_FALSE
	02 118	0x1: INT_MID_TRUE

#### 0x00011D1B S4\_CTRL\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### S4\_CTRL\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	SR=0 A=1
		0x0: INT_PRIORITY_FALSE
		0x1: INT_PRIORITY_TRUE

#### 0x00011D40 S4\_CTRL\_VOLTAGE\_CTL1

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH\_RB

# PMIC\_LATCHED\_WRITE=VOLTAGE\_CTL2

#### S4\_CTRL\_VOLTAGE\_CTL1

Bits	Name	Description
0	RANGE	0 : 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV)
		1 : 1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV)
		0x0: RANGE_HV_FALSE
		0x1: RANGE_HV_TRUE

# 0x00011D41 S4\_CTRL\_VOLTAGE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x14

Reset Name: PERPH\_RB

#### S4\_CTRL\_VOLTAGE\_CTL2

Bits	Na	me	Description
6:0	V_SET	27.0	Voltage = Vmin + VSET*(Vstep)

## 0x00011D44 S4\_CTRL\_PFM\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x85

Reset Name: PERPH\_RB

#### S4\_CTRL\_PFM\_CTL

Bits	Name	Description
7	PFM_VOLT_CTL	1=PFM voltage 1% over PWM voltage; 0=PFM voltage same as PWM voltage
		0x0: PFM_VOLT_BOOST_FALSE
		0x1: PFM_VOLT_BOOST_TRUE
6	PFM_IBOOST	1=Boost PFM Comparator bias current to 2uA; 0=bias current is 0.5uA 0x0: PFM_IBOOST_FALSE 0x1: PFM_IBOOST_TRUE

#### S4\_CTRL\_PFM\_CTL (cont.)

Bits	Name	Description
5	PFM_TYPE_I	1= Legacy PFM mode 0=Advanced PFM mode
		0x0: PFM_ADVANCED
		0x1: PFM_LEGACY
4	RESERVED	
3	RESERVED	
2	PFM_IPLIM_CTRL	0:Vdip_comp does not control IPLIM
		1:Set IPLIM same as PWM mode when Vdip_comp=1
		0x0: PFM_IPLIM_CTRL_FALSE
		0x1: PFM_IPLIM_CTRL_TRUE
1:0	PFM_IPLIM_DLY	00:Delay=75ns
		01:Delay=150ns
		10:Delay=300ns
		11:Delay=600ns
		0x0: PFM_IPLIM_CTRL_75NS
		0x1: PFM_IPLIMI_CTRL_150NS
		0x2: PFM_IPLIM_CTRL_300NS
		0x3: PFM_IPLIM_CTRL_600NS

# 0x00011D45 S4\_CTRL\_MODE\_CTL

Type: RW

Clock: PBUS WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

Define Buck Mode Transitions

#### S4\_CTRL\_MODE\_CTL

Bits	Name	Description
7	PWM	Force PWM
		0x0: PWM_NO_FORCE
		0x1: PWM_FORCE
6	AUTO_MODE	1=Automatically enter NPM based on current
		0x0: AUTO_FALSE
		0x1: AUTO_TRUE
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B) = '1'
		0x0: FOLLOW_PMIC_AWAKE_FALSE
		0x1: FOLLOW_PMIC_AWAKE_TRUE

#### S4\_CTRL\_MODE\_CTL (cont.)

Bits	Name	Description
3	FOLLOW_HWEN3	1' BUCK is in NPM when HWEN3 ='1', '0'= ignore HWEN3 0x0: FOLLOW_HWEN3_FALSE 0x1: FOLLOW_HWEN3_TRUE
2	FOLLOW_HWEN2	1' BUCK is in NPM when HWEN2 ='1', '0'= ignore HWEN2 0x0: FOLLOW_HWEN2_FALSE 0x1: FOLLOW_HWEN2_TRUE
1	FOLLOW_HWEN1	1' BUCK is in NPM when HWEN1 ='1', '0'= ignore HWEN1 0x0: FOLLOW_HWEN1_FALSE 0x1: FOLLOW_HWEN1_TRUE
0	FOLLOW_HWEN0	1' BUCK is in NPM when HWEN0 ='1', '0'= ignore HWEN0 0x0: FOLLOW_HWEN0_FALSE 0x1: FOLLOW_HWEN0_TRUE

# 0x00011D46 S4\_CTRL\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

# S4\_CTRL\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	1' = Enable the BUCK, '0' = do not force BUCK on 0x0: BUCK_ENABLE_FALSE 0x1: BUCK_ENABLE_TRUE
3	FOLLOW_HWEN3	1' BUCK is enabled when HWEN3 ='1', '0'= ignore HWEN3 0x0: FOLLOW_HWEN3_FALSE 0x1: FOLLOW_HWEN3_TRUE
2	FOLLOW_HWEN2	1' BUCK is enabled when HWEN2 ='1', '0'= ignore HWEN2 0x0: FOLLOW_HWEN2_FALSE 0x1: FOLLOW_HWEN2_TRUE
1	FOLLOW_HWEN1	1' BUCK is enabled when HWEN1 ='1', '0'= ignore HWEN1 0x0: FOLLOW_HWEN1_FALSE 0x1: FOLLOW_HWEN1_TRUE
0	FOLLOW_HWEN0	1' BUCK is enabled when HWEN0 ='1', '0'= ignore HWEN0 0x0: FOLLOW_HWEN0_FALSE 0x1: FOLLOW_HWEN0_TRUE

#### 0x00011D48 S4\_CTRL\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH RB

#### S4\_CTRL\_PD\_CTL

Bits	Name	Description
7	PD_EN	1' = Enable the pull-down when the regulator is disabled, '0' = pull-down is always disabled. Preset by trim register CTL_TRIM4
		0x0: PD_ENABLE_FALSE
		0x1: PD_ENABLE_TRUE

# 0x00011D68 S4\_CTRL\_UL\_LL\_CTRL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S4\_CTRL\_UL\_LL\_CTRL

Bits	Name	Description
7	UL_INT_EN	0 = Disable upper limit stop 1 = Enable upper limit stop 0x0: UL_INT_EN_FALSE 0x1: UL_INT_EN_TRUE
6	LL_INT_EN	0 = Disable lower limit stop 1 = Enable lower limit stop 0x0: LL_INT_EN_FALSE 0x1: LL_INT_EN_TRUE

#### 0x00011D69 S4\_CTRL\_UL\_VOLTAGE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x7F

Reset Name: PERPH\_RB

PMIC LOCKED=SEC ACCESS

#### S4\_CTRL\_UL\_VOLTAGE

Name	Description
V_SET	Sets upper limit for the allowed output voltage range if LIMIT_LO_EN is asserted.
	For EXT_RANGE = 0:
	VLIMIT_STOP_LO = 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV), where m = <6:0>
	For EXT_RANGE = 1:
	VLIMIT_STOP_LO =1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV), where m = <6:0>

# 0x00011D6B S4\_CTRL\_LL\_VOLTAGE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_LOCKED=SEC ACCESS

#### S4\_CTRL\_LL\_VOLTAGE

Bits	Name	Description
6:0	V_SET	Sets lower limit for the allowed output voltage range if LIMIT_LO_EN is asserted.
		For EXT_RANGE = 0:
		VLIMIT_STOP_LO = 0.375 to 1.5625 V at steps of 12.5 mV (Vmin = 0.375 V, Vstep = 12.5 mV), where m = <6:0>
		For EXT_RANGE = 1:
		VLIMIT_STOP_LO =1.550 to 3.1250 V at steps of 25.0 mV (Vmin = 1.550 V, Vstep = 25.0 mV), where m = <6:0>

#### 0x00011D7A S4\_CTRL\_CTLR\_MISC

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### S4\_CTRL\_CTLR\_MISC

Bits	Name	Description
7	SPARE_7	
6	SPARE_6	

#### S4\_CTRL\_CTLR\_MISC (cont.)

Bits	Name	Description
5	SPARE_5	
4	SPARE_4	
3	SPARE_3	
2	SPARE_2	1=OCP is reset when perph_en, en_ext, and when are all low, 0=OCP is reset by perph_en rising edge 0x1: SPARE_2_TRUE 0x0: SPARE_2_FALSE
1	SPARE_1	1=enable buck, 0=normal mode 0x1: SPARE_1_TRUE 0x0: SPARE_1_FALSE
0	SPARE_0	disable_ps_timeout 1=pulse skip timeout feature is disabled, 0=pulse skip timeout feature is enabled 0x1: SPARE_0_TRUE 0x0: SPARE_0_FALSE
2018-09-22-101-101R Delta-communications of the second sec		

# 51 Ultbuck\_hc\_ps\_dig Registers

#### 

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### S4\_PS\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	Indicates a change in the HW which is not intended to impact SW compatibility.

#### 

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### S4\_PS\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	Indicates a change in the HW which is not intended to impact SW compatibility.

#### 

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### S4\_PS\_REVISION3

	on
7:0 ANA_MINOR Indicates expanded functionality. Mir while being backward compatibility for	,

#### 

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

**Reset Name:** N/A

HW Version Register [31:24]

#### S4 PS REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	Indicates different interface version. Major version changes are not backward compatible. There will be a new Programming Guide document per major revision.

## 0x00011E04 S4\_PS\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x22

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### S4\_PS\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	SMPS 0x16: SMPS
		OXTO. GIVII G

ONN

#### 0x00011E05 S4\_PS\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x07

Reset Name: N/A

Peripheral SubType

#### S4\_PS\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	1 PS_LV2p5A: ultbuck power stage
		2 PS_LV3p0A: ultbuck power stage
		3 PS_LV1p8A: ultbuck power stage
	25	4 PS_MV1p5A: ultbuck power stage
	9 01° 01°	5 PS_MV2p5A: ultbuck power stage
	C. Capilles	6 PS2_LV3p0A: ultbuck power stage
	O'TO ME	7 PS2_MV2p5A: ultbuck power stage
	25	0x1: PS_LV2P5A
	V	0x2: PS_LV3P0A
		0x3: PS_LV1P8A
		0x4: PS_MV1P5A
		0x5: PS_MV2P5A
		0x6: PS2_LV3P0A
		0x7: PS2_MV2P5A

#### 

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

Interrupt Real Time Status Bits

#### S4\_PS\_INT\_RT\_STS

Bits	Name	Description
1	HIGH_CURRENT_INT2	Buck current exceeds set level 2 0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	Buck current exceeds set level 1 0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 0x00011E11 S4\_PS\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### S4\_PS\_INT\_SET\_TYPE

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 0x00011E12 S4\_PS\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

## S4\_PS\_INT\_POLARITY\_HIGH

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 0x00011E13 S4\_PS\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### S4\_PS\_INT\_POLARITY\_LOW

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

# 0x00011E14 S4\_PS\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### S4\_PS\_INT\_LATCHED\_CLR

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### S4\_PS\_INT\_EN\_SET

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE
		0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE
		0x1: HIGH_CURRENT_INT1_TRUE

#### 

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### S4\_PS\_INT\_EN\_CLR

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

#### 0x00011E18 S4\_PS\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### S4\_PS\_INT\_LATCHED\_STS

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE 0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE 0x1: HIGH_CURRENT_INT1_TRUE

## 0x00011E19 S4\_PS\_INT\_PENDING\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### S4\_PS\_INT\_PENDING\_STS

Bits	Name	Description
1	HIGH_CURRENT_INT2	0x0: HIGH_CURRENT_INT2_FALSE
	027	0x1: HIGH_CURRENT_INT2_TRUE
0	HIGH_CURRENT_INT1	0x0: HIGH_CURRENT_INT1_FALSE
	201, ENG.	0x1: HIGH_CURRENT_INT1_TRUE

## 0x00011E1A S4\_PS\_INT\_MID\_SEL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### S4\_PS\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x0: INT_MID_FALSE
		0x1: INT_MID_TRUE

#### 0x00011E1B S4\_PS\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### S4\_PS\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	SR=0 A=1
		0x0: INT_PRIORITY_FALSE
		0x1: INT_PRIORITY_TRUE

# 0x00011E4A S4\_PS\_PWM\_CURRENT\_LIM\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0xB4

Reset Name: PERPH RB

#### S4\_PS\_PWM\_CURRENT\_LIM\_CTL

Bits	Name	Description
7	CURRENT_LIM_EN	0 = disable 1 = enable 0x0: CURRENT_LIM_EN_FALSE 0x1: CURRENT_LIM_EN_TRUE
5:3	CURRENT_LIM_AUTOINT_ SEL	These 3 bits are used to control the intermediate (hot PFM), current limit threshold whenever there is a mode transition between PFM and PWM mode under Auto-mode operation.  Iplimit threshold depends on selected current rating of the power stage:  HC (PS_LV2P5A, PS_LV3P0A, PS_MV2P5A, PS2_LV3P0A, PS2_MV2P5A)> Iplimit = 4400 mA - m*530 mA  LC (PS_LV1P8A, PS_MV1P5A)> Iplimit = 2700 mA - m*320 mA where m is the bit value of bit<5:3>  Note: The preset value of these bits is set to around 1A. The final values are device specific and listed in the device SBI table.  0x0: CURRENT_LIM_AUTOINT_SEL_LC_2700MA_HC_4400MA 0x1: CURRENT_LIM_AUTOINT_SEL_LC_2380MA_HC_3870MA 0x2: CURRENT_LIM_AUTOINT_SEL_LC_2060MA_HC_3340MA 0x3: CURRENT_LIM_AUTOINT_SEL_LC_1740MA_HC_2810MA 0x4: CURRENT_LIM_AUTOINT_SEL_LC_1740MA_HC_2280MA 0x5: CURRENT_LIM_AUTOINT_SEL_LC_1100MA_HC_1750MA 0x6: CURRENT_LIM_AUTOINT_SEL_LC_1100MA_HC_1750MA 0x6: CURRENT_LIM_AUTOINT_SEL_LC_780MA_HC_1220MA 0x7: CURRENT_LIM_AUTOINT_SEL_LC_780MA_HC_1220MA

#### S4\_PS\_PWM\_CURRENT\_LIM\_CTL (cont.)

Bits	Name	Description
2:0	CURRENT_LIM_PWM_SEL	These 3 bits are for current limit threshold programming when operating in PWM mode.
		Iplimit threshold depends on selected current rating of the power stage:
		HC (PS_LV2P5A, PS_LV3P0A, PS_MV2P5A, PS2_LV3P0A, PS2_MV2P5A)> Iplimit = 4400 mA - m*530 mA
		LC (PS_LV1P8A, PS_MV1P5A)> Iplimit = 2700 mA - m*320 mA
		where m is the bit value of bit<2:0>
		Note: The preset value of these bits is set by using Trim. Please refer to IPLIM_TRIM_OPT and Recommended defaults; however, the final values are device specific and listed in the
		device SBI table.
		0x0: CURRENT_LIM_PWM_SEL_LC_2700MA_HC_4400MA
		0x1: CURRENT_LIM_PWM_SEL_LC_2380MA_HC_3870MA
		0x2: CURRENT_LIM_PWM_SEL_LC_2060MA_HC_3340MA
		0x3: CURRENT_LIM_PWM_SEL_LC_1740MA_HC_2810MA
		0x4: CURRENT_LIM_PWM_SEL_LC_1420MA_HC_2280MA
		0x5: CURRENT_LIM_PWM_SEL_LC_1100MA_HC_1750MA
		0x6: CURRENT_LIM_PWM_SEL_LC_780MA_HC_1220MA
		0x7: CURRENT_LIM_PWM_SEL_LC_460MA_HC_690MA

# 0x00011E4B S4\_PS\_PFM\_CURRENT\_LIM\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x84

Reset Name: PERPH RB

#### S4\_PS\_PFM\_CURRENT\_LIM\_CTL

Bits	Name	Description
7	CURRENT_LIM_EN	0 = disable
		1 = enable
		0x0: CURRENT_LIM_EN_FALSE
		0x1: CURRENT_LIM_EN_TRUE

#### S4\_PS\_PFM\_CURRENT\_LIM\_CTL (cont.)

Bits	Name	Description
2:0	CURRENT_LIM_SEL	Iplimit_sel<2:0> for current limit threshold programming when operating in PFM mode.
		Iplimit = 800 mA - m * 100 mA
		where m is the bit value of iplimit_sel<2:0>
		Note: The preset value and the final values of these bits are device specific and listed in the device SBI table.
		0x0: CURRENT_LIM_SEL_800MA
		0x1: CURRENT_LIM_SEL_700MA
		0x2: CURRENT_LIM_SEL_600MA
		0x3: CURRENT_LIM_SEL_500MA
		0x4: CURRENT_LIM_SEL_400MA
		0x5: CURRENT_LIM_SEL_300MA
		0x6: CURRENT_LIM_SEL_200MA
		0x7: CURRENT_LIM_SEL_100MA

#### 0x00011E80 S4\_PS\_HCINT\_EN

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

# S4\_PS\_HCINT\_EN

Bits	Name	Description
7	HCINT_EN	0 = INT disable
		1 = INT enable
		0x0: INT_DISABLE
		0x1: INT_ENABLE

# 0x00011E81 S4\_PS\_HCINT\_CONTROL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

# S4\_PS\_HCINT\_CONTROL

Bits	Name	Description
5	SET_WINDOW_WIDTH	This bit controls the deglitch window to set interrupt based on no. of cycles of 32KHz clock 0 = 2cycles to set 1 = 16cycles to set 0x0: CYCLES2 0x1: CYCLES16
4	RESET_WINDOW_WIDTH	This bit controls the deglitch window to reset interrupt based on no. of cycles of 32KHz clock 0 = 2cycles to reset 1 = 16cycles to reset 0x0: CYCLESRESET2 0x1: CYCLESRESET16
3:2	INT2_CUR_THRESHOLD	rated current - 10%*(m+1) 0x0: RATED_CURRENT_90PCT 0x1: RATED_CURRENT_80PCT 0x2: RATED_CURRENT_70PCT 0x3: RATED_CURRENT_60PCT
1:0	INT1_CUR_THRESHOLD	rated current - 10%*(m+3) 0x0: RATED_CURRENT_70PCT 0x1: RATED_CURRENT_60PCT 0x2: RATED_CURRENT_50PCT 0x3: RATED_CURRENT_40PCT

# 52 Bclk\_gen\_clk Registers

### 0x00011F00 S4\_FREQ\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

### S4\_FREQ\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

### 0x00011F01 S4\_FREQ\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: N/A

HW Version Register [15:8]

### S4\_FREQ\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00011F04 S4\_FREQ\_PERPH\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x1D

Reset Name: N/A

Peripheral Type

#### S4\_FREQ\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	BCLK GEN

### 0x00011F05 S4\_FREQ\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x19 Reset Name: N/A

Peripheral SubType

### S4\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	BCLK GEN CLK

### 0x00011F46 S4\_FREQ\_CLK\_ENABLE

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

### S4\_FREQ\_CLK\_ENABLE

Bits	Name	Description
7	EN_CLK_INT	0 = do not force the clock on
		1 = enable the clock
		0x0: FORCE_EN_DISABLED
		0x1: FORCE_EN_ENABLED

### S4\_FREQ\_CLK\_ENABLE (cont.)

Bits	Name	Description
0	FOLLOW_CLK_SX_REQ	0 = ignore smps_clk_req <x></x>
		1 = clock is enabled when the clocks request is high smps_clk_req <x>='1'</x>
		0x0: FALLOW_CLK_REQ_DISABLED
		0x1: FALLOW_CLK_REQ_ENABLED

### 0x00011F50 S4\_FREQ\_CLK\_DIV

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x0B

Reset Name: PERPH\_RB

PMIC LOCKED=SEC ACCESS, PMIC GANGED

## S4\_FREQ\_CLK\_DIV

Bits	Name	Description
3:0	CLK_DIV	clock_ frequency = 19.2MHz / (CLK_DIV + 1)
		FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz
	0,100	HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz
	o dillis	CLK_DIV = 0 is not supported, it will generate 9.6 MHz
	750 110	0x0: FREQ_9M6HZ_0
	2018-24 Chillip	0x1: FREQ_9M6HZ
	1	0x2: FREQ_6M4HZ
		0x3: FREQ_4M8HZ
		0x4: FREQ_3M8HZ
		0x5: FREQ_3M2HZ
		0x6: FREQ_2M7HZ
		0x7: FREQ_2M4HZ
		0x8: FREQ_2M1HZ
		0x9: FREQ_1M9HZ
		0xA: FREQ_1M7HZ
		0xB: FREQ_1M6HZ
		0xC: FREQ_1M5HZ
		0xD: FREQ_1M4HZ
		0xE: FREQ_1M3HZ
		0xF: FREQ_1M2HZ

### 0x00011F51 S4\_FREQ\_CLK\_PHASE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x07

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S4\_FREQ\_CLK\_PHASE

Bits	Name	Description
3:0	CLK_PHASE	Distributed clock phase select:
		clock phase delay = clock period * (CLK_PHASE / 16)

### 0x00011FC0 S4\_FREQ\_GANG\_CTL1

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

### S4\_FREQ\_GANG\_CTL1

Bits	Name	Description
7:0	GANG_LEADER_PID	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

### 0x00011FC1 S4\_FREQ\_GANG\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

### S4\_FREQ\_GANG\_CTL2

Bits	Name	Description
7	GANG_EN	0 = disable
		1 = enable
		When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral
		0x0: GANGING_DISABLED
		0x1: GANGING_ENABLED



# 53 Fts2p5\_ctrl Registers

### 0x00012000 S5\_CTRL\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x04

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

### S5\_CTRL\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

### S5\_CTRL\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00012002 S5\_CTRL\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### S5\_CTRL\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

### 0x00012003 S5\_CTRL\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [31:24]

#### S5\_CTRL\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

### 0x00012004 S5\_CTRL\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x1C

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

### S5\_CTRL\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	

### 0x00012005 S5\_CTRL\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x09

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

### S5\_CTRL\_PERPH\_SUBTYPE

l	Bits	Name	Description
	7:0	SUBTYPE	oi.

### 0x00012008 S5\_CTRL\_STATUS\_1

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: N/A

**Status Registers** 

### S5\_CTRL\_STATUS\_1

Bits	Name	Description
7	VREG_READY_FLAG	Indicates that VREG has reached a value that is greater than or equal to the threshold of a comparator tasked for VREG monitoring; masked to '0' during voltage stepping 0x0: VREG_READY_FLAG_FALSE 0x1: VREG_READY_FLAG_TRUE
6	VREG_FAULT_FLAG	Indicates a probable short circuit condition at VREG since VREG is below the VREG fault voltage level and the softstart ramp is done; current limit foldback is in use.  0x0: VREG_FAULT_FLAG_FALSE  0x1: VREG_FAULT_FLAG_TRUE

### S5\_CTRL\_STATUS\_1 (cont.)

Bits	Name	Description
1	NPM_FLAG	Indicates normal power mode is in use 0x0: NPM_FLAG_FALSE 0x1: NPM_FLAG_TRUE
0	STEPPER_DONE_FLAG	Softstart stepper and voltage stepper done 0x0: STEPPER_DONE_FLAG_FALSE 0x1: STEPPER_DONE_FLAG_TRUE

#### S5\_CTRL\_STATUS\_2 0x00012009

## S5\_CTRL\_STATUS

0	STEPPER_DONE_FLAG	0x0: STEPPER_DONE_FLAG_FALSE
		0x1: STEPPER_DONE_FLAG_TRUE
SE C	TDI STATUS 2	
35_C	TRL_STATUS_2	
Type:		
	PBUS_WRCLK	19
Reset S	State: Undefined	
Reset 1	Name: N/A	
Status 1	Registers	
		180
S5_CT	RL_STATUS_2	N. C.
Bits	Name	Description
4	ILS FLAG	Illegal limit stop flag: either of the following:
	9 69 1119	The upper limit stop VSET_ULS has been programmed to a value
	18, O.M.	below the lower limit stop VSET_LLS, or the lower limit stop
	30, 34	VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS
	1	0x0: ILS_FLAG_FALSE
		0x1: ILS_FLAG_TRUE
3	ULS_FLAG	Indicates that the voltage setpoint has been programmed to a
	_	value that is greater than or equal to the upper limit stop
		VSET_ULS 0x0: ULS_FLAG_FALSE
		0x1: ULS_FLAG_TRUE
	LLC FLAC	
2	LLS_FLAG	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS
		0x0: LLS_FLAG_FALSE
		0x1: LLS_FLAG_TRUE
1	GPL_HI_FLAG	Indicates that the voltage setpoint has reached a value that is
		greater than or equal to the high general purpose limit
		VSET_GPL_HI 0x0: GPL_HI_FLAG_FALSE
		0x1: GPL_HI_FLAG_TRUE
0	GPL_LO_FLAG	Indicates that the voltage setpoint has reached a value that is less
	O. L_LO_1 L/10	than or equal to the low general purpose limit VSET_GPL_LO
		0x0: GPL_LO_FLAG_FALSE
		0x1: GPL_LO_FLAG_TRUE
	1	1

#### 

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: PERPH RB

Interrupt Real Time Status Bits

### S5\_CTRL\_INT\_RT\_STS

Bits	Name	Description
2	VREG_FAULT_INT	Interrupt Real Time Status  0x0: VREG_FAULT_INT_FALSE  0x1: VREG_FAULT_INT_TRUE
1	VREG_READY_INT	Interrupt Real Time Status  0x0: VREG_READY_INT_FALSE  0x1: VREG_READY_INT_TRUE
0	VREG_ERROR_INT	Interrupt Real Time Status 0x0: VREG_ERROR_INT_FALSE 0x1: VREG_ERROR_INT_TRUE

## 0x00012011 S5\_CTRL\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

### S5\_CTRL\_INT\_SET\_TYPE

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_LEVEL_TRIGGERED 0x1: VREG_FAULT_INT_EDGE_TRIGGERED
1	VREG_READY_INT	0x0: VREG_READY_INT_LEVEL_TRIGGERED 0x1: VREG_READY_INT_EDGE_TRIGGERED
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_LEVEL_TRIGGERED 0x1: VREG_ERROR_INT_EDGE_TRIGGERED

### 0x00012012 S5\_CTRL\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

### S5\_CTRL\_INT\_POLARITY\_HIGH

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_RISING_EDGE_TRIGGER_DISABL 0x1: VREG_FAULT_INT_RISING_EDGE_TRIGGER_ENABL
1	VREG_READY_INT	0x0: VREG_READY_INT_RISING_EDGE_TRIGGER_DISABL 0x1: VREG_READY_INT_RISING_EDGE_TRIGGER_ENABL
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_RISING_EDGE_TRIGGER_DISABL 0x1: VREG_ERROR_INT_RISING_EDGE_TRIGGER_ENABL

### 0x00012013 S5\_CTRL\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

### S5\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALLING_EDGE_TRIGGER_DISABL 0x1: VREG_FAULT_INT_FALLING_EDGE_TRIGGER_ENABL
1	VREG_READY_INT	0x0: VREG_READY_INT_FALLING_EDGE_TRIGGER_DISABL 0x1: VREG_READY_INT_FALLING_EDGE_TRIGGER_ENABL
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_FALLING_EDGE_TRIGGER_DISABL 0x1: VREG_ERROR_INT_FALLING_EDGE_TRIGGER_ENABL

### 0x00012014 S5\_CTRL\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

### S5\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Description
2	VREG_FAULT_INT	
1	VREG_READY_INT	
0	VREG_ERROR_INT	0

### 0x00012015 S5\_CTRL\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

### S5\_CTRL\_INT\_EN\_SET

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_DISABL
		0x1: VREG_FAULT_INT_ENABL
1	VREG_READY_INT	0x0: VREG_READY_INT_DISABL
		0x1: VREG_READY_INT_ENABL
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_DISABL
		0x1: VREG_ERROR_INT_ENABL

#### 

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

### S5\_CTRL\_INT\_EN\_CLR

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_DISABL
		0x1: VREG_FAULT_INT_ENABL
1	VREG_READY_INT	0x0: VREG_READY_INT_DISABL
		0x1: VREG_READY_INT_ENABL
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_DISABL
		0x1: VREG_ERROR_INT_ENABL

## 0x00012018 S5\_CTRL\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

### S5\_CTRL\_INT\_LATCHED\_STS

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_NOT_TRIGGERED 0x1: VREG_FAULT_INT_TRIGGERED_AND_LATCHED
1	VREG_READY_INT	0x0: VREG_READY_INT_NOT_TRIGGERED 0x1: VREG_READY_INT_TRIGGERED_AND_LATCHED
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_NOT_TRIGGERED 0x1: VREG_ERROR_INT_TRIGGERED_AND_LATCHED

### 0x00012019 S5\_CTRL\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Pending is set if interrupt has been sent but not cleared.

### S5\_CTRL\_INT\_PENDING\_STS

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_NOT_PENDING 0x1: VREG_FAULT_INT_PENDING
1	VREG_READY_INT	0x0: VREG_READY_INT_NOT_PENDING 0x1: VREG_READY_INT_PENDING
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_NOT_PENDING 0x1: VREG_ERROR_INT_PENDING

### 0x0001201A S5\_CTRL\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### S5\_CTRL\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	Master ID that will receive the interrupt
		0x0: MID_0
		0x1: MID_1
		0x2: MID_2
		0x3: MID_3

### 0x0001201B S5\_CTRL\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

### S5\_CTRL\_INT\_PRIORITY

	Bits	Name	Description
ĺ	0	INT_PRIORITY	Interrupt Priority
			0x0: INT_PRIORITY_0
			0x1: INT_PRIORITY_1

### 0x00012040 S5\_CTRL\_VOLTAGE\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC GANGED, PMIC LATCHED WRITE=VOLTAGE CTL2

### S5\_CTRL\_VOLTAGE\_CTL1

Bits	Name	Description
0	MV_RANGE	0 = Use low voltage range as specified by VSET and PFM_VOFFSET
	27	1 = Use medium voltage range as specified by VSET and PFM_VOFFSET
	OS MINS	0x0: MV_RANGE_FALSE
	018,1161	0x1: MV_RANGE_TRUE

### 0x00012041 S5\_CTRL\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0xE5

Reset Name: PERPH RB

PMIC GANGED

### S5\_CTRL\_VOLTAGE\_CTL2

Bits	Name	Description
7:0	VSET	Output voltage set point in PWM mode and in PFM mode. VSET is not ENUM'd.
		For MV_RANGE = 0:
		VSET => 0.005V * m + 0.08V, where m = <7:0>
		For MV_RANGE = 1:
		VSET => 0.010V * m + 0.160V, where m = <7:0>

### 0x00012042 S5\_CTRL\_VSET\_VALID

**Type:** R

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: PERPH RB

#### S5\_CTRL\_VSET\_VALID

Bits	Name	Description
7:0	VSET_VALID	Readback the valid output voltage setpoint value. VSET_VALID is not ENUM'd.,,,,'

### 0x00012045 S5\_CTRL\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH RB

PMIC GANGED

### S5\_CTRL\_MODE\_CTL

Bits	Name	Description
7	NPM	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM) 0x0: NPM_NOT_FORCED 0x1: NPM_FORCED_IF_ENABL
6	AUTO_MODE	When NPM is not asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers 0 = AUTO mode is disabled 1 = AUTO mode is enabled 0x0: AUTO_MODE_FALSE 0x1: AUTO_MODE_TRUE

### 0x00012046 S5\_CTRL\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC GANGED

### S5\_CTRL\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	FTS enable control
		0 = Off
		1 = On
		0x0: FTS_DISABL
		0x1: FTS_ENABL

### 0x00012048 S5\_CTRL\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x88

Reset Name: PERPH RB

### S5\_CTRL\_PD\_CTL

Bits	Name	Description
7	PD_EN	0 = Strong pull-down is always disabled 1 = Strong pull-down is enabled when the regulator is disabled 0x0: STRONG_PD_ALWAYS_OFF 0x1: STRONG_PD_ON_WHEN_FTS_IS_DISABL
6	WEAK_PD_EN	0 = Weak pull-down is not enabled in OFF state 1 = Weak pull-down is enabled in OFF state 0x0: WEAK_PD_DISABL_IN_PMIC_OFF_STATE 0x1: SWEAK_PD_ENABL_IN_PMIC_OFF_STATE
5	WEAK_PD_PFM	0 = Weak pull-down is not enabled in PFM mode 1 = Weak pull-down is enabled in PFM mode 0x0: WEAK_PD_DISABL_IN_PFM 0x1: WEAK_PD_ENABL_IN_PFM
4	WEAK_PD_PWM	0 = Weak pull-down is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pull-down is enabled in PWM mode (and in HCPFM mode) 0x0: WEAK_PD_DISABL_IN_PWM_AND_HCPFM 0x1: WEAK_PD_ENABL_IN_PWM_AND_HCPFM
3	LEAK_PD_EN	0 = Leakage pull-down is always disabled 1 = Leakage pull-down is always enabled 0x0: LEAKAGE_PD_ALWAYS_OFF 0x1: LEAKAGE_PD_ALWAYS_ENABL

### 0x00012050 S5\_CTRL\_FREQ\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x05

Reset Name: PERPH\_RB

PMIC\_GANGED, PMIC\_LOCKED=SEC\_ACCESS

### S5\_CTRL\_FREQ\_CTL

Bits	Name	Description
3:0	FREQ_CTL	Clock frequency = 19.2MHz / (CLK_DIV + 1)
		FTS2.5 buck supports 0.8, 1.6, 3.2,4.8, and 6.4 MHz
		0000 = Not supported
		0001 = Not supported
		0010 = 6.4MHz
		0011 = 4.8MHz
		0100 = Not supported
		0101 = 3.2MHz
	. ( )	0110 = Not supported
		0111 = Not supported
		1000 = Not supported
	27.0	1001 = Not supported
	3 3	1010 = Not supported
	G. OTHILL	1011 = 1.6MHz
	2018-09 winds	1100 = Not supported
	7	1101 = Not supported
	V	1110 = Not supported
		1111 = Not supported
		0x2: FS_6M4HZ
		0x3: FS_4M8HZ
		0x5: FS_3M2MHZ
		0xB: FS_1M6MHZ

### 0x00012053 S5\_CTRL\_PHASE\_ID

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

### S5\_CTRL\_PHASE\_ID

Bits	Name	Description
3:0	PHASE_ID	Unique phase identifier. If less than or equal to PHASE_CNT_MAX, phase is active. If greater than PHASE_CNT_MAX, phase is inactive.  0x0: PHASE_NUMBER_1 0x1: PHASE_NUMBER_2 0x2: PHASE_NUMBER_3 0x3: PHASE_NUMBER_4

## 0x00012054 S5\_CTRL\_PHASE\_CNT\_MAX

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC GANGED

### S5\_CTRL\_PHASE\_CNT\_MAX

Bits	Name	Description
3:0	PHASE_CNT_MAX	Sets the maximum number of phases that the autonomous phase controller (APC) can use. If greater than or equal to PHASE_ID, the autonomous phase controller may or may not keep the phase active. If less than PHASE_ID, that phase will go to standby mode.

### 0x00012060 S5\_CTRL\_SS\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

PMIC GANGED

## S5\_CTRL\_SS\_CTL

Bits	Name	Description
4:3	SS_STEP	Softstart stepping voltage step size  00 = SS voltage step of 1 * LSB of VSET  01 = SS voltage step of 2 * LSB  10 = SS voltage step of 4 * LSB  11 = SS voltage step of 8 * LSB  0x0: SOFT_START_VSTEP_1_LSB  0x1: SOFT_START_VSTEP_2_LSB  0x2: SOFT_START_VSTEP_4_LSB  0x3: SOFT_START_VSTEP_8_LSB
2:0	SS_DELAY	Softstart delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz):  000 = 8-clock cycles (417ns)  001 = 16-clock cycles  010 = 32-clock cycles  011 = 64-clock cycles  100 = 128-clock cycles (6.67us)  101 = 256-clock cycles  110 = invalid  0x0: SOFT_START_TIME_STEP_417NS  0x1: SOFT_START_TIME_STEP_833NS  0x2: SOFT_START_TIME_STEP_1U67S  0x3: SOFT_START_TIME_STEP_3U3S  0x4: SOFT_START_TIME_STEP_6U7S  0x5: SOFT_START_TIME_STEP_13U3S  0x6: SOFT_START_TIME_STEP_13U3S  0x6: SOFT_START_TIME_STEP_26U7S  0x7: SOFT_START_TIME_STEP_53U3S

## 0x00012061 S5\_CTRL\_VS\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x85

Reset Name: PERPH\_RB

PMIC\_GANGED

## S5\_CTRL\_VS\_CTL

Bits	Name	Description
7	VS_EN	Voltage stepping control 0x0: VSTEPPER_DISABL 0x1: VSTEPPER_ENABL

### S5\_CTRL\_VS\_CTL (cont.)

Bits	Name	Description
4:3	VS_STEP	Voltage stepping voltage step size  00 = VS voltage step of 1 * LSB of VSET  01 = VS voltage step of 2 * LSB  10 = VS voltage step of 4 * LSB  11 = VS voltage step of 8 * LSB  0x0: VSTEPPER_STEP_SIZE_1_LSB  0x1: VSTEPPER_STEP_SIZE_2_LSB  0x2: VSTEPPER_STEP_SIZE_4_LSB  0x3: VSTEPPER_STEP_SIZE_8_LSB
2:0	VS_DELAY	Voltage stepping delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz):  000 = 8-clock cycles (417ns)  001 = 16-clock cycles  010 = 32-clock cycles  011 = 64-clock cycles  100 = 128-clock cycles (6.67us)  101 = 256-clock cycles  110 = invalid  111 = invalid  0x0: VSTEPPER_TIME_STEP_417NS  0x1: VSTEPPER_TIME_STEP_833NS  0x2: VSTEPPER_TIME_STEP_1U67S  0x3: VSTEPPER_TIME_STEP_3U3S  0x4: VSTEPPER_TIME_STEP_6U7S  0x5: VSTEPPER_TIME_STEP_13U3S  0x6: VSTEPPER_TIME_STEP_13U3S  0x6: VSTEPPER_TIME_STEP_26U7S  0x7: VSTEPPER_TIME_STEP_53U3S

## 0x00012066 S5\_CTRL\_CFG\_VREG\_OCP

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

### S5\_CTRL\_CFG\_VREG\_OCP

Bits	Name	Description
7	OCP_LAT_EN	0 = Do not latch off regulator during OCP conditions
		1 = Latch off regulator after OCP condition has been detected for at least 16 32kHz cycles outside of a stepper operation 0x0: OCP_LATCH_DISABL 0x1: OCP_LATCH_ENABL

### S5\_CTRL\_CFG\_VREG\_OCP (cont.)

Bits	Name	Description
6	OCP_RETRY_EN	0 = Do not autonomously clear latched OCP condition 1 = Autonomously clear latched OCP condition after 5ms 0x0: OCP_RETRY_DISABL 0x1: OCP_RETRY_ENABL
5	OCP_CLR	Toggle to clear a latched OCP condition and enable the regulator when PERPH_EN is asserted

### 0x00012068 S5\_CTRL\_UL\_LL\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_GANGED, PMIC\_LOCKED=SEC\_ACCESS

### S5\_CTRL\_UL\_LL\_CTL

Bits	Name	Description
7	ULEN 2018-09 miller	0 = Disable upper limit stop 1 = Enable upper limit stop 0x0: UL_STOP_DISABL 0x1: UL_STOP_ENABL
6	LL_EN	0 = Disable lower limit stop 1 = Enable lower limit stop 0x0: LL_STOP_DISABL 0x1: LL_STOP_ENABL

### 0x00012069 S5\_CTRL\_VSET\_ULS

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0xFF

Reset Name: PERPH RB

PMIC\_GANGED, PMIC\_LOCKED=SEC\_ACCESS

### S5\_CTRL\_VSET\_ULS

Bits	Name	Description
7:0	VSET_ULS	If UL_EN is asserted, and VSET is set to a value greater than or equal to VSET_ULS, ULS_FLAG and VREG_READY_INT are asserted For MV_RANGE = 0: VSET_ULS => 0.005V * m + 0.080V, where m = <7:0>
		For MV_RANGE = 1:
		VSET_ULS => 0.010V * m + 0.160V, where m = <7:0>

### 0x0001206A S5\_CTRL\_ULS\_VALID

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: PERPH\_RB

### S5\_CTRL\_ULS\_VALID

Bits	Name	Description
7:0	ULS_VALID	Readback the valid upper limit stop value

### 0x0001206B S5\_CTRL\_VSET\_LLS

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC GANGED, PMIC LOCKED=SEC ACCESS

### S5\_CTRL\_VSET\_LLS

Bits	Name	Description
7:0	VSET_LLS	If LL_EN is asserted, and VSET is set to a value less than or equal to VSET_LLS, LLS_FLAG and VREG_READY_INT are asserted For MV_RANGE = 0:  VSET_LLS => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1:  VSET_LLS => 0.010V * m + 0.160V, where m = <7:0>

### 0x0001206C S5\_CTRL\_LLS\_VALID

**Type:** R

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: PERPH RB

### S5\_CTRL\_LLS\_VALID

Bits	Name	Description
7:0	LLS_VALID	Readback the valid lower limit stop value

## 0x0001206D S5\_CTRL\_GPL\_HI

Type: RW

Clock: PBUS\_WRCLK Reset State: 0xFF

Reset Name: PERPH RB

PMIC\_GANGED, PMIC\_LOCKED=SEC\_ACCESS

### S5\_CTRL\_GPL\_HI

Bits	Name	Description
7:0	VSET_GPL_HI	When output voltage setpoint reaches a value greater than or equal to VSET_GPL_HI, set GPL_HI_FLAG and VREG_READY_INT For MV_RANGE = 0: VSET_GPL_HI => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET_GPL_HI => 0.010V * m + 0.160V, where m = <7:0>

### 0x0001206E S5\_CTRL\_GPL\_LO

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_GANGED, PMIC\_LOCKED=SEC\_ACCESS

### S5\_CTRL\_GPL\_LO

Bits	Name	Description
7:0	VSET_GPL_LO	When output voltage setpoint reaches a value less than or equal to VSET_GPL_LO value, set GPL_LO_FLAG and VREG_READY_INT
		For MV_RANGE = 0:
		VSET_GPL_LO => 0.005V * m + 0.80V, where m = <7:0>
		For MV_RANGE = 1:
		VSET_GPL_LO => 0.010V * m + 0.160V, where m = <7:0>

### 0x000120C0 S5\_CTRL\_GANG\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x20

Reset Name: shutdown2 rb

PMIC\_LOCKED=SEC ACCESS

### S5\_CTRL\_GANG\_CTL1

Bits	Name	Description
7:0	GANG_LEADER_PID	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

## 0x000120C1 S5\_CTRL\_GANG\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: shutdown2 rb

PMIC\_LOCKED=SEC\_ACCESS

### S5\_CTRL\_GANG\_CTL2

Bits	Name	Description
7	GANG_EN	0 = disable
		1 = enable
		When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral
		0x0: GANG_EN_FALSE
		0x1: GANG_EN_TRUE



# 54 Fts2p5\_ps Registers

### 0x00012100 S5\_PS\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

### S5\_PS\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software.
	· · ·	Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

### 0x00012101 S5\_PS\_REVISION2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

### S5\_PS\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00012102 S5\_PS\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### S5\_PS\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software.
		Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

### 0x00012103 S5\_PS\_REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### S5\_PS\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 

Type: R

Clock: PBUS\_WRCLK Reset State: 0x1C

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

### S5\_PS\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	

### 0x00012105 S5\_PS\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x04

Reset Name: N/A

Peripheral SubType

### S5\_PS\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	180

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## 0x00012140 S5\_PS\_VOLTAGE\_CTL1

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC GANGED, PMIC LATCHED WRITE=VOLTAGE CTL2

### S5\_PS\_VOLTAGE\_CTL1

Bits	Name	Description
0	MV_RANGE	0 = Use low voltage range as specified by VSET and PFM_VOFFSET
		1 = Use medium voltage range as specified by VSET and PFM_VOFFSET
		0x0: LV_RANGE
		0x1: MV_RANGE

#### 

Type: RW

Clock: PBUS\_WRCLK Reset State: 0xE5

Reset Name: PERPH RB

PMIC GANGED

### S5\_PS\_VOLTAGE\_CTL2

Bits	Name	Description
7:0	VSET	Output voltage set point in PWM mode and in PFM mode For MV RANGE = 0:
		VSET => 0.005V * m + 0.080V, where m = <7:0>
		For MV_RANGE = 1:
		VSET => 0.010V * m + 0.160V, where m = <7:0> If PFM VOFFSET EN is asserted and in PFM mode, add
		PFM_VOFFSET

## 0x00012145 S5\_PS\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH RB

PMIC GANGED

### S5\_PS\_MODE\_CTL

Bits	Name	Description
7	NPM	FTS NON-AUTO mode control
		0 = Low power mode (LPM) unless AUTO_MODE is asserted
		1 = Normal power mode (PWM)
		0x0: NPM_NOT_FORCED
		0x1: NPM_FORCED_IF_ENABL
6	AUTO_MODE	When NPM is not asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers
		0 = AUTO mode is disabled
		1 = AUTO mode is enabled
		0x0: AUTO_MODE_FALSE
		0x1: AUTO_MODE_TRUE

### 0x00012150 S5\_PS\_FREQ\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x05

Reset Name: PERPH\_RB

PMIC\_GANGED, PMIC\_LOCKED=SEC\_ACCESS

### S5\_PS\_FREQ\_CTL

Bits	Name	Description
3:0	FREQ_CTL	Clock frequency = 19.2MHz / (CLK_DIV + 1)
		FTS2.5 buck supports 0.8, 1.6, 3.2,4.8, and 6.4 MHz
		0000 = Not supported
		0001 = Not supported
		0010 = 6.4MHz
		0011 = 4.8MHz
		0100 = Not supported
		0101 = 3.2MHz
		0110 = Not supported
		0111 = Not supported
		1000 = Not supported
	2.5	1001 = Not supported
	00'0118	1010 = Not supported
	C. Capille	1011 = 1.6MHz
	O' Me	1100 = Not supported
	2018-09 winds	1101 = Not supported
	V	1110 = Not supported
		1111 = Not supported
		0x2: FS_6M4HZ
		0x3: FS_4M8HZ
		0x5: FS_3M2MHZ
		0xB: FS_1M6MHZ

### 

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

### S5\_PS\_PHASE\_ID

Bits	Name	Description	
3:0	PHASE_ID	Unique phase identifier. If less than or equal to PHASE_CNT_MAX, phase is active. If greater than PHASE_CNT_MAX, phase is inactive.  0x0: PHASE_NUMBER_1  0x1: PHASE_NUMBER_2  0x2: PHASE_NUMBER_3  0x3: PHASE_NUMBER_4	
S5_PS_PHASE_CNT_MAX  Type: RW Clock: PBUS_WRCLK Reset State: 0x00			
Reset N	Reset Name: PERPH_RB		
PMIC_GANGED			
S5_PS	_PHASE_CNT_MAX	01:700	
Bits	Name	Description	

#### 0x00012154 S5\_PS\_PHASE\_CNT\_MAX

### S5\_PS\_PHASE\_CNT\_MAX

Bits	Name	Description
3:0	PHASE_CNT_MAX	Sets the maximum number of phases that the autonomous phase controller (APC) can use. If greater than or equal to PHASE_ID, the autonomous phase controller may or may not keep the phase active. If less than PHASE_ID, that phase will go to standby mode.

### 0x000121C0 S5\_PS\_GANG\_CTL1

Type: RW

Clock: PBUS WRCLK Reset State: 0x20

Reset Name: shutdown2 rb

PMIC LOCKED=SEC ACCESS

### S5\_PS\_GANG\_CTL1

Bits	Name	Description
7:0	GANG_LEADER_PID	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID.  Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

#### 

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: shutdown2 rb

PMIC LOCKED=SEC ACCESS

### S5\_PS\_GANG\_CTL2

Bits	Name	Description
7	GANG_EN	0 = disable
		1 = enable
		When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral 0x0: GANG_EN_FALSE
		0x1: GANG_EN_TRUE
	2018-09-21-03	in con

# 55 Bclk\_gen\_clk Registers

### 0x00012200 S5\_FREQ\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

## S5\_FREQ\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

#### 

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: N/A

HW Version Register [15:8]

### S5\_FREQ\_REVISION2

Bit	S Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

### 0x00012204 S5\_FREQ\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x1D

Reset Name: N/A

Peripheral Type

### S5\_FREQ\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	BCLK GEN

### 0x00012205 S5\_FREQ\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x19 Reset Name: N/A

Peripheral SubType

### S5\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	BCLK GEN CLK

### 0x00012246 S5\_FREQ\_CLK\_ENABLE

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

### S5\_FREQ\_CLK\_ENABLE

Bits	Name	Description
7	EN_CLK_INT	0 = do not force the clock on
		1 = enable the clock
		0x0: FORCE_EN_DISABLED
		0x1: FORCE_EN_ENABLED

### S5\_FREQ\_CLK\_ENABLE (cont.)

Bits	Name	Description
0	FOLLOW_CLK_SX_REQ	0 = ignore smps_clk_req <x></x>
		1 = clock is enabled when the clocks request is high smps_clk_req <x>='1'</x>
		0x0: FALLOW_CLK_REQ_DISABLED
		0x1: FALLOW_CLK_REQ_ENABLED

### 0x00012250 S5\_FREQ\_CLK\_DIV

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x05

Reset Name: PERPH\_RB

PMIC LOCKED=SEC ACCESS, PMIC GANGED

## S5\_FREQ\_CLK\_DIV

Bits	Name	Description
3:0	CLK_DIV	clock_ frequency = 19.2MHz / (CLK_DIV + 1)
		FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz
	0,100	HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz
	o o nine	CLK_DIV = 0 is not supported, it will generate 9.6 MHz
	720 1101	0x0: FREQ_9M6HZ_0
	2018-24@minds	0x1: FREQ_9M6HZ
	1	0x2: FREQ_6M4HZ
		0x3: FREQ_4M8HZ
		0x4: FREQ_3M8HZ
		0x5: FREQ_3M2HZ
		0x6: FREQ_2M7HZ
		0x7: FREQ_2M4HZ
		0x8: FREQ_2M1HZ
		0x9: FREQ_1M9HZ
		0xA: FREQ_1M7HZ
		0xB: FREQ_1M6HZ
		0xC: FREQ_1M5HZ
		0xD: FREQ_1M4HZ
		0xE: FREQ_1M3HZ
		0xF: FREQ_1M2HZ

### 0x00012251 S5\_FREQ\_CLK\_PHASE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x03

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S5\_FREQ\_CLK\_PHASE

Bits	Name	Description
3:0	CLK_PHASE	Distributed clock phase select:
		clock phase delay = clock period * (CLK_PHASE / 16)

# 0x000122C0 S5\_FREQ\_GANG\_CTL1

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x20

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S5\_FREQ\_GANG\_CTL1

Bits	Name	Description
7:0	GANG_LEADER_PID	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

#### 0x000122C1 S5\_FREQ\_GANG\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

#### S5\_FREQ\_GANG\_CTL2

Bits	Name	Description
7	GANG_EN	0 = disable
		1 = enable
		When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral
		0x0: GANGING_DISABLED
		0x1: GANGING_ENABLED



# 56 Fts2p5\_ctrl Registers

# 0x00012300 S6\_CTRL\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x04

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### S6\_CTRL\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00012301 S6\_CTRL\_REVISION2

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### S6\_CTRL\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

# 0x00012302 S6\_CTRL\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### S6\_CTRL\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00012303 S6\_CTRL\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: N/A

HW Version Register [31:24]

#### S6\_CTRL\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 0x00012304 S6\_CTRL\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x1C

Reset Name: N/A

Peripheral Type

PMIC CONSTANT

#### S6\_CTRL\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	

#### 0x00012305 S6\_CTRL\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x09

Reset Name: N/A

Peripheral SubType

PMIC\_CONSTANT

#### S6\_CTRL\_PERPH\_SUBTYPE

l	Bits	Name	Description
	7:0	SUBTYPE	oi.

# 0x00012308 S6\_CTRL\_STATUS\_1

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: N/A

**Status Registers** 

#### S6\_CTRL\_STATUS\_1

Bits	Name	Description
7	VREG_READY_FLAG	Indicates that VREG has reached a value that is greater than or equal to the threshold of a comparator tasked for VREG monitoring; masked to '0' during voltage stepping 0x0: VREG_READY_FLAG_FALSE 0x1: VREG_READY_FLAG_TRUE
6	VREG_FAULT_FLAG	Indicates a probable short circuit condition at VREG since VREG is below the VREG fault voltage level and the softstart ramp is done; current limit foldback is in use.  0x0: VREG_FAULT_FLAG_FALSE  0x1: VREG_FAULT_FLAG_TRUE

#### S6\_CTRL\_STATUS\_1 (cont.)

Bits	Name	Description
1	NPM_FLAG	Indicates normal power mode is in use 0x0: NPM_FLAG_FALSE 0x1: NPM_FLAG_TRUE
0	STEPPER_DONE_FLAG	Softstart stepper and voltage stepper done 0x0: STEPPER_DONE_FLAG_FALSE 0x1: STEPPER_DONE_FLAG_TRUE

#### S6\_CTRL\_STATUS\_2 0x00012309

# S6\_CTRL\_STATUS

	OTEL TEN_BONE_TENO	0x0: STEPPER_DONE_FLAG_FALSE	
		0x1: STEPPER_DONE_FLAG_TRUE	
Type: Clock:	S6_CTRL_STATUS_2 Type: R Clock: PBUS_WRCLK Reset State: Undefined		
Reset N	Name: N/A		
Status 1	Registers		
	RL_STATUS_2	227	
Bits	Name	Description	
4	ILS_FLAG	Illegal limit stop flag: either of the following: The upper limit stop VSET_ULS has been programmed to a value below the lower limit stop VSET_LLS, or the lower limit stop VSET_LLS has been programmed to a value above the upper limit stop VSET_ULS  0x0: ILS_FLAG_FALSE  0x1: ILS_FLAG_TRUE	
3	ULS_FLAG	Indicates that the voltage setpoint has been programmed to a value that is greater than or equal to the upper limit stop VSET_ULS  0x0: ULS_FLAG_FALSE  0x1: ULS_FLAG_TRUE	
2	LLS_FLAG	Indicates that the voltage setpoint has been programmed to a value that is less than or equal to the lower limit stop VSET_LLS 0x0: LLS_FLAG_FALSE 0x1: LLS_FLAG_TRUE	
1	GPL_HI_FLAG	Indicates that the voltage setpoint has reached a value that is greater than or equal to the high general purpose limit VSET_GPL_HI 0x0: GPL_HI_FLAG_FALSE 0x1: GPL_HI_FLAG_TRUE	
0	GPL_LO_FLAG	Indicates that the voltage setpoint has reached a value that is less than or equal to the low general purpose limit VSET_GPL_LO 0x0: GPL_LO_FLAG_FALSE 0x1: GPL_LO_FLAG_TRUE	

#### 

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: PERPH RB

Interrupt Real Time Status Bits

#### S6\_CTRL\_INT\_RT\_STS

Bits	Name	Description
2	VREG_FAULT_INT	Interrupt Real Time Status  0x0: VREG_FAULT_INT_FALSE  0x1: VREG_FAULT_INT_TRUE
1	VREG_READY_INT	Interrupt Real Time Status 0x0: VREG_READY_INT_FALSE 0x1: VREG_READY_INT_TRUE
0	VREG_ERROR_INT	Interrupt Real Time Status 0x0: VREG_ERROR_INT_FALSE 0x1: VREG_ERROR_INT_TRUE

# 0x00012311 S6\_CTRL\_INT\_SET\_TYPE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

0 =use level trigger interrupts, 1 =use edge trigger interrupts

#### S6\_CTRL\_INT\_SET\_TYPE

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_LEVEL_TRIGGERED 0x1: VREG_FAULT_INT_EDGE_TRIGGERED
1	VREG_READY_INT	0x0: VREG_READY_INT_LEVEL_TRIGGERED 0x1: VREG_READY_INT_EDGE_TRIGGERED
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_LEVEL_TRIGGERED 0x1: VREG_ERROR_INT_EDGE_TRIGGERED

### 0x00012312 S6\_CTRL\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

1= Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### S6\_CTRL\_INT\_POLARITY\_HIGH

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_RISING_EDGE_TRIGGER_DISABL 0x1: VREG_FAULT_INT_RISING_EDGE_TRIGGER_ENABL
1	VREG_READY_INT	0x0: VREG_READY_INT_RISING_EDGE_TRIGGER_DISABL 0x1: VREG_READY_INT_RISING_EDGE_TRIGGER_ENABL
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_RISING_EDGE_TRIGGER_DISABL 0x1: VREG_ERROR_INT_RISING_EDGE_TRIGGER_ENABL

### 0x00012313 S6 CTRL INT POLARITY LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

1' = Interrupt will trigger on a level low (falling edge) event, '0' = level low triggering is disabled

#### S6\_CTRL\_INT\_POLARITY\_LOW

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_FALLING_EDGE_TRIGGER_DISABL 0x1: VREG_FAULT_INT_FALLING_EDGE_TRIGGER_ENABL
1	VREG_READY_INT	0x0: VREG_READY_INT_FALLING_EDGE_TRIGGER_DISABL 0x1: VREG_READY_INT_FALLING_EDGE_TRIGGER_ENABL
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_FALLING_EDGE_TRIGGER_DISABL 0x1: VREG_ERROR_INT_FALLING_EDGE_TRIGGER_ENABL

#### 0x00012314 S6\_CTRL\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### S6\_CTRL\_INT\_LATCHED\_CLR

Bits	Name	Description
2	VREG_FAULT_INT	
1	VREG_READY_INT	
0	VREG_ERROR_INT	0

# 0x00012315 S6\_CTRL\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### S6\_CTRL\_INT\_EN\_SET

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_DISABL
		0x1: VREG_FAULT_INT_ENABL
1	VREG_READY_INT	0x0: VREG_READY_INT_DISABL
		0x1: VREG_READY_INT_ENABL
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_DISABL
		0x1: VREG_ERROR_INT_ENABL

#### 

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### S6\_CTRL\_INT\_EN\_CLR

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_DISABL
		0x1: VREG_FAULT_INT_ENABL
1	VREG_READY_INT	0x0: VREG_READY_INT_DISABL
		0x1: VREG_READY_INT_ENABL
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_DISABL
		0x1: VREG_ERROR_INT_ENABL

# 0x00012318 S6\_CTRL\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Debug: Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### S6\_CTRL\_INT\_LATCHED\_STS

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_NOT_TRIGGERED 0x1: VREG_FAULT_INT_TRIGGERED_AND_LATCHED
1	VREG_READY_INT	0x0: VREG_READY_INT_NOT_TRIGGERED 0x1: VREG_READY_INT_TRIGGERED_AND_LATCHED
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_NOT_TRIGGERED 0x1: VREG_ERROR_INT_TRIGGERED_AND_LATCHED

## 0x00012319 S6\_CTRL\_INT\_PENDING\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Debug: Pending is set if interrupt has been sent but not cleared.

#### S6\_CTRL\_INT\_PENDING\_STS

Bits	Name	Description
2	VREG_FAULT_INT	0x0: VREG_FAULT_INT_NOT_PENDING 0x1: VREG_FAULT_INT_PENDING
1	VREG_READY_INT	0x0: VREG_READY_INT_NOT_PENDING 0x1: VREG_READY_INT_PENDING
0	VREG_ERROR_INT	0x0: VREG_ERROR_INT_NOT_PENDING 0x1: VREG_ERROR_INT_PENDING

# 0x0001231A S6\_CTRL\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

Selects the MID that will receive the interrupt

#### S6\_CTRL\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	Master ID that will receive the interrupt
		0x0: MID_0
		0x1: MID_1
		0x2: MID_2
		0x3: MID_3

#### 0x0001231B S6\_CTRL\_INT\_PRIORITY

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

SR=0 A=1

#### S6\_CTRL\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	Interrupt Priority 0x0: INT_PRIORITY_0 0x1: INT_PRIORITY_1

#### 0x00012340 S6\_CTRL\_VOLTAGE\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC GANGED, PMIC LATCHED WRITE=VOLTAGE CTL2

## S6\_CTRL\_VOLTAGE\_CTL1

Bits	Name	Description
0	MV_RANGE	0 = Use low voltage range as specified by VSET and PFM_VOFFSET
	27	1 = Use medium voltage range as specified by VSET and PFM_VOFFSET
	OS MINS	0x0: MV_RANGE_FALSE
	018,1161	0x1: MV_RANGE_TRUE

#### 0x00012341 S6\_CTRL\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0xE5

Reset Name: PERPH RB

PMIC GANGED

#### S6\_CTRL\_VOLTAGE\_CTL2

Bits	Name	Description
7:0	VSET	Output voltage set point in PWM mode and in PFM mode. VSET is not ENUM'd.
		For MV_RANGE = 0:
		VSET => 0.005V * m + 0.08V, where m = <7:0>
		For MV_RANGE = 1:
		VSET => 0.010V * m + 0.160V, where m = <7:0>

## 0x00012342 S6\_CTRL\_VSET\_VALID

**Type:** R

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: PERPH RB

#### S6\_CTRL\_VSET\_VALID

Bits	Name	Description
7:0	VSET_VALID	Readback the valid output voltage setpoint value. VSET_VALID is not ENUM'd.,,,,'

#### 0x00012345 S6\_CTRL\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH\_RB

PMIC GANGED

# S6\_CTRL\_MODE\_CTL

Bits	Name	Description
7	NPM	FTS NON-AUTO mode control 0 = Low power mode (LPM) unless AUTO_MODE is asserted 1 = Normal power mode (PWM) 0x0: NPM_NOT_FORCED 0x1: NPM_FORCED_IF_ENABL
6	AUTO_MODE	When NPM is not asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers 0 = AUTO mode is disabled 1 = AUTO mode is enabled 0x0: AUTO_MODE_FALSE 0x1: AUTO_MODE_TRUE

#### 0x00012346 S6\_CTRL\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC GANGED

#### S6\_CTRL\_EN\_CTL

Bits	Name	Description
7	PERPH_EN	FTS enable control
		0 = Off
		1 = On
		0x0: FTS_DISABL
		0x1: FTS_ENABL

# 0x00012348 S6\_CTRL\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: PERPH\_RB

#### S6\_CTRL\_PD\_CTL

Bits	Name	Description
7	PD_EN	0 = Strong pulldown is always disabled 1 = Strong pulldown is enabled when the regulator is disabled 0x0: STRONG_PD_ALWAYS_OFF 0x1: STRONG_PD_ON_WHEN_FTS_IS_DISABL
6	WEAK_PD_EN	0 = Weak pulldown is not enabled in OFF state 1 = Weak pulldown is enabled in OFF state 0x0: WEAK_PD_DISABL_IN_PMIC_OFF_STATE 0x1: SWEAK_PD_ENABL_IN_PMIC_OFF_STATE
5	WEAK_PD_PFM	0 = Weak pulldown is not enabled in PFM mode 1 = Weak pulldown is enabled in PFM mode 0x0: WEAK_PD_DISABL_IN_PFM 0x1: WEAK_PD_ENABL_IN_PFM
4	WEAK_PD_PWM	0 = Weak pulldown is not enabled in PWM mode (and in HCPFM mode) 1 = Weak pulldown is enabled in PWM mode (and in HCPFM mode) 0x0: WEAK_PD_DISABL_IN_PWM_AND_HCPFM 0x1: WEAK_PD_ENABL_IN_PWM_AND_HCPFM
3	LEAK_PD_EN	0 = Leakage pulldown is always disabled 1 = Leakage pulldown is always enabled 0x0: LEAKAGE_PD_ALWAYS_OFF 0x1: LEAKAGE_PD_ALWAYS_ENABL

#### 0x00012350 S6\_CTRL\_FREQ\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x05

Reset Name: PERPH\_RB

PMIC\_GANGED, PMIC\_LOCKED=SEC\_ACCESS

#### S6\_CTRL\_FREQ\_CTL

Bits	Name	Description
3:0	FREQ_CTL	Clock frequency = 19.2MHz / (CLK_DIV + 1)
		FTS2.5 buck supports 0.8, 1.6, 3.2,4.8, and 6.4 MHz
		0000 = Not supported
		0001 = Not supported
		0010 = 6.4MHz
	. (	0011 = 4.8MHz
		0100 = Not supported
		0101 = 3.2MHz
		0110 = Not supported
		0111 = Not supported
		1000 = Not supported
	2.5	1001 = Not supported
	9 01	1010 = Not supported
	C. Capille	1011 = 1.6MHz
	O' Me	1100 = Not supported
	2018-09 winds	1101 = Not supported
	V	1110 = Not supported
		1111 = Not supported
		0x2: FS_6M4HZ
		0x3: FS_4M8HZ
		0x5: FS_3M2MHZ
		0xB: FS_1M6MHZ

#### 0x00012353 S6\_CTRL\_PHASE\_ID

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

#### S6\_CTRL\_PHASE\_ID

Bits	Name	Description
3:0	PHASE_ID	Unique phase identifier. If less than or equal to PHASE_CNT_MAX, phase is active. If greater than PHASE_CNT_MAX, phase is inactive.  0x0: PHASE_NUMBER_1 0x1: PHASE_NUMBER_2 0x2: PHASE_NUMBER_3 0x3: PHASE_NUMBER_4

# 0x00012354 S6\_CTRL\_PHASE\_CNT\_MAX

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC GANGED

#### S6\_CTRL\_PHASE\_CNT\_MAX

Bits	Name	Description
3:0	PHASE_CNT_MAX	Sets the maximum number of phases that the autonomous phase controller (APC) can use. If greater than or equal to PHASE_ID, the autonomous phase controller may or may not keep the phase active. If less than PHASE_ID, that phase will go to standby mode.

#### 0x00012360 S6\_CTRL\_SS\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

PMIC GANGED

# S6\_CTRL\_SS\_CTL

Bits	Name	Description
4:3	SS_STEP	Softstart stepping voltage step size  00 = SS voltage step of 1 * LSB of VSET  01 = SS voltage step of 2 * LSB  10 = SS voltage step of 4 * LSB  11 = SS voltage step of 8 * LSB  0x0: SOFT_START_VSTEP_1_LSB  0x1: SOFT_START_VSTEP_2_LSB  0x2: SOFT_START_VSTEP_4_LSB  0x3: SOFT_START_VSTEP_8_LSB
2:0	SS_DELAY	Softstart delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz):  000 = 8-clock cycles (417ns)  001 = 16-clock cycles  010 = 32-clock cycles  011 = 64-clock cycles  100 = 128-clock cycles (6.67us)  101 = 256-clock cycles  110 = invalid  0x0: SOFT_START_TIME_STEP_417NS  0x1: SOFT_START_TIME_STEP_833NS  0x2: SOFT_START_TIME_STEP_1U67S  0x3: SOFT_START_TIME_STEP_3U3S  0x4: SOFT_START_TIME_STEP_6U7S  0x5: SOFT_START_TIME_STEP_13U3S  0x6: SOFT_START_TIME_STEP_13U3S  0x6: SOFT_START_TIME_STEP_26U7S  0x7: SOFT_START_TIME_STEP_53U3S

# 0x00012361 S6\_CTRL\_VS\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x85

Reset Name: PERPH\_RB

PMIC\_GANGED

# S6\_CTRL\_VS\_CTL

Bits	Name	Description
7	VS_EN	Voltage stepping control 0x0: VSTEPPER_DISABL 0x1: VSTEPPER_ENABL

#### S6\_CTRL\_VS\_CTL (cont.)

Bits	Name	Description
4:3	VS_STEP	Voltage stepping voltage step size  00 = VS voltage step of 1 * LSB of VSET  01 = VS voltage step of 2 * LSB  10 = VS voltage step of 4 * LSB  11 = VS voltage step of 8 * LSB  0x0: VSTEPPER_STEP_SIZE_1_LSB  0x1: VSTEPPER_STEP_SIZE_2_LSB  0x2: VSTEPPER_STEP_SIZE_4_LSB  0x3: VSTEPPER_STEP_SIZE_8_LSB
2:0	VS_DELAY	Voltage stepping delay between steps = 2 ^ (m + 3) / Fsys, where m = <2:0> (Fsys = 19.2 MHz):  000 = 8-clock cycles (417ns)  001 = 16-clock cycles  010 = 32-clock cycles  011 = 64-clock cycles  100 = 128-clock cycles (6.67us)  101 = 256-clock cycles  110 = invalid  111 = invalid  0x0: VSTEPPER_TIME_STEP_417NS  0x1: VSTEPPER_TIME_STEP_833NS  0x2: VSTEPPER_TIME_STEP_1U67S  0x3: VSTEPPER_TIME_STEP_3U3S  0x4: VSTEPPER_TIME_STEP_6U7S  0x5: VSTEPPER_TIME_STEP_13U3S  0x6: VSTEPPER_TIME_STEP_13U3S  0x6: VSTEPPER_TIME_STEP_26U7S  0x7: VSTEPPER_TIME_STEP_53U3S

# 0x00012366 S6\_CTRL\_CFG\_VREG\_OCP

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

# S6\_CTRL\_CFG\_VREG\_OCP

Bits	Name	Description
7	OCP_LAT_EN	0 = Do not latch off regulator during OCP conditions
		1 = Latch off regulator after OCP condition has been detected for at least 16 32kHz cycles outside of a stepper operation 0x0: OCP_LATCH_DISABL 0x1: OCP_LATCH_ENABL

#### S6\_CTRL\_CFG\_VREG\_OCP (cont.)

Bits	Name	Description
6	OCP_RETRY_EN	0 = Do not autonomously clear latched OCP condition 1 = Autonomously clear latched OCP condition after 5ms 0x0: OCP_RETRY_DISABL 0x1: OCP_RETRY_ENABL
5	OCP_CLR	Toggle to clear a latched OCP condition and enable the regulator when PERPH_EN is asserted

# 0x00012368 S6\_CTRL\_UL\_LL\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_GANGED, PMIC\_LOCKED=SEC\_ACCESS

#### S6\_CTRL\_UL\_LL\_CTL

Bits	Name	Description
7	UL_EN 2018-5MENITER	0 = Disable upper limit stop 1 = Enable upper limit stop 0x0: UL_STOP_DISABL 0x1: UL_STOP_ENABL
6	LL_EN	0 = Disable lower limit stop 1 = Enable lower limit stop 0x0: LL_STOP_DISABL 0x1: LL_STOP_ENABL

#### 0x00012369 S6\_CTRL\_VSET\_ULS

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0xFF

Reset Name: PERPH RB

PMIC\_GANGED, PMIC\_LOCKED=SEC\_ACCESS

#### S6\_CTRL\_VSET\_ULS

Bits	Name	Description
7:0	VSET_ULS	If UL_EN is asserted, and VSET is set to a value greater than or equal to VSET_ULS, ULS_FLAG and VREG_READY_INT are asserted For MV_RANGE = 0: VSET_ULS => 0.005V * m + 0.080V, where m = <7:0>
		For MV_RANGE = 1:
		VSET_ULS => 0.010V * m + 0.160V, where m = <7:0>

#### 0x0001236A S6\_CTRL\_ULS\_VALID

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: PERPH\_RB

#### S6\_CTRL\_ULS\_VALID

Bits	Name	Description
7:0	ULS_VALID	Readback the valid upper limit stop value

### 0x0001236B S6\_CTRL\_VSET\_LLS

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC GANGED, PMIC LOCKED=SEC ACCESS

#### S6\_CTRL\_VSET\_LLS

Bits	Name	Description
7:0	VSET_LLS	If LL_EN is asserted, and VSET is set to a value less than or equal to VSET_LLS, LLS_FLAG and VREG_READY_INT are asserted For MV_RANGE = 0:  VSET_LLS => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1:  VSET_LLS => 0.010V * m + 0.160V, where m = <7:0>

## 0x0001236C S6\_CTRL\_LLS\_VALID

**Type:** R

Clock: PBUS\_WRCLK
Reset State: Undefined
Reset Name: PERPH RB

#### S6\_CTRL\_LLS\_VALID

Bits	Name	Description
7:0	LLS_VALID	Readback the valid lower limit stop value

# 0x0001236D S6\_CTRL\_GPL\_HI

Type: RW

Clock: PBUS\_WRCLK Reset State: 0xFF

Reset Name: PERPH\_RB

PMIC\_GANGED, PMIC\_LOCKED=SEC\_ACCESS

## S6\_CTRL\_GPL\_HI

Bits	Name	Description
7:0	VSET_GPL_HI	When output voltage setpoint reaches a value greater than or equal to VSET_GPL_HI, set GPL_HI_FLAG and VREG_READY_INT For MV_RANGE = 0: VSET_GPL_HI => 0.005V * m + 0.080V, where m = <7:0> For MV_RANGE = 1: VSET_GPL_HI => 0.010V * m + 0.160V, where m = <7:0>

#### 0x0001236E S6\_CTRL\_GPL\_LO

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_GANGED, PMIC\_LOCKED=SEC\_ACCESS

#### S6\_CTRL\_GPL\_LO

Bits	Name	Description
7:0	VSET_GPL_LO	When output voltage setpoint reaches a value less than or equal to VSET_GPL_LO value, set GPL_LO_FLAG and VREG_READY_INT For MV_RANGE = 0: VSET_GPL_LO => 0.005V * m + 0.80V, where m = <7:0> For MV_RANGE = 1: VSET_GPL_LO => 0.010V * m + 0.160V, where m = <7:0>

#### 0x000123C0 S6\_CTRL\_GANG\_CTL1

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x23

Reset Name: shutdown2 rb

PMIC\_LOCKED=SEC ACCESS

#### S6\_CTRL\_GANG\_CTL1

Bits	Name	Description
7:0	GANG_LEADER_PID	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

# 0x000123C1 S6\_CTRL\_GANG\_CTL2

Type: RW

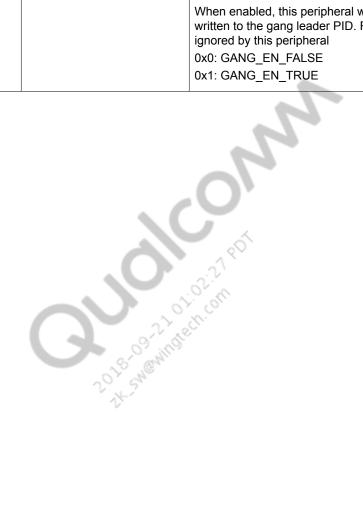
Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: shutdown2 rb

PMIC\_LOCKED=SEC\_ACCESS

#### S6\_CTRL\_GANG\_CTL2

Bits	Name	Description
7	GANG_EN	0 = disable
		1 = enable
		When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral
		0x0: GANG_EN_FALSE
		0x1: GANG_EN_TRUE



# 57 Fts2p5\_ps Registers

#### 0x00012400 S6\_PS\_REVISION1

#### S6\_PS\_REVISION1

S6_P5	S_REVISION1			
Clock:	Type: R Clock: PBUS_WRCLK Reset State: 0x02			
Reset N	Name: N/A			
HW Ve	rsion Register [7:0]	- of		
PMIC_	CONSTANT	2.21		
S6_PS_	S6_PS_REVISION1			
Bits	Name	Description		
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software.  Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.		

#### 0x00012401 S6\_PS\_REVISION2

**Type:** R

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### S6\_PS\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00012402 S6\_PS\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [23:16]

#### S6\_PS\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software.
		Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00012403 S6\_PS\_REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [31:24]

#### S6\_PS\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 

Type: R

Clock: PBUS\_WRCLK Reset State: 0x1C

Reset Name: N/A

Peripheral Type

PMIC\_CONSTANT

#### S6\_PS\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	

#### 0x00012405 S6\_PS\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x04

Reset Name: N/A

Peripheral SubType

#### S6\_PS\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	180

JUNG

# 0x00012440 S6\_PS\_VOLTAGE\_CTL1

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC GANGED, PMIC LATCHED WRITE=VOLTAGE CTL2

# S6\_PS\_VOLTAGE\_CTL1

Bits	Name	Description
0	MV_RANGE	0 = Use low voltage range as specified by VSET and PFM_VOFFSET
		1 = Use medium voltage range as specified by VSET and PFM_VOFFSET
		0x0: LV_RANGE
		0x1: MV_RANGE

#### 

Type: RW

Clock: PBUS\_WRCLK Reset State: 0xC2

Reset Name: PERPH RB

PMIC GANGED

#### S6\_PS\_VOLTAGE\_CTL2

Bits	Name	Description
7:0	VSET	Output voltage set point in PWM mode and in PFM mode
		For MV_RANGE = 0:
		VSET => 0.005V * m + 0.080V, where m = <7:0>
		For MV_RANGE = 1:
		VSET => $0.010V * m + 0.160V$ , where $m = <7:0>$
	.\(	If PFM_VOFFSET_EN is asserted and in PFM mode, add PFM_VOFFSET

# 0x00012445 S6\_PS\_MODE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH RB

PMIC GANGED

#### S6\_PS\_MODE\_CTL

Bits	Name	Description
7	NPM	FTS NON-AUTO mode control
		0 = Low power mode (LPM) unless AUTO_MODE is asserted
		1 = Normal power mode (PWM)
		0x0: NPM_NOT_FORCED
		0x1: NPM_FORCED_IF_ENABL
6	AUTO_MODE	When NPM is not asserted, FTS automatically enters and exits low power mode (PFM) based on load current qualifying triggers
		0 = AUTO mode is disabled
		1 = AUTO mode is enabled
		0x0: AUTO_MODE_FALSE
		0x1: AUTO_MODE_TRUE

# 0x00012450 S6\_PS\_FREQ\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x05

Reset Name: PERPH\_RB

PMIC\_GANGED, PMIC\_LOCKED=SEC\_ACCESS

#### S6\_PS\_FREQ\_CTL

Bits	Name	Description
3:0	FREQ_CTL	Clock frequency = 19.2MHz / (CLK_DIV + 1)
		FTS2.5 buck supports 0.8, 1.6, 3.2,4.8, and 6.4 MHz
		0000 = Not supported
		0001 = Not supported
		0010 = 6.4MHz
		0011 = 4.8MHz
		0100 = Not supported
		0101 = 3.2MHz
		0110 = Not supported
		0111 = Not supported
		1000 = Not supported
	2.5	1001 = Not supported
	00'0118	1010 = Not supported
	C. Capille	1011 = 1.6MHz
	O' Me	1100 = Not supported
	2018-09 winds	1101 = Not supported
	V	1110 = Not supported
		1111 = Not supported
		0x2: FS_6M4HZ
		0x3: FS_4M8HZ
		0x5: FS_3M2MHZ
		0xB: FS_1M6MHZ

#### 

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

#### S6\_PS\_PHASE\_ID

Bits	Name	Description
3:0	PHASE_ID	Unique phase identifier. If less than or equal to PHASE_CNT_MAX, phase is active. If greater than PHASE_CNT_MAX, phase is inactive.
		0x0: PHASE_NUMBER_1 0x1: PHASE_NUMBER_2
		0x2: PHASE_NUMBER_3 0x3: PHASE_NUMBER_4

#### 0x00012454 S6\_PS\_PHASE\_CNT\_MAX

#### S6\_PS\_PHASE\_CNT\_MAX

S6_PS_PHASE_CNT_MAX					
Type: RW Clock: PBUS_WRCLK Reset State: 0x00					
Reset Name: PER	Reset Name: PERPH_RB				
PMIC_GANGED	PMIC_GANGED				
		2.1			
S6_PS_PHASE_C	S6_PS_PHASE_CNT_MAX				
Bits	Name	Description			
3:0 PHASE_CI	NT_MAX	Sets the maximum number of phases that the autonomous phase controller (APC) can use. If greater than or equal to PHASE ID,			
	J. 40.	the autonomous phase controller may or may not keep the phase			

#### 0x000124C0 S6\_PS\_GANG\_CTL1

Type: RW

Clock: PBUS WRCLK **Reset State:** 0x23

Reset Name: shutdown2 rb

PMIC LOCKED=SEC ACCESS

#### S6\_PS\_GANG\_CTL1

Bits	Name	Description
7:0	GANG_LEADER_PID	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID.  Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

#### 

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: shutdown2 rb

PMIC LOCKED=SEC ACCESS

#### S6\_PS\_GANG\_CTL2

Bits	Name	Description
7	GANG_EN	0 = disable
		1 = enable
		When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral 0x0: GANG_EN_FALSE
		0x1: GANG_EN_TRUE
	2018-09-21-03	in con

# 58 Bclk\_gen\_clk Registers

### 0x00012500 S6\_FREQ\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

# S6\_FREQ\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

#### 

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: N/A

HW Version Register [15:8]

#### S6\_FREQ\_REVISION2

Bit	S Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00012504 S6\_FREQ\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x1D

Reset Name: N/A

Peripheral Type

#### S6\_FREQ\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	BCLK GEN

#### 0x00012505 S6\_FREQ\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x19 Reset Name: N/A

Peripheral SubType

### S6\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	BCLK GEN CLK

#### 0x00012546 S6\_FREQ\_CLK\_ENABLE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

#### S6\_FREQ\_CLK\_ENABLE

Bits	Name	Description
7	EN_CLK_INT	0 = do not force the clock on
		1 = enable the clock
		0x0: FORCE_EN_DISABLED
		0x1: FORCE_EN_ENABLED

#### S6\_FREQ\_CLK\_ENABLE (cont.)

Bits	Name	Description
0	FOLLOW_CLK_SX_REQ	0 = ignore smps_clk_req <x></x>
		1 = clock is enabled when the clocks request is high smps_clk_req <x>='1'</x>
		0x0: FALLOW_CLK_REQ_DISABLED
		0x1: FALLOW_CLK_REQ_ENABLED

# 0x00012550 S6\_FREQ\_CLK\_DIV

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x05

Reset Name: PERPH\_RB

PMIC LOCKED=SEC ACCESS, PMIC GANGED

# S6\_FREQ\_CLK\_DIV

Bits	Name	Description
3:0	CLK_DIV	clock_ frequency = 19.2MHz / (CLK_DIV + 1)
		FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz
	0,1 1,5	HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz
	.O. ville	CLK_DIV = 0 is not supported, it will generate 9.6 MHz
	2018. 24 Chillip	0x0: FREQ_9M6HZ_0
	2.5	0x1: FREQ_9M6HZ
	1	0x2: FREQ_6M4HZ
		0x3: FREQ_4M8HZ
		0x4: FREQ_3M8HZ
		0x5: FREQ_3M2HZ
		0x6: FREQ_2M7HZ
		0x7: FREQ_2M4HZ
		0x8: FREQ_2M1HZ
		0x9: FREQ_1M9HZ
		0xA: FREQ_1M7HZ
		0xB: FREQ_1M6HZ
		0xC: FREQ_1M5HZ
		0xD: FREQ_1M4HZ
		0xE: FREQ_1M3HZ
		0xF: FREQ_1M2HZ

### 0x00012551 S6\_FREQ\_CLK\_PHASE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x0B

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S6\_FREQ\_CLK\_PHASE

Bits	Name	Description
3:0	CLK_PHASE	Distributed clock phase select:
		clock phase delay = clock period * (CLK_PHASE / 16)

# 0x000125C0 S6\_FREQ\_GANG\_CTL1

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x23

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### S6\_FREQ\_GANG\_CTL1

Bits	Name	Description
7:0	GANG_LEADER_PID	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

# 0x000125C1 S6\_FREQ\_GANG\_CTL2

Type: RW

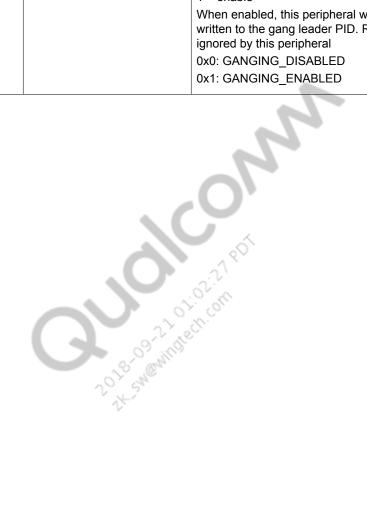
Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

#### S6\_FREQ\_GANG\_CTL2

Bits	Name	Description
7	GANG_EN	0 = disable
		1 = enable
		When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral
		0x0: GANGING_DISABLED
		0x1: GANGING_ENABLED



# 59 Ldo\_ult\_stepper\_dig Registers

## 0x00014000 LDO1\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO1\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00014001 LDO1\_REVISION2

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO1\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

# 0x00014002 LDO1\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: n/a

HW Version Register [23:16]

### LDO1\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00014003 LDO1\_REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: n/a

HW Version Register [31:24]

### LDO1\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

# 0x00014004 LDO1\_PERPH\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC\_CONSTANT

## LDO1\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	ULT LDO

# 0x00014005 LDO1\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x07

Reset Name: n/a

Peripheral SubType

### LDO1\_PERPH\_SUBTYPE

E	Bits	Name	Description
	7:0	SUBTYPE	N300_stepper: 0x15; N600_stepper: 0x06; N900_stepper: 0x14; N1200_stepper: 0x07

SINN

# 0x00014008 LDO1\_STATUS1

Type: R

Clock: PBUS\_WRCLK
Reset State: 0bXXXXXXX1

Reset Name: n/a

Status Registers

# LDO1\_STATUS1

Bits	Name	Description
7	VREG_OK	0 = VREG output voltage is below VREG_OK threshold, 1 = VREG output voltage is above VREG_OK threshold. VREG_OK is also high when LDO is in bypass mode 0x1: LDO_VOLTAGE_OK 0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	1 = VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

### LDO1\_STATUS1 (cont.)

Bits	Name	Description
0	STEPPER_DONE	indicates if LDO voltage steppering is done 0x1: STEPPER_DONE 0x0: STEPPER_NOT_DONE

#### 0x00014009 LDO1\_STATUS2

#### LDO1\_STATUS2

LDO1_STATUS2				
Clock:	Type: R Clock: PBUS_WRCLK Reset State: 0x00			
Reset N	Reset Name: n/a			
Status 1	Registers			
LDO1_	STATUS2			
Bits	Name	Description		
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode		
	.07	0x1: SOFTSTART_DONE 0x0: SOFTSTART_NOT_DONE		

#### 0x00014010 LDO1\_INT\_RT\_STS

Type: R

Clock: PBUS WRCLK **Reset State:** 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO1\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_ERR

# 0x00014011 LDO1\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO1\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level
		0x1: VREG_OK_LEVEL_TRIGGERED
		0x0: VREG_OK_EDGE_TRIGGERED

# 0x00014012 LDO1\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### **LDO1 INT POLARITY HIGH**

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	Oliche	0x1: VREG_OK_LOW_TRIGGERED
	7	0x0: VREG_OK_LOW_DISABLED

# 0x00014013 LDO1\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

### LDO1\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

## 0x00014014 LDO1\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

### LDO1\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

# 0x00014015 LDO1\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO1\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

# 0x00014016 LDO1\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

## LDO1\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

# 0x00014018 LDO1\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### LDO1\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27	0x0: LDO_VOLTAGE_OK
		P. Control of the Con

# 0x00014019 LDO1\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

### LDO1\_INT\_PENDING\_STS

E	Bits	Name	Description
	0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

# 0x0001401A LDO1\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO1\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

# 0x0001401B LDO1\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

# LDO1\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

# 0x00014041 LDO1\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x32

Reset Name: perph rb

Register for voltage programming bits going to LDO.

#### LDO1\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep). Vmin and Vsetp are minimal voltage and voltage step size, respectively. For ULT NMOS LDOs, Vmin=375mV, Vstep=12.5mV.

# 0x00014045 LDO1\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions. This register needs to be 0x00 for putting LDO in LPM.

# LDO1\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM 0x1: FORCED_NPM 0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	LDO is in active bypass mode when both BYPASS_ACT and BYPASS_EN are set to 1, while NPM is set to 0 0x1: BYPASS_ACT_TRUE 0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode 0x1: BYPASS_ENABLED 0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	1' = (LDO is in NPM when PMIC_AWAKE (SLEEP_B) = '1') or (has no effect on LDO operation mode when PMIC_AWAKE = '0'), '0' = has no effect on LDO operation mode no matter PMIC_AWAKE is 0 or 1  0x1: FOLLOW_PMIC_AWAKE_TRUE  0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00014046 LDO1\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

Enable control register.

# LDO1\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE

#### LDO1\_EN\_CTL (cont.)

Bits	Name	Description
0	FOLLOW_HW_EN0	NPM enable setting using HWEN0
		0x1: FOLLOW_HW_EN0_TRUE
		0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014048 LDO1\_PD\_CTL

### LDO1\_PD\_CTL

Type: RW Clock: PBUS_WRCLK Reset State: 0x80		
Reset Name: perph_rb		
LDO pulldown control		40
LDO1_	PD_CTL	
Bits	Name	Description
7	PULLDN_EN	1' = Enable the pulldown when the regulator is disabled, '0' = pulldown is always disabled.
		0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

# 0x0001404C LDO1\_SOFT\_START\_CTL

Type: RW

Clock: PBUS WRCLK Reset State: 0x80

Reset Name: perph\_rb

Soft start control register

### LDO1\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	1' = Enable LDO softstart function, '0' = Disable LDO softstart function.  0x1: SOFT_START_ENABLED  0x0: SOFT_START_DISABLED

# 0x00014052 LDO1\_CONFIG\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x04

Reset Name: perph rb

Config control register.

# LDO1\_CONFIG\_CTL

Bits	Name	Description
3	ACT_BYPASS_BUFF_EN	1' = LDO buffer stage is enabled when LDO is in active bypass mode, '0' = LDO buffer stage is disabled when LDO is in active bypass mode.  0x1: ACT_BYPASS_BUFF_ENABLED  0x0: ACT_BYPASS_BUFF_DISABLED
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM-LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED

# 0x00014061 LDO1\_VS\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x85

Reset Name: perph rb

LDO voltage stepper control register. NMOS LDO use only.

# LDO1\_VS\_CTL

Bits	Name	Description
7	VS_EN	Enables the stepper
		0x1: STEPPER_ENABLED
		0x0: STEPPER_DIABLED

### LDO1\_VS\_CTL (cont.)

Bits	Name	Description
2:0	VS_DELAY	Delay (clk_in = 19.2 MHz) -000 = 20 clock cycles (delay of 1 us) - 001 = 40 clock cycles (delay of 2 us) -010 = 80 clock cycles (delay of 4.1 us) -011 = 160 clock cycles (delay of 8.3 us) -100 = 320 clock cycles (delay of 16.6 us) -101 = 640 clock cycles (delay of 33.3 us) -110 = 1280 clock cycles (delay of 67 us) -111 = 2560 clock cycles (delay of 134 us) 0x7: DELAY_1_2560 0x6: DELAY_1_1280 0x5: DELAY_1_640 0x4: DELAY_1_320 0x3: DELAY_1_160 0x2: DELAY_1_80
		0x1: DELAY_1_40 0x0: DELAY_1_20

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# 60 Ldo\_ult\_stepper\_dig Registers

# 0x00014100 LDO2\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

### LDO2\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00014101 LDO2\_REVISION2

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

### LDO2\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

# 0x00014102 LDO2\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: n/a

HW Version Register [23:16]

#### LDO2\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00014103 LDO2 REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: n/a

HW Version Register [31:24]

#### LDO2\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

# 0x00014104 LDO2\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

### LDO2\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	ULT LDO

# 0x00014105 LDO2\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x07

Reset Name: n/a

Peripheral SubType

### LDO2\_PERPH\_SUBTYPE

E	Bits	Name	Description
	7:0	SUBTYPE	N300_stepper: 0x15; N600_stepper: 0x06; N900_stepper: 0x14; N1200_stepper: 0x07

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# 0x00014108 LDO2\_STATUS1

Type: R

Clock: PBUS\_WRCLK
Reset State: 0bXXXXXXX1

Reset Name: n/a

Status Registers

### LDO2\_STATUS1

Bits	Name	Description
7	VREG_OK	0 = VREG output voltage is below VREG_OK threshold, 1 = VREG output voltage is above VREG_OK threshold. VREG_OK is also high when LDO is in bypass mode 0x1: LDO_VOLTAGE_OK 0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode  0x1: ON_AND_BYPASSED  0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	1 = VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

### LDO2\_STATUS1 (cont.)

Bits	Name	Description
0	STEPPER_DONE	indicates if LDO voltage steppering is done 0x1: STEPPER_DONE 0x0: STEPPER_NOT_DONE

#### 0x00014109 LDO2\_STATUS2

### LDO2\_STATUS2

LDO2	_STATUS2	
	R PBUS_WRCLK State: 0x00	
Reset I	Name: n/a	
Status 1	Registers	
LDO2_	STATUS2	
Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
	.07	0x1: SOFTSTART_DONE 0x0: SOFTSTART_NOT_DONE

#### 0x00014110 LDO2\_INT\_RT\_STS

Type: R

Clock: PBUS WRCLK **Reset State:** 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO2\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_ERR

# 0x00014111 LDO2\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

### LDO2\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level
		0x1: VREG_OK_LEVEL_TRIGGERED
		0x0: VREG_OK_EDGE_TRIGGERED

# 0x00014112 LDO2\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

### LDO2\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

# 0x00014113 LDO2\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

### LDO2\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

## 0x00014114 LDO2\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO2\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

# 0x00014115 LDO2\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO2\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

# 0x00014116 LDO2\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

## LDO2\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

# 0x00014118 LDO2\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

# LDO2\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

# 0x00014119 LDO2\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

# LDO2\_INT\_PENDING\_STS

E	Bits	Name	Description
	0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

# 0x0001411A LDO2\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO2\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

# 0x0001411B LDO2\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

# LDO2\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

### 0x00014141 LDO2\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x42

Reset Name: perph rb

Register for voltage programming bits going to LDO.

#### LDO2\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep). Vmin and Vsetp are minimal voltage and voltage step size, respectively. For ULT NMOS LDOs, Vmin=375mV, Vstep=12.5mV.

# 0x00014145 LDO2\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions. This register needs to be 0x00 for putting LDO in LPM.

# LDO2\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM 0x1: FORCED_NPM 0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	LDO is in active bypass mode when both BYPASS_ACT and BYPASS_EN are set to 1, while NPM is set to 0 0x1: BYPASS_ACT_TRUE 0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode 0x1: BYPASS_ENABLED 0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	1' = (LDO is in NPM when PMIC_AWAKE (SLEEP_B) = '1') or (has no effect on LDO operation mode when PMIC_AWAKE = '0'), '0' = has no effect on LDO operation mode no matter PMIC_AWAKE is 0 or 1  0x1: FOLLOW_PMIC_AWAKE_TRUE  0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00014146 LDO2\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Enable control register.

# LDO2\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE

### LDO2\_EN\_CTL (cont.)

Bits	Name	Description
0	FOLLOW_HW_EN0	NPM enable setting using HWEN0
		0x1: FOLLOW_HW_EN0_TRUE
		0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014148 LDO2\_PD\_CTL

### LDO2\_PD\_CTL

LDO2_PD_CTL			
RW PBUS_WRCLK tate: 0x80			
ame: perph_rb			
lldown control	-O/-		
PD_CTL			
Name	Description		
PULLDN_EN	1' = Enable the pulldown when the regulator is disabled, '0' = pulldown is always disabled.  0x1: PULLDN_ENABLED  0x0: PULLDN_DIABLED		
] [	RW PBUS_WRCLK tate: 0x80  ame: perph_rb  Ildown control  PD_CTL  Name		

# 0x0001414C LDO2\_SOFT\_START\_CTL

Type: RW

Clock: PBUS WRCLK Reset State: 0x80

Reset Name: perph\_rb

Soft start control register

### LDO2\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	1' = Enable LDO softstart function, '0' = Disable LDO softstart function.  0x1: SOFT_START_ENABLED  0x0: SOFT_START_DISABLED

# 0x00014152 LDO2\_CONFIG\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x04

Reset Name: perph rb

Config control register.

### LDO2\_CONFIG\_CTL

Bits	Name	Description
3	ACT_BYPASS_BUFF_EN	1' = LDO buffer stage is enabled when LDO is in active bypass mode, '0' = LDO buffer stage is disabled when LDO is in active bypass mode.  0x1: ACT_BYPASS_BUFF_ENABLED  0x0: ACT_BYPASS_BUFF_DISABLED
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM-LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED

# 0x00014161 LDO2\_VS\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x85

Reset Name: perph rb

LDO voltage stepper control register. NMOS LDO use only.

# LDO2\_VS\_CTL

Bits	Name	Description
7	VS_EN	Enables the stepper
		0x1: STEPPER_ENABLED 0x0: STEPPER_DIABLED

### LDO2\_VS\_CTL (cont.)

Bits	Name	Description
2:0	VS_DELAY	Delay (clk_in = 19.2 MHz) -000 = 20 clock cycles (delay of 1 us) - 001 = 40 clock cycles (delay of 2 us) -010 = 80 clock cycles (delay of 4.1 us) -011 = 160 clock cycles (delay of 8.3 us) -100 = 320 clock cycles (delay of 16.6 us) -101 = 640 clock cycles (delay of 33.3 us) -110 = 1280 clock cycles (delay of 67 us) -111 = 2560 clock cycles (delay of 134 us) 0x7: DELAY_1_2560 0x6: DELAY_1_1280 0x5: DELAY_1_640 0x4: DELAY_1_320 0x3: DELAY_1_160 0x2: DELAY_1_80 0x1: DELAY_1_40
		0x0: DELAY_1_20

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# 61 Ldo\_ult\_stepper\_dig Registers

# 0x00014200 LDO3\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

### LDO3\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00014201 LDO3\_REVISION2

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

### LDO3\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

# 0x00014202 LDO3\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: n/a

HW Version Register [23:16]

#### LDO3\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00014203 LDO3\_REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: n/a

HW Version Register [31:24]

#### LDO3\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

# 0x00014204 LDO3\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

### LDO3\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	ULT LDO

# 0x00014205 LDO3\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x07

Reset Name: n/a

Peripheral SubType

### LDO3\_PERPH\_SUBTYPE

E	Bits	Name	Description
	7:0	SUBTYPE	N300_stepper: 0x15; N600_stepper: 0x06; N900_stepper: 0x14; N1200_stepper: 0x07

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# 0x00014208 LDO3\_STATUS1

Type: R

Clock: PBUS\_WRCLK
Reset State: 0bXXXXXXX1

Reset Name: n/a

Status Registers

# LDO3\_STATUS1

Bits	Name	Description
7	VREG_OK	0 = VREG output voltage is below VREG_OK threshold, 1 = VREG output voltage is above VREG_OK threshold. VREG_OK is also high when LDO is in bypass mode 0x1: LDO_VOLTAGE_OK 0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	1 = VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

### LDO3\_STATUS1 (cont.)

Bits	Name	Description
0	STEPPER_DONE	indicates if LDO voltage steppering is done 0x1: STEPPER_DONE 0x0: STEPPER_NOT_DONE

#### 0x00014209 LDO3\_STATUS2

#### LDO3\_STATUS2

LDO3_STATUS2			
	R PBUS_WRCLK State: 0x00		
Reset 1	Name: n/a		
Status 1	Registers		
LDO3_	STATUS2		
Bits	Name	Description	
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode 0x1: SOFTSTART_DONE 0x0: SOFTSTART_NOT_DONE	
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF	

#### 0x00014210 LDO3\_INT\_RT\_STS

Type: R

Clock: PBUS WRCLK **Reset State:** 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO3\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_ERR

# 0x00014211 LDO3\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO3\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level
		0x1: VREG_OK_LEVEL_TRIGGERED
		0x0: VREG_OK_EDGE_TRIGGERED

# 0x00014212 LDO3\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

### LDO3\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

# 0x00014213 LDO3\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

### LDO3\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

# 0x00014214 LDO3\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO3\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

## 0x00014215 LDO3\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO3\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

# 0x00014216 LDO3\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

## LDO3\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED 0x0: VREG_OK_ERROR_DISABLED
		UXU. VREG_OK_ERROR_DISABLED

# 0x00014218 LDO3\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

## LDO3\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

# 0x00014219 LDO3\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

### LDO3\_INT\_PENDING\_STS

E	Bits	Name	Description
	0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

# 0x0001421A LDO3\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO3\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

# 0x0001421B LDO3\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

# LDO3\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

# 0x00014241 LDO3\_VOLTAGE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x44

Reset Name: perph rb

Register for voltage programming bits going to LDO.

#### LDO3\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep). Vmin and Vsetp are minimal voltage and voltage step size, respectively. For ULT NMOS LDOs, Vmin=375mV, Vstep=12.5mV.

# 0x00014245 LDO3\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions. This register needs to be 0x00 for putting LDO in LPM.

# LDO3\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM 0x1: FORCED_NPM 0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	LDO is in active bypass mode when both BYPASS_ACT and BYPASS_EN are set to 1, while NPM is set to 0 0x1: BYPASS_ACT_TRUE 0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode 0x1: BYPASS_ENABLED 0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	1' = (LDO is in NPM when PMIC_AWAKE (SLEEP_B) = '1') or (has no effect on LDO operation mode when PMIC_AWAKE = '0'), '0' = has no effect on LDO operation mode no matter PMIC_AWAKE is 0 or 1  0x1: FOLLOW_PMIC_AWAKE_TRUE  0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00014246 LDO3\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Enable control register.

# LDO3\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE

## LDO3\_EN\_CTL (cont.)

	Bits	Name	Description
Г	0	FOLLOW_HW_EN0	NPM enable setting using HWEN0
			0x1: FOLLOW_HW_EN0_TRUE
			0x0: FOLLOW_HW_EN0_FALSE
-1			

# 0x00014248 LDO3\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

LDO pulldown control

### LDO3\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	1' = Enable the pulldown when the regulator is disabled, '0' = pulldown is always disabled.  0x1: PULLDN_ENABLED  0x0: PULLDN_DIABLED

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# 0x0001424C LDO3\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph\_rb

Soft start control register

### LDO3\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	1' = Enable LDO softstart function, '0' = Disable LDO softstart function.  0x1: SOFT_START_ENABLED  0x0: SOFT_START_DISABLED

# 0x00014252 LDO3\_CONFIG\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x04

Reset Name: perph rb

Config control register.

# LDO3\_CONFIG\_CTL

Bits	Name	Description
3	ACT_BYPASS_BUFF_EN	1' = LDO buffer stage is enabled when LDO is in active bypass mode, '0' = LDO buffer stage is disabled when LDO is in active bypass mode.  0x1: ACT_BYPASS_BUFF_ENABLED  0x0: ACT_BYPASS_BUFF_DISABLED
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM-LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED

# 0x00014261 LDO3\_VS\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x85

Reset Name: perph rb

LDO voltage stepper control register. NMOS LDO use only.

# LDO3\_VS\_CTL

Bits	Name	Description
7	VS_EN	Enables the stepper
		0x1: STEPPER_ENABLED
		0x0: STEPPER_DIABLED

### LDO3\_VS\_CTL (cont.)

Bits	Name	Description
2:0	VS_DELAY	Delay (clk_in = 19.2 MHz) -000 = 20 clock cycles (delay of 1 us) - 001 = 40 clock cycles (delay of 2 us) -010 = 80 clock cycles (delay of 4.1 us) -011 = 160 clock cycles (delay of 8.3 us) -100 = 320 clock cycles (delay of 16.6 us) -101 = 640 clock cycles (delay of 33.3 us) -110 = 1280 clock cycles (delay of 67 us) -111 = 2560 clock cycles (delay of 134 us) 0x7: DELAY_1_2560 0x6: DELAY_1_1280 0x5: DELAY_1_640 0x4: DELAY_1_320 0x3: DELAY_1_160 0x2: DELAY_1_80
		0x1: DELAY_1_40 0x0: DELAY_1_20

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# 62 Ldo\_ult\_dig Registers

# 0x00014300 LDO4\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

### LDO4\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00014301 LDO4\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

### LDO4\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00014302 LDO4\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO4\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014303 LDO4 REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO4\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 0x00014304 LDO4\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

#### LDO4\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00014305 LDO4\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x2D

Reset Name: n/a

Peripheral SubType

#### LDO4\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

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#### 0x00014308 LDO4\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

#### LDO4\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

#### 0x00014309 LDO4\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

#### LDO4\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

# 0x00014310 LDO4\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO4\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

#### 0x00014311 LDO4\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO4\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level
		0x1: VREG_OK_LEVEL_TRIGGERED
		0x0: VREG_OK_EDGE_TRIGGERED

# 0x00014312 LDO4\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### LDO4\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	245	0x0: VREG_OK_LOW_DISABLED

#### 0x00014313 LDO4\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO4\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true  0x1: VREG_OK_RISING_TRIGGERED  0x0: VREG_OK_FALLING_TRIGGERED

#### 0x00014314 LDO4\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO4\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

#### 0x00014315 LDO4\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO4\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014316 LDO4\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### LDO4\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014318 LDO4\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### LDO4\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

#### 0x00014319 LDO4\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

#### LDO4\_INT\_PENDING\_STS

Bits	Name	Description
0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

#### 0x0001431A LDO4\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO4\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

#### 0x0001431B LDO4\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### LDO4\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

#### 0x00014341 LDO4\_VOLTAGE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x04

Reset Name: perph\_rb

#### LDO4\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep).
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

## 0x00014345 LDO4\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions

#### LDO4\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE
		0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode
		0x1: BYPASS_ENABLED
		0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B)
	0	0x1: FOLLOW_PMIC_AWAKE_TRUE
	277	0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00014346 LDO4\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### LDO4\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014348 LDO4\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO4\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED
		0x0: PULLDN_DIABLED

## 0x0001434A LDO4\_OCP\_CTL1

#### LDO4\_OCP\_CTL1

LDO4	_OCP_CTL1			
Type: RW Clock: PBUS_WRCLK Reset State: 0x80				
Reset 1	Reset Name: perph_rb			
LDO4_	LDO4_OCP_CTL1			
Bits	Name	Description		
7	OCP_EN	Enable the OCP feature		
	O'TO ME	0x1: OCP_ENABLED		
	27 9	O.O. OOD DIADIED		
	1	0x0: OCP_DIABLED		
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)		
5	OCP_TEST_MODE	_		
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)		

#### 0x0001434B LDO4\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO4\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

## 0x0001434C LDO4\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO4\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED

#### 0x00014352 LDO4\_CONFIG\_CTL

#### LDO4\_CONFIG\_CTL

LDO4	_CONFIG_CTL			
Clock: Reset S	Type: RW Clock: PBUS_WRCLK Reset State: 0x04  Reset Name: perph rb			
IXCSCI 1	value. perpii_10			
LDO4_	LDO4_CONFIG_CTL			
Bits	Name	Description		
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED 0x0: ACT_BYPASS_BUFF_DISABLED		
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED		

# 63 Ldo\_ult\_dig Registers

#### 0x00014400 LDO5\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO5\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014401 LDO5\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO5\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00014402 LDO5\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO5\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014403 LDO5 REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO5\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 0x00014404 LDO5\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC\_CONSTANT

#### LDO5\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00014405 LDO5\_PERPH\_SUBTYPE

Type: R

#### LDO5\_PERPH\_SUBTYPE

	PBUS_WRCLK State: 0x2A	
Reset Name: n/a		
Peripheral SubType		M.
LDO5_	PERPH_SUBTYPE	-01
Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV P50: 0x28; LV P150: 0x29; LV P300: 0x2A;

#### LDO5\_STATUS1 0x00014408

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

#### LDO5\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

## 0x00014409 LDO5\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

## LDO5\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

## 0x00014410 LDO5\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO5\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

#### 0x00014411 LDO5\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO5\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level
		0x1: VREG_OK_LEVEL_TRIGGERED
		0x0: VREG_OK_EDGE_TRIGGERED

# 0x00014412 LDO5\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### LDO5\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

#### 0x00014413 LDO5\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO5\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true  0x1: VREG_OK_RISING_TRIGGERED  0x0: VREG_OK_FALLING_TRIGGERED

#### 0x00014414 LDO5\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO5\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

#### 0x00014415 LDO5\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO5\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014416 LDO5\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### LDO5\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014418 LDO5\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### LDO5\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

#### 0x00014419 LDO5\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

#### LDO5\_INT\_PENDING\_STS

E	Bits	Name	Description
	0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

#### 0x0001441A LDO5\_INT\_MID\_SEL

Type: RW

Clock: PBUS WRCLK **Reset State:** 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO5\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

#### 0x0001441B LDO5\_INT\_PRIORITY

Type: RW

Clock: PBUS WRCLK Reset State: 0x00 Reset Name: perph rb

#### LDO5\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

#### 0x00014441 LDO5\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x04

Reset Name: perph rb

#### LDO5\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

#### LDO5\_MODE\_CTL2 0x00014445

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions

#### LDO5\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM 0x1: FORCED_NPM 0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE 0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode 0x1: BYPASS_ENABLED 0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B) 0x1: FOLLOW_PMIC_AWAKE_TRUE 0x0: FOLLOW_PMIC_AWAKE_FALSE
LDO5_EN_CTL		
Type:	RW	

## 0x00014446

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO5\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014448 LDO5\_PD\_CTL

**Type:** RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO5\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

## 0x0001444A LDO5\_OCP\_CTL1

#### LDO5\_OCP\_CTL1

LDO5	LDO5_OCP_CTL1		
Clock: Reset S	Type: RW Clock: PBUS_WRCLK Reset State: 0x80		
Reset I	Name: perph_rb	2.1	
LDO5_	LDO5_OCP_CTL1		
Bits	Name	Description	
7	OCP_EN	Enable the OCP feature	
	To Me	0x1: OCP_ENABLED	
	77.5	0x0: OCP_DIABLED	
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)	
		0x1: OCP_TEST_MODE	
		0x0: OCP_NORMAL_MODE	

#### 0x0001444B LDO5\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO5\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

#### 0x0001444C LDO5\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO5\_SOFT\_START\_CTL

Bits	Name	Description	
7	SOFT_START	0x1: SOFT_START_ENABLED	
		0x0: SOFT_START_DISABLED	
LDO5	_CONFIG_CTL		
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x04		
Reset 1	Reset Name: perph_rb		
LDO5_CONFIG_CTL			
Bits	Name	Description	
3	ACT RYPASS BLIEF EN	0v1: ACT RVDASS BLIFE ENABLED	

#### 0x00014452 LDO5\_CONFIG\_CTL

# LDO5\_CONFIG\_CTL

Bits	Name	Description
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED
	8. Online	0x0: ACT_BYPASS_BUFF_DISABLED
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED

# 64 Ldo\_ult\_dig Registers

#### 0x00014500 LDO6\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO6\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014501 LDO6\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO6\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00014502 LDO6\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO6\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014503 LDO6 REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO6\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 0x00014504 LDO6\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

#### LDO6\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00014505 LDO6\_PERPH\_SUBTYPE

Type: R

#### LDO6\_PERPH\_SUBTYPE

Clock: PBUS_WRCLK Reset State: 0x2A		
Reset Name: n/a		
Peripheral SubType		
LDO6_PERPH_SUBTYPE		·O,
Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

#### LDO6\_STATUS1 0x00014508

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

#### LDO6\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

## 0x00014509 LDO6\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

#### LDO6\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

# 0x00014510 LDO6\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO6\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

#### 0x00014511 LDO6\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO6\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level 0x1: VREG_OK_LEVEL_TRIGGERED 0x0: VREG_OK_EDGE_TRIGGERED

# 0x00014512 LDO6\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### LDO6\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO ME	0x1: VREG_OK_LOW_TRIGGERED
	245	0x0: VREG_OK_LOW_DISABLED

#### 0x00014513 LDO6\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO6\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

#### 0x00014514 LDO6\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO6\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

#### 0x00014515 LDO6\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO6\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014516 LDO6\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### LDO6\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED 0x0: VREG_OK_ERROR_DISABLED

#### 0x00014518 LDO6\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### LDO6\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

#### 0x00014519 LDO6\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

#### LDO6\_INT\_PENDING\_STS

E	Bits	Name	Description
	0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

#### 0x0001451A LDO6\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO6\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

#### 0x0001451B LDO6\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

#### LDO6\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

#### 0x00014541 LDO6\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x04

Reset Name: perph rb

#### LDO6\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

## 0x00014545 LDO6\_MODE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK
Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions

#### LDO6\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE
		0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode
		0x1: BYPASS_ENABLED
		0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B)
	0	0x1: FOLLOW_PMIC_AWAKE_TRUE
	277	0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00014546 LDO6\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### LDO6\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014548 LDO6\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO6\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

## 0x0001454A LDO6\_OCP\_CTL1

#### LDO6\_OCP\_CTL1

LDO6	_OCP_CTL1			
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x80			
Reset N	Name: perph_rb			
LDO6_	LDO6_OCP_CTL1			
Bits	Name	Description		
7	OCP_EN	Enable the OCP feature		
	OFTENE	0x1: OCP_ENABLED		
	1	0x0: OCP_DIABLED		
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)		
		0x1: OCP_TEST_MODE		
		0x0: OCP_NORMAL_MODE		

#### 0x0001454B LDO6\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO6\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

## 0x0001454C LDO6\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO6\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED

#### 0x00014552 LDO6\_CONFIG\_CTL

#### LDO6\_CONFIG\_CTL

LDO6	_CONFIG_CTL	
Type: RW Clock: PBUS_WRCLK Reset State: 0x04  Reset Name: perph rb		
IXCSCt 1	vame: perpii_10	
LDO6_	CONFIG_CTL	O'm
Bits	Name	Description
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED 0x0: ACT_BYPASS_BUFF_DISABLED
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED

# 65 Ldo\_ult\_dig Registers

#### 0x00014600 LDO7\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO7\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014601 LDO7\_REVISION2

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO7\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00014602 LDO7\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO7\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014603 LDO7 REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO7\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 0x00014604 LDO7\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

#### LDO7\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00014605 LDO7\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x29

Reset Name: n/a

Peripheral SubType

#### LDO7\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

SUNC

# 0x00014608 LDO7\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

#### LDO7\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

#### 0x00014609 LDO7\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

#### LDO7\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

# 0x00014610 LDO7\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO7\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

# 0x00014611 LDO7\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO7\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level
		0x1: VREG_OK_LEVEL_TRIGGERED
		0x0: VREG_OK_EDGE_TRIGGERED

# 0x00014612 LDO7\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### LDO7\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

# 0x00014613 LDO7\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO7\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

# 0x00014614 LDO7\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

## LDO7\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

# 0x00014615 LDO7\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO7\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

# 0x00014616 LDO7\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### LDO7\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED 0x0: VREG_OK_ERROR_DISABLED
		UXU. VREG_OK_ERROR_DISABLED

# 0x00014618 LDO7\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

# LDO7\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

# 0x00014619 LDO7\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

# LDO7\_INT\_PENDING\_STS

Bits	Name	Description
0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

# 0x0001461A LDO7\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO7\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

# 0x0001461B LDO7\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

# LDO7\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

# 0x00014641 LDO7\_VOLTAGE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x04

Reset Name: perph rb

#### LDO7\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

# 0x00014645 LDO7\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions

#### LDO7\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE
		0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode
		0x1: BYPASS_ENABLED
		0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B)
	0	0x1: FOLLOW_PMIC_AWAKE_TRUE
	277	0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00014646 LDO7\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### LDO7\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014648 LDO7\_PD\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

# LDO7\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

# 0x0001464A LDO7\_OCP\_CTL1

#### LDO7\_OCP\_CTL1

		N	
LDO7	_OCP_CTL1		
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x80		
Reset N	Name: perph_rb		
LD07_	OCP_CTL1	ozom m.com	
Bits	Name	Description	
7	OCP_EN	Enable the OCP feature	
	O'TO ME	0x1: OCP_ENABLED	
	2	0x0: OCP_DIABLED	
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)	
		0x1: OCP_TEST_MODE	
		0x0: OCP_NORMAL_MODE	

# 0x0001464B LDO7\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO7\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

# 0x0001464C LDO7\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

#### LDO7\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED
LDO7	_CONFIG_CTL	
	RW PBUS_WRCLK State: 0x04	
Reset 1	Name: perph_rb	2180
LDO7_	CONFIG_CTL	1.02 M
Bits	Name	Description
3	ACT BYDASS BLIEF EN	0v1: ACT RVDASS RIFE ENARIED

#### 0x00014652 LDO7\_CONFIG\_CTL

# LDO7\_CONFIG\_CTL

Bits	Name	Description
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED
	8. Online	0x0: ACT_BYPASS_BUFF_DISABLED
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED

# 66 Ldo\_ult\_dig Registers

# 0x00014700 LDO8\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO8\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00014701 LDO8\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO8\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

# 0x00014702 LDO8\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO8\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00014703 LDO8 REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO8\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

# 0x00014704 LDO8\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

#### LDO8\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00014705 LDO8\_PERPH\_SUBTYPE

Type: R

#### LDO8\_PERPH\_SUBTYPE

	PBUS_WRCLK State: 0x0B	
Reset I	Name: n/a	
Periphe	eral SubType	N
LDO8_	PERPH_SUBTYPE	·O,
Bits	Name	Description

#### LDO8\_STATUS1 0x00014708

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

# LDO8\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

# 0x00014709 LDO8\_STATUS2

Type: R

Clock: PBUS\_WRCLK Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

# LDO8\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

# 0x00014710 LDO8\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO8\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

# 0x00014711 LDO8\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO8\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level 0x1: VREG_OK_LEVEL_TRIGGERED 0x0: VREG_OK_EDGE_TRIGGERED

# 0x00014712 LDO8\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

# LDO8\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

# 0x00014713 LDO8\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO8\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

# 0x00014714 LDO8\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO8\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM
		0x0: VREG_OK_ERROR_NOT_REARM

# 0x00014715 LDO8\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO8\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

# 0x00014716 LDO8\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### LDO8\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED 0x0: VREG_OK_ERROR_DISABLED

# 0x00014718 LDO8\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

# LDO8\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

# 0x00014719 LDO8\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

# LDO8\_INT\_PENDING\_STS

E	Bits	Name	Description
	0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

# 0x0001471A LDO8\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO8\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

# 0x0001471B LDO8\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

# LDO8\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

# 0x00014741 LDO8\_VOLTAGE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK
Reset State: 0x5C

Reset Name: perph rb

#### LDO8\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

# 0x00014745 LDO8\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions

#### LDO8\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE
		0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode
		0x1: BYPASS_ENABLED
		0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B)
	0	0x1: FOLLOW_PMIC_AWAKE_TRUE
	277	0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00014746 LDO8\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### LDO8\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014748 LDO8\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

#### LDO8\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

# 0x0001474A LDO8\_OCP\_CTL1

#### LDO8\_OCP\_CTL1

LDO8	_OCP_CTL1				
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x80				
Reset N	Name: perph_rb	22			
LDO8_	LDO8_OCP_CTL1				
Bits	Name	Description			
7	OCP_EN	Enable the OCP feature			
	O'TO ME	0x1: OCP_ENABLED			
	0x0: OCP_DIABLED				
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)			
		0x1: OCP_TEST_MODE			
		0x0: OCP_NORMAL_MODE			

# 0x0001474B LDO8\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO8\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

# 0x0001474C LDO8\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

#### LDO8\_SOFT\_START\_CTL

Bits	Name	Description		
7	SOFT_START	0x1: SOFT_START_ENABLED		
		0x0: SOFT_START_DISABLED		
LDO8	LDO8_CONFIG_CTL			
Type: RW Clock: PBUS_WRCLK Reset State: 0x04				
	Reset State: 0x04  Reset Name: perph_rb			
LDO8_CONFIG_CTL				
Bits	Name	Description		
2	ACT DVDAGG DIJEE	EN OVI ACT DVDACC DIEE ENADIED		

#### 0x00014752 LDO8\_CONFIG\_CTL

# LDO8\_CONFIG\_CTL

Bits	Name	Description
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED
	8. Online	0x0: ACT_BYPASS_BUFF_DISABLED
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED

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# 0x00014800 LDO9\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO9\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00014801 LDO9\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO9\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

# 0x00014802 LDO9\_REVISION3

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO9\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00014803 LDO9 REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO9\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

# 0x00014804 LDO9\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC\_CONSTANT

#### LDO9\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00014805 LDO9\_PERPH\_SUBTYPE

Type: R

#### LDO9\_PERPH\_SUBTYPE

	PBUS_WRCLK State: 0x0B	
Reset Name: n/a		
Peripheral SubType		M. Comments
LDO9_	PERPH_SUBTYPE	·O,
Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

#### 0x00014808 LDO9\_STATUS1

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

# LDO9\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

# 0x00014809 LDO9\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

# LDO9\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

# 0x00014810 LDO9\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO9\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

# 0x00014811 LDO9\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO9\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level
		0x1: VREG_OK_LEVEL_TRIGGERED
		0x0: VREG_OK_EDGE_TRIGGERED

# 0x00014812 LDO9\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

#### LDO9\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	245	0x0: VREG_OK_LOW_DISABLED

# 0x00014813 LDO9\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO9\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true  0x1: VREG_OK_RISING_TRIGGERED  0x0: VREG_OK_FALLING_TRIGGERED

# 0x00014814 LDO9\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

## LDO9\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

# 0x00014815 LDO9\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO9\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

# 0x00014816 LDO9\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

# LDO9\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

# 0x00014818 LDO9\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

# LDO9\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

# 0x00014819 LDO9\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

#### LDO9\_INT\_PENDING\_STS

E	Bits	Name	Description
	0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

# 0x0001481A LDO9\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO9\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

# 0x0001481B LDO9\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

# LDO9\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

# 0x00014841 LDO9\_VOLTAGE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK
Reset State: 0x7C

Reset Name: perph rb

#### LDO9\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

# 0x00014845 LDO9\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph\_rb

Define LDO Mode Transitions

#### LDO9\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE
		0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode
		0x1: BYPASS_ENABLED
		0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B)
	0,	0x1: FOLLOW_PMIC_AWAKE_TRUE
	27,48	0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00014846 LDO9\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### LDO9\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014848 LDO9\_PD\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

#### LDO9\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

# 0x0001484A LDO9\_OCP\_CTL1

#### LDO9\_OCP\_CTL1

LDO9	_OCP_CTL1			
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x80			
Reset N	Name: perph_rb			
LDO9_	LDO9_OCP_CTL1			
Bits	Name	Description		
7	OCP_EN	Enable the OCP feature		
	07. 40	0x1: OCP_ENABLED		
	2,47,3	0x0: OCP_DIABLED		
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)		
		0x1: OCP_TEST_MODE		
		0x0: OCP_NORMAL_MODE		

# 0x0001484B LDO9\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO9\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

# 0x0001484C LDO9\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

#### LDO9\_SOFT\_START\_CTL

Bits	Name	Description	
7	SOFT_START	0x1: SOFT_START_ENABLED	
		0x0: SOFT_START_DISABLED	
LDO9	_CONFIG_CTL		
Clock:	Type: RW  Clock: PBUS_WRCLK  Reset State: 0x04		
Reset 1	Reset Name: perph_rb		
LDO9_	LDO9_CONFIG_CTL		
Bits	Name	Description	
2	ACT DVDACC DIEE	EN OVA: ACT DVDASS DIEE ENADIED	

#### 0x00014852 LDO9\_CONFIG\_CTL

# LDO9\_CONFIG\_CTL

Bits	Name	Description
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED
	8. Online	0x0: ACT_BYPASS_BUFF_DISABLED
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED

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# 0x00014900 LDO10\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO10\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00014901 LDO10\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO10\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

# 0x00014902 LDO10\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

# LDO10\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

# 0x00014903 LDO10\_REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO10\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

# 0x00014904 LDO10\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

#### LDO10\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00014905 LDO10\_PERPH\_SUBTYPE

Type: R

#### LDO10\_PERPH\_SUBTYPE

	PBUS_WRCLK State: 0x09	
Reset I	Name: n/a	
Peripheral SubType		
LDO10	_PERPH_SUBTYPE	·O,
Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

#### LDO10\_STATUS1 0x00014908

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

#### LDO10\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

# 0x00014909 LDO10\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

# LDO10\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

# 0x00014910 LDO10\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO10\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

# 0x00014911 LDO10\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO10\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level 0x1: VREG_OK_LEVEL_TRIGGERED 0x0: VREG_OK_EDGE_TRIGGERED

# 0x00014912 LDO10\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

# LDO10\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

# 0x00014913 LDO10\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO10\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

# 0x00014914 LDO10\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

# LDO10\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM
		0x0: VREG_OK_ERROR_NOT_REARM

# 0x00014915 LDO10\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET\_MASK

#### LDO10\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

# 0x00014916 LDO10\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

# LDO10\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

# 0x00014918 LDO10\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

# LDO10\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

# 0x00014919 LDO10\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

#### LDO10\_INT\_PENDING\_STS

Bits	Name	Description
0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

#### 0x0001491A LDO10\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO10\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

#### 0x0001491B LDO10\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

## LDO10\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

#### 0x00014941 LDO10\_VOLTAGE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK
Reset State: 0x54

Reset Name: perph rb

#### LDO10\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

## 0x00014945 LDO10\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions

#### LDO10\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE
		0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode
		0x1: BYPASS_ENABLED
		0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B)
	0,	0x1: FOLLOW_PMIC_AWAKE_TRUE
	27,48	0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00014946 LDO10\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### LDO10\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014948 LDO10\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

#### LDO10\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED
		0x0: PULLDN_DIABLED

## 0x0001494A LDO10\_OCP\_CTL1

#### LDO10\_OCP\_CTL1

LDO1	0_OCP_CTL1				
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x80				
Reset N	Name: perph_rb				
LDO10	_OCP_CTL1	in cours			
Bits	Name	Description			
7	OCP_EN	Enable the OCP feature			
	O'L WE	0x1: OCP_ENABLED			
	7,5	0x0: OCP_DIABLED			
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)			
		0x1: OCP_TEST_MODE			
		0x0: OCP_NORMAL_MODE			

#### 0x0001494B LDO10\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO10\_OCP\_CTL2

Bit	s Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

## 0x0001494C LDO10\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

#### LDO10\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED

#### 0x00014952 LDO10\_CONFIG\_CTL

#### LDO10\_CONFIG\_CTL

LDO10_CONFIG_CTL				
Type: RW Clock: PBUS_WRCLK Reset State: 0x04				
Reset I	Name: perph_rb	21.8		
LDO10	_CONFIG_CTL	02/10		
Bits	Name	Description		
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED 0x0: ACT_BYPASS_BUFF_DISABLED		
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED		

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#### 0x00014A00 LDO11\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO11\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014A01 LDO11\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO11\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00014A02 LDO11\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO11\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014A03 LDO11\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO11\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00014A04 LDO11\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

#### LDO11\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00014A05 LDO11\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x0B

Reset Name: n/a

Peripheral SubType

#### LDO11\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

SUNC

## 0x00014A08 LDO11\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

#### LDO11\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

## 0x00014A09 LDO11\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

#### LDO11\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

## 0x00014A10 LDO11\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO11\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

#### 0x00014A11 LDO11\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO11\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level
		0x1: VREG_OK_LEVEL_TRIGGERED
		0x0: VREG_OK_EDGE_TRIGGERED

## 0x00014A12 LDO11\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### LDO11\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

#### 0x00014A13 LDO11\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO11\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

#### 0x00014A14 LDO11\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO11\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM
		0x0: VREG_OK_ERROR_NOT_REARM

### 0x00014A15 LDO11\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO11\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014A16 LDO11\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### LDO11\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014A18 LDO11\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### LDO11\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

## 0x00014A19 LDO11\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

#### LDO11\_INT\_PENDING\_STS

Bits	Name	Description
0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

#### 0x00014A1A LDO11\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO11\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

## 0x00014A1B LDO11\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

## LDO11\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

#### 0x00014A41 LDO11\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x60

Reset Name: perph rb

#### LDO11\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

## 0x00014A45 LDO11\_MODE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions

#### LDO11\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE
		0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode
		0x1: BYPASS_ENABLED
		0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B)
	0	0x1: FOLLOW_PMIC_AWAKE_TRUE
	277	0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00014A46 LDO11\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

## LDO11\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014A48 LDO11\_PD\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

#### LDO11\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

## 0x00014A4A LDO11\_OCP\_CTL1

#### LDO11\_OCP\_CTL1

LDO1	LDO11_OCP_CTL1		
Clock: Reset S	Type: RW Clock: PBUS_WRCLK Reset State: 0x80		
Reset N	Name: perph_rb	N. C.	
LDO11	LDO11_OCP_CTL1		
Bits	Name	Description	
7	OCP_EN	Enable the OCP feature	
	O'TO ME	0x1: OCP_ENABLED	
	2	0x0: OCP_DIABLED	
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)	
		0x1: OCP_TEST_MODE	
		0x0: OCP_NORMAL_MODE	

#### 0x00014A4B LDO11\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO11\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

## 0x00014A4C LDO11\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

#### LDO11\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED

## 0x00014A52 LDO11\_CONFIG\_CTL

## LDO11\_CONFIG\_CTL

I DO1	LDO11_CONFIG_CTL		
Type: Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x04		
Reset I	Reset Name: perph_rb		
LDO11	LDO11_CONFIG_CTL		
Bits	Name	Description	
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED 0x0: ACT_BYPASS_BUFF_DISABLED	
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED	

## 70 Ldo\_ult\_dig Registers

#### 0x00014B00 LDO12\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO12\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00014B01 LDO12\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO12\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00014B02 LDO12\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO12\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014B03 LDO12\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO12\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00014B04 LDO12\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

#### LDO12\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00014B05 LDO12\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x09

Reset Name: n/a

Peripheral SubType

#### LDO12\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

SUNC

## 0x00014B08 LDO12\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

#### LDO12\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

## 0x00014B09 LDO12\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

#### LDO12\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

## 0x00014B10 LDO12\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO12\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_ERR

#### 0x00014B11 LDO12\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

#### LDO12\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level 0x1: VREG_OK_LEVEL_TRIGGERED 0x0: VREG_OK_EDGE_TRIGGERED

## 0x00014B12 LDO12\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### LDO12\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

#### 0x00014B13 LDO12\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO12\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

#### 0x00014B14 LDO12\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO12\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

#### 0x00014B15 LDO12\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO12\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014B16 LDO12\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### LDO12\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014B18 LDO12\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### LDO12\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27	0x0: LDO_VOLTAGE_OK
		P. Control of the Con

### 0x00014B19 LDO12\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

#### LDO12\_INT\_PENDING\_STS

Bits	Name	Description
0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

#### 0x00014B1A LDO12\_INT\_MID\_SEL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO12\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

## 0x00014B1B LDO12\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

#### LDO12\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

#### 0x00014B41 LDO12\_VOLTAGE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK
Reset State: 0x60

Reset Name: perph rb

#### LDO12\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

## 0x00014B45 LDO12\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions

#### LDO12\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE
		0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode
		0x1: BYPASS_ENABLED
		0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B)
	0,	0x1: FOLLOW_PMIC_AWAKE_TRUE
	27,48	0x0: FOLLOW_PMIC_AWAKE_FALSE

## 0x00014B46 LDO12\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

## LDO12\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014B48 LDO12\_PD\_CTL

**Type:** RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO12\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

## 0x00014B4A LDO12\_OCP\_CTL1

#### LDO12\_OCP\_CTL1

LDO1	LDO12_OCP_CTL1			
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x80			
Reset N	Name: perph_rb			
LDO12	LDO12_OCP_CTL1			
Bits	Name	Description		
7	OCP_EN	Enable the OCP feature		
	O'T WE	0x1: OCP_ENABLED		
	2,45	0x0: OCP_DIABLED		
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)		
		0x1: OCP_TEST_MODE		
		0x0: OCP_NORMAL_MODE		

#### 0x00014B4B LDO12\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO12\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

## 0x00014B4C LDO12\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO12\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED

## 0x00014B52 LDO12\_CONFIG\_CTL

#### LDO12\_CONFIG\_CTL

LDO12_CONFIG_CTL		
Type: RW Clock: PBUS_WRCLK Reset State: 0x04		
Name: perph_rb	180	
LDO12_CONFIG_CTL		
Name	Description	
ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED	
3. Online	0x0: ACT_BYPASS_BUFF_DISABLED	
MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error	
1	amp are short circuited during NPM?LPM transition	
-	0x1: MODE_TRAN_ENH_ENABLED	
	0x0: MODE_TRAN_ENH_DISABLED	
	RW PBUS_WRCLK State: 0x04 Name: perph_rb _CONFIG_CTL Name ACT_BYPASS_BUFF_EN	

## 71 Ldo\_ult\_dig Registers

#### 0x00014C00 LDO13\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO13\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014C01 LDO13\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO13\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00014C02 LDO13\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO13\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014C03 LDO13\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO13\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

### 0x00014C04 LDO13\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

#### LDO13\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00014C05 LDO13\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: n/a

Peripheral SubType

#### LDO13\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

SUNC

## 0x00014C08 LDO13\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

## LDO13\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

## 0x00014C09 LDO13\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

#### LDO13\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

## 0x00014C10 LDO13\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO13\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

#### 0x00014C11 LDO13\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO13\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level
		0x1: VREG_OK_LEVEL_TRIGGERED
		0x0: VREG_OK_EDGE_TRIGGERED

## 0x00014C12 LDO13\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### LDO13\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

#### 0x00014C13 LDO13\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO13\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

#### 0x00014C14 LDO13\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO13\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

### 0x00014C15 LDO13\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO13\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014C16 LDO13\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### LDO13\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED 0x0: VREG_OK_ERROR_DISABLED

#### 0x00014C18 LDO13\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### LDO13\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

### 0x00014C19 LDO13\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

#### LDO13\_INT\_PENDING\_STS

E	Bits	Name	Description
	0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

#### 0x00014C1A LDO13\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO13\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

## 0x00014C1B LDO13\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

#### LDO13\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

## 0x00014C41 LDO13\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x6A

Reset Name: perph rb

#### LDO13\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

## 0x00014C45 LDO13\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions

#### LDO13\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE
		0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode
		0x1: BYPASS_ENABLED
		0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B)
	0	0x1: FOLLOW_PMIC_AWAKE_TRUE
	277	0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00014C46 LDO13\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### LDO13\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014C48 LDO13\_PD\_CTL

**Type:** RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO13\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

## 0x00014C4A LDO13\_OCP\_CTL1

#### LDO13\_OCP\_CTL1

LDO13_OCP_CTL1					
Type: RW Clock: PBUS_WRCLK Reset State: 0x80					
Keset 1	Reset Name: perph_rb				
LDO13_OCP_CTL1					
Bits	Name	Description			
7	OCP_EN	Enable the OCP feature			
	O' ME	0x1: OCP_ENABLED			
	2,45	0x0: OCP_DIABLED			
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)			
		0x1: OCP_TEST_MODE			
		0x0: OCP_NORMAL_MODE			

#### 0x00014C4B LDO13\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO13\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

## 0x00014C4C LDO13\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO13\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED

### 0x00014C52 LDO13\_CONFIG\_CTL

#### LDO13\_CONFIG\_CTL

LDO1	3_CONFIG_CTL	
Type: RW Clock: PBUS_WRCLK Reset State: 0x04  Reset Name: perph_rb  LDO13_CONFIG_CTL		
Bits	Name	Description
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED
	3. Onlins	0x0: ACT_BYPASS_BUFF_DISABLED
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED
		0x0: MODE_TRAN_ENH_DISABLED

## 72 Ldo\_ult\_dig Registers

#### 0x00014D00 LDO14\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO14\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014D01 LDO14\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC\_CONSTANT

#### LDO14\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00014D02 LDO14\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO14\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014D03 LDO14 REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO14\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00014D04 LDO14\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

#### LDO14\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00014D05 LDO14\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: n/a

Peripheral SubType

#### LDO14\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

SUNC

## 0x00014D08 LDO14\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

#### LDO14\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

#### 0x00014D09 LDO14\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

#### LDO14\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

## 0x00014D10 LDO14\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO14\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

#### 0x00014D11 LDO14\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

#### LDO14\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level 0x1: VREG_OK_LEVEL_TRIGGERED 0x0: VREG_OK_EDGE_TRIGGERED

## 0x00014D12 LDO14\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

#### LDO14\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

#### 0x00014D13 LDO14\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO14\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true  0x1: VREG_OK_RISING_TRIGGERED  0x0: VREG_OK_FALLING_TRIGGERED

#### 0x00014D14 LDO14\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO14\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM
		0x0: VREG_OK_ERROR_NOT_REARM

### 0x00014D15 LDO14\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO14\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014D16 LDO14\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### LDO14\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014D18 LDO14\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### LDO14\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

### 0x00014D19 LDO14\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

#### LDO14\_INT\_PENDING\_STS

Bits	Name	Description
0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

#### 0x00014D1A LDO14\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO14\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

## 0x00014D1B LDO14\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

#### LDO14\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

#### 0x00014D41 LDO14\_VOLTAGE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK
Reset State: 0x04

Reset Name: perph rb

#### LDO14\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

## 0x00014D45 LDO14\_MODE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions

#### LDO14\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM 0x1: FORCED_NPM 0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE 0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode 0x1: BYPASS_ENABLED 0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B) 0x1: FOLLOW_PMIC_AWAKE_TRUE 0x0: FOLLOW_PMIC_AWAKE_FALSE

## 0x00014D46 LDO14\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### LDO14\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014D48 LDO14\_PD\_CTL

**Type:** RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO14\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

### 0x00014D4A LDO14\_OCP\_CTL1

#### LDO14\_OCP\_CTL1

LDO1	LDO14_OCP_CTL1			
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x80			
Reset N	Name: perph_rb			
LDO14_OCP_CTL1				
LDOIT	_001_0121	W.		
Bits	Name	Description		
		Description  Enable the OCP feature		
Bits	Name	•		
Bits	Name	Enable the OCP feature		
Bits	Name	Enable the OCP feature  0x1: OCP_ENABLED		
Bits 7	Name OCP_EN	Enable the OCP feature 0x1: OCP_ENABLED 0x0: OCP_DIABLED		

#### 0x00014D4B LDO14\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO14\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

## 0x00014D4C LDO14\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO14\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED

### 0x00014D52 LDO14\_CONFIG\_CTL

## LDO14\_CONFIG\_CTL

	L DOMA CONFIG. OT		
LDO1	LDO14_CONFIG_CTL		
Type: RW Clock: PBUS_WRCLK Reset State: 0x04			
Reset I	Name: perph_rb	18	
LDO14	LDO14_CONFIG_CTL		
Bits	Name	Description	
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED 0x0: ACT_BYPASS_BUFF_DISABLED	
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED	

## 73 Ldo\_ult\_dig Registers

#### 0x00014E00 LDO15\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO15\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

### 0x00014E01 LDO15\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO15\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00014E02 LDO15\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

## LDO15\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014E03 LDO15\_REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO15\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00014E04 LDO15\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

#### LDO15\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00014E05 LDO15\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: n/a

Peripheral SubType

#### LDO15\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

SUNC

## 0x00014E08 LDO15\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

#### LDO15\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

## 0x00014E09 LDO15\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

#### LDO15\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

## 0x00014E10 LDO15\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO15\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

#### 0x00014E11 LDO15\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

#### LDO15\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level 0x1: VREG_OK_LEVEL_TRIGGERED 0x0: VREG_OK_EDGE_TRIGGERED

## 0x00014E12 LDO15\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### LDO15\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

#### 0x00014E13 LDO15\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO15\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true  0x1: VREG_OK_RISING_TRIGGERED  0x0: VREG_OK_FALLING_TRIGGERED

#### 0x00014E14 LDO15\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO15\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

#### 0x00014E15 LDO15\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO15\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014E16 LDO15\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### LDO15\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014E18 LDO15\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### LDO15\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

### 0x00014E19 LDO15\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

#### LDO15\_INT\_PENDING\_STS

Bits	Name	Description
0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

#### 0x00014E1A LDO15\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO15\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

## 0x00014E1B LDO15\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

### LDO15\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

#### 0x00014E41 LDO15\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x04

Reset Name: perph\_rb

#### LDO15\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

## 0x00014E45 LDO15\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions

#### LDO15\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE
		0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode
		0x1: BYPASS_ENABLED
		0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B)
	0,	0x1: FOLLOW_PMIC_AWAKE_TRUE
	27,48	0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00014E46 LDO15\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### LDO15\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014E48 LDO15\_PD\_CTL

**Type:** RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO15\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

## 0x00014E4A LDO15\_OCP\_CTL1

#### LDO15\_OCP\_CTL1

LDO1	5_OCP_CTL1			
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x80			
Reset N	Name: perph_rb			
LDO15	LDO15_OCP_CTL1			
Bits	Name Description			
7	OCP_EN	Enable the OCP feature		
	O'T WE	0x1: OCP_ENABLED		
	2,45	0x0: OCP_DIABLED		
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)		
		0x1: OCP_TEST_MODE		
		0x0: OCP_NORMAL_MODE		

#### 0x00014E4B LDO15\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO15\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

## 0x00014E4C LDO15\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO15\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED

### 0x00014E52 LDO15\_CONFIG\_CTL

## LDO15\_CONFIG\_CTL

LDO1	LDO15_CONFIG_CTL			
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x04			
Reset I	Reset Name: perph_rb			
LDO15	LDO15_CONFIG_CTL			
Bits	Name	Description		
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED 0x0: ACT_BYPASS_BUFF_DISABLED		
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED		

## 74 Ldo\_ult\_dig Registers

#### 0x00014F00 LDO16\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO16\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00014F01 LDO16\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO16\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00014F02 LDO16\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO16\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00014F03 LDO16\_REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO16\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 0x00014F04 LDO16\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

#### LDO16\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00014F05 LDO16\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x28

Reset Name: n/a

Peripheral SubType

#### LDO16\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

SUNC

## 0x00014F08 LDO16\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

#### LDO16\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

## 0x00014F09 LDO16\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

#### LDO16\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

## 0x00014F10 LDO16\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### LDO16\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

#### 0x00014F11 LDO16\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

#### LDO16\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level 0x1: VREG_OK_LEVEL_TRIGGERED 0x0: VREG_OK_EDGE_TRIGGERED

## 0x00014F12 LDO16\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### LDO16\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

#### 0x00014F13 LDO16\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO16\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

#### 0x00014F14 LDO16\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO16\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

### 0x00014F15 LDO16\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO16\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014F16 LDO16\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### LDO16\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00014F18 LDO16\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### LDO16\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

### 0x00014F19 LDO16\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

#### LDO16\_INT\_PENDING\_STS

Bits	Name	Description
0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

#### 0x00014F1A LDO16\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO16\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

#### 0x00014F1B LDO16\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

## LDO16\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

#### 0x00014F41 LDO16\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x04

Reset Name: perph rb

#### LDO16\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

## 0x00014F45 LDO16\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph\_rb

Define LDO Mode Transitions

#### LDO16\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE
		0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode
		0x1: BYPASS_ENABLED
		0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B)
	0	0x1: FOLLOW_PMIC_AWAKE_TRUE
	277	0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00014F46 LDO16\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### LDO16\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00014F48 LDO16\_PD\_CTL

**Type:** RW

Clock: PBUS\_WRCLK
Reset State: 0x80

Reset Name: perph rb

#### LDO16\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

## 0x00014F4A LDO16\_OCP\_CTL1

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x80

Reset Name: perph rb

#### LDO16\_OCP\_CTL1

Bits	Name	Description
7	OCP_EN	Enable the OCP feature
	Or Ma	0x1: OCP_ENABLED
	2 2 3	0x0: OCP_DIABLED
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)
		0x1: OCP_TEST_MODE
		0x0: OCP_NORMAL_MODE

#### 0x00014F4B LDO16\_OCP\_CTL2

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO16\_OCP\_CTL2

Bit	s Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

## 0x00014F4C LDO16\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK **Reset State:** 0x80

Reset Name: perph rb

#### LDO16\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED

#### 0x00014F52 LDO16\_CONFIG\_CTL

## LDO16\_CONFIG\_CTL

LDO1	LDO16_CONFIG_CTL		
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x04		
Reset I	Reset Name: perph_rb		
LDO16	LDO16_CONFIG_CTL		
Bits	Name	Description	
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED 0x0: ACT_BYPASS_BUFF_DISABLED	
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED	

## 75 Ldo\_ult\_dig Registers

#### 0x00015000 LDO17\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### LDO17\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

### 0x00015001 LDO17\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO17\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00015002 LDO17\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO17\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00015003 LDO17\_REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO17\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 0x00015004 LDO17\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC\_CONSTANT

## LDO17\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

## 0x00015005 LDO17\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x0B

Reset Name: n/a

Peripheral SubType

## LDO17\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

SUNC

## 0x00015008 LDO17\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: n/a

Status Registers

## LDO17\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

## 0x00015009 LDO17\_STATUS2

Type: R

Clock: PBUS\_WRCLK Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

## LDO17\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

# 0x00015010 LDO17\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

## LDO17\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

## 0x00015011 LDO17\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

## LDO17\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level 0x1: VREG_OK_LEVEL_TRIGGERED 0x0: VREG_OK_EDGE_TRIGGERED

## 0x00015012 LDO17\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

## LDO17\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

## 0x00015013 LDO17\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

## LDO17\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true  0x1: VREG_OK_RISING_TRIGGERED  0x0: VREG_OK_FALLING_TRIGGERED

## 0x00015014 LDO17\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

## LDO17\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

## 0x00015015 LDO17\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO17\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

## 0x00015016 LDO17\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

## LDO17\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

## 0x00015018 LDO17\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

## LDO17\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

## 0x00015019 LDO17\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

## LDO17\_INT\_PENDING\_STS

E	Bits	Name	Description
	0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

## 0x0001501A LDO17\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO17\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

## 0x0001501B LDO17\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

## LDO17\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A
		0x0: INT_PRIORITY_SR

## 0x00015041 LDO17\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x58

Reset Name: perph rb

#### LDO17\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

## 0x00015045 LDO17\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph\_rb

Define LDO Mode Transitions

## LDO17\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE
		0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode
		0x1: BYPASS_ENABLED
		0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B)
	0	0x1: FOLLOW_PMIC_AWAKE_TRUE
	27,48	0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00015046 LDO17\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

## LDO17\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00015048 LDO17\_PD\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

## LDO17\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

## 0x0001504A LDO17\_OCP\_CTL1

#### LDO17\_OCP\_CTL1

LDO1	LDO17_OCP_CTL1			
	Type: RW Clock: PBUS_WRCLK Reset State: 0x80			
Reset N	Name: perph_rb	an'		
LDO17	LDO17_OCP_CTL1			
Bits	Name	Description		
7	OCP_EN	Enable the OCP feature		
	O'TO WE	0x1: OCP_ENABLED		
	1,1	0x0: OCP_DIABLED		
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)		
		0x1: OCP_TEST_MODE		
		0x0: OCP_NORMAL_MODE		

## 0x0001504B LDO17\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

## LDO17\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

## 0x0001504C LDO17\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

## LDO17\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED

#### 0x00015052 LDO17\_CONFIG\_CTL

## LDO17\_CONFIG\_CTL

LDO1	LDO17_CONFIG_CTL			
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x04			
Reset I	Name: perph_rb	.2180		
LDO17	LDO17_CONFIG_CTL			
Bits	Name	Description		
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED 0x0: ACT_BYPASS_BUFF_DISABLED		
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED		

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## 0x00015100 LDO18\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

## LDO18\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00015101 LDO18\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

## LDO18\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x00015102 LDO18\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO18\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00015103 LDO18\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

## LDO18\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00015104 LDO18\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

## LDO18\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

## 0x00015105 LDO18\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x09

Reset Name: n/a

Peripheral SubType

## LDO18\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

SUNC

## 0x00015108 LDO18\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

## LDO18\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

## 0x00015109 LDO18\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

## LDO18\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VPEC ON	indicate whether the regulator is on
	VREG_ON	0x1: LDO ON
	05	0x0: LDO_OFF

# 0x00015110 LDO18\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

## LDO18\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

## 0x00015111 LDO18\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

## LDO18\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level 0x1: VREG_OK_LEVEL_TRIGGERED 0x0: VREG_OK_EDGE_TRIGGERED

## 0x00015112 LDO18\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

## LDO18\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

## 0x00015113 LDO18\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

## LDO18\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

## 0x00015114 LDO18\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

## LDO18\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM 0x0: VREG_OK_ERROR_NOT_REARM

## 0x00015115 LDO18\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO18\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

## 0x00015116 LDO18\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

## LDO18\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

## 0x00015118 LDO18\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

## LDO18\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

## 0x00015119 LDO18\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

## LDO18\_INT\_PENDING\_STS

Bits	Name	Description
0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

## 0x0001511A LDO18\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO18\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

## 0x0001511B LDO18\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

## LDO18\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

## 0x00015141 LDO18\_VOLTAGE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK
Reset State: 0x4C

Reset Name: perph rb

#### LDO18\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

#### LDO18\_MODE\_CTL2 0x00015145

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions

## LDO18\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM 0x1: FORCED_NPM 0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE 0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode 0x1: BYPASS_ENABLED 0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B) 0x1: FOLLOW_PMIC_AWAKE_TRUE 0x0: FOLLOW_PMIC_AWAKE_FALSE

# LDO18\_EN\_CTL 0x00015146

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

## LDO18\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00015148 LDO18\_PD\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

## LDO18\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED
		0x0: PULLDN_DIABLED

## 0x0001514A LDO18\_OCP\_CTL1

#### LDO18\_OCP\_CTL1

LDO1	8_OCP_CTL1				
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x80				
Reset N	Name: perph_rb				
LDO18	LDO18_OCP_CTL1				
Bits	Name	Description			
7	OCP_EN	Enable the OCP feature			
	O'TO THE	0x1: OCP_ENABLED			
	2,45	0x0: OCP_DIABLED			
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)			
		0x1: OCP_TEST_MODE			
		0x0: OCP_NORMAL_MODE			

## 0x0001514B LDO18\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

## LDO18\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

## 0x0001514C LDO18\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

## LDO18\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED

#### 0x00015152 LDO18\_CONFIG\_CTL

## LDO18\_CONFIG\_CTL

LDO18_CONFIG_CTL				
Type: RW Clock: PBUS_WRCLK Reset State: 0x04				
Reset I	Reset Name: perph_rb			
LDO18_CONFIG_CTL				
Bits	Name	Description		
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED 0x0: ACT_BYPASS_BUFF_DISABLED		
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED		

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## 0x00015200 LDO19\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

## LDO19\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00015201 LDO19\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC\_CONSTANT

## LDO19\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x00015202 LDO19\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: n/a

HW Version Register [23:16]

## LDO19\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00015203 LDO19 REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: n/a

HW Version Register [31:24]

## LDO19\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00015204 LDO19\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

## LDO19\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	ULT LDO

## 0x00015205 LDO19\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x07

Reset Name: n/a

Peripheral SubType

## LDO19\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	N300_stepper: 0x15; N600_stepper: 0x06; N900_stepper: 0x14; N1200_stepper: 0x07

SINN

## 0x00015208 LDO19\_STATUS1

Type: R

Clock: PBUS\_WRCLK
Reset State: 0bXXXXXXX1

Reset Name: n/a

Status Registers

## LDO19\_STATUS1

Bits	Name	Description
7	VREG_OK	0 = VREG output voltage is below VREG_OK threshold, 1 = VREG output voltage is above VREG_OK threshold. VREG_OK is also high when LDO is in bypass mode 0x1: LDO_VOLTAGE_OK 0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	1 = VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

## LDO19\_STATUS1 (cont.)

Bits	Name	Description
0	STEPPER_DONE	indicates if LDO voltage steppering is done
		0x1: STEPPER_DONE
		0x0: STEPPER_NOT_DONE

#### 0x00015209 LDO19\_STATUS2

#### LDO19\_STATUS2

LDO19_STATUS2			
	R PBUS_WRCLK State: 0x00		
Reset N	Name: n/a		
Status 1	Registers		
LDO19	_STATUS2		
Bits	Name	Description	
		Description	
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode  0x1: SOFTSTART_DONE  0x0: SOFTSTART_NOT_DONE	

#### 0x00015210 LDO19\_INT\_RT\_STS

Type: R

Clock: PBUS WRCLK **Reset State:** 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

## LDO19\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_ERR

## 0x00015211 LDO19\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

## LDO19\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level
		0x1: VREG_OK_LEVEL_TRIGGERED
		0x0: VREG_OK_EDGE_TRIGGERED

## 0x00015212 LDO19\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

## LDO19\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	243	0x0: VREG_OK_LOW_DISABLED

## 0x00015213 LDO19\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

## LDO19\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

Ldo\_ult\_stepper\_dig Registers

## 0x00015214 LDO19\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

## LDO19\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM
		0x0: VREG_OK_ERROR_NOT_REARM

## 0x00015215 LDO19\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO19\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

## 0x00015216 LDO19\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

## LDO19\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

## 0x00015218 LDO19\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

## LDO19\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

## 0x00015219 LDO19\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

## LDO19\_INT\_PENDING\_STS

Bits	Name	Description
0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

## 0x0001521A LDO19\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO19\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

## 0x0001521B LDO19\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

## LDO19\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

## 0x00015241 LDO19\_VOLTAGE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x4A

Reset Name: perph rb

Register for voltage programming bits going to LDO.

#### LDO19\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep). Vmin and Vsetp are minimal voltage and voltage step size, respectively. For ULT NMOS LDOs, Vmin=375mV, Vstep=12.5mV.

## 0x00015245 LDO19\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

Define LDO Mode Transitions. This register needs to be 0x00 for putting LDO in LPM.

## LDO19\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM 0x1: FORCED_NPM 0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	LDO is in active bypass mode when both BYPASS_ACT and BYPASS_EN are set to 1, while NPM is set to 0 0x1: BYPASS_ACT_TRUE 0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode 0x1: BYPASS_ENABLED 0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	1' = (LDO is in NPM when PMIC_AWAKE (SLEEP_B) = '1') or (has no effect on LDO operation mode when PMIC_AWAKE = '0'), '0' = has no effect on LDO operation mode no matter PMIC_AWAKE is 0 or 1  0x1: FOLLOW_PMIC_AWAKE_TRUE  0x0: FOLLOW_PMIC_AWAKE_FALSE

## 0x00015246 LDO19\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Enable control register.

## LDO19\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE

## LDO19\_EN\_CTL (cont.)

	Bits	Name	Description
Г	0	FOLLOW_HW_EN0	NPM enable setting using HWEN0
			0x1: FOLLOW_HW_EN0_TRUE
			0x0: FOLLOW_HW_EN0_FALSE
-1			

## 0x00015248 LDO19\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

LDO pulldown control

## LDO19\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	1' = Enable the pulldown when the regulator is disabled, '0' = pulldown is always disabled.  0x1: PULLDN_ENABLED  0x0: PULLDN_DIABLED

ONN

## 0x0001524C LDO19\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph\_rb

Soft start control register

## LDO19\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	1' = Enable LDO softstart function, '0' = Disable LDO softstart function.  0x1: SOFT_START_ENABLED  0x0: SOFT_START_DISABLED

## 0x00015252 LDO19\_CONFIG\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x04

**Reset Name:** perph\_rb

Config control register.

## LDO19\_CONFIG\_CTL

Bits	Name	Description
3	ACT_BYPASS_BUFF_EN	1' = LDO buffer stage is enabled when LDO is in active bypass mode, '0' = LDO buffer stage is disabled when LDO is in active bypass mode.  0x1: ACT_BYPASS_BUFF_ENABLED  0x0: ACT_BYPASS_BUFF_DISABLED
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM-LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED

## 0x00015261 LDO19\_VS\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x85

Reset Name: perph rb

LDO voltage stepper control register. NMOS LDO use only.

## LDO19\_VS\_CTL

Bits	Name	Description
7	VS_EN	Enables the stepper
		0x1: STEPPER_ENABLED
		0x0: STEPPER_DIABLED

## LDO19\_VS\_CTL (cont.)

Bits	Name	Description
2:0	VS_DELAY	Delay (clk_in = 19.2 MHz) -000 = 20 clock cycles (delay of 1 us) - 001 = 40 clock cycles (delay of 2 us) -010 = 80 clock cycles (delay of 4.1 us) -011 = 160 clock cycles (delay of 8.3 us) -100 = 320 clock cycles (delay of 16.6 us) -101 = 640 clock cycles (delay of 33.3 us) -110 = 1280 clock cycles (delay of 67 us) -111 = 2560 clock cycles (delay of 134 us) 0x7: DELAY_1_2560 0x6: DELAY_1_1280 0x5: DELAY_1_640 0x4: DELAY_1_320 0x3: DELAY_1_160 0x2: DELAY_1_80
		0x1: DELAY_1_40 0x0: DELAY_1_20

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# 78 Ldo\_ult\_dig Registers

## 0x00015500 LDO22\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

## LDO22\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00015501 LDO22\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

## LDO22\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

## 0x00015502 LDO22\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [23:16]

#### LDO22\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x00015503 LDO22 REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO22\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

## 0x00015504 LDO22\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x21

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

## LDO22\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

## 0x00015505 LDO22\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x0A

Reset Name: n/a

Peripheral SubType

## LDO22\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	P50: 0x08; P150: 0x09; P300: 0x0A; P600: 0x0B; P1200: 0x0C; P450: 0x0D; LV_P50: 0x28; LV_P150: 0x29; LV_P300: 0x2A; LV_P600: 0x2B; LVP1200: 0x2C; LV_P450: 0x2D

SUNC

## 0x00015508 LDO22\_STATUS1

Type: R

Clock: PBUS\_WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

## LDO22\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
2	BYPASS_LDO	LDO is ON and in bypass mode 0x1: ON_AND_BYPASSED 0x0: OFF_OR_NON_BYPASS
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

## 0x00015509 LDO22\_STATUS2

Type: R

Clock: PBUS\_WRCLK
Reset State: 0b0X000000

**Reset Name:** n/a
Status Registers

## LDO22\_STATUS2

Bits	Name	Description
7	SOFTSTART_DONE	indicates that the startup is complete LDO in normal mode
		0x1: SOFTSTART_DONE
		0x0: SOFTSTART_NOT_DONE
6	OCP_LATCHED	sticky status bit, once OCP is detected, this bit is set, and remain set until SW write OCP_LATCHED_CLR to clear it 0x1: OCP_LATCHED  0x0: OCP_NOT_LATCHED
5	VREG_ON	indicate whether the regulator is on 0x1: LDO_ON 0x0: LDO_OFF

## 0x00015510 LDO22\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

## LDO22\_INT\_RT\_STS

Bits	Name	Description
0	VREG_OK_RT_STS	Regulator has been successfully enabled
		0x1: LDO_ENABLE_SUCCESS
		0x0: LDO_ENABLE_ERR

#### 0x00015511 LDO22\_INT\_SET\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

#### LDO22\_INT\_SET\_TYPE

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level 0x1: VREG_OK_LEVEL_TRIGGERED 0x0: VREG_OK_EDGE_TRIGGERED

# 0x00015512 LDO22\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### LDO22\_INT\_POLARITY\_HIGH

Bits	Name	Description
0	VREG_OK_HIGH	Edge type, rising or Level type, high true
	O'TO WE	0x1: VREG_OK_LOW_TRIGGERED
	245	0x0: VREG_OK_LOW_DISABLED

### 0x00015513 LDO22\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

#### LDO22\_INT\_POLARITY\_LOW

Bits	Name	Description
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

#### 0x00015514 LDO22\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO22\_INT\_LATCHED\_CLR

Bits	Name	Description
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM
		0x0: VREG_OK_ERROR_NOT_REARM

## 0x00015515 LDO22\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### LDO22\_INT\_EN\_SET

Bits	Name	Description
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00015516 LDO22\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC\_CLR\_MASK=INT\_EN\_SET

#### LDO22\_INT\_EN\_CLR

Bits	Name	Description
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00015518 LDO22\_INT\_LATCHED\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### LDO22\_INT\_LATCHED\_STS

Bits	Name	Description
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled
		0x1: LDO_VOLTAGE_LOW
	27.0	0x0: LDO_VOLTAGE_OK

## 0x00015519 LDO22\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

#### LDO22\_INT\_PENDING\_STS

Bits	Name	Description
0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

### 0x0001551A LDO22\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO22\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
		0x0: INT_MID_SEL_0

#### 0x0001551B LDO22\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00
Reset Name: perph rb

#### LDO22\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR

## 0x00015541 LDO22\_VOLTAGE\_CTL2

**Type:** RW

Clock: PBUS\_WRCLK
Reset State: 0x54

Reset Name: perph rb

#### LDO22\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	VSET	Voltage = Vmin + VSET*(Vstep)
		Vmin and Vstep are minimal voltage and voltage step size respectively.
		For ULT PMOS LDOs, Vmin=1.75 V, Vstep=12.5 mV.

# 0x00015545 LDO22\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph\_rb

Define LDO Mode Transitions

#### LDO22\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE
		0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode
		0x1: BYPASS_ENABLED
		0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B)
	0	0x1: FOLLOW_PMIC_AWAKE_TRUE
	27,48	0x0: FOLLOW_PMIC_AWAKE_FALSE

# 0x00015546 LDO22\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### LDO22\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on 0x1: EN_LDO_INT_TRUE 0x0: EN_LDO_INT_FALSE
0	FOLLOW_HW_EN0	LDO enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

#### 0x00015548 LDO22\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

#### LDO22\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled 0x1: PULLDN_ENABLED 0x0: PULLDN_DIABLED

# 0x0001554A LDO22\_OCP\_CTL1

#### LDO22\_OCP\_CTL1

LDO2	2_OCP_CTL1		
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x80		
Reset N	Name: perph_rb	222	
LDO22	_OCP_CTL1	Com	
Bits	Name	Description	
7	OCP_EN	Enable the OCP feature	
	To Me	0x1: OCP_ENABLED	
	27.5	0x0: OCP_DIABLED	
5	OCP_TEST_MODE	SW write this bit to enable the OCP test mode (current limited)	
		0x1: OCP_TEST_MODE	
		0x0: OCP NORMAL MODE	

#### 0x0001554B LDO22\_OCP\_CTL2

Type: W

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO22\_OCP\_CTL2

Bits	Name	Description
6	OCP_LATCHED_CLR	SW write this bit to clear the OCP_LATCHED status bit 0x1: OCP_LATCHED_CLR

# 0x0001554C LDO22\_SOFT\_START\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph rb

#### LDO22\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED

#### 0x00015552 LDO22\_CONFIG\_CTL

#### LDO22\_CONFIG\_CTL

LDO22_CONFIG_CTL			
Clock:	Type: RW Clock: PBUS_WRCLK Reset State: 0x04		
Reset I	Reset Name: perph_rb		
LDO22	_CONFIG_CTL	02/10	
Bits	Name	Description	
3	ACT_BYPASS_BUFF_EN	0x1: ACT_BYPASS_BUFF_ENABLED 0x0: ACT_BYPASS_BUFF_DISABLED	
2	MODE_TRAN_ENH_EN	PMOS LDO only, when set high, the internal nodes in the error amp are short circuited during NPM?LPM transition 0x1: MODE_TRAN_ENH_ENABLED 0x0: MODE_TRAN_ENH_DISABLED	

# 79 Ldo\_dig Registers

#### 0x00015600 LDO23\_REVISION1

#### LDO23\_REVISION1

LDO2	LDO23_REVISION1		
Clock:	Type: R Clock: PBUS_WRCLK Reset State: 0x00		
Reset 1	Name: n/a		
HW Ve	ersion Register [7:0]		
PMIC_	PMIC_CONSTANT		
LDO23	LDO23_REVISION1		
Bits	Name Description		
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.	

#### 0x00015601 LDO23\_REVISION2

Type: R

Clock: PBUS WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### LDO23\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x00015602 LDO23\_REVISION3

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: n/a

HW Version Register [23:16]

#### LDO23\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x00015603 LDO23 REVISION4

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: n/a

HW Version Register [31:24]

#### LDO23\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 0x00015604 LDO23\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x04

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

#### LDO23\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LDO

#### 0x00015605 LDO23\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x03

Reset Name: n/a

Peripheral SubType

#### LDO23\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	P50 for example

# 0x00015608 LDO23\_STATUS1

Type: R

Clock: PBUS\_WRCLK
Reset State: 0bXX000XX

Reset Name: n/a

Status Registers

#### LDO23\_STATUS1

Bits	Name	Description
7	VREG_OK	VREG output voltage level. VREG_OK is always high when LDO is in bypass mode  0x1: LDO_VOLTAGE_OK  0x0: LDO_VOLTAGE_LOW
	# 0 DETECTED	
5	ILS_DETECTED	upper limit is programmed to a value less than the lower limit 0x1: UPPER_LIMIT_SETTING_ERR
		0x0: UPPER_LIMIT_SETTING_OK
4	UL_VOLTAGE_DETECTED	Last voltage set was above UL_Voltage  0x1: VOLTAGE_LEVEL_SETTING_OVERLIMIT  0x0: VOLTAGE_LEVEL_SETTING_OK

# LDO23\_STATUS1 (cont.)

Bits	Name	Description
3	LL_VOLTAGE_DETECTED	Last voltage set was below LL_Voltage 0x1: VOLTAGE_LEVEL_SETTING_UNDERLIMIT 0x0: VOLTAGE_LEVEL_SETTING_OK
1	NPM_TRUE	VREG_OK and LDO is in NPM 0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK

#### 0x00015609 LDO23\_STATUS2

# LDO23\_STATUS2

1		0x1: NPM_VOLTAGE_OK 0x0: NOT_NPM_OR_VOLTAGE_NOT_OK
Type: Clock: Reset S Reset M	3_STATUS2  R PBUS_WRCLK State: 0b0000000X  Name: n/a Registers  _STATUS2	22.27 RDT
Bits	Name	Description
Bits 7	Name SOFTSTART_DONE	Description indicates that the startup is complete LDO in normal mode 0x1: SOFTSTART_DONE 0x0: SOFTSTART_NOT_DONE
		indicates that the startup is complete LDO in normal mode 0x1: SOFTSTART_DONE
7	SOFTSTART_DONE  OVER_CURRENT_DETECT	indicates that the startup is complete LDO in normal mode 0x1: SOFTSTART_DONE 0x0: SOFTSTART_NOT_DONE current limit of the LDO is reached 0x1: OVER_CURRENT_DETECTED

#### 0x0001560A LDO23\_STATUS3

Type: R

Clock: PBUS WRCLK Reset State: Undefined

Reset Name: n/a

**Status Registers** 

#### LDO23\_STATUS3

Bits	Name	Description
7	LDO_RANGE_SEL	range selection control bit going to LDO 0x1: LDO_RANGE_SELECTED 0x0: LDO_RANGE_NOT_SELECTED
6:0	LDO_VSET	voltage programming bits going to LDO 0x1: LDO_PROGRAM_SELECTED 0x0: LDO_PROGRAM_NOT_SELECTED

#### 0x00015610 LDO23\_INT\_RT\_STS

#### LDO23\_INT\_RT\_STS

		0x0: LDO_PROGRAM_SELECTED  0x0: LDO_PROGRAM_NOT_SELECTED	
LDO2	LDO23_INT_RT_STS		
	R PBUS_WRCLK State: 0x00		
Reset N	Name: n/a		
Interruj	Interrupt Real Time Status Bits		
LDO23	LDO23_INT_RT_STS		
Bits	Name	Description	
1	LIMIT_ERROR_RT_STS	Last voltage set was below or equal to LL_Voltage 0x1: VOLTAGE_LEVEL_SETTING_UNDERLIMIT 0x0: VOLTAGE_LEVEL_SETTING_OK	
0	VREG_OK_RT_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_ERR	

#### 0x00015611 LDO23\_INT\_SET\_TYPE

Type: RW

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO23\_INT\_SET\_TYPE

Bits	Name	Description
1	LIMIT_ERROR_TYPE	Interrupt type, edge or level
		0x1: LIMIT_ERROR_LEVEL_TRIGGERED 0x0: LIMIT_ERROR_EDGE_TRIGGERED

#### LDO23\_INT\_SET\_TYPE (cont.)

Bits	Name	Description
0	VREG_OK_TYPE	Interrupt type, edge or level 0x1: VREG_OK_LEVEL_TRIGGERED 0x0: VREG_OK_EDGE_TRIGGERED

#### 0x00015612 LDO23\_INT\_POLARITY\_HIGH

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** perph\_rb

#### LDO23\_INT\_POLARITY\_HIGH

Bits	Name	Description
1	LIMIT_ERROR_HIGH	Edge type, rising or Level type, high true 0x1: LIMIT_ERROR_HIGH_TRIGGERED 0x0: LIMIT_ERROR_HIGH_DISABLED
0	VREG_OK_HIGH	Edge type, rising or Level type, high true 0x1: VREG_OK_LOW_TRIGGERED 0x0: VREG_OK_LOW_DISABLED

#### 0x00015613 LDO23\_INT\_POLARITY\_LOW

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### LDO23\_INT\_POLARITY\_LOW

Bits	Name	Description
1	LIMIT_ERROR_LOW	Edge type, falling or Level type, low true  0x1: LIMIT_ERROR_RISING_TRIGGERED  0x0: LIMIT_ERROR_FALLING_TRIGGERED
0	VREG_OK_LOW	Edge type, falling or Level type, low true 0x1: VREG_OK_RISING_TRIGGERED 0x0: VREG_OK_FALLING_TRIGGERED

## 0x00015614 LDO23\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing a '1' to this interrupt will rearm the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

#### LDO23\_INT\_LATCHED\_CLR

Bits	Name	Description
1	LIMIT_ERROR_LATCHED_	0x1: LIMIT_ERROR_REARM
	CLR	0x0: LIMIT_ERROR_NOT_REARM
0	VREG_OK_LATCHED_CLR	0x1: VREG_OK_ERROR_REARM
	. (	0x0: VREG_OK_ERROR_NOT_REARM

#### 0x00015615 LDO23\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC\_SET\_MASK

#### LDO23 INT EN SET

Bits	Name	Description
1	LIMIT_ERROR_EN_SET	0x1: LIMIT_ERROR_ENABLED
		0x0: LIMIT_ERROR_DISABLED
0	VREG_OK_EN_SET	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00015616 LDO23\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### LDO23\_INT\_EN\_CLR

Bits	Name	Description
1	LIMIT_ERROR_EN_CLR	0x1: LIMIT_ERROR_ENABLED
		0x0: LIMIT_ERROR_DISABLED
0	VREG_OK_EN_CLR	0x1: VREG_OK_ERROR_ENABLED
		0x0: VREG_OK_ERROR_DISABLED

#### 0x00015618 LDO23\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### LDO23 INT LATCHED STS

Bits	Name	Description
1	LIMIT_ERROR_LATCHED_S TS	Last voltage set was below or equal to LL_Voltage 0x1: VOLTAGE_LEVEL_SETTING_UNDERLIMIT 0x0: VOLTAGE_LEVEL_SETTING_OK
0	VREG_OK_LATCHED_STS	Regulator has been successfully enabled 0x1: LDO_VOLTAGE_LOW 0x0: LDO_VOLTAGE_OK

#### 0x00015619 LDO23\_INT\_PENDING\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Debug: Pending is set if interrupt has been sent but not cleared.

#### LDO23\_INT\_PENDING\_STS

Bits	Name	Description
1	LIMIT_ERROR_PENDING_S TS	Last voltage set was below or equal to LL_Voltage 0x1: VOLTAGE_LEVEL_SETTING_UNDERLIMIT 0x0: VOLTAGE_LEVEL_SETTING_OK
0	VREG_OK_PENDING_STS	Regulator has been successfully enabled 0x1: LDO_ENABLE_SUCCESS 0x0: LDO_ENABLE_FALSE

# 0x0001561A LDO23\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Selects the MID that will receive the interrupt

#### LDO23\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	0x1: INT_MID_SEL_1
	J. S. M. Chr.	0x0: INT_MID_SEL_0

#### 0x0001561B LDO23\_INT\_PRIORITY

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### LDO23\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	0x1: INT_PRIORITY_A 0x0: INT_PRIORITY_SR
		0x0. INT_FRIORITI_5R

### 0x00015640 LDO23\_VOLTAGE\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: perph rb

This register is latched to VOLTAGE\_CTL2 register. Need to write to VOLTAGE\_CTL2 register after writing to this register to update the RANGE value.

#### LDO23\_VOLTAGE\_CTL1

Bits	Name	Description
2:0	RANGE	See details on following sheet

# 0x00015641 LDO23\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x2C

Reset Name: perph\_rb

#### LDO23\_VOLTAGE\_CTL2

Bits		Name	Description
6:0	VSET	30, 24	Voltage = Vmin + VSET*(Vstep)
		1	Vmin and Vstep are minimal voltage and voltage step size respectively.
			For ULT PMOS LDOs, Vmin=0.75 V, Vstep=12.5 mV.

#### 0x00015645 LDO23\_MODE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph\_rb

Define LDO Mode Transitions

#### LDO23\_MODE\_CTL2

Bits	Name	Description
7	NPM	Force NPM
		0x1: FORCED_NPM
		0x0: FORCED_NPM_FALSE

#### LDO23\_MODE\_CTL2 (cont.)

Bits	Name	Description
6	BYPASS_ACT	0x1: BYPASS_ACT_TRUE 0x0: BYPASS_ACT_FALSE
5	BYPASS_EN	Enable LDO bypass mode 0x1: BYPASS_ENABLED 0x0: BYPASS_DISABLED
4	FOLLOW_PMIC_AWAKE	NPM when PMIC_AWAKE (SLEEP_B) 0x1: FOLLOW_PMIC_AWAKE_TRUE 0x0: FOLLOW_PMIC_AWAKE_FALSE
3	NPM_FOLLOW_HW_EN3	NPM mode setting using HWEN3 0x1: NPM_FOLLOW_HW_EN3_TRUE 0x0: NPM_FOLLOW_HW_EN3_FALSE
2	NPM_FOLLOW_HW_EN2	NPM mode setting using HWEN2 0x1: NPM_FOLLOW_HW_EN2_TRUE 0x0: NPM_FOLLOW_HW_EN2_FALSE
1	NPM_FOLLOW_HW_EN1	NPM mode setting using HWEN1 0x1: NPM_FOLLOW_HW_EN1_TRUE 0x0: NPM_FOLLOW_HW_EN1_FALSE
0	NPM_FOLLOW_HW_EN0	NPM mode setting using HWEN0 0x1: NPM_FOLLOW_HW_EN0_TRUE 0x0: NPM_FOLLOW_HW_EN0_FALSE

# 0x00015646 LDO23\_EN\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

## LDO23\_EN\_CTL

Bits	Name	Description
7	EN_LDO_INT	1' = Enable the LDO, '0' = do not force LDO on
		0x1: EN_LDO_INT_TRUE
		0x0: EN_LDO_INT_FALSE
3	FOLLOW_HW_EN3	NPM enable setting using HWEN3
		0x1: FOLLOW_HW_EN3_TRUE
		0x0: FOLLOW_HW_EN3_FALSE
2	FOLLOW_HW_EN2	NPM enable setting using HWEN2
		0x1: FOLLOW_HW_EN2_TRUE
		0x0: FOLLOW_HW_EN2_FALSE

#### LDO23\_EN\_CTL (cont.)

Bits	Name	Description
1	FOLLOW_HW_EN1	NPM enable setting using HWEN1 0x1: FOLLOW_HW_EN1_TRUE 0x0: FOLLOW HW EN1 FALSE
0	FOLLOW_HW_EN0	NPM enable setting using HWEN0 0x1: FOLLOW_HW_EN0_TRUE 0x0: FOLLOW_HW_EN0_FALSE

## 0x00015648 LDO23\_PD\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph\_rb

#### LDO23\_PD\_CTL

Bits	Name	Description
7	PULLDN_EN	Enable the pulldown when the regulator is disabled
		0x1: PULLDN_ENABLED
	22.	0x0: PULLDN_DIABLED

#### 0x0001564A LDO23\_CURRENT\_LIM\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x80

Reset Name: perph\_rb

#### LDO23\_CURRENT\_LIM\_CTL

Bits	Name	Description
7	CURRENT_LIM_EN	0x1: CURRENT_LIM_ENABLED 0x0: CURRENT_LIM_DISABLED
5	CURRENT_LIM_TESTMOD E_EN	Current Limit for test mode (lower limit) 0x1: CURRENT_LIM_TESTMODE_ENABLED 0x0: CURRENT_LIM_TESTMODE_DISABLED

### 0x0001564C LDO23\_SOFT\_START\_CTL

Type: RW

Clock: PBUS WRCLK Reset State: 0x80

Reset Name: perph rb

#### LDO23\_SOFT\_START\_CTL

Bits	Name	Description
7	SOFT_START	0x1: SOFT_START_ENABLED
		0x0: SOFT_START_DISABLED

#### 0x00015652 LDO23\_CONFIG\_CTL

#### LDO23\_CONFIG\_CTL

LDO23_CONFIG_CTL			
Type: RW Clock: PBUS_WRCLK Reset State: 0xF0			
	Reset Name: perph_rb		
LDO23	_CONFIG_CTL	Oam	
Bits	Name	Description	
7:6	CLAMP CTRL		
1.0	CLAIVIP_CTRL	For N1200 LDO only, changes the clamp voltage for undershoot improvement	
5	CLAMP_EN		
	8.0 Willis	improvement  For N1200 LDO only, undershoot improvement  0x1: CLAMP_ENABLED	

#### 0x00015668 LDO23\_LL\_VOLTAGE\_CTL1

Type: RW

Clock: PBUS WRCLK Reset State: 0x00

Reset Name: perph rb

PMIC\_LOCKED=SEC\_ACCESS

#### LDO23\_LL\_VOLTAGE\_CTL1

Bits	Name	Description
2:0	LL_RANGE	See details on following sheet

#### 0x00015669 LDO23\_LL\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

PMIC\_LOCKED=SEC ACCESS

#### LDO23\_LL\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	LL_VSET	See details on following sheet

N

# 0x0001566A LDO23\_UL\_VOLTAGE\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x04

**Reset Name:** perph\_rb

PMIC LOCKED=SEC ACCESS

#### LDO23\_UL\_VOLTAGE\_CTL1

Bits	Name	Description
2:0	UL_RANGE	See details on following sheet

### 0x0001566B LDO23\_UL\_VOLTAGE\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x7F

Reset Name: perph rb

PMIC\_LOCKED=SEC\_ACCESS

#### LDO23\_UL\_VOLTAGE\_CTL2

Bits	Name	Description
6:0	UL_VSET	See details on following sheet

#### 0x000156D0 LDO23\_SEC\_ACCESS

Type: RW

#### LDO23\_SEC\_ACCESS

	PBUS_WRCLK State: 0x00	
Reset Name: dVdd_rb		N
PMIC_LOCKING		N
LDO23	S_SEC_ACCESS	·O,
Bits	Name	Description
	Name	Description

# 80 Pwm\_slice Registers

### 0x0001BC00 PWM\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

PMIC CONSTANT

#### PWM\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

#### 0x0001BC01 PWM\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: N/A

HW Version Register [15:8]

PMIC CONSTANT

#### PWM\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x0001BC04 PWM\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x13

**Reset Name:** N/A

Peripheral Type

PMIC\_CONSTANT

#### PWM\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	LPG

## 0x0001BC05 PWM PERPH SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x0B

Reset Name: N/A

Peripheral SubType

PMIC CONSTANT

#### PWM\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	PWM Channel

#### 0x0001BC41 PWM\_PWM\_SIZE\_CLK

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x04

Reset Name: PERPH\_RB

This register sets the PWM frequency according to the foll. formula

PWM FREQ =

PWM FREQ CLK SELECT/(2^(PWM SIZE))\*(2^(PWM FREQ EXPONENT)\*PWM FRE

Q PRE DIVIDE)

#### PWM\_PWM\_SIZE\_CLK

Bits	Name	Description
2	PWM_SIZE	0 = 6-bit PWM
		1 = 9-bit PWM
		0x0: PWM_6BIT
		0x1: PWM_9BIT
1:0	PWM_FREQ_CLK_SELECT	sets the PWM master clock
		00 = no clock
		01 = 1 kHz
		10 = 32 kHz
		11 = 19.2 MHz
		0x0: NOCLK
		0x1: CLK_1KHZ
		0x2: CLK_32KHZ
		0x3: CLK_19P2MHZ

# 0x0001BC42 PWM\_PWM\_FREQ\_PREDIV\_CLK

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

This register selects the pre-divide and exponent values to divide down the PWM master clock

#### PWM\_PWM\_FREQ\_PREDIV\_CLK

Bits	Name	Description
6:5	PWM_FREQ_PRE_DIVIDE	00 = 1
		01 = 3
		10 = 5
		11 = 6
		0x0: PREDIV_ONE
		0x1: PREDIV_THREE
		0x2: PREDIV_FIVE
		0x3: PREDIV_SIX

#### PWM\_PWM\_FREQ\_PREDIV\_CLK (cont.)

Bits	Name	Description
2:0	PWM_FREQ_EXPONENT	000 = 0
		001 = 1
		111 = 7
		0x0: EXP_ZERO
		0x1: EXP_ONE
		0x2: EXP_TWO
		0x3: EXP_THREE
		0x4: EXP_FOUR
		0x5: EXP_FIVE
		0x6: EXP_SIX
		0x7: EXP_SEVEN
1		

# 0x0001BC43 PWM\_PWM\_TYPE\_CONFIG

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH\_RB

#### **PWM PWM TYPE CONFIG**

Bits	Name	Description
5	EN_GLITCH_REMOVAL	0 = no glitch removal, PWM outputs are updated immediately 1 = glitch removal, PWM outputs are updated only on PWM period boundaries 0x0: GLITCH_REMOVE_DIS 0x1: GLITCH_REMOVE_EN

#### 0x0001BC44 PWM\_PWM\_VALUE\_LSB

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH\_RB

PWM VALUE LSB

#### PWM\_PWM\_VALUE\_LSB

Bits	Name	Description
7:0	PWM_VALUE_LSB	lower 8 bits of PWM

#### 0x0001BC45 PWM\_PWM\_VALUE\_MSB

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PWM VALUE MSB

#### PWM\_PWM\_VALUE\_MSB

Bits	Name	Description
0	PWM_VALUE_MSB	MSB (bit 9) of PWM

### 0x0001BC46 PWM\_ENABLE\_CONTROL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

Enables PWM output

#### PWM\_ENABLE\_CONTROL

Bits	Name	Description
7	EN_MODULE	0 = Module disabled (High Z)
		1 = Module enabled
		0x0: PWM_DISABLE
		0x1: PWM_ENABLE

#### 0x0001BC47 PWM\_PWM\_SYNC

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

#### PWM\_PWM\_SYNC

Bits	Name	Description
0	SYNC_PWM	Writing 1 to this register will update the 6/9-bit PWM value. This bit is auto-cleared

# 81 Codec\_digital Registers

### 0x0001F000 CDC\_D\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### CDC\_D\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

## 0x0001F001 CDC\_D\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [15:8]

PMIC\_CONSTANT

#### CDC\_D\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x0001F004 CDC\_D\_PERPH\_TYPE

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x23

Reset Name: n/a

Peripheral Type

PMIC CONSTANT

#### CDC\_D\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	

## 0x0001F005 CDC D PERPH SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x03

Reset Name: n/a

Peripheral SubType

PMIC CONSTANT

#### CDC\_D\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	

#### 0x0001F010 CDC\_D\_INT\_RT\_STS

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### CDC\_D\_INT\_RT\_STS

Bits	Name	Description
7	MBHC_SWITCH_INT	

#### CDC\_D\_INT\_RT\_STS (cont.)

Bits	Name	Description
6	MBHC_MIC_ELECTRICAL_I NS_REM_DET	
5	MBHC_BUTTON_PRESS_D ET	
4	MBHC_BUTTON_RELEASE _DET	
3	MBHC_MIC_ELECTRICAL_I NS_REM_DET1	
2	D_CDC_SPKR_OCP_INT	72
1	D_CDC_SPKR_CLIP_INT	
0	D_CDC_SPKR_CNP_INT	

# 0x0001F011 CDC\_D\_INT\_SET\_TYPE

Type: R

Clock: PBUS\_WRCLK
Reset State: 0xFF

Reset Name: perph\_rb

0 = use level trigger interrupts, 1 = use edge trigger interrupts

# CDC\_D\_INT\_SET\_TYPE

Bits	Name	Description
7	MBHC_SWITCH_INT	Read register description above
6	MBHC_MIC_ELECTRICAL_I NS_REM_DET	Read register description above
5	MBHC_BUTTON_PRESS_D ET	Read register description above
4	MBHC_BUTTON_RELEASE _DET	Read register description above
3	MBHC_MIC_ELECTRICAL_I NS_REM_DET1	Read register description above
2	D_CDC_SPKR_OCP_INT	Read register description above
1	D_CDC_SPKR_CLIP_INT	Read register description above
0	D_CDC_SPKR_CNP_INT	Read register description above

#### 0x0001F012 CDC\_D\_INT\_POLARITY\_HIGH

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0xFF

Reset Name: perph rb

1 = Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### CDC\_D\_INT\_POLARITY\_HIGH

Bits	Name	Description
7	MBHC_SWITCH_INT	Read register description above
6	MBHC_MIC_ELECTRICAL_I NS_REM_DET	Read register description above
5	MBHC_BUTTON_PRESS_D ET	Read register description above
4	MBHC_BUTTON_RELEASE _DET	Read register description above
3	MBHC_MIC_ELECTRICAL_I NS_REM_DET1	Read register description above
2	D_CDC_SPKR_OCP_INT	Read register description above
1	D_CDC_SPKR_CLIP_INT	Read register description above
0	D_CDC_SPKR_CNP_INT	Read register description above

### 0x0001F013 CDC\_D\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

#### CDC\_D\_INT\_POLARITY\_LOW

Bits	Name	Description
7	MBHC_SWITCH_INT	Read register description above
6	MBHC_MIC_ELECTRICAL_I NS_REM_DET	Read register description above
5	MBHC_BUTTON_PRESS_D ET	Read register description above

#### CDC\_D\_INT\_POLARITY\_LOW (cont.)

Bits	Name	Description
4	MBHC_BUTTON_RELEASE _DET	Read register description above
3	MBHC_MIC_ELECTRICAL_I NS_REM_DET1	Read register description above
2	D_CDC_SPKR_OCP_INT	Read register description above
1	D_CDC_SPKR_CLIP_INT	Read register description above
0	D_CDC_SPKR_CNP_INT	Read register description above

## 0x0001F014 CDC\_D\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

1 = rearms the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

0 = has no effect

#### CDC\_D\_INT\_LATCHED\_CLR

Bits	Name	Description
7	MBHC_SWITCH_INT	Read register description above
6	MBHC_MIC_ELECTRICAL_I NS_REM_DET	Read register description above
5	MBHC_BUTTON_PRESS_D ET	Read register description above
4	MBHC_BUTTON_RELEASE _DET	Read register description above
3	MBHC_MIC_ELECTRICAL_I NS_REM_DET1	Read register description above
2	D_CDC_SPKR_OCP_INT	Read register description above
1	D_CDC_SPKR_CLIP_INT	Read register description above
0	D_CDC_SPKR_CNP_INT	Read register description above

#### 0x0001F015 CDC\_D\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt.

Reading this register will readback enable status

PMIC\_SET\_MASK

#### CDC\_D\_INT\_EN\_SET

Bits	Name	Description
7	MBHC_SWITCH_INT	Read register description above
6	MBHC_MIC_ELECTRICAL_I NS_REM_DET	Read register description above
5	MBHC_BUTTON_PRESS_D ET	Read register description above
4	MBHC_BUTTON_RELEASE _DET	Read register description above
3	MBHC_MIC_ELECTRICAL_I NS_REM_DET1	Read register description above
2	D_CDC_SPKR_OCP_INT	Read register description above
1	D_CDC_SPKR_CLIP_INT	Read register description above
0	D_CDC_SPKR_CNP_INT	Read register description above

#### 0x0001F016 CDC\_D\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### CDC\_D\_INT\_EN\_CLR

Bits	Name	Description
7	MBHC_SWITCH_INT	Read register description above

#### CDC\_D\_INT\_EN\_CLR (cont.)

Bits	Name	Description
6	MBHC_MIC_ELECTRICAL_I NS_REM_DET	Read register description above
5	MBHC_BUTTON_PRESS_D ET	Read register description above
4	MBHC_BUTTON_RELEASE _DET	Read register description above
3	MBHC_MIC_ELECTRICAL_I NS_REM_DET1	Read register description above
2	D_CDC_SPKR_OCP_INT	Read register description above
1	D_CDC_SPKR_CLIP_INT	Read register description above
0	D_CDC_SPKR_CNP_INT	Read register description above

# 0x0001F018 CDC\_D\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### CDC\_D\_INT\_LATCHED\_STS

Bits	Name	Description
7	MBHC_SWITCH_INT	
6	MBHC_MIC_ELECTRICAL_I NS_REM_DET	
5	MBHC_BUTTON_PRESS_D ET	
4	MBHC_BUTTON_RELEASE _DET	
3	MBHC_MIC_ELECTRICAL_I NS_REM_DET1	
2	D_CDC_SPKR_OCP_INT	
1	D_CDC_SPKR_CLIP_INT	
0	D_CDC_SPKR_CNP_INT	

# 0x0001F019 CDC\_D\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

Pending is set if interrupt has been sent but not cleared.

#### CDC\_D\_INT\_PENDING\_STS

Bits	Name	Description
7	MBHC_SWITCH_INT	2
6	MBHC_MIC_ELECTRICAL_I NS_REM_DET	
5	MBHC_BUTTON_PRESS_D ET	0.
4	MBHC_BUTTON_RELEASEDET	1 POT
3	MBHC_MIC_ELECTRICAL_I NS_REM_DET1	02.00
2	D_CDC_SPKR_OCP_INT	
1	D_CDC_SPKR_CLIP_INT	
0	D_CDC_SPKR_CNP_INT	

## 0x0001F01A CDC\_D\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

Selects the MID that will receive the interrupt

#### CDC\_D\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	indicates ID of the master which is supposed to process the interrupt

#### 0x0001F01B CDC\_D\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Choosing priority type - SR or A

#### CDC\_D\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	Writing 0 selects SR priority, writing 1 selects A priority.

#### 0x0001F043 CDC\_D\_PIN\_STATUS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

These register bits contain the current state of the pads to allow software, read access.

#### CDC\_D\_PIN\_STATUS

Bits	Name	Description
4	PAD_STATUS4	State of the cdc_pdm_clk pad
3	PAD_STATUS3	State of the cdc_pdm_sync pad
2	PAD_STATUS2	State of the cdc_pdm_rx2 pad
1	PAD_STATUS1	State of the cdc_pdm_rx1 pad
0	PAD_STATUS0	State of the cdc_pdm_rx0 pad

#### 0x0001F044 CDC\_D\_HDRIVE\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

PDM Buffer Drive Strength Configuration

#### CDC\_D\_HDRIVE\_CTL

Bits	Name	Description
1:0	HDRIVE_CTL	0x0: LOW10PF
		0x1: MID20PF
		0x2: HIGH40PF
		0x3: VERYHIGH50PF

## 0x0001F046 CDC\_D\_CDC\_RST\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### CDC\_D\_CDC\_RST\_CTL

Bits	Name		Description
7	DIG_SW_RST_N	202	CDC_DIG_RST_N (active low) is AND with System Reset to generate the Digital core reset.  0x0: RESET  0x1: REMOVE_RESET

#### 0x0001F048 CDC D CDC TOP CLK CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Top ClockControl Register. This register enables or disables the registers in the Main Clock

**Domains** 

#### CDC\_D\_CDC\_TOP\_CLK\_CTL

Bits	Name	Description
3	A_MCLK2_EN	Specifies Analog MCLK Div by 2 Clock EnableState 0x0: DISABLE 0x1: ENABLE
2	A_MCLK_EN	Specifies Analog MCLK Clock EnableState 0x0: DISABLE 0x1: ENABLE

#### 0x0001F049 CDC\_D\_CDC\_ANA\_CLK\_CTL

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

RX Analog Path Clock Control Register. This register enables clocks to Analog RX domains.

#### CDC\_D\_CDC\_ANA\_CLK\_CTL

Bits	Name	Description
5	TXA_CLK25_EN	Specifies TX0 and Tx1 Analog Path Clock Enable State
		0x0: DISABLE
		0x1: ENABLE
4	SPKR_CLK_EN	Specifies RX4 Analog Path Clock Enable State
		0x0: DISABLE
		0x1: ENABLE
1	EAR_HPHL_CLK_EN	Specifies RX1 Analog Path Clock Enable State
		0x0: DISABLE
		0x1: ENABLE
0	EAR_HPHR_CLK_EN	Specifies RX0 Analog Path Clock Enable State
	27.0	0x0: DISABLE
	Og ingl	0x1: ENABLE

#### 0x0001F04A CDC\_D\_CDC\_DIG\_CLK\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

This register enables clocks to all of the main digital data paths

#### CDC\_D\_CDC\_DIG\_CLK\_CTL

Bits	Name	Description
7	RXD_PDM_CLK_EN	Specifies RXD_PDM Digital Path Clock Enable State 0x0: DISABLE 0x1: ENABLE
6	NCP_CLK_EN	Specifies NCP Digital Path Clock Enable State 0x0: DISABLE 0x1: ENABLE

#### CDC\_D\_CDC\_DIG\_CLK\_CTL (cont.)

Bits	Name	Description
5	BOOST_CLK_EN	Specifies BOOST Digital Path Clock Enable State 0x0: DISABLE 0x1: ENABLE
4	TXD_CLK_EN	Specifies TX Digital Path Clock Enable State 0x0: DISABLE 0x1: ENABLE
3	D_MBHC_CLK_EN	Specifies Digital MBHC Clock EnableState 0x0: DISABLE 0x1: ENABLE
2	RXD3_CLK_EN	Specifies RX3 Digital Path Clock Enable State 0x0: DISABLE 0x1: ENABLE
1	RXD2_CLK_EN	Specifies RX2 Digital Path Clock Enable State 0x0: DISABLE 0x1: ENABLE
0	RXD1_CLK_EN	Specifies RX1 Digital Path Clock Enable State 0x0: DISABLE 0x1: ENABLE

## 0x0001F050 CDC\_D\_CDC\_CONN\_TX1\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: perph\_rb

#### CDC\_D\_CDC\_CONN\_TX1\_CTL

Bits	Name	Description
1:0	SERIAL_TX1_MUX	Configures connectivity mux, to choose the input to serializer in the TX1 path 0x0: ADC_1 0x1: RX_PDM_LB 0x2: ZERO

## 0x0001F051 CDC\_D\_CDC\_CONN\_TX2\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x02

#### CDC\_D\_CDC\_CONN\_TX2\_CTL

Bits	Name	Description
1:0	SERIAL_TX2_MUX	Configures connectivity mux, to choose the input to serializer in the TX2 path 0x0: ADC_2 0x1: RX_PDM_LB 0x2: ZERO

# 0x0001F052 CDC\_D\_CDC\_CONN\_HPHR\_DAC\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### CDC\_D\_CDC\_CONN\_HPHR\_DAC\_CTL

Bits	Name	Description
0	RX_SEL	Configures connectivity mux, to choose the input to HPHR DAC input path.  0x0: RX1  0x1: RX2

#### 0x0001F053 CDC\_D\_CDC\_CONN\_RX1\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### CDC\_D\_CDC\_CONN\_RX1\_CTL

Bits	Name	Description
1:0	RX1_INP_SEL	Configures connectivity mux, to choose the serial input to the deserializer in the RX1 input path.
		0x0: RX1
		0x1: TX_LB_ADC1
		0x2: TX_LB_ADC2

#### 0x0001F054 CDC\_D\_CDC\_CONN\_RX2\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### CDC\_D\_CDC\_CONN\_RX2\_CTL

Bits	Name	Description
1:0	RX2_INP_SEL	Configures connectivity mux, to choose the serial input to the deserializer in the RX2 input path.
		0x0: RX2
		0x1: TX_LB_ADC1
		0x2: TX_LB_ADC2

## 0x0001F055 CDC\_D\_CDC\_CONN\_RX3\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph rb

#### CDC\_D\_CDC\_CONN\_RX3\_CTL

Bits	Name	Description
1:0	RX3_INP_SEL	Configures connectivity mux, to choose the serial input to the deserializer in the RX3 input path.  0x0: RX3  0x1: TX_LB_ADC1  0x2: TX_LB_ADC2

#### 0x0001F056 CDC\_D\_CDC\_CONN\_RX\_LB\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### CDC\_D\_CDC\_CONN\_RX\_LB\_CTL

Bits	Name	Description
1:0	RX_LB_SEL	Configures connectivity mux, to choose loopback Rx fir data.  0x0: RX1_FIR_DATA  0x1: RX2_FIR_DATA  0x2: RX3_FIR_DATA

## 0x0001F058 CDC\_D\_CDC\_RX\_CTL1

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x7C

Reset Name: perph\_rb

#### CDC\_D\_CDC\_RX\_CTL1

Bits	Name	Description
6	DEM_DITHER_ENABLE	When set to 1, enables Dither bits generation, defaults to 1 0x0: DISABLE 0x1: ENABLE
5	DEM_MID_ENABLE	When set to 1, enables Mid bits generation, defaults to 1 0x0: DISABLE 0x1: ENABLE
4	DEM_MOD_SWITCHING_B LOCK_ENABLE	When set to 1, enables Modified Switching Block (S41), defaults to 1 0x0: DISABLE 0x1: ENABLE
3	DEM_SWITCHING_BLOCK_ ENABLE	When set to 1, enables Switching Block, defaults to 1 0x0: DISABLE 0x1: ENABLE
2	DEM_SEGMENTING_BLOC K_ENABLE	When set to 1, enables Segmenting Block, defaults to 1 0x0: DISABLE 0x1: ENABLE
1	DEM_BYPASS	DEM bypass test data (26 bits) is defined by the 4 DEM_BYPASS_DATA registers, described later in this document. 0x0: NO_BYPASS 0x1: BYPASS
0	FIR_BYPASS	When set = 1, enables the bypass of the FIR filter. Only lower 4 bits of 9 bit output will be non zero. Default to 0.  0x0: NO_BYPASS  0x1: BYPASS

## 0x0001F059 CDC\_D\_CDC\_RX\_CTL2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x7C

#### CDC\_D\_CDC\_RX\_CTL2

Bits	Name	Description
6	DEM_DITHER_ENABLE	When set to 1, enables Dither bits generation, defaults to 1 0x0: DISABLE 0x1: ENABLE
5	DEM_MID_ENABLE	When set to 1, enables Mid bits generation, defaults to 1 0x0: DISABLE 0x1: ENABLE
4	DEM_MOD_SWITCHING_B LOCK_ENABLE	When set to 1, enables Modified Switching Block (S41), defaults to 1 0x0: DISABLE 0x1: ENABLE
3	DEM_SWITCHING_BLOCK_ ENABLE	When set to 1, enables Switching Block, defaults to 1 0x0: DISABLE 0x1: ENABLE
2	DEM_SEGMENTING_BLOC K_ENABLE	When set to 1, enables Segmenting Block, defaults to 1 0x0: DISABLE 0x1: ENABLE
1	DEM_BYPASS	DEM bypass test data (26 bits) is defined by the 4 DEM_BYPASS_DATA registers, described later in this document. 0x0: NO_BYPASS 0x1: BYPASS
0	FIR_BYPASS	When set = 1, enables the bypass of the FIR filter. Only lower 4 bits of 9 bit output will be non zero. Default to 0.  0x0: NO_BYPASS  0x1: BYPASS

## 0x0001F05A CDC\_D\_CDC\_RX\_CTL3

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x7C

Reset Name: perph\_rb

#### CDC\_D\_CDC\_RX\_CTL3

Bits	Name	Description
6	DEM_DITHER_ENABLE	When set to 1, enables Mid bits generation, defaults to 1 0x0: DISABLE 0x1: ENABLE
5	DEM_MID_ENABLE	When set to 1, enables Dither bits generation, defaults to 1 0x0: DISABLE 0x1: ENABLE

#### CDC\_D\_CDC\_RX\_CTL3 (cont.)

Bits	Name	Description
4	DEM_MOD_SWITCHING_B LOCK_ENABLE	When set to 1, enables Modified Switching Block (S41), defaults to 1 0x0: DISABLE 0x1: ENABLE
3	DEM_SWITCHING_BLOCK_ ENABLE	When set to 1, enables Switching Block, defaults to 1 0x0: DISABLE 0x1: ENABLE
2	DEM_SEGMENTING_BLOC K_ENABLE	When set to 1, enables Segmenting Block, defaults to 1 0x0: DISABLE 0x1: ENABLE
1	DEM_BYPASS	DEM bypass test data (26 bits) is defined by the 4 DEM_BYPASS_DATA registers, described later in this document. 0x0: NO_BYPASS 0x1: BYPASS
0	FIR_BYPASS	When set = 1, enables the bypass of the FIR filter. Only lower 4 bits of 9 bit output will be non zero. Default to 0. 0x0: NO_BYPASS 0x1: BYPASS

## 0x0001F05B CDC\_D\_DEM\_BYPASS\_DATA0

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

#### CDC\_D\_DEM\_BYPASS\_DATA0

Bits	Name	Description
7:0	DEM_BYPASS_DATA0	Lowest 8 bits of 26 bit DEM output test data field for DEM bypass testing

## 0x0001F05C CDC\_D\_DEM\_BYPASS\_DATA1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

#### CDC\_D\_DEM\_BYPASS\_DATA1

Bits	Name	Description
7:0	DEM_BYPASS_DATA0	bits 8 to 15 of 26 bit DEM output test data field for DEM bypass testing

#### 0x0001F05D CDC\_D\_DEM\_BYPASS\_DATA2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### CDC\_D\_DEM\_BYPASS\_DATA2

Bits	Name	Description
7:0	DEM_BYPASS_DATA0	bits 16 to 24 of 26 bit DEM output test data field for DEM bypass testing

## 0x0001F05E CDC\_D\_DEM\_BYPASS\_DATA3

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### CDC\_D\_DEM\_BYPASS\_DATA3

Bits	Name	Description
1:0	DEM_BYPASS_DATA0	upper 2 bits of 26 bit DEM output test data field for DEM bypass testing

# 82 Codec\_analog Registers

#### 0x0001F100 CDC\_A\_REVISION1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [7:0]

PMIC CONSTANT

#### CDC\_A\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x0001F101 CDC\_A\_REVISION2

**Type:** R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

HW Version Register [15:8]

PMIC CONSTANT

#### CDC\_A\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x0001F102 CDC\_A\_REVISION3

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: n/a

HW Version Register [23:16]

#### CDC\_A\_REVISION3

Bits	Name	Description
7:0	ANA_MINOR	This number is incremented for analog change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Software changes may be required to take advantage of the new features. Minor resets to zero when Major increments.

#### 0x0001F103 CDC\_A\_REVISION4

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: n/a

HW Version Register [31:24]

#### CDC\_A\_REVISION4

Bits	Name	Description
7:0	ANA_MAJOR	This number is incremented when changes are made to the analog HW that are not backwards compatible with existing software.

#### 0x0001F104 CDC\_A\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x23

Reset Name: n/a

Peripheral Type

PMIC\_CONSTANT

#### CDC\_A\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	

#### 0x0001F105 CDC\_A\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x0B

Reset Name: n/a

Peripheral SubType

PMIC CONSTANT

#### CDC A PERPH SUBTYPE

l	Bits	Name	Description
	7:0	SUBTYPE	oi.

#### 0x0001F110 CDC\_A\_INT\_RT\_STS

Type: R

Clock: PBUS\_WRCLK

Reset State: 0x00

Reset Name: n/a

Interrupt Real Time Status Bits

#### CDC\_A\_INT\_RT\_STS

Bits	Name	Description
5	D_CDC_HPHL_CNP_INT	0 =
		1 =
4	D_CDC_HPHR_CNP_INT	1 = 0 =
3	D_CDC_EAR_CNP_INT	1 = 0 =
2	D_CDC_HPHL_OCP_INT	1 = 0 =

#### CDC\_A\_INT\_RT\_STS (cont.)

Bits	Name	Description
1	D_CDC_HPHR_OCP_INT	1 =
		0 =
0	D_CDC_EAR_OCP_INT	1 =
		0 =

#### 0x0001F111 CDC\_A\_INT\_SET\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x3F

Reset Name: perph\_rb

0 =use level trigger interrupts, 1 =use edge trigger interrupts

## CDC\_A\_INT\_SET\_TYPE

Bits	Name	Description
5	D_CDC_HPHL_CNP_INT	Read register description above
4	D_CDC_HPHR_CNP_INT	Read register description above
3	D_CDC_EAR_CNP_INT	Read register description above
2	D_CDC_HPHL_OCP_INT	Read register description above
1	D_CDC_HPHR_OCP_INT	Read register description above
0	D_CDC_EAR_OCP_INT	Read register description above

#### 0x0001F112 CDC\_A\_INT\_POLARITY\_HIGH

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x3F

Reset Name: perph\_rb

1 = Interrupt will trigger on a level high (rising edge) event, 0 = level high triggering is disabled

#### CDC\_A\_INT\_POLARITY\_HIGH

Bits	Name	Description
5	D_CDC_HPHL_CNP_INT	Read register description above
4	D_CDC_HPHR_CNP_INT	Read register description above
3	D_CDC_EAR_CNP_INT	Read register description above

#### CDC\_A\_INT\_POLARITY\_HIGH (cont.)

Bits	Name	Description
2	D_CDC_HPHL_OCP_INT	Read register description above
1	D_CDC_HPHR_OCP_INT	Read register description above
0	D_CDC_EAR_OCP_INT	Read register description above

#### 0x0001F113 CDC\_A\_INT\_POLARITY\_LOW

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

1 = Interrupt will trigger on a level low (falling edge) event, 0 = level low triggering is disabled

#### CDC\_A\_INT\_POLARITY\_LOW

Bits	Name	Description
5	D_CDC_HPHL_CNP_INT	Read register description above
4	D_CDC_HPHR_CNP_INT	Read register description above
3	D_CDC_EAR_CNP_INT	Read register description above
2	D_CDC_HPHL_OCP_INT	Read register description above
1	D_CDC_HPHR_OCP_INT	Read register description above
0	D_CDC_EAR_OCP_INT	Read register description above

## 0x0001F114 CDC\_A\_INT\_LATCHED\_CLR

Type: W

Clock: PBUS\_WRCLK Reset State: 0x00

**Reset Name:** perph\_rb

1 = rearms the interrupt when an interrupt is pending. It clears the internal sticky and sent bits

0 = has no effect

#### CDC\_A\_INT\_LATCHED\_CLR

Bits	Name	Description
5	D_CDC_HPHL_CNP_INT	Read register description above
4	D_CDC_HPHR_CNP_INT	Read register description above

#### CDC\_A\_INT\_LATCHED\_CLR (cont.)

Bits	Name	Description
3	D_CDC_EAR_CNP_INT	Read register description above
2	D_CDC_HPHL_OCP_INT	Read register description above
1	D_CDC_HPHR_OCP_INT	Read register description above
0	D_CDC_EAR_OCP_INT	Read register description above

#### 0x0001F115 CDC\_A\_INT\_EN\_SET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

writing '0' to this register has no effect. Writing a '1' will enable the corresponding interrupt. Reading this register will readback enable status

PMIC SET MASK

#### CDC\_A\_INT\_EN\_SET

Bits	Name	Description
5	D_CDC_HPHL_CNP_INT	Read register description above
4	D_CDC_HPHR_CNP_INT	Read register description above
3	D_CDC_EAR_CNP_INT	Read register description above
2	D_CDC_HPHL_OCP_INT	Read register description above
1	D_CDC_HPHR_OCP_INT	Read register description above
0	D_CDC_EAR_OCP_INT	Read register description above

#### 0x0001F116 CDC\_A\_INT\_EN\_CLR

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

writing '0' to this register has no effect. Writing a '1' will disable the corresponding interrupt. Reading this register will readback enable status

PMIC CLR MASK=INT EN SET

#### CDC\_A\_INT\_EN\_CLR

Bits	Name	Description
5	D_CDC_HPHL_CNP_INT	Read register description above
4	D_CDC_HPHR_CNP_INT	Read register description above
3	D_CDC_EAR_CNP_INT	Read register description above
2	D_CDC_HPHL_OCP_INT	Read register description above
1	D_CDC_HPHR_OCP_INT	Read register description above
0	D_CDC_EAR_OCP_INT	Read register description above

## 0x0001F118 CDC\_A\_INT\_LATCHED\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit.

#### CDC\_A\_INT\_LATCHED\_STS

Bits	Name	Description
5	D_CDC_HPHL_CNP_INT	Read register description above
4	D_CDC_HPHR_CNP_INT	Read register description above
3	D_CDC_EAR_CNP_INT	Read register description above
2	D_CDC_HPHL_OCP_INT	Read register description above
1	D_CDC_HPHR_OCP_INT	Read register description above
0	D_CDC_EAR_OCP_INT	Read register description above

#### 0x0001F119 CDC\_A\_INT\_PENDING\_STS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: n/a

Pending is set if interrupt has been sent but not cleared.

#### CDC\_A\_INT\_PENDING\_STS

Bits	Name	Description
5	D_CDC_HPHL_CNP_INT	Read register description above
4	D_CDC_HPHR_CNP_INT	Read register description above
3	D_CDC_EAR_CNP_INT	Read register description above
2	D_CDC_HPHL_OCP_INT	Read register description above
1	D_CDC_HPHR_OCP_INT	Read register description above
0	D_CDC_EAR_OCP_INT	Read register description above

#### 0x0001F11A CDC\_A\_INT\_MID\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

Selects the MID that will receive the interrupt

#### CDC\_A\_INT\_MID\_SEL

Bits	Name	Description
1:0	INT_MID_SEL	indicates ID of the master which is supposed to process the interrupt

#### 0x0001F11B CDC\_A\_INT\_PRIORITY

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

Choosing priority type - SR or A

#### CDC\_A\_INT\_PRIORITY

Bits	Name	Description
0	INT_PRIORITY	

## 0x0001F140 CDC\_A\_MICB\_1\_EN

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### CDC\_A\_MICB\_1\_EN

Bits	Name	Description
7	MICB_EN	0x0: DISABLE
		0x1: ENABLE
6	CAP_MODE	0x0: EXT_BYP_CAP
		0x1: NO_EXT_BYP_CAP
5	PULL_DOWN_EN	0x0: DISABLE
		0x1: ENABLE
4	PULL_UP_EN	0x0: DISABLE
		0x1: ENABLE
3:1	OPA_STG3_TAIL_CURR	0x0: I_30_UA
		0x1:1_45_UA
		0x2: I_60_UA
	0	0x3: I_75_UA
	2 2	0x4: I_90_UA
	,0° ,in <sup>0</sup>	0x5: I_105_UA
	18. O. M.	0x6: I_120_UA
	20 54	0x7: I_135_UA
0	TX3N_GND_SEL	0x0: TX_GND
		0x1: HPH_REF

## 0x0001F141 CDC\_A\_MICB\_1\_VAL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x20

## CDC\_A\_MICB\_1\_VAL

Bits	Name	Description
7:3	MICB_OUT_VAL	0x0: V1P60V
		0x1: V1P65V
		0x2: V1P70V
		0x3: V1P75V
		0x4: V1P80V
		0x5: V1P85V
		0x6: V1P90V
		0x7: V1P95V
		0x8: V2P00V
		0x9: V2P05V
		0xA: V2P10V
		0xB: V2P15V
		0xC: V2P20V
		0xD: V2P25V
	10	0xE: V2P30V
		0xF: V2P35V
		0x10: V2P40V
		0x11: V2P45
		0x12: V2P50V
	,0,	0x13: V2P55V
	2,18	0x14: V2P60V
	10 in	0x15: V2P65V
	2018:09:21 III.	0x16: V2P70V
	30, 24	0x17: V2P75V 0x18: V2P80V
	1	0x19: V2P80V
		0X19. V2F03V
2:1	IFILT_RES_VAL	0x0: R_3600M_OHM
		0x1: R_1800M_OHM
		0x2: R_1200M_OHM
		0x3: R_900M_OHM
0	MICB_PWR_SWCH_OVRD_	0x0: AUTO
	EN	0x1: VDD_MIC_BIAS

## 0x0001F142 CDC\_A\_MICB\_1\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

#### CDC\_A\_MICB\_1\_CTL

Bits	Name	Description
7	REF_OPA_EN	0x0: DISABLE
		0x1: ENABLE
6	INT_PRECHRG_BYP	0x0: INT_PRECHRG_SEL
		0x1: EXT_PRECHRG_SEL
5	EXT_PRECHRG_EN	0x0: DISABLE
		0x1: ENABLE
4:2	RESERVED	
1	CFILT_REF_SEL	0x0: CDC_GND_CFILT
		0x1: HPH_REF
0	PLUG_PNP_OVRD	0x0: ENABLE
		0x1: DISABLE

## 0x0001F143 CDC\_A\_MICB\_1\_INT\_RBIAS

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x49

Reset Name: perph\_rb

## CDC\_A\_MICB\_1\_INT\_RBIAS

Bits	Name	Description
7	TX1_INT_RBIAS_EN	0x0: DISABLE 0x1: ENABLE
6	TX1N_INT_PULLUP_EN	0x0: TX1N_TO_GND 0x1: TX1N_TO_MBIAS
5	TX1N_GND_SEL	0x0: TX_GND 0x1: HPH_REF
4	TX2_INT_RBIAS_EN	0x0: DISABLE 0x1: ENABLE
3	TX2N_INT_PULLUP_EN	0x0: TX2N_TO_GND 0x1: TX2N_TO_MBIAS
2	TX2N_GND_SEL	0x0: TX_GND 0x1: HPH_REF
1	TX3_INT_RBIAS_EN	0x0: DISABLE 0x1: ENABLE
0	TX3_INT_PULLUP_EN	0x0: TX2N_TO_GND 0x1: TX2N_TO_MBIAS

## 0x0001F144 CDC\_A\_MICB\_2\_EN

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x20

Reset Name: perph rb

#### CDC\_A\_MICB\_2\_EN

Bits	Name	Description
7	MICB_EN	0x0: DISABLE
		0x1: ENABLE
6	PULL_UP_EN	0x0: DISABLE
		0x1: ENABLE
5	PULL_DOWN_EN	0x0: DISABLE
		0x1: ENABLE
4:3	MBHC_AZ_CTL	0x0: DEFAULT_AZ_EQ_MICB_EN_B
		0x1: DISABLE_AZ
		0x2: ENABLE_AZ
2:0	ZDET_IBIAS_CTRL	0x0: ZDET_IBIAS_1UA
		0x1: ZDET_IBIAS_4UA
		0x2: ZDET_IBIAS_11UA
	27 18	0x3: ZDET_IBIAS_14UA
	O'S airig	0x4: ZDET_IBIAS_0P5UA
	18, 164	0x5: ZDET_IBIAS_2UA
	20, 24	0x6: ZDET_IBIAS_5P5UA
	1	0x7: ZDET_IBIAS_7UA

## 0x0001F145 CDC\_A\_TX\_1\_2\_ATEST\_CTL\_2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

## CDC\_A\_TX\_1\_2\_ATEST\_CTL\_2

Bits	Name	Description
7:2	RESERVED	RESERVED
1	TX1N_FLOAT_EN	0: DISABLE 1: ENABLE
0	TX1N_CFILT_REF_SEL	0: CFILT_REF 1: IN1_M

## 0x0001F146 CDC\_A\_MASTER\_BIAS\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### CDC\_A\_MASTER\_BIAS\_CTL

Bits	Name	Description
5	MASTER_BIAS_EN	0x0: DISABLE
		0x1: ENABLE
4	V2I_BUFFER_EN	0x0: DISABLE
		0x1: ENABLE
3:2	RESERVED	
1	RESERVED	
0	SPKR_BIAS	0x0: IPOLY
	.0	0x1: ITRIM

## 0x0001F147 CDC\_A\_MBHC\_DET\_CTL\_1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x35

Reset Name: perph rb

#### CDC\_A\_MBHC\_DET\_CTL\_1

Bits	Name	Description
7	L_DET_EN	0x0: DISABLE
		0x1: ENABLE
6	GND_DET_EN	0x0: DISABLE
		0x1: ENABLE
5	MECH_DETECTION_TYPE	0x0: REMOVAL
		0x1: INSERTION
4:3	MIC_CLAMP_CTL	0x0: MANUAL_CONTROL_CLAMP_OFF
		0x1: MANUAL_CONTROL_CLAMP_ON
		0x2: AUTOMATIC_CONTROL_CLAMP_MIC
2	MBHC_BIAS_EN	0x0: DISABLE
		0x1: ENABLE
1	ZDET_LEGACY_EN	0x0: RAMP
		0x1: LEGACY

#### CDC\_A\_MBHC\_DET\_CTL\_1 (cont.)

Bits	Name	Description
0	ELECT_DETECTION_TYPE	0x0: REMOVAL 0x1: INSERTION

#### 0x0001F150 CDC\_A\_MBHC\_DET\_CTL\_2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: perph rb

#### CDC\_A\_MBHC\_DET\_CTL\_2

Bits	Name	Description
7:6	HS_L_DET_PULL_UP_CTR	0x0: OFF
	L	0x1: I_IP0_UA
		0x2: I_2P0_UA
		0x3: I_3P0_UA
5	HS_L_DET_COMPARATOR	0x0: OFF
	_CTRL	0x1: V_0P9_VDD
4	HPHL_PLUG_TYPE	0x0: NC
	3.09 ming	0x1: NO
3	GND_PLUG_TYPE	0x0: NC
	27.5	0x1: NO
2:1	ELECT_SCHMT_ISRC_CTR	0x0: DISABLE_ALL
	L	0x1: ENABLE_MIC_HPHL_HPHR
		0x2: ENABLE_HPHL_HPHR
		0x3: ENABLE_MIC_HPHL
0	SW_HPH_LP_100K_TO_GN	0x0: DISABLE
	D	0x1: ENABLE

## 0x0001F151 CDC\_A\_MBHC\_FSM\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

#### CDC\_A\_MBHC\_FSM\_CTL

Bits	Name	Description
7	MBHC_FSM_EN	0x0: DISABLE 0x1: ENABLE
6:4	BTN_ISRC_CTRL	0x0: OFF 0x1: I_50_UA 0x2: I_75_UA 0x3: I_100_UA 0x4: I_125_UA 0x5: I_150_UA 0x6: I_175_UA 0x7: I_200_UA
3	ZDET_L_MEAS_EN	0x0: DISABLE 0x1: ENABLE
2	ZDET_R_MEAS_EN	0x0: DISABLE 0x1: ENABLE
1	ZDET_CHG	0x0: DISCHG 0x1: CHG
0	ZDET_DISCHG_CAP_CTL	0x0: DISABLE 0x1: ENABLE

## 0x0001F152 CDC\_A\_MBHC\_DBNC\_TIMER

**Type:** RW

Clock: PBUS\_WRCLK
Reset State: 0x98

## CDC\_A\_MBHC\_DBNC\_TIMER

Bits	Name	Description
7:4	INSREM_DBNC	0x0: T_0_MS 0x1: T_8_MS 0x2: T_16_MS 0x3: T_32_MS 0x4: T_48_MS 0x5: T_64_MS 0x6: T_96_MS 0x7: T_128_MS 0x8: T_192_MS 0x9: T_256_MS 0xA: T_384_MS 0xB: T_512_MS 0xC: T_768_MS 0xD: T_1024_MS 0xE: T_1536_MS 0xF: T_2048_MS
3:2	BTN_DBNC	0x0:T_0_MS 0x1:T_8_MS 0x2:T_16_MS 0x3:T_32_MS
1	ZDET_DISCHG_FAST_RAM P_CTL	0x0: FAST_RAMP 0x1: NOM_RAMP
0	RESERVED	

## 0x0001F153 CDC\_A\_MBHC\_BTN\_ZDET\_CTL\_0

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

## CDC\_A\_MBHC\_BTN\_ZDET\_CTL\_0

Bits	Name	Description
7:5	BTN0_VREF_COARSE	0x0: V_0_MV 0x1: V_100_MV 0x2: V_200_MV 0x3: V_300_MV 0x4: V_400_MV 0x5: V_500_MV 0x6: V_600_MV 0x7: V_700_MV

#### CDC\_A\_MBHC\_BTN\_ZDET\_CTL\_0 (cont.)

Bits	Name	Description
4:2	BTN0_VREF_FINE	0x0: V_0P0_MV
		0x1: V_12P5_MV
		0x2: V_25P0_MV
		0x3: V_37P5_MV
		0x4: V_50P0_MV
		0x5: V_62P5_MV
		0x6: V_75P0_MV
		0x7: V_87P5_MV
1	ZDET_CONN_RAMP_L	0x0: DISCONNECT
		0x1: CONNECT
0	ZDET_CONN_RAMP_R	0x0: DISCONNECT
		0x1: CONNECT

## 0x0001F154 CDC\_A\_MBHC\_BTN\_ZDET\_CTL\_1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x20

Reset Name: perph\_rb

#### CDC\_A\_MBHC\_BTN\_ZDET\_CTL\_1

Bits	Name	Description
7:5	BTN1_VREF_COARSE	0x0: V_0_MV
		0x1: V_100_MV
		0x2: V_200_MV
		0x3: V_300_MV
		0x4: V_400_MV
		0x5: V_500_MV
		0x6: V_600_MV
		0x7: V_700_MV
4:2	BTN1_VREF_FINE	0x0: V_0P0_MV
		0x1: V_12P5_MV
		0x2: V_25P0_MV
		0x3: V_37P5_MV
		0x4: V_50P0_MV
		0x5: V_62P5_MV
		0x6: V_75P0_MV
		0x7: V_87P5_MV
1	ZDET_CONN_FIXED_L	0x0: DISCONNECT
		0x1: CONNECT
0	ZDET_CONN_FIXED_R	0x0: DISCONNECT
		0x1: CONNECT

## 0x0001F155 CDC\_A\_MBHC\_BTN\_ZDET\_CTL\_2

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x40

Reset Name: perph\_rb

#### CDC\_A\_MBHC\_BTN\_ZDET\_CTL\_2

Bits	Name	Description
7:5	BTN2_VREF_COARSE	0x0: V_0_MV
		0x1: V_100_MV
		0x2: V_200_MV
		0x3: V_300_MV
		0x4: V_400_MV
		0x5: V_500_MV
		0x6: V_600_MV
	. (	0x7: V_700_MV
4:2	BTN2_VREF_FINE	0x0: V_0P0_MV
		0x1: V_12P5_MV
	. ( )	0x2: V_25P0_MV
		0x3: V_37P5_MV
		0x4: V_50P0_MV
	27	0x5: V_62P5_MV
	0 0 die	0x6: V_75P0_MV
	S. Owills	0x7: V_87P5_MV
1	ZDET_RAMP_CAP_CTL	0x0: AUTO_SWITCH_CAP
	1	0x1: MANUAL_SWITCH_CAP
0	ZDET_RAMP_RATE_CTL	0x0: R_1P0X_RAMP_RATE
		0x1: R_1P2X_RAMP_RATE

#### 0x0001F156 CDC\_A\_MBHC\_BTN3\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x61

#### CDC\_A\_MBHC\_BTN3\_CTL

Bits	Name	Description
7:5	BTN3_VREF_COARSE	0x0: V_0_MV 0x1: V_100_MV 0x2: V_200_MV 0x3: V_300_MV 0x4: V_400_MV 0x5: V_500_MV 0x6: V_600_MV 0x7: V_700_MV
4:2	BTN3_VREF_FINE	0x0: V_0P0_MV 0x1: V_12P5_MV 0x2: V_25P0_MV 0x3: V_37P5_MV 0x4: V_50P0_MV 0x5: V_62P5_MV 0x6: V_75P0_MV 0x7: V_87P5_MV
1:0	HS_VREF	0x0: V_1P4_V 0x1: V_1P5_V 0x2: V_1P6_V 0x3: V_1P7_V

## 0x0001F157 CDC\_A\_MBHC\_BTN4\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x80

Reset Name: perph\_rb

#### CDC\_A\_MBHC\_BTN4\_CTL

Bits	Name	Description
7:5	BTN4_VREF_COARSE	0x0: V_0_MV 0x1: V_100_MV 0x2: V_200_MV 0x3: V_300_MV 0x4: V_400_MV 0x5: V_500_MV 0x6: V_600_MV 0x7: V_700_MV

#### CDC\_A\_MBHC\_BTN4\_CTL (cont.)

Bits	Name	Description
4:2	BTN4_VREF_FINE	0x0: V_0P0_MV
		0x1: V_12P5_MV
		0x2: V_25P0_MV
		0x3: V_37P5_MV
		0x4: V_50P0_MV
		0x5: V_62P5_MV
		0x6: V_75P0_MV
		0x7: V_87P5_MV
1:0	RESERVED	

## 0x0001F158 CDC\_A\_MBHC\_RESULT\_1

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### CDC\_A\_MBHC\_RESULT\_1

Bits	Name	Description
5	ZDETB5_RESULT	0x0: COMP_LOW
	18. Onill	0x1: COMP_HIGH
4	BTN4_ZDETB4_RESULT	0x0: COMP_LOW
	1	0x1: COMP_HIGH
3	BTN3_ZDETB3_RESULT	0x0: COMP_LOW
		0x1: COMP_HIGH
2	BTN2_ZDETB2_RESULT	0x0: COMP_LOW
		0x1: COMP_HIGH
1	BTN1_ZDETB1_RESULT	0x0: COMP_LOW
		0x1: COMP_HIGH
0	BTN0_ZDETB0_RESULT	0x0: COMP_LOW
		0x1: COMP_HIGH

## 0x0001F159 CDC\_A\_MBHC\_RESULT\_2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

#### CDC\_A\_MBHC\_RESULT\_2

Bits	Name	Description
7:5	RESERVED	
4	AUTO_CLAMP_CTL	0x0: AUTO_CLAMP_CTL_OFF 0x1: AUTO_CLAMP_CTL_ON
3	HPHL_SCHMT_RESULT	0x0: REMOVED 0x1: INSERTED
2	HPHR_SCHMT_RESULT	0x0: REMOVED 0x1: INSERTED
1	MIC_SCHMT_RESULT	0x0: REMOVED 0x1: INSERTED
0	HS_COMP_RESULT	0x0: COMP_LOW 0x1: COMP_HIGH

## 0x0001F160 CDC\_A\_TX\_1\_EN

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x03

Reset Name: perph\_rb

## CDC\_A\_TX\_1\_EN

Bits	Name	Description
7	CH1_EN	0x0: DISABLE
		0x1: ENABLE
6:3	CH1_GAIN	0x0: G_0_DB
		0x2: G_6_DB
		0x4: G_12_DB
		0x6: G_18_DB
		0x7: G_21_DB
		0x8: G_24_DB
2:0	TXFE1_AAF2_CURR_CTL	0x0: I_1_NA
		0x1: I_6_NA
		0x2: I_11_NA
		0x3: I_16_NA
		0x4: I_21_NA
		0x5: I_26_NA
		0x6: I_31_NA
		0x7: I_36_NA

## 0x0001F161 CDC\_A\_TX\_2\_EN

**Type:** RW

Clock: PBUS\_WRCLK
Reset State: 0x03

Reset Name: perph rb

#### CDC\_A\_TX\_2\_EN

Bits	Name	Description
7	CH2_EN	0x0: DISABLE
		0x1: ENABLE
6:3	CH2_GAIN	0x0: G_0_DB
		0x2: G_6_DB
		0x4: G_12_DB
		0x6: G_18_DB
		0x7: G_21_DB
		0x8: G_24_DB
2:0	TXFE2_AAF2_CURR_CTL	0x0: I_1_NA
		0x1: I_6_NA
		0x2: I_11_NA
		0x3: I_16_NA
	, 0,	0x4: I_21_NA
	2,0	0x5: I_26_NA
	10m 60	0x6: I_31_NA
	J.B. W. Chill	0x7: I_36_NA

## 0x0001F165 CDC\_A\_TX\_1\_2\_OPAMP\_BIAS

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x4B

Reset Name: perph\_rb

## CDC\_A\_TX\_1\_2\_OPAMP\_BIAS

Bits	Name	Description
7:5	ADC_INT1_OPAMP_BIAS	0x0: I_2_UA 0x1: I_3_UA 0x2: I_4_UA 0x3: I_5_UA 0x4: I_6_UA
		0x5: I_7_UA 0x6: I_8_UA 0x7: I_9_UA

#### CDC\_A\_TX\_1\_2\_OPAMP\_BIAS (cont.)

Bits	Name	Description
4:3	ADC_INT2_OPAMP_BIAS	0x0: I_0P5_UA
		0x1: I_1_UA
		0x2: I_1P5_UA
		0x3: I_2_UA
2:0	ADC_REF_BIAS	0x0: I_1_UA
		0x1: I_1P5_UA
		0x2: I_2_UA
		0x3: I_2P5_UA
		0x4: I_3_UA
		0x5: I_3P5_UA
		0x6: I_4_UA
		0x7: I_4P5_UA

## 0x0001F166 CDC\_A\_TX\_1\_2\_TXFE\_CLKDIV

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x51

Reset Name: perph\_rb

#### CDC\_A\_TX\_1\_2\_TXFE\_CLKDIV

Bits	Name	Description
7:5	TXFE_1_2_CLK_DIV_RATIO	0x0: DIV_BY_1
	_A1	0x1: DIV_BY_2
		0x2: DIV_BY_4
		0x3: DIV_BY_8
		0x4: DIV_BY_16
		0x5: DIV_BY_32
		0x6: DIV_BY_64
		0x7: DIV_BY_128
4	TXFE_1_2_CLK_DIV_RATIO	0x0: DIV_BY_1
	_A2	0x1: DIV_BY_25
3:1	TXFE_1_2_CLK_DIV_RATIO	0x0: DIV_BY_1
	_B1	0x1: DIV_BY_2
		0x2: DIV_BY_4
		0x3: DIV_BY_8
		0x4: DIV_BY_16
		0x5: DIV_BY_32
		0x6: DIV_BY_64
		0x7: DIV_BY_128
0	TXFE_1_2_CLK_DIV_RATIO	0x0: DIV_BY_1
	_B2	0x1: DIV_BY_25

## 0x0001F167 CDC\_A\_TX\_3\_EN

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: perph rb

#### CDC\_A\_TX\_3\_EN

Bits	Name	Description
7	CH3_EN	0x0: DISABLE
		0x1: ENABLE
6:3	CH3_GAIN	0x0: G_0_DB
		0x2: G_6_DB
		0x4: G_12_DB
		0x6: G_18_DB
		0x7: G_21_DB
	\((	0x8: G_24_DB
2:0	TXFE_1_2_OPAMP_CURR_	0x0: I_1P5_UA
	CTL	0x1: I_2P0_UA
		0x2: I_2P5_UA
		0x3: I_3P0_UA
	, 0,	0x4: I_3P5_UA
	2,8	0x5: I_4P0_UA
	10 09 indi	0x6: I_4P5_UA
	018, 46 M	0x7: I_5P0_UA

#### 0x0001F180 CDC\_A\_NCP\_EN

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x26

Reset Name: perph\_rb

#### CDC\_A\_NCP\_EN

Bits	Name	Description
5	NCP_CLIM_EN	0x0: DISABLE
		0x1: ENABLE
4	NCP_BYPASS	0x1: BYPASS_NCP_GND
		0x0: NO_BYPASS_NCP
3	FB_BYPASS	0x0: ENABLE_FB_LOOP
		0x1: BYPASS_FB_LOOP
2	CURR_STARVE_EN	0x0: DISABLE
		0x1: ENABLE

#### CDC\_A\_NCP\_EN (cont.)

Bits	Name	Description
1	GLITCH_SUP_EN	0x0: DISABLE
		0x1: ENABLE
0	NCP_EN	0x0: DISABLE
		0x1: ENABLE

#### 0x0001F181 CDC\_A\_NCP\_CLK

#### CDC\_A\_NCP\_CLK

CDC_	A_NCP_CLK	
Reset S Reset N	RW PBUS_WRCLK State: 0x23 Name: perph_rb	
Bits	Name	Description
5	CLK_SEL	0x1: CODEC_MCLK 0x0: RESERVED
4	CLK_INV	0x0: NON_INV_CLK 0x1: INVERTED_CLK
3:0	CLK_DIV	0x0: DIV_BY_2 0x1: DIV_BY_4 0x2: DIV_BY_6 0x3: DIV_BY_8 0x4: DIV_BY_10 0x5: DIV_BY_12 0x6: DIV_BY_14 0x7: DIV_BY_14 0x7: DIV_BY_16 0x8: DIV_BY_18 0x9: DIV_BY_20 0xA: DIV_BY_22 0xB: DIV_BY_24 0xC: DIV_BY_24 0xC: DIV_BY_28 0xE: DIV_BY_30 0xF: DIV_BY_32

## 0x0001F182 CDC\_A\_NCP\_DEGLITCH

Type: RW

Clock: PBUS WRCLK **Reset State:** 0x5B

## CDC\_A\_NCP\_DEGLITCH

Bits	Name	Description
7:6	IB_DG_CTRL	0x0: I_1_UA 0x1: I_2_UA 0x2: I_3_UA 0x3: I_4_UA
5:3	NON_TOVP_OUT	0x0: NON_OVP_TIME_7_NS 0x1: NON_OVP_TIME_12_NS 0x2: NON_OVP_TIME_17P5_NS 0x3: NON_OVP_TIME_22P8_NS 0x4: NON_OVP_TIME_28P9_NS 0x5: NON_OVP_TIME_34P6_NS 0x6: NON_OVP_TIME_40P8_NS 0x7: NON_OVP_TIME_46P8_NS
2:0	NON_TOVP_IN	0x0: NON_OVP_TIME_7_NS 0x1: NON_OVP_TIME_12_NS 0x2: NON_OVP_TIME_17P5_NS 0x3: NON_OVP_TIME_22P8_NS 0x4: NON_OVP_TIME_28P9_NS 0x5: NON_OVP_TIME_34P6_NS 0x6: NON_OVP_TIME_40P8_NS 0x7: NON_OVP_TIME_46P8_NS

## 0x0001F183 CDC\_A\_NCP\_FBCTRL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0xA8

Reset Name: perph\_rb

## CDC\_A\_NCP\_FBCTRL

Bits	Name	Description
7	FB_LIMIT_EN	0x0: DISABLE
		0x1: ENABLE
6	FB_EN_SWCLK	0x0: CONTROLS_SWTICHING_CLK
		0x1: NOT_CONTROL_SWITCHING_CLK
5	FB_CLK_INV	0x0: NON_INVERTED_CLK
		0x1: INVERTED_CLK
4	SAMPLE_BYP	0x0: SAMPLE_WITH_CLK
		0x1: WITHOUT_SAMPLER
3	SAMPLE_SWCLK_BYP	0x0: CLOCK_DIVIDER_OR_MCLK
		0x1: SWITCHING_CLOCK

#### CDC\_A\_NCP\_FBCTRL (cont.)

Bits	Name	Description
2	SAMPLE_MCLK_BYP	0x0: CLOCK_DIVIDER 0x1: MCLK
1:0	SAMPLE_FREQ_DIV	0x0: DIV_FREQ_0P5 0x1: DIV_FREQ_2 0x2: DIV_FREQ_4 0x3: DIV_FREQ_8

## 0x0001F184 CDC\_A\_NCP\_BIAS

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x29

Reset Name: perph\_rb

#### CDC\_A\_NCP\_BIAS

Bits	Name	Description
7:5	IB_LDO_1UA	0x0: I_0P5_UA
	0)	0x1: I_1_UA
	2,5	0x2: I_1P5_UA
	10 m	0x3: I_2_UA
	S. Owill	0x4: I_2P5_UA
	2018-09-21 tyle	0x5: I_3_UA
	7	0x6: I_3P5_UA
	· V	0x7: I_4_UA
4:3	IB_DG_CTRL2	0x0: I_5_UA
		0x1: I_10_UA
		0x2: I_15_UA
		0x3: I_20_UA
2:0	IB_COMP1_5UA	0x0: I_2P5_UA
		0x1: I_5_UA
		0x2: I_7P5_UA
		0x3: I_10_UA
		0x4: I_12P5_UA
		0x5: I_15_UA
		0x6: I_17P5_UA
		0x7: I_20_UA

#### 0x0001F185 CDC\_A\_NCP\_VCTRL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0xA4

Reset Name: perph\_rb

#### CDC\_A\_NCP\_VCTRL

Bits	Name	Description
7:6	SEL_FB_FLIM	0x0: SW_CLK_DIV_8 0x1: SW_CLK_DIV_16 0x2: SW_CLK_DIV_32 0x3: SW_CLK_DIV_64
5:3	LDO_VCTRLB	0x0: VDR_2P2V 0x1: VDR_2P4V 0x2: VDR_2P6V 0x3: VDR_2P8V 0x4: VDR_3V 0x5: VDR_3P2V 0x6: VDR_3P4V 0x7: VDR_3P6V
2:0	VNEG_OUT	0x0: VNEG_1P1V 0x1: VNEG_1P2V 0x2: VNEG_1P3V 0x3: VNEG_1P4V 0x4: VNEG_1P5V 0x5: VNEG_1P6V 0x6: VNEG_1P7V 0x7: VNEG_1P8V

#### 0x0001F187 CDC\_A\_NCP\_CLIM

Type: RW

Clock: PBUS\_WRCLK Reset State: 0xD5

Reset Name: perph\_rb

#### CDC\_A\_NCP\_CLIM

Bits	Name	Description
7:5	IN_SW_2_DELAY	0x0: SW_2_DELAY_CLK_DIV_2
		0x1: SW_2_DELAY_CLK_DIV_4
		0x2: SW_2_DELAY_CLK_DIV_8
		0x3: SW_2_DELAY_CLK_DIV_16
		0x4: SW_2_DELAY_CLK_DIV_32
		0x5: SW_2_DELAY_CLK_DIV_64
		0x6: SW_2_DELAY_CLK_DIV_128
		0x7: SW_2_DELAY_CLK_DIV_256
4:3	IN_SW_1_DELAY	0x0: SW_1_DELAY_CLK_DIV_32
		0x1: SW_1_DELAY_CLK_DIV_64
		0x2: SW_1_DELAY_CLK_DIV_128
		0x3: SW_1_DELAY_CLK_DIV_256
2:0	IN_SW_0_DELAY	0x0: SW_0_DELAY_CLK_DIV_2
		0x1: SW_0_DELAY_CLK_DIV_4
		0x2: SW_0_DELAY_CLK_DIV_8
		0x3: SW_0_DELAY_CLK_DIV_16
	. ( )	0x4: SW_0_DELAY_CLK_DIV_32
		0x5: SW_0_DELAY_CLK_DIV_64
	03	0x6: SW_0_DELAY_CLK_DIV_128
	27	0x7: SW_0_DELAY_CLK_DIV_256

#### 0x0001F190 CDC\_A\_RX\_CLOCK\_DIVIDER

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0xE8

Reset Name: perph\_rb

#### CDC\_A\_RX\_CLOCK\_DIVIDER

Bits	Name	Description
7:1	RX_CLK_DIVIDER	0x0: DIV_4 0x32: DIV_72 0x74: DIV_96 0x7F: DIV_512
0	DTEST_EN	0x0: DISABLE 0x1: ENABLE

#### 0x0001F191 CDC\_A\_RX\_COM\_OCP\_CTL

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0xCF

Reset Name: perph rb

#### CDC\_A\_RX\_COM\_OCP\_CTL

Bits	Name	Description
7:5	OCP_CURR_LIMIT	0x0: I_280MA
		0x2: I_370MA
		0x3: I_440MA
		0x4: I_140MA
		0x6: I_185MA
		0x7: I_220MA
4	OCP_FSM_EN	0x0: DISABLE
	\((	0x1: ENABLE
3:0	N_CONN_ATTEMPTS	0x0: N_0
		0x1: N_1
		0xF: N_15

#### 0x0001F192 CDC\_A\_RX\_COM\_OCP\_COUNT

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x6E

Reset Name: perph rb

#### CDC\_A\_RX\_COM\_OCP\_COUNT

Bits	Name	Description
7:5	RUN_N_CYCLES	0x0: N_511
		0x3: N_2047
		0x7: N_4095
4:2	WAIT_N_CYCLES	0x0: N_511
		0x3: N_2047
		0x7: N_4095
1	FSM_LOCK_EN	0x0: DISABLE
		0x1: ENABLE

#### 0x0001F193 CDC\_A\_RX\_COM\_BIAS\_DAC

**Type:** RW

Clock: PBUS\_WRCLK
Reset State: 0x10

Reset Name: perph rb

#### CDC\_A\_RX\_COM\_BIAS\_DAC

Bits	Name	Description
7	RX_BIAS_EN	0x0: DISABLE 0x1: ENABLE
6:5	TEST_BIAS_CURR	0x0: I_0UA 0x1: I_1UA 0x2: I_2UA 0x3: I_3UA
4	DAC_CLK_SEL	0x0: ANALOG 0x1: DIGITAL
3:2	DAC_GAIN	0x0: G_0DB 0x1: G_0P27DB 0x2: G_0P54DB
0	DAC_REF_EN	0x0: DISABLE 0x1: ENABLE

#### 0x0001F194 CDC\_A\_RX\_HPH\_BIAS\_PA

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x5A

Reset Name: perph rb

#### CDC\_A\_RX\_HPH\_BIAS\_PA

Bits	Name	Description
7:4	DAC_BIAS_CURR	0x0: I_0P0UA
		0x1: I_0P5UA
		0x5: I_2P5UA
		0xA: I_5P0UA
		0xF: I_7P5UA
3:0	PA_BIAS_CURR	0x0: I_0P0UA
		0x1: I_0P5UA
		0x5: I_2P5UA
		0xA: I_5P0UA
		0xF: I_7P5UA

#### 0x0001F195 CDC\_A\_RX\_HPH\_BIAS\_LDO\_OCP

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x69

Reset Name: perph rb

#### CDC\_A\_RX\_HPH\_BIAS\_LDO\_OCP

Bits	Name	Description
7:6	LDO_OTA_BIAS_CURR	0x0: I_1P5UA 0x1: I_2P0UA 0x2: I_2P5UA 0x3: I_3P0UA
5:4	LDO_OUT_BIAS_CURR	0x0: I_3P0UA 0x1: I_3P5UA 0x2: I_4P0UA 0x3: I_4P5UA
3:2	OCP_REF_CURR	0x0: I_4P0UA 0x1: I_4P5UA 0x2: I_5P0UA 0x3: I_5P5UA
1:0	SPK_DAC_BIAS_CURR	0x0: I_2P0UA 0x1: I_2P5UA 0x2: I_3P0UA 0x3: I_3P5UA

#### 0x0001F196 CDC\_A\_RX\_HPH\_BIAS\_CNP

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x29

Reset Name: perph rb

#### CDC\_A\_RX\_HPH\_BIAS\_CNP

Bits	Name	Description
7:4	WG_CURR	0x0: I_0P0UA 0x1: I_0P5UA 0x5: I_2P5UA 0xA: I_5P0UA 0xF: I_7P5UA
3:2	OTA_BIAS_CURR	0x0: I_3P0UA 0x1: I_3P5UA 0x2: I_4P0UA 0x3: I_4P5UA

#### CDC\_A\_RX\_HPH\_BIAS\_CNP (cont.)

Bits	Name	Description
1:0	VBAT_LDO_CURR	0x0: I_0P5UA
		0x1: I_1P0UA
		0x2: I_1P5UA
		0x3: I_2P0UA

#### 0x0001F197 CDC\_A\_RX\_HPH\_CNP\_EN

#### CDC\_A\_RX\_HPH\_CNP\_EN

CDC_A_RX_HPH_CNP_EN		
Type: RW Clock: PBUS_WRCLK Reset State: 0x80  Reset Name: perph_rb  CDC_A_RX_HPH_CNP_EN		
Bits	Name	Description
7	FSM_CLK_EN	0x0: DISABLE 0x1: ENABLE
6	FSM_RESET	0x0: NORMAL_OP 0x1: RESET
5:4	HPH_PA_EN	0x0: NONE 0x1: HPHR 0x2: HPHL 0x3: HPHR_HPHL
3	FSM_OVERRIDE_EN	0x0: DISABLE 0x1: ENABLE
2	RESERVED	
1	RESERVED	
0	RESERVED	

#### 0x0001F198 CDC\_A\_RX\_HPH\_CNP\_WG\_CTL

Type: RW

Clock: PBUS WRCLK Reset State: 0xDA

Reset Name: perph\_rb

#### CDC\_A\_RX\_HPH\_CNP\_WG\_CTL

Bits	Name	Description
7	GM3_BOOST_EN	0x0: DISABLE
		0x1: ENABLE

#### CDC\_A\_RX\_HPH\_CNP\_WG\_CTL (cont.)

Bits	Name	Description
6	PWR_DN_SEQ_EN	0x0: DISABLE
		0x1: ENABLE
5:3	VREF_TIMER	0x0: T_0US
		0x1: T_1X0P72US
		0x3: T_3X0P72US
		0x7: T_7X0P72US
2:0	CURR_LDIV_CTL	0x0: DIV_250
		0x1: DIV_333
		0x2: DIV_500
		0x3: DIV_1000
		0x7: DIV_2000

#### 0x0001F199 CDC\_A\_RX\_HPH\_CNP\_WG\_TIME

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x16

Reset Name: perph\_rb

#### CDC\_A\_RX\_HPH\_CNP\_WG\_TIME

Bits	Name	Description
7:2	WG_FINE_TIMER	0x0: T_0MS 0x1: T_1MS 0x5: T_5MS 0x3F: T_60MS
1:0	VBAT_LDO_OUT	0x0: V_1P9V 0x1: V_2P8V 0x2: V_3P0V 0x3: V_3P2V

#### 0x0001F19B CDC\_A\_RX\_HPH\_L\_PA\_DAC\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x20

Reset Name: perph rb

#### CDC\_A\_RX\_HPH\_L\_PA\_DAC\_CTL

Bits	Name	Description
7:4	GM3_IBIAS_CTL	0x1: GM_400_PCT
		0x2: GM_200_PCT
		0x4: GM_100_PCT
		0x8: GM_50_PCT
		0xC: GM_33_PCT
3	DAC_DATA_EN	0x0: DISABLE
		0x1: ENABLE
2	DAC_SAMPLE_EDGE_SEL	0x0: FALLING
		0x1: RISING
1	DATA_RESET	0x0: NORMAL_OP
		0x1: RESET
0	INV_DATA	0x0: DISABLE
		0x1: ENABLE

#### 0x0001F19D CDC\_A\_RX\_HPH\_R\_PA\_DAC\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x20

Reset Name: perph\_rb

#### CDC\_A\_RX\_HPH\_R\_PA\_DAC\_CTL

Bits	Name	Description
7:4	GM3_IBIAS_CTL	0x1: GM_400_PCT
		0x2: GM_200_PCT
		0x4: GM_100_PCT
		0x8: GM_50_PCT
		0xC: GM_33_PCT
3	DAC_DATA_EN	0x0: DISABLE
		0x1: ENABLE
2	DAC_SAMPLE_EDGE_SEL	0x0: FALLING
		0x1: RISING
1	DATA_RESET	0x0: NORMAL_OP
		0x1: RESET
0	INV_DATA	0x0: DISABLE
		0x1: ENABLE

#### 0x0001F19E CDC\_A\_RX\_EAR\_EN

**Type:** RW

Clock: PBUS\_WRCLK Reset State: 0x12

Reset Name: perph\_rb

#### CDC\_A\_RX\_EAR\_EN

Bits	Name	Description
7	PA_SEL	0x0: HPH 0x1: EAR
6	EAR_PA_EN	0x0: DISABLE 0x1: ENABLE
5	GAIN	For EAR:  0x0: POS_1P5_DB  0x1: POS_6_DB  For HPH:  0x0: POS_M4P5_DB  0x1: POS_0_DB
4:3	EAR_CM_SEL	0x0: VCM_1P5V 0x1: VCM_1P56V 0x2: VCM_1P6V 0x3: VCM_1P65V
2:1	EAR_CMBUF_BIAS_CURR	0x0: I_1P5UA 0x1: I_2P0UA 0x2: I_2P5UA 0x3: I_3P0UA
0	SPK_VBAT_LDO_EN	0x0: DISABLE 0x1: ENABLE

#### 0x0001F1A0 CDC\_A\_RX\_HPH\_STATUS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x0C

Reset Name: perph rb

#### CDC\_A\_RX\_HPH\_STATUS

Bits	Name	Description
7:0	STATUS	

#### 0x0001F1A1 CDC\_A\_RX\_EAR\_STATUS

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x10

Reset Name: perph rb

#### CDC\_A\_RX\_EAR\_STATUS

Bits	Name	Description
7:5	EAR_STATUS	
4	FRZ_B_STATUS	0: FREEZE_ASSERT 1: FREEZE_DEASSERT

#### 0x0001F1B0 CDC\_A\_SPKR\_DAC\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x83

Reset Name: perph\_rb

#### CDC\_A\_SPKR\_DAC\_CTL

Bits	Name	Description
7	REF_EN	0x0: DISABLE
	20,5%	0x1: ENABLE
6:5	DAC_GAIN	0x0: POS_0P00_DB
		0x1: POS_0P27_DB
		0x2: POS_0P54_DB
4	DAC_RESET	0x0: NORMAL
		0x1: RESET
3	CLK_POLARITY	0x0: FALLING
		0x1: RISING
2	MCLK_SEL	0x0: MCLK
		0x1: NCPCLK
1	CAL_BYPASS	0x1: NORMAL
		0x0: BYPASS
0	CLK_4X_B	0x0: NORMAL_4XCLK
		0x1: NORMAL_CLK

#### 0x0001F1B1 CDC\_A\_SPKR\_DRV\_CLIP\_DET

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x91

Reset Name: perph rb

#### CDC\_A\_SPKR\_DRV\_CLIP\_DET

Bits	Name	Description
7:5	CLIP_LIMIT	0x0: N_0 0x1: N_1 0x2: N_2 0x3: N_3 0x4: N_4 0x5: N_5 0x6: N_6 0x7: N_7
4:2	FIFO_LEN	0x0: N_1 0x1: N_2 0x2: N_3 0x3: N_4 0x4: N_5 0x5: N_6 0x6: N_7 0x7: N_8
1:0	CLIP_MODE	0x0: DISABLE 0x1: ENABLE_CLIP_DET 0x2: CNP_TEST_START_UP 0x3: CNP_TEST_SHUT_DOWN

#### 0x0001F1B2 CDC\_A\_SPKR\_DRV\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x69

Reset Name: perph\_rb

#### CDC\_A\_SPKR\_DRV\_CTL

Bits	Name	Description
7	CLASSD_PA_EN	0x0: DISABLE
		0x1: ENABLE
6	CAL_EN	0x0: DISABLE
		0x1: ENABLE

#### CDC\_A\_SPKR\_DRV\_CTL (cont.)

Bits	Name	Description
5	SETTLE_EN	0x0: DISABLE
		0x1: ENABLE
4	PWM_STATES	0x1: PWM_2STATE
		0x0: PWM_3STATE
3	FW_EN	0x0: DISABLE
		0x1: ENABLE
2	BOOST_SET	0x0: DISABLE
		0x1: ENABLE
1	CMFB_SET	0x0: I_200UA
		0x1: I_300UA
0	GAIN_SET	0x1: G12DB
		0x0: Reserved

#### 0x0001F1B3 CDC\_A\_SPKR\_ANA\_BIAS\_SET

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x41

Reset Name: perph\_rb

#### CDC\_A\_SPKR\_ANA\_BIAS\_SET

Bits	Name	Description
7:5	INT1_CMFB_CURR	0x0: I_9P00UA
		0x1: I_9P50UA
		0x2: I_10P00UA
		0x3: I_10P50UA
		0x4: I_11P00UA
		0x5: I_11P50UA
		0x6: I_12P00UA
		0x7: I_12UA50
4:2	SAR_DAC_CURR	0x0: I_2P5UA
		0x1: I_4P5UA
		0x2: I_6P5UA
		0x3: I_8P5UA
		0x4: I_10P5UA
		0x5: I_12P5UA
		0x6: I_14P5UA
		0x7: I_16P5UA

#### CDC\_A\_SPKR\_ANA\_BIAS\_SET (cont.)

Bits	Name	Description
1:0	INT2_OPAMP_CURR	0x0: I_7P00UA
		0x1: I_7P50UA
		0x2: I_8P00UA
		0x3: I_8P50UA

#### 0x0001F1B4 CDC\_A\_SPKR\_OCP\_CTL

#### CDC\_A\_SPKR\_OCP\_CTL

CDC_A_SPKR_OCP_CTL			
Clock: Reset S Reset M	Type: RW Clock: PBUS_WRCLK Reset State: 0xE1 Reset Name: perph_rb CDC_A_SPKR_OCP_CTL		
Bits	Name	Description	
7	OCP_EN	0x0: DIABLE 0x1: ENABLE	
6	OCP_HOLD	0x0: DIABLE 0x1: ENABLE	
5:4	OCP_CURR_LIMIT	0x0: ZEROP5A 0x1: TWOP5A 0x2: THREEP0A 0x3: FOURP0A	
3:2	GLITCH_FILTER	0x0: T160NS 0x1: T120NS 0x2: T80NS 0x3: T40NS	
1:0	INT2_SF_CURR	0x0: I_10P00UA 0x1: I_15P00UA 0x2: I_20P00UA 0x3: I_25P00UA	

#### 0x0001F1B5 CDC\_A\_SPKR\_PWRSTG\_CTL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x1E

Reset Name: perph\_rb

#### CDC\_A\_SPKR\_PWRSTG\_CTL

Name	Description
BBM_EN	0x0: DIABLE
	0x1: ENABLE
HBRDGE_EN	0x0: DIABLE
	0x1: ENABLE
CLAMP_EN	0x0: DIABLE
	0x1: ENABLE
DEADTIME	0x0: T20NS
	0x1: T15NS
	0x2: T10NS
	0x3: T05NS
SLEW	0x0: T20NS
	0x1: T15NS
\ (	0x2: T10NS
	0x3: T05NS
DAC_EN	0x0: DIABLE
	0x1: ENABLE
	BBM_EN  HBRDGE_EN  CLAMP_EN  DEADTIME  SLEW

# 0x0001F1B6 CDC\_A\_SPKR\_DRV\_MISC

Clock: PBUS\_WRCLK **Reset State:** 0xCB

Reset Name: perph rb

#### CDC\_A\_SPKR\_DRV\_MISC

Bits	Name	Description
7:5	CMP_CURR	0x0: I_2P25UA
		0x1: I_3P00UA
		0x2: I_3P50UA
		0x3: I_4P00UA
		0x4: I_4P50UA
		0x5: I_5P00UA
		0x6: I_5P50UA
		0x7: I_6P00UA
4:3	INT1_OTA1_CURR	0x0: I_14UA
		0x1: I_15UA
		0x2: I_16UA
		0x3: I_17UA

#### CDC\_A\_SPKR\_DRV\_MISC (cont.)

Bits	Name	Description
2:1	INT2_OTA2_CURR	0x0: I_14UA 0x1: I_15UA 0x2: I_16UA 0x3: I_17UA
0	PWM_CLK_SEL	0x0: CLK_600KHZ 0x1: CLK_300KHZ

#### 0x0001F1C0 CDC\_A\_BOOST\_CURRENT\_LIMIT

Type: RW

Clock: PBUS\_WRCLK Reset State: 0xE2

Reset Name: perph rb

#### CDC\_A\_BOOST\_CURRENT\_LIMIT

Bits	Name	Description
7	MAX_CURR_LIM_ENABLE	0: DISABLE 1: ENABLE
6	ENABLE_OCPON_PS	0: FOLLOW_PS 1: ALWAYS_ON_WITH_PS_MODE
5	ENABLE_SOFTSTART	0: DISABLE 1: ENABLE
4	SOFTSTART_DELAY	0: DEL_240US 1: DEL_400US
2:0	SET_CURRENT_MAX	0x0: I_0P5A 0x1: I_1P0A 0x2: I_1P5A 0x3: I_2P0A 0x4: I_2P5A 0x5: I_3P0A 0x6: I_3P5A 0x7: I_4P0A

#### 0x0001F1C1 CDC\_A\_BOOST\_OUTPUT\_VOLTAGE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x14

Reset Name: perph rb

#### CDC\_A\_BOOST\_OUTPUT\_VOLTAGE

Bits	Name	Description
4:0	SET_OUTPUT_VOLTAGE	0x0: VOUT_4P000V
		0x1: VOUT_4P050V
		0x2: VOUT_4P100V
		0x3: VOUT_4P150V
		0x4: VOUT_4P200V
		0x5: VOUT_4P250V
		0x6: VOUT_4P300V
		0x7: VOUT_4P350V
		0x8: VOUT_4P400V
		0x9: VOUT_4P450V
		0xA: VOUT_4P500V
		0xB: VOUT_4P550V
		0xC: VOUT_4P600V
		0xD: VOUT_4P650V
	\ (	0xE: VOUT_4P700V
		0xF: VOUT_4P750V
		0x10: VOUT_4P800V
		0x11: VOUT_4P850V
		0x12: VOUT_4P900V
	0	0x13: VOUT_4P950V
	27.0	0x14: VOUT_5P000V
	9 19	0x15: VOUT_5P050V
	2018:54 CWINTER	0x16: VOUT_5P100V
	20) EM	0x17: VOUT_5P150V
		0x18: VOUT_5P200V
		0x19: VOUT_5P250V
		0x1A: VOUT_5P300V
		0x1B: VOUT_5P350V
		0x1C: VOUT_5P400V
		0x1D: VOUT_5P450V
		0x1E: VOUT_5P500V
		0x1F: VOUT_5P550V

#### 0x0001F1C2 CDC\_A\_BOOST\_BYPASS\_MODE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x18

Reset Name: perph\_rb

#### CDC\_A\_BOOST\_BYPASS\_MODE

Bits	Name	Description
7	EN_PFET_BYPASS	0: DISABLE_BYPASS 0: BYPASS_PFET
6	PFET_FORCE	0: FORCE_PFET_OFF 1: FORCE_PFET_ON
5	BYPASS_MODE_EN	0: DISABLE_BYPASS_MODE 1: ENABLE_BYPASS_MODE
4	EN_MONITOR	0: DISABLE_MONITOR 1: ENABLE_MONITOR
3	EN_VCOMPARE	0: DISABLE_VCOMPARE 1: ENABLE_VCOMPARE
2	OUTPUT_PULLDOWN_EN	0: DISABLE_PULLDOWN 1: ENABLE_PULLDOWN
1	EN_NFET_BYPASS	0: PWM_CTL_NFET 1: EXTERNAL_CTL_NFET
0	NFET_FORCE	0: FORCE_NFET_OFF 1: FORCE_NFET_ON

#### 0x0001F1C3 CDC\_A\_BOOST\_EN\_CTI

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x5F

Reset Name: perph\_rb

#### CDC\_A\_BOOST\_EN\_CTL

Bits	Name	Description
7	BOOST_ENABLE	0x0: MODULE_DISABLE
		0x1: MODULE_ENABLE
6	PULSE_SKIP_MODE	0x0: DISABLE
		0x1: ENABLE
5:4	PULSE_SKIP_THRES	0x0: PULSESKIP_THRES_50MA
		0x1: PULSESKIP_THRES_100MA
		0x2: PULSESKIP_THRES_150MA
		0x3: PULSESKIP_THRES_200MA
3:2	LOOP_COMP_CAP	0x0: C_40PF
		0x1: C_60PF
		0x2: C_80PF
		0x3: C_100PF

#### CDC\_A\_BOOST\_EN\_CTL (cont.)

Bits	Name	Description
1:0	LOOP_COMP_RES	0x0: R_100K 0x1: R_200K 0x2: R_500K 0x3: R_600K

#### 0x0001F1C5 CDC\_A\_RDSON\_MAX\_DUTY\_CYCLE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0xC0

Reset Name: perph rb

#### CDC\_A\_RDSON\_MAX\_DUTY\_CYCLE

Bits	Name	Description
7	NFET_SW_SIZE	0x0: TWOBY3_FULL_SIZE
		0x1: FULL_SIZE
6	EN_MAX_DUTY_CYCLE	0x0: DISABLE
	277	0x1: ENABLE

#### 0x0001F1C8 CDC\_A\_SPKR\_SAR\_STATUS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph rb

#### CDC\_A\_SPKR\_SAR\_STATUS

Bits	Name	Description
6:0	SAR_ADC	Default is x00 only if SPKR PA is enabled (xB2 bit 7 is 1).

#### 0x0001F1C9 CDC\_A\_SPKR\_DRV\_STATUS

Type: R

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

#### CDC\_A\_SPKR\_DRV\_STATUS

Bits	Name	Description
7	CAL_STOP	
6	POS_PMOS_OCP_1	
5	POS_NMOS_OCP_2	
4	NEG_PMOS_OCP_1	
3	NEG_NMOS_OCP_2	
1	CLIP_DET_P	
0	CLIP_DET_N	<i>N</i>

#### 0x0001F1CE CDC\_A\_PBUS\_ADD\_CSR

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: perph\_rb

SW write to this pointer register before read from analog register to avoid read back timing

#### CDC\_A\_PBUS\_ADD\_CSR

Bits	Name	Description
7:0	REG	

#### 0x0001F1CF CDC\_A\_PBUS\_ADD\_SEL

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: perph\_rb

This register is used to select PBUS address or PBUS\_ADD\_CSR

#### CDC\_A\_PBUS\_ADD\_SEL

Bits	Name	Description
0	REG	

## 83 Codec BOOST\_FREQ\_BCLK\_gen\_clk Registers

#### 0x0001F200 CDC\_BOOST\_FREQ\_REVISION1

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

#### CDC\_BOOST\_FREQ\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

#### 0x0001F201 CDC\_BOOST\_FREQ\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: N/A

HW Version Register [15:8]

#### CDC\_BOOST\_FREQ\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x0001F204 CDC\_BOOST\_FREQ\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x1D

Reset Name: N/A

Peripheral Type

#### CDC\_BOOST\_FREQ\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	BCLK GEN

#### 0x0001F205 CDC\_BOOST\_FREQ\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x19 Reset Name: N/A

Peripheral SubType

#### CDC\_BOOST\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	BCLK GEN CLK

#### 0x0001F246 CDC\_BOOST\_FREQ\_CLK\_ENABLE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

#### CDC\_BOOST\_FREQ\_CLK\_ENABLE

Bits	Name	Description
7	EN_CLK_INT	0 = do not force the clock on
		1 = enable the clock
		0x0: FORCE_EN_DISABLED
		0x1: FORCE_EN_ENABLED

#### CDC\_BOOST\_FREQ\_CLK\_ENABLE (cont.)

Bits	Name	Description
0	FOLLOW_CLK_SX_REQ	0 = ignore smps_clk_req <x></x>
		1 = clock is enabled when the clocks request is high smps_clk_req <x>='1'</x>
		0x0: FALLOW_CLK_REQ_DISABLED
		0x1: FALLOW_CLK_REQ_ENABLED

#### 0x0001F250 CDC\_BOOST\_FREQ\_CLK\_DIV

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x05

Reset Name: PERPH\_RB

PMIC LOCKED=SEC ACCESS, PMIC GANGED

#### CDC BOOST FREQ CLK DIV

Bits	Name	Description
3:0	CLK_DIV	clock_ frequency = 19.2MHz / (CLK_DIV + 1)
		FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz
	0,1 1,5	HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz
	.O. ville	CLK_DIV = 0 is not supported, it will generate 9.6 MHz
	2018. 24 Chillip	0x0: FREQ_9M6HZ_0
	2.5	0x1: FREQ_9M6HZ
	1	0x2: FREQ_6M4HZ
		0x3: FREQ_4M8HZ
		0x4: FREQ_3M8HZ
		0x5: FREQ_3M2HZ
		0x6: FREQ_2M7HZ
		0x7: FREQ_2M4HZ
		0x8: FREQ_2M1HZ
		0x9: FREQ_1M9HZ
		0xA: FREQ_1M7HZ
		0xB: FREQ_1M6HZ
		0xC: FREQ_1M5HZ
		0xD: FREQ_1M4HZ
		0xE: FREQ_1M3HZ
		0xF: FREQ_1M2HZ

#### 0x0001F251 CDC\_BOOST\_FREQ\_CLK\_PHASE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x08

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### CDC\_BOOST\_FREQ\_CLK\_PHASE

Bits	Name	Description
3:0	CLK_PHASE	Distributed clock phase select:
		clock phase delay = clock period * (CLK_PHASE / 16)

#### 0x0001F2C0 CDC\_BOOST\_FREQ\_GANG\_CTL1

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### CDC\_BOOST\_FREQ\_GANG\_CTL1

Bits	Name	Description
7:0	GANG_LEADER_PID	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

#### 0x0001F2C1 CDC\_BOOST\_FREQ\_GANG\_CTL2

Type: RW

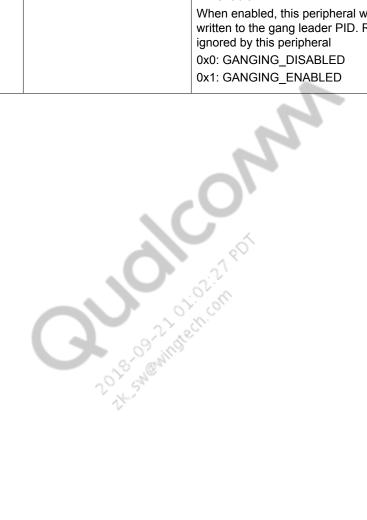
Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### CDC\_BOOST\_FREQ\_GANG\_CTL2

Bits	Name	Description
7	GANG_EN	0 = disable
		1 = enable
		When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral
		0x0: GANGING_DISABLED
		0x1: GANGING_ENABLED



### 84 Codec NCP\_FREQ\_BCLK\_gen\_clk Registers

#### 0x0001F300 CDC\_NCP\_FREQ\_REVISION1

**Type:** R

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: N/A

HW Version Register [7:0]

#### CDC\_NCP\_FREQ\_REVISION1

Bits	Name	Description
7:0	DIG_MINOR	This number is incremented for digital change that is not intended to affect software or any change that adds a new feature but is backwards compatible with old software. Minor resets to zero when Major increments

#### 0x0001F301 CDC\_NCP\_FREQ\_REVISION2

Type: R

Clock: PBUS\_WRCLK Reset State: 0x02

Reset Name: N/A

HW Version Register [15:8]

#### CDC\_NCP\_FREQ\_REVISION2

Bits	Name	Description
7:0	DIG_MAJOR	This number is incremented when changes are made to the digital HW that are not backwards compatible with existing software.

#### 0x0001F304 CDC\_NCP\_FREQ\_PERPH\_TYPE

Type: R

Clock: PBUS\_WRCLK Reset State: 0x1D

Reset Name: N/A

Peripheral Type

#### CDC\_NCP\_FREQ\_PERPH\_TYPE

Bits	Name	Description
7:0	TYPE	BCLK GEN

#### 0x0001F305 CDC\_NCP\_FREQ\_PERPH\_SUBTYPE

Type: R

Clock: PBUS\_WRCLK
Reset State: 0x19

Reset Name: N/A

Peripheral SubType

#### CDC\_NCP\_FREQ\_PERPH\_SUBTYPE

Bits	Name	Description
7:0	SUBTYPE	BCLK GEN CLK

#### 0x0001F346 CDC\_NCP\_FREQ\_CLK\_ENABLE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x01

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

#### CDC\_NCP\_FREQ\_CLK\_ENABLE

Bits	Name	Description
7	EN_CLK_INT	0 = do not force the clock on
		1 = enable the clock
		0x0: FORCE_EN_DISABLED
		0x1: FORCE_EN_ENABLED

#### CDC\_NCP\_FREQ\_CLK\_ENABLE (cont.)

Bits	Name	Description
0	FOLLOW_CLK_SX_REQ	0 = ignore smps_clk_req <x></x>
		1 = clock is enabled when the clocks request is high smps_clk_req <x>='1'</x>
		0x0: FALLOW_CLK_REQ_DISABLED
		0x1: FALLOW_CLK_REQ_ENABLED

#### 0x0001F350 CDC\_NCP\_FREQ\_CLK\_DIV

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x01

Reset Name: PERPH\_RB

PMIC\_LOCKED=SEC\_ACCESS, PMIC\_GANGED

#### CDC\_NCP\_FREQ\_CLK\_DIV

Bits	Name	Description
3:0	CLK_DIV	clock_ frequency = 19.2MHz / (CLK_DIV + 1)
		FTS2 Buck supports 3.2, 4.8, 6.4 and 9.6 MHz
	0,1 1,5	HF2 Buck supports 1.6, 2.4, 2.74, 3.2, 3.8, 4.8, and 6.4 MHz
	.O. ville	CLK_DIV = 0 is not supported, it will generate 9.6 MHz
	2018. 24 Chillip	0x0: FREQ_9M6HZ_0
	2.5	0x1: FREQ_9M6HZ
	1	0x2: FREQ_6M4HZ
		0x3: FREQ_4M8HZ
		0x4: FREQ_3M8HZ
		0x5: FREQ_3M2HZ
		0x6: FREQ_2M7HZ
		0x7: FREQ_2M4HZ
		0x8: FREQ_2M1HZ
		0x9: FREQ_1M9HZ
		0xA: FREQ_1M7HZ
		0xB: FREQ_1M6HZ
		0xC: FREQ_1M5HZ
		0xD: FREQ_1M4HZ
		0xE: FREQ_1M3HZ
		0xF: FREQ_1M2HZ

#### 0x0001F351 CDC\_NCP\_FREQ\_CLK\_PHASE

Type: RW

Clock: PBUS\_WRCLK Reset State: 0x0F

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### CDC\_NCP\_FREQ\_CLK\_PHASE

Bits	Name	Description
3:0	CLK_PHASE	Distributed clock phase select:
		clock phase delay = clock period * (CLK_PHASE / 16)

#### 0x0001F3C0 CDC\_NCP\_FREQ\_GANG\_CTL1

Type: RW

Clock: PBUS\_WRCLK
Reset State: 0x00

Reset Name: PERPH RB

PMIC LOCKED=SEC ACCESS

#### CDC\_NCP\_FREQ\_GANG\_CTL1

Bits	Name	Description
7:0	GANG_LEADER_PID	When GANG_EN (GANG_CTL2[7]) is set, this peripheral will write the same data that is written to the gang leader Peripheral ID. Reads to the gang leader Peripheral ID are ignored by this peripheral. Ganged peripherals must reside within the same Slave ID

#### 0x0001F3C1 CDC\_NCP\_FREQ\_GANG\_CTL2

Type: RW

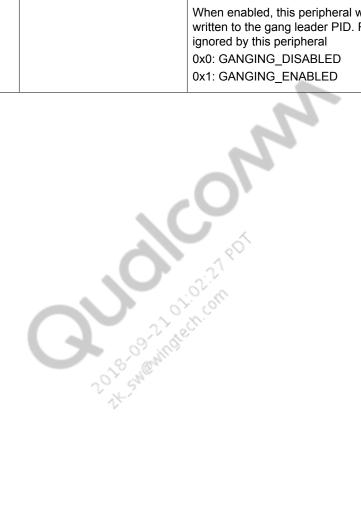
Clock: PBUS\_WRCLK Reset State: 0x00

Reset Name: PERPH RB

PMIC\_LOCKED=SEC\_ACCESS

#### CDC\_NCP\_FREQ\_GANG\_CTL2

Bits	Name	Description
7	GANG_EN	0 = disable
		1 = enable
		When enabled, this peripheral will write the same data that is written to the gang leader PID. Reads to the gang leader PID are ignored by this peripheral
		0x0: GANGING_DISABLED
		0x1: GANGING_ENABLED



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