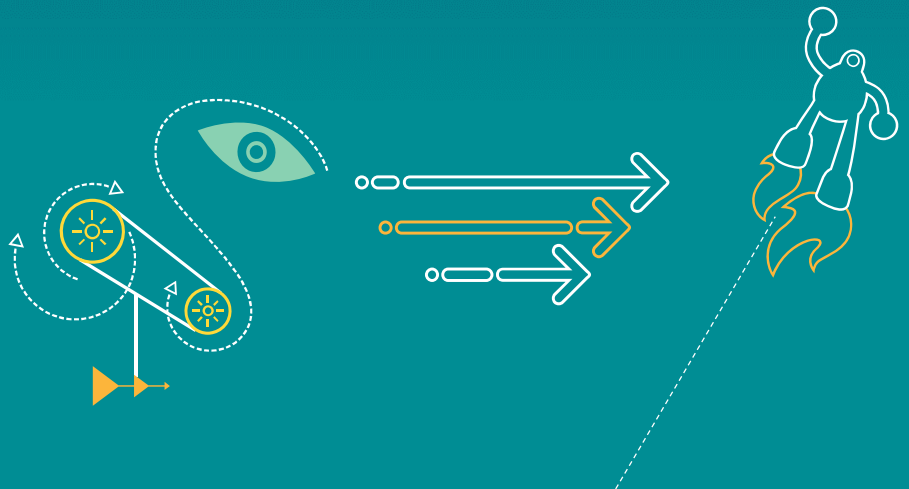
Limits Management Hardware (LMh) Overview

Qualcomm Technologies, Inc.



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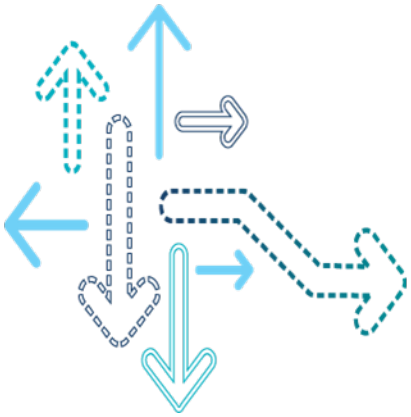
Revision History

Revision	Date	Description
A	October 2014	Initial release
B	March 2015	Added information regarding LMh support in MSM8992
C	September 2015	Expanded common coverage of all relevant chipsets
D	August 2016	Updated slides 6-12 and 19 to include MSM8998 details

Contents

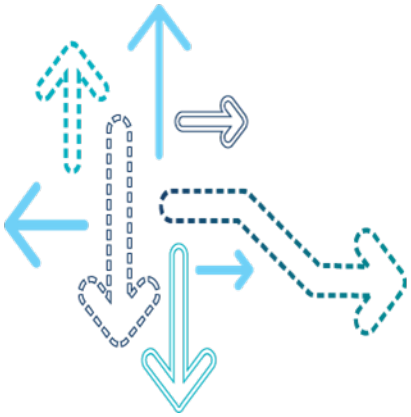
Introduction



Introduction

- On a high-performance device with an advanced CPU subsystem, peak current requirements for the CPU subsystem is large when the device operates at a peak-rated performance and temperature.
- LMh is a hardware-based protection circuit that has two main functions:
  - Manage the peak current consumed by the CPU subsystem within the specified capability of the PMIC supply rail
  - Provide fast thermal management response if CPUs are overheating
- LMh adds to the MSM device's reliability and robustness, by helping to maintain the rail voltage when the current demand exceeds the PMIC's capability.
- LMh hardware reduces the CPU performance when an extreme current or thermal condition is detected. This performance reduction occurs without any other impact to the operation of the software running on the CPU subsystem.

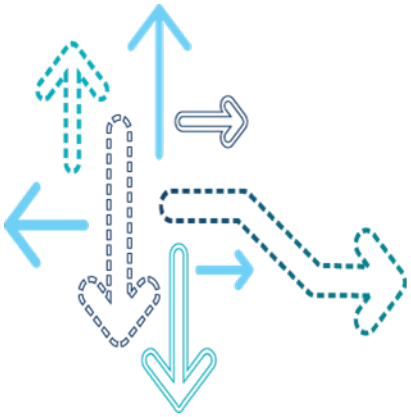
Background Information



How LMh Works

- When an LMh mitigation node detects an extreme current or thermal condition, LMh hardware throttles the CPU performance.
- This performance reduction occurs without any other impact to the operation of the software running on the CPU subsystem.
- LMh is hardware based, which runs concurrently and independently from existing thermal engine. CPU throttling through LMh is only expected to occur when critical temperature level is reached or upon rapid rises in temperature.
- Thermal management for sustained periods is expected to be handled by existing thermal software, i.e. Kernel Thermal Monitor (KTM) and user space Thermal Engine.

LMh Feature Summary



LMh Feature Summary by Chipset

	Peak current management	Thermal management	Battery current limiting (BCL)
MSM8998	3 nodes (CPU cluster 0 and 1, GPU)	3 nodes (CPU cluster 0 and 1, GPU)	1 node (notification from PMIC)
MSM8996	1 node for current on APC rail (supplying both clusters)	7 nodes: • LLM_cp <cluster 0/1><cpu 0/1> – CPU thermal throttling • LLM_l2 <cluster 0/1> – monitoring L2 • LLM_m4m0 – monitoring M4M	Managed by BCL software (not handled by LMh)
MSM8994	1 node for current on APC1 (performance cluster)	8 node (A53 cluster cores 0-3, A57 cluster cores 0-3)	Managed by BCL software (not handled by LMh)
MSM8992	Current management not needed	6 sensors (A53 cluster cores 0- 3, A57 cluster cores 0, 1)	Managed by BCL software (not handled by LMh)
MSM8976	1 node for A72 cluster	11 tsens sensors	Managed by BCL software (not handled by LMh)

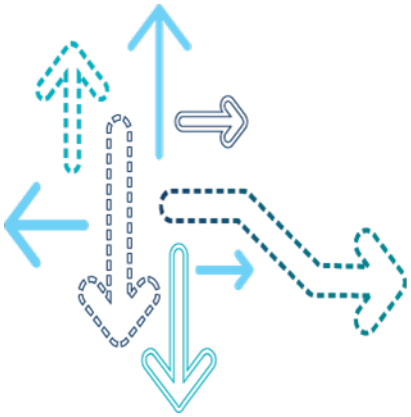
LMH DCVSh Driver (MSM8998)

- On MSM8998, LMh DCVSh (Dynamic Clock and Voltage Scaling) registers two mitigation nodes into the thermal software framework, one per CPU cluster.
  - limits_sensor – 00 for CPU cluster 0
  - limits_sensor – 01 for CPU cluster 1
- HLOS KTM votes for frequency changes by setting thresholds on these nodes
  - Request is made directly to hardware (faster response)
  - KTM aggregates thermal requests in HLOS; thus, there is no change from perspective of thermal engine and clients
- These virtual sensors are set up in HLOS for the purpose of frequency requests, and is not capable of reading out a temperature.

BCL Mitigation by LMh (MSM8998)

- On MSM8998, PMIC hardware monitors BCL voltage and current conditions, and then sends notifications directly to LMh hardware.
  - This notification arrangement is enabled by using “qcom, msm-bcl-lmh” as BCL peripheral in device tree.
- BCL thresholds are still configured by BCL HLOS driver (based on device tree settings). BCL HLOS driver is responsible for listening and reporting vbat_adc and ibat_high interrupts.
- When PMIC notifies LMh of any I_{bat} or V_{bat} violation, LMh request changes on the clock frequency to throttle the CPU’s performance.
- For information on the BCL HLOS driver, refer to *Battery Current Limit (BCL) Overview and Tuning* (80-NM328-709).

LMh Logging and Information



LMh Intensity

- LMh driver reports an intensity value to indicate LMh activity.
- The intensity is expressed as a percentage of time (since the last update) when LMh throttling occurred. It is not the percentage of performance impact.
- The LMh intensity for each sensor is accessible in user space through sysfs interfaces.

  ```
  cat /sys/class/thermal/thermal_zone#/temp
  ```
- When LMh is not throttling, the sysfs interface node has a value 0.

Kernel Logging

- During initial LMh sensor registration, the sensor names are printed.

```
<6>[   10.607871] lmh_lite:lmh_parse_sensor Registering sensor:[LLM_IA57]
<6>[   10.608467] lmh_lite:lmh_parse_sensor Registering sensor:[THRM_57-0]
<6>[   10.608891] lmh_lite:lmh_parse_sensor Registering sensor:[THRM_57-1]
<6>[   10.609277] lmh_lite:lmh_parse_sensor Registering sensor:[THRM_57-2]
<6>[   10.609628] lmh_lite:lmh_parse_sensor Registering sensor:[THRM_57-3]
<6>[   10.610027] lmh_lite:lmh_parse_sensor Registering sensor:[THRM_53-0]
<6>[   10.610400] lmh_lite:lmh_parse_sensor Registering sensor:[THRM_53-1]
<6>[   10.610789] lmh_lite:lmh_parse_sensor Registering sensor:[THRM_53-2]
<6>[   10.611211] lmh_lite:lmh_parse_sensor Registering sensor:[THRM_53-3]
<7>[   10.611649] lmh_lite:lmh_sensor_init LMH Sensor Init complete
```

- When LMh is triggered, messages appear in the kernel log:

```
<7>[   46.984271] lmh_lite:lmh_handle_isr LMH Interrupt triggered
<7>[   46.984296] lmh_lite:lmh_notify Lmh hw interrupt:
<Interrupt_status_reg_value>
<6>[   46.984380] lmh_lite:lmh_read_and_notify Sensor:[LLM_IA57] interrupt
triggered
```

- These kernel messages are printed when the throttling ends:

```
<6>[   47.065564] lmh_lite:lmh_reset Zero throttling. Re-enabling interrupt
<7>[   47.376454] lmh_lite:lmh_notify LMH not throttling. Enabling interrupt
```

Ftrace Logging

- LMh driver outputs trace events to ftrace. It is recommended to use ftrace for collecting continuous data for testing.

  Set thermal trace events as shown below to enable ftrace :

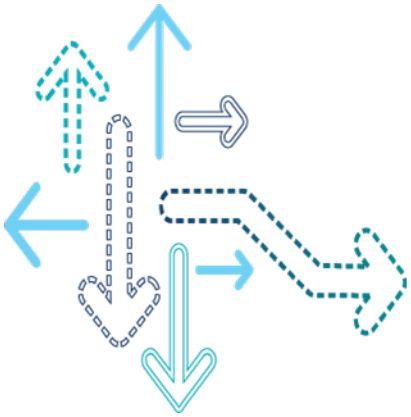
```
echo 150384 > /sys/kernel/debug/tracing/buffer_size_kb
echo "" > /sys/kernel/debug/tracing/set_event
echo "" > /sys/kernel/debug/tracing/trace
echo thermal:* > /sys/kernel/debug/tracing/set_event
<  … run some tests …  >
cat /sys/kernel/debug/tracing/trace > /data/local/trace.txt  // Save ftrace log (may take a few minutes)
```

- After it is enabled, ftrace log shows interrupt received/clear and the LMh intensity with sensor name (refer to chipset summary table).

  ftrace log example:

```
lmh_event_call: Event:[Lmh Interrupt]    //Interrupt indicates LMh triggered
lmh_event_call: Event:[GET_INTENSITY enter] //LMh driver reads LMh intensity
lmh_event_call: Event:[GET_INTENSITY exit]
lmh_sensor_reading: Sensor:[LLM_cp01] throttling intensity:6 //Intensity value for sensor; indicates throttling
lmh_sensor_interrupt: Sensor:[LLM_cp01] throttling intensity:6
lmh_event_call: Event:[GET_INTENSITY enter]
lmh_event_call: Event:[GET_INTENSITY exit]
lmh_sensor_interrupt: Sensor:[LLM_cp01] throttling intensity:0 //Intensity is zero, means throttling is done
lmh_event_call: Event:[Lmh Interrupt Clear]      // Clear LMh interrupt
```

FAQs



FAQs

Q. Is LMh tunable by customers?

A. No, LMh is set to ensure PMIC maximum current limit and CPU maximum temperature limit is not exceeded.

Q. Is LMh a replacement for thermal engine?

A. No, LMh runs concurrently and independently from thermal engine software. CPU throttling through LMh is only expected to occur when critical temperature level is reached or upon rapid rises in the temperature. Thermal management for sustained periods is expected to be handled by existing thermal software, i.e. Kernel Thermal Monitor and user space Thermal Engine.

Q. Does LMh affect existing thermal tuning procedure?

A. No, thermal tuning should be performed using the same methodology as shown in previous chipsets.

Q. Is it possible to identify when LMh has been triggered?

A. Yes, LMh actions are visible through ftrace, kernel log and sysfs nodes. LMh logging details are discussed later in this document.

References

Title	Number
Qualcomm Technologies, Inc.	
Battery Current Limit (BCL) Overview and Tuning	80-NM328-709

Questions?

https://createpoint.qti.qualcomm.com