GC5025 COB

1/5’’5Mega CMOS Image Sensor

DataSheet

Rev.1.1

2017-01-11

Ordering Information

◆ **GC5025W**

(Colored, 150um, back grinding, reconstructed wafer)

GENERATION REVISION HISTORY

REV.	*EFFECTIVE DATE*	*DESCRIPTION OF CHANGES*	*PREPARED BY*
1.0	*2016-7-12*	*Document Release*	*AE Dept.*
1.1	*2017-1-11*	*Update COB package , Pixel array ,Pixel information and DC Characteristics*	*AE Dept*

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Content

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1. Sensor Overview

1.1 General Description

GC5025 is a high quality 5Mega CMOS image sensor, for mobile phone camera applications and digital camera products. GC5025 incorporates a 2608H x 1960Vpixel array, on-chip 10-bit ADC, and image signal processor.

The full scale integration of high-performance and low-power functions makes the GC5025 fit the design, reduce implementation process, and extend the battery life of cell phones, PDAs, and a wide variety of mobile applications.

It provides RAW10 and RAW8 data formats with MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/5 inch
- 1.12μmx1.12μm TSI pixel
- Output formats: Raw Bayer 10bit/8bit
- Power supply requirement: AVDD28: 2.7~3.0V
  DVDD: 1.15~1.25V
  IOVDD: 1.7~1.9V
- PLL support
- Windowing support
- MIPI(2_lane) interface support
- Horizontal/Vertical mirror
- Image processing module
- OTP support(2K Bits)：static DD/module information/WB
- Package: COB/wafer

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1.3 Application

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipments

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/5 inch
Pixel Size	1.12μm x 1.12μm(BSI)
Active pixel array	2592 x 1944
Shutter type	Electronic rolling shutter
ADC resolution	10 bit ADC
Max Frame rate	30fps@full size
Power Supply	AVDD28: 2.7~3.0V DVDD: 1.15~1.25V IOVDD: 1.7~1.9V
Power Consumption	105mW@30fps
SNR	37dB
Dark Current	15e-/s
Sensitivity	2400e-/Lux*s
Dynamic range	63dB
Operating temperature:	-20℃~70℃
Stable Image temperature	0~50℃
Max Optimal lens chief ray angle(CRA)	30.98°(non-linear)
Package type	CSP/COB/wafer

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2. DC Characteristics

2.1 Standby Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	20	50	uA
Digital	I_{DVDD}	—	80	800	uA
I/O	I_{IOVDD}	—	100	200	uA

RST: L, PWND: L
Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.2 Power off Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	0	0	uA
Digital	I_{DVDD}	—	0	0	uA
I/O	I_{IOVDD}	—	0	0	uA

Power off, T_j=25℃

2.3 Operation Current

- **Full size (MIPI 2 lane @864Mbps/Lane)**

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	15	20	mA
Digital	I_{DVDD}	—	50	60	mA
I/O	I_{IOVDD}	—	1	2	mA

INCLK: 24MHz, Frame rate: 30fps , Raw 10

Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.4 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Power supply	V_{AVDD}	2.7	2.8	3.0	V
	V_{DVDD}	1.15	1.2	1.25	V
	V_{IOVDD}	1.7	1.8	1.9	V
Digital Input(Conditions: AVDD = 2.8V, DVDD = 1.2V, IOVDD = 1.8V)					
Input voltage HIGH	V_{IH}	1.4			V
Input voltage LOW	V_{IL}			0.6	V
Digital Output(Conditions: AVDD = 2.8V, IOVDD = 1.8V, standard Loading 25PF)					
Output voltage HIGH	V_{OH}	1.6			V
Output voltage LOW	V_{OL}			0.2	V

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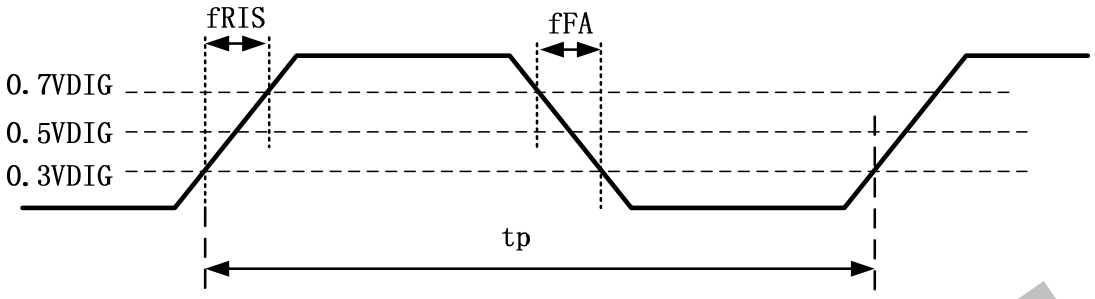
3. AC Characteristics

Master clock wave diagram



Input clock square waveform specifications：

Item	Symbol	Min.	Typ.	max	unit
Frequency	f_{SCK}	6	24	27	MHz
jitter (period, peak-to-peak)	T_{jitter}			600	ps
Rise Time	f_{RISE}	1		15	ns
Fall Time	f_{FALL}	1		15	ns
Duty Cycle	f_{DUTY}	40		60	%
Input Leakage	f_{ILEAK}	-10		10	μA

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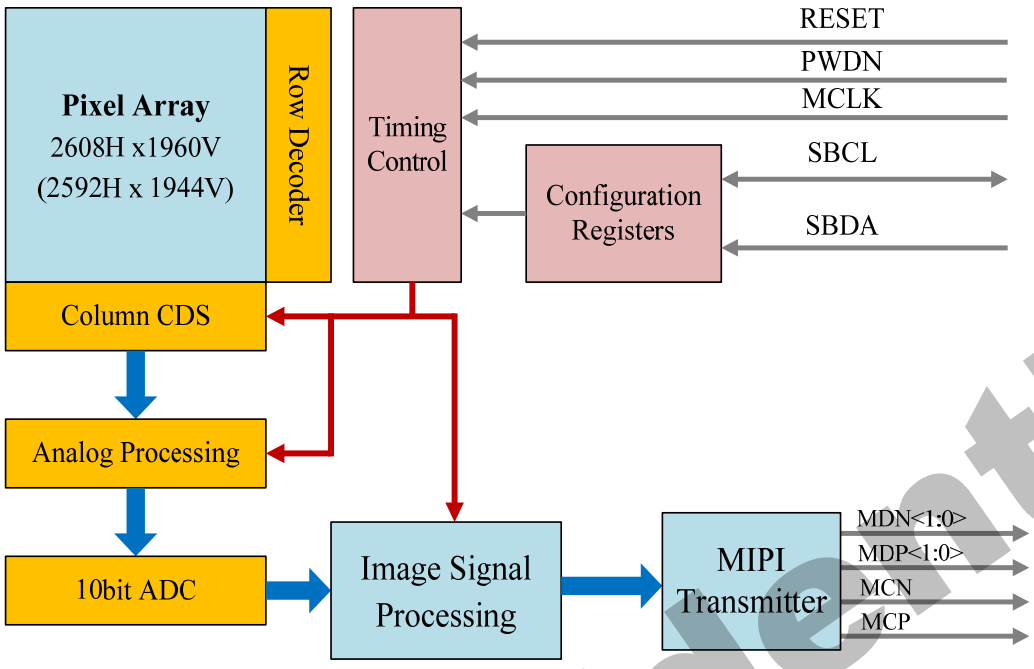
4. Block Diagram



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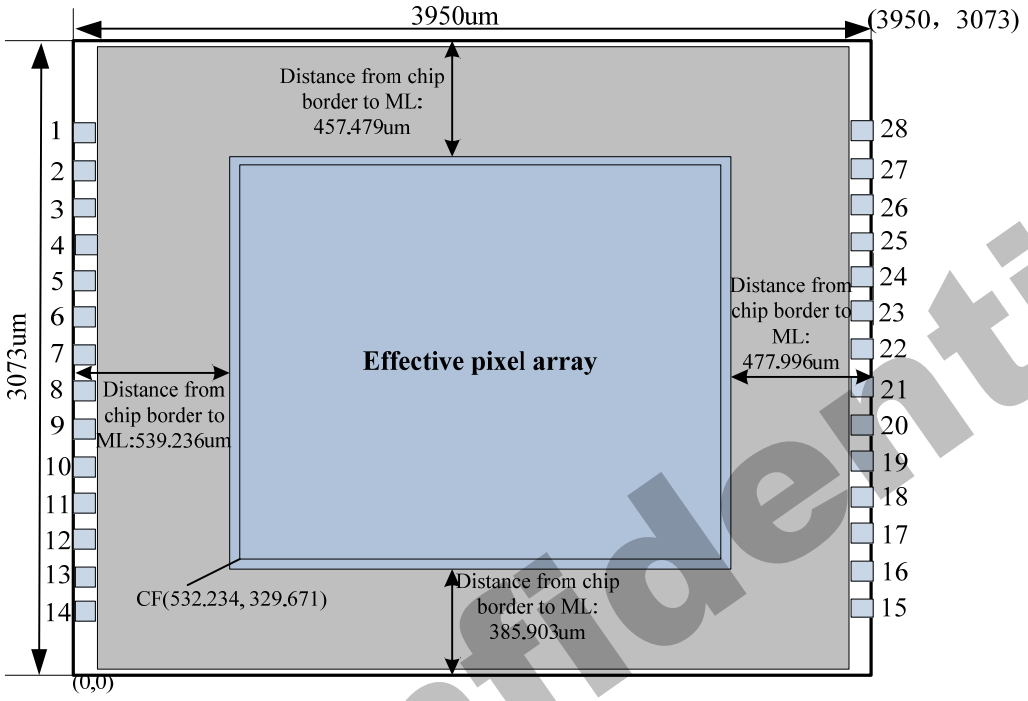
5. COB Package

5.1 Pin Diagram (COB)

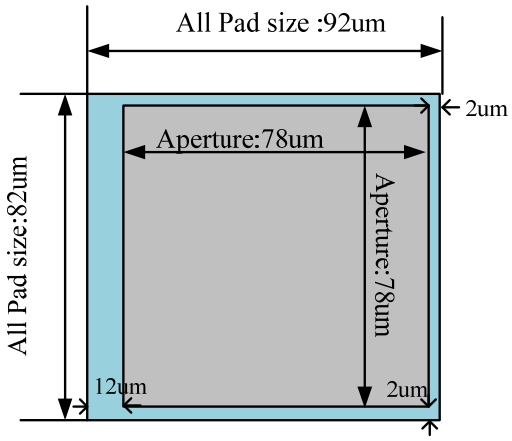


Top View

***Die size: 3950 x 3073μm (without scribe line)**

Scribe line: 80um

***Thickness of die (wafer):150±10μm**



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5.2 Pin Descriptions

Pin	X(Pos)	Y(Pos)	Name	Pin Type	Description
1	54	2901.5	AVDD28	Power	Main power supply pin:2.7~3.0V, Please connect 2.2μF capacitor to analog ground
2	54	2691.5	AGND	Ground	Ground for analog
3	54	2481.5	NC	/	/
4	54	2271.5	NC	/	/
5	54	2061.5	VRSG	Power	Internal power supply, please connect 1μF capacitor to analog ground.
6	54	1851.5	VOTP	Power	For OTP power supply：6.5V
7	54	1641.5	VREF	Power	Internal power supply, please connect 1μF capacitor to analog ground.
8	54	1431.5	VTX	Power	Internal power supply, please connect 1μF capacitor to analog ground.
9	54	1221.5	IOVDD	Power	Power supply for I/O circuits: 1.7~1.9V,Please connect 1μF capacitor to digital ground.
10	54	1011.5	RESETB	I/O	Chip reset control: 0: chip reset 1: normal work
11	54	801.5	PWDN	I/O	Sensor power down control: 1: normal work 0: standby
12	54	591.5	FSYNC	I/O	Frame sync
13	54	381.5	SBDA	Output	Two-wire serial bus, data
14	54	171.5	DGND	Ground	Ground for digital
15	3896	171.5	DVDD12	POWER	Digital power supply pin: 1.15~1.25V, please connect 1μF capacitor to digital ground.
16	3896	381.5	DGND	Ground	Ground for digital
17	3896	591.5	SBCL	Output	Two-wire serial bus, clock
18	3896	801.5	MDN1	Output	MIPI data <1> (-)
19	3896	1011.5	MDP1	Output	MIPI data <1> (+)
20	3896	1221.5	MCN	Output	MIPI clock (-)

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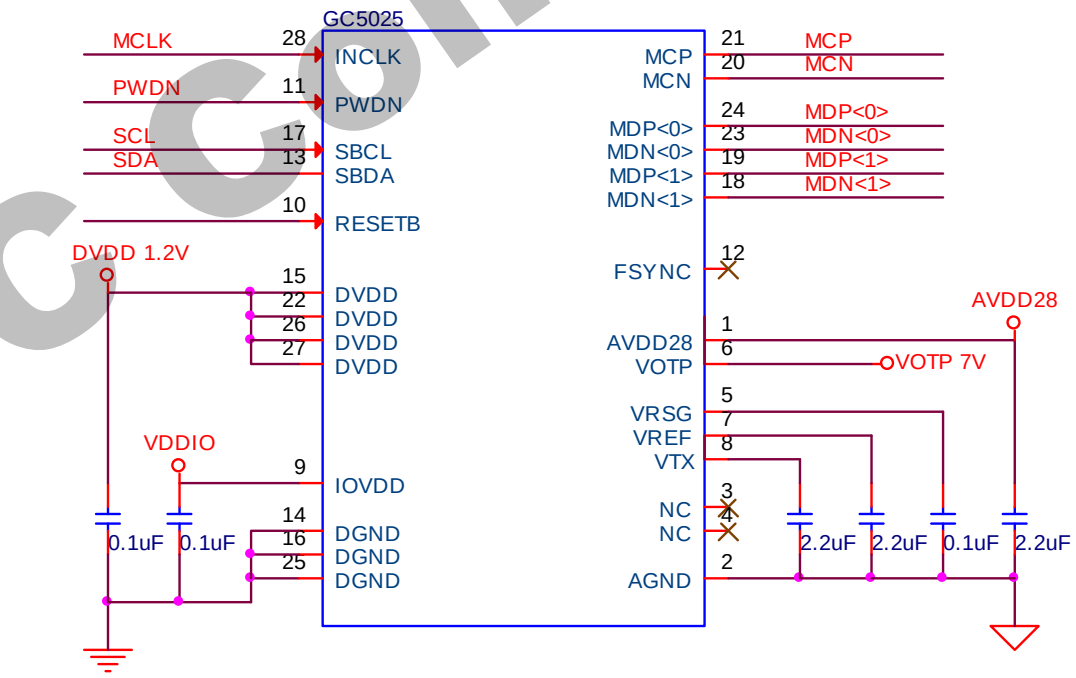
21	3896	1431.5	MCP	Output	MIPI clock (+)
22	3896	1641.5	DVDD12	Power	Digital power supply pin: 1.15~1.25V, please connect 1μF capacitor to digital ground.
23	3896	1851.5	MDN0	Output	MIPI data <0> (-)
24	3896	2061.5	MDP0	Output	MIPI data <0> (+)
25	3896	2271.5	DGND	Ground	Ground for digital
26	3896	2481.5	DVDD12	Power	Digital power supply pin: 1.15~1.25V, please connect 1μF capacitor to digital ground.
27	3896	2691.5	DVDD12	Power	Digital power supply pin: 1.15~1.25V, please connect 1μF capacitor to digital ground.
28	3896	2901.5	INCLK	Input	Sensor input clock

5.3 Reference circuit design

MIPI 2 lane



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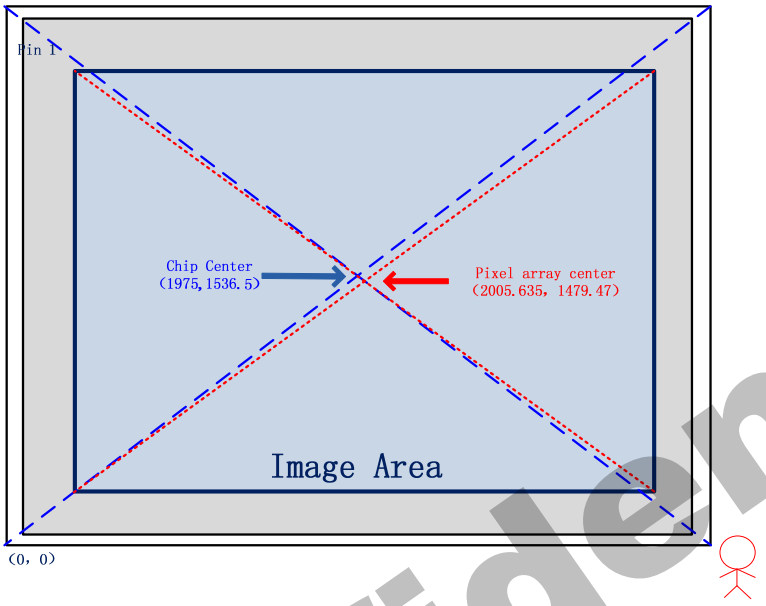
6. Optical Specifications

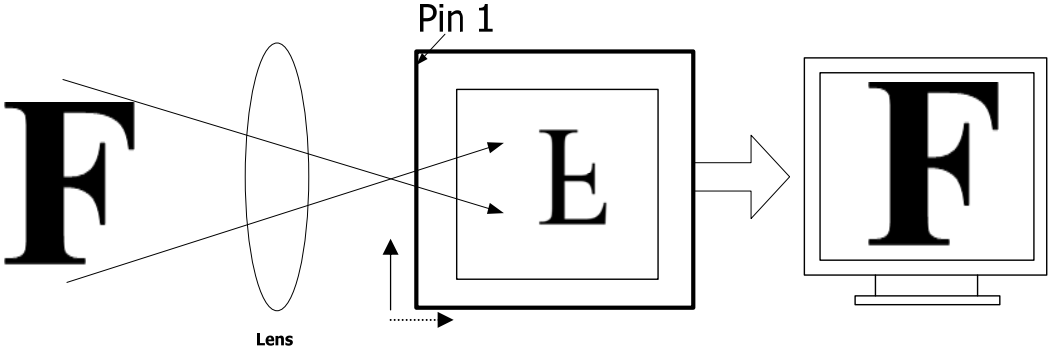
6.1 Optical Center (unit: μm)



Top View

6.2 Readout Position

The GC5025 default status is readout from the lower left corner with pin 1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so mirrored image output results when Pin 1 is located in the upper left corner.



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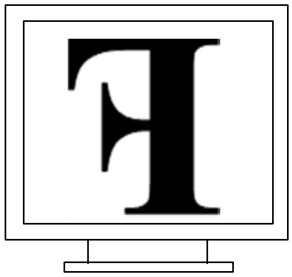
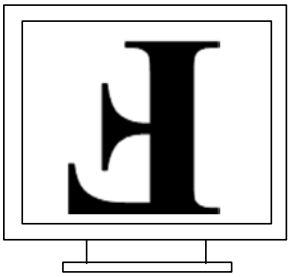
Readout direction can be set by the registers.

Function	Register Address	Register Value	First Pixel
Normal	P0:0x17[1:0]	00	Gr
Horizontal mirror	P0:0x17[1:0]	01	R
Vertical Flip	P0:0x17[1:0]	10	B
Horizontal Mirror and Vertical Flip	P0:0x17[1:0]	11	Gb



Horizontal Mirror



Horizontal Mirror and Vertical Flip

Vertical Flip

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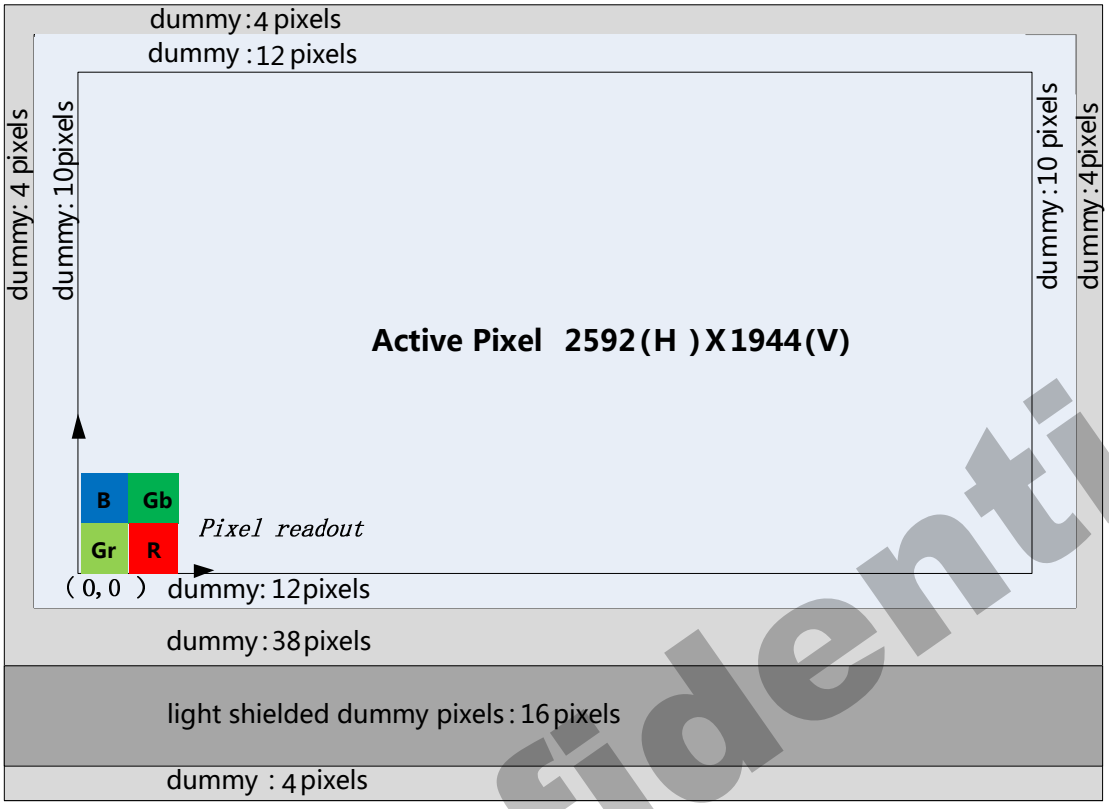
6.3 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 2591. If flip in column, column is read out from 2591 to 0.

If no flip in row, row is read out from 0 to 1943. If flip in row, row is read out from 1943to 0.

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6.4 Lens Chief Ray Angle (CRA)

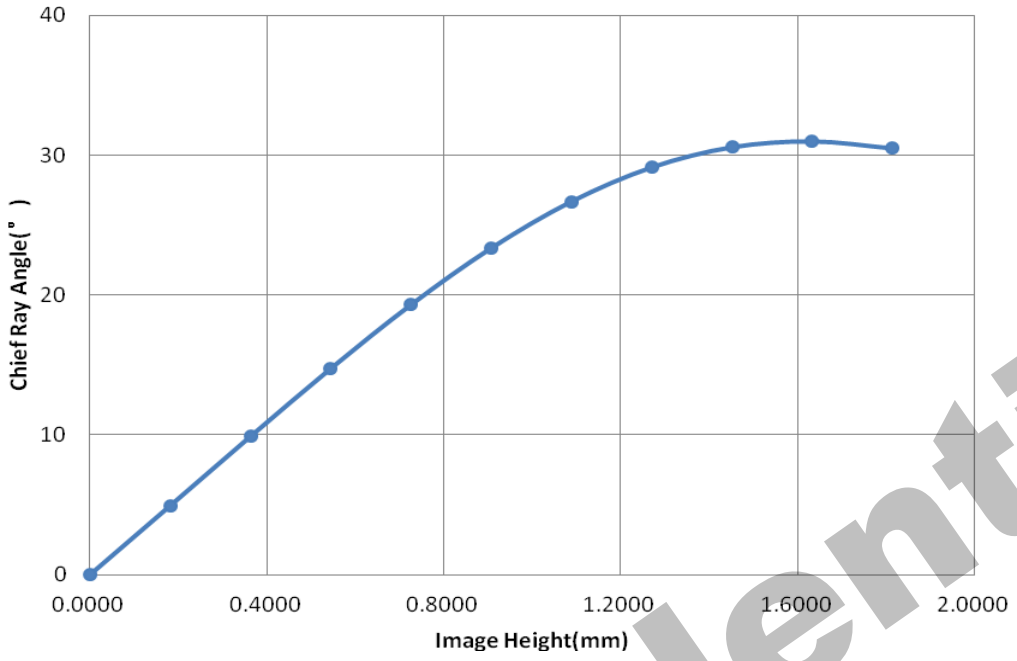

Image Height（%）	Image Height（mm)	CRA (degree)
00	0.0000	0.00
10	0.1814	4.94
20	0.3629	9.89
30	0.5443	14.74
40	0.7258	19.30
50	0.9072	23.35
60	1.0886	26.68
70	1.2701	29.12
80	1.4515	30.56
90	1.6330	30.98
100	1.8144	30.48

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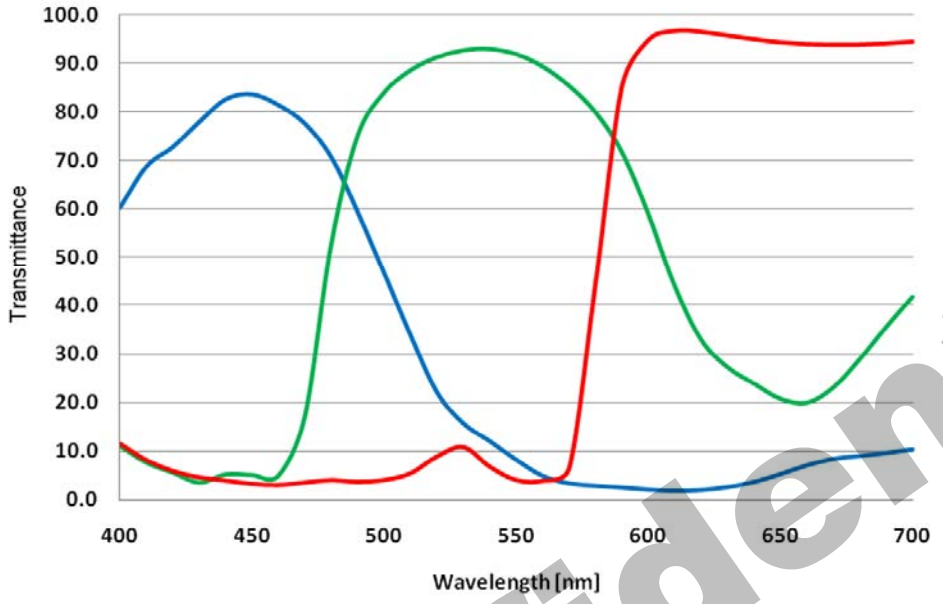
6.5 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below:



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7. Two-wire Serial Bus Communication

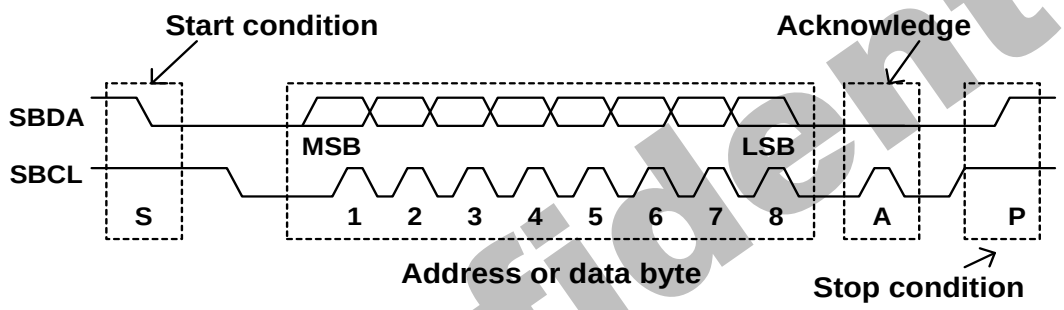
GC5025 Device Address:

Serial bus write address = 0x6e Serial bus read address = 0x6f

7.1 Protocol

The host must perform the role of a communications master and GC5025 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL.**



Single Register Writing:

S	6EH	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	6EH	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	6EH	A	Register Address	A	S	6FH	A	Data	NA	P

Notes:

From master to slave From slave to master

S: Start condition **P:** Stop condition

A: Acknowledge bit **NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value

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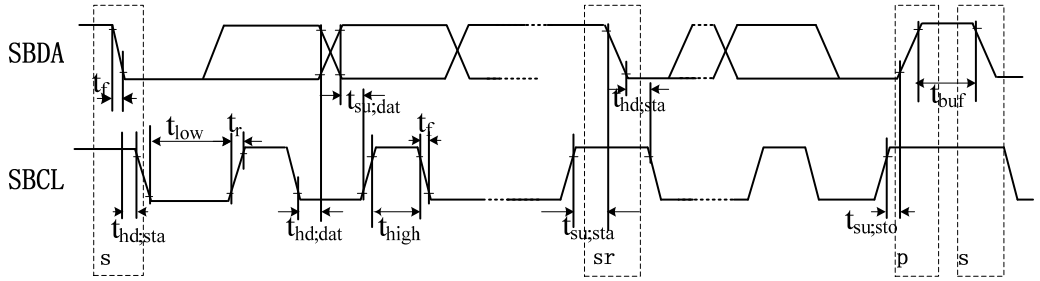
7.2 Serial Bus Timing



Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between a stop and a start	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	0.6	--	--	ns
Data hold time	$t_{hd;dat}$	0	--	0.9	ns
Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	pf

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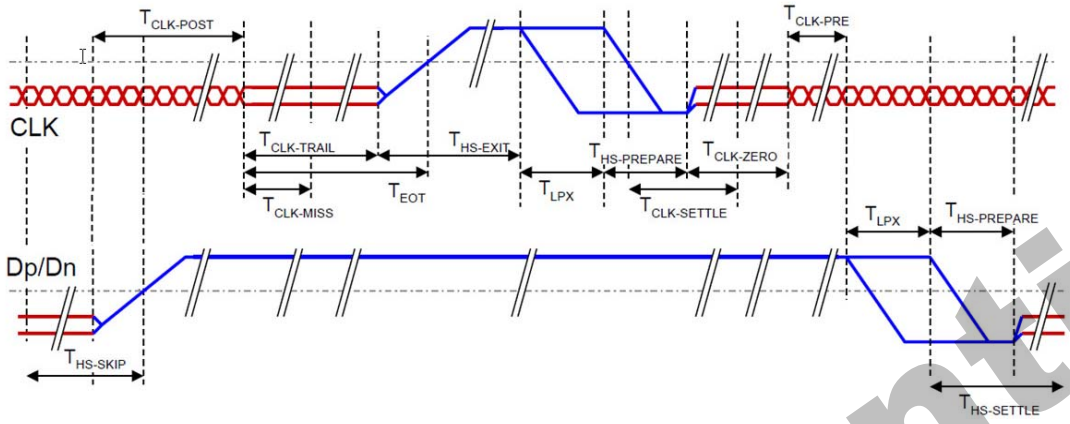
8. Applications

8.1 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP (and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous (independent of the high speed clock).

$T_{CLK\_HS\_PREPARE}$: setting by Register P3: 0x22

T_{CLK_ZERO}: setting by Register P3: 0x23

T_{CLK_PRE}: setting by Register P3: 0x24

T_{CLK_POST}: setting by Register P3: 0x25

T_{CLK_TRAIL}: setting by Register P3: 0x26

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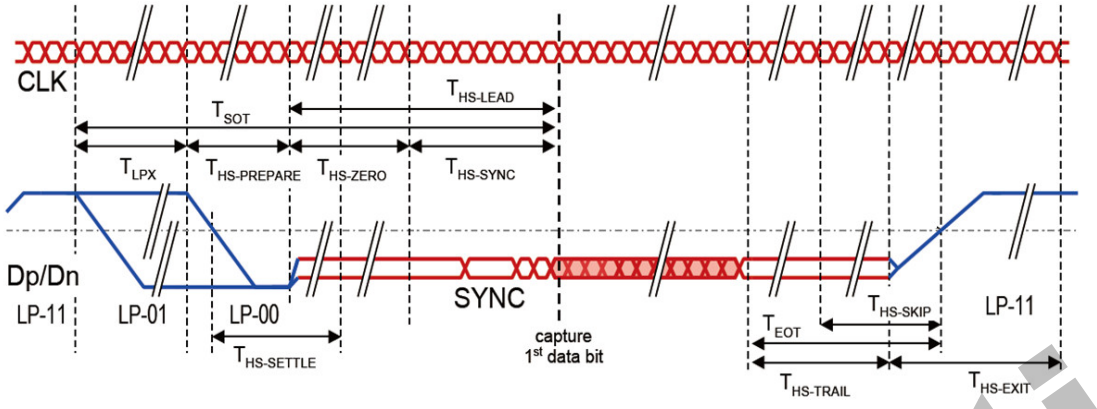
8.2 Data Burst



Notice:

- Clock keeps running and samples data lanes (except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY (a few bytes).
- Time-out to ignore line values during line state transition.

T_{LPX}: setting by Register P3: 0x21

$T_{HS\_PREPARE}$: setting by Register P3: 0x29

T_{HS_ZERO}: setting by Register P3: 0x2a

T_{HS_TRAIL}: setting by Register P3: 0x2b

T_{HS_EXIT}: setting by Register P3: 0x27

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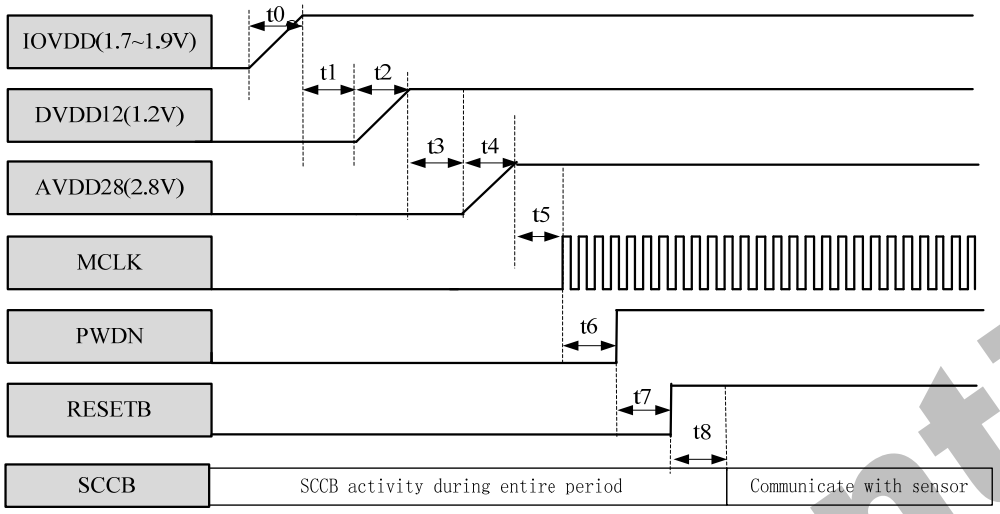
9. Power On/Off Sequence

9.1 Power On Sequence



Parameter	Description	Min.	Max.	Unit
t0	IOVDD rising time	50		µs
t1	From IOVDD to DVDD12	0		µs
t2	DVDD12 rising time	50		µs
t3	From DVDD12 to AVDD28	0		µs
t4	AVDD28 rising time	50		µs
t5	From AVDD28 to MCLK applied	0		µs
t6	From MCLK applied to Sensor enable	0		µs
t7	From PWDN pull high to RESET pull high	0		µs
t8	From Power on to SCCB works	25		mclk
SCCB	Frequency		400	KHz

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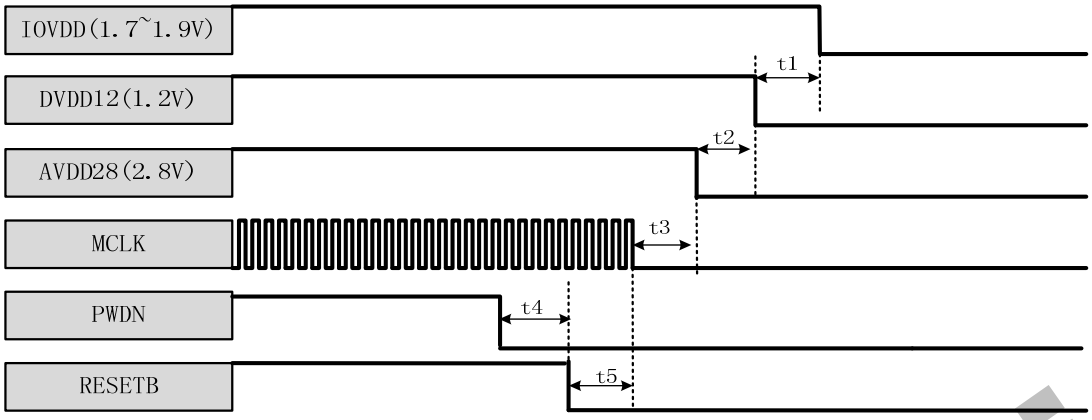
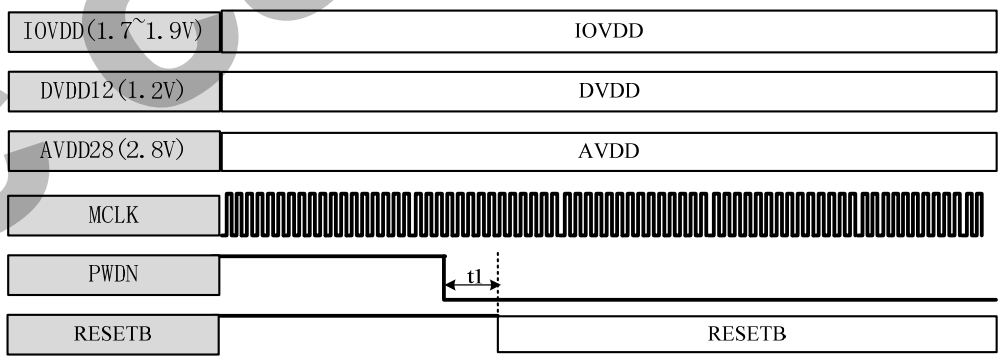
9.2 Power Off Sequence



Parameter	Description	Min.	Max.	Unit
t1	From DVDD12 to IOVDD power down	0		μs
t2	From AVDD28 to DVDD12 power down	0		μs
t3	From MCLK disable to sensor AVDD28 power down	0		μs
t4	From sensor disable to RESET pull low	0		μs
t5	From sensor RESET pull low to MCLK disable	0		μs

- Recommended power on/off sequence is above.
- If the sensor's power cannot be cut off, please keep power supply, then set PWDN pin high. It will make sensor standby

9.3 Standby Sequence



Parameter	Description	Min.	Max.	Unit
t1	From sensor disable to RESETB pull low(if possible)	0		us

- Register should be reload before works.

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10. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0xf0	**Sensor_ID_high**	**8**	**0x50**	**RO**	Chip ID high
0xf1	**Sensor_ID_low**	**8**	**0x25**	**RO**	Chip ID low
0xf2	I2C_open_enapwd_dn	2	0x00	RW	[5] I2C_open_ena [4] pwd_dn 0: pulldown 1: not pull
0xf3	OTP	8	0x00	WR	[7] read speed up [6] OTP_write WO [5] OTP_read WO [4] write speed up [3] OTP_acc_mode [2:0] OTP write interval
0xf7	PLL_mode1	4	0x00	RW	[3] scale_mode(dvpmode) [2] freq div2 switch delay mode , (need vs_st>0x10) [1] div2en [0] pll_en
0xf8	PLL_mode2	8	0x00	RW	[7:6] NA [5:0] divx4 eg:mclk 24 divx4=8 so pllclk_nodiv=24*8*4=768 for mipi pllclk=pllclk_nodiv/4=768/4=192
0xf9	analog_pwc	8	0x01	RW	[7:1] NA [0] apwd --- Not wether which will cause suicide
0xfa	clk_div_mode	8	0x00	RW	[7] div2 enable [6] close div2_frame mode [5] wpllclk_sel [4] mdclk_en [3] NA [2] NA [1] div2 [0] div 1
0xfb	I2c_device_id	8	0x74	RW	[7:1] I2C device id: 6e [0] NA
0xfc	cm_mode	8	0x00	RW	[7] regf clk enable [6] sys_rclk sel

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					[5] div2_mode [4] NA [3] isp all clock enable [2] serial clk enable [1] re_lock_pll [0] not_use_pll
0xfd	regf_buf_mode	5	0x00	RW	[4] cen_mode [3] buf_en [2] regf_buf_clk_en [1:0] sel_flag 1: buf2 0: buf1
0xfe	Reset related	8	0x00	RW	[7] soft_reset [6] cm_reset [5] mipi_reset [4] CISCTL_reset_n [2:0] page_select

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
P0:0x03	exp_in_high	6	0x00	RW	[5:0] exp_in[13:8]
P0:0x04	exp_in_low	8	0x10	RW	exp_in[7:0]
P0:0x05	HB_high	4	0x02	RW	[3:0] HB[11:8]
P0:0x06	HB_low	8	0x30	RW	HB[7:0]
P0:0x07	VB_high	5	0x00	RW	[4:0] VB[12:8]
P0:0x08	VB_low	8	0x10	RW	VB[7:0]
P0:0x09	Row_start_high	3	0x00	RW	[2:0] row_start[10:8]
P0:0x0a	Row_start_low	8	0x00	RW	Row_start[7:0]
P0:0x0b	Col_start_high	4	0x00	RW	[3:0]col_start[11:8]
P0:0x0c	Col_start_low	7	0x00	RW	[7:1] Col_start[7:1]
P0:0x0d	win_height_high	3	0x07	RW	[2:0] Win_ height[10:8]
P0:0x0e	win_height_low	8	0xe0	RW	Win_height[7:0]
P0:0x0f	win_width_high	4	0x05	RW	[3:0] Win_ width[11:8]
P0:0x10	win_width_low	7	0x20	RW	[7:1] win_width[7:1]
P0:0x13	Vs_st	8	0x15	RW	[7:0] Vs_st
P0:0x14	Vs_et	8	0x02	RW	[7:0] Vs_et
P0:0x17	CISCTL_mode1	8	0xc0	RW	[7:2] reserved [1] updown [0] mirror

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P1:0xa8	Strobe_request, Strobe_ack Strobe_mode	8	0x32	RW	[7] strobe_request [6] strobe_ack, ready_only [5] delay ack [4] led always on [3] whole frame [2] whole vb [1] enable [0] 0: Xenon 1: LED
P1:0xa9	Strobe_start_row	8	0x00	RW	Strobe_start_row
P1:0xaa	Strobe_lasts_row[7:0]	8	0x04	RW	Strobe_lasts_row[7:0]
P1:0xab	Strobe_lasts_row[13:8]	6	0x00	RW	[5:0] Strobe_lasts_row[13:8]
P1:0xac	Strobe_start_frame, Strobe_skip_frame	8	0x30	RW	[7:4] Strobe_start_frame [3:0] Strobe_skip_frame
P1:0xad	Strobe_luma_th	8	0x40	RW	[7:0] strobe_luma_th
P1:0xae	Strobe_mode2	4	0x00	RW	[3] out en [2] request_neg_mode [1] env_adaptive_mode [0] request_D_mode

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Address	Name	Width	Default Value	R/W	Description
P3:0x01	DPHY_analog_mode1	8	0x00	RW	[7] disable_set[1] [6:5] clkctr [4] NA [3] disable_set[0] [2] dphy_lane1_en [1] dphy_lane0_en [0] dphy_clk_en
P3:0x02	DPHY_analog_mode2	8	0x00	RW	[7:6] data1ctr [5:4] data0ctr [3] NA [2:0] mipi_diff
P3:0x03	DPHY_analog_	8	0x00	RW	[7] clklane_p2s_sel

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	mode3				[6] NA [5] data1delay1s [4] data0delay1s [3] clk_delay1s [2] mipi_en [1:0] clkhs_ph
P3:0x04	FIFO_prog_full_level[7:0]	8	0x08	RW	[7:0] FIFO_prog_full_level[7:0]
P3:0x05	FIFO_prog_full_level[11:8]	4	0x00	RW	[7:4] NA [3:0] FIFO_prog_full_level[11:8]
P3:0x06	FIFO_mode	8	0x00	RW	[7] NA [6] RF2 32X32 cen [5] mipi write gate mode [4] FIFO_rst_mode [3] RAW10_bit_swicth_mode [2] NA [1] write fifo gate mode [0] read fifo gate mode
P3:0x11	LDI_set	8	0x2b	RW	RAW8：0x2a RAW10：0x2b
P3:0x12	LWC_set[7:0]	8	0xa8	RW	Raw8：2592
P3:0x13	LWC_set[15:8]	8	0x0c	RW	Raw10：2592x5/4
P3:0x14	SYNC_set	8	0xb8	RW	SYNC_set
P3:0x15	DPHY_mode	8	0x10	RW	[7] NA [6] freq_div2 MIPI para invar [5] DATA lane gate mode [4] all_lane_open_mode [3:2] switch_msb_mode [1:0] clklane_mode
P3:0x16	LP_set	8	0x29	RW	[7:6] hi-z [5:4] use define [3:2] 1 [1:0] 0
P3:0x18	DPHY_analog_mode4	8	0x00	RW	[7:4] mp_reserve [3:2] data0hs_ph [1:0] data1hs_ph
P3:0x1b	Fifo2_prog_full_level	6	0x0c	RW	[5:0] Fifo2_prog_full_level
P3:0x1c	Fifo2_push_prog_full_level	6	0x10	RW	[5:0] Fifo2_push_prog_full_level
P3:0x1d	Sram_test_mode	4	0x02	RW	[3] 1:write_fifo_gate mode [2] 1:read_fifo_gate mode [1] 1:sram gate

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					[0] sram test mode
P3:0x20	T_init_set	8	0x80	RW	Timing of initial setting, more than 100 us
P3:0x21	T_LPX_set	8	0x10	RW	Timing of LP setting, more than 50ns
P3:0x22	T_CLK_HS_PREPARE_set	8	0x05	RW	Timing of COCLK HS PREPARE setting, 38ns ~95ns LP00
P3:0x23	T_CLK_zero_set	8	0x30	RW	Timing of COCLK HS zero setting, more than 300ns
P3:0x24	T_CLK_PRE_set	8	0x02	RW	Timing of COCLK HS PRE of Data setting, more than 8UI
P3:0x25	T_CLK_POST_set	8	0x10	RW	Timing of COCLK HS Post of Data setting, 60ns +52UI
P3:0x26	T_CLK_TRAIL_set	8	0x08	RW	Timing of COCLK tail setting, 60ns
P3:0x27	T_HS_exit_set	8	0x10	RW	Timing of HS exit setting, more than 100ns
P3:0x28	T_wakeup_set	8	0xa0	RW	Timing of wakeup setting, 1ms
P3:0x29	T_HS_PREPARE_set	8	0x06	RW	Timing of data HS PREPARE setting, 45+4UI~85+5UI
P3:0x2a	T_HS_Zero_set	8	0x0a	RW	Timing of data HS zero setting, 140ns
P3:0x2b	T_HS_TRAIL_set	8	0x08	RW	Timing of data HS trail setting, 60ns
P3:0x30	MIPI_test	2	0x00	RW	[7:2] NA [1:0] MIPI_test [1] clk [0] data
P3:0x31	MIPI_test_data0	8	0x96	RW	MIPI_test_data0
P3:0x32	MIPI_test_data1	8	0x3a	RW	MIPI_test_data1
P3:0x33	MIPI_test_data2	8	0x87	RW	MIPI_test_data2
P3:0x34	MIPI_test_data3	8	0xb5	RW	MIPI_test_data3
P0:0x3e	fifo_pop_error fifo_push_error fif01_full fifo1_error	4	0x00	RW	W: [3] clear_fifo_pop_error [2] clear_fifo_push_error [1] clear_fifo1_full [0] clear_fifo1_error R: [3] fifo_pop_error_valid [2] fifo_push_error_valid [1] fifo1_full_valid [0] fifo1_error_valid
P0:0x3f	CIS2_mode	8	0x00	RW	[7] LaneEna [6] NA [5] ULPEna [4] MIPI_ena

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					[3] NA [2] RAW8_mode [1] line_sunc_mode [0] DoubleLane_en

ISP Related

Address	Name	Width	Default Value	R/W	Description
P0:0x90	win_mode	1	0x01	RW	[7:1] NA [0] crop out win mode
P0:0x91	Crop_win_y1_high	3	0x00	RW	[7:3] NA [2:0] Crop _win_y1[10:8]
P0:0x92	Crop_win_y1_low	8	0x00	RW	Crop _win_y1[7:0]
P0:0x93	Crop_win_x1_high	4	0x00	RW	[7:4] NA [3:0] Crop _win_x1[11:8]
P0:0x94	Crop_win_x1_low	8	0x00	RW	Crop _win_x1[7:0]
P0:0x95	out_win_height_high	3	0x07	RW	[7:3] NA [2:0] Out window height[10:8]
P0:0x96	out_win_height_low	8	0x98	RW	Out window height[7:0]
P0:0x97	out_win_width_high	4	0x0a	RW	[7:4] NA [3:0] Out window width[11:8]
P0:0x98	out_win_width_low	8	0x20	RW	Out window width[7:0]

BLK

Address	Name	Width	Default Value	R/W	Description
P0:0x40	Blk_mode1	8	0x23	RW	[7:2] reserved [1] dark_current_en [0] offset_en
P0:0x45	manual_G1_odd_offset	6	0x00	RW	manual_G1_odd_offset S5
P0:0x46	manual_R1_odd_offset	6	0x00	RW	manual_R1_odd_offset S5
P0:0x47	manual_B2_odd_offset	6	0x00	RW	manual_B2_odd_offset S5

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P0:0x48	manual_G2_odd_offset	6	0x00	RW	manual_G2_odd_offset S5
P0:0x60	offset_ratio	8	0x00	RW	offset_ratio ,1.7
P0:0x61	dark_current_ratio	8	0x80	RW	dark_current_ratio ,1.7

GLOBAL/PRE/POSTGAIN

Address	Name	Width	Default Value	R/W	Description
P0:0xb0	Global_gain	8	0x40	RW	Global gain
P0:0xb1	Auto_pregain_high	4	0x01	RW	[3:0] Auto_pregain[9:6] 100->1x
P0:0xb2	Auto_pregain_low	6	0x00	RW	[7:2] Auto_pregain[5:0]
P0:0xb6	Gain_code	4	0x00	RW	[7:4] NA [3:0] Gain_code
P0:0xb7	buf_freq_div2	1	0x00	RW	[7:1] NA [0] freq_div2
P0:0xc6	Channel_gain_G1_odd[10:3]	8	0x80	RW	[7:0] Channel_gain_G1_odd[10:3]
P0:0xc7	Channel_gain_R1_odd[10:3]	8	0x80	RW	[7:0] Channel_gain_R1_odd[10:3]
P0:0xc8	Channel_gain_B2_odd[10:3]	8	0x80	RW	[7:0] Channel_gain_B2_odd[10:3]
P0:0xc9	Channel_gain_G2_odd[10:3]	8	0x80	RW	[7:0] Channel_gain_G2_odd[10:3]
P0:0xc4	Channel_gain_G1_odd[2:0] Channel_gain_R1_odd[2:0]	8	0x00	RW	[6:4] Channel_gain_G1_odd[2:0] [2:0] Channel_gain_R1_odd[2:0]
P0:0xc5	Channel_gain_B2_odd[2:0] Channel_gain_G2_odd[2:0]	8	0x00	RW	[6:4] Channel_gain_B2_odd[2:0] [2:0] Channel_gain_G2_odd[2:0]

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