GC8034 COB

1/4″ 8Mega CMOS Image Sensor

Datasheet

Rev.1.4

2017-11-23

Ordering Information

◆ **GC8034W(Pcode:200)**

(Color, 200um, back grinding, reconstructed wafer)

GENERATION REVISION HISTORY

REV.	*EFFECTIVE DATE*	*DESCRIPTION OF CHANGES*	*PREPARED BY*
V1.0	*2017-03-10*	*Document Release*	*AE Dept.*
V1.1	*2017-05-12*	*Update Standby Sequence* *Update mipi data rate*	*AE Dept.*
V1.2	*2017-07-24*	*Update Package and TBD parameters*	*AE Dept.*
V1.3	*2017-10-23*	*Update Package*	*AE Dept.*
V1.4	*2017-11-23*	*Update Thickness of die*	*AE Dept.*

Content

1. Sensor Overview

1.1 General Description

GC8034 is a 1/4-inch format CMOS digital image sensor, with an active pixel of 3264H x 2448V. It incorporates sophisticated on-die camera functions such as windowing, mirror, row binning and skip modes. It is programmable through a simple two-wire serial interface and has very low power consumption. It provides RAW10 and RAW8 data formats with MIPI interface.

The full scale integration of high-performance and low-power functions make the GC8034 fit the design, reduce implementation process, and extend the battery life of cell phones, PDAs, and a wide variety of mobile applications.

1.2 Features

- Standard optical format of 1/4 inch
- Output formats: Raw Bayer 10bit/8bit
- Power supply requirement: AVDD28: 2.8V
  DVDD12: 1.2V
  IOVDD: 1.8V
- Data rate: MIPI 4 Lane 30fps@ full size 672Mbps/lane；
  MIPI 2Lane 30fps@ full size 1286.4Mbps/lane
- Windowing support
- MIPI(2_lane/4_lane) interface support
- Horizontal/Vertical mirror
- 8K-bits OTP support for user (WB, LSC, and etc.)
- 2X2 binning readout function
- Dual sensor synchronization operation
- Auto Black level calibration

1.3 Technical Specifications

Parameter	Typical value
Optical Format	1/4 inch
Pixel Size	1.12μm x 1.12μm(BSI)
Active pixel array	3264 x 2448
Shutter type	Electronic rolling shutter
ADC resolution	10 bit ADC
Max Frame rate	30fps@full size
Power Supply	AVDD28: 2.7~3.0V DVDD12: 1.15~1.3V IOVDD: 1.7~3.0V
Power Consumption	180mW@30fps
SNR	36.77dB
Dark Current	34e-/s(60℃)
Sensitivity	2628 e-/lux.s
Dynamic range	63.5dB
Operating temperature:	-20~70℃
Stable Image temperature	0~60℃
Max optimal lens chief ray angle(CRA)	32.55 °(non-linear)
Package type	TPLCC/COB
Input clock frequency	6~27MHz

2. DC Characteristics

2.1 Standby Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	30	60	uA
Digital	I_{DVDD}	—	1	5	mA
I/O	I_{IOVDD}	—	20	200	uA

RST: L, PWND: L

Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.2 Power off Current

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	0	0	uA
Digital	I_{DVDD}	—	0	0	uA
I/O	I_{IOVDD}	—	0	0	uA

Power off, T_j=25℃

2.3 Operation Current

- **Full size (MIPI 2 lane @1286.4Mbps/Lane)**

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	20	35	mA
Digital	I_{DVDD}	—	95	140	mA
I/O	I_{IOVDD}	—	4	10	mA

INCLK: 24MHz, Frame rate: 30fps , Raw 10

Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

- **Full size (MIPI 4 lane @672Mbps/Lane)**

Item	Symbol	Min	Typ	Max	Unit
Analog	I_{AVDD}	—	20	35	mA
Digital	I_{DVDD}	—	90	140	mA
I/O	I_{IOVDD}	—	3	10	mA

INCLK: 24MHz, Frame rate: 30fps , Raw 10

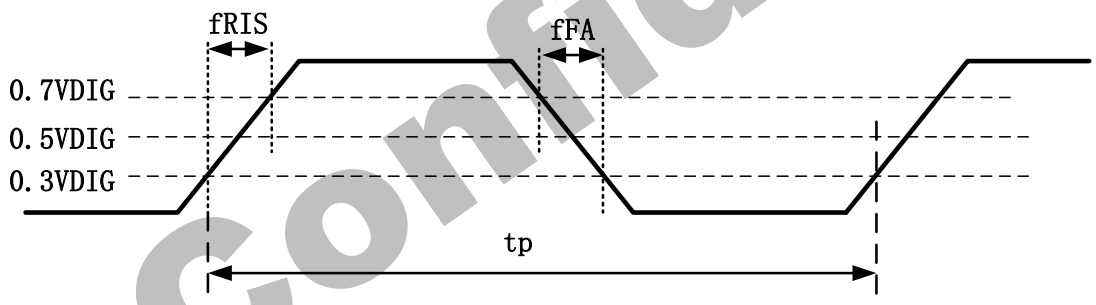
Typ. Analog: 2.8V, Digital: 1.2V, I/O:1.8V, T_j=25℃

2.4 DC Characteristics

Item	Symbol	Min	Typ	Max	Unit
Power supply	V_{AVDD}	2.7	2.8	3.0	V
	V_{DVDD}	1.15	1.2	1.3	V
	V_{IOVDD}	1.7	1.8	3.0	V
Digital Input(Conditions: AVDD = 2.8V, DVDD = 1.2V, IOVDD = 1.8V)					
Input voltage HIGH	V_{IH}	0.7*VIF			V
Input voltage LOW	V_{IL}			0.3*VIF	V
Digital Output(Conditions: AVDD = 2.8V, IOVDD = 1.8V, standard Loading 25PF)					
Output voltage HIGH	V_{OH}	0.65*VIF			V
Output voltage LOW	V_{OL}			0.35*VIF	V

3. AC Characteristics

Master clock wave diagram

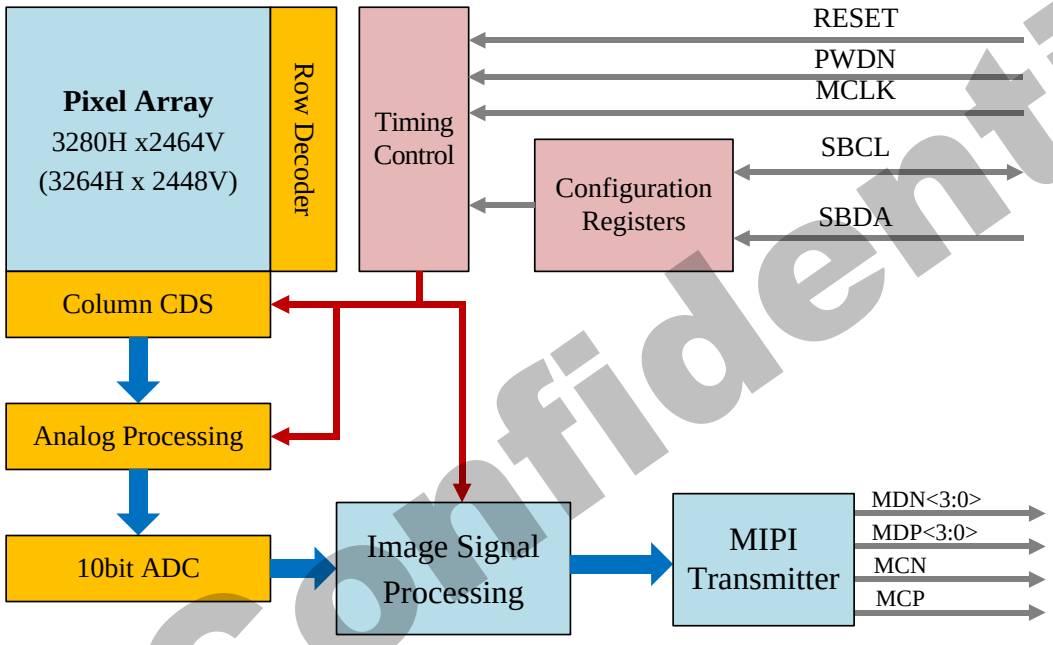


Input clock square waveform specifications：

Item	Symbol	Min.	Typ.	max	unit
Frequency	f_{SCK}	6	24	27	MHz
jitter (period, peak-to-peak)	T_{jitter}			600	ps
Rise Time	f_{RISE}	1		15	ns
Fall Time	f_{FALL}	1		15	ns
Duty Cycle	f_{DUTY}	40		60	%

4. Block Diagram

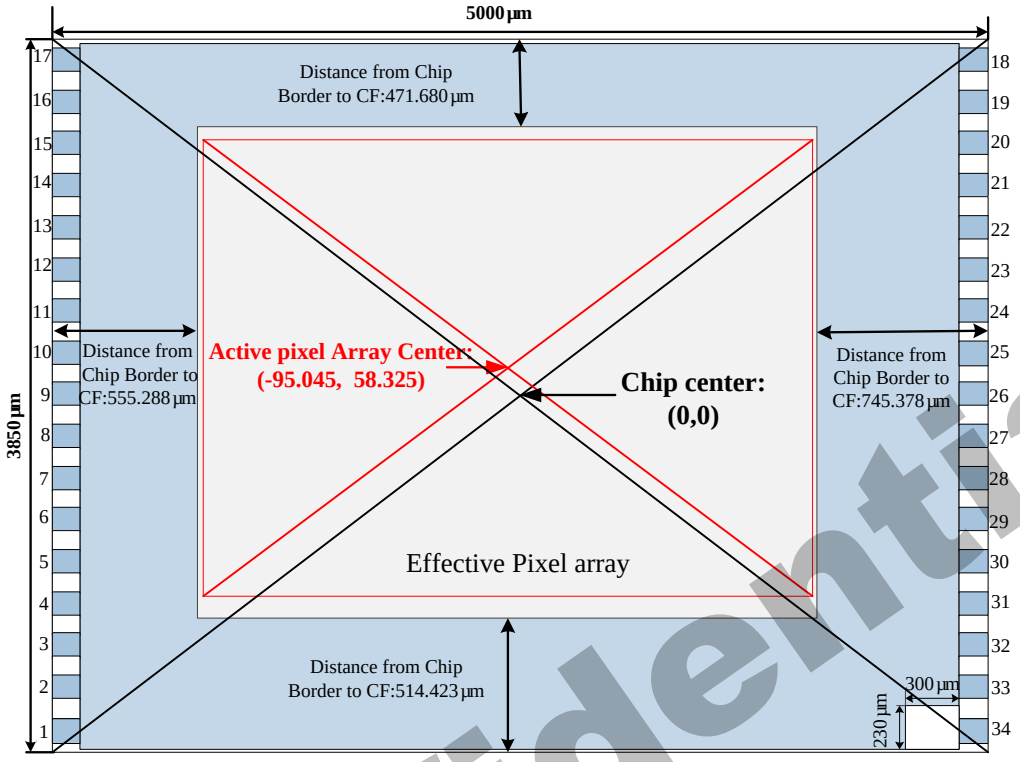
The GC8034 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) to generate all internal clocks from a single master input clock running between 6 MHz and 27 MHz. Output interface clocks may be generated by dedicated PLL for maximal flexibility in interface frequency and for EMI avoidance. The maximum data rate is 1286.4 Mbps at MIPI 2-lane, corresponding to the pixel rate of 320 MHz.



The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise caused by the in-pixel amplifier offset deviation. To eliminate those noise components, a Correlated Double Sampling (CDS) circuit is used before converting to digital.

The output from the ADC is a 10-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain which provides further data path corrections and applies digital gain. A shading correction block is used to compensate for color/brightness shading introduced by the lens. Additional functionality is provided which includes deterministic pattern generator, and a MIPI CSI-2 frame formatter with embedded line support.

5. COB Package

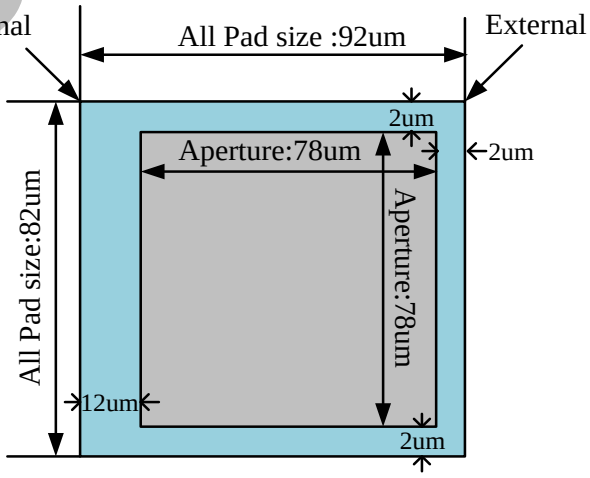


Top View

5.1 Pin Diagram(unit: μm)

***Die size: 5000x3850μm(without scribe line)**

***Thickness of die(wafer):200±10μm**



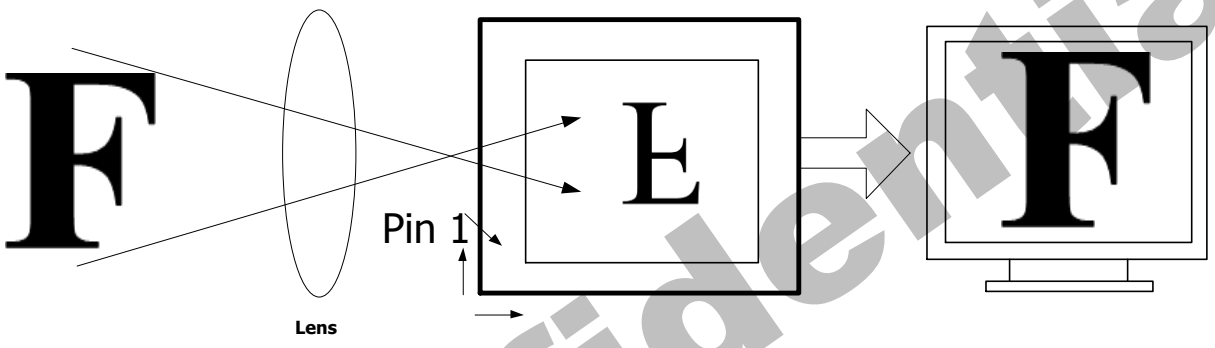
5.2 Pin Descriptions

Pin	POS X(um)	POS Y(um)	Name	Pin Type	Description
1	-2446	-1680	DGND	Ground	Digital ground
2	-2446	-1470	DVDD12	Power	Digital power supply pin: 1.2V
3	-2446	-1260	FSYNC	I/O	Frame sync control
4	-2446	-1050	SBDA	Output	I2C data
5	-2446	-840	SBCL	Output	I2C clock
6	-2446	-630	PWDN	I/O	Sensor power down control: 0: standby 1: normal work
7	-2446	-420	RESETB	I/O	Chip reset control: 0: chip reset 1: normal work
8	-2446	-210	IOVDD	Power	Power supply for I/O circuits: 1.7~3.0V
9	-2446	0	VOTP	Power	Internal power supply
10	-2446	210	VTX	Power	Internal power supply
11	-2446	420	VREF	Power	Internal power supply
12	-2446	630	AVDD28	Power	Main power supply pin: 2.8V
13	-2446	840	VRSEL	Power	Internal power supply
14	-2446	1050	NC	/	/
15	-2446	1260	NC	/	/
16	-2446	1470	AGND	Ground	Analog ground
17	-2446	1680	AVDD28	Power	Main power supply pin: 2.8V
18	2446	1680	IN_CLK	Input	Main clock
19	2446	1470	PLLVDD	Power	Internal power supply
20	2446	1260	DVDD12	Power	Digital power supply pin: 1.2V
21	2446	1050	DGND	Ground	Digital ground
22	2446	840	MDP<2>	Output	MIPI data <2> (+)
23	2446	630	MDN<2>	Output	MIPI data <2> (-)
24	2446	420	MDP<0>	Output	MIPI data <0> (+)
25	2446	210	MDN<0>	Output	MIPI data <0> (-)
26	2446	0	DVDD12	Power	Digital power supply pin: 1.2V
27	2446	-210	MCP	Output	MIPI clock (+)
28	2446	-420	MCN	Output	MIPI clock (-)
29	2446	-630	MDP<1>	Output	MIPI data <1> (+)
30	2446	-840	MDN<1>	Output	MIPI data <1> (-)
31	2446	-1050	MDP<3>	Output	MIPI data <3> (+)
32	2446	-1260	MDN<3>	Output	MIPI data <3> (-)
33	2446	-1470	DGND	Ground	Digital ground
34	2446	-1680	DVDD12	Power	Digital power supply pin: 1.2V

6. Optical Specifications

6.1 Readout Position

The GC8034 default status is readout from the lower right corner with pin 1 located in the bottom of left. The proper image output as follow when Pin 1 is located in the lower left corner as the lens inverts image vertically and horizontally.

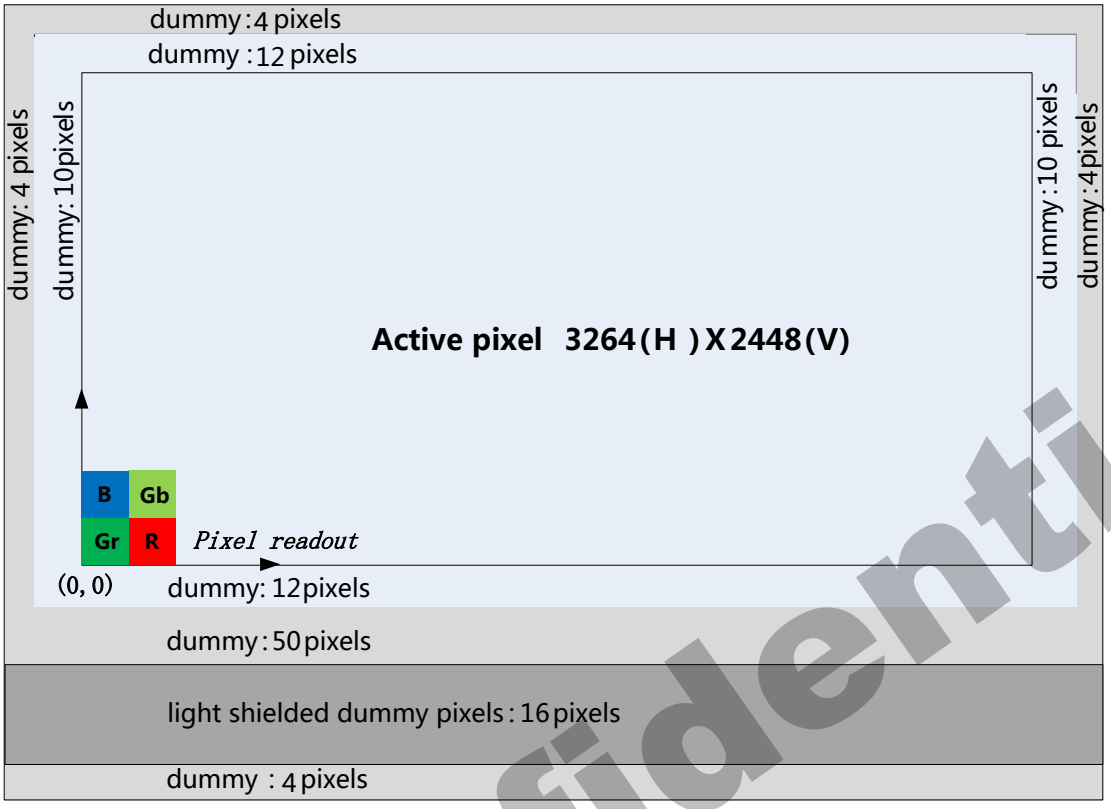


Readout direction can be set by the registers.

Function	Register Address	Register Value	First Pixel
Normal	P0:0x17[1:0]	00	Gr
Horizontal mirror	P0:0x17[1:0]	01	R
Vertical Flip	P0:0x17[1:0]	10	B
Horizontal Mirror and Vertical Flip	P0:0x17[1:0]	11	Gb

Horizontal Mirror Vertical Flip Horizontal Mirror and Vertical Flip

6.2 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 3263. If flip in column, column is read out from 3263 to 0.

If no flip in row, row is read out from 0 to 2447.If flip in row, row is read out from 2447 to 0.

6.3 Lens Chief Ray Angle (CRA)

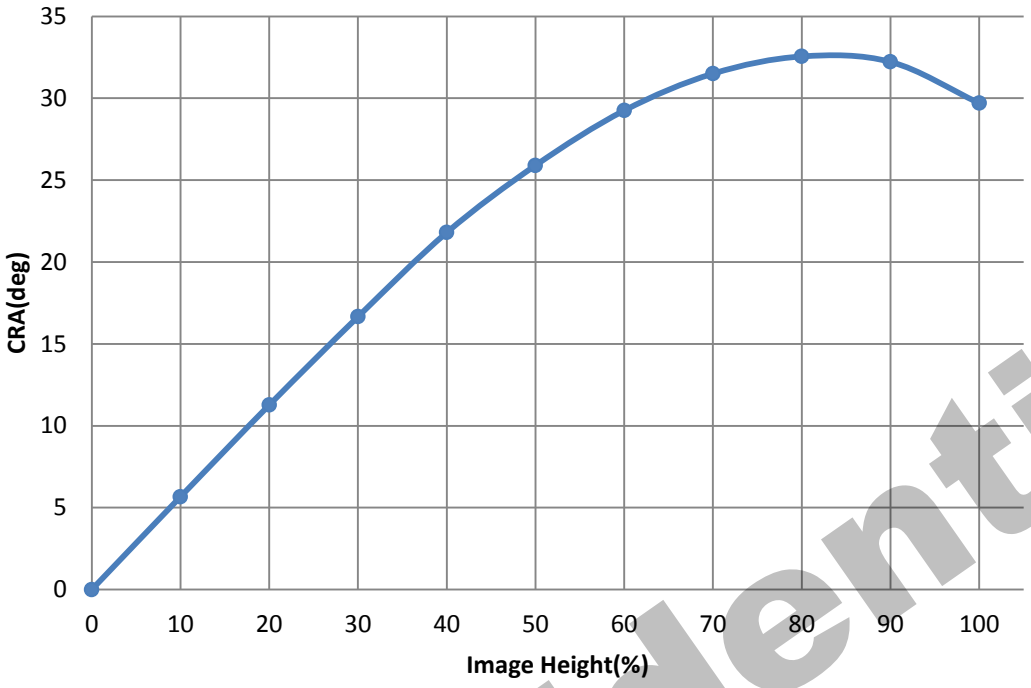
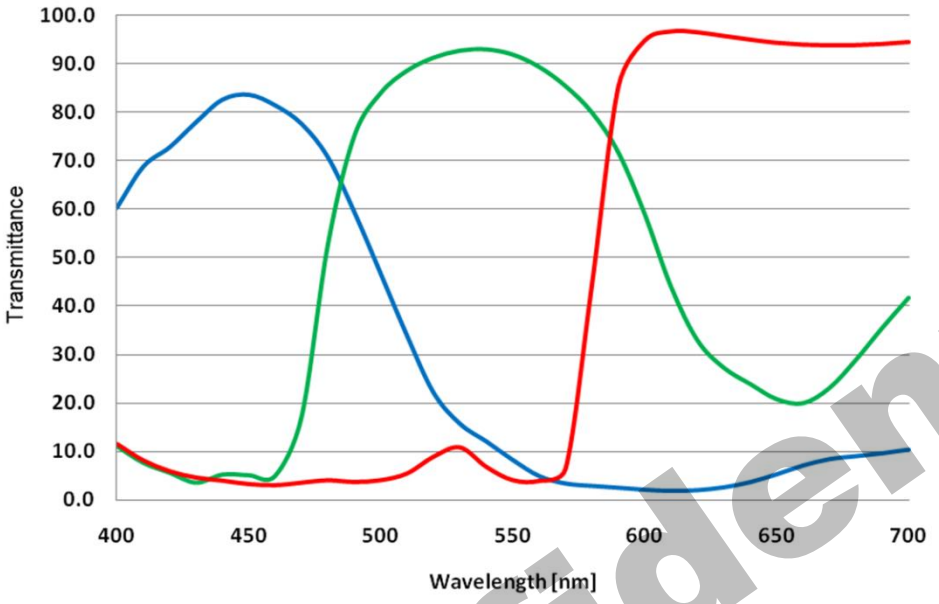


Image Height（%）	Image Height（mm)	CRA (degree)
00	0.000	0.0
10	0.230	5.67
20	0.459	11.27
30	0.689	16.66
40	0.919	21.80
50	1.149	25.90
60	1.378	29.25
70	1.608	31.50
80	1.838	32.55
90	2.068	32.22
100	2.297	29.70

6.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below:



7. Two-wire Serial Bus Communication

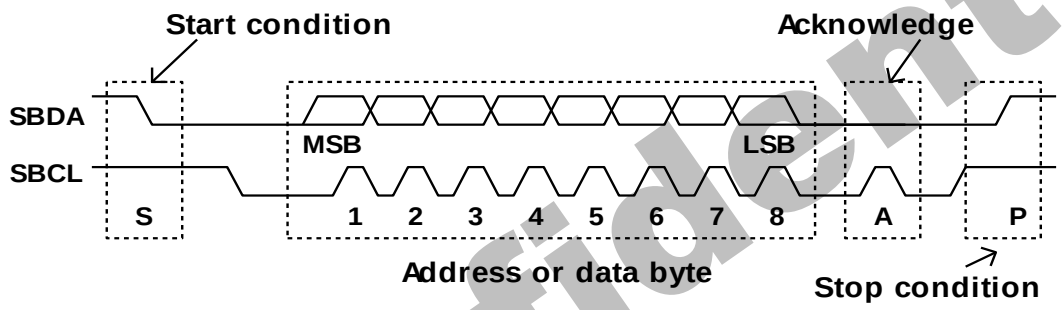
GC8034 Device Address:

serial bus write address = 0x6e, serial bus read address = 0x6f

7.1 Protocol

The host must perform the role of a communications master and GC8034 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL.**



Single Register Writing:

S	6eH	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	6eH	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	6eH	A	Register Address	A	S	6fH	A	Data	NA	P

Notes:

From master to slave From slave to master

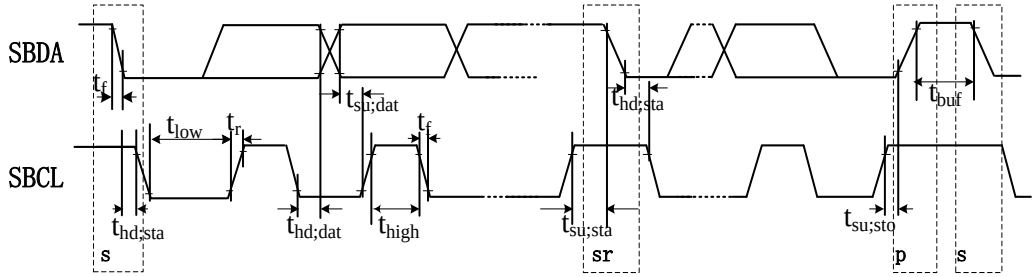
S: Start condition **P:** Stop condition

A: Acknowledge bit **NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value

7.2 Serial Bus Timing



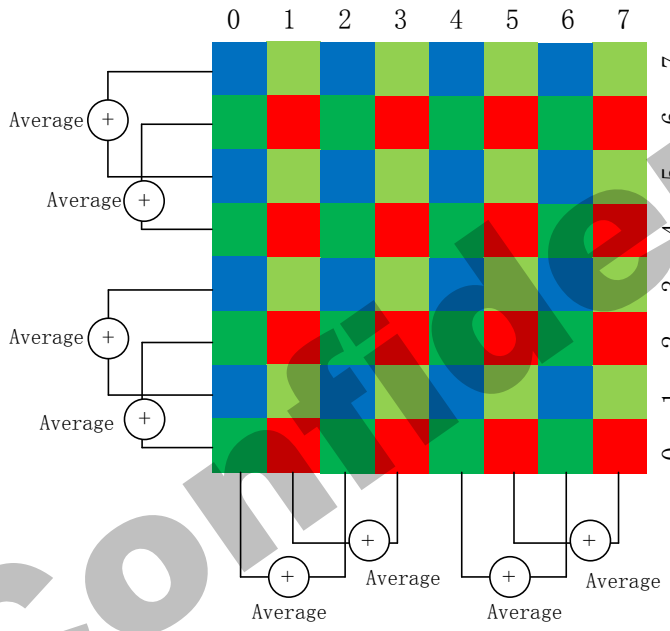
Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between a stop and a start	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	600	--	--	ns
Data hold time	$t_{hd;dat}$	0	--	900	ns
Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	pf

8. Function features

8.1 Binning mode

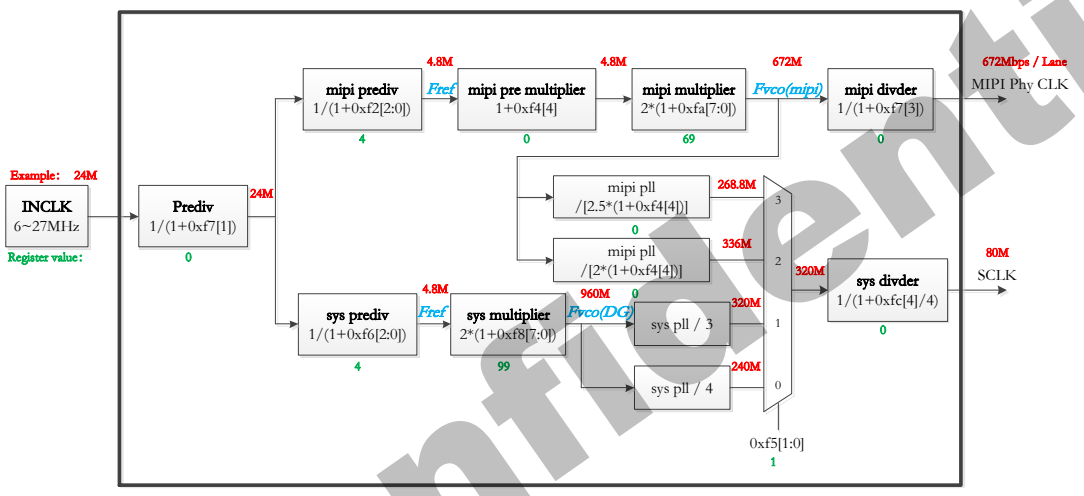
Binning read-out can be used to obtain an image of lower resolution for full field of view.

The following diagram describes on 2x2 averaged binning operations. Pixels of two adjacent rows and columns are averaged, and read out as one output pixel.

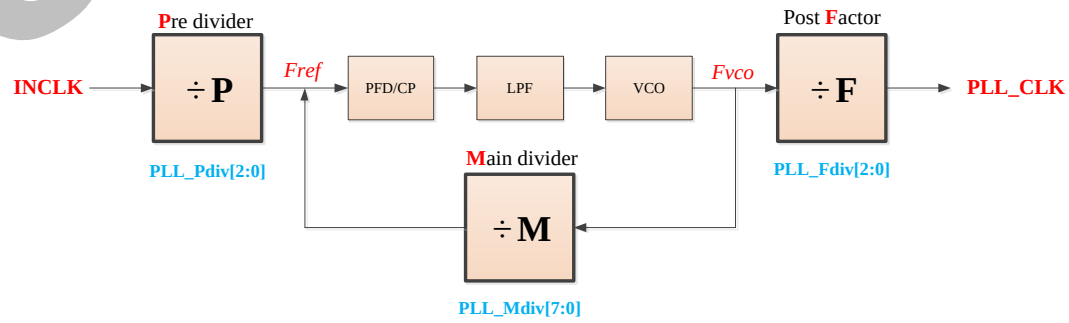


8.2 PLL and clock Generator

This chapter deals with the controlling over PLL and clock dividers in GC8034. In general, user should not apply clock control changes over the published modes of operation defined. In case the user requests to make adaptation in an operating mode for his application, it is strongly suggested that he contacts an FAE and describe its needs. It is not the intention of this document to give the user tools to create new modes of operation.



The clock system uses system phase-locked loop (PLL_DG), system clock dividers, interface phase-locked loop (PLL_MIPI), and interface clock dividers to generate all internal clocks from a single master input clock running between 6MHz and 27MHz.



$$\text{PLL\_CLK} = \text{INCLK} \times \left[\frac{M}{P} \times \frac{1}{F}\right]$$

PLL_DG Component Output Frequency

Parameter	Min.	Typ.	Max.	Unit	Remarks
Input frequency range	6	--	27	MHz	INCLK frequency range
Reference frequency range	4	--	12	MHz	Output of pre divider (Fref)
VCO frequency range	624	--	1150	MHz	Output of PLL multiplier VCO oscillation range (Fvco)
PLL output frequency range	156	--	1150	MHz	Output of PLL post factor

PLL_MIPI Component Output Frequency

Parameter	Min.	Typ.	Max.	Unit	Remarks
Input frequency range	6	--	27	MHz	INCLK frequency range
Reference frequency range	4	--	12	MHz	Output of pre divider (Fref)
VCO frequency range	624	--	1440	MHz	Output of PLL multiplier VCO oscillation range (Fvco)
PLL output frequency range	78	--	1440	MHz	Output of PLL post factor

8.3 Gain Control

GC8034 can apply analog gain and digital gain on CMOS.

Analog Gain is controlled by P0:0xb6

P0:0xb6	A Gain	P0:0xb6	A Gain
0x00	1x	0x05	5.6x
0x01	1.4x	0x06	8x
0x02	2x	0x07	11.2x
0x03	2.8x	0x08	16x
0x04	4x	/	/

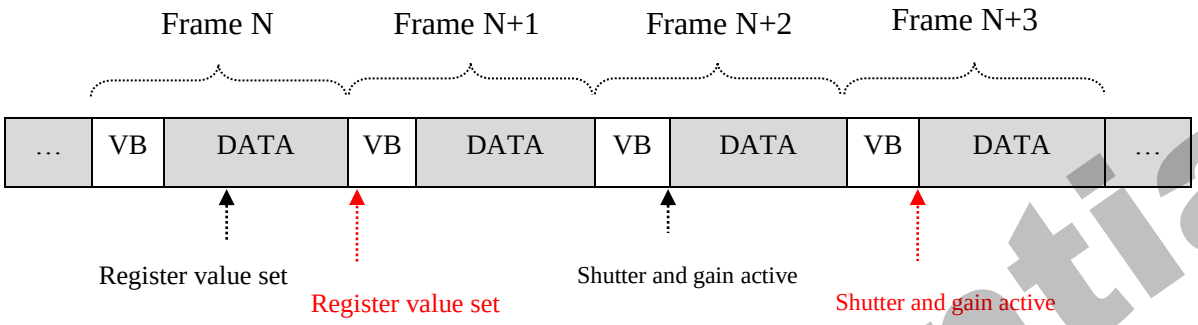
Digital Gain is controlled by P0:0xb1[3:0],0xb2[7:0]

D gain= 0xb1 + 0xb2 / 256, Max gain=15.99x

8.4 Shutter and Gain

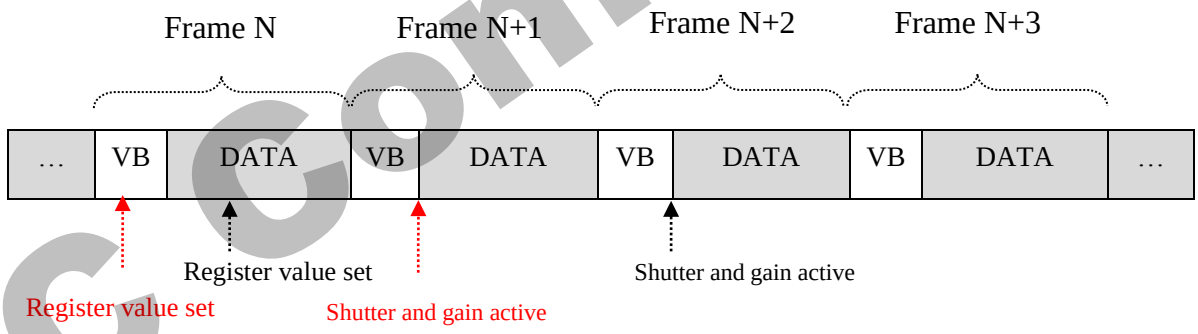
Mode1：

When P0:0x8e[7]=0, if you set shutter and gain at the frame N, shutter and gain will active at the frame N+2,.



Mode2：

When P0:0x8e[7]=1, if you set shutter and gain at the frame N in VBlank, shutter and gain will active at the frame N+1; if you set shutter and gain at the frame N in DATA, shutter and gain will active at the frame N+2 .

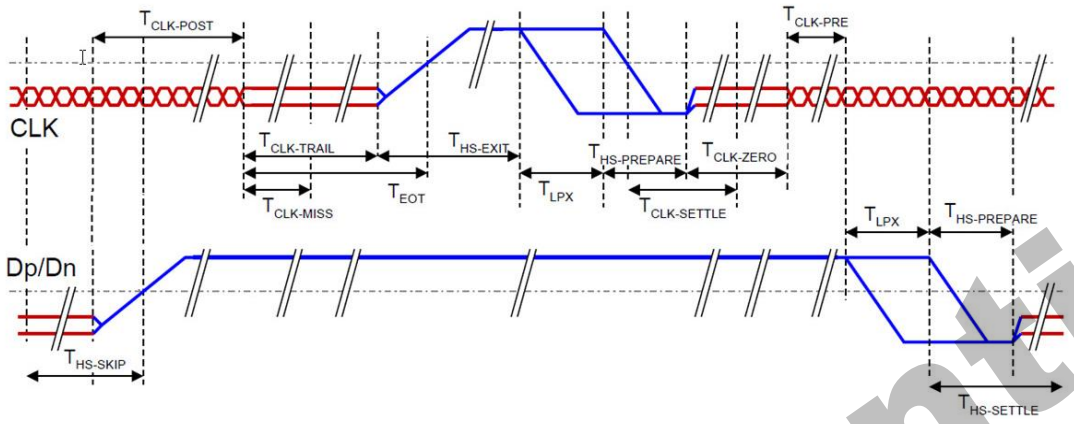


8.5 One Time Programmable(OTP) Memory

The GC8034 supports a maximum of 8k bits (1024 bytes) of one time programmable(OTP) memory to store module information, shading, WB, which can be controlled through the SCCB.

9. Applications

9.1 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching.
- Clock can go to LP only if data lanes are in LP(and nothing relies on it).
- In Low-Power data lanes are conceptually asynchronous(independent of the high speed clock).

  $T_{CLK\_HS\_PRE}$: setting by Register P3: 0x22

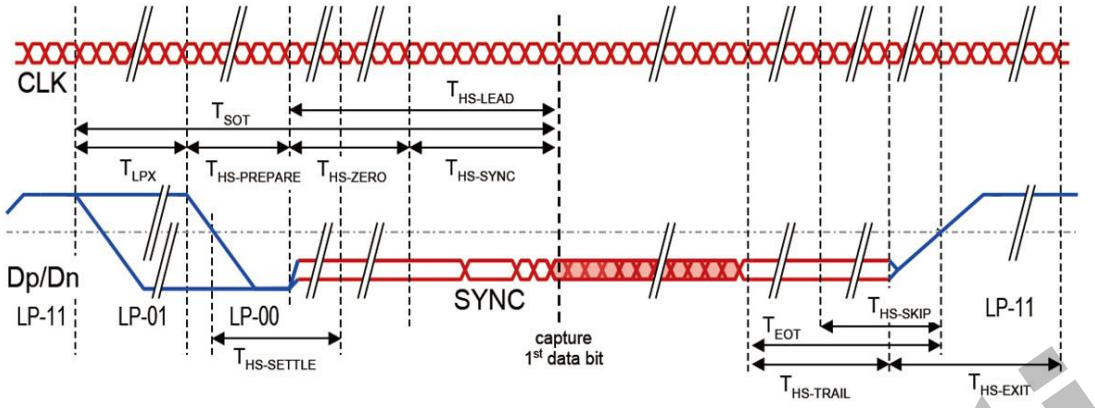
  T_{CLK_ZERO} : setting by Register P3: 0x23

  T_{CLK_PRE} : setting by Register P3: 0x24

  T_{CLK_POST} : setting by Register P3: 0x25

  T_{CLK_TRAIL} : setting by Register P3: 0x26

9.2 Data Burst



Notice:

- Clock keeps running and samples data lanes(except for lanes in LPS).
- Unambiguous leader and trailer sequences required to distill real bits.
- Trailer is removed inside PHY(a few bytes).
- Time-out to ignore line values during line state transition.

T_{LPX}: setting by Register P3: 0x21

$T_{HS\_PREPARE}$: setting by Register P3: 0x29

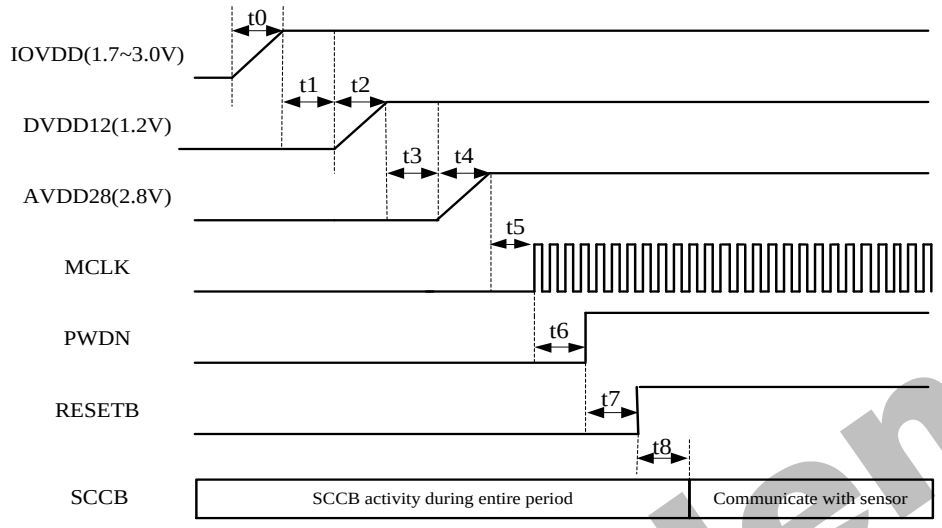
T_{HS_ZERO}: setting by Register P3: 0x2a

T_{HS_TRAIL}: setting by Register P3: 0x2b

T_{HS_EXIT}: setting by Register P3: 0x27

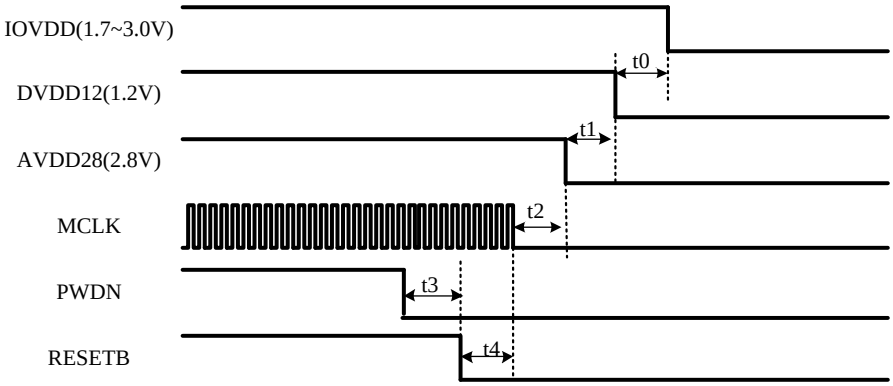
10. Power On/Off Sequence

10.1 Power On Sequence



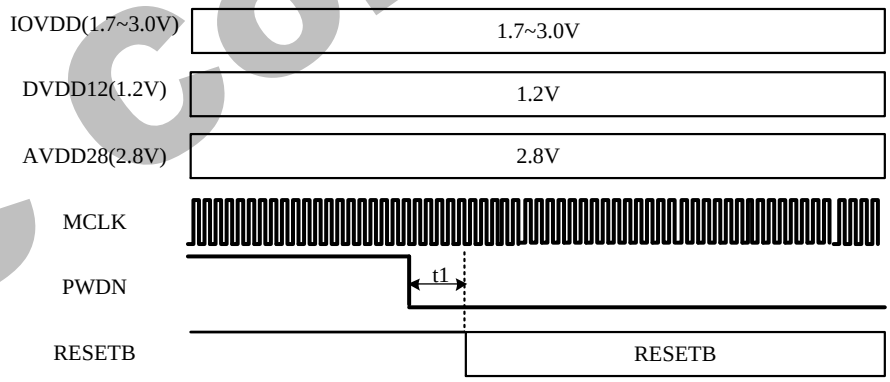
Parameter	Description	Min.	Typ	Max.	Unit
t0	IOVDD rising time	50			µs
t1	From IOVDD to DVDD12	0			µs
t2	DVDD12 rising time	50			µs
t3	From DVDD12 to AVDD28	10			µs
t4	AVDD28 rising time	50			µs
t5	From AVDD28 to MCLK applied	10			µs
t6	From MCLK applied to Sensor enable	10			µs
t7	From PWDN pull high to RESET pull high	0			µs
t8	From RESET pull high to SCCB works	25			inclk

10.2 Power Off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From DVDD12 to IOVDD power down	0		us
t1	From AVDD28 to DVDD12 power down	0		us
t2	From MCLK disable to AVDD28 power down	0		us
t3	From sensor disable to RESET pull low	0		us
t4	From sensor RESET pull low to MCLK disable	0		us

10.3 Standby Sequence



Parameter	Description	Min.	Max.	Unit
t1	From sensor disable to RESETB pull low(if possible)	0		us

11. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0xf0	**CHIP_ID_high**	**8**	**0x80**	**RO**	**[7:0]CHIP ID high**
0xf1	**CHIP_ID_low**	**8**	**0x44**	**RO**	**[7:0]CHIP ID low**
0xf2	analog_pwd I2C_open_ena pwd_dn read_clock_mode mdclk_en	5	0x80	RW	[7]apwd [6]OTP_auto_start(WO) [5] I2C_open_ena [4] pwd_dnb [3] div2_mode [2] read_clock_switch_gating [1]read_clock_mode [0]mdclk_en
0xf3	OTP_mode_new	8	0x00	RW	[7]auto generate Read signal [6]OTP_write (WO) [5]OTP_read (WO) [4]auto generate Write signal [3] NA [2:0] OTP_read_interval
0xf4	Pll_ldo_mode	8	0x10	RW	[7:4]pll_ldo_mode[3:0] [7]pll_ldo_en [6:5]pll_ldo_set [4]pll_2lane_en [3]OTP_enable [2]write_one_bit [1]addr_auto_acc [0]read_one_bit
0xf5	Clk_sel	8	0x19	RW	[7]pllmp_div2p5_inv_mode [6] close_2_frame_freq [5:3]rclk_sel [2:0]wclk_sel
0xf6	use_sync_clk refmp_div refdg_div	7	0xc4	RW	[7]use_sync_clk [6:4]refmp_div [2:0]refdg_div

0xf7	PLL_mode1	8	0x80	RW	[7]freq_div2_hold [6]freq_div2_analog [5]bypass_clk_auto_switch [4]pllmp_en [3]mipi_div2 [2]freq div2 [1]div2en [0]plldg_en
0xf8	PLL_mode2	8	0x16	RW	[7:0]plldg_div
0xf9	Pll_ldo_mode[7:4]	4	0x0	RW	[7]PLLdg_rst [6]PLLmp_rst [5] refdg_rst [4] refmp_rst [3:0] pll_reserve
0xfa	clk_div_mode	8	0x4a	RW	[7:0]pllmp div
0xfb	i2c_device_id	8	0x6e	RO	[7:1] i2c_device_id [0] NA
0xfc	cm_mode	8	0x08	RW	[7] regf clk enable [6] pllmp_div2_enable [5] read_clock_en [4] div2 [3] mclk enable [2] serail_clk enable [1] re_lock_pll [0] not_use_pll
0xfd	REGF_BUF_mode	6	0x00	RW	[7]pll_clk_rst(WO) [5]REGF_rewg_select [4]cen_mode [3]buf_en [2]page_select_mode [1:0]sel_flag
0xfe	Page_select	3	0x00	RW	[7]soft_rst (WO) [6]cm_rst (WO) [5]MIPI_rst (WO) [4]CISCTL_rst (WO) [3]NA [2:0]page select

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
P0:0x01	CISCTL_buf_exp2_in[14:8]	7	0x00	RW	[7] NA [6:0] CISCTL_buf_exp2_in[14:8]
P0:0x02	CISCTL_buf_exp2_in [7:0]	8	0x04	RW	[7:0] CISCTL_buf_exp2_in[7:0]
P0:0x03	CISCTL_buf_exp_in [14:8]	7	0x00	RW	[7] NA [6:0] CISCTL_cur_exp_out[14:8]
P0:0x04	CISCTL_buf_exp_in [7:0]	8	0x10	RW	[7:0] CISCTL_cur_exp_out[7:0]
P0:0x05	buf_CISCTL_capt_hb[11:8]	4	0x02	RW	H Blanking
P0:0x06	buf_CISCTL_capt_hb [7:0]	8	0x20	RW	
P0:0x07	buf_CISCTL_capt_vb [12:8]	5	0x00	RW	Vertical Blanking
P0:0x08	buf_CISCTL_capt_vb [7:0]	8	0x10	RW	
P0:0x09	buf_CISCTL_capt_row_start[11:8]	8	0x00	RW	[7:4] reserved [3:0]Row Start[11:8]
P0:0x0a	buf_CISCTL_capt_row_start [7:0]	8	0x00	RW	Row Start[7:0]
P0:0x0b	buf_CISCTL_capt_col_start [11:8]	4	0x00	RW	[3:0] colstart[11:8] [7:1] colstart[7:1]
P0:0x0c	buf_CISCTL_capt_col_start [7:1]	7	0x00	RW	[0] NA
P0:0x0d	buf_CISCTL_capt_win_height[11:8]	4	0x09	RW	[7:4] NA [3:0] Window height[11:8]
P0:0x0e	buf_CISCTL_capt_win_height [7:0]	8	0xa0	RW	Window height[7:0]
P0:0x0f	buf_CISCTL_capt_win_width [11:8]	4	0x0c	RW	[7:4] NA [3:0] Window width[11:8]
P0:0x10	buf_CISCTL_capt_win_width [7:1]	7	0xd0	RW	[7:1]window width[7:1] [0] NA
P0:0x13	buf_CISCTL_vs_st	8	0x14	RW	vs_st

P0:0x14	buf_CISCTL_vs_et	8	0x01	RW	vs_et
P0:0x15	buf_CISCTL_row_head_width, buf_CISCTL_row_tail_width	8	0x00	RW	[7:2] CISCTL_row_head_width [1:0] CISCTL row tail width
P0:0x17	buf_CISCTL_mode1	8	0xc0	RW	[7:2] reserved [1]updown, [0]mirror
P0:0xb9	fsync_mode_new	8	0x13	RW	[7:2] fsync_time [1:0]2’b11: old mode 2’b10: clear_start 2’b01: clear_stop 2’b00:update_flop
P0:0xba	fsync_update_mode_new	1	0x0	RW	[0] fsync_update_mode_new
P0:0xbb	read_clock_another	3	0x01	RW	[2:0] read_clock_another

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
P3:0x01	DPHY_analog_mode1	8	0x00	RW	[7]NA [6:5] data0ctr [4:3] clkctr [2] DPHY_lane1_en [1] DPHY_lane0_en [0] DPHY_clk_en
P3:0x02	DPHY_analog_mode2	8	0x00	RW	[7]NA [6:5] data1ctr [4:3]NA [2:0] mipi_diff
P3:0x03	DPHY_analog_mode3	8	0x00	RW	[7] mipi_en [6] data1delay1s [5] data0delay1s [4] clkdelay1s [3:2] disable_set [1:0] clkhs_ph
P3:0x04	FIFO_prog_full_level[7:0]	8	0x04	RW	[7:0]FIFO_prog_full_level[7:0]

P3:0x05	FIFO_prog_full_level[11:8]	4	0x00	RW	[7:4] NA [3:0] FIFO_prog_full_level[11:8]
P3:0x06	FIFO_mode	8	0x00	RW	[7] compress [6] decompress [5] mipi write gate mode [4] fifo_rst_mode [3]bit10_switch [2]NA [1] write fifo gate [0] read fifo gate
P3:0x11	LDI_set	8	0x2b	RW	RAW10
P3:0x12	LWC_set[7:0]	8	0xf0	RW	3264x5/4 RAW10
P3:0x13	LWC_set[15:8]	8	0x0f	RW	3264x5/4 RAW10
P3:0x14	SYNC_set	8	0xb8	RW	SYNC_set
P3:0x15	DPHY_mode	8	0x10	RW	[7]NA [6]mipi para invar when div2 [5]DATA lane gate [4]all_lane_open_mode [3:2]switch_msb_mode [1:0] clklane_mode
P3:0x16	LP_set	8	0x29	RW	[7:6] hi-z [5:4]use define [3:2] 1 [1:0] 0
P3:0x17	DPHY_analog_mode7	8	0x00	RW	[7:6]data3lpfb_sel [5:4]data2lpfb_sel [3:2]data1lpfb_sel [1:0]data0lpfb_sel
P3:0x18	DPHY_analog_mode4	8	0x01	RW	[7]NA [6:5]data3ctr [4:3]data2ctr [2]dphy_data3_en [1]dphy_data2_en [0]clklane_p2s_sel
P3:0x19	DPHY_analog_mode5	8	0x00	RW	[7:6]data0hs_ph [5:4] data1hs_ph [3:2] data2hs_ph [1:0] data3hs_ph

P3:0x1a	DPHY_analog_mode6	8	0x00	RW	[7:4]mp_reserve [3]data3delay1s [2]data2delay1s [1:0]clkpfb_sel
P3:0x1b	fifo2_prog_full_level	6	0x10	RW	[5:0]fifo2_prog_full_level
P3:0x1c	fifo2_push_prog_full_level	6	0x10	RW	[5:0]fifo2_push_prog_full_level
P3:0x1d	sram_test_mode	4	0x02	RW	[3]RF1_not_split [2]RF1 cen [1]RF1 gate [0]NA sram test
P3:0x20	T_init_set	8	0x80	RW	Timing of initial setting, more than 100 us
P3:0x21	T_LPX_set	8	0x10	RW	Timing of LP setting, more than 50ns
P3:0x22	T_CLK_HS_PREPARE_set	8	0x05	RW	Timing of COCLK HS PREPARE setting, 38ns ~95ns LP00
P3:0x23	T_CLK_zero_set	8	0x30	RW	Timing of COCLK HS zero setting, more than 300ns
P3:0x24	T_CLK_PRE_set	8	0x02	RW	Timing of COCLK HS PRE of Data setting, more than 8UI
P3:0x25	T_CLK_POST_set	8	0x10	RW	Timing of COCLK HS Post of Data setting, 60ns +52UI
P3:0x26	T_CLK_TRAIL_set	8	0x08	RW	Timing of COCLK tail setting, 60ns
P3:0x27	T_HS_exit_set	8	0x10	RW	Timing of HS exit setting, more than 100ns
P3:0x28	T_wakeup_set	8	0xa0	RW	Timing of wakeup setting, 1ms
P3:0x29	T_HS_PREPARE_set	8	0x06	RW	Timing of data HS PREPARE setting, 45+4UI~85+5UI
P3:0x2a	T_HS_Zero_set	8	0x0a	RW	Timing of data HS zero setting, 140ns
P3:0x2b	T_HS_TRAIL_set	8	0x08	RW	Timing of data HS trail setting, 60ns
P3:0x30	MIPI_test	4	0x00	RW	[7:4] NA [3]Test_clk_hsvalid [2]Test_data_hsvalid [1]MIPI_Test_clk_mode [0]MIPI_Test
P3:0x31	MIPI_test_data0	8	0x96	RW	MIPI_test_data0
P3:0x32	MIPI_test_data1	8	0x3a	RW	MIPI_test_data1
P3:0x33	MIPI_test_data2	8	0x87	RW	MIPI_test_data2
P3:0x34	MIPI_test_data3	8	0xb5	RW	MIPI_test_data3

P0:0x3e	Fifo1_error_valid	4	0x00	R/W	[3]Fifo_pop_error_valid, [2]Fifo_push_error_valid, [1]Fifo1_full_valid, [0]Fifo1_error_valid
P0:0x3f	Buf_CSI2_mode	8	0x00	RW	[7]lane_ena [6]Four lane [5]ULP_mode [4]MIPI_ena [3]NA [2]RAW8 [1]line_sync_mode [0]double_lane_den

ISP Related

Address	Name	Width	Default Value	R/W	Description
P0:0x80	block_enable1_buf	8	0x00	RW	[7:6]dd_mode [5]INBF_en [4]first_dd_en [3] CDD_en [2] CDD_map [1] BFF_en [0] DPC_en
P0:0x84	cp_clk_mux	7	0x00	RW	[6] OTPCPCLK_en [5:4]cp_clk_sel 00:mclk 01:serial_clk_in 10:wpll_clk 11:rpll_clk [3:0]cp_clk_div
P0:0x8c	debug_mode2	8	0x10	RW	[7:3]reserved [2]input_test_image [1]PREGAIN_test_image, [0]OUT test_image
P0:0x90	win_mode_buf	1	0x01	RW	[7:1]NA [0]crop out win mode
P0:0x91	out_win_y1[11:8]	4	0x00	RW	[7:4] NA [3:0] Crop _win_y1[11:8]
P0:0x92	out_win_y1[7:0]	8	0x00	RW	Crop _win_y1[7:0]

P0:0x93	out_win_x1[11:8]	4	0x00	RW	[7:4] NA [3:0] Crop _win_x1[11:8]
P0:0x94	out_win_x1[7:0]	8	0x00	RW	Crop _win_x1[7:0]
P0:0x95	out_win_height[11:8]	4	0x09	RW	[7:4] NA [3:0] Out window height[11:8]
P0:0x96	out_win_height[7:0]	8	0x90	RW	Out window height[7:0]
P0:0x97	out_win_width[11:8]	4	0x0c	RW	[7:4] NA [3:0] Out window width[11:8]
P0:0x98	out_win_width[7:0]	8	0xc0	RW	Out window width[7:0]
P0:0xbc	Binning_out_mode_buf, Debug_mode7	8	0x09	RW	[7:6] binning_out_mode [5] NA [4]ANALOG_mode2_change_BLK_switch_last_one_frame_more [3]ANALOG_mode2_change_close_frame_en [2:0]ANALOG_mode2_change_close_frame_number
P0:0xc1	CTL_STOP_COUNTER	8	0x17	RW	CTL_STOP_COUNTER
P0:0xc2	Not_one_more_row_exp_th[14:8]	7	0x07	RW	[6:0] Not_one_more_row_exp_th[14:8]
P0:0xc3	Not_one_more_row_exp_th[7:0]	8	0xd0	RW	[7:0] Not_one_more_row_exp_th[7:0]
P1:0xbf	WB_offset	8	0x40	RW	WB_offset

OTP

Address	Name	Width	Default Value	R/W	Description
P0:0xbd	OTP_win_width[7:0]	8	0xc0	RW	[7:0] OTP_win_width[7:0]
P0:0xbe	OTP_win_height[11:8] OTP_win_width[11:8]	8	0x9c	RW	[7:4] OTP_win_height[11:8], [3:0] OTP_win_width[11:8]
P0:0xbf	OTP_win_height[7:0]	8	0x90	RW	[7:0] OTP_win_height[7:0]

P0:0xca	OTP_write_interval[8] OTP_addr_show ANALOG_mode8	7	0x0e	RW	[7] OTP_write_interval[8] [6] OTP_addr_show [5]NA [4:0] reserved
P0:0xd4	OTP_mode_temp	7	0x00	RW	[7:6] reserved [5:2]page sel [1:0]addr[9:8]
P0:0xd5	OTP_access_addr	8	0x00	RW	OTP_access_addr[7:0]
P0:0xd6	OTP_write_value	8	0x00	RW	OTP_write_value
P0:0xd7	OTP_read_value	8	0x00	RO	OTP_read_value

BLK

Address	Name	Width	Default Value	R/W	Description
P0:0x40	BLK_mode1	8	0x23	RW	[7:2] reserved [1] dark_current_en [0] offset_en
P0:0x45	manual_G1_odd_offset	8	0x00	RW	manual_G1_odd_offset
P0:0x46	manual_R1_odd_offset	8	0x00	RW	manual_R1_odd_offset
P0:0x47	manual_B2_odd_offset	8	0x00	RW	manual_B2_odd_offset
P0:0x48	manual_G2_odd_offset	8	0x00	RW	manual_G2_odd_offset

GLOBAL/PRE/POSTGAIN

Address	Name	Width	Default Value	R/W	Description
P0:0xb0	global_gain_buf	8	0x40	RW	Global gain
P0:0xb1	buf_auto_pregain_sync[11:8]	4	0x01	RW	[7:4] NA [3:0] Auto_pregain[11:8]
P0:0xb2	buf_auto_pregain[7:0]	8	0x00	RW	[7:0] Auto_pregain[7:0]
P0:0xb3	col_gain_en partition_mode max_col_level	6	0x2c	RW	[7:6]NA [5]col_gain_en, [4]partition_mode [3:0]max_col_level

P0:0xb4	total_gain_sync[15:8]	8	0x01	RW	total_gain[15:8]
P0:0xb5	total_gain[7:0]	8	0x00	RW	total_gain[7:0]
P0:0xb6	buf_col_code	4	0x06	RW	[7:4] NA [3:0] Col_code
P0:0xad	debug_mode6_buf	8	0x00	RW	[7]NA [6]binning_row_mode [5]binning_single_en [4]col_scaler_en [3:0]NA
P0:0xc0	Colgain_G1_offset_odd_buf[1:0] Colgain_R1_offset_odd_buf[1:0] Colgain_B2_offset_odd_buf[1:0] Colgain_G2_offset_odd_buf[1:0]	8	0x00	RW	[7:6]Colgain_G1_offset_odd[1:0] [5:4]Colgain_R1_offset_odd[1:0] [3:2]Colgain_B2_offset_odd[1:0] [1:0]Colgain_G2_offset_odd[1:0]
P0:0xc4	colgain_G1_offset_odd_buf[9:2]	8	0x00	RW	colgain_G1_offset_odd[9:2]
P0:0xc5	colgain_R1_offset_odd_buf[9:2]	8	0x00	RW	colgain_R1_offset_odd[9:2]
P0:0xc6	colgain_B2_offset_odd_buf[9:2]	8	0x00	RW	colgain_B2_offset_odd[9:2]
P0:0xc7	colgain_G2_offset_odd_buf[9:2]	8	0x00	RW	colgain_G2_offset_odd[9:2]
P1:0x84	channel_gain_G1_odd[10:3]	8	0x80	RW	G1 odd Channel gain[10:3]
P1:0x85	channel_gain_R1_odd [10:3]	8	0x80	RW	R1 odd Channel gain[10:3]
P1:0x86	channel_gain_B2_odd [10:3]	8	0x80	RW	B2 odd Channel gain[10:3]
P1:0x87	channel_gain_G2_odd [10:3]	8	0x80	RW	G2 odd Channel gain[10:3]
P1:0x88	channel_gain_G1_odd[2:0] channel_gain_R1_odd[2:0]	6	0x00	RW	[7]NA [6:4] channel_gain_G1_odd[2:0] [3]NA [2:0] channel_gain_R1_odd[2:0]

P1:0x89	channel_gain_B2_odd[2:0] channel_gain_G2_odd[2:0]	6	0x00	RW	[7]NA [6:4] channel_gain_B2_odd[2:0] [3]NA [2:0] channel_gain_G2_odd[2:0]

LSC

Address	Name	Width	Default Value	R/W	Description
P1:0xc9	LSC_RAM_CLR	4		RW	[3] CLR_OK [0] LSC_RAM_CLR
P1:0xca	LSC_ADDR	8		RW	LSC_ADDR
P1:0xcc	LSC_DATA	8		RW	LSC_DATA
P1:0xa0	lsc_test_image auto_lsc_en lsc_en	8	0x10	RW	[7:3] reserved [2]lsc_test_image [1]auto_lsc_en [0]lsc_en

STROBE

Address	Name	Width	Default Value	R/W	Description
P1:0xe0	Strobe_request (R)Strobe_ack Strobe_mode	8	0x30	RW	[7] Strobe_request, [6]W:NA;R:Strobe_ack, [5]strobe_ack_trigger sel [4]strobe_request_D en [3]strobe_whole_frame_mode [2]strobe_whole_vb_mode [1]badframe_strobe en [0]strobe en
P1:0xe1	Strobe_start_row	8	0x00	RW	Strobe_start_row
P1:0xe2	Strobe_lasts_row[7:0]	8	0x04	RW	Strobe_lasts_row[7:0]
P1:0xe3	Strobe_lasts_row[13:8]	6	0x00	RW	[5:0]Strobe_lasts_row[13:8]
P1:0xe4	Strobe_start_frame Strobe_skip_frame	8	0x30	RW	[7:4]Strobe_start_frame, [3:0]Strobe_skip_frame
P1:0xe5	Strobe_luma_th	8	0x40	RW	Strobe_luma_th

P1:0xe6	Strobe_mode2	6	0x00	RW	[5] adv_valid [4] whole 2 frame [3] out_en [2] request_neg_mode [1] env_adaptive_mode [0] request_D_mode