S5K3L8XX

1/3.06" 13M CMOS Image Sensor

Revision 0.01
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Data Sheet

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Chip Handling Guide

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When using semiconductor devices, ensure that the environment is protected against static electricity:

1. Wear antistatic clothes and use earth band.
2. All objects that are in direct contact with devices must be made up of materials that do not produce static electricity.
3. Ensure that the equipment and work table are earthed.
4. Use ionizer to remove electron charge.

Contamination

Do not use semiconductor products in an environment exposed to dust or dirt adhesion.

Temperature/Humidity

Semiconductor devices are sensitive to:

- Environment
- Temperature
- Humidity

High temperature or humidity deteriorates the characteristics of semiconductor devices. Therefore, do not store or use semiconductor devices in such conditions.

Mechanical Shock

Do not to apply excessive mechanical shock or force on semiconductor devices.

Chemical

Do not expose semiconductor devices to chemicals because exposure to chemicals leads to reactions that deteriorate the characteristics of the devices.

Light Protection

In non- Epoxy Molding Compound (EMC) package, do not expose semiconductor IC to bright light. Exposure to bright light causes malfunctioning of the devices. However, a few special products that utilize light or with security functions are exempted from this guide.

Radioactive, Cosmic and X-ray

Radioactive substances, cosmic ray, or X-ray may influence semiconductor devices. These substances or rays may cause a soft error during a device operation. Therefore, ensure to shield the semiconductor devices under environment that may be exposed to radioactive substances, cosmic ray, or X-ray.

EMS (Electromagnetic Susceptibility)

Strong electromagnetic wave or magnetic field may affect the characteristic of semiconductor devices during the operation under insufficient PCB circuit design for Electromagnetic Susceptibility (EMS).

Revision History

Revision No.	Date	Description	Author(s)
0.00	Oct. 14. 2014	• Initial draft	YB Kim
0.01	Nov. 5. 2014	• Update bonding coordinator	YB Kim
		•	

Revision Descriptions for Revision 0.00

Chapter Name	Page	Major Changes comparing with Last Version
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Register RW Access Type Conventions

Type	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
W	Write Only	The application has permission to write in the Register field.
RW	Read & Write	The application has permission to read and writes in the Register field. The application sets this field by writing 1’b1 and clears it by writing 1’b0.

Register Value Conventions

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

Reset Value Conventions

Expression	Description
0	Clears the register field
1	Sets the register field
x	Don't care condition

Warning: Some bits of control registers are driven by hardware or write operation only. As a result the indicated reset value and the read value after reset might be different.

List of Terms

Terms	Descriptions

List of Acronyms

Acronyms	Descriptions

1 Product Overview

1.1 Introduction

The S5K3L8XX is a highly integrated 13M pixel camera chip that includes a CMOS image sensor (CIS), image correction functionality and serial transmission using 4-lane MIPI. It is designed for fast yet low PWR operation, delivering full resolution capture at 30 frames per second (fps) and full field of view (16:9) FHD video at 60fps. It is fabricated by the SAMSUNG 65nm back side illumination (BSI) CMOS image sensor process developed for imaging applications to realize a high-efficiency and low-PWR photo sensor. The sensor consists of 4208 × 3120 effective pixels that meet with the 1/3.06-inch optical format.

The CIS has on-chip 10-bit ADC arrays to digitize the pixel output and on-chip Correlated Double Sampling (CDS) to drastically reduce Fixed Pattern Noise (FPN). It incorporates on-chip camera functions such as defect correction, exposure setting, white balance setting, image scaling and image data compression.

The S5K3L8XX CIS is programmable through a CCI serial interface and includes on-chip one-time programmable (OTP) none-volatile memory (NVM).

The S5K3L8XX is suitable for a low-PWR camera module with a 2.8 V/1.2 V PWR supply.

1.2 Features

- 13Mp sensor with 1/3.06"optics
- Pixel size: 1.12 μm
- Effective resolution: 4208 (H) × 3120 (V)
- Electronic rolling shutter and global reset
- Support digital video stabilization margins in main view modes
- Frame rate:
  - Capture: 13M-4:3 30 fps (3939 Mbps)
  - FHD video: 10M-16:9 30 fps (2990 Mbps) / 2.7M (16:9) 60 fps (1494 Mbps)
  - HD video: 1.5M-16:9 100 fps
  - High speed: QVGA 240 fps
- Interfaces:
  - Fine interface frequency control using additional dedicated PLL for EMI avoidance and integration flexibility.
  - MIPI CSI2 – four lanes (1.15Gbps per lane)
  - Output formats: RAW8 (using DPCM/PCM compression), RAW10
- Control interface : CCI (Camera Control Interface)
  - I2C-compatible – Two-wire serial communication circuit up to 400 kHz.
- Xenon/LED flash
- Mechanical shutter
- Dual sensor synchronize
- Line WDR (Wide Dynamic Range)
- 16 Kbit on-chip OTP memory to support defect corrections, Lens shading & chip ID.
- Analog gain x16
- Vertical and horizontal flip mode
- Continuous frame capture mode
- 2/2, 3/3, 4/4 – average/average-sub-sampling readout
- Pixel elimination readout function
- Bayer downscaler function for ratios of - x1.5, x2, x2.5, x3, ..., x8 & x1.25
- Bad pixel correction
- Lens shading
- Built-in test pattern generation
- Supply voltage: 2.8 V for analog and 2.8 V or 1.8 V for I/O, 1.2 V for digital core supply
- Operating temperature: – 30 °C to + 70 °C

1.3 Block Diagram

The S5K3L8XX is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip phase-locked loop (PLL) to generate all internal clocks from a single master input clock running between 12 MHz and 56 MHz. Output interface clocks may be generated by dedicated PLL for maximal flexibility in interface frequency and for EMI avoidance. The maximum pixel rate is 3960 Mbps at MIPI 4-lane, corresponding to the pixel rate of 396 MHz at CSI-2 RAW10.

The block diagram of the sensor is shown in *Figure 1*.

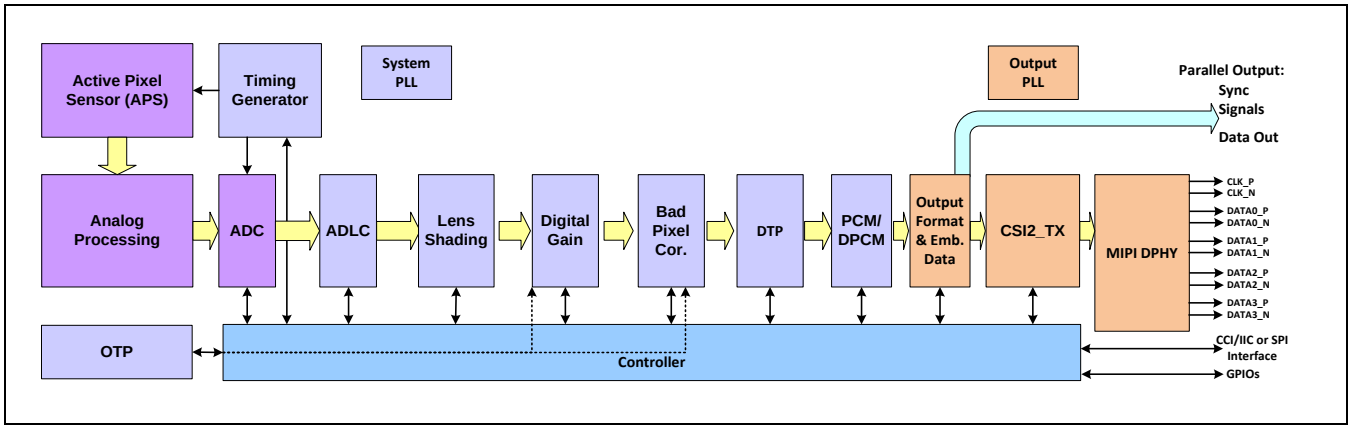

Figure 1 Function Block Diagram

The image sensor has an on-chip ADC. A column parallel ADC scheme is used for low-PWR analog processing.

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise caused by the in-pixel amplifier offset deviation. To eliminate these noise components, a Correlated Double Sampling (CDS) circuit is used before converting to digital.

The output from the ADC is a 10-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain, which provides further data path corrections and applies digital gain.

The digital processing chain performs - row noise reduction, frame black level recovery, compensation for various analog circuit variations and non-uniform pixel levels. These compensations are very flexible allowing different compensation per pixels type & exposure level.

Low PWR, bad pixel correction block is used to fix pre-defined defects that are not handled perfectly by the host ISP bad pixel correction block, such as bad pixel clusters and small level outliers. Isolated bad pixels and pixel pairs can be dynamically detected and replaced based on neighboring pixels pattern.

Next, flexible digital scaling can be performed for video or zoom modes, enabling downscaling by x1.5 to x8 in x0.5 steps.

In addition the S5K3L8XX perform & activate deterministic pattern generator, a PCM/DPCM compressor and a MIPI CSI-2 frame formatter with embedded line support.

The sensor is interfaced using a set of control and status registers that can be used to control many aspects of the sensor behavior, including frame size, exposure and gain setting. These registers can be accessed through a CCI interface.

1.4 Device Operating Modes

The Sensor module has four operating modes (*Table 1*). Moving from one mode to another is achieved by issuing the appropriate mode command via the CCI serial control interface, the RSTN (XSHUTDOWN) signal changing state and the PWR supplies. By default, S5K3L8XX PWRs up with the CSI-2 serial data interface enabled. *Figure 2* defines the valid mode changes for the sensor module.

Table 1 Operating Mode Summary

PWR State	Description
PWR-off	PWR supplies are turned off.
Hardware standby	No communication with the sensor is possible. Internal core PWR shut-off by external VDDD PWR down.
Software standby	CCI communication with sensor is possible. Core PWR is on. Entry to SW standby mode is either by mode_select or by software_reset CCI commands.
Streaming	The sensor module is fully PWRed and is streaming image data on the CSI-2 bus.

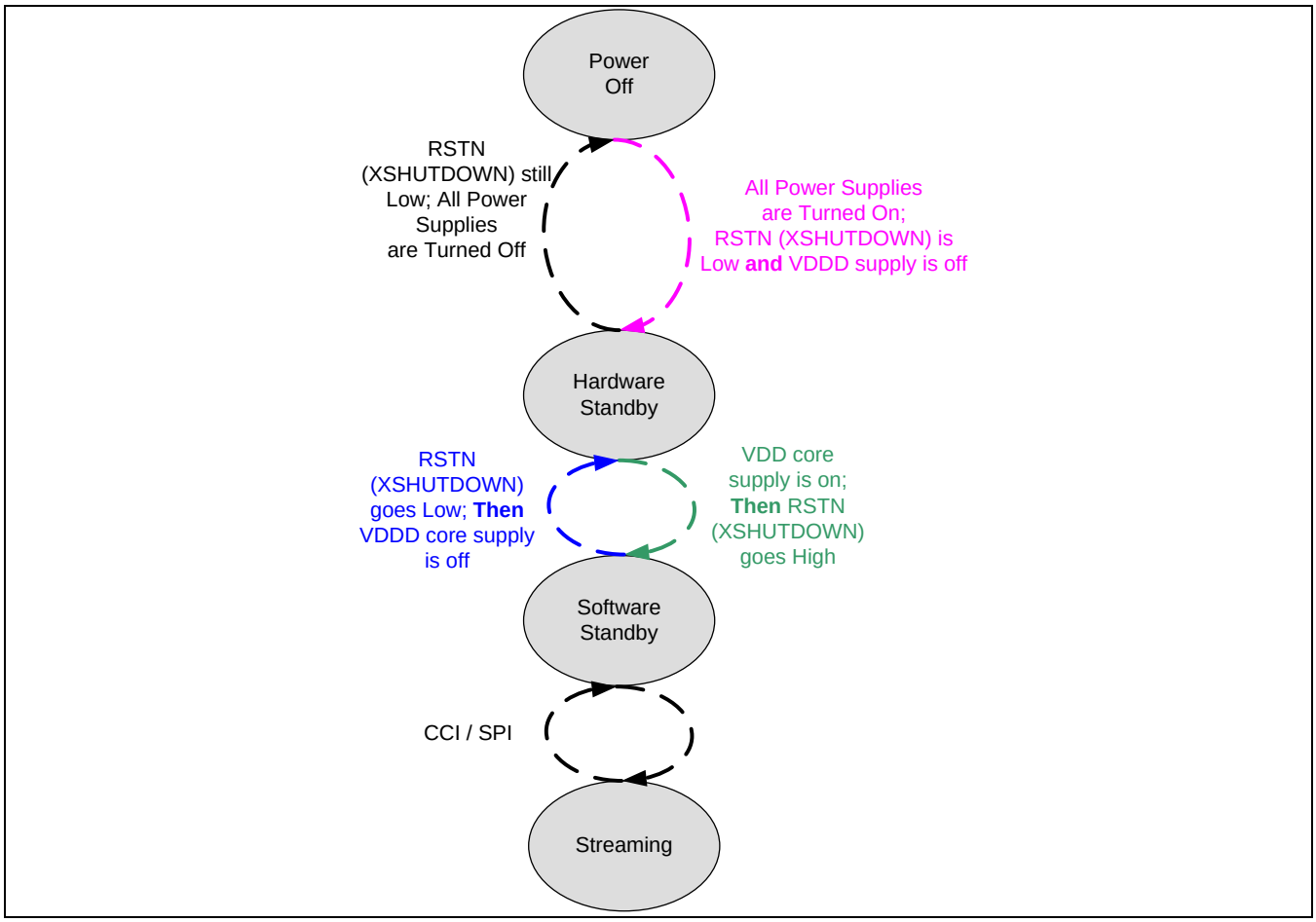

Figure 2 System State Diagram

2 Pad Configuration (Preliminary)

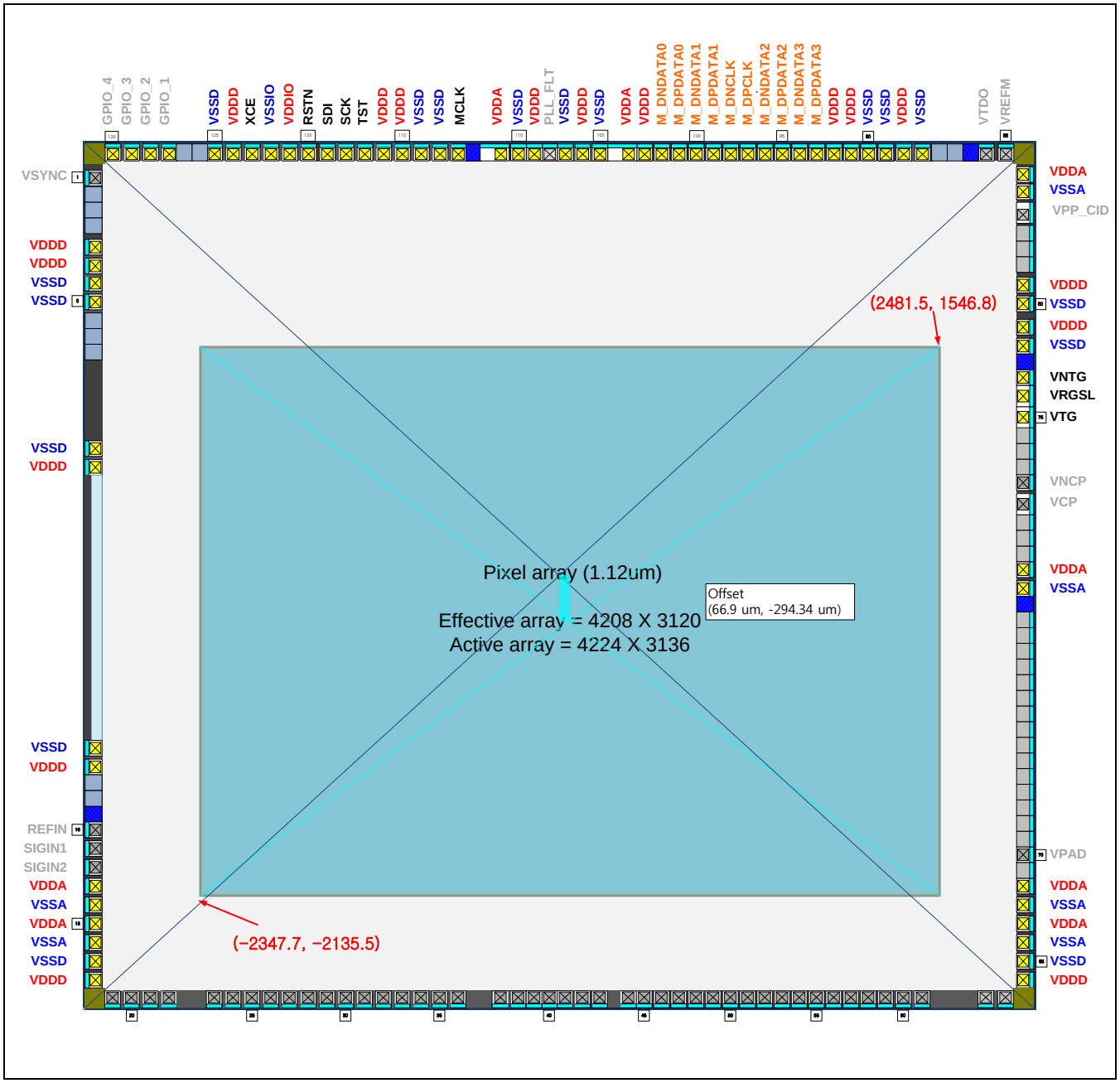

Figure 3 Pad Configuration

2.1 Pad Description (Preliminary)

Table 2 Pad Description

Pad No.	Pad Name	Type	Description
1	VSYNC	BI	Vertical Sync
2	VDDD	PWR	1.2V Digital PWR
3	VDDD	PWR	1.2V Digital PWR
4	VSSD	GND	Digital GND
5	VSSD	GND	Digital GND
6	VSSD	GND	Digital GND
7	VDDD	PWR	1.2V Digital PWR
8	VSSD	GND	Digital GND
9	VDDD	PWR	1.2V Digital PWR
10	REFIN	BI	Analog Monitoring Pad
11	SIGIN1	BI	Analog Monitoring Pad
12	SIGIN2	BI	Analog Monitoring Pad
13	VDDA	PWR	2.8V Analog PWR
14	VSSA	GND	Analog GND
15	VDDA	PWR	2.8V Analog PWR
16	VSSA	GND	Analog GND
17	VSSD	GND	Digital GND
18	VDDD	PWR	1.2V Digital PWR
19 ~ 63	NC	NC	NC pad
64	VDDD	PWR	1.2V Digital PWR
65	VSSD	GND	Digital GND
66	VSSA	GND	Analog GND
67	VDDA	PWR	2.8V Analog PWR
68	VSSA	GND	Analog GND
69	VDDA	PWR	2.8V Analog PWR

Pad No.	Pad Name	Type	Description
70	VPAD	BI	Analog Monitoring Pad
71	VSSA	GND	Analog GND
72	VDDA	PWR	2.8V Analog PWR
73	VCP	PWR	Analog Monitoring Pad
74	VNCP	GND	Analog Monitoring Pad
75	VTG	PWR	Connect to 0.2uF Cap
76	VRGSL	PWR	Connect to 0.2uF Cap
77	VNTG	GND	Connect to 2.2uF Cap
78	VSSD	GND	Digital GND
79	VDDD	PWR	1.2V Digital PWR
80	VSSD	GND	Digital GND
81	VDDD	PWR	1.2V Digital PWR
82	VPP	PWR	OTP Test Pad
83	VSSA	GND	Analog GND
84	VDDA	PWR	2.8V Analog PWR
85	VREFM	BI	OTP Test pad
86	VTDO	BI	OTP Test pad
87	VSSD	GND	Digital GND
88	VDDD	PWR	1.2V Digital PWR
89	VSSD	GND	MIPI Digital GND
90	VSSD	GND	MIPI Digital GND
91	VDDD	PWR	1.2V MIPI Digital/IO PWR
92	VDDD	PWR	1.2V MIPI Digital/IO PWR
93	M_DPDATA3	BI	Serial Data Output 3 - positive
94	M_DNDATA3	BI	Serial Data Output 3 - negative
95	M_DPDATA2	BI	Serial Data Output 2 - positive
96	M_DNDATA2	BI	Serial Data Output 2 - negative

Pad No.	Pad Name	Type	Description
97	M_DPCLK	BI	Serial Clock Output - positive
98	M_DNCLK	BI	Serial Clock Output - negative
99	M_DPDATA1	BI	Serial Data Output 1 - positive
100	M_DNDATA1	BI	Serial Data Output 1 - negative
101	M_DPDATA0	BI	Serial Data Output 0 - positive
102	M_DNDATA0	BI	Serial Data Output 0 - negative
103	VDDD	PWR	1.2V MIPI Digital/IO PWR
104	VDDA	PWR	2.8V MIPI Analog PWR
105	VSSD	GND	MIPI Digital GND
106	VDDD	PWR	1.2V Digital PWR
107	VSSD	GND	Digital GND
108	PLL_FLT	BI	PLL monitoring
109	VDDD	PWR	1.2V PLL Digital PWR
110	VSSD	GND	PLL Digital GND
111	VDDA	PWR	2.8V PLL Analog PWR
112	MCLK	I	External Input Clock
113	VSSD	GND	Digital GND
114	VSSD	GND	Digital GND
115	VDDD	PWR	1.2V Digital PWR
116	VDDD	PWR	1.2V Digital PWR
117	TST	BI	EDS test configuration pin. Tie low in normal operation
118	SCK	BI	Serial communication clock input
119	SDI	BI	CCI data
120	RSTN	I	Master Reset, Active low (XSHUTDOWN)
121	VDDIO	PWR	1.8, 2.8V I/O PWR
122	VSSIO	GND	1.8, 2.8V I/O GND

Pad No.	Pad Name	Type	Description
123	XCE	BI	CCI slave address selection (0: 20h/21h 1: 5Ah/5Bh)
124	VDDD	PWR	1.2V Digital PWR
125	VSSD	GND	Digital GND
126	GPIO_1	BI	General In/Out 1
127	GPIO_2	BI	General In/Out 2
128	GPIO_3	BI	General In/Out 3
129	GPIO_4	BI	General In/Out 4, VSYCN_IN

3 Pixel Array Information

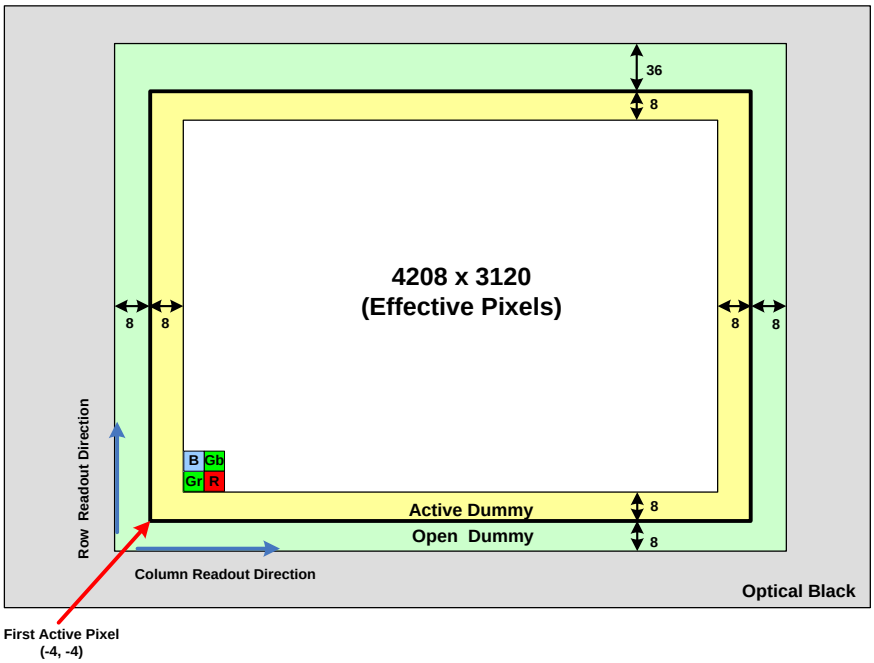

Figure 4 Pixel Array Information

NOTE: Top view on chip.
Displayed image will be flipped.

4 Functional Operation Modes

S5K3L8XX can support a wide range of operation modes.

Operation mode is function of several mode parameters such as:

- Interface bandwidth
- Requested sensor output size and sensor operation mode
- CIS output size and number of bits per pixel e.g. RAW10, RAW8+ (8 bit in DPCM/PCM compression)
- Required Vertical blank time
- PWR consumption limitations e.g. use single PLL, limited MIPI lanes, system lower PWR modes.

Typical operation modes and related typical settings are presented in this table.

Table 3 Typical Functional Operation Modes

Mode	Frame Rate	Horizontal FOV loss	CIS Output		Output Parameters			Sensor Output						MIPI Parameters	
			Output Width	Output Height	Vblank [uS]	Output Bittage	Bit Clk [Mhz]	WOI Width	H Analog Scale	H Dig Scale	WOI Height	V Analog Scale	V Dig Scale	Num. Lanes	Cont. Clk
13.1M 4:3 30FPS	30.06	0%	4208	3120	1005	10	1125	4208	1	1	3120	1	1	4	Yes
13.1M 4:3 30FPS 8bit	30.04	0%	4208	3120	1252	8	940	4208	1	1	3120	1	1	4	Yes
13.1M 3:4 26FPS	26.04	0%	4208	3120	1353	10	970	4208	1	1	3120	1	1	4	Yes
13.1M 3:4 24FPS	24.04	0%	4208	3120	3431	10	940	4208	1	1	3120	1	1	4	Yes
10M 16:9 (D.I.S)	34.11	0%	4208	2368	267	10	940	4208	1	1	2368	1	1	4	Yes
10M 16:9 (D.I.S)	30.04	0%	4208	2368	3043	10	900	4208	1	1	2368	1	1	4	Yes
2.7M 16:9 (D.I.S)	62.00	0%	2104	1183	1035	10	900	4208	2	1	1183	2	1	2	Yes
FHD (No D.I.S)	66.02	9%	1920	1080	1319	10	800	3840	2	1	1080	2	1	2	Yes
HD (D.I.S)	115.04	0%	1400	790	366	10	800	4200	1	3	790	3	1	2	Yes
HD (No D.I.S)	120.10	9%	1280	720	998	10	800	3840	1	3	720	4	1	2	Yes
VGA	180.27	9%	640	480	377	10	800	3840	2	3	480	6	1	1	Yes
QVGA	300.45	9%	320	240	601	10	800	3840	4	3	240	12	1	1	Yes

5 Video Timing

5.1 Overview

The output image size is a function of the size of the addressed region of the pixel array and the sub-sampling programmed factor. *Figure 5* shows the video timing overview.

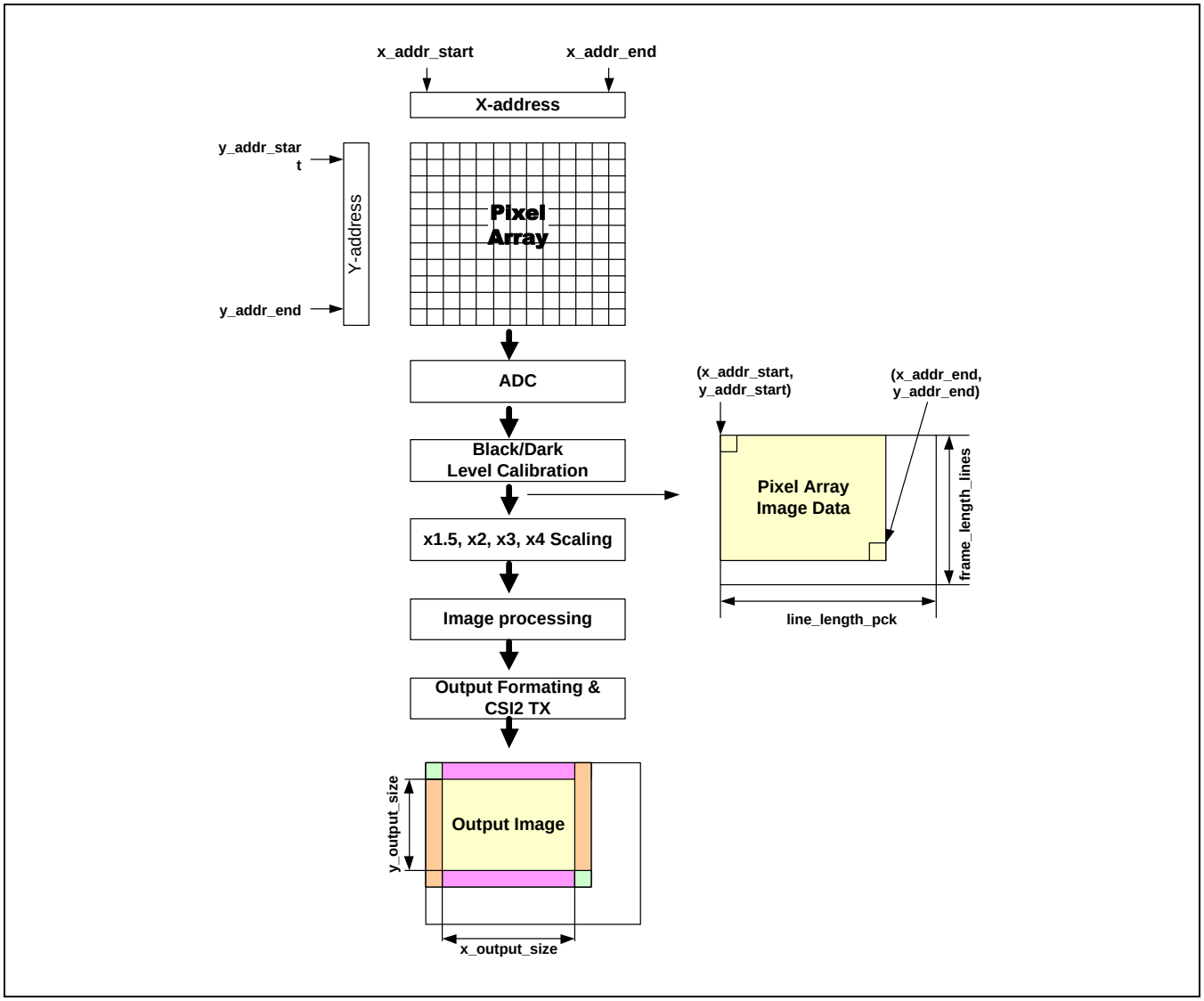

Figure 5 Video Timing Overview

5.2 Pixel Array Addresses

Addressable pixel array is defined as the pixel address range to be read. The addressable pixel array can be assigned anywhere on the pixel array. The addressed region of the pixel array is controlled by the h_addr_start, v_addr_start, h_addr_end and v_addr_end register.

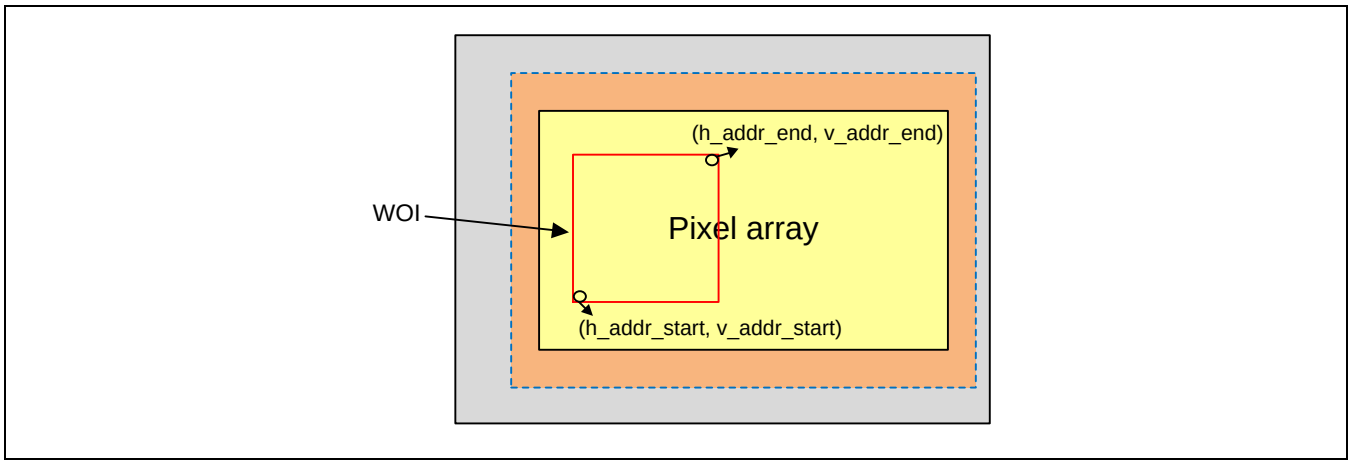

Figure 6 Window of Interest on Pixel Array

5.3 Horizontal Mirror and Vertical Flip

The pixel data is normally read out from left to right in the horizontal direction and from top to bottom in the vertical direction. By changing the mirror/flip mode, the read-out sequence can be reversed, and the resulting image can be flipped like a mirror image. Pixel data is then read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. The horizontal mirror and the vertical flip mode can be programmed by the image orientation register.

The sensor module supports four possible pixel readout orders, as described in the sections below:

a) Standard Readout
The addressed region of the horizontal pixel data output is controlled by the x_addr_start and x_output_width registers. The addressed region of the vertical pixel data output is controlled by the y_addr_start and y_output_depth registers.

b) Horizontally Mirrored Readout
The addressed region of the horizontal pixel data output is controlled by the x_addr_end, and x_output_width registers, and the vertical pixel data output is the same as that of the standard readout.

c) Vertical Flipped Readout
The horizontal pixel data output is same as that of the standard readout, and the addressed region of the vertical pixel data output is controlled by the y_addr_end and y_output_depth registers.

d) Horizontally Mirrored and Vertically Flipped Readout
The addressed region of the horizontal pixel data output is controlled by the x_addr_end and x_output_width registers. The addressed region of the vertical pixel data output is controlled by the y_addr_end and y_output_depth registers.

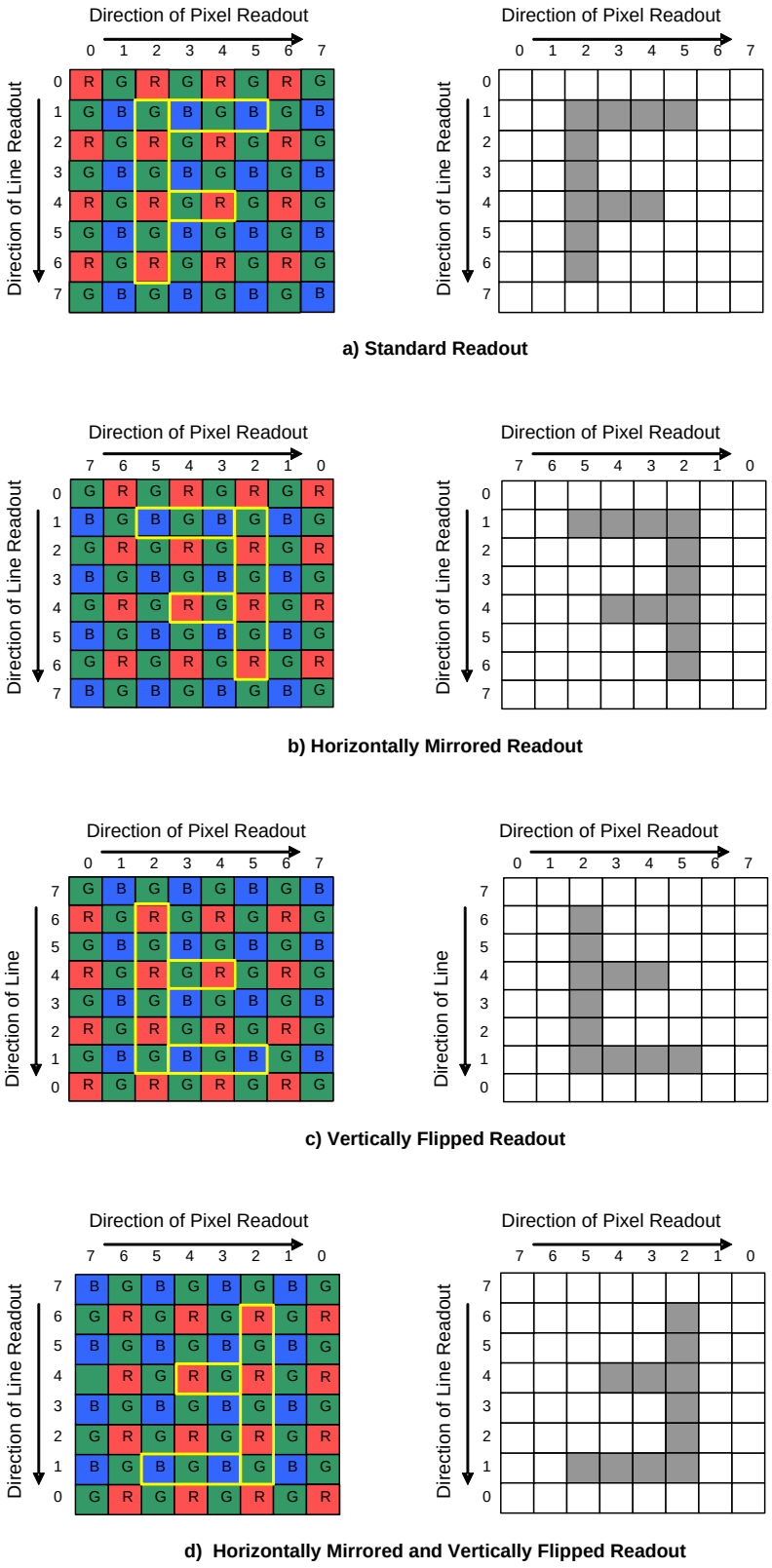

Figure 7 Horizontal Mirror and Vertical Flip

5.4 Sub-Sampled Readout

By programming the x and y odd and even increment registers (x_even_inc, x_odd_inc, y_even_inc, y_odd_inc), the sensor can be configured to read out sub-sampled pixel data.

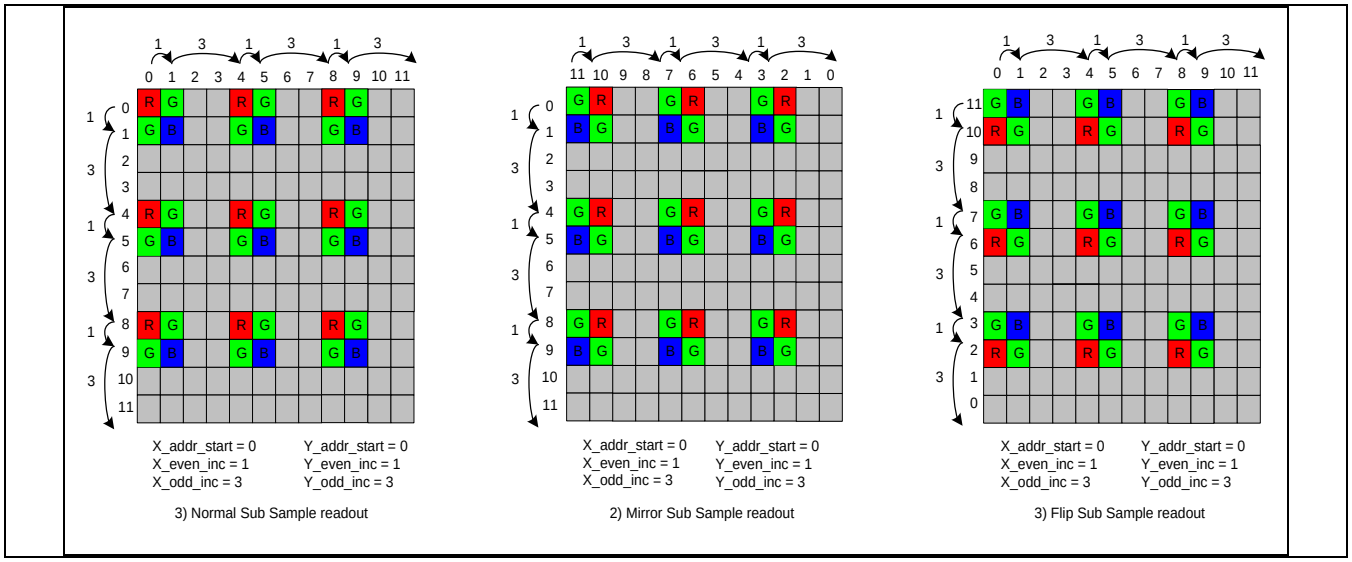

Figure 8 Example of Sub-Sampled Readout

5.4.1 Averaged Sub-Sampled Readout

By programming the averaged sub-sampling enable register, the sensor can be configured to read out pixel data that has been averaged with adjacent pixels.

5.5 Frame Rate Control (Virtual Frame)

The line rate and the frame rate can be changed by varying the size of the virtual frame. The virtual frame's width and depth are controlled by the line_length_pck and frame_length_lines register. The horizontal and vertical blanking times (horizontal blanking time: line_length_pck-x_output_size, vertical blanking time: frame_length_lines-y_output_size) should meet system requirements.

Frame rate = vt_pix_clk/(frame_length_lines × line_length_pck)

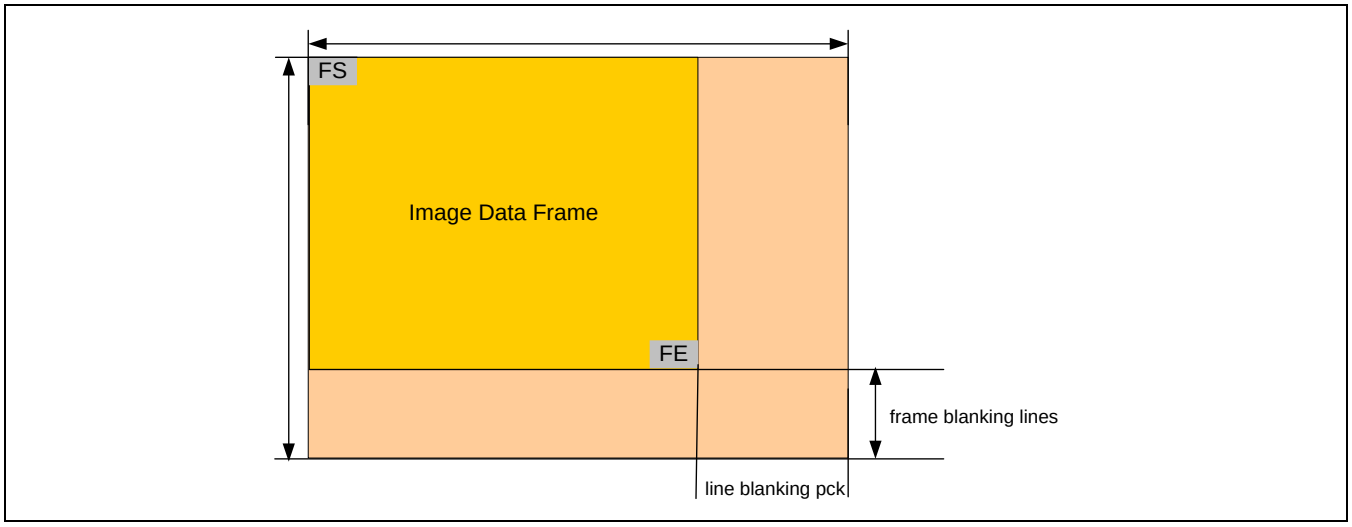

Figure 9 Virtual Frame Format Example

5.5.1 Integration Time Control (Electronic Shutter Control)

The pixel integration time is controlled by the shutter operation. During the shutter operation, the amount of time-integration time-is determined by the column Step Integration Time Control Register (fine_integration_time) and the line Step Integration Time Control Register (coarse_integration_time). The total integration time of the sensor module can be calculated using the following formula:

Total_integration_time = {coarse_integration_time × line_length_pck + fine_integration_time + const} × pclk period[sec]

const parameter is calculated internally according to sensor settings and is fixed per sensor configuration. Const parameter can be checked for any configuration by read of reg_gtg_aig_tx_ptr1 register (0xF470).

5.6 PLL and Clock Generator

The S5K3L8XX clock system uses system phase-locked loop (PLL), system clock dividers, output PLL, and output clock dividers to generate all internal clocks from a single master input clock running between 12 MHz and 56MHz.

Output interface clocks may be generated by the System PLL. In this case the Output PLL will be PWRed-down and overall system PWR reduced.

Alternatively dedicated Output PLL may be used for maximal flexibility in interface frequency and for EMI avoidance. The maximum System PLL VCO frequency is 1 GHz and Output PLL VCO frequency is 1.15 GHz

Clock dividers are used to generate all system clocks from one or two PLL sources.

The charge pump clock and the ADC clock are used for A/D conversion circuits, pixel clock and pixel clock/2 are used for pixel processing and sensor control. Bit clock and output clock are set according to the required output rate.

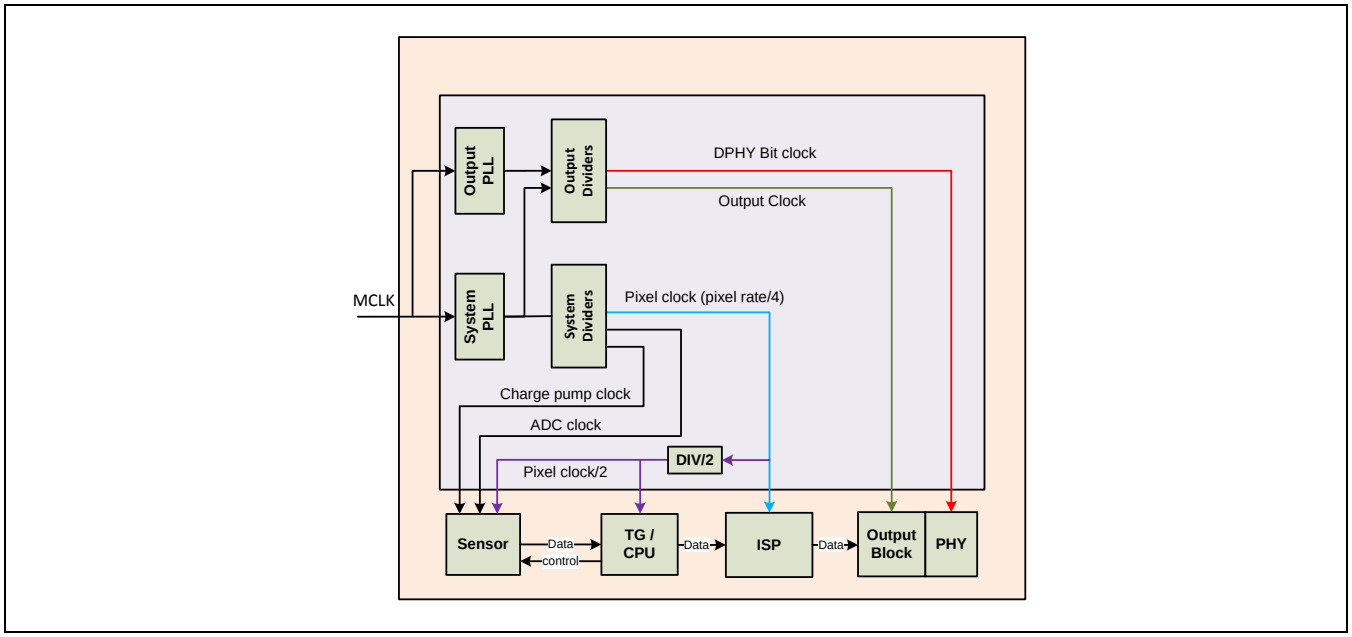

Figure 10 Clock System Block Diagram

5.6.1 Clock Relationships

The host provides the external input clock (with values varying between 12-56 MHz) in addition to setting dividers and multipliers in order to get the required video timing and output pixel clocks.

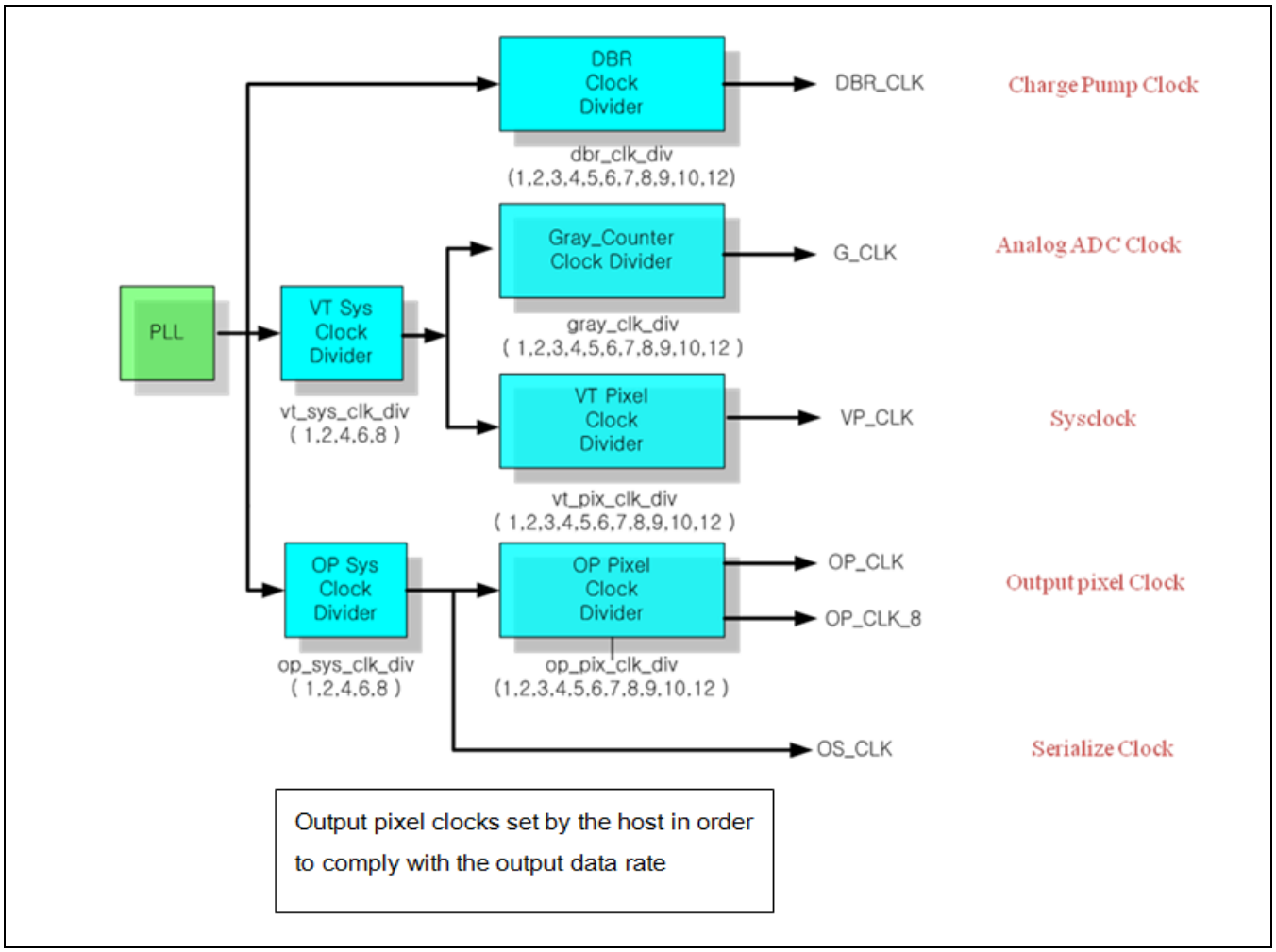

Figure 11 Clock Relationships

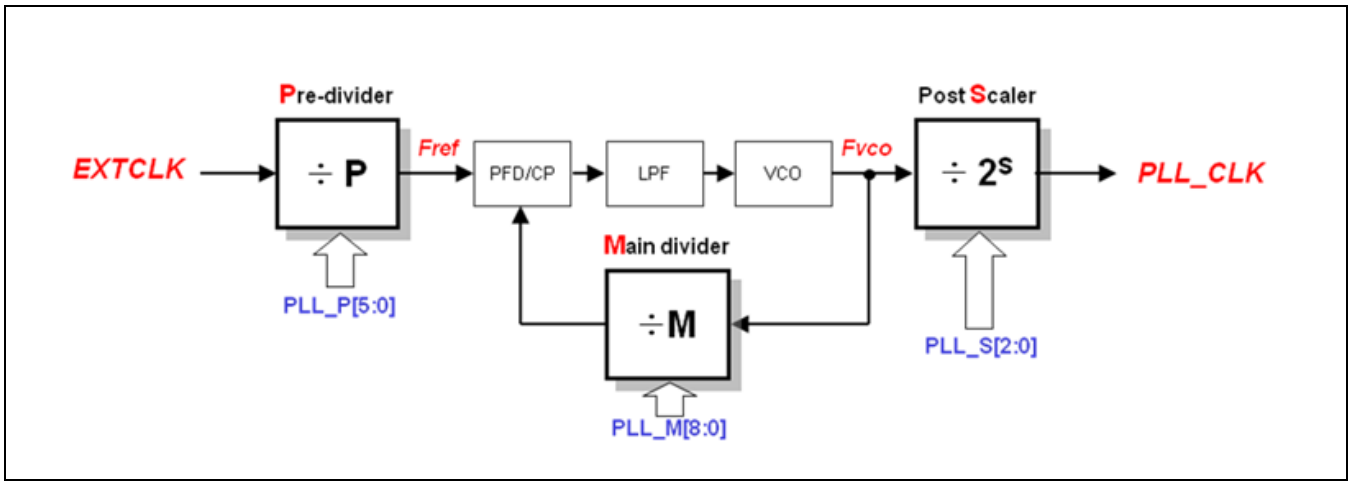

Figure 12 PLL Frequency Synthesis

$$PLL\_CLK = EXTCLK \times \left[\frac{M}{P} \times \frac{1}{2^S}\right]$$

NOTE: PLL_S = 0 and is not controllable. Post dividers are used for lower frequency synthesis.

Table 4 PLL Component Output Frequency

Parameter	Min.	Typ.	Max.	Unit	Remarks
Input frequency range	12	–	56	MHz	EXTCLK frequency range
Reference frequency range	2.5	–	5	MHz	Output of pre-divider (Fref)
System PLL VCO frequency range	500	–	1000	MHz	Output of System PLL multiplier VCO oscillation range (Fvco)
System PLL output frequency range	31.25	–	1000	MHz	Output of System PLL post scaler. Minimum value is just for test. (S ≥ 4)
Output VCO frequency range	500	–	1150	MHz	Output of Output PLL multiplier VCO oscillation range (Fvco)
Output PLL output frequency range	31.25	–	1150	MHz	Output of Output PLL post scaler. Minimum value is just for test. (S ≥ 4)

NOTE: 1. For high frame rates as 13M 30 FPS, MIPI-DPHY PLL may be configured to 1.15 GHz

NOTE: 2. For more information about the PLL and clock system control, refer to the application note.

5.6.2 Master Clock Waveform Diagram

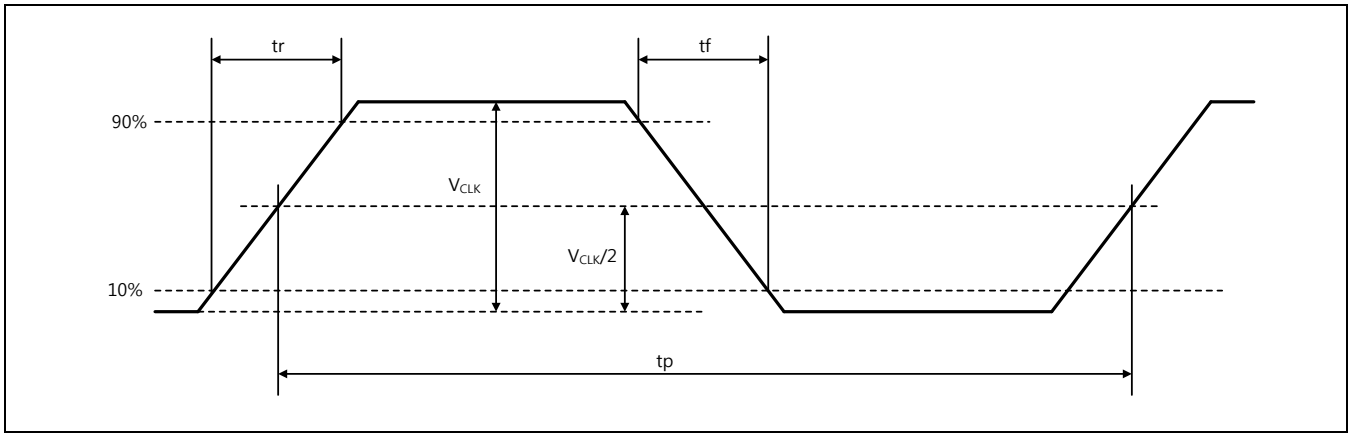

Figure 13 Master Clock Waveform Diagram

MCLK is the input clock to the S5K3L8XX sensor, sometimes refer as EXTCLK.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
MCLK clock frequency	EXTCLK	12	–	56	MHz	–
MCLK period	tp	17.86	41.6	166.6	ns	–
MCLK rise/fall time	tr/tf	–	–	8		–
MCLK jitter (periodic)	Tjitter	–	–	200	ps	–
MCLK jitter (peak-to-peak)	–	–	–	0.1 V_{CLK}	V	–

6 Control Interface

S5K3L8XX control is done using register writes.

S5K3L8XX can be controlled using the Camera Control Interface (CCI) control interface.

Table 5 CCI PAD

	CCI
SDI	SDA
SCK	SCL
XCE	I2C_ID
	–

6.1 Camera Control Interface (CCI)

S5K3L8XX supports the Camera Control Interface (CCI), which is an I2C fast-mode compatible interface for controlling the transmitter. S5K3L8XX always acts as a slave in the CCI bus. CCI is capable of handling several slaves in the bus, but multi-master mode is not supported. Typically, only the receiver and transmitter are connected to the CCI bus. This makes a pure SW implementation possible.

Typically the CCI is separate from the system I2C bus, but I2C-compatibility ensures that it is also possible to connect the transmitter to the system I2C bus. CCI is a subset of the I2C protocol, including the minimum combination of obligatory features for the I2C slave device specified in the I2C specification. Therefore, transmitters complying with the CCI specification can also be connected to the system I2C bus. However, it is important to ensure that the I2C masters do not try to utilize these I2C features, which are not supported in transmitters complying with the CCI specification. Each transmitter conformed to the CCI specification may have additional features implemented to support I2C.

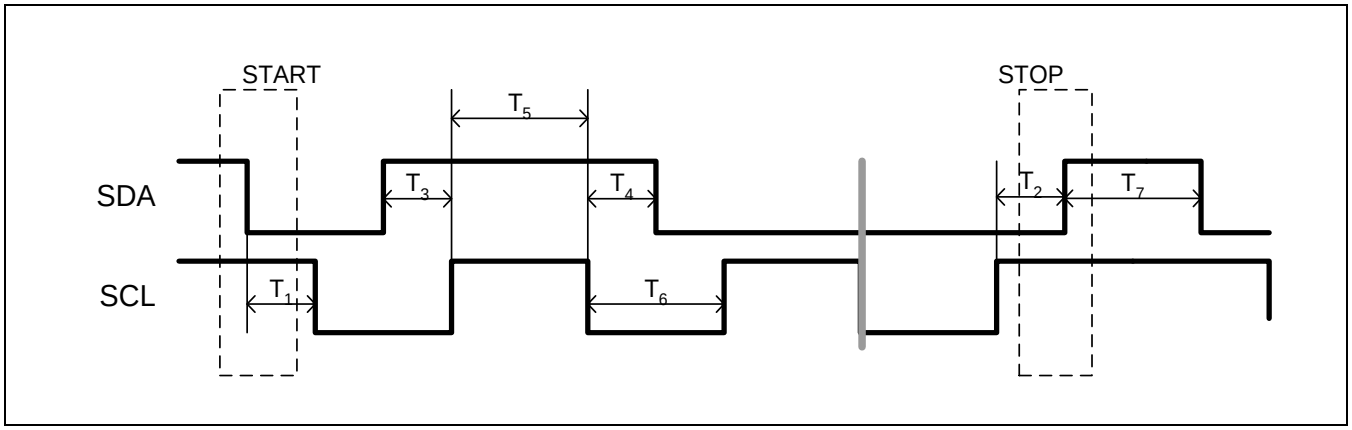

Figure 14 I2C Timing

Table 6 I2C Standard Mode Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	100	kHz
Hold time for START condition	T_1	4.0	–	µs
Setup time for STOP condition	T_2	4.0	–	
Data setup time	T_3	250	–	ns
Data hold time	T_4	0	3.45	µs
High period of the SCL clock	T_5	4.0	–	
Low period of the SCL clock	T_6	4.7	–	
Bus free time between STOP and START conditions	T_7	4.7	–	
Rise time for both SDA and SCL signals	–	–	1000	ns
Fall time for both SDA and SCL signals	–	–	300	
Capacitive load for each bus line	CB	–	400	pF

Table 7 I2C Fast Mode Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	400	kHz
Hold time for start condition	T_1	0.6	–	µs
Setup time for stop condition	T_2	0.6	–	
Data setup time, external clock (MCLK) above 12.8MHz	T_3	0.1	–	µs
Data setup time, external clock (MCLK) below 12.8MHz		0.6	–	
Data hold time	T_4	0	0.9	µs
High period of the SCL clock	T_5	0.6	–	
Low period of the SCL clock	T_6	1.3	–	
Bus free time between stop and start conditions	T_7	1.3	–	
Rise time for both SDA and SCL signals	–	–	300	ns
Fall time for both SDA and SCL signals	–	–	300	
Capacitive load for each bus line	CB	–	400	pF

NOTE: Fast mode can be supported with above-12.8 MHz external clock (MCLK).

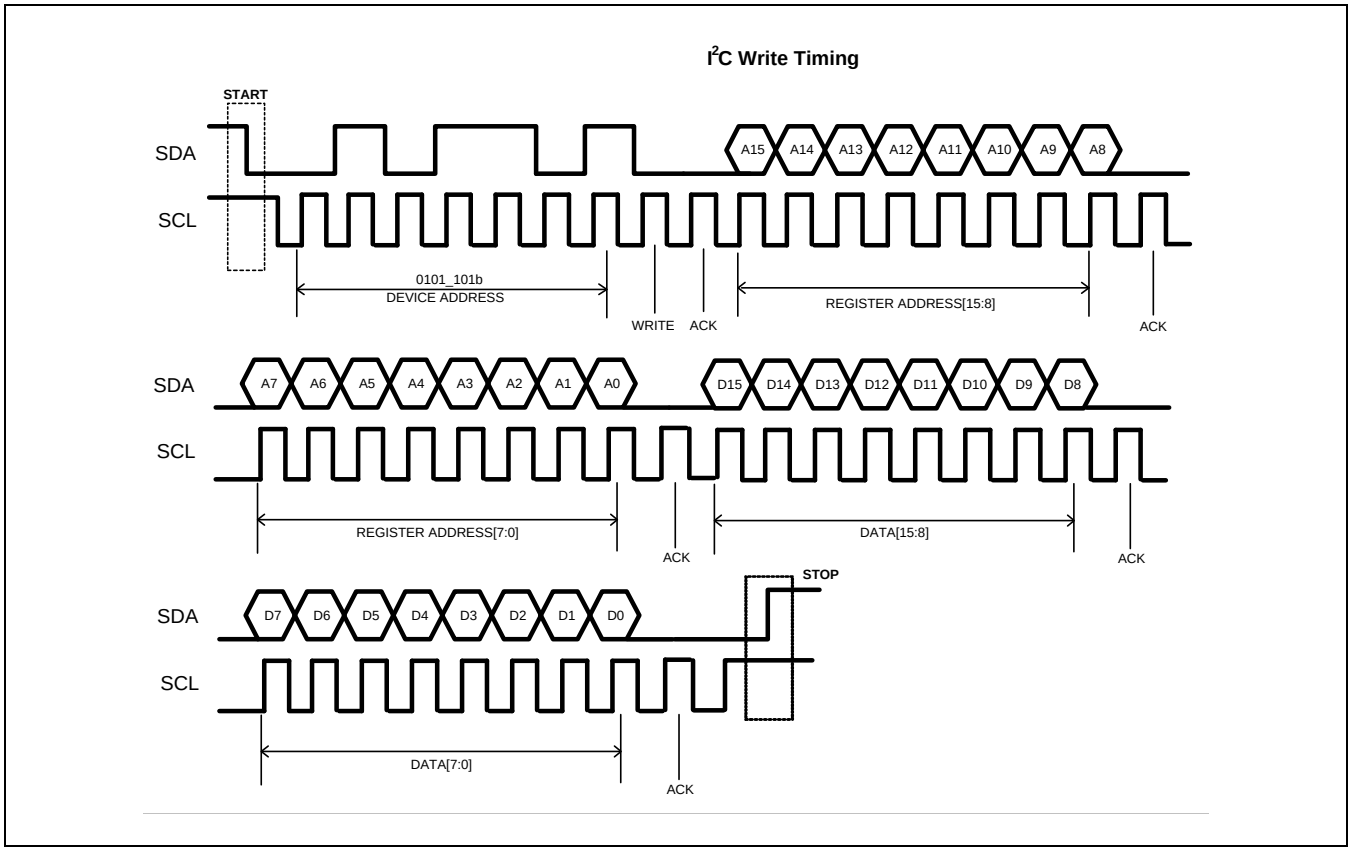

Figure 15 I2C Write Timing Example

NOTE: The device address can be changed by pin configuration of I2C_ID, as described in the pad description.

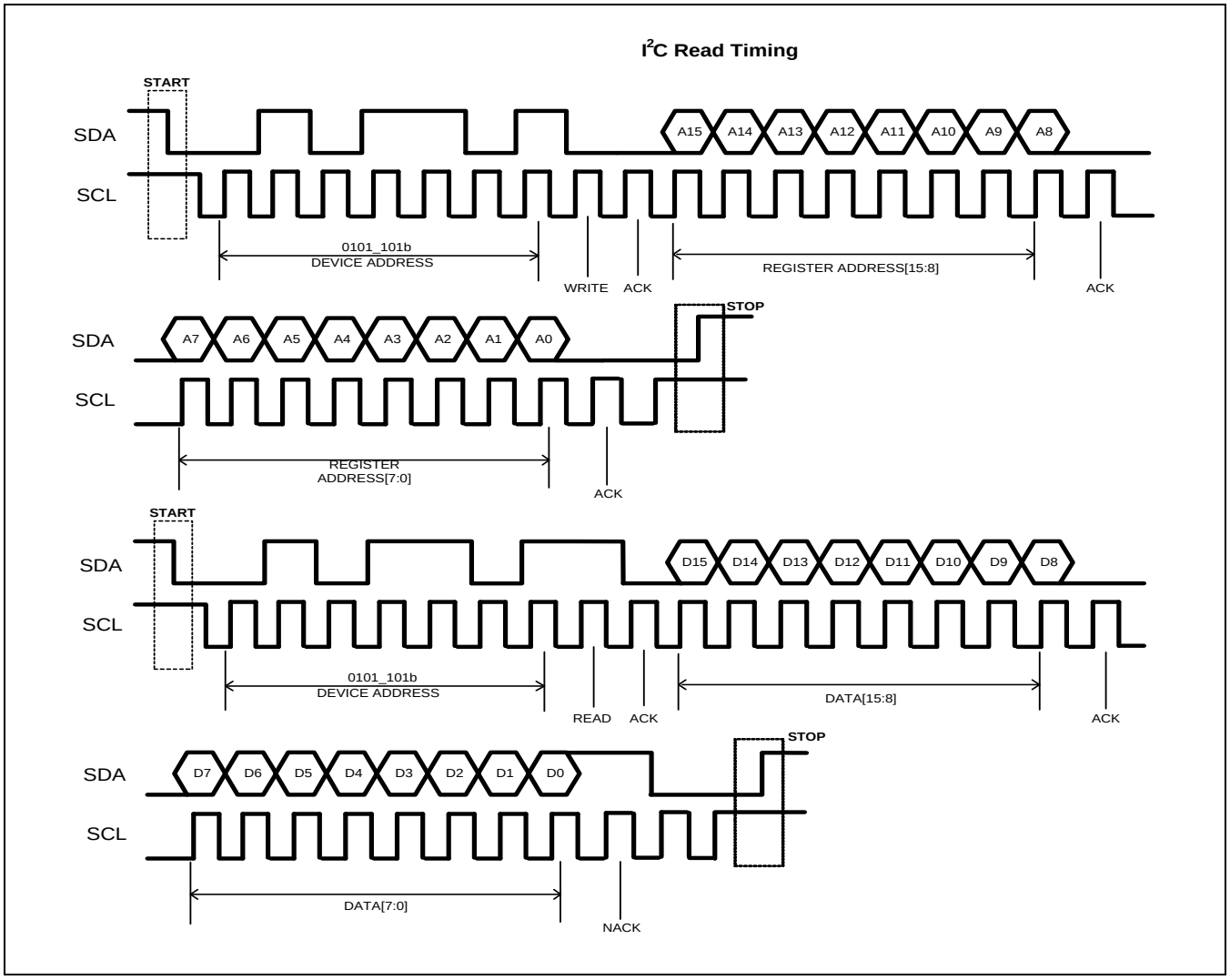

Figure 16 I2C Read Timing Example

NOTE: The device address can be changed by the pin configuration of I2C_ID, as described in the pad description.

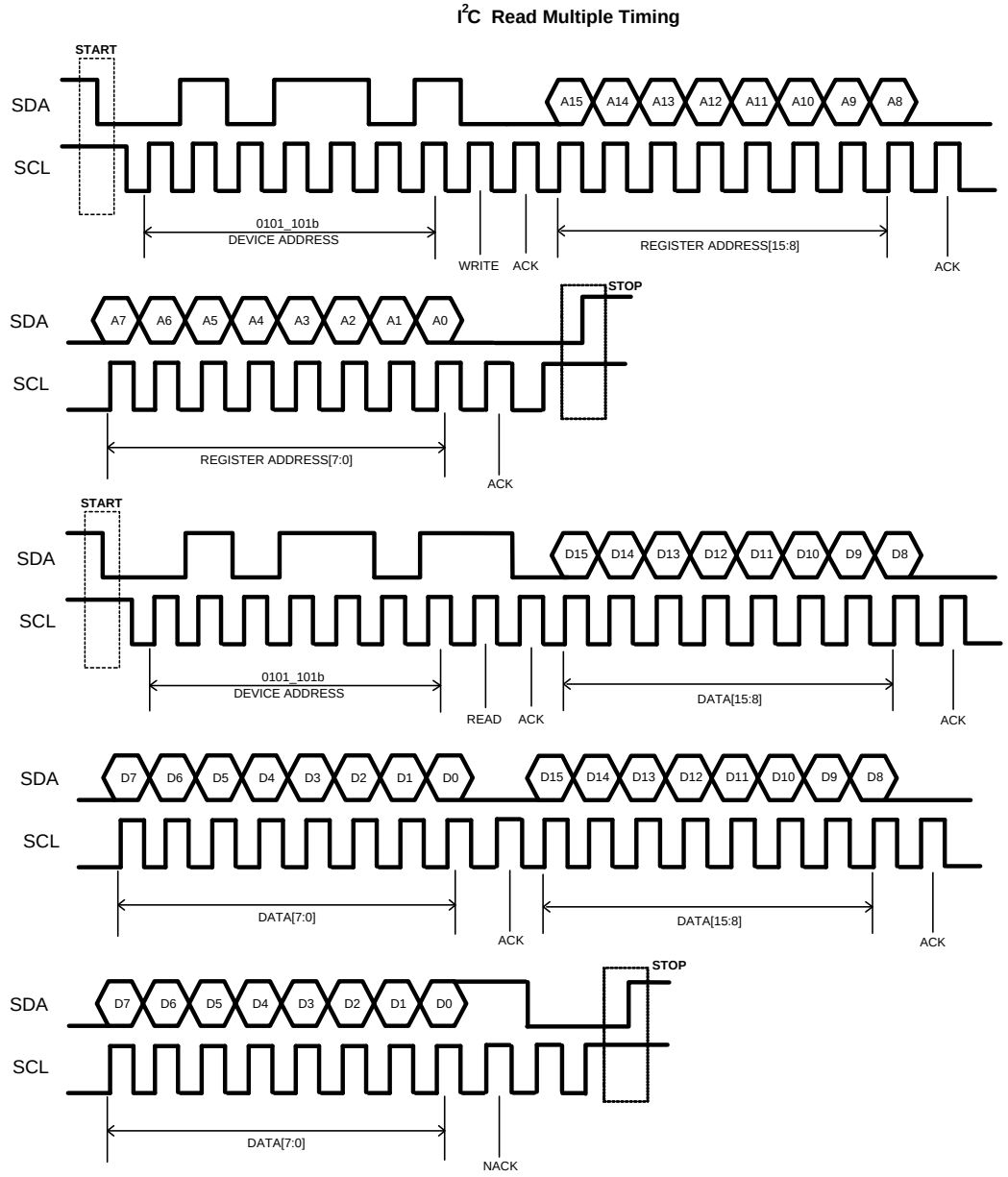

Figure 17 I2C Read Multiple Timing Example

NOTE: The device address can be changed by the pin configuration of I2C_ID, as described in the pad description.

It is possible to configure up to two I2C slave addresses using I2C_ID pins.

Table 8 I2C ID Address (XCE Pad)

XCE	Slave Address (7-bit + Read Mode)	Slave Address (7-bit + Write Mode)	Comment
0	0010_0001b/21h	0010_0000b/20h	Address 1
1	0101_1011b/5Bh	0101_1010b/5Ah	Address 2

7 PWR Up/Down Sequence

7.1 PWR-Up Sequence

The digital and analog supply voltages can be PWRed up in any order, e.g., VDDD/VDDIO then VDDA/VPIX or VDDA/VPIX/VDDIO then VDDD.

On PWR up, RSTN (XSHUTDOWN) should be low when the PWR supplies are brought up, then the sensor module will go into hardware standby mode. As long as RSTN is low and VDDD is down, the sensor module stays in hardware standby mode.

The assertion of RSTN ensures that the CCI register values are initialized correctly to their default values.

When RSTN will go 'high', all PADs will exit from FAIL-SAFE mode, and switch to Normal operating mode.

The MCLK clock can either be initially low and then enabled during software standby mode or MCLK can be a free running clock.

NOTE:

1. At hardware standby mode external VDDD should be OFF.
2. For minimal SW standby PWR external clock (MCLK) should be off
3. S5K3L8XX does not support PWR gating in stand by mode. For minimal PWR consumption it is necessary to PWR down externally in standby mode.

Table 9 PWR-Up Sequence Timing Constraints (Serial Output Case)

Constant	Label	Min.	Max.	Unit
VDDA/VPIX/VDDD/VDDIO rising time	t0	VDDA/VPIX/VDDD/VDDIO may rise in any order. The rising separation can vary from 0ns to indefinite.		ns
VDDD rising to RSTN (XSHUTDOWN) rising	t2	0.0		ns
RSTN (XSHUTDOWN) rising to first CCI transaction	t3	10	–	us
Minimum No. of MCLK (EXTCLK) cycles prior to the first CCI transaction	t4	23,000 (1),(2)	–	MCLK cycles
PLL startup/lock time	t5	–	1	ms
Entering streaming mode-first frame start sequence (fixed part)	t6	–	10	
Entering streaming mode-first frame start sequence (variable part)	t7	The delay is the coarse integration time value		lines
DPHY recovery time (TWAKEUP)	t8	1	–	ms
DPHY initialization period (TINIT)	t9	0.1	–	

NOTE:

1. In case that set-file is loaded from NVM t4 may increase (depending on the set-file size). Yet, in this case Device configuration time is decreased
2. In case that first CCI command is SW reset, 100 MCLK cycles are required from valid MCLK until issuing SW reset command & t4 period is required until the successive CCI command can be issued

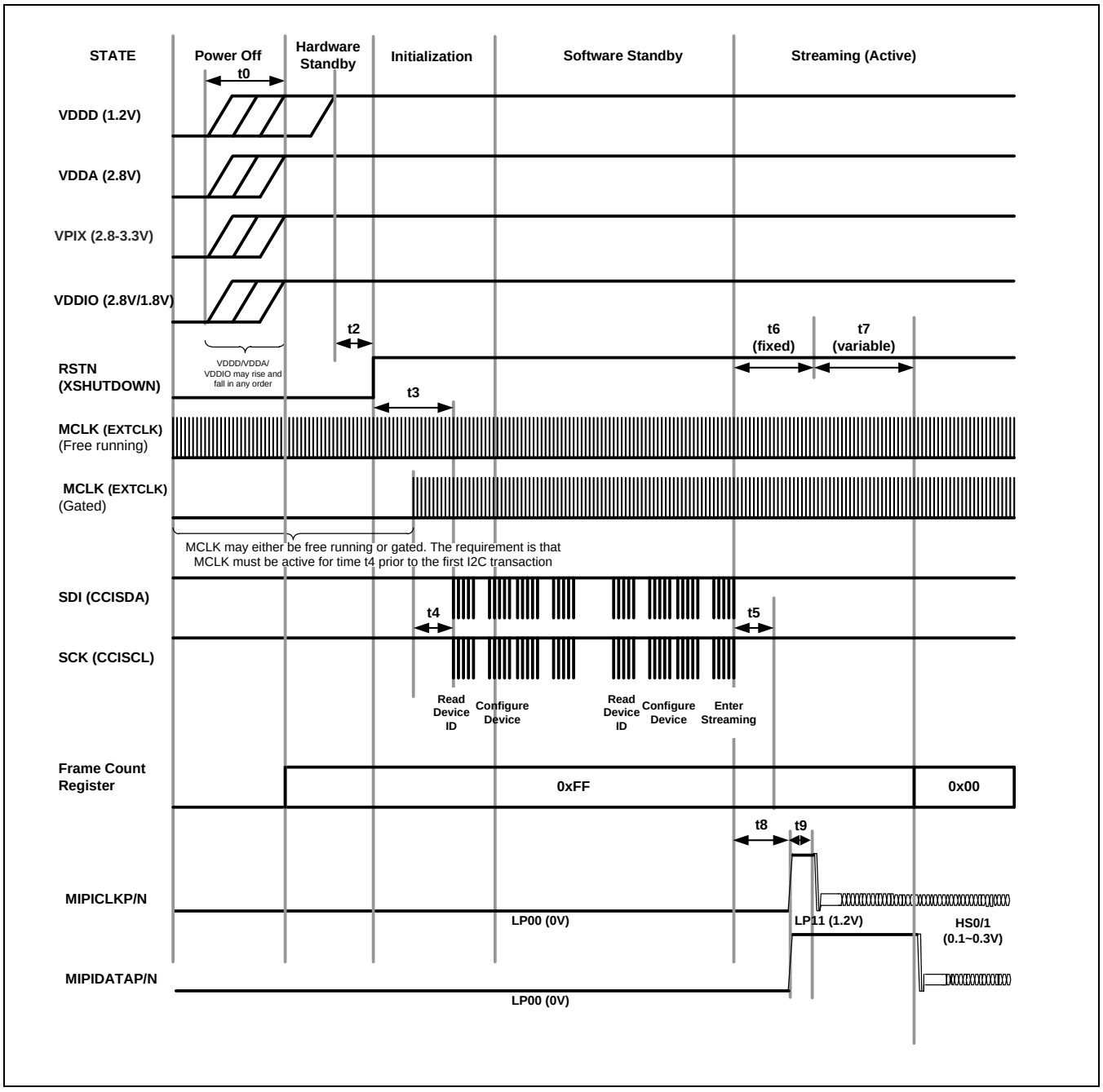

Figure 18 PWR-Up Sequence (Serial Output Case)

7.2 PWR-Down Sequence

The digital and analog supply voltages can be PWRed down in any order, e.g., VDDD/VDDIO then VDDA/VPIX or VDDA/VPIX/VDDIO then VDDD.

Similar to the PWR-up sequence, the MCLK (EXTCLK): input clock may be either gated or continuous.

If the CCI command to exit streaming is received while a frame of valid active data is being output, then the sensor module must wait for the frame end code before entering software standby mode. Frame end code may come either after all frame pixels were transmitted or during the frame when next line transmission is completed - based on a configuration register (Refer to S5K3L8XX application notes for details)

If the CCI command to exit streaming mode is received during the inter frame time, then the sensor module must enter software standby mode immediately.

Table 10 PWR-Down Sequence Timing Constraints (Serial Output Case)

Constant	Label	Min.	Max.	Unit
Enter Software Standby CCI command-Device in Software Standby mode	t0	If outputting a frame of MIPI, the data waits for the MIPI frame end code before entering software standby; otherwise enter software standby mode immediately.		–
Minimum number of MCLK (EXTCLK) cycles after the last CCI transaction or MIPI frame end code.	t1	512	–	MCLK cycles
Last I2C Transaction or MIPI frame end code-RSTN (XSHUTDOWN) falling	t2	512	–	
RSTN (XSHUTDOWN) falling to VDDD falling	t3	0.0	RSTN falling and VDDD falling can be in any order	ns
VDDD falling to RSTN (XSHUTDOWN) falling	t4	0.0		
VDDA/VPIX/VDDD/VDDIO falling time	t5	VDDA/VDDD/VDDIO may fall in any order. The rising separation can vary from 0 ns to indefinite		

NOTE: For minimal PWR at hardware standby mode external VDDD should be OFF.

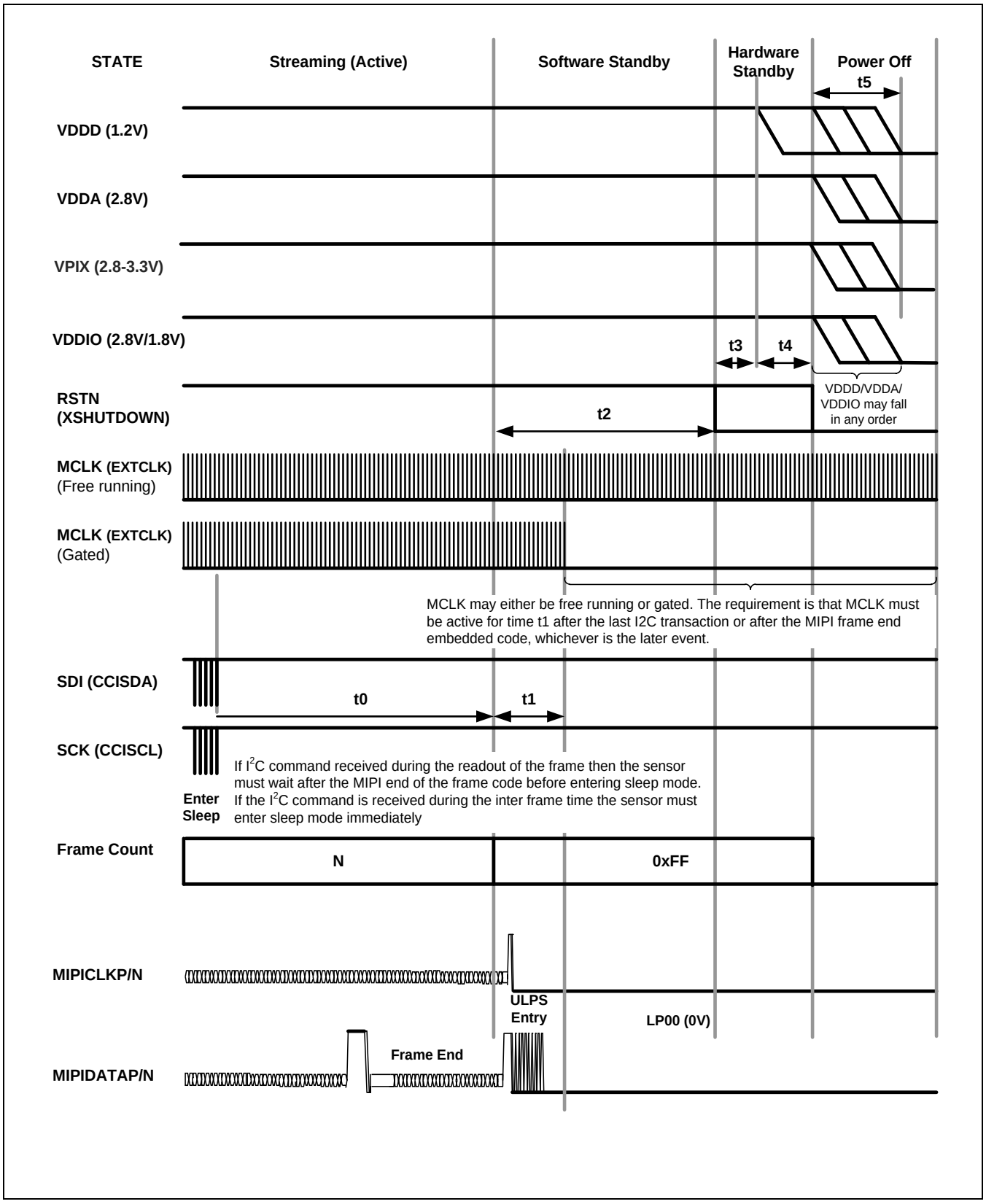

Figure 19 PWR-Down Sequence (Serial Output Case)

7.3 Software Standby Mode Sequence

Entering software standby mode is the same as entering hardware standby mode but without RSTN (XSHUTDOWN) assertion to low and without applying external VDDD PWR down.

There are several options to define how the last frame before entering the Software Reset is handled, according to the following parameter.

Table 11 Abort Frame Timing Transition Options upon entering SW Reset

Timing Transition Type	Setting
abort_timing_on_sw_stby	0 = Abort timing Immediately, even during read out. 1 = Abort timing after read out ends 2 = Abort timing on end of frame.

7.4 WDR Mode for System PWR-Up

The S5K3L8XX include WDR mode which is useful for shortening system PWR-Up period.

In this mode, the S5K3L8XX can be programmed upon PWR-up with settings for 2 different exposure types for the first 2 frames. This allows using 2 different image types thus reaching faster convergences of the required exposure level in the system. This is performed using the parameters - use_2nd_frame_settings.

The S5K3L8XX support also “immediate” mode, allowing changing exposure level on the immediate successive frame (refer to section 8.1).

8 Functional Features

8.1 Frame Timing Control

When sensor frame timing configuration change is requested by host (Refer to section 8.1.1.3 *Settings Affecting Frame Timing*) by register setting with "group parameter hold" request, S5K3L8XX firmware detects the change and forces frame timing change in one of the following options:

a) Preserve frame timing without outputting the corrupted frame to host (skip frame)

b) Preserve frame timing and output corrupted frame

c) Timing abort: After end of readout including VBLANK period.

d) Timing abort: After frame readout ends but before VBLANK period.

e) Timing abort: Immediate abort (including during frame read out).

Frame timing examples may be found in the following figures;

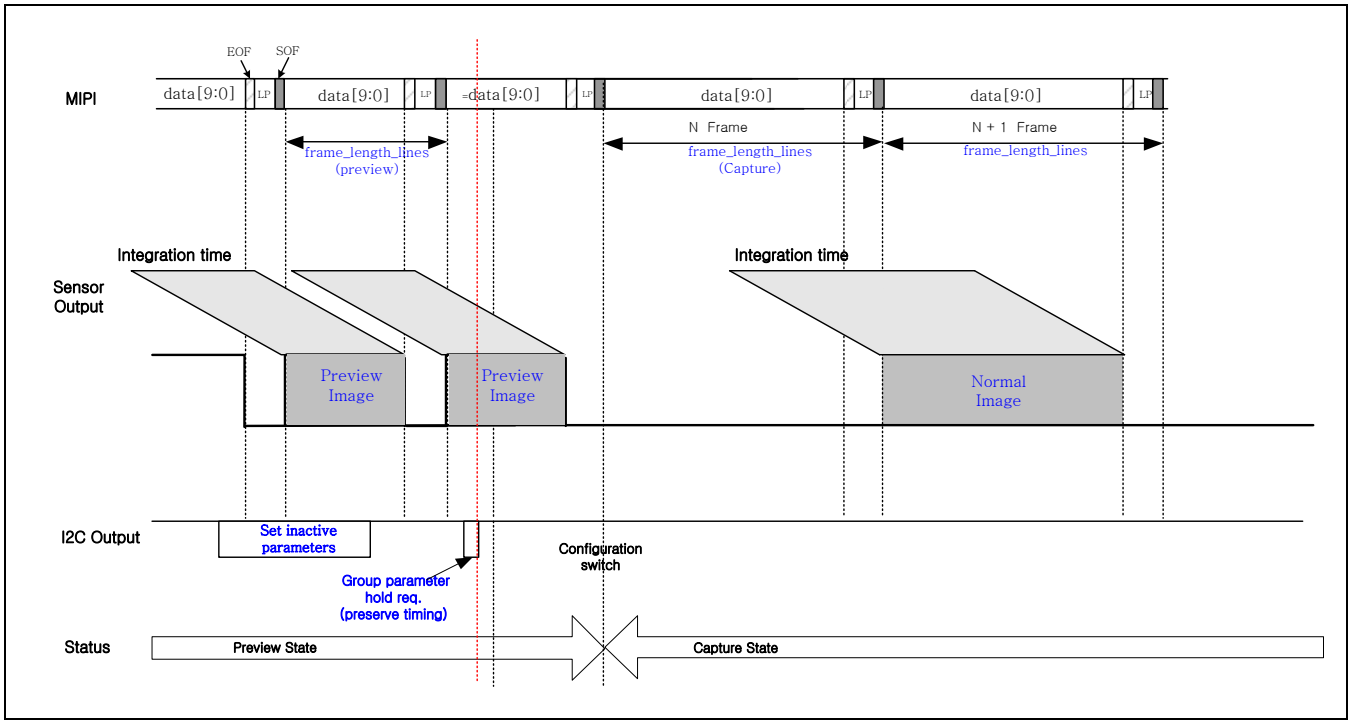

Figure 20 Example-Case (a); Preserve Frame Timing Without Outputting the Corrupted Frame to Host

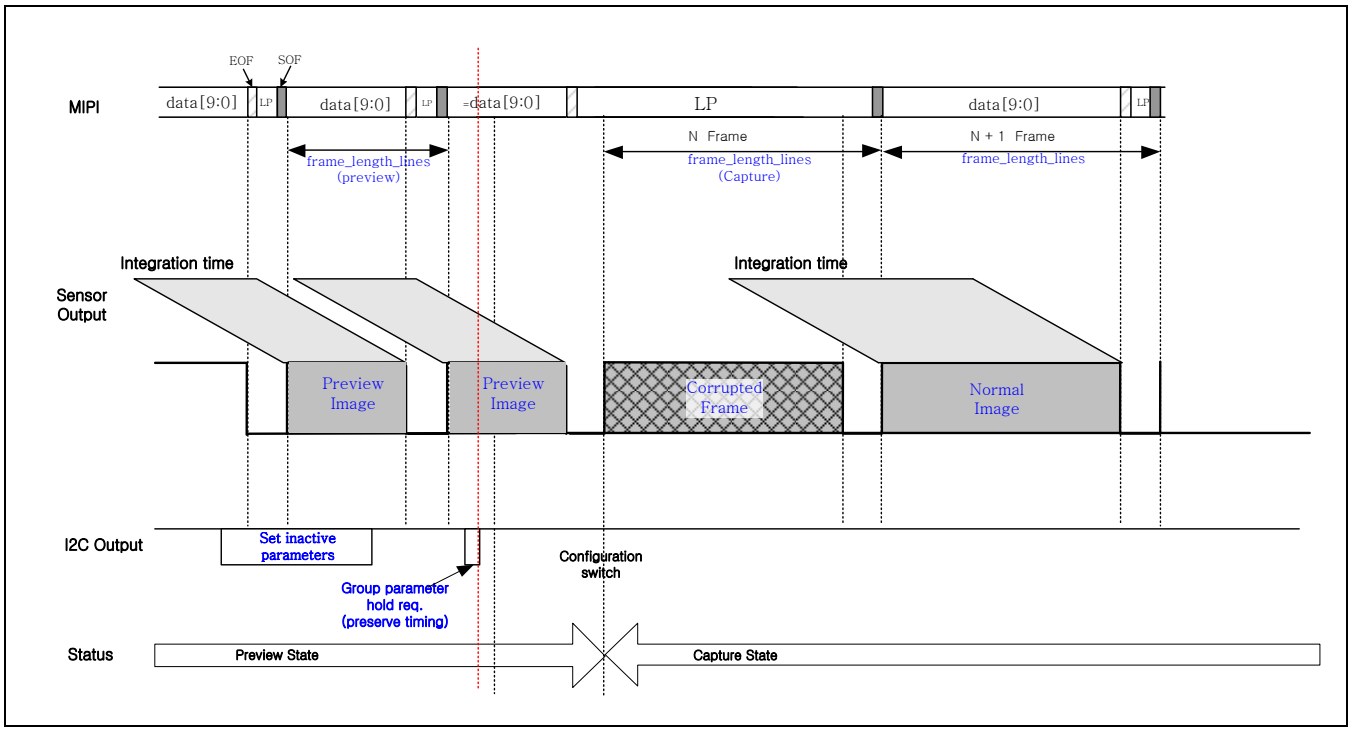

Figure 21 Example-Case (b); Preserve Frame Timing and Output Corrupted Frame

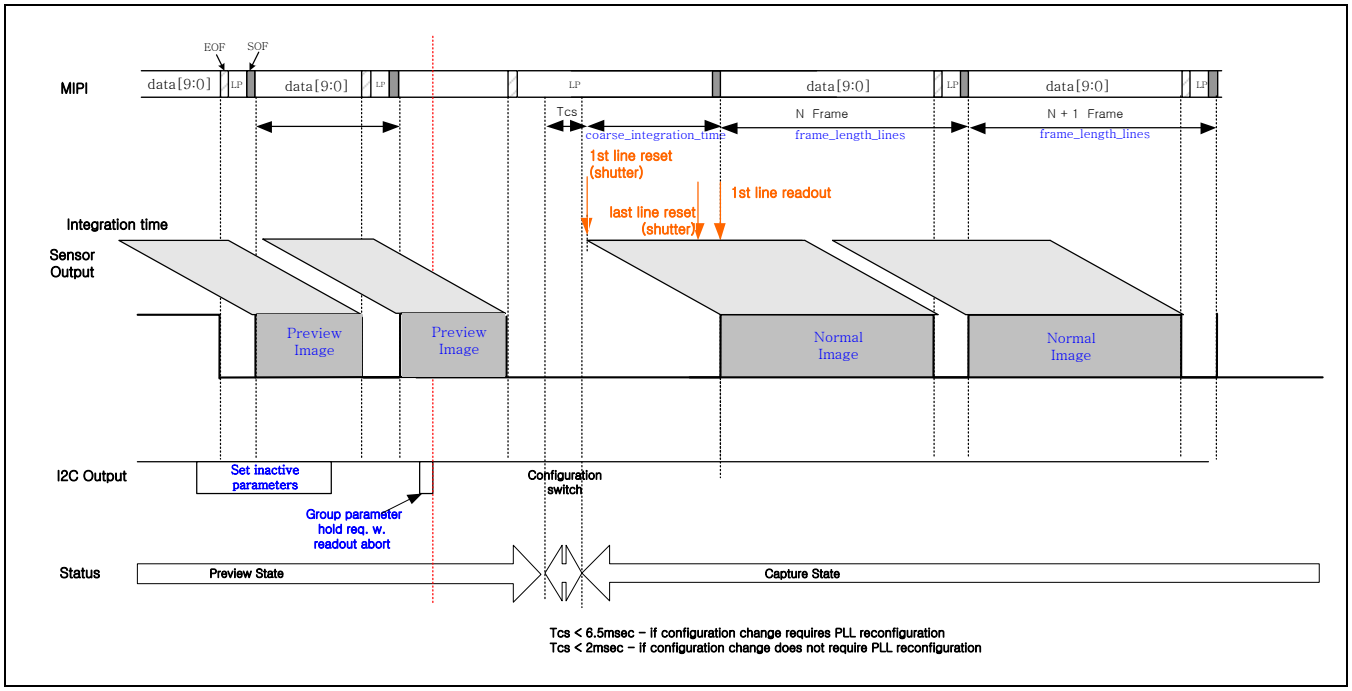

Figure 22 Example-Case (c); Timing abort: After End of Readout and VBLANK

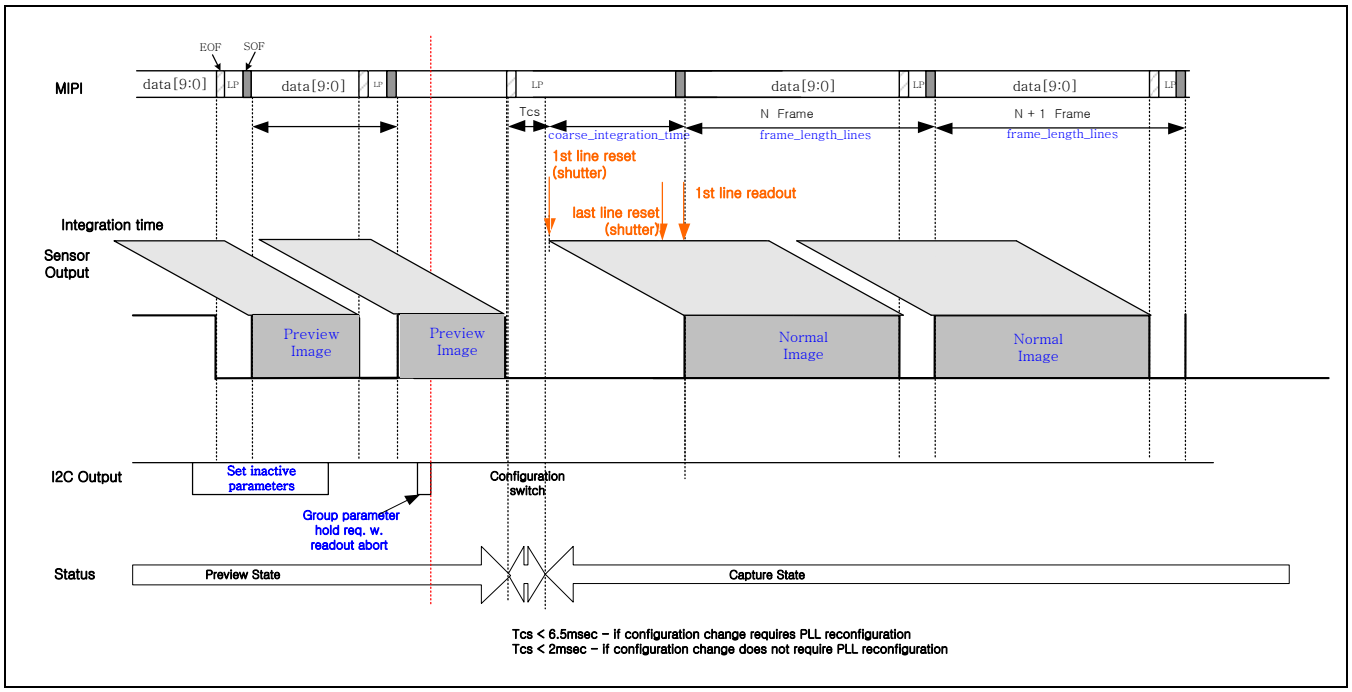

Figure 23 Example-Case (d); Timing abort: After Frame Readout Ends But Before VBLANK Time

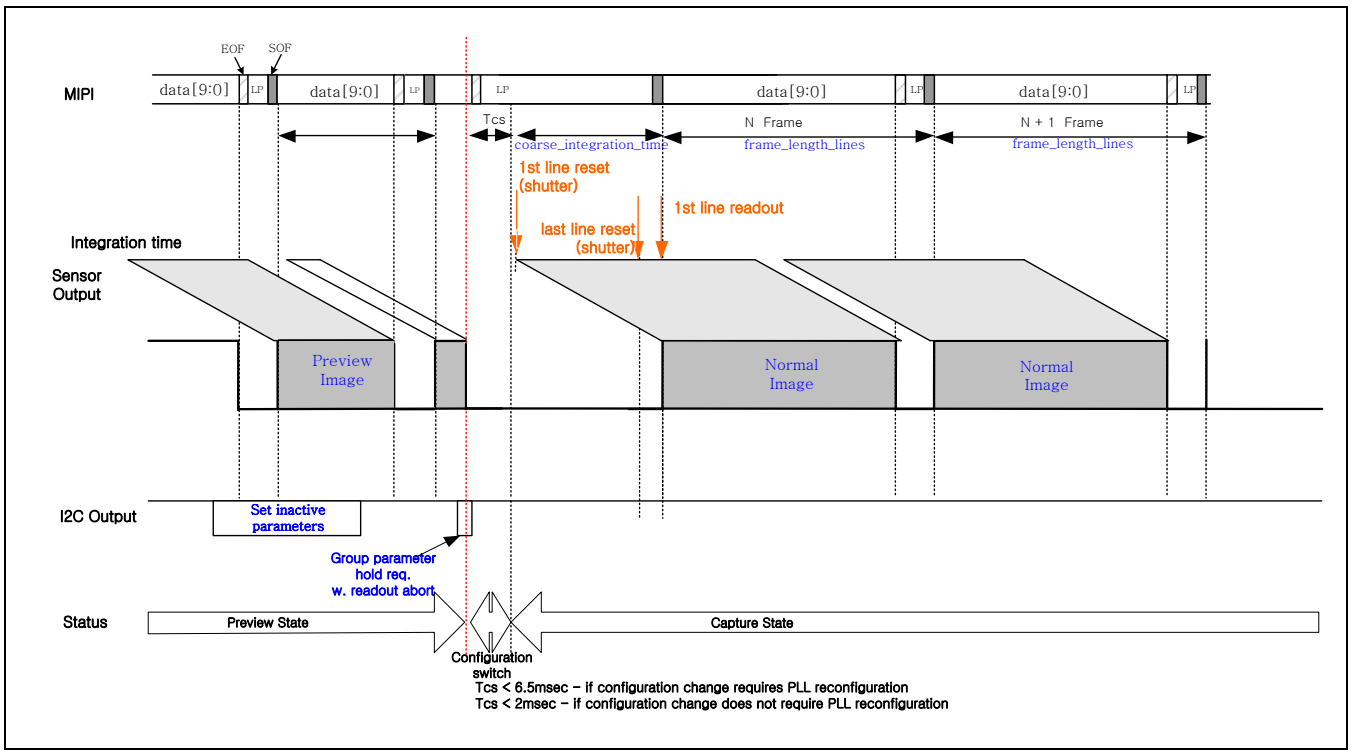

Figure 24 Example-Case (e); Timing Abort: Immediate Abort (Including During Frame Read Out).

8.1.1 Frame Timing Control Configuration

Table 12 Frame Timing Transition Options

	Description
1	Preserve timing and output the corrupted frame
2	Preserve timing skip the corrupted frame
3	Abort after end of timing frame
4	Abort after frame read out ends
5	Abort immediately, even during frame read out (NOTE)

NOTE: The abort immediately has 3 exceptions where the command response will be delayed slightly:

a. Command detected during first 10 timing lines: In this case, firmware will delay the actual abort after the dark lines are finished, and OUTIF transmitted the MIPI short packet "frame-start".
b. Command detected during last 10 readout lines: In this case, firmware will delay the actual abort after readout ends (in order to prevent problematic timing of internal firmware interrupts).
c. Command detected during last 10 timing lines (just before frame ends anyway): In this case, firmware will delay the actual abort after normal API registers read that happens anyway around this time.

8.1.1.1 Rolling Shutter Frame Timing Configuration Change

Table 13 Abort/Preserve Timing Options

Timing Transition Type	Setting
b_abort_timing_on_ch_cfg	0 = Preserve timing (Keep frame rate) 1 = Abort timing if next frame is corrupted (On configuration change)

Table 14 Corrupted Frames Options On Preserve Timing Mode:

Timing Transition Type	Setting
mask_corrupted_frames	0 = Output the corrupted frame. 1 = Don't output the corrupted frame.

Table 15 Rolling Shutter Frame Timing Transition Options

Timing Transition Type	Setting
abort_timing_method_on_rolling_sh	0 = Abort timing Immediately, even during read out. 1 = Abort timing after read out ends 2 = Abort timing on end of frame

8.1.1.2 Mechanical Shutter Frame Timing Configuration Change

Table 16 Mechanical Shutter Frame Timing Transition Options

Timing Transition Type	Setting
abort_timing_mechanical_sh	0 = Abort timing Immediately, even during read out. 1 = Abort timing after read out ends 2 = Abort timing on end of frame

8.1.1.3 Settings Affecting Frame Timing

These are main parameters that if changed will result in frame timing configuration change:

Table 17 Parameters that Cause Frame Timing Change if Modified

Input Size, Mirror, Binning or Line Timing	PLL Modification	If BPC is Enabled
frame_timing_x_addr_start frame_timing_x_addr_end frame_timing_y_addr_start frame_timing_y_addr_end frame_timing_line_length_pck output_data_format sub_sample_x_odd_inc sub_sample_x_even_inc sub_sample_y_odd_inc sub_sample_y_even_inc binning_mode binning_type binning_ver_bin_inc general_setup_image_orientation force_ch_cfg_value min_timing_lines rw_wdr_multiple_exp_mode rw_wdr_exposure_control rw_wdr_exposure_ratio_numer_to_long rw_wdr_exposure_ratio_numer_to_short rw_wdr_exposure_ratio_denum rw_wdr_exposure_order vendor_sensor_enable_af_pixels	clocks_vt_pix_clk_div clocks_vt_sys_clk_div clocks_pre_pll_clk_div clocks_pll_multiplier clocks_op_pix_clk_div clocks_op_sys_clk_div clocks_secnd_pre_pll_clk_div clocks_secnd_pll_multiplier	scaling_mode scaling_scale_m scaling_digital_crop_x_offset scaling_digital_crop_y_offset vendor_sensor_offset_x vendor_sensor_offset_y

8.2 Analog Sensor

8.2.1 Analog to Digital Converter (ADC)

The image sensor has an on-chip ADC. A two-channel column parallel ADC scheme is used for high-speed analog processing.

8.2.2 Analog Gain Control

The user can control the gain of the pixel signal (AG) by using the analog gain control registers.

Analog gain (AG) of up to x16 is supported.

AG precision is determined according to analog_gain_extra_frac_bits Register.

The analogue_gain_code_global register is used to set the analog gain according to these equations:

Table 18 Analog Gain (AG) Control

AnalogGainPrecision	AG
analog_gain_extra_frac_bits = 0 (Default)	AG = analogue_gain_code_global/32
analog_gain_extra_frac_bits = 1	AG = analogue_gain_code_global/64
analog_gain_extra_frac_bits = 2	AG = analogue_gain_code_global/128
analog_gain_extra_frac_bits = 3	AG = analogue_gain_code_global/256

8.2.3 ADC Resolution

The supported ADC effective resolutions are 8/9/10-bit

8.3 Embedded Line

S5K3L8XX may be configured to generate an embedded MIPI header with frame information.

8.4 ISP (Image Signal Processor) Functions

8.4.1 Dual Correlated Double Sampling Statistics

This mechanism of "auto calibration" collects statistical data from the analog circuits and adjusts/keeps optimal analog settings.

8.4.2 Analog Dark Level Correction

This mechanism is responsible for row noise reduction and frame black level recovery by subtracting a weighted sum of optical black pixels. Also, the block collects temperature statistics.

8.4.3 Periodic Offset Mismatch Correction

A difference between analog circuits and channels might produce an undesired position-dependent mismatch (checkers pattern). The algorithms correct additive/offset components of periodic mismatch by adding 4 (2x2) coefficients to appropriate pixels.

8.4.4 Global Offset Correction (GOS)

The GOS model is used for compensating non-uniform pixel offset levels. Such offsets can be caused by non-uniform distribution of dark current in sensor due to various system reasons. The compensation is performed correlatively to the location in the pixel array. The GOS model is flexible and based on fully configurable 10x8 grid. Bilinear interpolation is used to define offset levels between grid points. The model can be programmed to be correlated to system parameters such as temperature.

8.4.5 Periodic Gain Mismatch Correction

The difference between analog circuits and channels might produce an undesired position-dependent mismatch (checkers pattern). The algorithms correct the multiplicative/gain component of periodic mismatch by applying 4 (2x2) coefficients to appropriate pixels.

8.4.6 De-speckle (Bad pixel correction)

Bad pixel correction block is used to fix pre-defined defects that are not handled perfectly by the host ISP bad pixel correction block, such as bad pixel clusters and small level outliers. Isolated bad pixels and pixel pairs can be dynamically detected and replaced based on neighboring pixels pattern at normal mode except WDR mode.

8.4.7 Lens shading correction

A shading correction block is used to compensate for color/brightness shading introduced by the lens

8.4.8 DPCM/PCM Image Compression

10-bit output may be compressed using DPCM/PCM 10-bit to 8-bit compression.

8.4.9 Output Formatting

Raw sensor data in Bayer format is outputted with 8 or 10-bit accuracy.

8-bit output may be uncompressed or compressed.

8.5 General Purpose IO Control (Preliminary)

Table 19 GPIO Functional Table

	STROBE OUT	GPI/GPO
GPIO_1_PAD	Flash/M.Shutter	GPI/GPO
GPIO_2_PAD	Flash/M.Shutter	GPI/GPO
GPIO_3_PAD	Flash/M.Shutter	GPI/GPO
GPIO_4_PAD	Flash/VSYNC_IN	GPI/GPO

8.6 Wide Dynamic Range (WDR) Support

The S5K3L8XX contain a mechanism that enable reaching Wide Dynamic Range (WDR) image capturing at both Video & still modes, allowing high quality image capturing in cases of mixed lightening scenes.

Wide dynamic range acquisition is done by having Multiple Integration Time within the same frame. This is done by interlace pixels of short and long exposure times.

The pixel array of S5K3L8XX support interlacing pixels of short and long exposure times within same frame. Amount of exposure difference between short & long exposed pixels is controllable to allow adapting to present scene. ISP functions as Dark Level Correction & Global Offset Correction allows different handling for short & long exposed pixels. Merging short & long exposed pixels is done within external companion ISP (or Application processor).

8.7 Dual sensor synchronize

The S5K3L8XX contain a mechanism that enable supporting 3D-application. It is important to control 2 sensors' rolling shutters with same timing. The S5K3L8XX supports 3D camera application as shown in the block diagram of Figure 25. The sensor must have to match the VSYNC from the other sensor in each video format.

The following schematic drawing shows the block diagram of 3D-application

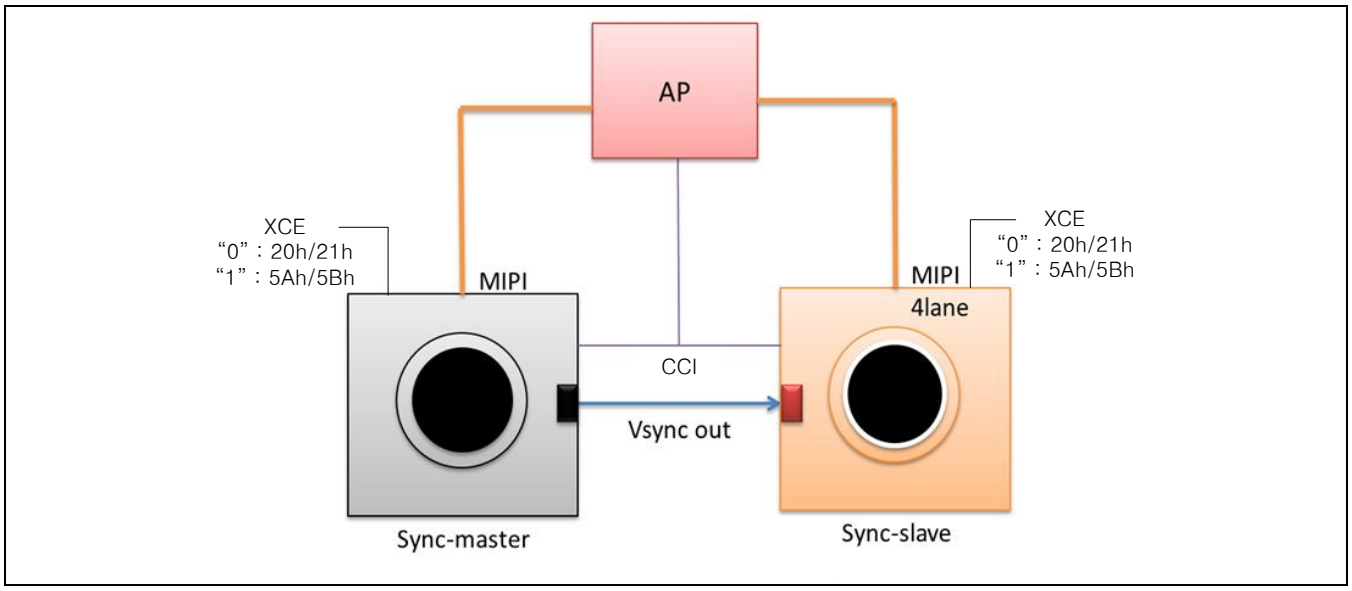

Figure 25 Dual Sensor Synchronize

8.8 System

8.8.1 Clock System

Described in: *5.6 PLL and Clock Generator*

8.8.2 Reset System

Asynchronous HW reset is performed using the RSTN (XSHUTDOWN) pin.

SW reset is possible using CCI register access.

8.8.3 CPU Sub-System

Cortex M3-based system

8.8.4 CCI Slave

The CCI control interface is high priority AHB masters. This allows CPU-independent register access.

8.8.5 Memory System

ROM, RAM on Cortex M3 AHB bus.

ROM code may be modified using on-chip application for FW function replacement.

8.9 NVM OTP Memory

The NVM memory module is a non-volatile OTP (one-timing programming) memory module. This module enables the saving of unique data to each chip at the production stage.

OTP memory is used to store the following unique information:

- Chip ID data – production history data to be stored during die sorting
- Process-dependent calibration parameters
- Bad clusters pixel map for de-speckle
- Parameter for Lens shading

There are three different ways to access each NVM memory:

- Externally, using IO pads by configuring the chip to a dedicated test mode and performing full OTP memory IP write/read protocol.
- Internally, through the APB bus using the controller.
- Internally, through the APB bus by writing dedicated registers and performing full NVM write/read protocol.
- The S5K3L8XX is capable of storing Firmware set-file in the OTP memory. This is useful for shortening its PWR-up sequence as loading set-file via the serial interface can be skipped in this case.

8.9.1 OTP Read/Write Procedure

Contact your FAE for more details.

8.10 Global Reset

The S5K3L8XX provides global reset mode. Global reset allows all rows to have the same integration start and end. Global reset mode is used in conjunction with the external mechanical shutter controlled by the host. The host must program following the sequence and restrictions.

There are three options of operation for the mechanical shutter mode.

- **reset_mode = 0:** The TG waits for the end of the read out of the current frame, and then starts the mechanical shutter mode.
- **reset_mode = 1:** The current rolling shutter frame is truncated at the end of the nearest line, and the mechanical shutter mode is started.
- **reset_mode = 2:** The MS mode will wait for the end of the timing frame.
- **reset_mode = 3:** Illegal.

There is 1H time uncertainty from the MS host command. All timings in the sequence are synchronized to the end of the frame (in case of tgr_glb_reset_mode = 1 it is the end of the nearest line).

8.10.1 Global Reset-Single Frame

The Mechanical Shutter mode (MS) is a special mode in the Global Management block. It is used to capture a frame in a non-rolling shutter mode by exposing all of the array lines at a specific time.
The readout process is performed as always in a line-by-line manner.
The following schematic drawing shows the MS mode from preview to MS and back to preview.

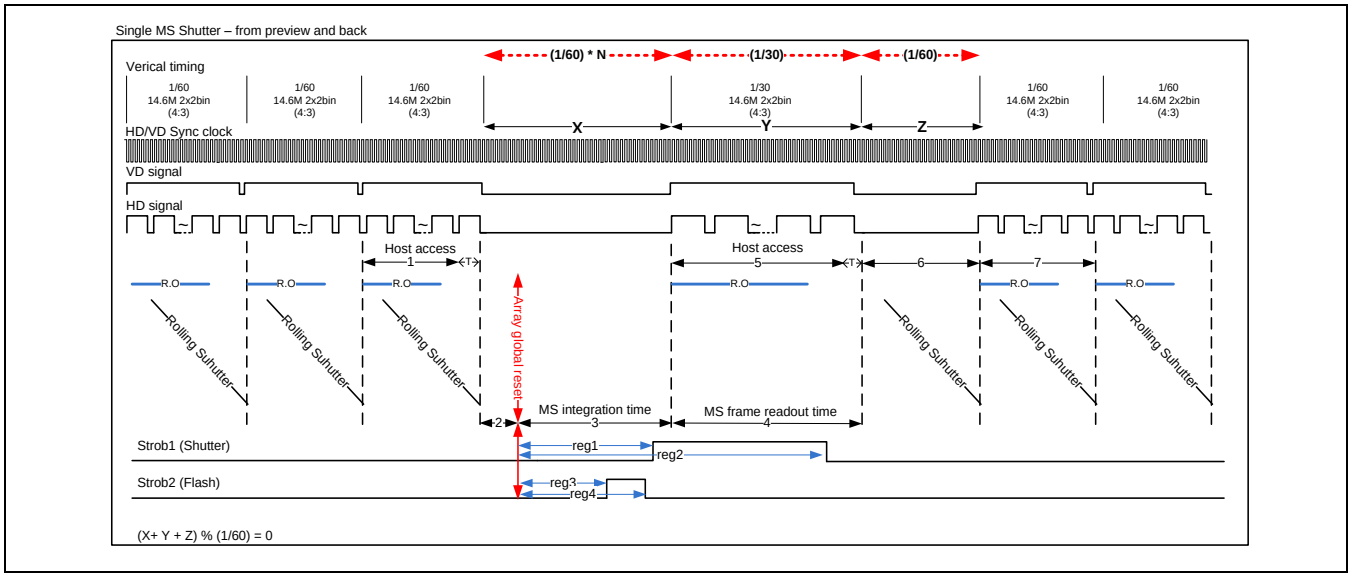

Figure 26 Mechanical Shutter Single Frame

Table 20 Mechanical Shutter Single Frame

Phase	Title	Description
1	Host access for MS	Host access for MS. System at preview mode.
2	Pre global reset	After preview frame is finished, additional time is required for the setting of the array global reset.
3	MS integration time	The entire array is in the integration state until readout starts. Strobe1 and strobe2 for mechanical shutter and xenon are controlled by register pulse generation.
4	MS frame readout	MS configuration frame is output.
5	Host access for preview	Host access for back to preview. Will follow with blank time for integration period.
6	MS frame readout	Integration time for first preview frame.
7	MS frame readout	First preview frame after MS.

1. Timing until the first capture image (X) is a multiple of the preview frame rate.
2. Capture image timing (Y) is a multiple of the preview frame rate.
3. Timing until the first preview image (Z) after capture is a multiple of the preview frame rate.
4. S5K3L8XX maintains a certain time between the HD and VD falling edge to data output under any conditions.
5. S5K3L8XX maintains a certain low period of VD within 1 V time.

8.10.2 Global Reset-with Frame Truncation

The following schematic drawing shows the MS mode from preview to MS with truncated frame:

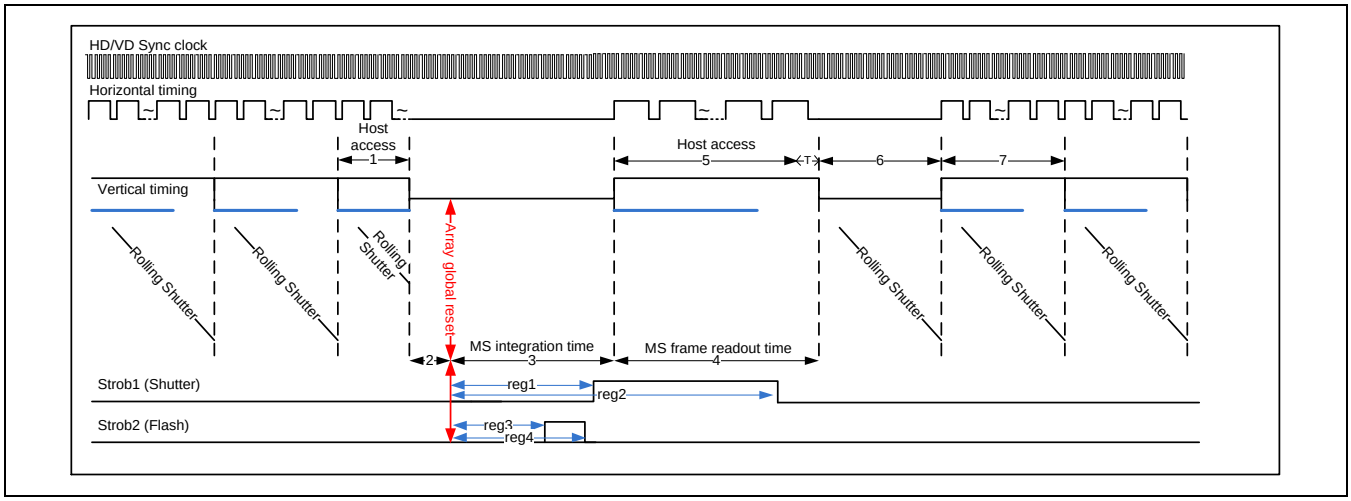

Figure 27 Mechanical Shutter with Frame Truncation

Table 21 Mechanical Shutter with Frame Truncation

Phase	Title	Description
1	Host access for MS	Host access for MS. System in preview mode.
2	Pre global reset	After current frame is immediately truncated, additional time is required for the setting of the array global reset.
3	MS integration time	The entire array is in the integration state until readout starts. Strobe1 and strobe2 are controlled by the register for mechanical shutter and xenon pulses.
4	MS frame readout	MS configuration frame is output.
5	Host access for preview	Host access for back to preview. Will follow with blank time for the integration period.
6	MS frame readout	Integration time for the first preview frame.
7	MS frame readout	First preview frame after MS.

8.11 Test Pattern

S5K3L8XX may be configured to generate deterministic test patterns.

9 Output Data Interface

The S5K3L8XX MIPI CSI-2 interface is a four-lane high-speed serial interface that connects the camera sensor to a host processor. The S5K3L8XX MIPI core IP is compatible with the MIPI Alliance Standards for D-PHY, CSI2 and DSI.

The maximum high speed clock frequency of the MIPI Core is 1.15 GHz.

Main features:

- Main output frame rates:
- Capture: 13M-4:3 30 fps (3939 Mbps)
- FHD video: 10M-16:9 30 fps (2990 Mbps)/2.7M (16:9) 60 fps (1494 Mbps)
- HD video: 1.5M-16:9 100 fps
- High speed: QVGA 240 fps
- MIPI CSI-2: Four lanes with a maximum of 1.15 GHz (bit clock rate) each (144 MHz byte clock).
- Supported data types: RAW,8 RAW10
- Integrated MIPI DPHY V0.90 compatible
- MIPI transmit only
- Support up to four data lanes, one clock lane
- ULPM: Ultra low PWR mode supported

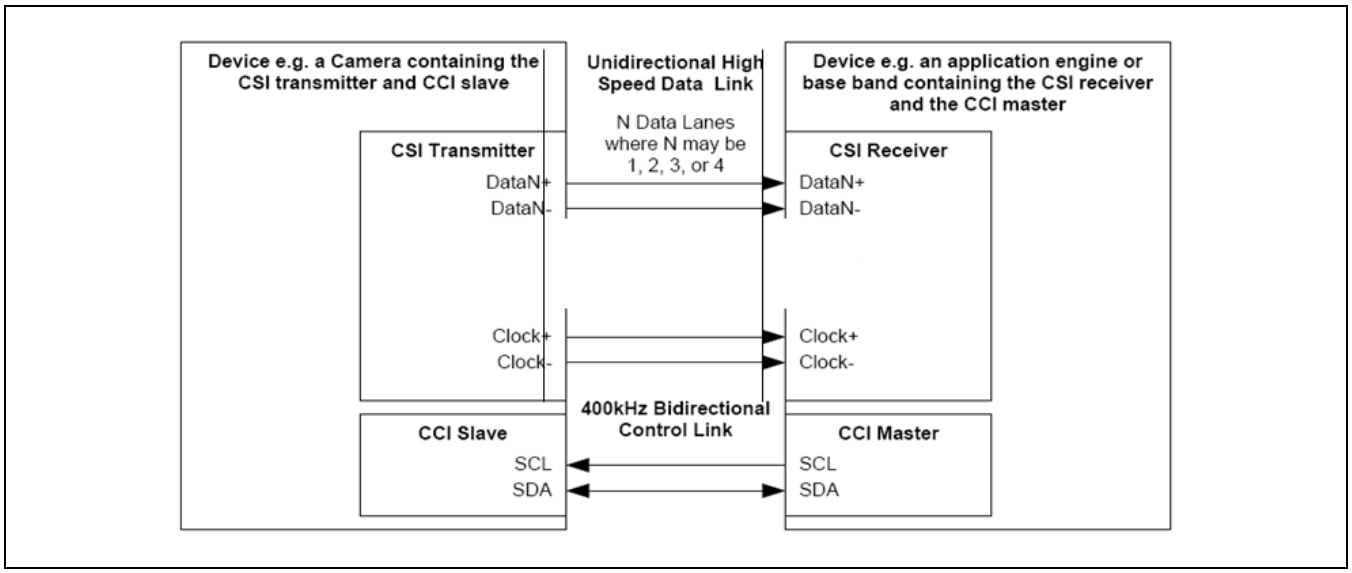

Figure 28 CSI-2 and CCI Transmitter and Receiver Interface

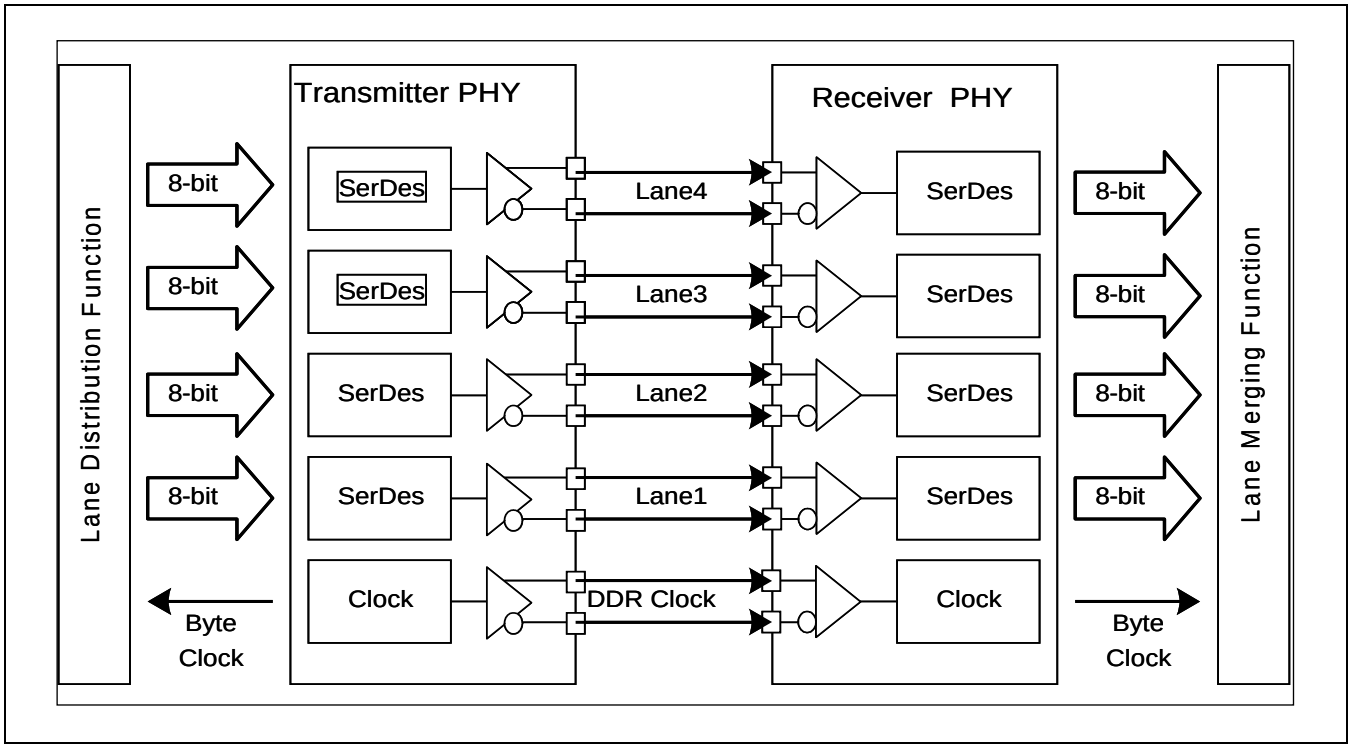

Figure 29 Four Lane Transmitter and Four Lane Receiver Example

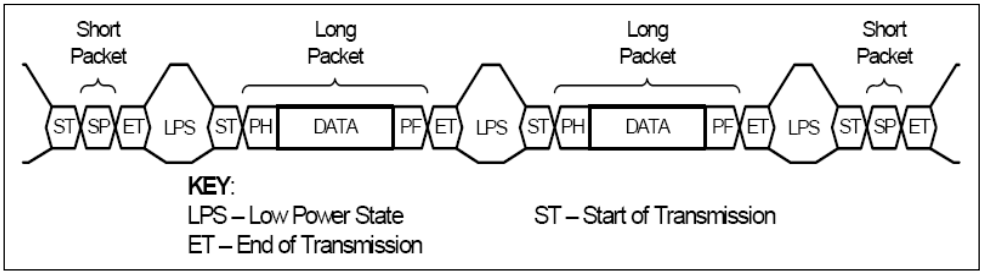

Figure 30 Low Level Protocol Packet Overview

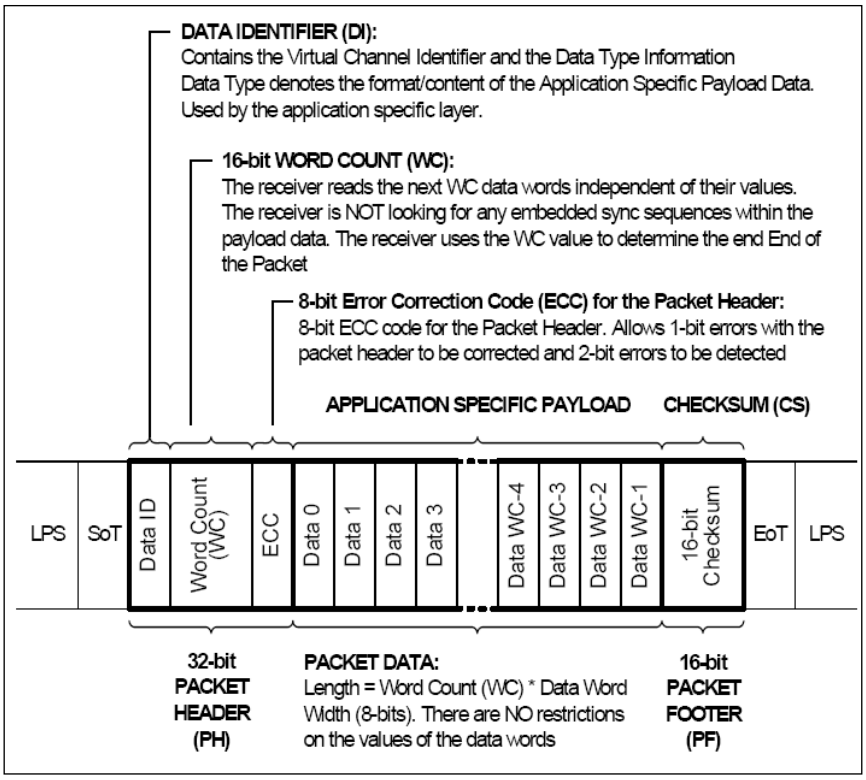

Figure 31 Long Packet Structure

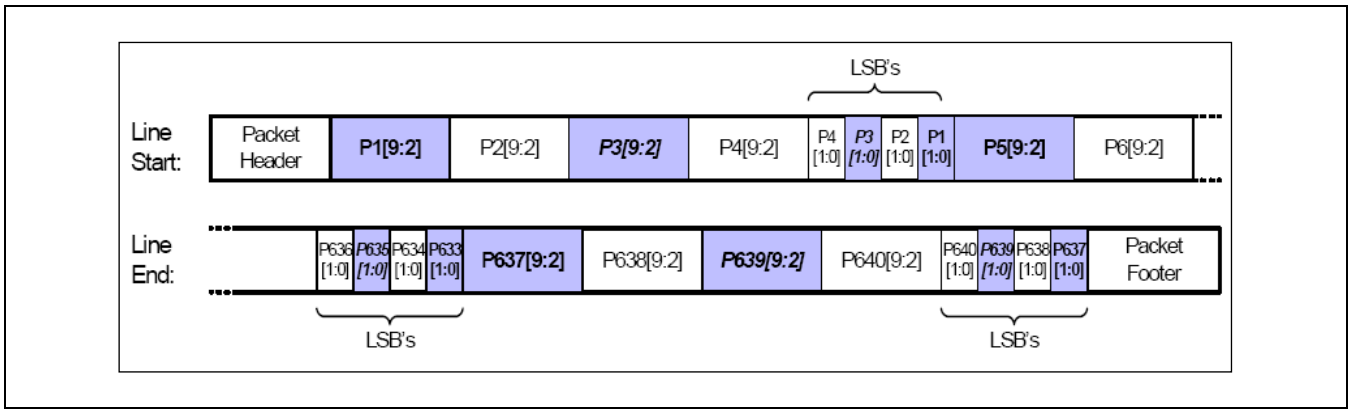

Figure 32 RAW10 Transmission

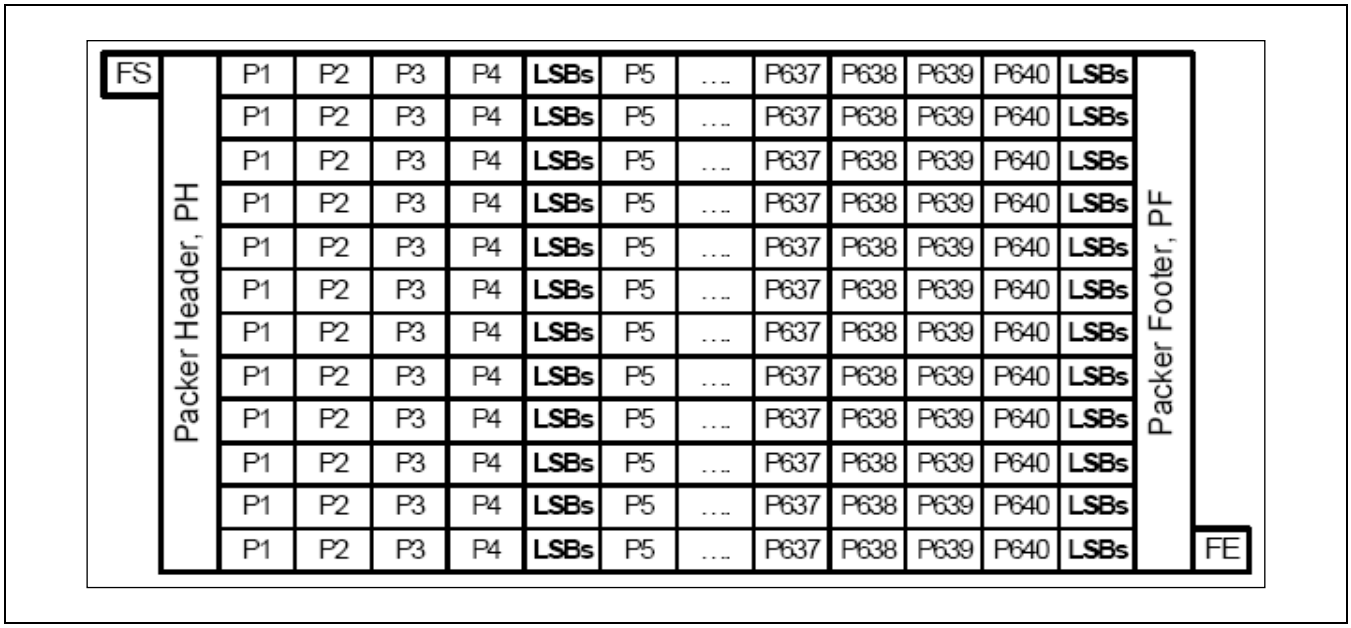

Figure 33 RAW10 Frame Format

10 Electrical Characteristics

10.1 Absolute Maximum Rating

Table 22 Absolute Maximum Rating

Description	Symbol	Min.	Typ.	Max.	Unit
Digital absolute Max. (1)	VDDD (Max.)	– 0.3	–	1.8	V
Analog absolute Max. (2)	VDDA (Max.)	– 0.3	–	4	
I/O absolute Max. (3)	VDDIO (Max.)	– 0.3	–	3.6	
Digital input voltages (4)	VIP	– 0.3	–	VDDIO + 0.3	
VCAP analog voltage (5)	VCAP	–0.3	–	4.2	
Storage temperature	TSTR	– 40	–	85	°C

NOTE:

1. Digital Supply 1.3 V + 0.5 V
2. Analog Supply 2.9 V + 1.1 V
3. IO Supply 2.9 V + 0.7 V
4. Digital Inputs: MCLK, RSTN, XCE, SDI, SCK, GPIO_1/2/3
5. Voltage on external analog capacitors

10.2 Operating Conditions

Table 23 Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit
Digital PWR supply (1)	VDDD	1.15	1.2	1.3	V
Analog PWR supply (2)	VDDA	2.7	2.8	3.0	
I/O supply	VDDIO	1.7	2.8	3.0	
Digital input voltages (3)	VIP	0	–	VDDA	
VCAP analog voltage	VCAP	0	–	4.2	
Test temperature (4)	TTEST	21	23	25	°C
Optimum operating temperature (5)	TOPT	5	–	40	
Normal operating temperature (6)	TOPR	– 25	–	55	
Functional operating temperature (7)	TFUNC	– 30	–	70	

NOTE:

1. Digital Supply Tolerances: Lower limit 1.2 V – 50 mV, Upper Limit: 1.2 V + 100 mV
2. Analog Supply Tolerances: Lower limit 2.8 V – 100 mV, Upper Limit: 2.8 V + 200 mV
3. Digital Inputs: MCLK, RSTN (XSHUTDOWN), SCL, SDA
4. Test Temperature – image quality test conditions
5. Optimum Operating Temperature – no visible degradation in image quality
6. Normal Operating Temperature – camera produces acceptable images
7. Functional Operating Temperature – camera fully functional

10.3 DC Characteristics

Table 24 DC Characteristics

(VDDA = 2.7 V to 3.0 V, VIP = 1.8 V ± 0.1 V (or 2.7 V to 3.0 V), T_A = – 30 to + 70 °C, CLOAD = 20 pF)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	VIH	–	0.7 × VIP	–	–	V
	VIL	–	–	–	0.3 × VIP	
Input leakage current	IIL	VIN = VIP or VSS	– 10	–	10	μA
High level output voltage	VOH	IOH = – 100 μA	VDIG – 0.2	–	–	V
		IOH = – 6, – 8 mA	0.7 × VIO	–	–	
Low level output voltage	VOL	IOL = 100 μA	–	–	0.2	
		IOL = 6, 8 mA	–	–	0.3 × VIO	
High-Z output leakage current	IOZ	VOUT = VSS or VDDD	– 10	–	10	μA
Input capacitance	CIN	–	–	–	5	pF
Supply current	IHWSBA	Hardware standby mode analog	–	TBD	TBD	μA
	IHWSBD	Hardware standby mode digital	–	–	–	
	ISWSB1A	Software standby mode analog	–	TBD	TBD	
	ISWSB1D	Software standby mode digital	–	TBD	TBD	
	ISWSB2A	Software standby mode analog	–	–	TBD	
	ISWSB2D	Software standby mode digital	–	TBD	TBD	
		Streaming mode analog 13M@30 fps 4:3	–	TBD	TBD	
		Streaming mode analog 13M@24 fps 4:3	–	TBD	TBD	
		Streaming mode analog 10M@30 fps 16:9	–	TBD	TBD	
		Streaming mode analog 2.6M@30 fps 16:9	–	TBD	TBD	
	ISTRMD2	Streaming mode digital 13M@30 fps 4:3	–	TBD	TBD	
		Streaming mode digital 13M@24 fps 4:3	–	TBD	TBD	
		Streaming mode digital 10M@30 fps 16:9	–	TBD	TBD	
		Streaming mode digital 2.6M@30 fps 16:9	–	TBD	TBD	
	ISTRMIO	Streaming mode digital @30 fps	–	–	TBD	

10.4 AC Characteristics

Table 25 AC Characteristics

(VDDA = 2.7 V to 3.0 V, VIP = 1.8 V ± 0.1 V (or 2.7 V to 3.0 V), T_A = – 30 to + 70 °C)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
External clock frequency (NOTE)	fXCLK	–	12	–	56.0	MHz
External clock duty cycle (NOTE)	fXDUTY	–	45	–	55	%
PLL locking time	tLOCK	–	–	200	1000	µs

NOTE: Applied to MCLK pin

10.5 TX Driver Characteristics

Table 26 Tx HS Transmitter DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
VCMTX	HS transmit static common-mode voltage	150	200	250	mV	(1)
|ΔVCMTX (1, 0)|	VCMTX mismatch when output is Differential-1 or Differential-0	–	–	5		(2)
|VOD|	HS transmit differential voltage	140	200	270		(1)
|ΔVOD|	VOD mismatch when output is Differential-1 or Differential-0	–	–	10		(2)
VOHHS	HS output high voltage	–	–	360		(1)
ZOS	Single ended output impedance	40	50	62.5	Ω	–
ΔZOS	Single ended output impedance mismatch	–	–	10	%	–

NOTE:

1. Value when driving into load impedance anywhere in the ZID range.
2. It is recommended that the implementer minimize ΔVOD and ΔVCMTX (1, 0) in order to minimize radiation and optimize signal integrity.

Table 27 Tx HS Transmitter AC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
VCMTX (HF)	Common-level variation above 450 MHz	–	–	15	mVRMS	–
VCMTX (LF)	Common-level variation between 50 to 450 MHz	–	–	25	mVPEAK	–
tR and tF	20 % to 80 % rise time and fall time	–	–	0.3	UI	1
		150	–	–	ps	–

NOTE: UI is equal to 1/(2*fh). "f" is the highest fundamental frequency for data transmission.

Table 28 Tx LP Transmitter DC Specifications

Parameter	Description	Min.	Typ.	Max.	Unit
V_{OH}	Thevenin output high level	1.15	1.2	1.3	V
V_{OL}	Thevenin output low level	– 50	–	50	mV
Z_{OLP}	Output impedance of LP transmitter	110	–	–	Ω

Table 29 Tx LP Transmitter AC Specifications

Parameter	Description		Min.	Typ.	Max.	Unit
T_{RLP}/T_{FLP}	15 % to 85 % rise time and fall time		–	–	25	ns
T_{REOT}	30 % to 85 % rise time and fall time		–	–	35	
$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	–	–	
		All other pulses	20	–	–	
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock		90	–	–	–
–	Slew rate @ CLOAD = 20 pF		30	–	150	mV/ns
	Slew rate @ CLOAD = 70 pF		30	–	100	
C_{LOAD}	Load capacitance		0	–	70	pF

11 Mechanical

11.1 Package Specification

Refer to S5K3L8XX_Assembly_Guide.