Preliminary

Specification of

YACJ3B0C9SHC

[Rev. 0.6]

1/3” 13M Pixel

CMOS Image Sensor

[Hi-1332]

Revision History

Version	Date	Comments
0.0	2015/11/03	YACJ3B0C9SHC Datasheet is released (Preliminary)
0.1	2015/11/5	Errata is modified
0.2	2016/01/14	Reference Module Schematic is modified
0.3	2016/03/15	h mirror is newly defined
0.4	2016/06/29	Min Mclk & Schematic are modified.
0.5	2016/06/30	Notification of register description change
0.6	2016/08/02	orientation register and standby figure are modified

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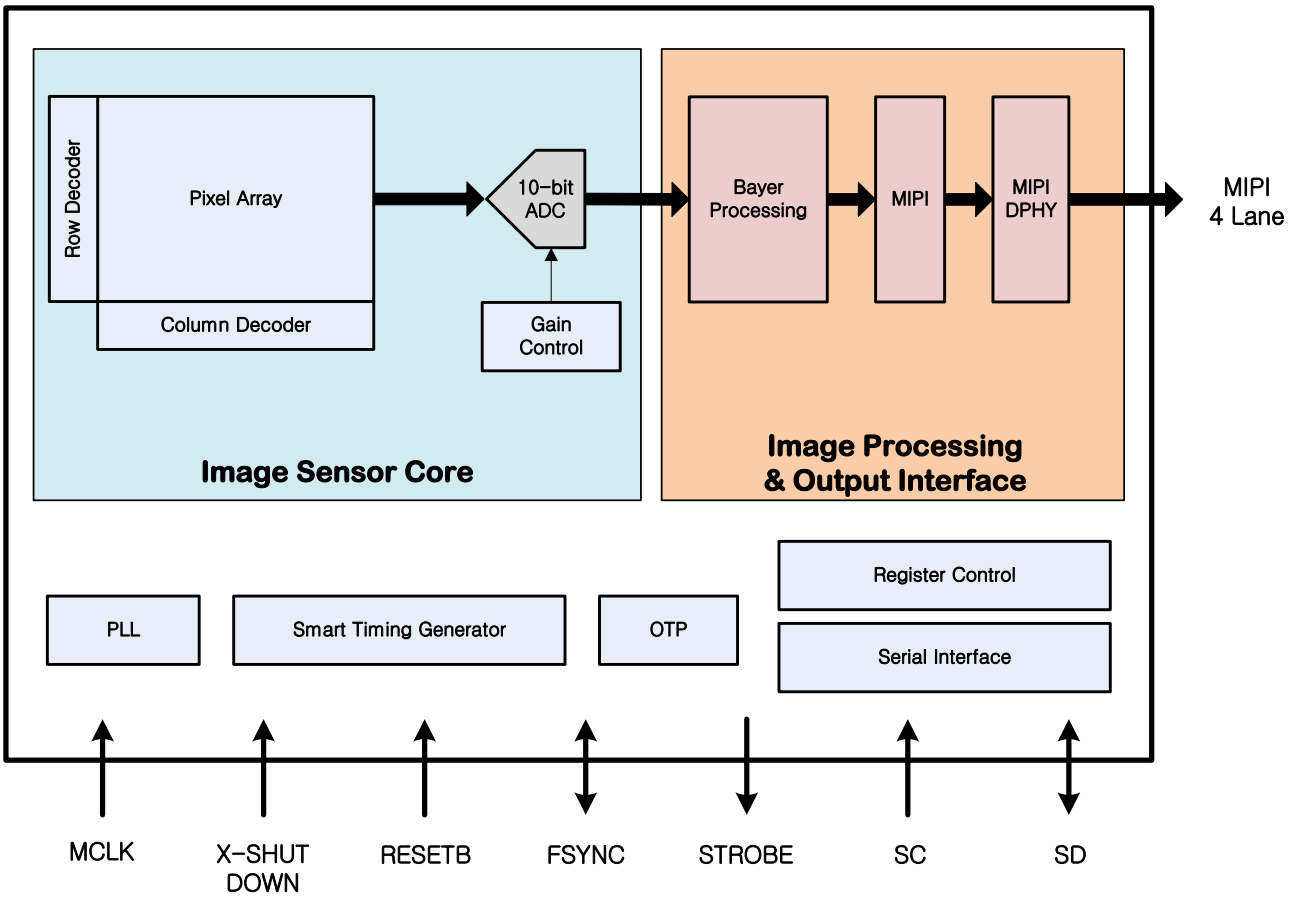
1. OVERVIEW

1.1. Description

YACJ3B0C9SHC is a high quality 13mega-pixel single chip CMOS image sensor for mobile phone camera applications and digital still camera products.

YACJ3B0C9SHC incorporates a 4208x3120 pixel array, on-chip 10-bit ADC and an image signal processor. Unique sensor technology enhances image quality by reducing FPN (Fixed Pattern Noise), horizontal/vertical line noise and random noise.

<Figure 1. Block Diagram>



1.2. Applications

- Mobile Phone Camera / Digital Still Camera
- PC Camera / Video Conference

1.3. Key Features

- Pixel Size : 1.12um X 1.12um, BSI
- Effective Image Size : 4730.88um (H) X 3512.32um(V) (4224 X 3136)
- Resolution : 4208 X 3120
- Color Filter : RGB Bayer
- Optical Format : 1/3 inch
- Frame Rate : 30fps@ 4208x3120,
  60fps@ Full HD 1080P,
  60fps@ HD 720P
- Power Supply : Analog : 2.8V,
  IO : 1.8V / 2.8V
  Core(Digital) : 1.2V
- Power Consumption :
  227mW @ 30fps, 4208x3120
  201mW @ 60fps, FHD 1080P
  185mW @ 60fps, HD 720P
- ADC : 10bit
- PLL : On Chip
- Operation Temperature: -20 ~ 60°C
- Master Clock : 10 ~ 27MHz
- Output Format : RGB Bayer 10bit
- Windowing : Programmable
- Host Interface : two-wire serial bus interface
- Analog Binning
- Sub-Sample : 1/2, 1/3,1/4,1/6
- Image Flip : X/Y Flip
- Black Level Calibration
- Digital gain control : x1 ~ x16, (1/512 step)
- Built-in test pattern generation
- Internal PLL for high speed clock generation
- MIPI 1/2/4-Lane (Max 1.2Gbps)
- Standby mode for power saving
- 8KB OTP Memory
- Lens Shading Correction
- Strobe Control : Support Xenon / LED Type
- On-chip Defect correction for couplets & Clusters
- Line-interlaced long-short output for iHDR (inter-line HDR)
- Support for PDAF(Optional)

2. Electrical characteristics

2.1. Key Features

[Table 1. DC Characteristics]

Item	Symbol	Min	Typ	Max	Unit	Note
Digital Core Circuit Power Supply Voltage	$V_{DD:D}$	1.15	1.2	1.3	V	
Analog Circuit Power Supply Voltage	$V_{DD:A}$	2.7	2.8	3.0	V	
Analog Pixel Circuit Power Supply Voltage	$V_{DD:P}$	2.7	2.8	3.0	V	
Digital I/O Circuit Power Supply Voltage	$V_{DD:I}$	1.7/2.7	1.8/2.8	2.0/3.0	V	1
H level Input Voltage	V_{IH}	0.7 * $V_{DD:I}$			V	
L level Input Voltage	V_{IL}			0.3 * $V_{DD:I}$	V	

Note1) VDD:I Typical voltage 1.8V (min 1.7V, max 2.0V)
VDD:I Typical volage 2.8V (min 2.7V, max 3.0V)

[Table 2. Temperature Characteristics]

Item	Symbol	Rating	Unit	Note
Storage Temperature	T_{STR}	-40 ~ 80	°C	
Functional Operating Temperature	T_{FUN}	-20 ~ 60	°C	Camera fully functional

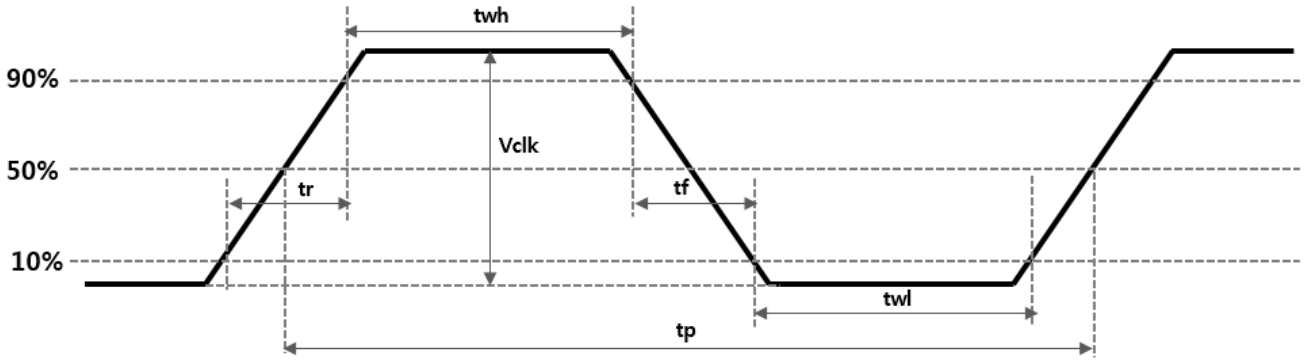
[Table 3. Power Consumption]

Item	Condition		Min	Typ	Max	Unit	Note
Full@30fps	$V_{DD:A}$ &$V_{DD:P}$=2.8V			46	58	mA	1
	$V_{DD:D}$=1.2V			81	108	mA	
	$V_{DD:I}$	1.8V		0.5	1	mA	2
		2.8V		1	2	mA	
FHD 1080P@60fps	$V_{DD:A}$ &$V_{DD:P}$=2.8V			46	58	mA	1
	$V_{DD:D}$=1.2V			59	78	mA	
	$V_{DD:I}$	1.8V		0.5	1	mA	2
		2.8V		1	2	mA	
HD 720P@60fps	$V_{DD:A}$ &$V_{DD:P}$=2.8V			46	58	mA	1
	$V_{DD:D}$=1.2V			46	60	mA	
	$V_{DD:I}$	1.8V		0.5	1	mA	2
		2.8V		1	2	mA	
Stand by Current					200	uA	3

Note1) Because current of analog circuit depends on the registers' values, it is measured at specific register's value .
Note2) Because power consumption of VDD:I depends on the output load and system environment, users should supply enough current to sensor for stable operation. It is measured when output load is floated.
Note3) Standby current is measured at XSHUTDOWN = LO and MCLK = LO.
We recommend that power should be turned off, when low standby power consumption is required

2.1.1 Master Clock Waveform Specification

< Figure 1.1 Master Clock Waveform Diagram >



[Table 4.1 Master Clock(MCLK) AC Characteristics >

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Frequency	MCLK	10	24	27	MHz
MCLK Amplitude	Vclk	1.7/2.7	1.8/2.8	2.0/3.0	V
MCLK Duty Cycle	twh/twl	0.45tp		0.55tp	ns
MCLK Clock Period	tp	37.0		100	ns
MCLK Rise/Fall Time	tr/tf			10	ns
MCLK Jitter(Peak-to-Peak)	Tjitter			600	ps

2.2. MIPI Features

[Table 4. HS Transmitter DC Specifications]

Parameter	Description	Min	Typ	Max	Unit
VCMTX	HS transmit static common-mode voltage	150	200	250	mV
|△VCMTX(1,0) |	VCMTX mismatch when Differential-1 or Differential-0			5	mV
| VOD |	HS transmit differential voltage	140	200	270	mV
|△VOD |	VOD mismatch when Differential-1 or Differential-0			10	mV
VOHHS	HS output high voltage			360	mV
ZOS	Single ended output impedance	40	50	62.5	Ω
△ZOS	Single ended output impedance mismatch			10	%

[Table 5. HS Transmitter AC Specifications]

Parameter	Description	Min	Typ	Max	Unit
△VCMTX(HF)	Common-level variation above 450MHz			15	mVRMS
△VCMTX(LF)	Common-level variations between 50-450MHz			25	mVPEAK
tR and tF	20% ~ 80% rise time and fall time			0.3	UI
		150			ps

[Table 6. LP Transmitter DC Specifications]

Parameter	Description	Min	Typ	Max	Unit
VOH	Thevenin output high level	1.1	1.2	1.3	V
VOL	Thevenin output low level	-50		50	mV
ZOLP	Output impedance of LP transmitter	110			Ω

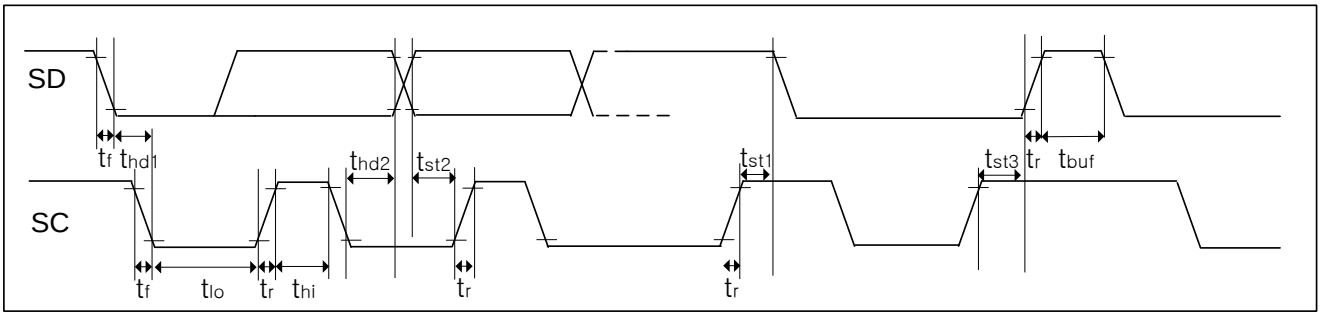
[Table 7. LP Transmitter AC Specifications]

Parameter	Description		Min	Typ	Max	Unit
TRLP/TFLP	15%~85% rise time and fall time				25	ns
TREOT	30%~85% rise time and fall time				35	ns
TLP-PULSE-TX	Pulse width of the LP exclusive – OR clock	First LP exclusive – OR clock pulse after Stop state or last pulse before Stop state	40			ns
		All other pulses	20			ns
TLP-PER-TX	Period of the LP LP exclusive – OR clock		90			ns
δV/δtSR	Slew rate @ CLOAD = 0pF		30		500	mV/ns
	Slew rate @ CLOAD = 20pF		30		150	mV/ns
	Slew rate @ CLOAD =70pF		30		100	mV/ns
CLOAD	Load capacitance		0		70	pF

3. Two-Wire Serial Bus Interface

3.1. Timing Specifications

<Figure 2. AC Timing of Two Wire Serial Bus >



[Table 8. AC Characteristics of Two Wire Serial Bus]

Parameter	Symbol	Min.	Typ.	Max.	Unit
SC frequency	f_{sck}	100		400	KHz
SC low period	t_{lo}	1.3		-	us
SC high period	t_{hi}	0.6		-	us
SC setup time for START condition	t_{st1}	0.6		-	us
SC setup time for STOP condition	t_{st3}	0.6		-	us
SC hold time for START condition	t_{hd1}	0.6		-	us
SD setup time	t_{st2}	0.6		-	us
SD hold time	t_{hd2}	0		-	us
Bus free time Between STOP and START condition	t_{buf}	1.3		-	us
Rising time of both SD and SC	t_r	-		0.3	us
Falling time of both SD and SC	t_f	-		0.3	us
Capacitive load of SC/SD	C_b	-		100	pF
Pull-up resistor on SC and SD			1.5		kΩ

3.2. Bus Operation

The two-wire serial bus interface is used to write and read the required data into registers in this sensor. Sensor can operate as a slave device only. The two-wire serial bus interface is controlled by SD (serial data) and SC (serial clock). SD is bidirectional bus.

Operation has single byte programming and multiple byte programming. Users doesn't need to set continuously register address on programming multiple byte because the sensor increases register address automatically. This will reduce time to program registers.

Following figures show write and read operations.

Note) Before programming the two-wire serial bus interface, MCLK and RESETB,XSHUTDOWN should be supplied.

In YACJ3B0C9SHC, Slave address is controlled by the I2C_ID_SEL1(#23) and I2C_ID_SEL0 (#51) pads.

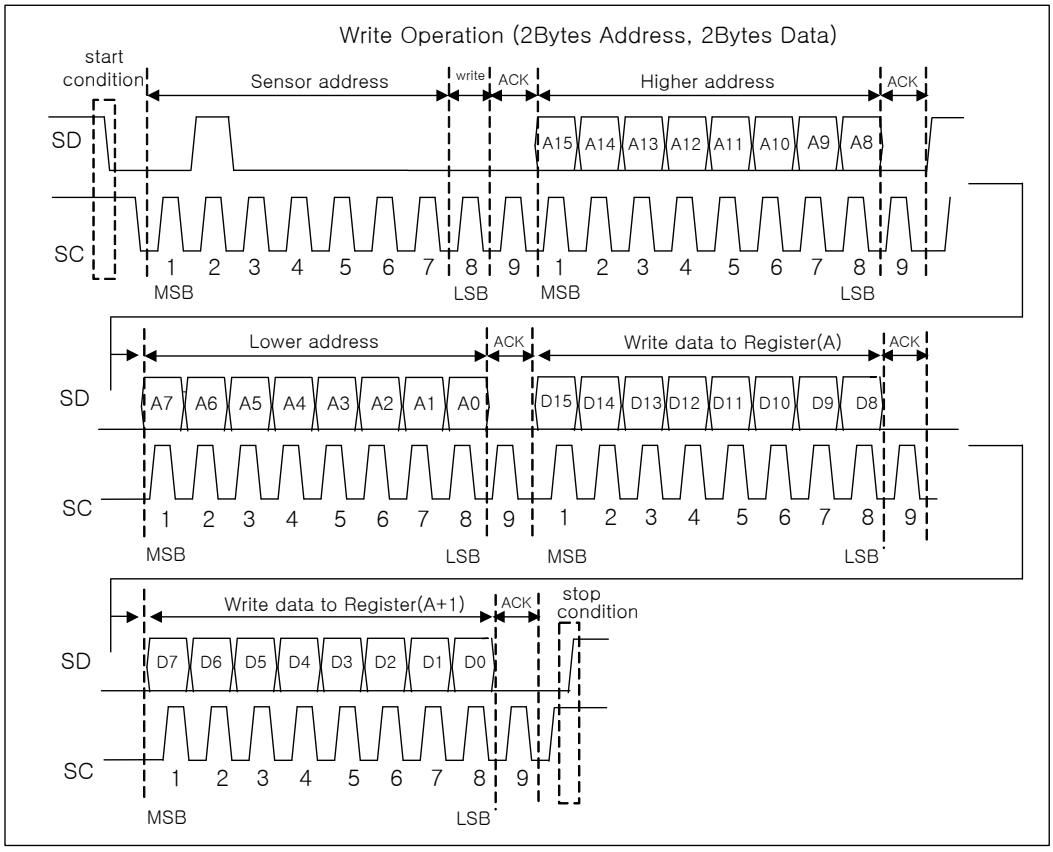
[Table 9. Slave address setting]

Slave address(@ 8bit)	I2C_ID_SEL1	I2C_ID_SEL 0
0x40	Low(default)	Low(default)
0x42	Low	High
0x44	High	Low
0x46	High	High

3.2.1. Write Operation (2 bytes address – 2byte data format)

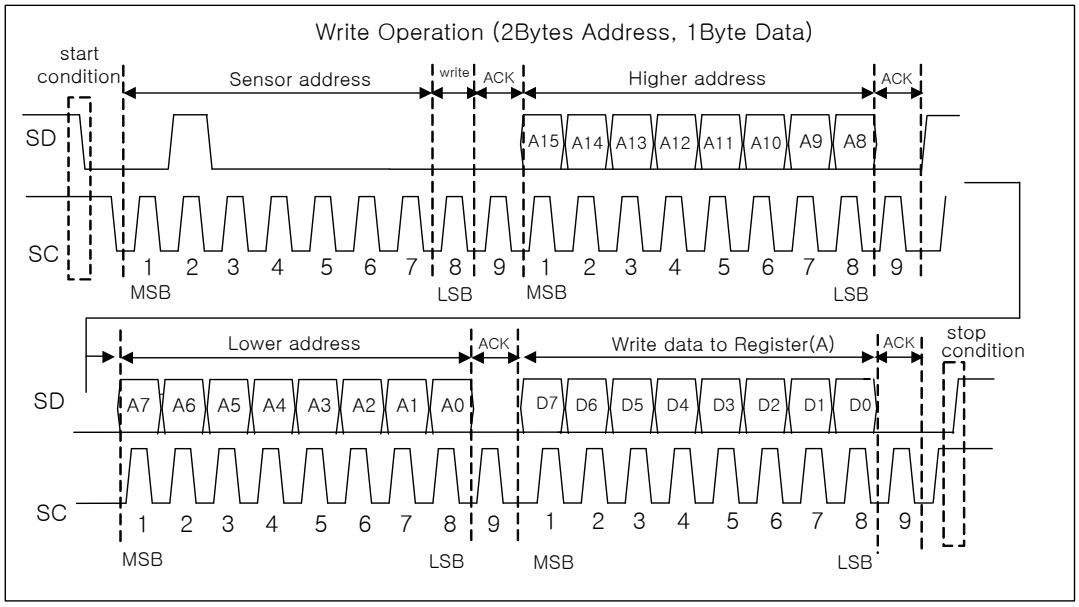
2 Byte address 1byte data format is used OTP operations.

<Figure 3. Write Operation - 2bytes address/2bytes data format>



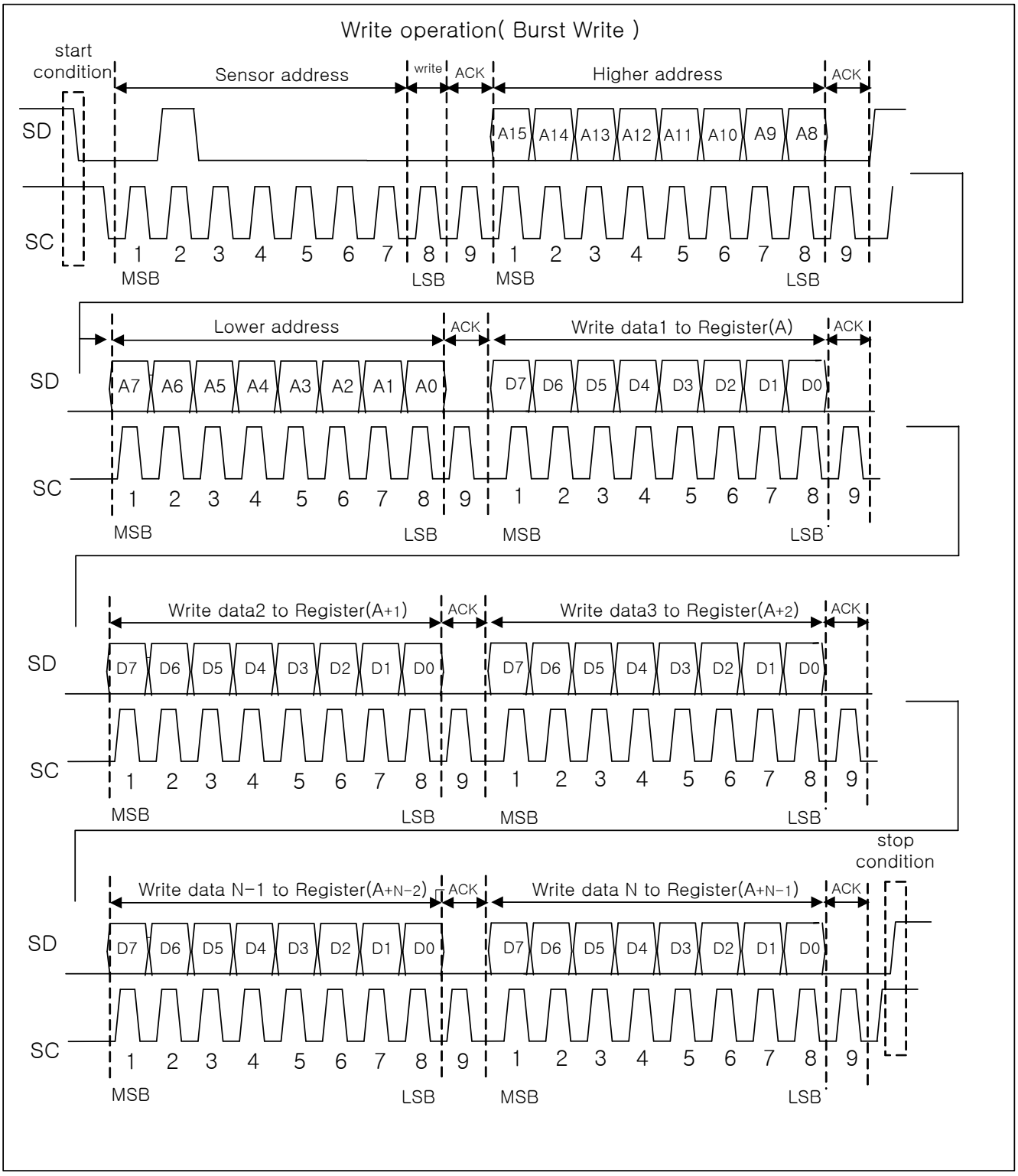
3.2.2. Write Operation (2 bytes address – 1byte data format)

<Figure 4. Write Operation - 2byte address/1byte data format>



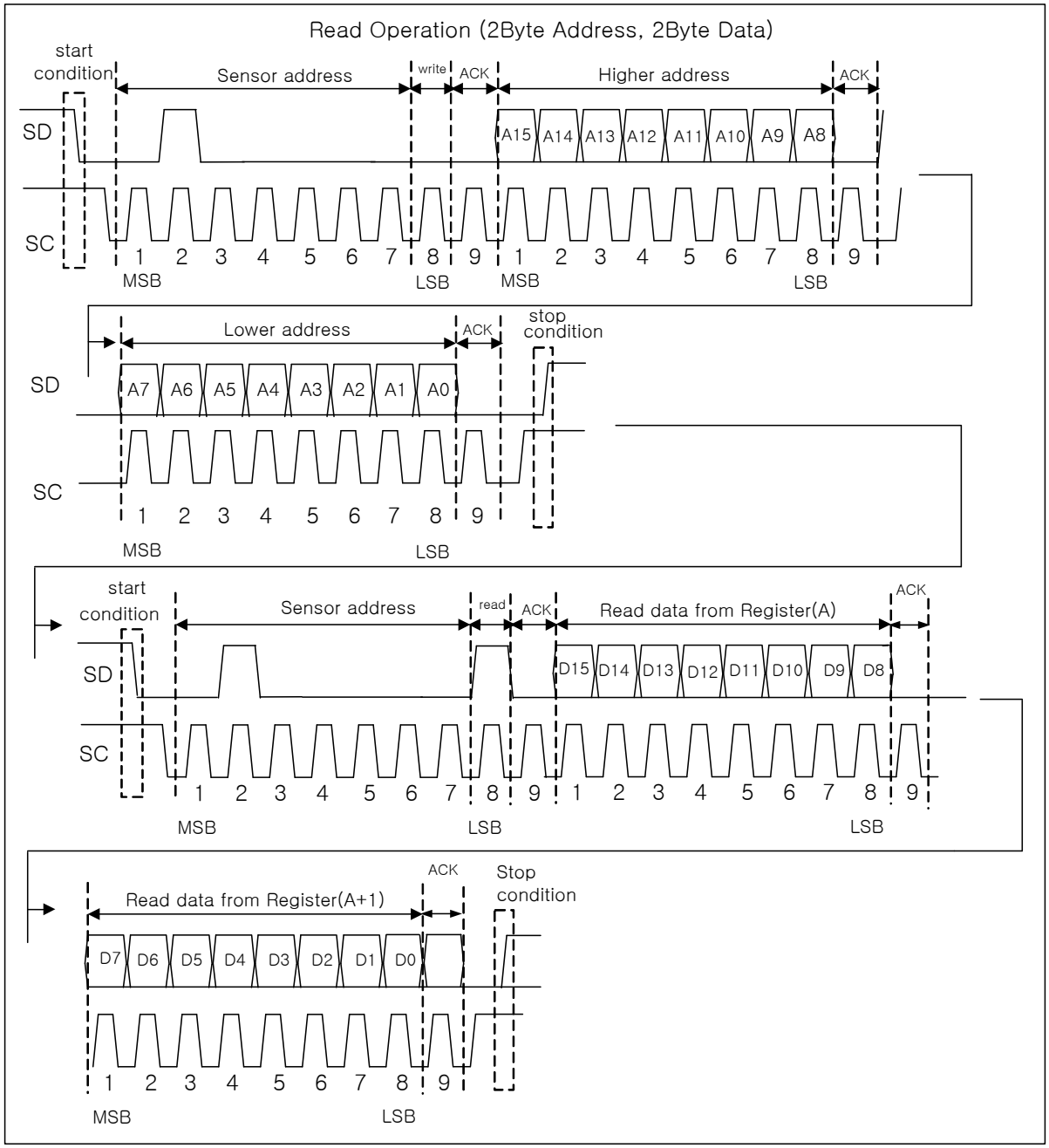
3.2.3. Write Operation (Burst Write)

<Figure 5. Write Operation – Burst Write>



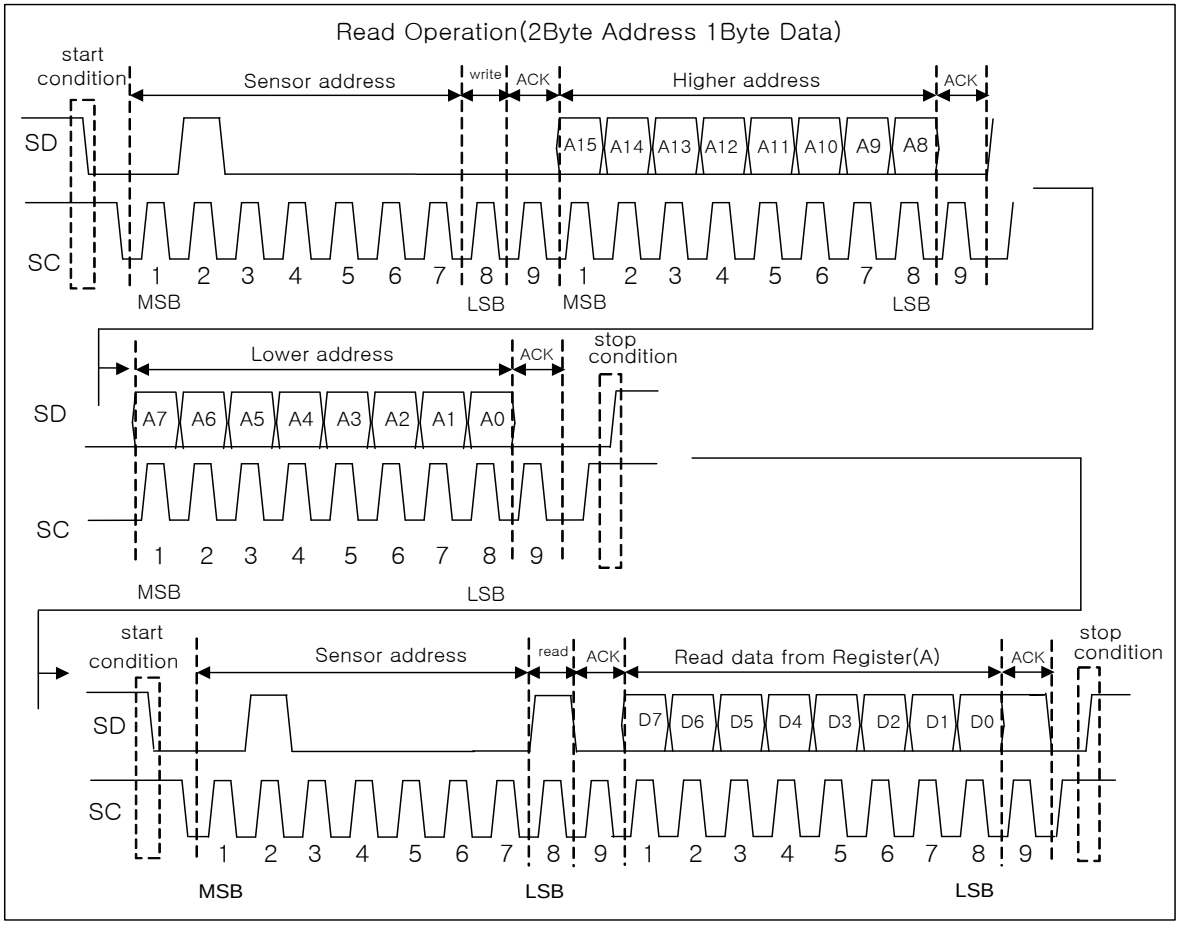
3.2.4. Read Operation (2 bytes address – 2bytes data format)

<Figure 6. Read Operation - 2bytes address/2bytes data format >



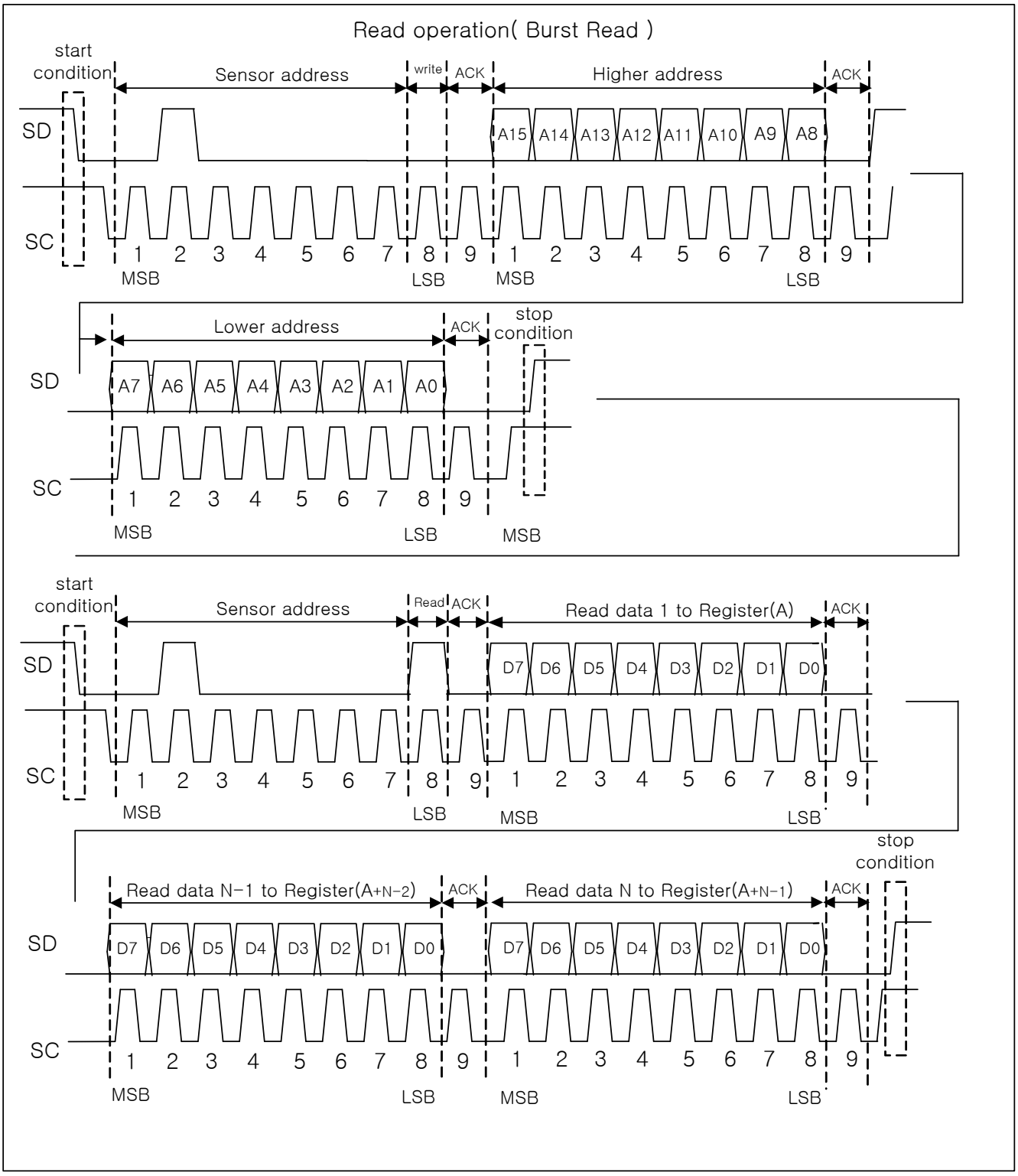
3.2.5. Read Operation (2 bytes address – 1byte data format)

<Figure 7. Read Operation - 2bytes address/1byte data format >



3.2.6. Read Operation (Burst Read)

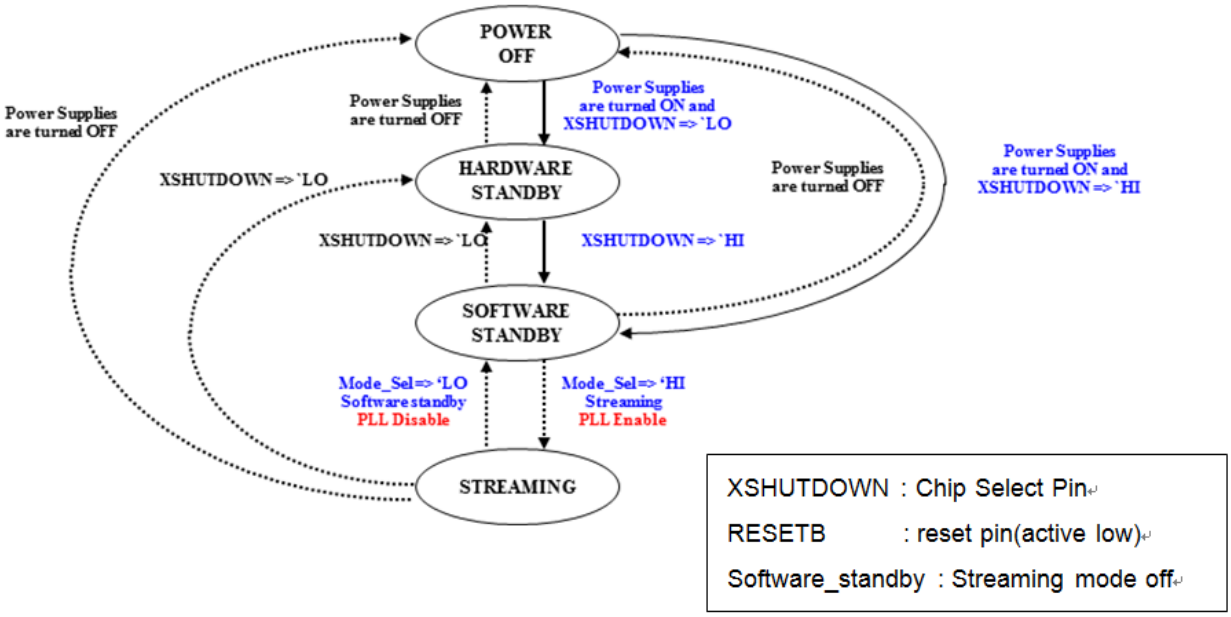
<Figure 8 . Read Operation - Bust Read >



4. FUNCTION DESCRIPTION

4.1. Operation Mode

<Figure 9. System State Diagram>



[Table 10. Operation Mode Summary]

Power State	Description	Activate
Power OFF	Power supplies are turned off	None
Hardware Standby	No communication with the sensor is possible Low level on XSHUTDOWN pin and stopping EXTCLK	XSHUTDOWN Low MCLK Low
Software Standby	CCI communication with sensor is possible PLL is ready for fast return to Streaming mode	Power consumption is arrowed to achieve fast transition between streaming and SW Standby modes. MCLK Pad Enabled
Streaming	The sensor module is fully powered and is streaming image data on the CCP2 bus. (Initialized all logic block with APOR)	All Logic, MCLK Pad Enabled

In operating mode, two type of usage may be possible.

First, XSHUTDOWN and RESETB pin is used to control the operating mode which is traditional way.

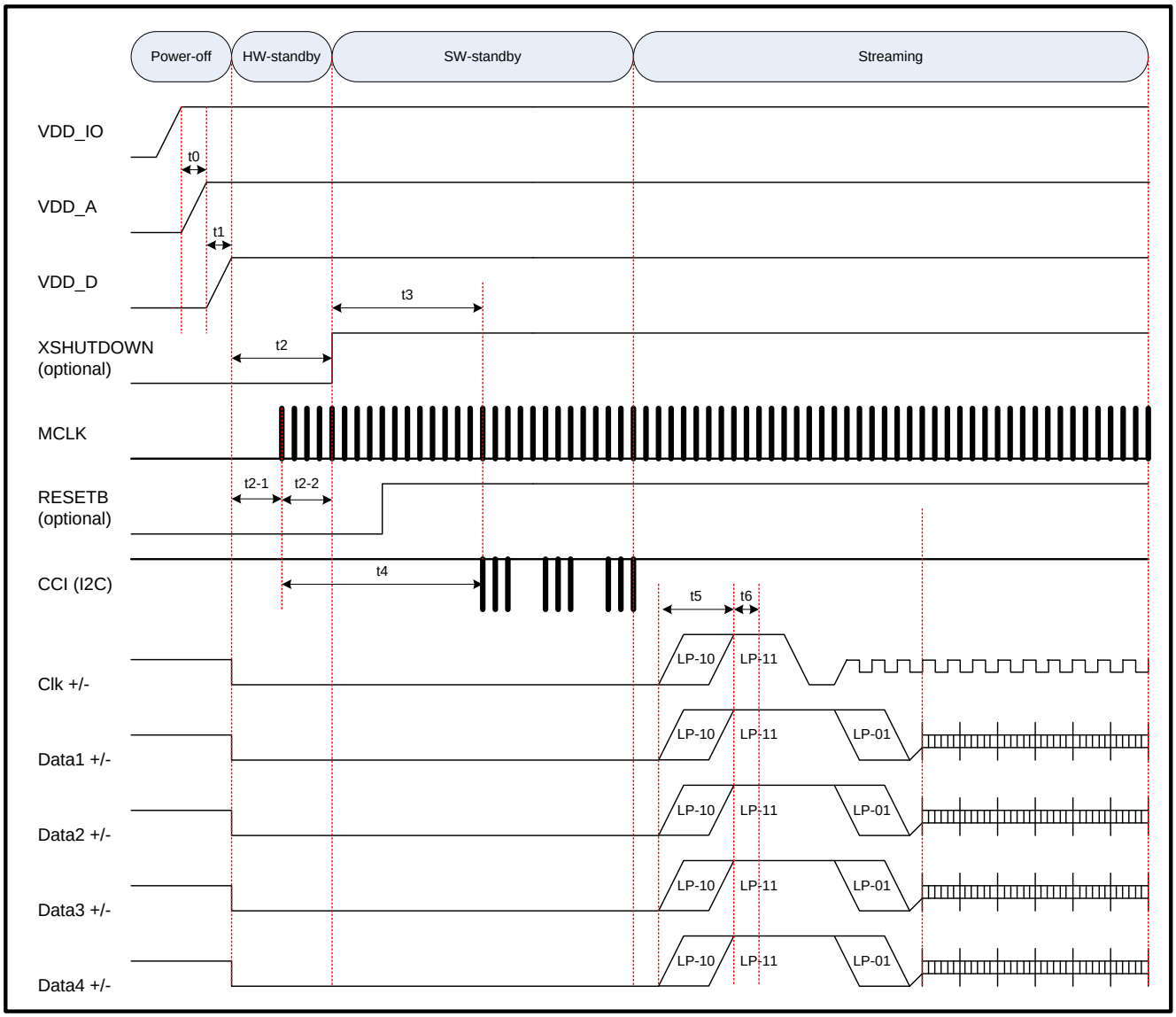
Second, to minimize the module pin connection, XSHUTDOWN and RESETB can be omitted in module connection. In the case, the sensor will be automatically enabled when external clock(MCLK) is active. And then, the internal POR is used to initialize the sensor status.

4.2. Power Timing

Power On Sequence (Normal control)

VDDIO 2.8V/1.8V(ON) → VDDA 2.8V(ON) → VDDD 1.2V (ON) → MCLK(ON) → XSHUTDOWN(L→H) → RESETB(ON) → Set registers for normal operation → Normal Operation

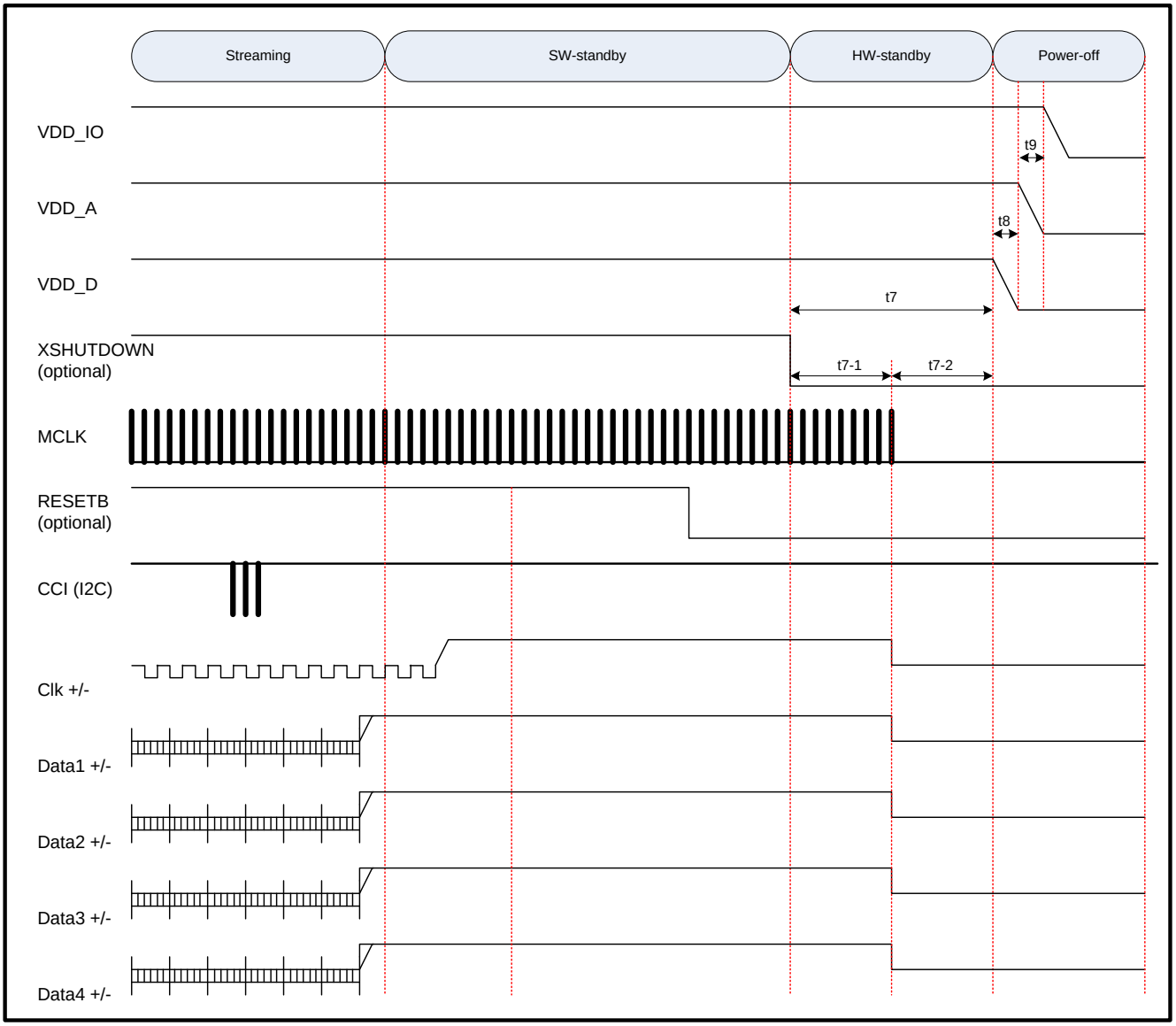
<Figure 10. Timing of Power on Sequence>



Power Off Sequence (Normal control)

Normal Operation → Power Sleep command and disable PLL → SC, SD (OFF) → RESETB(OFF) → XSHUTDOWN(H→L)→ MCLK(OFF)→ VDDD 1.2V (OFF) → VDDA 2.8V(OFF) → VDDIO 2.8V/1.8V(OFF)

<Figure 11. Timing of Power off Sequence>



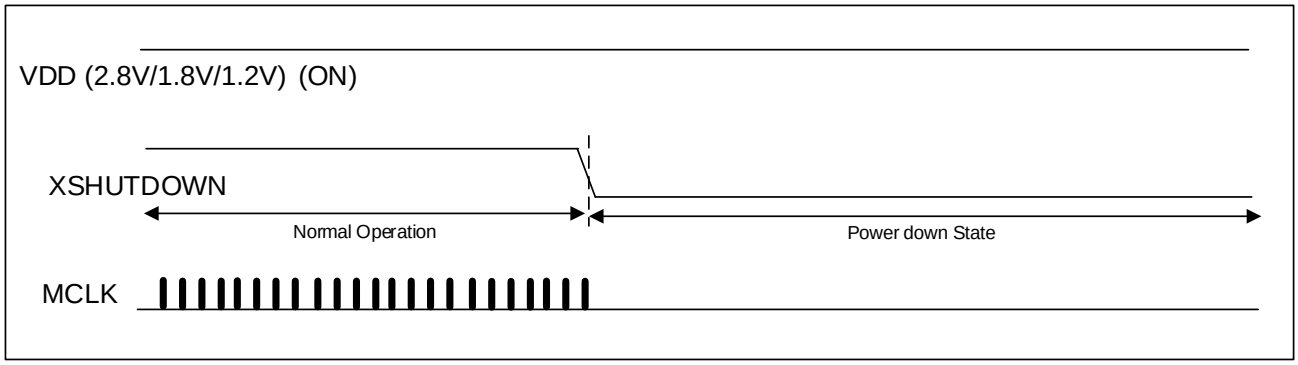
[Table 11. Timing of Power Sequence]

Constraint	Label	Min	Max	Unit
VDD_IO rising – VDD_A rising	t_0	VDD_IO, VDD_A and VDDD may rise in any order The rising separation can vary from 0ns to indefinite		ns
VDD_A rising – VDD_D rising	t_1			ns
VDD_D rising – XSHUTDOWN rising	t_2	0.0		ns
VDD_D rising – MCLK running	t_{2-1}	0.0		ns
MCLK running – XSHUTDOWN rising	t_{2-2}	0.0		ns
XSHUTDOWN rising – First I2C transaction	t_3	2400		MCLK cycles
Minimum no of EXTCLK cycles prior to the first I2C transaction. With XSHUTDOWN.	t_4	2400		MCLK cycles
D-PHY power-up	t_5	1	1.1	ms
D-PHY init	t_6	100	110	us
XSHUTDOWN falling – VDD_D falling	t_7	0.0		ns
XSHUTDOWN falling – MCLK stop	t_{7-1}	0.0		ns
MCLK stop – VDD_D falling	t_{7-2}	0.0		ns
VDD_D falling – VDD_A falling	t_8	VDD_IO, VDD_A and VDD_D may fall in any order. The falling separation can vary from 0ns to indefinite		ns
VDD_A falling – VDD_IO falling	t_9			

From Normal Operation State to Stand-by(Power down) State

When XSHUTDOWN is disabled, output pins go to Hi-Z.

<Figure 12. Timing of Normal to Stand-by>



From Stand-by(Power down) State to Normal Operation State

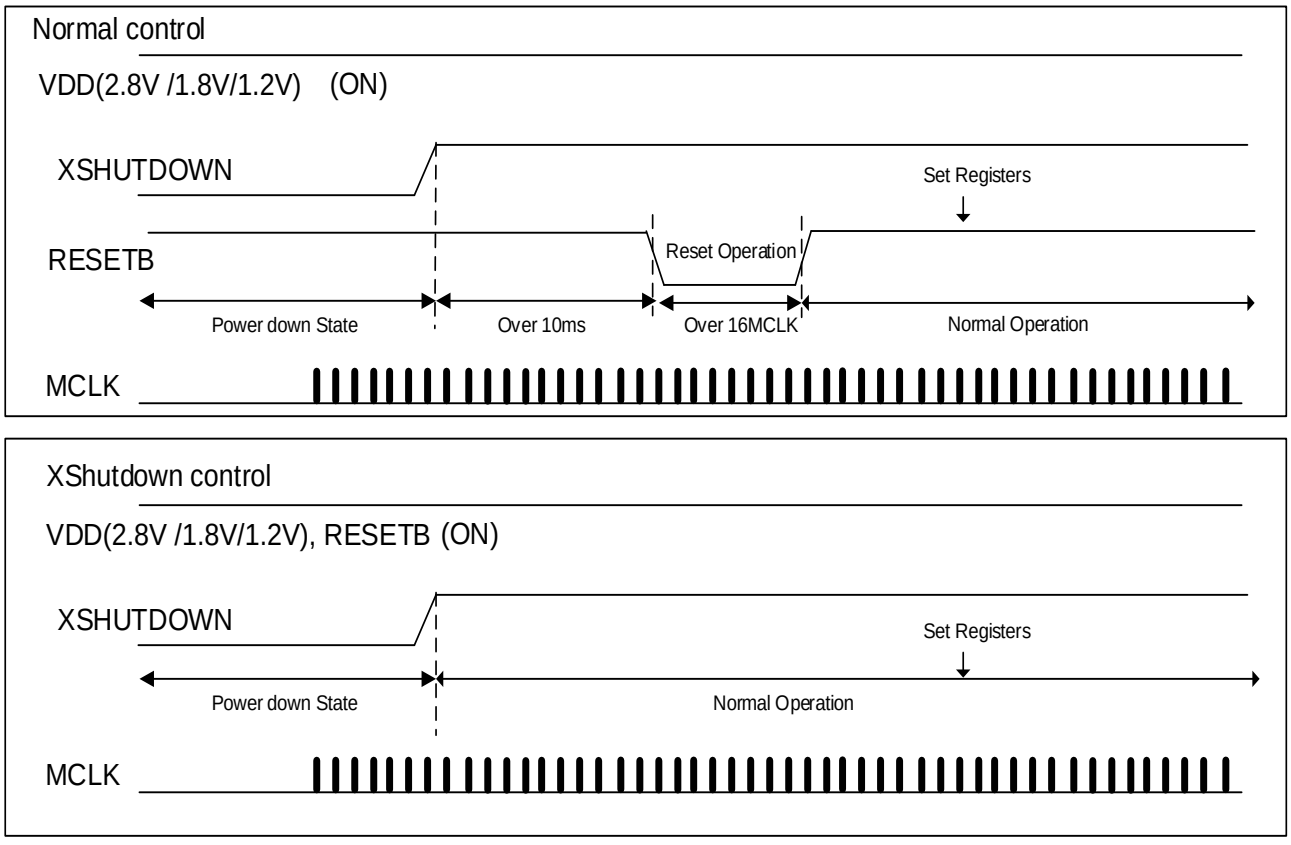
1) Set XSHUTDOWN to Hi.

2) Wait 10ms.

3) Set RESETB from Low to Hi.

4) Set the registers for normal operation

<Figure 13. Timing of Stand-by to Normal >



4.3. Black Level Calibration(BLC)

Black level is caused from pixel characteristics and analog channel offset. It makes poor image quality in dark condition and misleads color balance. To reduce these phenomenon, sensor automatically calibrates the black level every frame. The masked pixels in pixel array are used to calculate the black level.

4.4. Analog Gain Control

Global gain register (0x003A) sets the analog gain. The maximum analog gain is 16x. Table 13 shows the recommended gain settings:

[Table 12. Analog Gain Register]

Addr.	Register Name	Description	Default
0x003A 0x003B	analog_gain_code_global	Analog Gain *register value range = 0x0000 ~ 0x00F0(recommend)* $\text{Analog Gain} = \frac{Reg.value}{16} + 1$	0x00

[Table 10. Analog Gain Setting]

Register value		Gain(X)	Register value		Gain(X)
Dec	Hex		Dec	Hex	
0	0x0000	x1.0	128	0x0080	x9.0
8	0x0008	x1.5	136	0x0088	x9.5
16	0x0010	x2.0	144	0x0090	x10.0
24	0x0018	x2.5	152	0x0098	x10.5
32	0x0020	x3.0	160	0x00A0	x11.0
40	0x0028	x3.5	168	0x00A8	x11.5
48	0x0030	x4.0	176	0x00B0	x12.0
56	0x0038	x4.5	184	0x00B8	x12.5
64	0x0040	x5.0	192	0x00C0	x13.0
72	0x0048	x5.5	200	0x00C8	x13.5
80	0x0050	x6.0	208	0x00D0	x14.0
88	0x0058	x6.5	216	0x00D8	x14.5
96	0x0060	x7.0	224	0x00E0	x15.0
104	0x0068	x7.5	232	0x00E8	x15.5
112	0x0070	x8.0	240	0x00F0	x16.0
120	0x0078	x8.5			

4.5. Integration Time

The integration (exposure) time of the YACJ3B0C9SHC is controlled by the Integation time(integ_time : 0x0003, 0x0004, 0x0005) registers.

Total_integration_time = interg_time x line_length_pck x pck_clk_period

[Table 11. Integration Time Register]

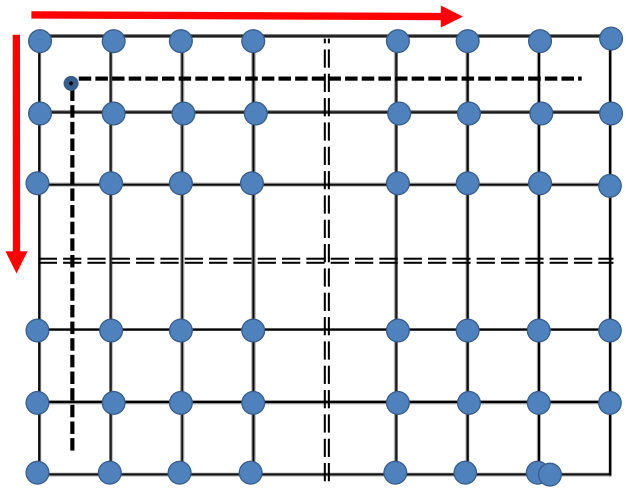
Addr.	Bit	Register Name	Description	Default
0x0002 0x0003	B[3:0]	integ_time_hw	The integration time control [19:0]	0x00
0x0004 0x0005	B[15:0]	integ_time		0x0100
0x0008 0x0009	B[15:0]	line_length_pck	Line Length [15:0]	0x0EE0

4.6. Lens Shading Correction(LSC)

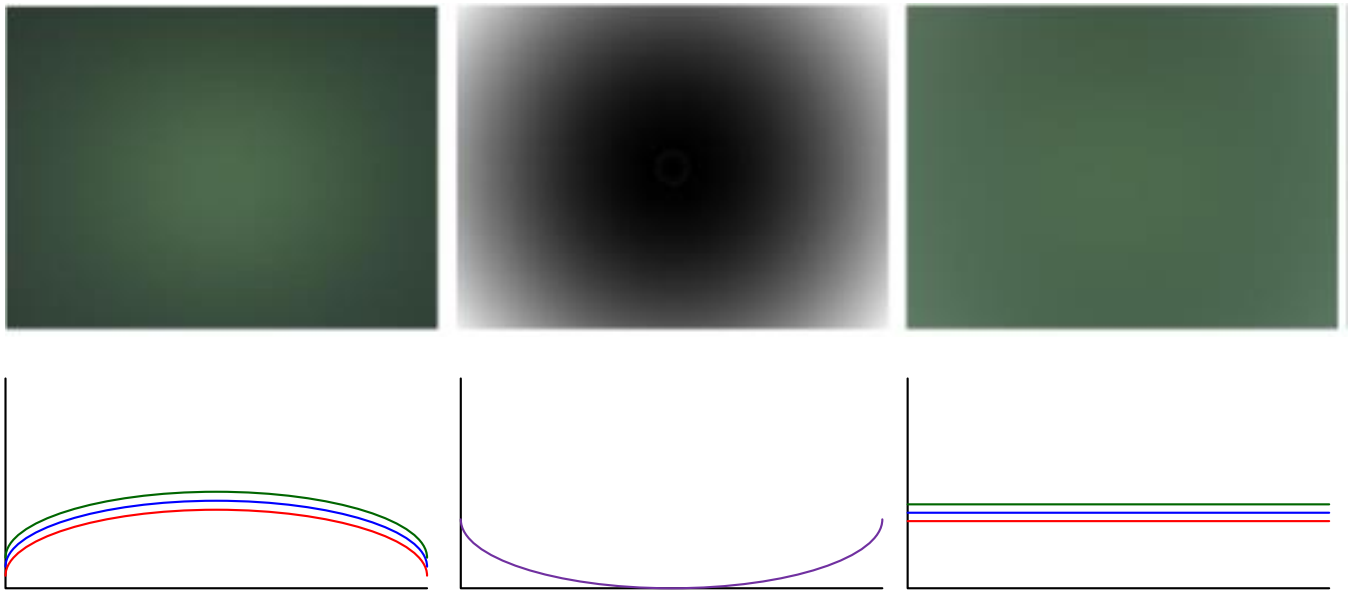
The circumstance area of pixel array does not have enough quantity of light due to optical characteristics of lens. It causes reduction of signal near peripheral of pixel array. The reduction of signal depends on both pixel' s location and color. To compensate the problem, shading correction is done by controlling the correction gain, which depends on pixel's location and color.

Shading correction changes automatically, based on the illumination type. The storages which is used for seed values are OTP or SRAM.

<Figure 14. LSC X-Y 2D interpolation>



<Figure 15. LSC Result image>



(a) Original image **(b) LSC Gain image** **(c) LSC result image**

Above Figure shows the original image, LSC gain and LSC result image.

4.7. Digital Gain Control

The digital gain processing supports both the global gain control and the separate gains control for each color channel (R, Gr, Gb, B). Each gain control register is comprised of 13bit. The bit [12:9] control the integer portion and the bit [8:0] control the decimal portion of gain (512step size). The digital gain is represented as a following equation.

$$Digital\_Gain = \left(bit[12:9] + \frac{bit[8:0]}{512} \right)$$

Each digital gain control register has a range from 0x through 15.99x.

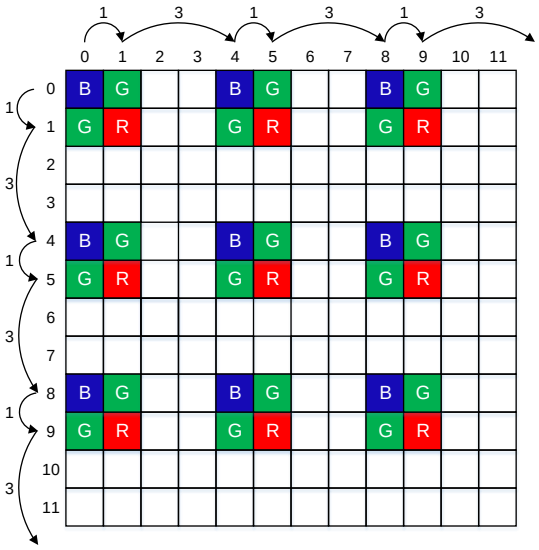
4.8. Subsampling & Binning

YACJ3B0C9SHC supports Subsampling Mode and 2x2 Binning Mode.

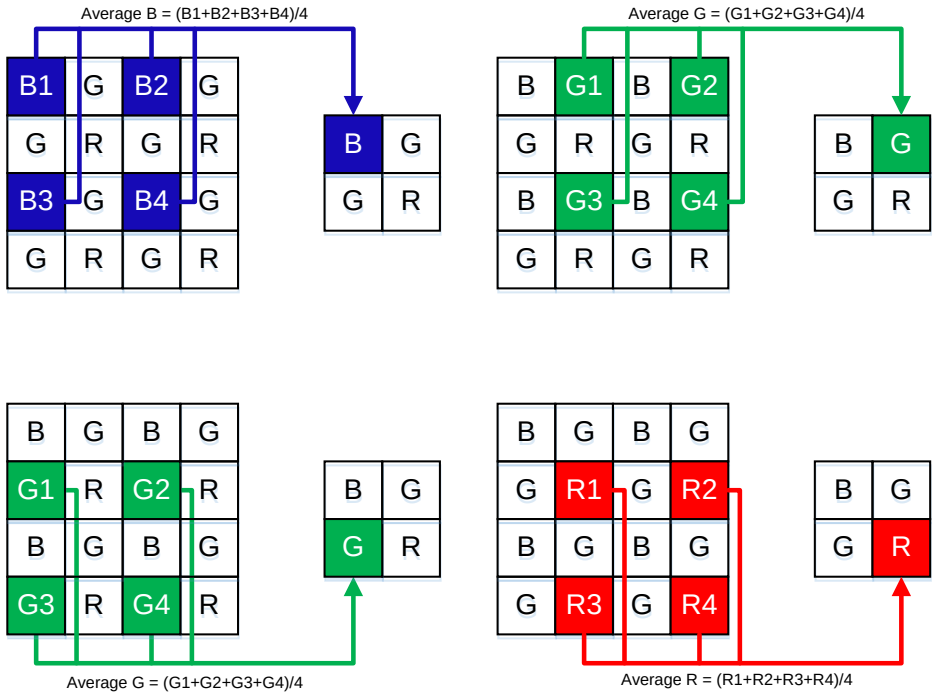
[Table 13. Subsampling and 2x2 Binning Register]

Addr.	Bit	Register Name	Description	Default
0x000C	[15:8]	binning_mode	Binning mode enable	0x00
0x001E 0x001F	[15:8]	x_odd_inc	Active x odd increase value	0x11
	[7:0]	x_even_inc	Active x even increase value	0x11
0x0032 0x0033	[15:8]	y_odd_inc_vact	Active y odd increase value	0x11
	[7:0]	y_even_inc_vact	Active y even increase value	0x11

<Figure 16. 1/2 Sub Sampling mode>



<Figure 17. 2x2 Binning mode>



4.9. Horizontal Scaling

The image scaling function within a sensor module provides a downscaling operation using Bayer data to reduce the size while covering the same angle of view of the original image. Each downscaled output pixel is calculated by taking a weighted average of input pixels which are composed of neighboring pixels. The image scaling function of the Bayer Scaler supports horizontal down to x1/2 ,x1/3, x1/4, x1/6 scale in X (Horizontal).
For example, when X scaling is enabled for a x1/2 scale factor, output image is reduced by half in X directions. This results in output image that is half of the input image size. The scaled output size is represented as a following equation depending on the scale factor.

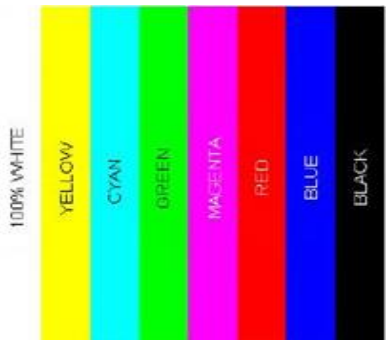
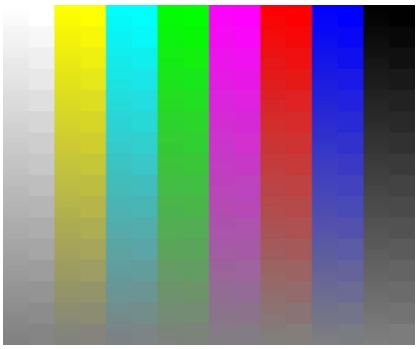
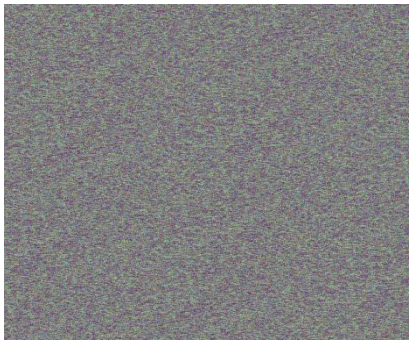
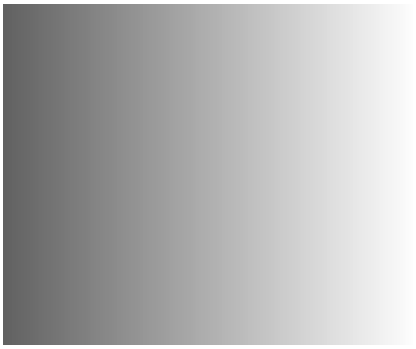
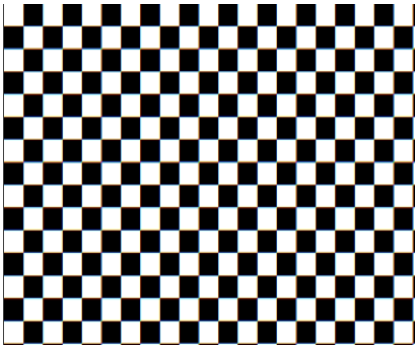
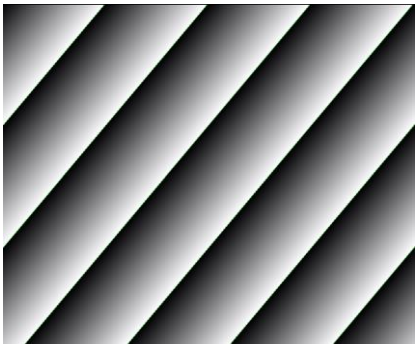
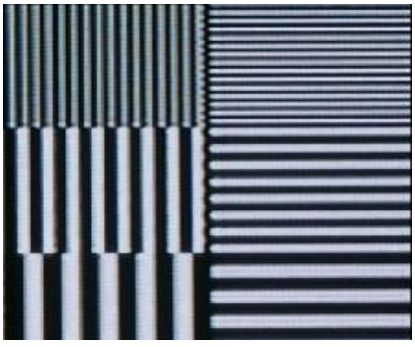
[Table 14. Horizontal Scaling Register]

Addr.	Register Name	Description	Default
0x0A0E 0x0A0F	hbin_mode	Horizontal Binning Mode [2:0] : 3'h0 – Bypass [2:0] : 3'h2 – 1/2 Horizontal binning [2:0] : 3'h3 – 1/3 Horizontal binning [2:0] : 3'h4 – 1/4 Horizontal binning [2:0] : 3'h6 – 1/6 Horizontal binning	0x00

4.10. Test Pattern Generator

For testing, we support various test patterns, such as color bar/ fade to gray color bar/ PN9 pattern etc.

<Figure 18. Test patterns>

Solid color bar	100% color bars
	
Fade to gray color bars	**PN9**
	
Horizental/Vertical gradient	**Check board**
	
Slant	**Resolution**
	

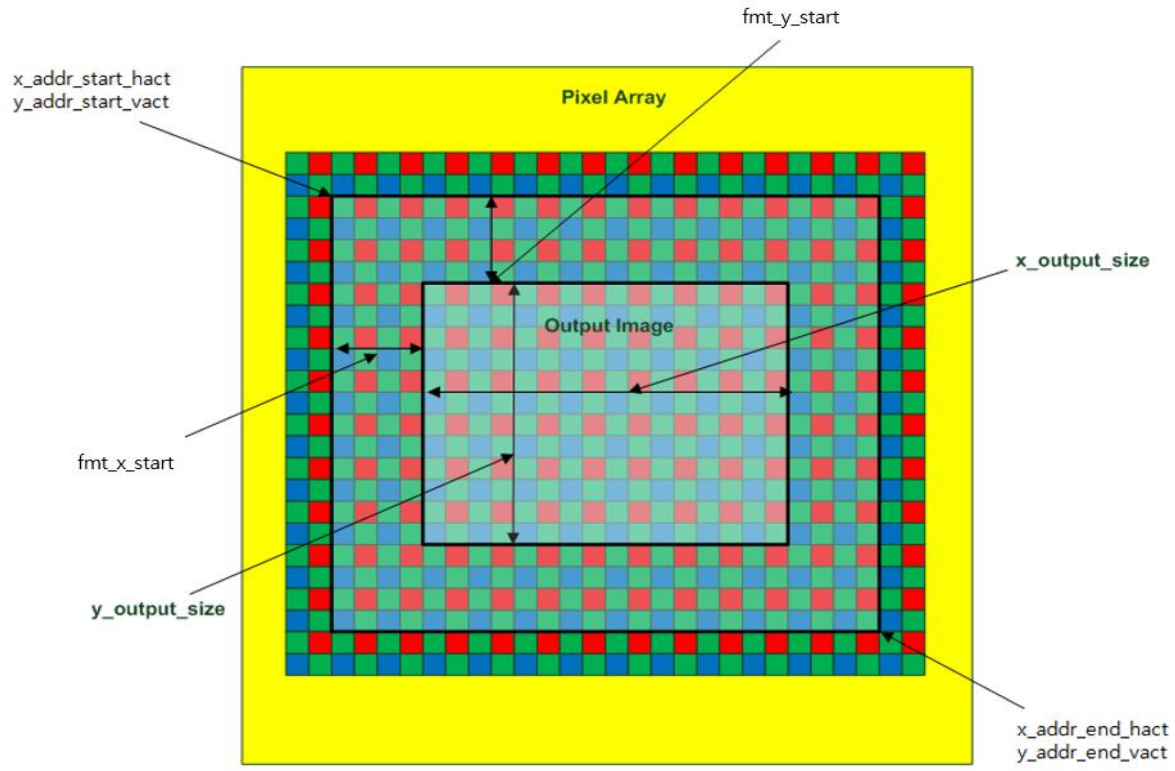
[Table 15. Test Patterns register]

Addr.	Register Name	Description	Default
0x0A04 0x0A05	isp_en_l	B[0] - Test pattern generation enable	0x0
0x020A 0x020B	test_pattern_mode	B[15:12] Reserved	0x0000
		B[11:8] Test pattern mode 0 – no pattern(default) 1 – solid colour 2 – 100% colour bars 3 – Fade to grey' colour bars 4 – PN9 5 – horizontal gradient pattern 6 – vertical gradient pattern 7 – check board 8 – slant pattern 9 – Resolution pattern 10 ~ 15 - Reserved	
		B[7:0] Reserved	

4.11. Windowing

Sensor has a rectangular pixel array 4208 X 3120. The array can be windowed by the output crop. These crop functions operate by controlling offset(start pixel point) register and cropping image size register.

<Figure 19. Output Image windowing >



[Table 16. Image Windowing Register]

Addr.	Register Name	Description	Default
0x0012	r_x_addr_start_hact_h	active x start address	0x00
0x0013	r_x_addr_start_hact_l		0x08
0x0026	r_y_addr_start_vact_h	active y start address	0x00
0x0027	r_y_addr_start_vact_l		0x40
0x0018	r_x_addr_end_hact_h	active x end address	0x10
0x0019	r_x_addr_end_hact_l		0x87
0x002C	r_y_addr_end_vact_h	active y end address	0x0C
0x002D	r_y_addr_end_vact_l		0xF7
0x0A12	r_x_output_size_h	fmt column output size	0x10
0x0A13	r_x_output_size_l		0x70
0x0A14	r_y_output_size_h	fmt row output size	0x0C
0x0A15	r_y_output_size_l		0x30
0x0804	fmt_x_start_h	column start pixel	0x00
0x0805	fmt_x_start_l		0x00
0x0806	fmt_y_start_h	row start pixel	0x00
0x0807	fmt_y_start_l		0x00

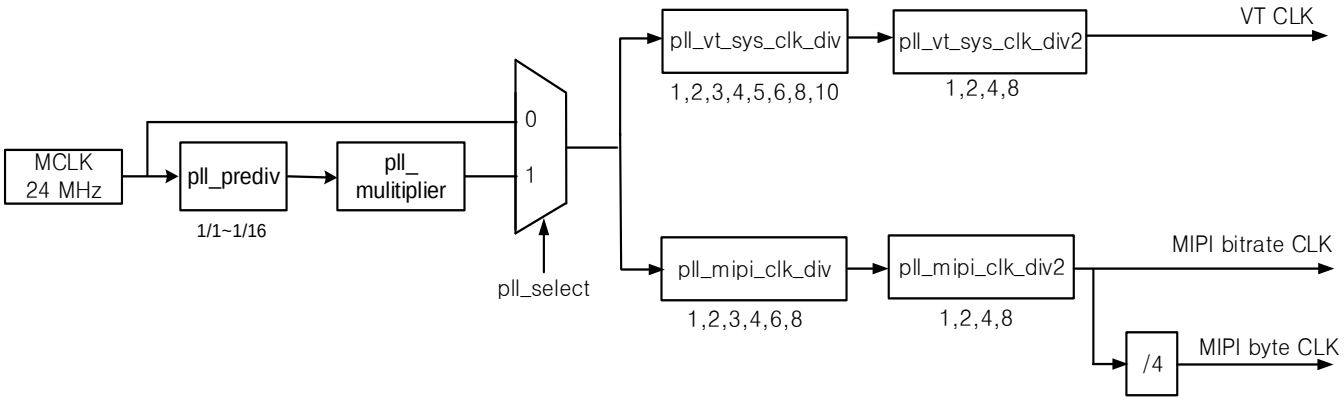
4.12. PLL

The PLL is used for clock generation for the digital block and MIPI transmitter. It consists of PFD(Phase Frequency Detector), charge pump (CP) and 2nd order loop-filter, 4-bit programmable pre-divider and 8-bit programmable multiplier. The clock generator is used for clock generation for digital part and MIPI transmitter. It consists of the divider for digital part and the divider for MIPI. The top block is shown in below Figure.

[Table 17. Register map of PLL]

Addr.	Register Name	Description	Default
0x304C	pll_static13	[15:8] : d2a_pll_mdiv [7:6] : d2a_pll_vt_sys_clk_div2 [5:2] :d2a_pll_prediv [1] : d2a_pll_reset [0] : d2a_pll_clkgen_en	0x4B 0x0A
0x404C	pll_static14	[15] : d2a_pll_clkgen_reset [14] : d2a_pll_clkgen_mipi_reset [13:11] : d2a_pll_vt_sys_clk_div [10:8] : d2a_pll_ramp_clk_div [7:5] : d2a_pll_mipi_clk_div [4:2] : d2a_pll_icp_sel [1:0] : d2a_pll_mipi_clk_div2	0xF8 0x08

<Figure 20. Block Diagram of PLL>



4.13. MIPI

YACJ3B0C9SHC supports serial data output through 1/2/4-lane MIPI(Mobile Industry Processor Interface). YACJ3B0C9SHC has four data lanes and one clock lane. The MIPI output transmitter runs up to 1.2Giga bit/sec each lane.

[Table 18. CSI lane mode register]

Addr.	Register Name	Description	Default
0x0902[7:6]	data_lane_mode	0x00 - 1 lane mode 0x01 - 2 lane mode 0x11 - 4 lane mode	0x11

The design follows CSI-2(Camera Serial Interface-2) specification. The CSI-2 specification defines standard data transmission and control interfaces between transmitter and receiver. The CSI-2 is unidirectional differential serial interface with data and clock signals; the physical layer of this interface is the "*MIPI Alliance Standard for D-PHY*". The high speed serial interface uses the following output-only signal pairs. (4 channnel data lanes and clock lane in accordance with CCP2 / MIPI specification.)

[Table 19. MIPI serial interface]

Output pin	Descrpition
DATA1_P / DATA1_N	Data lane Dp / Dn
DATA2_P / DATA2_N	
DATA3_P / DATA3_N	
DATA4_P / DATA4_N	
CLK_P / CLK_N	Clock lane Cp / Cn

The control interface (referred as CCI) is a bi-directional control interface compatible with I2C standard. YACJ3B0C9SHC supports both continuous clock behavior and non-continuous clock behavior on the clock lane. The serial interface can reduce power consumption by entering ULPS(Ultra Low Power State) mode. Each data lanes and clock lane are set to the ULPS mode when the sensor is in the hardware standby or soft standby system state.

In order to operate MIPI serial interface, sensor must set both MIPI Power enable register and TX enable register at power up and after reset. The MIPI Reset register is used to initialize MIPI operation, normally not used.

[Table 20. Timing Configuration register]

Addr.	Register Name	Description	Default
0x0915	tlpx	D-PHY spec require : 50ns	0x05
0x0916	tclk_prepare	D-PHY spec require : > 38ns, < 95ns	0x05
0x0917	tclk_zero	D-PHY spec require : tclk_prepare + tclk_go > 300ns	0x1A
0x0919	ths_prepare	D-PHY spec require : 40ns + 4UI, < 85ns + 6UI	0x05
0x091A	ths_zero_min	D-PHY spec require : ths_prepare + ths_go > 145ns + 10UI	0x0A

0x091B	ths_trail	D-PHY spec require : > MAX(8UI, 60ns + 4UI)	0x09
0x091C	tclk_post	D-PHY spec require : > 60ns + 52UI	0x0D
0x091D	tclk_trail_min	D-PHY spec require : > 60ns	0x08

Many kinds of timing constraints are specified in the D-PHY specification. In order to satisfy this specifications, user needs to adjust timing value to control analog block. Registers from 0x0915 to 0x091D are used for this purpose. If you change the clock operating speed, reconfigulate registers.

4.14. Frame structure

Frame Structure is controlled by Line length pck, frame length lines, x_addr_start, y_addr_start, x_addr_end and y_addr_end.

Frame length lines control

1. Frame length lines are controlled by 0x0006, 0x0007 at full readout mode.

Line length pcks control

1. Line length pcks are controlled by 0x0008, 0x0009 at full readout mode.
2. Minimum line length pck

-. normal,sub-sampling : 600

Visible pixel data size control

1. Visible pixel width is controlled by x_addr_start [0x0012, 0x0013], x_addr_end [0x0018, 0x0019], y_addr_start [0x0026, 0x0027], y_addr_end[0x002C, 0x002D] .

-. Visible pixel width = x_addr_end – x_addr_start + 1

-. Visible pixel height = y_addr_end – y_addr_start + 1

Blank time control

1. Line blank time

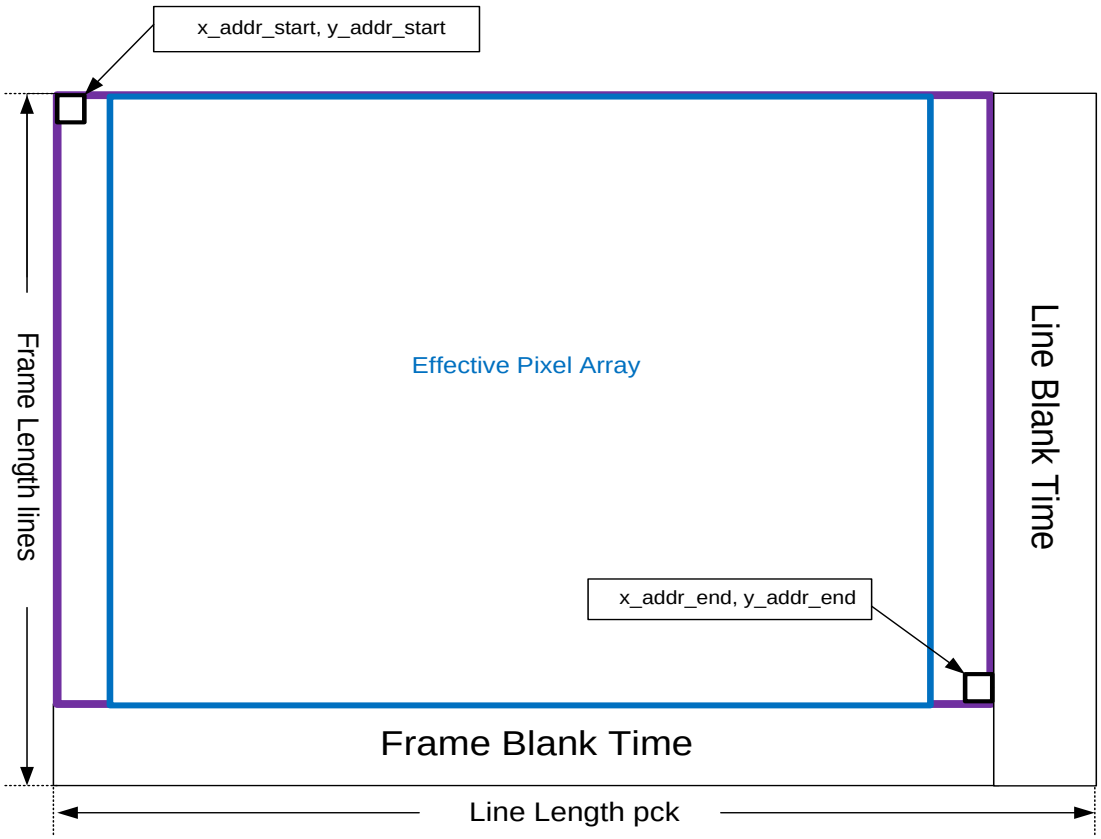
-. Line blank time = line length pck – visible pixel width

2. Frame blank time

-. Frame blank time = frame length lines – visible pixel height

-. Minimum blank time : 45 lines

<Figure 21. Frame Structure>



4.15. Line-interlaced long-short output for HDR

High dynamic range (HDR) technology delivers better image quality and brighter, truer colors by accurately representing the wide range of intensity levels found in direct sunlight and in the deepest shadows.

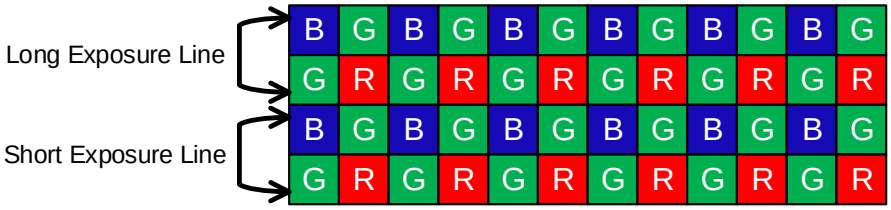
Line-interlaced long-short output for HDR, dual exposure HDR that not only improves the dynamic range, but also reduces motion artifacts and eliminates frame buffer requirements without compromising frame resolution or speed.

In HDR mode, the exposure is still controlled by a rolling shutter. However, the frame data is separated into “long exposure” and “short exposure” in every two rows. Long exposure time is controlled by registers 0x0003, 0x0004 and 0x0005. Short exposure time is controlled by registers 0x0053, 0x0054 and 0x0055.

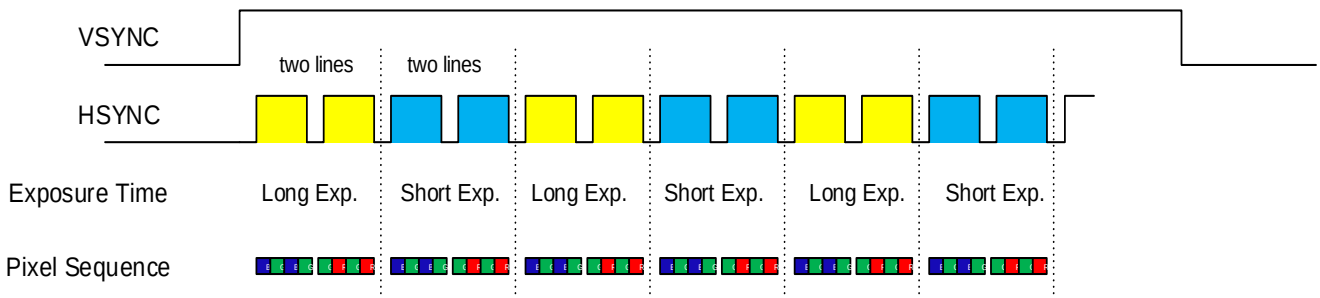
[Table 21. HDR control registers]

Addr.	Register Name	Description	Default
0x004D	hdr_en	hdr_en[0] HDR mode enable	0x00
0x0003	integ_time_hw	{ integ_time_hw[3:0], integ_time_h[7:0], integ_time_l[7:0] } → 20bit integration time for HDR mode (Long)	0x00
0x0004	integ_time_h		0x01
0x0005	integ_time_l		0x00
0x0053	integ_time_s_hw	{ integ_time_s_hw[3:0], integ_time_s_h[7:0], integ_time_s_l[7:0] } → 20bit integration time for HDR mode (Short)	0x00
0x0054	integ_time_s_h		0x01
0x0055	integ_time_s_l		0x00

<Figure 22. HDR Pixel Sequence>



<Figure 23. HDR Output Timming>



4.16. Fixed Frame Rate Timing

There are two kinds of frame rate. One is fixed frame rate and another is variable frame rate. Fixed frame rate mode can be enabled when 0x003C[0] bit is asserted. If fixed frame rate mode is enabled, maximum coarse integration time(0x0003, 0x0004, 0x0005) is (frame length – 6).

And variable frame rate mode can be enabled when 0x003C[0] bit is de-asserted. In variable frame rate mode, frame length is changed automatically according to coarse integration time. Specific frame length lines according to coarse integration time can be calculated by below formula.

If (coarse_integration_time < (frame_length-6))

Frame length = Register setting value of frame length lines

else

Frame length = coarse integration time + 6

And frame time can be calculated by below formula.

Frame time = (line length pck) x (frame length) x VT_CLK_period.

[Table 22. Frame Time Calculation]

Fixed Frame Time

If (Coarse_Integration_Time < Coarse_Integration_Time_Min)
➔ Coarse_Integration_Time = 6
Else if (Coarse_Integration_Time > Frame_length – 6(Coarse_Integration_Time _Max_Margin))
➔ Coarse_Integration_Time = Frame_Length - 6
Else
➔ Coarse_Integration_Time = Coarse_Integration_Time

Variable Frame Time

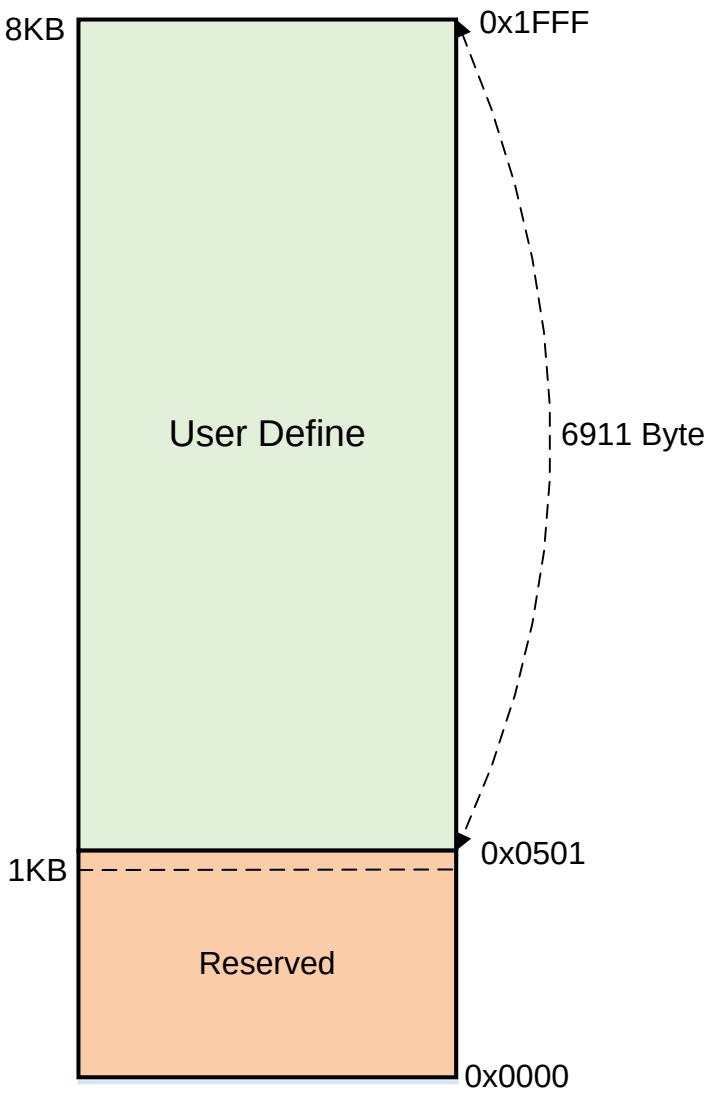
If (Coarse_Integration_Time < Coarse_Integration_Time_Min)
➔ Coarse_Integration_Time = Min_Coarse_Integration_Time
Else
➔ Coarse_Integration_Time = Coarse_Integration_Time
 	
If (Coarse_Integration_Time ≤ Frame_length – 6(Coarse_Integration_Time _Max_Margin))
➔ Frame_Length = Frame_Length
Else
➔ Frame_Length = Coarse_Integration_Time + 6(Coarse_Integration_Time _Max_Margin)

4.17. OTP Memory Map

The YACJ3B0C9SHC features 8KByte of OTP (one time programmable) memory, individual moduel and sensor specific information. The user may program which set to be used. OTP can be accessed via two-wire serial interface.

If user want to get more information, please contact to SKhynix FAE engineer or refer to sererate OTP guide documents.

<Figure 24. OTP Memory Map>



5. REGISTER DESCRIPTION

Notification

SKhynix doesn't have any responsibility or liability for any failures if using reserved register addresses.

[Table 23. Register Description]

Address (Hex)	Register	Description	Default (Hex)	Renewal Frame
		TG Registers		
0x0000	image_orient	Image orientation	0x00	Next
0x0002	frame_length_lines_hw	Frame Length high word	0x00	Next
0x0003	coarse_integ_time	The integration time control { integ_time_hw[3:0], integ_time_h [7:0], integ_time_l [7:0] } → 20bit @integration time for HDR mode (Long)	0x00	Next
0x0004			0x01	Next
0x0005			0x00	Next
0x0006	frame_length_lines	Frame Length	0x0C	Next
0x0007			0x98	Next
0x0008	line_length_pck	Line Length	0x02	Next
0x0009			0x6C	Next
0x000C	binning_mode	Binning mode enable	0x00	Next
0x000D			0x00	Next
0x0012	x_addr_start	active x start address	0x00	Next
0x0013			0x08	Next
0x0018	x_addr_end	active x end address	0x10	Next
0x0019			0x87	Next
0x001E	x_odd_inc	Active x odd increase value	0x11	Next
0x001F	x_even_inc	Active x even increase value	0x11	Next
0x0026	y_addr_start	active y start address	0x00	Next
0x0027			0x40	Next
0x002C	y_addr_endt	active y end address	0x0C	Next
0x002D			0xF7	Next
0x002E	y_odd_inc_fobp	Frame obp y odd increase value	0x11	Next
0x002F	y_even_inc_fobp	Frame obp y even increase value	0x11	Next
0x0032	y_odd_inc_vact	Active y odd increase value	0x11	Next
0x0033	y_even_inc_vact	Active y even increase value	0x11	Next
0x003A	analog_gain_code_global	Analog Gain	0x00	Next
0x003B			0x00	Next
0x003D	image_orient	Image orientation	0x00	Next
0x0046	r_grouped_para_hold	Grouped parameter hold	0x00	Next
0x004C	tg_enable	TG enable	0x00	Current

0x004D	hdr_en	HDR mode enable	0x00	Next
0x0053	integ_time_s_hw	{ integ_time_s_hw[3:0], integ_time_s_h[7:0], integ_time_s_l[7:0] } → 20bit integration time for HDR mode (Short)	0x00	Next
0x0054	integ_time_s_h		0x01	Next
0x0055	integ_time_s_l		0x00	Next
OTP Registers				
0x0702	otp_cmd	OTP command for read/write	0x00	Current
0x0706	otp_wdata	OTP write data	0x00	Current
0x0708	otp_rdata	OTP read data	0x00	Current
0x070A	otp_addr	OTP write/read address	0x00	Current
0x070B			0x00	Current
Test Pattern Registers				
0x020A	test_pattern_mode	Test Pattern mode	0x00	Next
0x020C	test_data_red	The test data used to replace red pixel data	0x00	Next
0x020D			0x00	Next
0x020E	test_data_greenR	The test data used to replace green pixel data on rows that also have red pixels	0x00	Next
0x020F			0x00	Next
0x0210	test_data_blue	The test data used to replaced blue pixel data	0x00	Next
0x0211			0x00	Next
0x0212	tetst_data_greenB	The test data used to replaced green pixel data on rows that also have blue pixels	0x00	Next
0x0213			0x00	Next
0x0214	horizontal_cursor_width	Defines the width of the horizontal cursor(in pixels)	0x00	Next
0x0215			0x00	Next
0x0216	horizontal_cursor_position	Defines the top edge of the horizontal cursor	0x00	Next
0x0217			0x00	Next
0x0218	vertical_cursor_width	Defines the width of the vertical cursor(in pixels)	0x00	Next
0x0219			0x00	Next
0x021A	vertical_cursor_position	Defines the left hand edge of the vertical cursor. A value of 0xFFFF switches the vertical cursor into automatic mode where it automatic mode where it automatically advances every frame.	0x00	Next
0x021B			0x00	Next
Digital Gain Registers				
0x0508	dgain_gr	Digital Gr gain control (0 ~ 15.99x)	0x02	Next
0x0509			0x00	Next
0x050A	dgain_gb	Digital Gb gain control (0 ~ 15.99x)	0x02	Next
0x050B			0x00	Next
0x050C	dgain_r	Digital R gain control (0 ~ 15.99x)	0x02	Next
0x050D			0x00	Next
0x050E	dgain_b	Digital B gain control (0 ~ 15.99x)	0x02	Next
0x050F			0x00	Next

Formatter Control Registers				
0x0804	x_start_h	column start pixel (high byte)	0x00	Next
0x0805	x_start_l	column start pixel (low byte)	0x00	Next
0x0806	y_start_h	row start pixel (high byte)	0x00	Next
0x0807	y_start_l	row start pixel (low byte)	0x00	Next
MIPI Control Registers				
0x0902	MIPI_tx_op_mode	MIPI operating mode	0xC3	Current
0x0915	tlpx	length of any Low-Power state period.	0x05	Current
0x0916	tclk_prepare	time to drive LP-00 to prepare for HS clock transmission	0x05	Current
0x0917	tclk_zero	time for lead HS-0 drive period before starting clock.zero	0x1A	Current
0x0919	ths_prepare	time to drive LP-00 before starting the HS transmission on a Data Lane.	0x05	Current
0x091A	ths_zero	time to send HS-0, i.e. turn on the line termination and drive the interconnect with the HS driver, prior to sending the SoT Sync sequence.	0x0A	Current
0x091B	ths_trail	time the transmitter must drive the flipped last data bit after sending the last payload data bit of a HS transmission burst.	0x09	Current
0x091C	tclk_post	time that the transmitter	0x0D	Current
0x091D	tclk_trail_min	the time to drive HS differential state after last layload clock bit of a HS transmission burst.	0x08	Current
ISP Common Registers				
0x0A00	mode_sel	streaming mode	0x00	Current
0x0A02	fast_standby_mode	fast standby mode	0x00	Current
0x0A04	isp_en	Isp enable h B[0] – MIPI enable	0x01	Current
0x0A05		Isp enable l B[0] – TPG enable B[1] – ADPC enable B[2] – LSC enable B[3] – DGA enable B[5] – Hscaler enable B[6] – FMT enable	0x40	Current
0x0A10	data_pedestal	data pedestal value	0x40	Current
0x0A11	pedestal_en	Pedestal enable	0x00	Current
Window Registers				
0x0A12	x_output_size	Formatter column output size	0x10	Next
0x0A13			0x70	Next
0x0A14	y_output_size	Formatter row output size	0x0C	Next
0x0A15			0x30	Next
Horizontal Scale Register				
0x0A0F	hbin_mode	Horizontal Scale Mode	0x00	Next
BLC Control Registers				
0x0C00	blc_ctl1	BLC enable	0x8C	Current
PAD Control				
0x0D00	drvst_fsync	driving strength of FSYNC IO.	0x07	Current

0x0D01	drvst_sda	driving strength of SDA	0x07	Current
0x0D02	drvst_strobe	driving strength of STROBE	0x07	Current
System Control Registers				
0x0F02	pll_cfg1	pll enable	0x00	Current
0x0F03	pll_cfg2	pll_lock_time control	0x06	Current
0x0F14	sensor_id	I2C slave address 0x20 @ 7bit 0x40 @ 8bit	0x20	Current
0x0F16	model_id_hi	mode ID high byte	0x32	RO
0x0F17	model_id_lo	model ID low byte	0x13	RO

5.1. TG Control Registers

0x0000: image_orientation [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:10]		Reserved	0000_00b
B[9]	V_flip	Vertical Flip Enable [0: no flip, 1: Vertical Flip]. Image orientation need to change reg. 0x0000 and 0x003C.	0b
B[8]	H_mirror	Horizontal Mirror Enable [0: no mirror, 1: Horizontal Mirror]. Image orientation need to change reg. 0x0000 and 0x003C.	0b
B[7:0]		Reserved	

0x0002: coarse_integration_time_hw [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	
B[7:0]	coarse_integration_time_hw	The coarse integration time control	0000_0000b

0x0004: coarse_integration_time [default=0x0100, r/w]

Bit	Function	Description	Default
B[15:8]	coarse_integration_time	The coarse integration time control	0000_0001b
B[7:0]			0000_0000b

0x0006: frame_length_lines [default=0x0C98, r/w]

Bit	Function	Description	Default
B[15:8]	frame_length_lines	Frame length (Units : lines)	0000_1100b
B[7:0]			1001_1000b

0x0008: line_length_pck [default=0x02, r/w]

Bit	Function	Description	Default
B[15:8]	line_length_pck	Line length pck	0000_0010b
B[7:0]			0110_1100b

0x000C: binning_mode [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	binning_mode	0 - None 1 – enabled	0b
B[7:0]		Reserved	0000_0000b

0x0012: x_addr_start [default=0x0008, r/w]

Bit	Function	Description	Default
B[15:8]	x_addr_start	x start address	0000_0000b
B[7:0]			0000_1000b

0x0018: x_addr_ end [default=0x1087, r/w]

Bit	Function	Description	Default
B[15:8]	x_addr_ end	x end address	0001_0000b
B[7:0]			1000_0111b

0x001E: x_odd_inc [default=0x1101, r/w]

Bit	Function	Description	Default
B[15:8]	x_odd_inc	Increment for odd pixels in the readout order	0001_0001b
B[7:0]			0001_0001b

0x0026: y_addr_start [default=0x0040, r/w]

Bit	Function	Description	Default
B[15:8]	y_addr_start	y start address	0000_0000b
B[7:0]			0100_0000b

0x002C: y_addr_ end [default=0x0CF7, r/w]

Bit	Function	Description	Default
B[15:8]	y_addr_ end	y end address	0000_1100b
B[7:0]			1111_0111b

0x002E: y_odd_inc_fobp [default=0x1111, r/w]

Bit	Function	Description	Default
B[15:8]	y_odd_inc_fob	Increment for frame obp odd lines in the readout order	0001_0001b
B[7:0]	p		0001_0001b

0x0032: y_odd_inc_vact [default=0x1111, r/w]

Bit	Function	Description	Default
B[15:8]	y_odd_inc	Increment for odd lines in the readout order	0001_0001b
B[7:0]	_vact		0001_0001b

0x003A: analog_gain_code_global [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	Analog_gain_ code_global	Reserved	0000_0000b
B[7:0]		Global Analogue Gain Code	0000_0000b

0x003C: image_orientation [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:2]		Reserved	0000_00b
B[1]	V_flip	Vertical Flip Enable [0: no flip, 1: Vertical Flip]. Image orientation need to change reg. 0x0000 and 0x003C.	0b
B[0]	H_mirror	Horizontal Mirror Enable [0: no mirror, 1: Horizontal Mirror]. Image orientation need to change reg. 0x0000 and 0x003C.	0b

0x0046: grouped_para_hold [default=0x00, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	grouped_para _hold	grouped parameter hold Set to envelope a series of parameter changes as a group of changes that should be made so as to effect the output stream on the same frame boundary	0b
B[7:0]		Reserved	0000_0000b

0x004C: tg_enable [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	tg_enable	0 : tg_disable 1 : tg_enable	0b
B[7:1]		Reserved	0000_000b
B[0]	hdr_en	0 : HDR Mode disable 1 : HDR Mode enable	0b

0x0052: integration_time_s_hw [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	0000_0000b
B[7:0]	integration_time_s_hw	The integration time for HDR mode (Short) < Related reg. 0x0054, 0x0055 >	0000_0000b

0x0054: integration_time_s_h [default=0x01, r/w]

Bit	Function	Description	Default
B[15:8]	integration_time_s	The integration time for HDR mode (Short) – < Related reg. 0x0053, 0x0055 >	0000_0001b
B[7:0]			0000_0000b

5.2. OTP

0x0702: otp_cmd [default=0x00, r/w]

Bit	Function	Description	Default
B[7:2]		Reserved	0000_00b
B[1]	otp_write_cmd	Continuous write	0b
B[0]	otp_read_cmd	Continuous read	0b

0x0706: otp_wdata [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	otp_wdata	OTP write data	0000_0000b

0x0708: otp_rdata [default=0x00, r/o]

Bit	Function	Description	Default
B[7:0]	otp_rdata	OTP read data	0000_0000b

0x070A: otp_addr [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	otp_addr	OTP write/read address high	0000_0000b

0x070B: otp_addr_l [default=0x00, r/w]

Bit	Function	Description	Default
B[7:0]	otp_addr_l	OTP write/read address low	0000_0000b

5.3. TPG

0x020A: test_pattern_mode [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:12]		Reserved	0000b
B[11:8]	Test_pattern_mode	Test pattern mode 0 – no pattern(default) 1 – solid colour 2 – 100% colour bars 3 – Fade to grey' colour bars 4 – PN9 5 – horizontal gradient pattern 6 – vertical gradient pattern 7 – check board 8 – slant pattern 9 – resolution pattern 10 ~ 255 - Reserved	0000b
B[7:0]		Reserved	0000_0000b

0x020C: test_data_red [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	test_data_red	The test data used to replace red pixel data	0000_0000b
B[7:0]			0000_0000b

0x020E: test_data_greenR [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	test_data_greenR	The test data used to replace greenR pixel data	0000_0000b
B[7:0]			0000_0000b

0x0210: test_data_blue [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	test_data_blue	The test data used to replace blue pixel data	0000_0000b
B[7:0]			0000_0000b

0x0212: test_data_greenB [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	test_data_greenB	The test data used to replace greenB pixel data	0000_0000b
B[7:0]			0000_0000b

0x0214: horizontal_cursor_width [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	Horizontal_cursor_width	Defines the width of the horizontal cursor(in pixels)	0000_0000b
B[7:0]			0000_0000b

0x0216: horizontal_cursor_position [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	Horizontal_cursor_position	Defines the top edge of the horizontal cursor	0000_0000b
B[7:0]			0000_0000b

0x0218: vertical_cursor_width [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	Vertical_cursor_width	Defines the width of the vertical cursor(in pixels)	0000_0000b
B[7:0]			0000_0000b

0x021A: vertical_cursor_position [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	Vertical_cursor_position	Defines the left hand edge of the vertical cursor. A value of 0xFFFF switches the vertical cursor into automatic mode where it automatic mode where it automatically advances every frame.	0000_0000b
B[7:0]			0000_0000b

5.4. Digital Gain

0x0508: digital_gain_gr [default=0x0200, r/w]

Bit	Function	Description	Default
B[15:13]	digital_gain_gr	Reserved	0000b
B[12:8]		Digital gain for Gr channel (high byte [12:0])	0010b
B[7:0]			0000_0000b

0x050A: digital_gain_gb [default=0x0200, r/w]

Bit	Function	Description	Default
B[15:13]	Digital_gain_greenB	Reserved	0000b
B[12:8]		Digital gain for Gb channel (high byte [12:0])	0010b
B[7:0]			0000_0000b

0x050C: digital_gain_r [default=0x0200, r/w]

Bit	Function	Description	Default
B[15:13]	Digital_gain_r	Reserved	0000b
B[12:8]		Digital gain for R channel (high byte [12:8])	0010b
B[7:0]			0000_0000b

0x050E: digital_gain_b [default=0x0200, r/w]

Bit	Function	Description	Default
B[15:13]	Digital_gain_b	Reserved	0000b
B[12:8]		Digital gain for B channel (high byte [12:8])	0010b
B[7:0]			0000_0000b

5.5. FORMATTER

0x0804: X_START [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	X_START	Column start pixel	0000_0000b
B[7:0]			0000_0000b

0x0806: Y_START [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]	Y_START	Row start pixel	0000_0000b
B[7:0]			0000_0000b

5.6. MIPI

0x0902:MIPI_tx_op_mode [default=0xC300, r/w]

Bit	Function	Description	Default
B[15:14]	Lane Mode	MIPI lane mode 00 : 1 lane mode 01 : 2 lane mode 11 : 4 lane mode	11b
B[13]	Data Format	MIPI data format 0 : RAW10 mode 1 : RAW8 mode	0b
B[12]	Line synchronization	Line synchronization enable 1 : MIPI line start/end pachet on 0 : MIPI line start/end packet off	0b
B[11]	MIPI line number	MIPI line number enable 1 : MIPI line number on 0 : MIPI line number off	0b
B[10]	MIPI frame number	MIPI frame number enable 1 : MIPI frame number on 0 : MIPI frame number off	0b
B[9]	MIPI clock mode	MIPI clock mode selection 0:non-continuous clock mode 1:continuous clock mode	1b
B[8]	MIPI frame number	MIPI frame count reset 0 : MIPI frame count reset off 1 : MIPI frame count reset on	1b
B[7:0]		Reseved	0000_0000b

0x0914: tlpx [default=0x0005, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	
B[7:0]	Tlpx	Tlpx is the length of any Low-Power state period	0000_0101b

0x0916: tclk_prepare [default=0x051A, r/w]

Bit	Function	Description	Default
B[15:8]	Tclk_prepare	Tclk prepare is the time to drive LP-00 to prepare for HS clock transmission.	0000_0101b
B[7:0]	Tclk_zero	Tclk zero is the time for lead HS-0 drive period before starting clock	0001_1010b

0x0919: ths_prepare [default=0x05, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	
B[7:0]	Ths_prepare	Ths prepare is the time to drive LP-00 before starting the HS transmission on a Data Lane.	0000_0101b

0x091A: ths_zero [default=0x0A09, r/w]

Bit	Function	Description	Default
B[15:8]	Ths_zero	Ths zero minimum is the time to send HS-0, i.e. turn on the line termination and drive the interconnect with the HS driver, prior to sending the SoT Sync sequence	0000_1010b
B[7:0]	Ths_trail	Ths trail is the time the transmitter must drive the flipped last data bit after sending the last payload data bit of a HS transmission burst. This time is required by the receiver to determine EoT.	0000_1001b

0x091C: tclk_post [default=0x0D08, r/w]

Bit	Function	Description	Default
B[15:8]	Tclk_post	Time that the transmitter shall continue sending HS clock after the last associated data lane has transitioned to LP mode. Host will control that suitable value is used	0000_1101b
B[7:0]	Tclk_trail_min	Tclk trail minimum is the time to drive HS differential state after last layload clock bit of a HS transmission burst.	0000_1000b

5.7. ISP Common

0x0A00: mode_sel [default=0x00, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	0000_000b
B[8]	mode_sel	1 – streaming 0 – sw_standby	0b
B[7:0]		Reserved	0000_0000b

0x0A02: fast_standby_mode [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	0000_000b
B[8]	fast_standby_mode	1 – Fast standby mode (enable mode change from streaming mode to sw standby mode at line blank) 0 – Normal standby mode	0b
B[7:0]		Reserved	0000_0000b

0x0A04: isp_en [default=0x0140, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	0000_000b
B[8]	mipi enable	MIPI enable	1b
B[7]		Reserved	0b
B[6]	fmt enable	Formatter enable	1b
B[5]	H scaler enable	Horizontal scaler enable	0b
B[4]		Reserved	0b
B[3]	dga enable	Digital gain enable	0b
B[2]	lsc enable	Lense shading correction enable	0b
B[1]	adpc enable	adpc enable	0b
B[0]	tpg enable	Test pattern generation enable	0b

0x0A10: data_pedestal [default=0x4000, r/w]

Bit	Function	Description	Default
B[15:8]	data_pedestal	data pedestal value	0100_0000b
B[7:4]		Reserved	0000b
B[3]	DGA_pedestal_en	Digital Gain Pedestal enble	0b
B[2]	LSC pedestal_en	LSC Pedestal enble	0b
B[1:0]		Reserved	00b

5.8. Window

0x0A12: x_output_size [default=0x1070, r/w]

Bit	Function	Description	Default
B[15:8]	x_output_size	Formatter column output size	0001_0000b
B[7:0]			0111_0000b

0x0A14: y_output_size [default=0x0C30, r/w]

Bit	Function	Description	Default
B[15:8]	y_output_size	Formatter row output size	0000_1100b
B[7:0]			0011_0000b

5.9. Horizontal SCALER

0x0A0E: hbin_mode [default=0x0000, r/w]

Bit	Function	Description	Default
B[15:8]		Reserved	0000_0000b
B[7:3]		Reserved	0000_0b
B[2:0]	X Scale Ratio	Downscale ratio of X dimension 3'h6 : 1/6 scale 3'h4 : 1/4 scale 3'h3 : 1/3 scale 3'h2 : 1/2 scale 3'h0 : Bypass	000b

5.10. BLC

0x0C00: blc_ctl0 [default=0x8C00, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	1000_110b
B[8]	en_blc	BLC enable	0b
B[7:0]		Reseved	0000_0000b

5.11. PAD CTRL

0x0D00: drvst_fsync [default=0x0707, r/w]

Bit	Function	Description	Default
B[15:11]		Reserved	0000_0b
B[10:8]	drvst_fsync	driving strength of FSYNC IO.	111b

B[7:3]		Reserved	0000_0b
B[2:0]	**drvst_sda**	driving strength of SDA	111b

0x0D02: drvst_strobe [default=0x0700, r/w]

Bit	Function	Description	Default
B[15:11]		Reserved	0000_0b
B[10:8]	**drvst_strobe**	driving strength of STROBE	111b
B[7:0]		Reserved	0000_000b

5.12. SMU

0x0F02: pll_cfg1 [default=0x0006, r/w]

Bit	Function	Description	Default
B[15:9]		Reserved	0000_000b
B[8]	**pll_cfg1**	0 – pll bypass 1 – pll enable	0b
B[7:0]	**pll_cfg2**	pll lock time = pll_cfg2[7:0] * 256 cycle * MCLK period	0000_0110b

0x0F14: sensor_id [default=0x2000, r/w]

Bit	Function	Description	Default
B[15:8]	**sensor_id**	I2C slave address 0x20 @ 7bit 0x40 @ 8bit	0010_0000b
B[7:0]		Reserved	0000_0000b

0x0F16: model_id [default=0x3213, r/o]

Bit	Function	Description	Default
B[15:8]	**model_id**	Sensor model ID higher byte (MSB)	0011_0010b
B[7:0]			0001_0011b

5.13. PLL

0x304C: [default=0x4B0B, r/w]

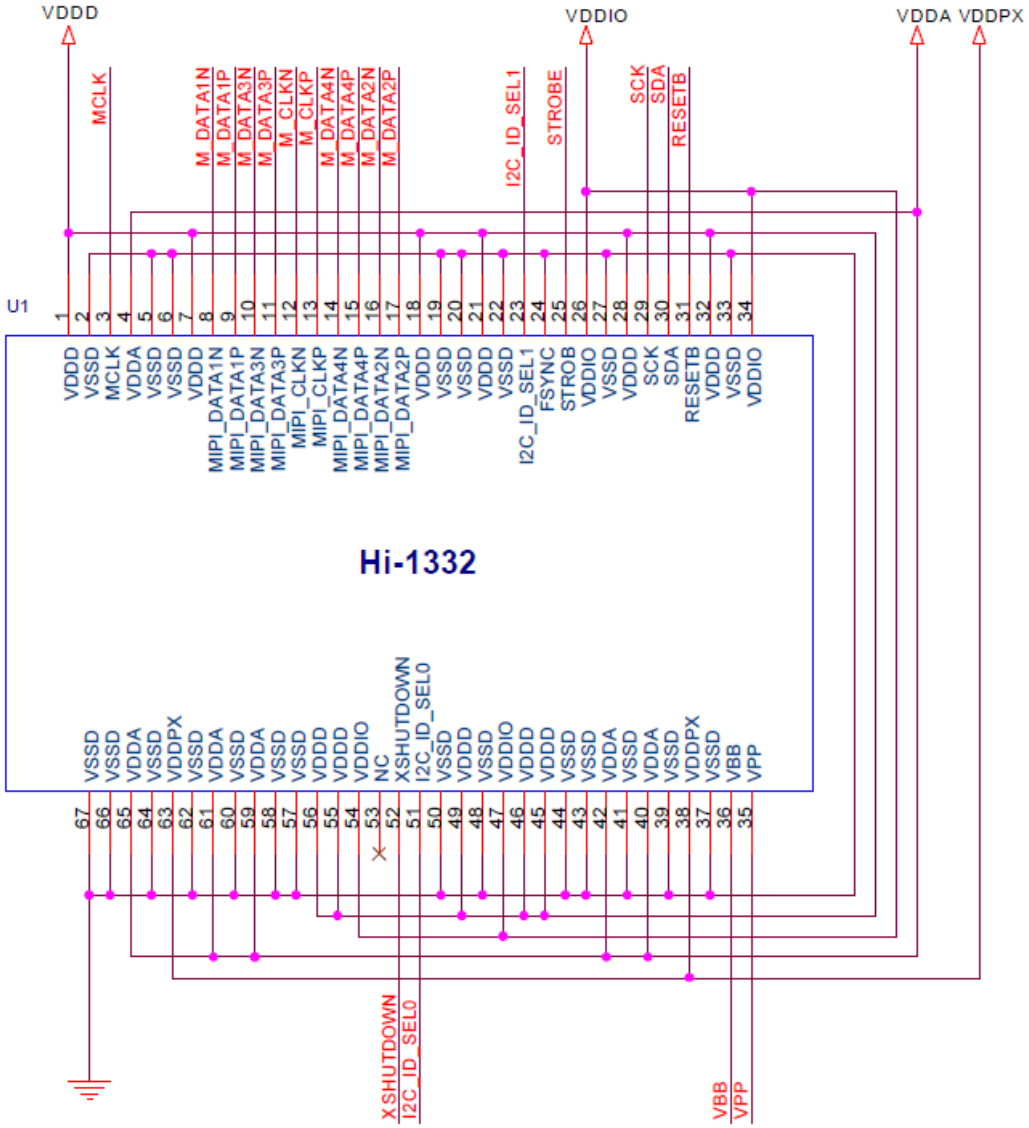
Bit	Function	Description	Default
B[15:8]	**M-DIV ratio**	Set M-divier dividing ratio 00010000 : 16 to 11111111: 255	01001011b
B[7:6]	**VT SYS CLK DIV2 ratio**	Set VT_SYS CLK divider 2 dividing ratio 00: /1 01: /2 10: /4 11: /8	00b
B[5:2]	**PRE-DIV ratio**	Set Pre-divider dividing ratio 0000 : 1/1, 0001 : 1/2, 0010 : 1/3, 0011 : 1/4, 0100 : 1/5, 0101 : 1/6, 0110 : 1/7, 0111 : 1/8 1000 : 1/9, 1001 : 1/10, 1010 : 1/11, 1011 : 1/12, 1100 : 1/13, 1101 : 1/14, 1110 : 1/15, 1111 : 1/16	0010b
B[1]	**PLL reset**	Reset PLL block 0 : RESET 1 : SET	1b
B[0]	**CLKGEN enable**	Enable CLKGEN block 0 : DISABLE 1 : ENABLE	0b

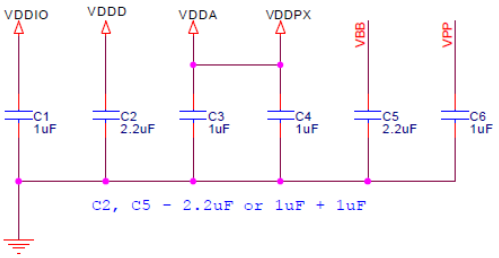
0x404C: [default=0xF808, r/w]

Bit	Function	Description	Default
B[15]	**CLKGEN reset**	Reset CLKGEN block 0 : RESET 1 : SET	1b
B[14]	**CLKGEN MIPI reset**	Reset MIPI CLKGEN block 0 : RESET 1 : SET	1b
B[13:11]	**VT SYS CLK DIV ratio**	Set VT_SYS CLK divider dividing ratio 000 : /1 001 : /2 010 : /3 011 : /4 100 : /5 101 : /6 110 : /8 111 : /10	111b
B[10:8]	**RAMP CLK DIV ratio**	Set RAMP CLK divider dividing ratio 000 : /1 001 : /2 010 : /3 011 : /4 100 : /5 101 : /6	000b
B[7:5]	**MIPI CLK DIV ratio**	Set MIPI CLK divider dividing ratio 000 : /1 001 : /2 010 : /3 011 : /4 100 : /6 101 : /8	000b
B[4:2]	**Icp sel**	Set CHARGE PUMP current 000 : 0 uA 001 : 5 uA 010 : 10 uA 011 : 15 uA 100 : 20 uA 101 : 25 uA 110 : 30 uA 111 : 35 uA	010b
B[1:0]	**MIPI CLK DIV2 ratio**	Set MIPI CLK divider 2 dividing ratio 00 : /1 01 : /2 10 : /4 11 : /8	00b

6. Reference Module Schematic

<Figure 25. Module Schematic>





Power supply
VDDIO : 1.8V or 2.8V
VDDA, VDDPX : 2.8V
VDDD : 1.2V

I2C Slave address

PAD	Input	I2C Slave address
#51 (I2C_ID_SEL0) #23 (I2C_ID_SEL1)	Low(GND) Low(GND)	W 0x40@8bit/R 0x41@8bit
#51 (I2C_ID_SEL0) #23 (I2C_ID_SEL1)	Low(GND) High(VDDIO)	W 0x44@8bit/R 0x45@8bit
#51 (I2C_ID_SEL0) #23 (I2C_ID_SEL1)	High(VDDIO) Low(GND)	W 0x42@8bit/R 0x43@8bit
#51 (I2C_ID_SEL0) #23 (I2C_ID_SEL1)	High(VDDIO) High(VDDIO)	W 0x46@8bit/R 0x47@8bit

Sensor control

PAD	Normal Control	X-Shutdown Control
X-SHUTDOWN (PAD #52)	Connect to AP GPIO	Connect to AP GPIO
RESETB (PAD #31)	Connect to AP GPIO	Connect to VDDIO

Note :
If user does not want to control RESETB(Use Only X-SHUTDOWN Pin) the RESETB Should be connect to VDDIO

7. Spectral Response

To be determinded.