Preliminary

Specification of

YACG4D0C9SHC

[Rev. 0.1]

1/4” 8M Pixel

CMOS Image Sensor

[Hi-846]

Revision History

Version	Date	Comments
0.0	2016/07/08	YACG4D0C9SHC(Hi-846) Datasheet is released (Preliminary)
0.1	2016/09/13	Register description change (Preliminary)

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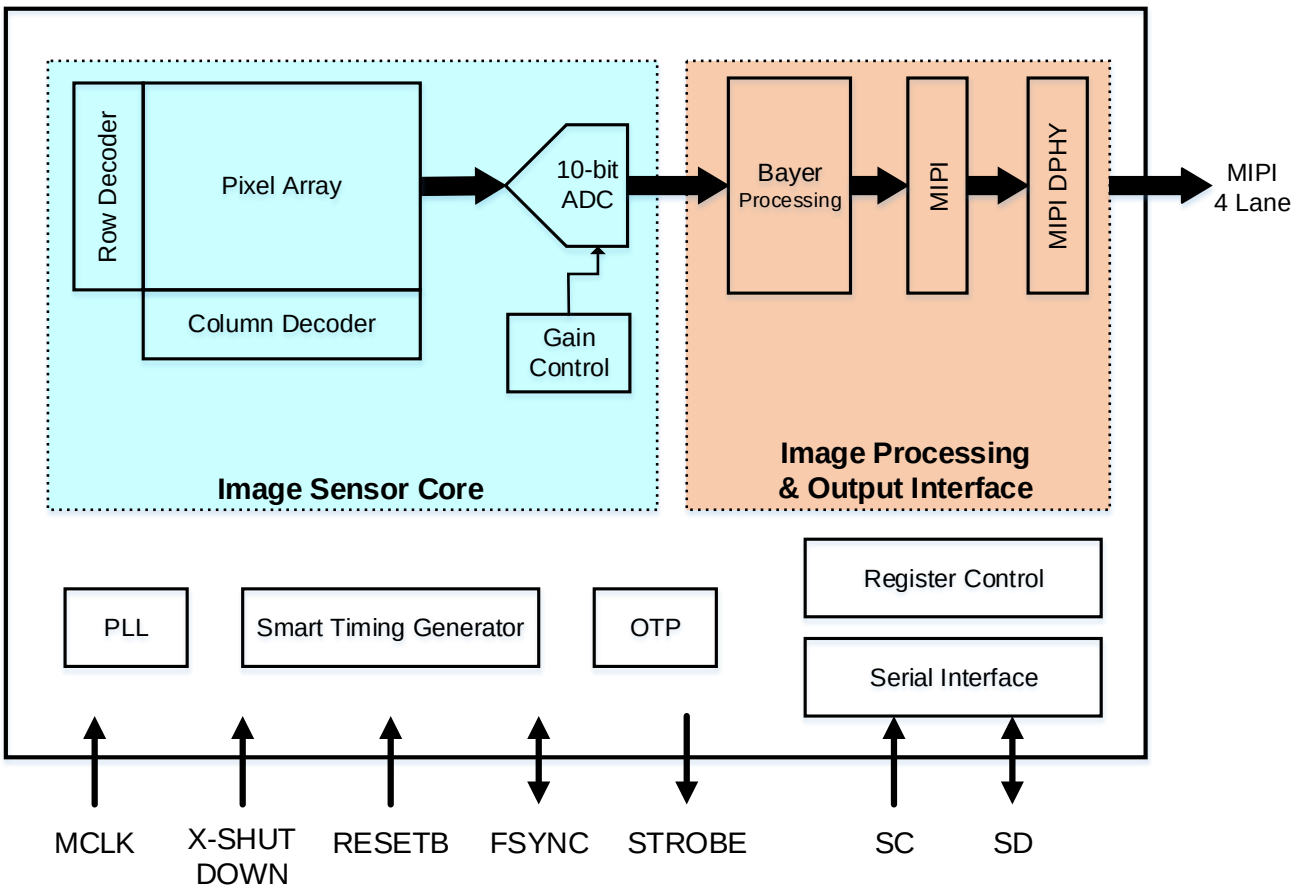
1. OVERVIEW

1.1. Description

YACG4D0C9SHC is a high quality 8mega-pixel single chip CMOS image sensor for mobile phone camera applications and digital still camera products.

YACG4D0C9SHC incorporates a 3264 x 2448 pixel array, on-chip 10-bit ADC and an image signal processor. Unique sensor technology enhances image quality by reducing FPN (Fixed Pattern Noise), horizontal/vertical line noise and random noise.

<Figure 1. Block Diagram>



1.2. Applications

- Mobile Phone Camera / Digital Still Camera
- PC Camera / Video Conference

1.3. Key Features

- Pixel Size : 1.12um X 1.12um, BSI
- Effective Image Size : 3673.60um (H) X 2759.68um(V) (3280 X2464)
- Resolution : 3,264H X 2,448V
- Color Filter : RGB Bayer
- Optical Format : 1/4 inch
- Frame Rate : 30fps@ QUXGA
  60fps@ Full HD 1080P(Crop)
  90fps@ HD 720P
- Power Supply : Analog : 2.8V @VDDA
  IO : 1.8V / 2.8V @VDDI
  Digital : 1.2V @VDDD
- Power Consumption : TBD mW@ 30fps, QUXGA
  TBD mW@ 60fps, FHD 1080P(Crop)
  TBD mW@ 90fps, HD 720P
- ADC : 10bit
- PLL : On Chip
- Operation Temperature: -20 ~ 60°C
- Master Clock : 10 ~ 27MHz
- Output Format : RGB Bayer 10
- Windowing : Programmable
- Host Interface : two-wire serial bus interface
- Sub-Sample : 1/2, 1/4
- Image Flip : X/Y Flip
- Black Level Calibration
- Analog gain control : x1~x16
- Digital gain control : x1 ~ x15.99, (1/512 step)
- Built-in test pattern generation
- Internal PLL for high speed clock generation
- MIPI 4-Lane (Max 720Mbps on each lane)
- MIPI 2-Lane (Max 1.44Gbps on each lane)
- Standby mode for power saving
- 8KB OTP Memory
- Flash Strobe Control : Support Xenon / LED Type
- On-chip Defect correction for couplets & Clusters
- Line-interlaced long-short output for iHDR (inter-line HDR)
- 2D Lens Shading Correction

2. Electrical characteristics

2.1. Key Features

[Table 1. DC Characteristics]

Item	Symbol	Min	Typ	Max	Unit	Note
Digital Core Circuit Power Supply Voltage	$V_{DD:D}$	1.15	1.2	1.3	V	
Analog Circuit Power Supply Voltage	$V_{DD:A}$	2.7	2.8	3.0	V	
Digital I/O Circuit Power Supply Voltage	$V_{DD:I}$	1.7/2.7	1.8/2.8	2.0/3.0	V	1
H level Input Voltage	V_{IH}	0.7 * $V_{DD:I}$			V	
L level Input Voltage	V_{IL}			0.3 * $V_{DD:I}$	V	

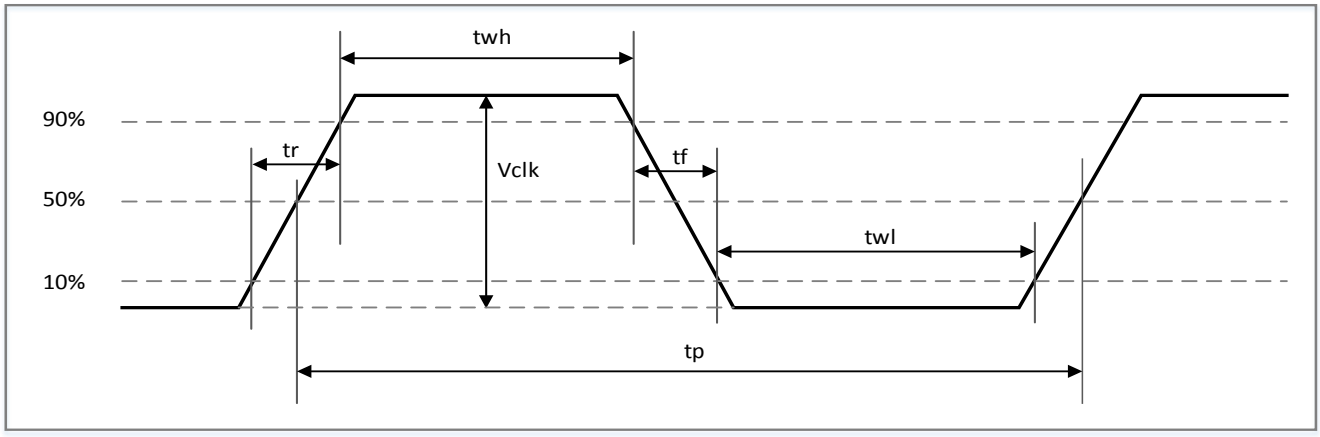
Note1) VDD:I Typical voltage 1.8V (min 1.7V, max 2.0V)
VDD:I Typical voltage 2.8V (min 2.7V, max 3.0V)

[Table 2. Temperature Characteristics]

Item	Symbol	Rating	Unit	Note
Storage Temperature	T_{STR}	-40 ~ 80	°C	
Functional Operating Temperature	T_{FUN}	-20 ~ 60	°C	Camera fully functional

2.1.1. Master Clock Waveform Specification

<Figure 2. Master Clock Waveform Diagram>



[Table 3. Master Clock Characteristics]

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Frequency	MCLK	10	24	27	Mhz
MCLK Amplitude	Vclk	1.7/2.6	1.8/2.8	1.9/3.0	V
MCLK duty cycle	twh/twl	0.45*Tp	0.5*Tp	0.55*Tp	ns
MCLK Clock Period	Tp	37.03	41.66	100	ns
MCLK Rise/Fail Time	tr/tf			10	ns
MCLK Jitter(Peak-to-Peak)	Tjitter			600	ps

2.1.2. Power Consumption

[Table 4. Power Consumption]

Item	Condition		Min	Typ	Max	Unit	Note
Full@30fps	$V_{DD:A}$ &$V_{DD:P}$=2.8V			TBD		mA	1
	$V_{DD:D}$=1.2V			TBD		mA	
	$V_{DD:I}$	1.8V		TBD		mA	2
		2.8V		TBD		mA	
FHD 1080P@60fps (Crop)	$V_{DD:A}$ &$V_{DD:P}$=2.8V			TBD		mA	1
	$V_{DD:D}$=1.2V			TBD		mA	
	$V_{DD:I}$	1.8V		TBD		mA	2
		2.8V		TBD		mA	
HD 720P@90fps	$V_{DD:A}$ &$V_{DD:P}$=2.8V			TBD		mA	1
	$V_{DD:D}$=1.2V			TBD		mA	
	$V_{DD:I}$	1.8V		TBD		mA	2
		2.8V		TBD		mA	
Stand by Current				TBD		uA	3

Note1) Because current of analog circuit depends on the registers' values, it is measured at specific register's value .
Note2) Because power consumption of VDD:I depends on the output load and system environment, users should supply enough current to sensor for stable operation. It is measured when output load is floated.
Note3) Standby current is measured at XSHUTDOWN = LO and MCLK = LO.
We recommend that power should be turned off, when low standby power consumption is required

2.2. MIPI Features

[Table 5. HS Transmitter DC Specifications]

Parameter	Description	Min	Typ	Max	Unit
VCMTX	HS transmit static common-mode voltage	150	200	250	mV
|△VCMTX(1,0) |	VCMTX mismatch when Differential-1 or Differential-0			5	mV
| VOD |	HS transmit differential voltage	140	200	270	mV
|△VOD |	VOD mismatch when Differential-1 or Differential-0			10	mV
VOHHS	HS output high voltage			360	mV
ZOS	Single ended output impedance	40	50	62.5	Ω
△ZOS	Single ended output impedance mismatch			10	%

[Table 6. HS Transmitter AC Specifications]

Parameter	Description	Min	Typ	Max	Unit
△VCMTX(HF)	Common-level variation above 450MHz			15	mVRMS
△VCMTX(LF)	Common-level variations between 50-450MHz			25	mVPEAK
tR and tF	20% ~ 80% rise time and fall time			0.3	UI
		150			ps

[Table 7. LP Transmitter DC Specifications]

Parameter	Description	Min	Typ	Max	Unit
VOH	Thevenin output high level	1.1	1.2	1.3	V
VOL	Thevenin output low level	-50		50	mV
ZOLP	Output impedance of LP transmitter	110			Ω

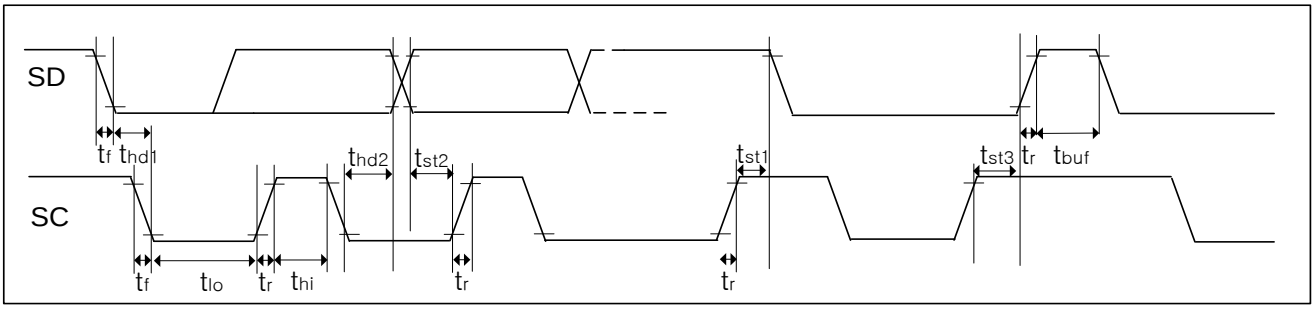
[Table 8. LP Transmitter AC Specifications]

Parameter	Description		Min	Typ	Max	Unit
TRLP/TFLP	15%~85% rise time and fall time				25	ns
TREOT	30%~85% rise time and fall time				35	ns
TLP-PULSE-TX	Pulse width of the LP exclusive – OR clock	First LP exclusive – OR clock pulse after Stop state or last pulse before Stop state	40			ns
		All other pulses	20			ns
TLP-PER-TX	Period of the LP LP exclusive – OR clock		90			ns
δV/δtSR	Slew rate @ CLOAD = 0pF		30		500	mV/ns
	Slew rate @ CLOAD = 20pF		30		150	mV/ns
	Slew rate @ CLOAD =70pF		30		100	mV/ns
CLOAD	Load capacitance		0		70	pF

3. Two-Wire Serial Bus Interface

3.1. Timing Specifications

<Figure 3. AC Timing of Two Wire Serial Bus>



[Table 9. AC Characteristics of Two Wire Serial Bus]

Parameter	Symbol	Min.	Typ.	Max.	Unit
SC frequency	f_{sck}	100		400	KHz
SC low period	t_{lo}	1.3		-	us
SC high period	t_{hi}	0.6		-	us
SC setup time for START condition	t_{st1}	0.6		-	us
SC setup time for STOP condition	t_{st3}	0.6		-	us
SC hold time for START condition	t_{hd1}	0.6		-	us
SD setup time	t_{st2}	0.6		-	us
SD hold time	t_{hd2}	0		-	us
Bus free time Between STOP and START condition	t_{buf}	1.3		-	us
Rising time of both SD and SC	t_r	-		0.3	us
Falling time of both SD and SC	t_f	-		0.3	us
Capacitive load of SC/SD	C_b	-		100	pF
Pull-up resistor on SC and SD			1.5		kΩ

3.2. Bus Operation

The two-wire serial bus interface is used to write and read the required data into registers in this sensor. Sensor can operate as a slave device only. The two-wire serial bus interface is controlled by SD (serial data) and SC (serial clock). SD is bidirectional bus. Operation has single byte programming and multiple byte programming. Users doesn't need to set continuously register address on programming multiple byte because the sensor increases register address automatically. This will reduce time to program registers.

Following figures show write and read operations.

Note) Before programming the two-wire serial bus interface, MCLK and RESETB, XSHUTDOWN should be supplied.

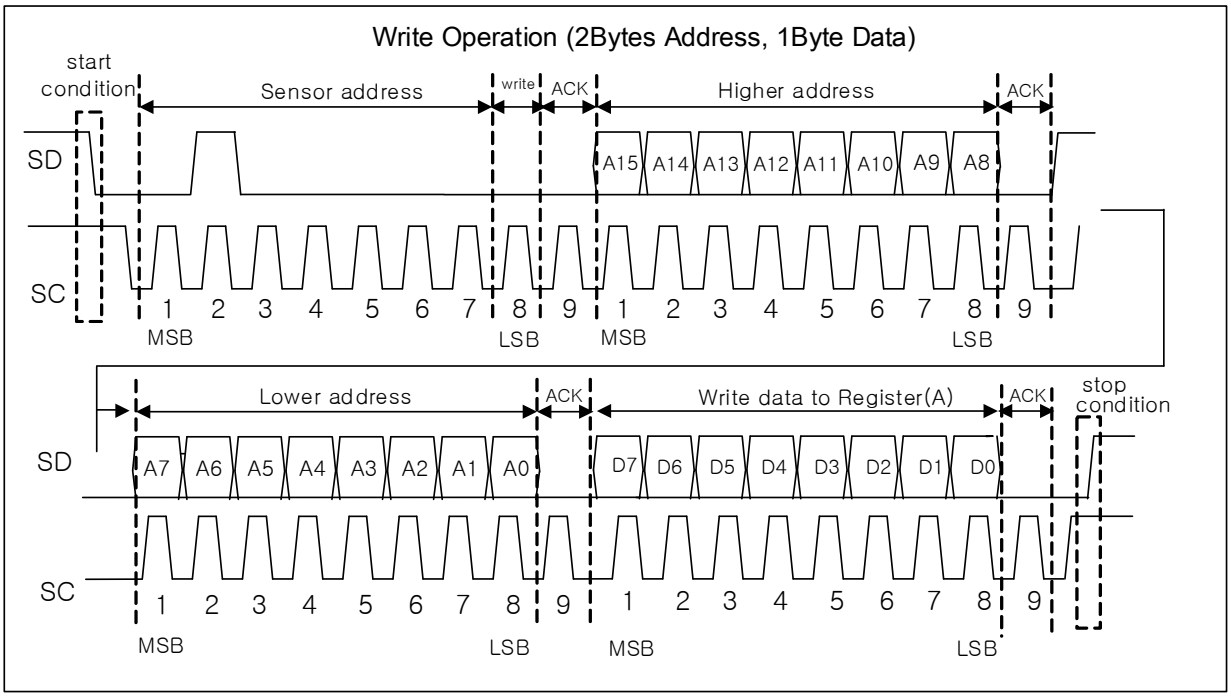
In YACG4D0C9SHC, Slave address is controlled by the I2C_ID_SEL0(pad #15) and I2C_ID_SEL1 (pad #29) pads.

[Table 10. Slave address setting]

Slave address(@ 8bit)	I2C_ID_SEL0	I2C_ID_SEL1
W : 0x40 / R : 0x41	Low(default)	Low(default)
W : 0x44 / R : 0x45	Low	High
W : 0x42 / R : 0x43	High	Low
W : 0x46 / R : 0x47	High	High

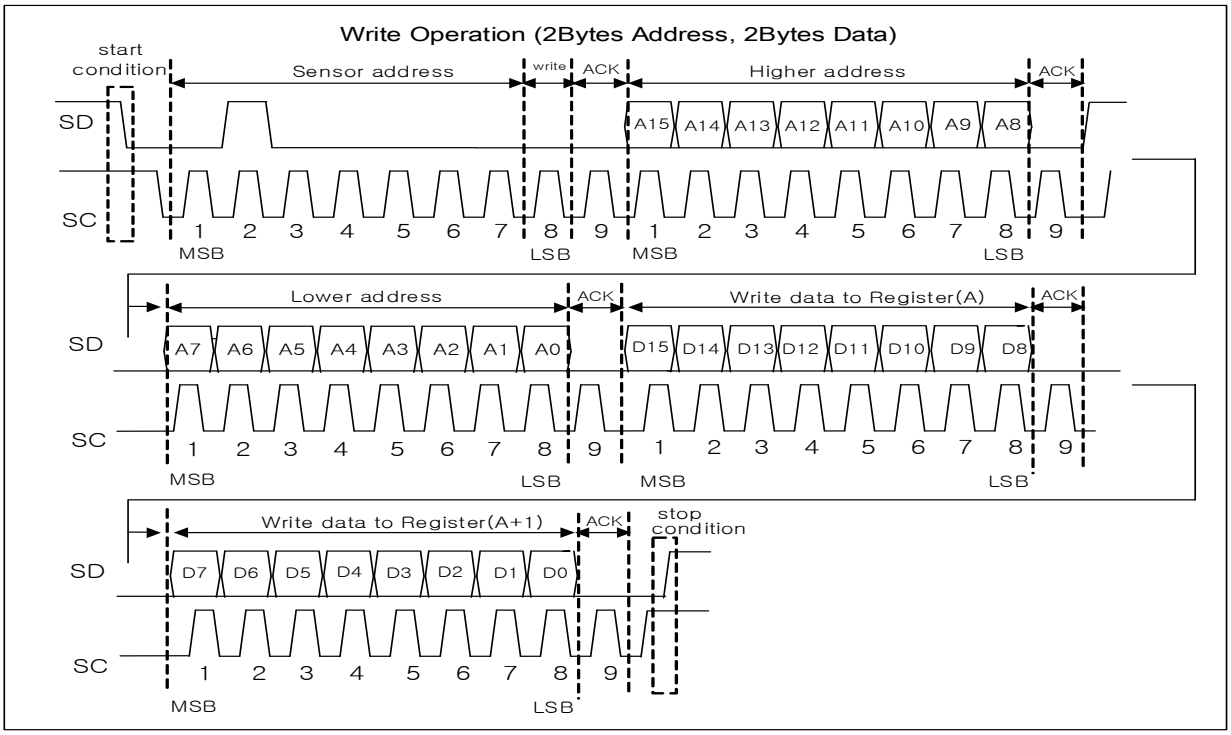
3.2.1. Write Operation (2 bytes address – 1byte data format)

<Figure 4. Write Operation through Two Wire Serial Bus>



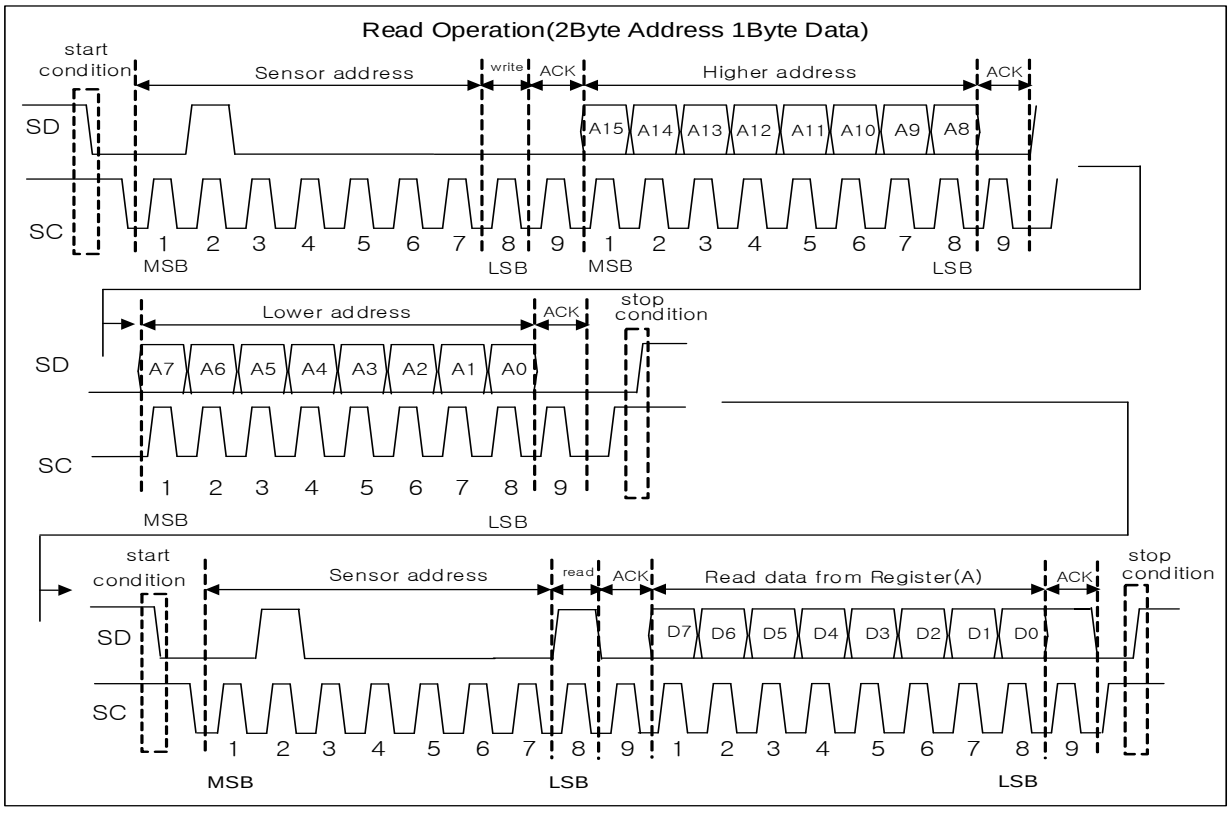
3.2.2. Write Operation (2 bytes address – 2byte data format)

<Figure 5. Write Operation through Two Wire Serial Bus>



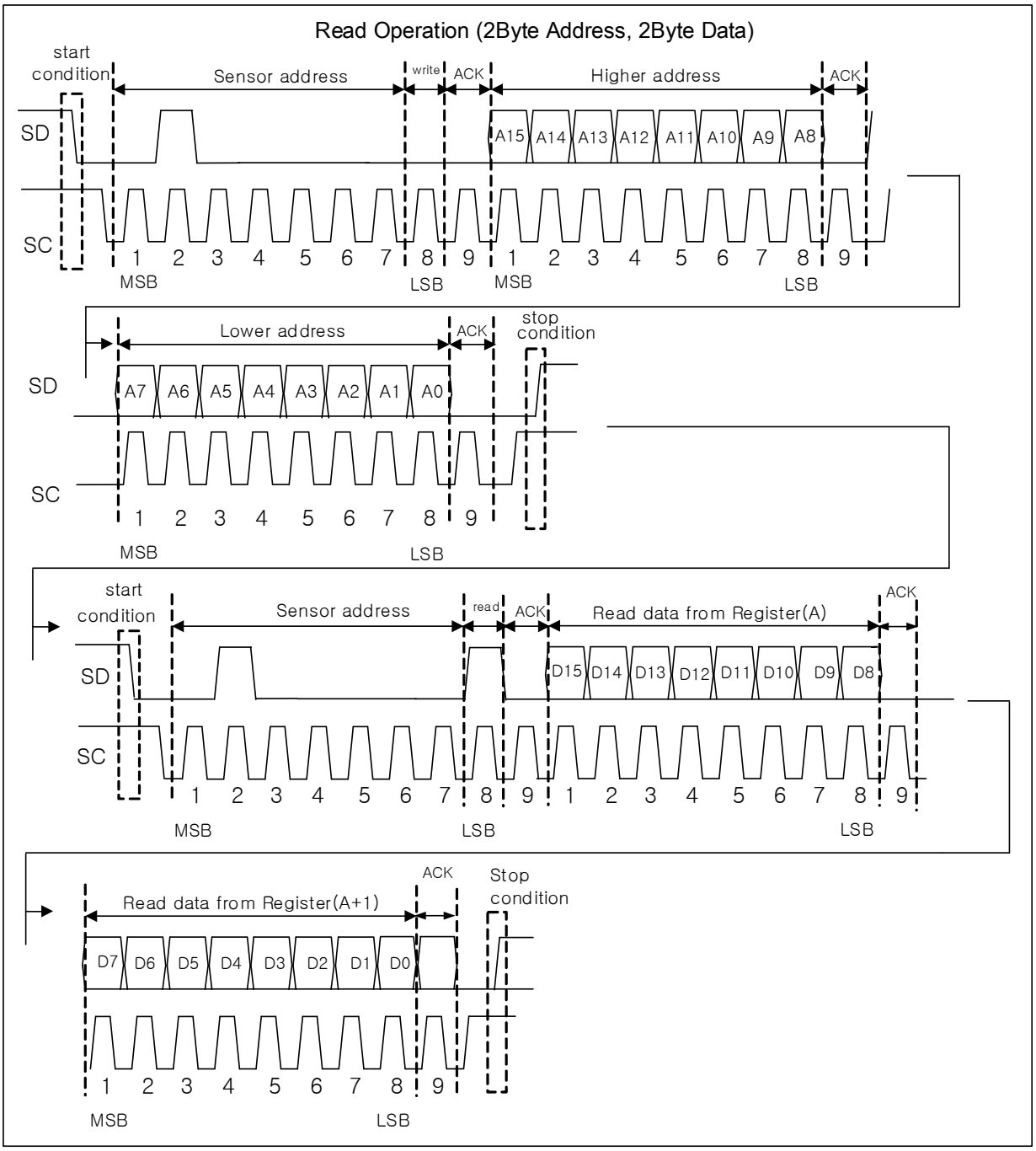
3.2.3. Read Operation (2 bytes address – 1byte data format)

<Figure 6. Read Operation through Two Wire Serial Bus>



3.2.4. Read Operation (2 bytes address – 2byte data format)

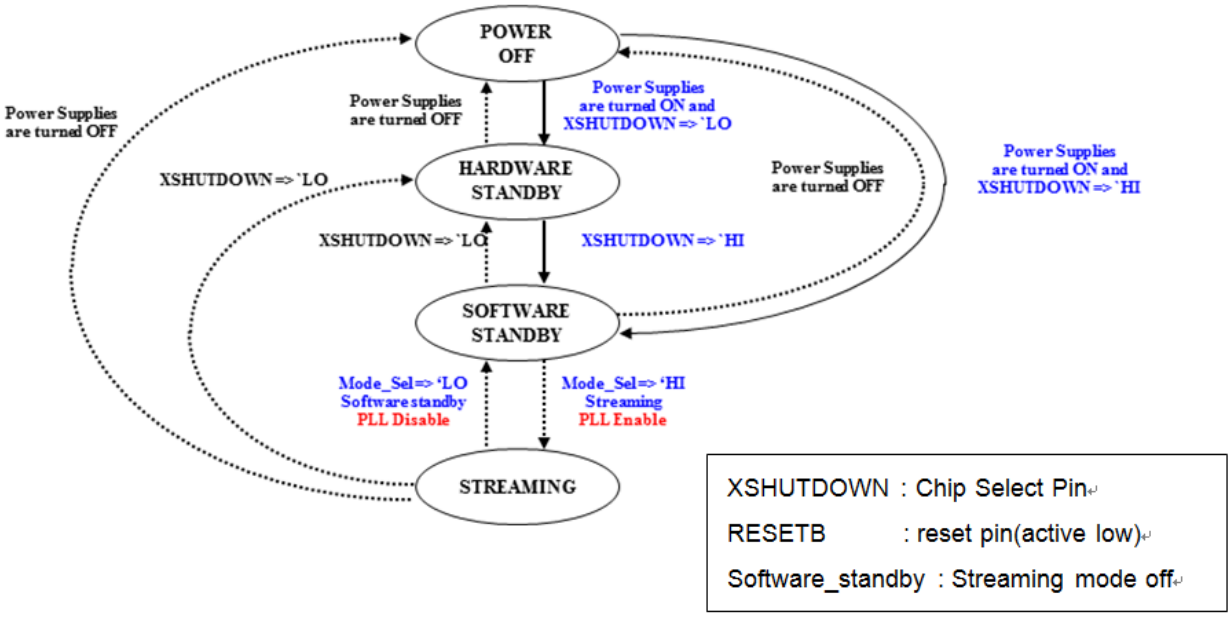
<Figure 7. Read Operation through Two Wire Serial Bus>



4. FUNCTION DESCRIPTION

4.1. Operation Mode

<Figure 8. System State Diagram>



[Table 11. Operation Mode Summary]

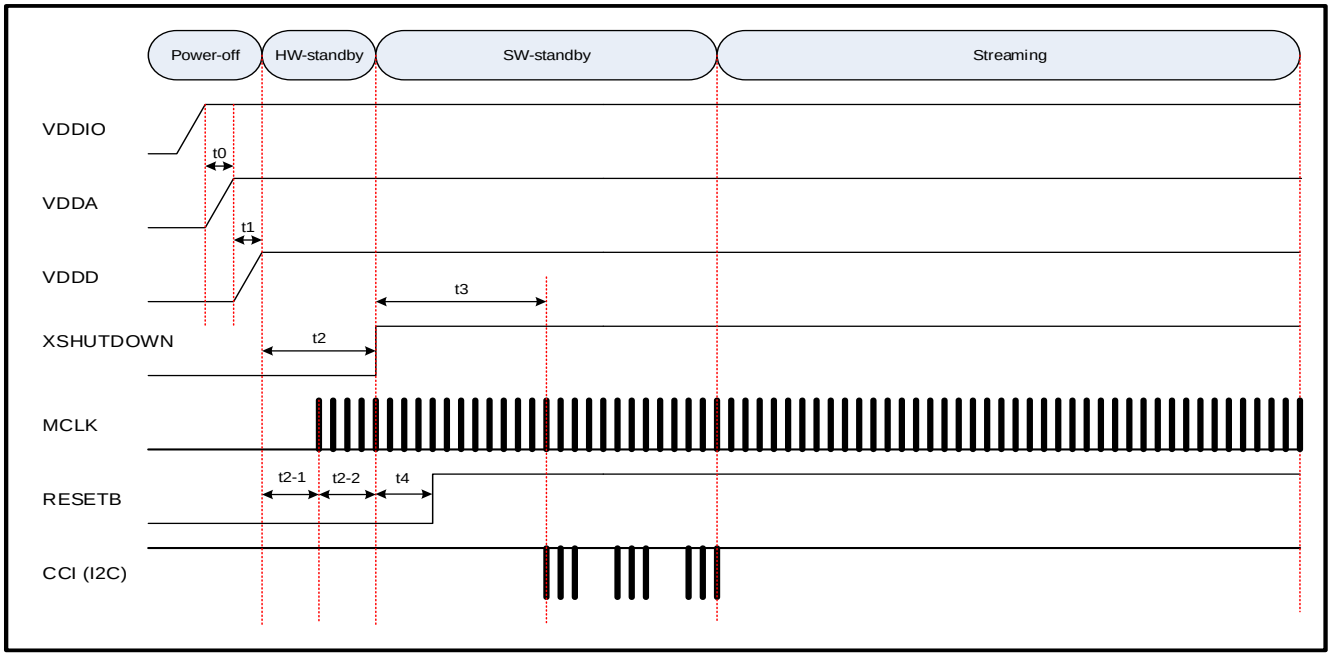
Power State	Description	Activate
Power OFF	Power supplies are turned off.	None
Hardware Standby	No communication with the sensor is possible Low level on XSHUTDOWN pin and stopping EXTCLK.	XSHUTDOWN Low MCLK Low
Software Standby	Two-wire serial communication with sensor is possible PLL is ready for fast return to streaming mode.	MCLK Pad Enabled
Streaming	The sensor is fully powered and streaming image data on the MIPI CSI-2 bus.	All Logic, MCLK Pad Enabled

4.2. Power Timing

4.2.1. Power On Sequence (Normal control)

VDDIO 2.8V/1.8V(ON) → VDDA 2.8V(ON) → VDDD 1.2V (ON) → MCLK(ON) → XSHUTDOWN(L→H) → RESETB(ON) → Set registers for normal operation → Normal Operation

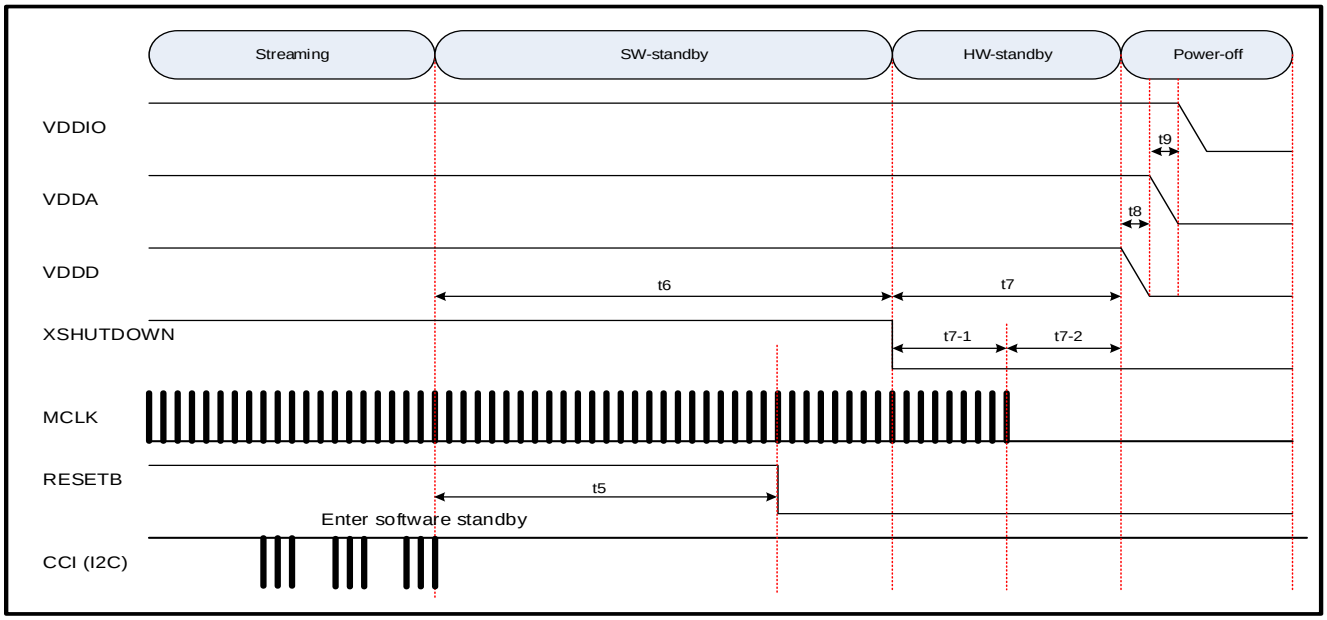
<Figure 9. Timing of Power on Sequence(Normal Mode)>



4.2.2. Power Off Sequence (Normal control)

Normal Operation → Power Sleep command and disable PLL → SC, SD (OFF) → RESETB(OFF) → XSHUTDOWN(H→L)→ MCLK(OFF)→ VDDD 1.2V (OFF) → VDDA 2.8V(OFF) → VDDIO 2.8V/1.8V(OFF)

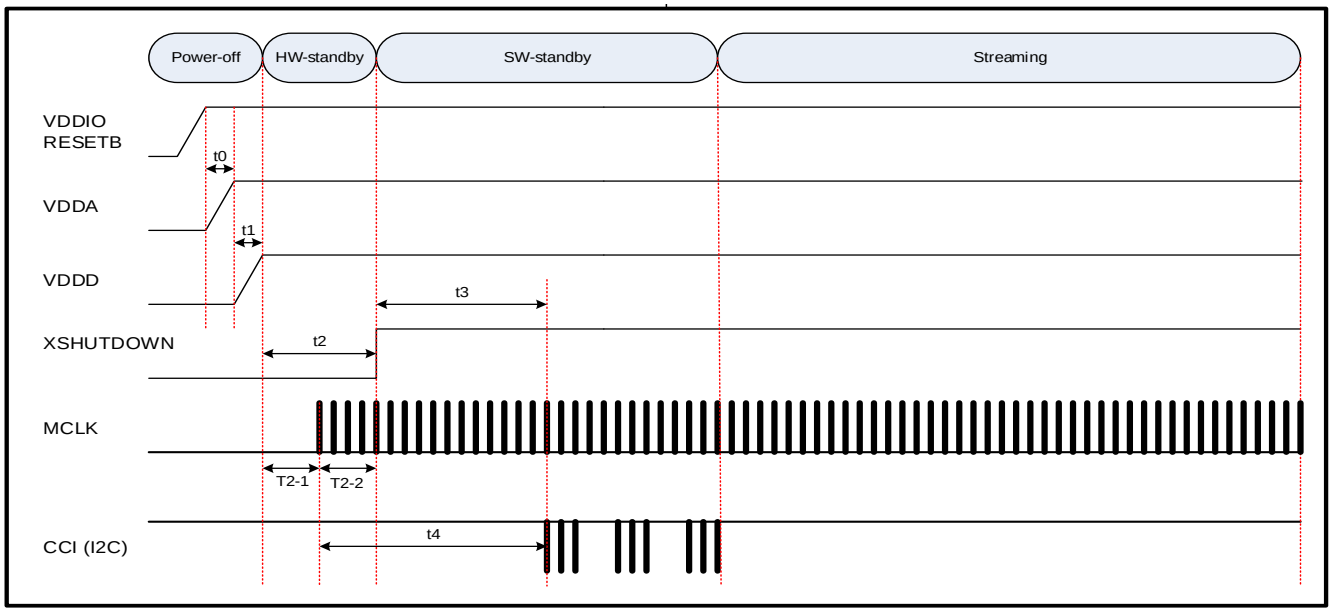
<Figure 10. Timing of Power off Sequence(Normal Mode)>



4.2.3. Power On Sequence (XShutdown control)

VDDIO 2.8V/1.8V(ON) → VDDA 2.8V(ON) → VDDD 1.2V (ON) → MCLK(ON) → XSHUTDOWN(L→H) → Set registers for normal operation → Normal Operation

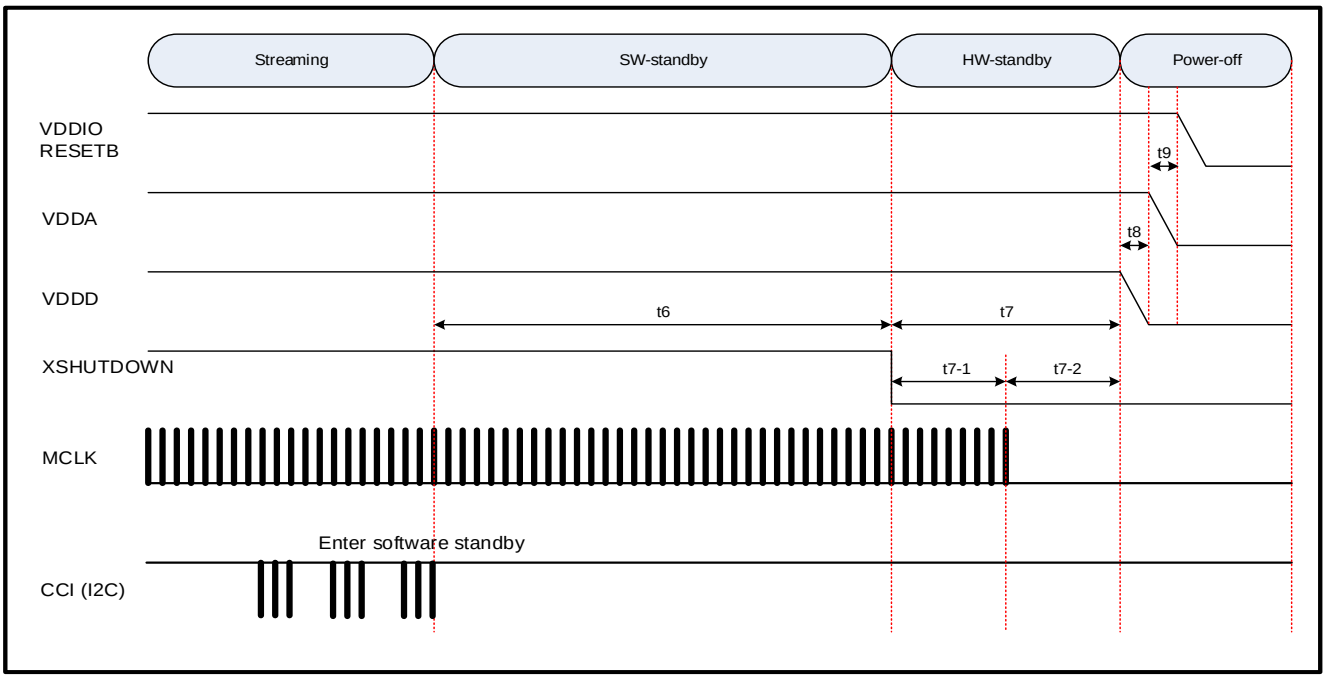
<Figure 11. Timing of Power on Sequence>



4.2.4. Power Off Sequence (XShutdown control)

Normal Operation → Power Sleep command and disable PLL → SC, SD (OFF) → XSHUTDOWN(H→L)→ MCLK(OFF)→ VDDD 1.2V (OFF) → VDDA 2.8V(OFF) → VDDIO 2.8V/1.8V(OFF)

<Figure 12. Timing of Power off Sequence>



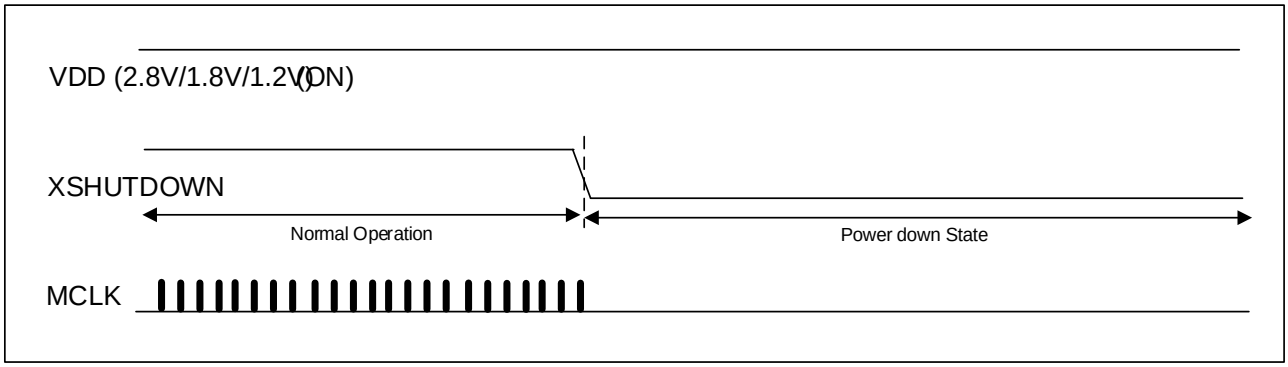
[Table 12. Timing of Power Sequence]

Constraint	Label	Min	Max	Unit
VDDIO rising – VDDA rising	t_0	VDDIO, VDDA and VDDD may rise in any order The rising separation can vary from 0ns to indefinite		ns
VDDA rising – VDDD rising	t_1			ns
VDDD rising – XSHUTDOWN rising	t_2	0.0		ns
VDDD rising – MCLK running	t_{2-1}	0.0		ns
MCLK running – XSHUTDOWN rising	t_{2-2}	0.0		ns
XSHUTDOWN rising – First I2C transaction	t_3	2400		MCLK cycles
Minimum no of MCLK cycles prior to the first I2C transaction. With XSHUTDOWN.	t_4	2400		MCLK cycles
D-PHY power-up	t_5	1.0		ns
D-PHY init	T_6	100		us
XSHUTDOWN failing – VDDD falling	T_7	0.0		ns
XSHUTDOWN falling – MCLK stop	T_{7-1}	0.0		ns
MCLK stop – VDDD falling	T_{7-2}	0.0		ns
VDDD falling – VDDA falling	T_8	VDDIO, VDDA and VDDD may fall in any order. The falling separation can vary from 0ns to indefinite		ns
VDDA falling – VDDIO falling	T_9			ns

4.2.5. From Normal Operation State to Stand-by(Power down) State

When XSHUTDOWN is disabled, output pins go to Hi-Z.

<Figure 13. Timing of Normal to Stand-by>



4.2.6. From Stand-by(Power down) State to Normal Operation State

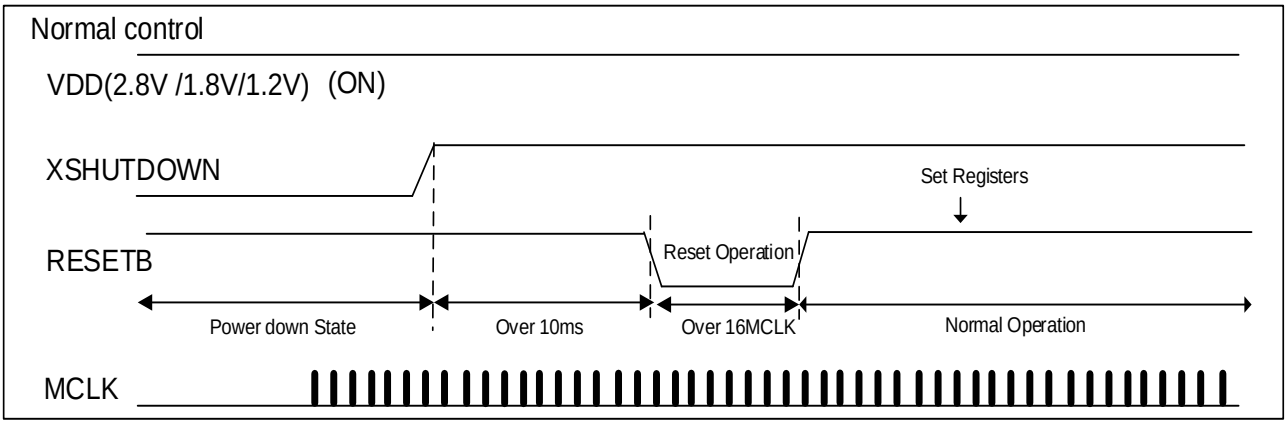
1) Set XSHUTDOWN to Hi.

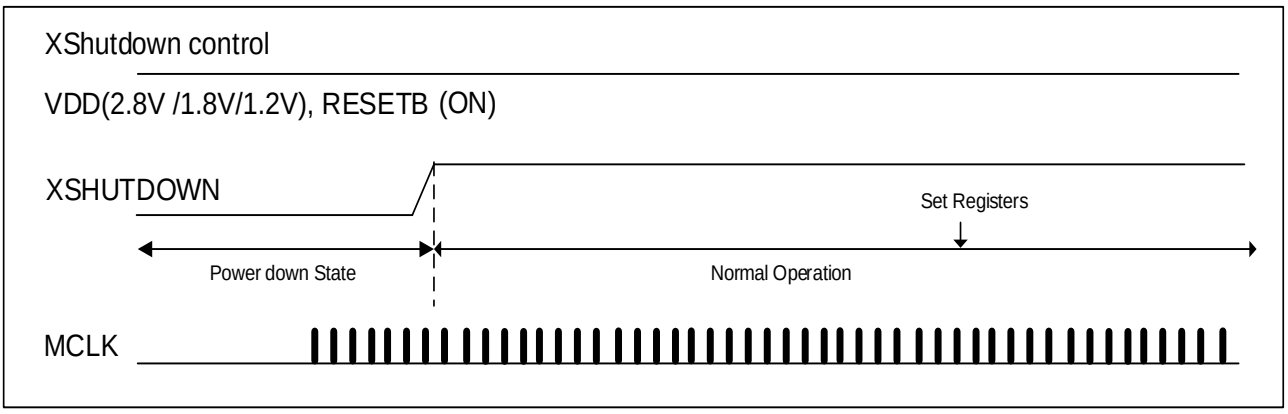
2) Wait 10ms.

3) Set RESETB from Low to Hi.

4) Set the registers for normal operation

<Figure 14. Timing of Stand-by to Normal>





4.3. Test Pattern Generator (TPG)

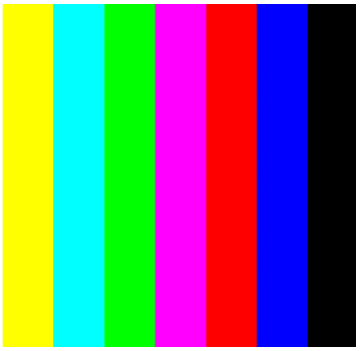
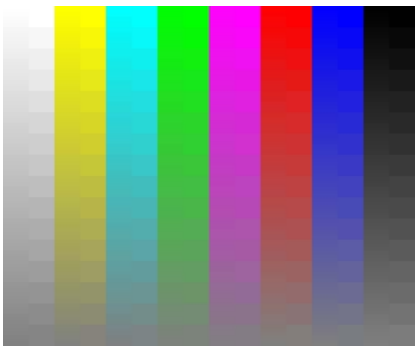
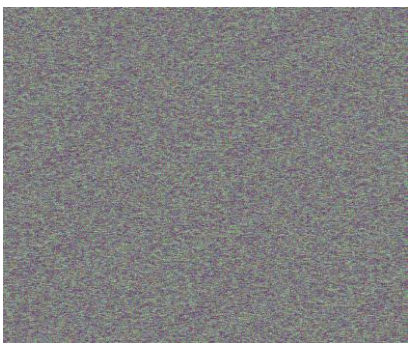
For testing, we support various test patterns, such as color bars/ fade to gray color bars/ PN9 pattern etc.

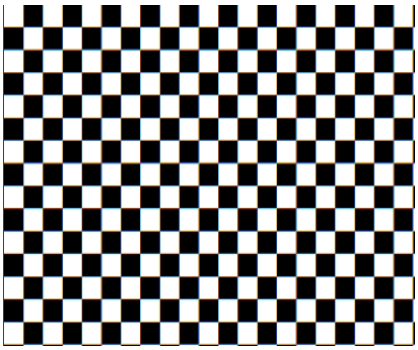
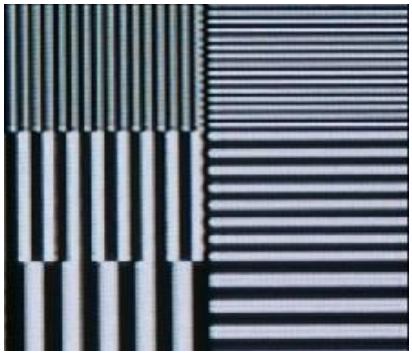
The output type of digital test pattern is controlled by Test_pattern_mode register(0x020A[3:0]). The digital test pattern function is controlled by isp_en register (0x0A05[0]).

[Table 13. Test Pattern register]

Addr.	Register Name	Description	Default
0x0A05	isp_en_l	B[0] - Test pattern generation enable	0x0
0x020A	test_pattern_mode	B[3:0]Test pattern mode 0 – no pattern(default) 1 – solid color 2 – 100% color bars 3 – Fade to grey color bars 4 – PN9 5 – horizontal gradient pattern 6 – vertical gradient pattern 7 – check board 8 – slant pattern 9 – Resolution pattern	0x00

<Figure 15. Test patterns>

Solid color	100% color bars
	
Fade to gray color bars	**PN9**
	

Horizental/Vertical gradient	Check board
	
Slant	**Resolution**
	

4.4. Black Level Calibration(BLC)

Black level is caused from pixel characteristics and analog channel offset. It makes poor image quality in dark condition and misleads color balance. To reduce these phenomenon, sensor automatically calibrates the black level every frame. The masked pixels in pixel array are used to calculate the black level.

4.5. Integration Time

The integration (exposure) time is controlled by the Integration time(integ_time : 0x0073, 0x0074, 0x0075) registers. The line length(0x0008, 0x0009) is used by the mode between normal and binning.

Total_integration_time = integration_time x (line_length_pck / 4)x pck_clk_period

[Table 14. Integration Time]

Addr.	Register Name	Description	Default
0x0008	line_length_pck_h	Line Length [15:8]	0x0E
0x0009	line_length_pck_l	Line Length [7:0]	0xD8
0x0073	integ_time_hw	The integration time control [19:16]	0x00
0x0074	integ_time_h	The integration time control [15:8]	0x01
0x0075	integ_time_l	The integration time control [7:0]	0x00

4.6. Analog Gain Control

Global gain register (0x0076) sets the analog gain. The maximum analog gain is 16x. Next table shows the recommended gain settings:

[Table 15. Analog Gain Register]

Addr.	Register Name	Description	Default
0x0076	analog_gain_code_global	Analog Gain *register value range = 0x0000 ~ 0x00F0(recommend)* $\text{Analog Gain} = \frac{Reg.value}{16} + 1$	0x0000

[Table 16. Analog Gain Setting]

Register value		Gain(X)	Register value		Gain(X)
Dec	Hex		Dec	Hex	
0	0x0000	x1.0	128	0x0080	x9.0
8	0x0008	x1.5	136	0x0088	x9.5
16	0x0010	x2.0	144	0x0090	x10.0
24	0x0018	x2.5	152	0x0098	x10.5
32	0x0020	x3.0	160	0x00A0	x11.0
40	0x0028	x3.5	168	0x00A8	x11.5
48	0x0030	x4.0	176	0x00B0	x12.0
56	0x0038	x4.5	184	0x00B8	x12.5
64	0x0040	x5.0	192	0x00C0	x13.0
72	0x0048	x5.5	200	0x00C8	x13.5
80	0x0050	x6.0	208	0x0D0	x14.0
88	0x0058	x6.5	216	0x00D8	x14.5
96	0x0060	x7.0	224	0x00E0	x15.0
104	0x0068	x7.5	232	0x00E8	x15.5
112	0x0070	x8.0	240	0x00F0	x16.0
120	0x0078	x8.5			

4.7. Digital Gain Control

The digital gain processing supports the separate gains control for each color channel (R, Gr, Gb, B). Each gain control register is comprised of 13bit. The bit [12:9] control the integer portion and the bit [8:0] control the decimal portion of gain (512step size). The digital gain is represented as a following equation.

$$Digital\_Gain = \left(bit[12:9] + \frac{bit[8:0]}{512} \right)$$

Each digital gain control register has a range from 0x through 15.99x.

4.8. Bayer Scaler (Horizontal)

The image scaling function within a sensor module provides a downscaling operation using Bayer data to reduce the size while covering the same angle of view of the original image. Each downscaled output pixel is calculated by taking a weighted average of input pixels which are composed of neighboring pixels. The image scaling function of the Bayer Scaler supports horizontal down to x1/2 , x1/4 scale in X (Horizontal).

For example, when X scaling is enabled for a x1/2 scale factor, output image is reduced by half in X directions. This results in output image that is half of the input image size. The scaled output size is represented as a following equation depending on the scale factor.

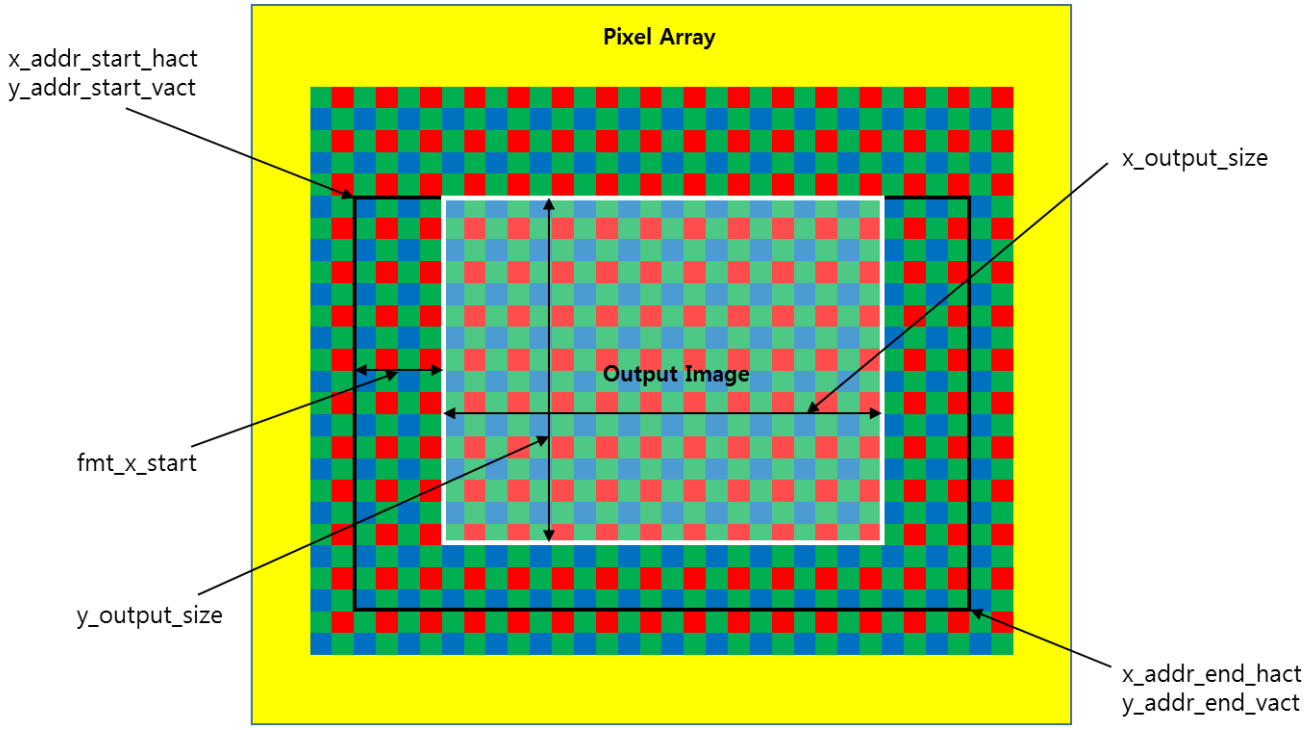
[Table 17. Image Scaler Register]

Addr.	Register Name	Description	Default
0x0A22	hbin_mode	B[7:2] : Reserved B[1:0] : Horizontal Binning Mode 10 : 1/4 Horizontal binning 01 : 1/2 Horizontal binning 00 : Bypass	0x00

4.9. Windowing

Sensor has a rectangular pixel array 3280 X 2464. The array can be windowed by the output crop. These crop functions operate by controlling offset(start pixel point) register and cropping image size register.

<Figure 16. Output Image windowing>



[Table 18. Image Windowing Register]

Addr.	Register Name	Description	Default
0x0026	y_addr_start_vact_h	active y start address	0x00
0x0027	y_addr_start_vact_l		0x38
0x002C	y_addr_end_vact_h	active y end address	0x09
0x002D	y_addr_end_vact_l		0xD7
0x0120	x_addr_start_hact_h	active x start address	0x00
0x0121	x_addr_start_hact_l		0x44
0x0122	x_addr_end_hact_h	active x end address	0x03
0x0123	x_addr_end_hact_l		0x78
0x0A12	x_output_size_h	fmt column output size	0x0C
0x0A13	x_output_size_l		0xD0
0x0A14	y_output_size_h	fmt row output size	0x09
0x0A15	y_output_size_l		0xA0
0x0804	fmt_x_start_h	column start pixel	0x00
0x0805	fmt_x_start_l		0x00

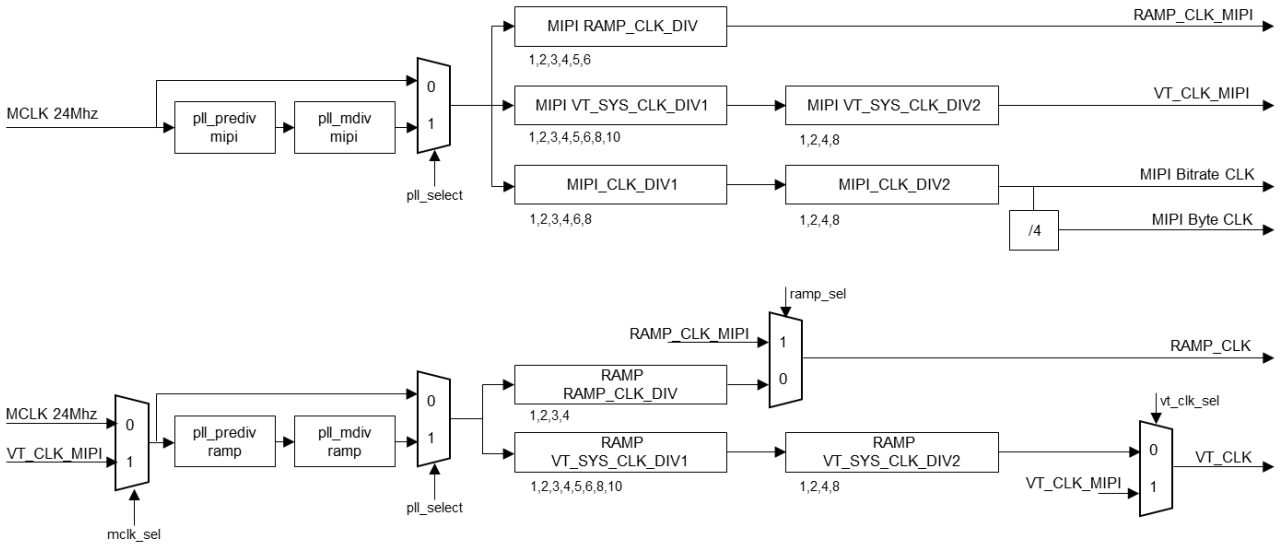
4.10. PLL

The PLL is used for clock generation for the digital block and MIPI transmitter. It consists of PFD(Phase Frequency Detector), charge pump (CP) and 2nd order loop-filter, 4-bit programmable pre-divider and 8-bit programmable main-divider. The clock generator is used for clock generation for digital part and MIPI transmitter. It consists of the divider for digital part and the divider for MIPI.

[Table 19. Register map of PLL]

Addr.	Register Name	Description	Default
0x0F32 0x0F33	Pll_cfg_ramp1	[15:12] : Reserved [11:8] : PLL_prediv_ramp [7:0] : PLL_mdiv_ramp	0x07 0x50
0x0F34 0x0F35	Pll_cfg_ramp2	[15:8] : Reserved [7] : Reserved [6:5] : PLL_ramp_clk_div [4:3] : PLL_vt_sys_clk_div2 [2:0] : PLL_vt_sys_clk_div1	0x00 0x24
0x0F38 0x0F39	Pll_cfg_mipi1	[15:12] : Reserved [11:8] : PLL_prediv_mipi [7:0] : PLL_mdiv_mipi	0x02 0x5A
0x0F2A 0x0F2B	Pll_cfg_mipi2	[15] : Reserved [14] : PLL_mipi_d_byte_clk_sel [13] : PLL_mipi_ramp_div_en [12:11] : PLL_mipi_clk_div2 [10:8] : PLL_mipi_clk_div1 [7:5] : PLL_mipi_ramp_clk_div [4:3] : PLL_mipi_vt_sys_clk_div2 [2:0] : PLL_mipi_vt_sys_clk_div1	0x41 0x24

<Figure 17. Block Diagram of PLL>



4.11. MIPI

YACG4D0C9SHC supports serial data output through 2/4-lane MIPI(Mobile Industry Processor Interface). YACG4D0C9SHC has four data lanes and one clock lane. The MIPI output transmitter runs up to 720 Mega bit/sec each lane.

[Table 20. CSI lane mode register]

Addr.	Register Name	Description	Default
0x0902[7:6]	data_lane_mode	0x01 - 2 lane mode 0x11 - 4 lane mode	0x11

The design follows CSI-2(Camera Serial Interface-2) specification. The CSI-2 specification defines standard data transmission and control interfaces between transmitter and receiver. The CSI-2 is unidirectional differential serial interface with data and clock signals; the physical layer of this interface is the "*MIPI Alliance Standard for D-PHY*". The high speed serial interface uses the following output-only signal pairs. (4 channel data lanes and clock lane in accordance with CCP2 / MIPI specification.)

[Table 21. MIPI serial interface]

Output pin	Description
DATA1_P / DATA1_N	Data lane Dp / Dn
DATA2_P / DATA2_N	
DATA3_P / DATA3_N	
DATA4_P / DATA4_N	
CLK_P / CLK_N	Clock lane Cp / Cn

The control interface (referred as CCI) is a bi-directional control interface compatible with I2C standard. YACG4D0C9SHC supports both continuous clock behavior and non-continuous clock behavior on the clock lane. The serial interface can reduce power consumption by entering ULPS(Ultra Low Power State) mode. Each data lanes and clock lane are set to the ULPS mode when the sensor is in the hardware standby or soft standby system state.

In order to operate MIPI serial interface, sensor must set both MIPI Power enable register and TX enable register at power up and after reset. The MIPI Reset register is used to initialize MIPI operation, normally not used.

[Table 22. Timing Configuration register]

Addr.	Register Name	Description	Default
0x0915	tlpx	D-PHY spec require : 50ns	0x05
0x0916	tclk_prepare	D-PHY spec require : > 38ns, < 95ns	0x05
0x0917	tclk_zero	D-PHY spec require : tclk_prepare + tclk_go > 300ns	0x1A
0x0919	ths_prepare	D-PHY spec require : 40ns + 4UI, < 85ns + 6UI	0x05
0x091A	ths_zero_min	D-PHY spec require : ths_prepare + ths_go > 145ns + 10UI	0x0A
0x091B	ths_trail	D-PHY spec require : > MAX(8UI, 60ns + 4UI)	0x09
0x091C	tclk_post	D-PHY spec require : > 60ns + 52UI	0x0D
0x091D	tclk_trail_min	D-PHY spec require : > 60ns	0x08

Many kinds of timing constraints are specified in the D-PHY specification. In order to satisfy this specifications, user needs to adjust timing value to control analog block. Registers from 0x0915 to 0x091D are used for this purpose. If you change the clock operating speed, reconfigurate registers.

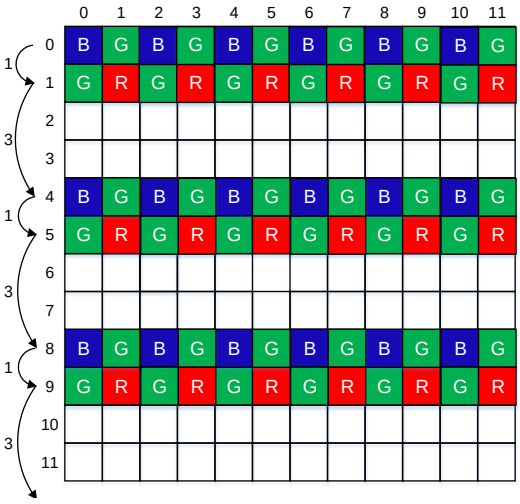
4.12. Subsampling & Binning

YACG4D0C9SHC supports Vertical Subsampling Mode (1/2, 1/4) and Binning Mode (1/2, 1/4).

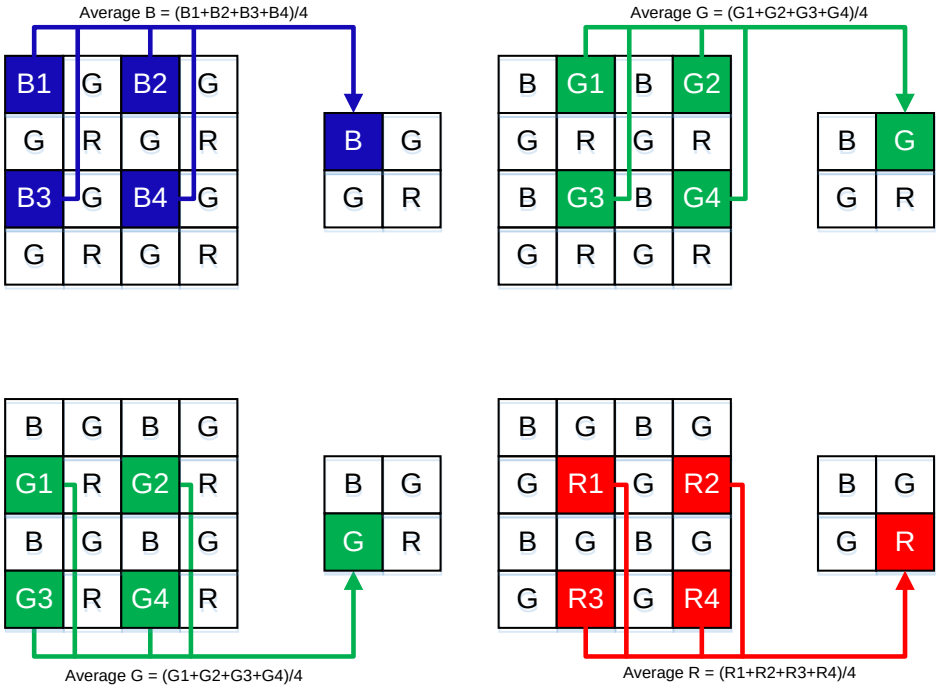
[Table 23. Binning Mode]

Addr.	Register Name	Description	Default
0x000C	binning_mode	Binning mode enable	0x00
0x002E	y_odd_inc_fobp	Frame obp y odd increase value	0x11
0x002F	y_even_inc_fobp	Frame obp y even increase value	0x11
0x0032	y_odd_inc_vact	Active y odd increase value	0x11
0x0033	y_even_inc_vact	Active y even increase value	0x11

<Figure 18. 1/2 Sub Sampling mode>



<Figure 19. 2x2 Binning mode>



4.13. Frame structure

Frame structure is controlled by line length pck, frame length lines, x_addr_start_hact, y_addr_start_vact, x_addr_end_hact, and y_addr_end_vact.

Frame length lines control

1. Frame length lines are controlled by 0x0006, 0x0007 at full readout mode.

Line length pck control

1. Line length pck is controlled by 0x0008, 0x0009 at full/analog subsampling readout mode.
2. Minimum line length pck
   -. normal,sub-sampling : 3800

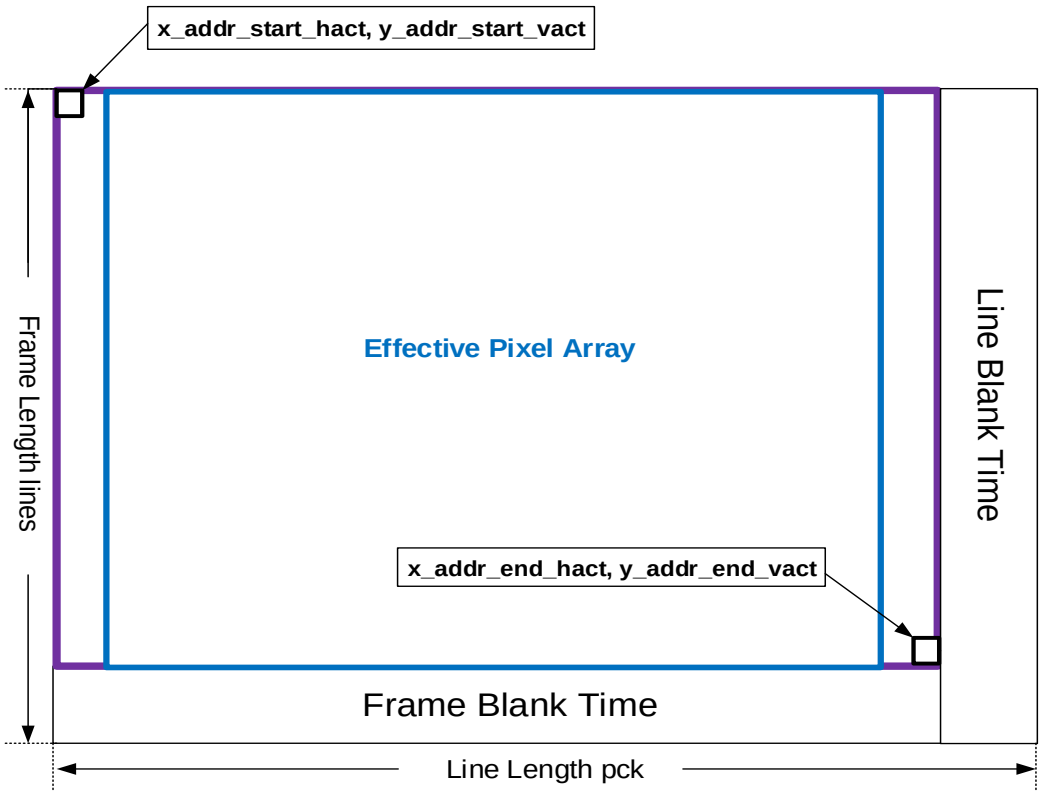
Visible pixel data size control

1. Visible pixel width is controlled by x_addr_start_hact [0x0120, 0x0121], x_addr_end_hact [0x0122, 0x0123], y_addr_start_vact [0x0026, 0x0027] and y_addr_end_vact [0x002C, 0x002D].
   -. Visible pixel width = (x_addr_end_hact – x_addr_start_hact) * 4
   -. Visible pixel height = y_addr_end_vact – y_addr_start_vact + 1
2. If 0x0034[2] bit is disabled , Visible pixel width and height is 0.

Blank time control

1. Line blank time
   -. Line blank time = line length pck – (visible pixel width / 4)
2. Frame blank time
   -. Frame blank time = frame length lines – visible pixel height
   -. Minimum blank time : 40 lines

<Figure 20. Frame Structure>



4.14. Fixed Frame Rate Timing

There are two kinds of frame rate. One is fixed frame rate and another is variable frame rate. Fixed frame rate mode can be enabled when 0x003C[0] bit is asserted. If fixed frame rate mode is enabled, maximum coarse integration time(0x0074, 0x0075) is 'frame length – 6'.

And variable frame rate mode can be enabled when 0x003C[0] bit is de-asserted. In variable frame rate mode, frame length is changed automatically according to coarse integration time. Specific frame length lines according to coarse integration time can be calculated by below formula.

If (coarse_integration_time ≥ (frame_length-6))

Frame length = coarse integration time + 6

else

Frame length = Register setting value of frame length lines

And frame time can be calculated by below formula.

Frame time = (line length pck) x (frame length) x VT_CLK_priode.

[Table 24. Frame Time Calculation]

Fixed Frame Time

If (Coarse_Integration_Time > Frame_length – 6(Coarse_Integration_Time _Max_Margin))
➔ Coarse_Integration_Time = Frame_Length - 6
Else
➔ Coarse_Integration_Time = Coarse_Integration_Time

Variable Frame Time

If (Coarse_Integration_Time ≥ Frame_length – 6(Coarse_Integration_Time _Max_Margin))
➔ Frame_Length = Coarse_Integration_Time + 6(Coarse_Integration_Time _Max_Margin)
Else
➔ Frame_Length = Coarse_integration_Time

4.15. Line-interlaced long-short output for HDR

High dynamic range (HDR) technology delivers better image quality and brighter, truer colors by accurately representing the wide range of intensity levels found in direct sunlight and in the deepest shadows.

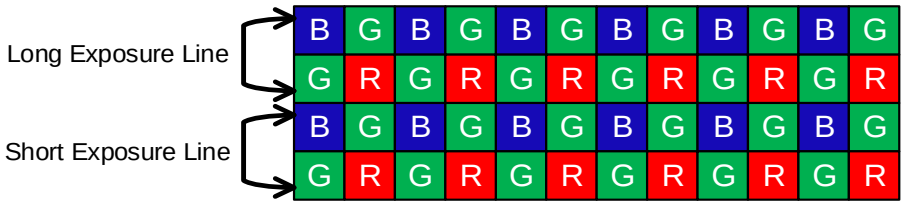
Line-interlaced long-short output for HDR, dual exposure HDR that not only improves the dynamic range, but also reduces motion artifacts and eliminates frame buffer requirements without compromising frame resolution or speed.

In HDR mode, the exposure is still controlled by a rolling shutter. However, the frame data is separated into “long exposure” and “short exposure” in every two rows. Long exposure time is controlled by registers 0x0073, 0x0074, and 0x0075. Short exposure time is controlled by registers 0x0072, 0x0070, and 0x0071.

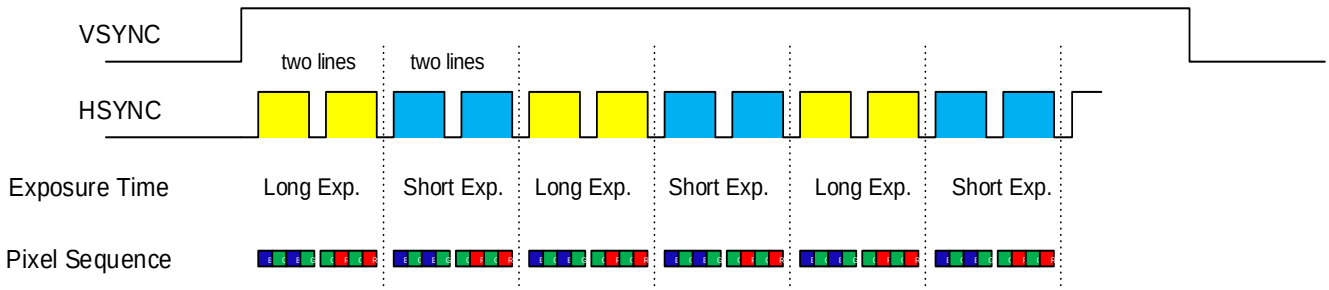
[Table 25. HDR control registers]

Addr.	Register Name	Description	Default
0x004D	hdr_en	hdr_en[0] HDR mode enable	0x00
0x0073	integ_time_hw	{ integ_time_hw[3:0], integ_time_h[8:0], integ_time_l[8:0] } → 20bit integration time for HDR mode (Long)	0x00
0x0074	integ_time_h		0x01
0x0075	integ_time_l		0x00
0x0072	integ_time_s_hw	{ integ_time_s_hw[3:0], integ_time_s_h[8:0], integ_time_s_l[8:0] } → 20bit integration time for HDR mode (Short)	0x00
0x0070	integ_time_s_h		0x01
0x0071	integ_time_s_l		0x00

<Figure 21. HDR Pixel Sequence>



<Figure 22. HDR Output Timing>

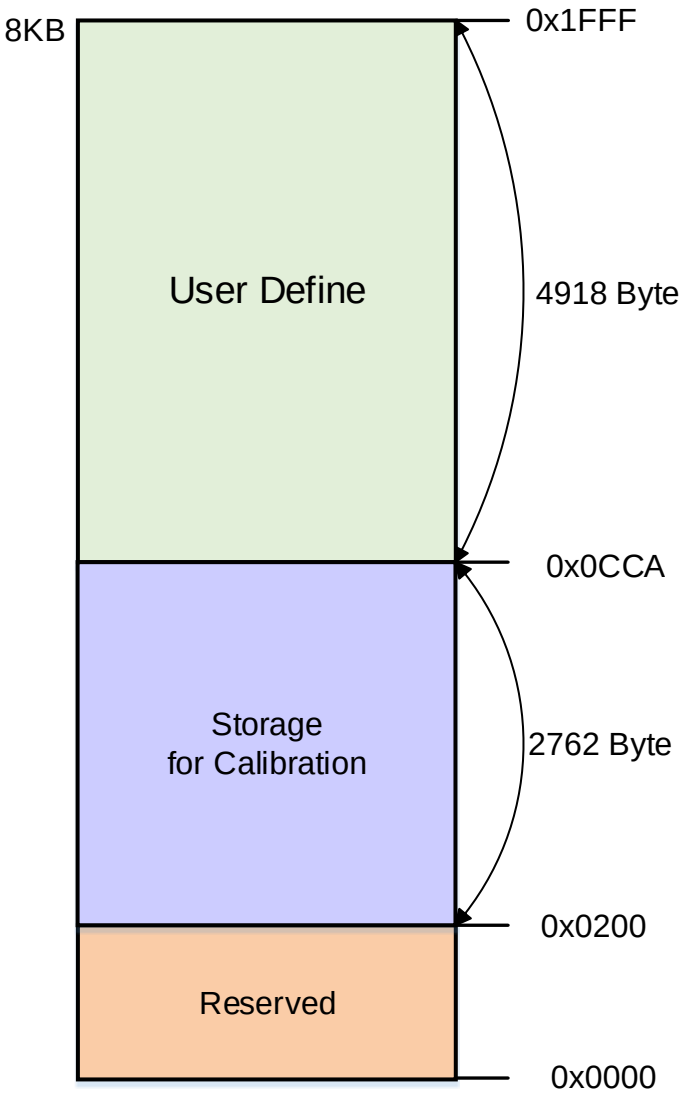


4.16. OTP Memory Map

The YACG4D0C9SHC features 8KByte of OTP(One Time Programmable) memory, individual moduel and sensor specific information. The user may program which set to be used. OTP can be accessed via two-wire serial interface.

If user want to get more information, please contact to SKhynix FAE engineer or refer to sererate OTP guide documents.

<Figure 23. OTP Memory Map>

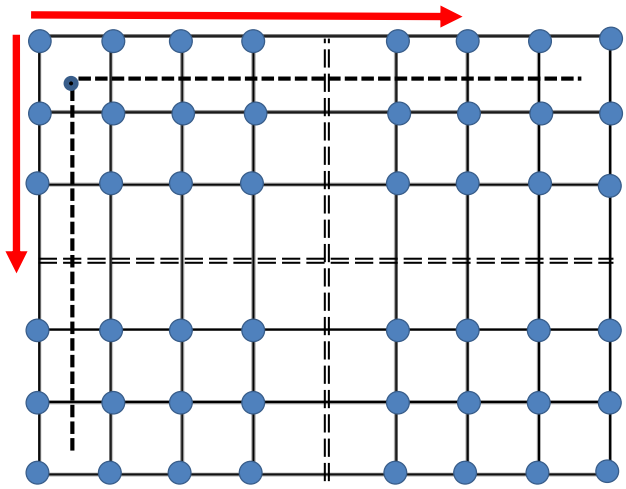


4.17. Lens Shading Correction(LSC)

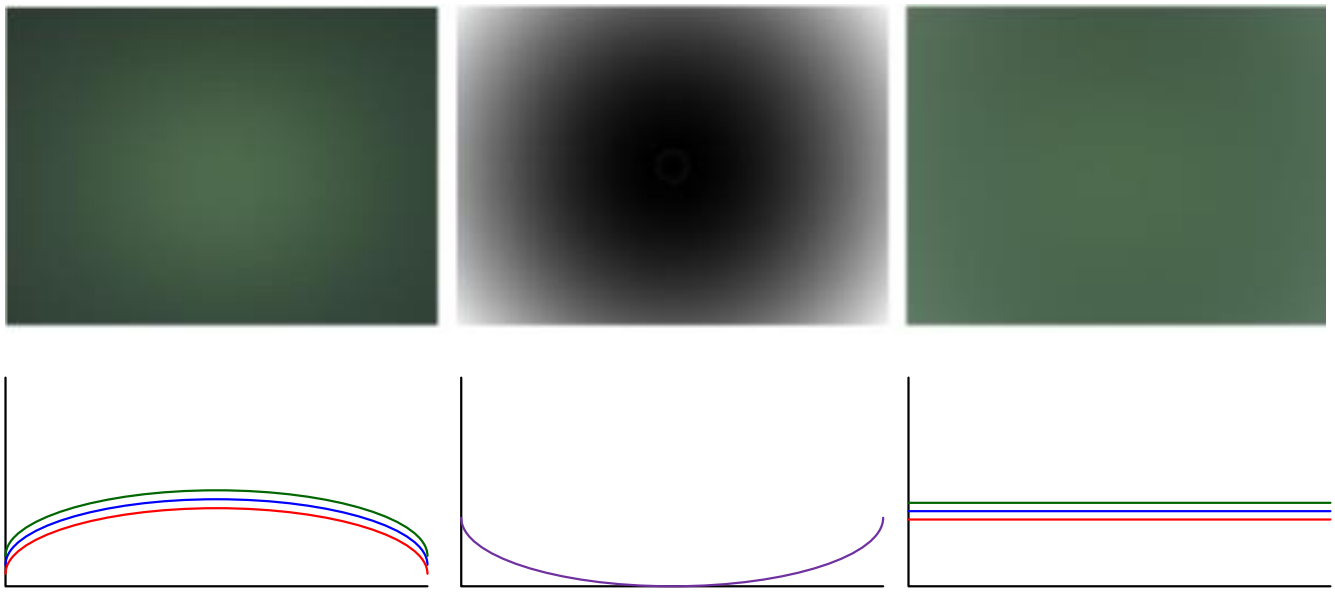
The circumstance area of pixel array does not have enough quantity of light due to optical characteristics of lens. It causes reduction of signal near peripheral of pixel array. The reduction of signal depends on both pixel' s location and color. To compensate the problem, shading correction is done by controlling the correction gain, which depends on pixel's location and color.

Shading correction changes automatically, based on the illumination type. The storages which is used for seed values are OTP or SRAM.

<Figure 24. LSC X-Y 2D interpolation>



<Figure 25. LSC Result image>



(a) Original image **(b) LSC Gain image** **(c) LSC result image**

5. REGISTER DESCRIPTION

Notification

SKhynix doesn't have any responsibility or liability for any failures if using reserved register addresses.

5.1. TG

0x0006: frame_length_lines_h [default=0x09, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	frame_length_lines_h	Frame length (Units : lines)	0000_1001b	Next

0x0007: frame_length_lines_l [default=0xD8, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	frame_length_lines_l	Frame length (Units : lines)	1101_1000b	Next

0x0008: line_length_pck_h [default=0x0E, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	line_length_pck_h	Line length (Units : pixels)	0000_1110b	Next

0x0009: line_length_pck_l [default=0xD8, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	line_length_pck_l	Line length (Units : pixels)	1101_1000b	Next

0x000C: binning_mode [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:2]		Reserved	0000_00b	Next
B[1:0]	binning_mode	0 – None 1 – 1/2 binning 3 – 1/4 binning	00b	

0x000E: image_orientation [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:2]		Reserved	0000_00b	Next
B[1]	V_flip	Vertical Flip Enable [0: no flip, 1: Vertical Flip]	0b	
B[0]	H_mirror	Horizontal Mirror Enable [0:no mirror,1:Horizontal Mirror]	0b	

0x0026: y_addr_start_vact_h [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	y_addr_start_vact_h	y start address	0000_0000b	Next

0x0027: y_addr_start_vact_l [default=0x40, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	y_addr_start_vact_l	y start address	0010_0000b	Next

0x002C: y_addr_ end _vact_h [default=0x09, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	y_addr_ end_vact_h	y end address	0000_1001b	Next

0x002D: y_addr_end_vact_l [default=0xCF, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	y_addr_ end_vact_l	y end address	1100_1111b	Next

0x002E: y_odd_inc_fobp [default=0x11, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	y_odd_inc_fobp	Increment for frame obp odd lines in the readout order	0001_0001b	Next

0x002F: y_even_inc_fobp [default=0x11, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	y_even_inc_fobp	Increment for frame obp odd lines in the readout order	0001_0001b	Next

0x0032: y_odd_inc_vact [default=0x11, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	y_odd_inc_vact	Increment for odd lines in the readout order	0001_0001b	Next

0x0033: y_even_inc_vact [default=0x11, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	y_even_inc_vact	Increment for even lines in the readout order	0001_0001b	Next

0x0046: grouped_para_hold [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:1]		Reserved	0000_000b	Next
B[0]	grouped_para _hold	grouped parameter hold Set to envelope a series of parameter changes as a group of changes that should be made so as to effect the output stream on the same frame boundary 0 : Release 1 : Hold	0b	

0x0047: ae_sync_mode [default=0x02, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:2]		Reserved:	0000_00b	Next
B[1]	per_frame_co ntrol	Per frame control 0: disable 1: enable	1b	
B[0]	fast_para_upd ate	Fast parameter update 0: disable 1: enable	0b	

0x004C: tg_enable [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:1]		Reserved	0000_000b	Current
B[0]	tg_enable	0 : tg_disable 1 : tg_enable	0b	

0x004D: hdr_enable [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:1]		Reserved	0000_000b	Next
B[0]	hdr_en	0 : HDR Mode disable 1 : HDR Mode enable	0b	

0x0070: coarse_integ_time_s_h [default=0x01, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	coarse_integ_time_s_h	The coarse integration time for HDR mode (Short)< Related reg. 0x0072, 0x0071>	0000_0001b	Next

0x0071: coarse_integ_time_s_l [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	coarse_integ_time_s_l	The coarse integration time for HDR mode(Short)< Related reg. 0x0072, 0x0070>	0000_0000b	Next

0x0072: coarse_integ_time_s_hw [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	coarse_integ_time_s_hw	The coarse integration time for HDR mode (Short) < Related reg. 0x0070, 0x0071>	0000_0000b	Next

0x0073: coarse_integ_time_hw [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	integration_time_hw	The coarse integration time control < Related reg. 0x0074, 0x0075 >	0000_0000b	Next

0x0074: coarse_integ_time_h [default=0x01, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	coarse_integ_time _h	The coarse integration time control < Related reg. 0x0073, 0x0075 >	0000_0001b	Next

0x0075: coarse_integ_time_l [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	coarse_integ_time_l	The coarse integration time control < Related reg. 0x0073, 0x0074 >	0000_0000b	Next

0x0077: analog_gain_code_global [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	Analog_gain_code_global_l	Global Analogue Gain Code	0000_0000b	Next

0x0120: x_addr_start_hact_h [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	x_addr_start_hact_h	x start address	0000_0000b	Next

0x0121: x_addr_start_hact_l [default=0x44, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	x_addr_start_hact_l	x start address	0100_0100b	Next

0x0122: x_addr_ end_hact_h [default=0x03, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	x_addr_end_hact_h	x end address	0000_0011b	Next

0x0123: x_addr_end_hact_l [default=0x78, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	x_addr_end_hact_l	x end address	0111_1000b	Next

5.2. OTP

0x0702: otp_cmd [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:2]		Reserved	0000_00b	Current
B[1]	otp_write_cmd	Continuous write	0b	
B[0]	otp_read_cmd	Continuous read	0b	

0x0706: otp_wdata [default=0x00, w/o]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	otp_wdata	OTP write data	0000_0000b	Current

0x0708: otp_rdata [default=0x00, r/o]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	otp_rdata	OTP read data	0000_0000b	Current

0x070A: otp_addr_h [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	otp_addr_h	OTP write/read address high	0000_0000b	Current

0x070B: otp_addr_l [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	otp_addr_l	OTP write/read address low	0000_0000b	Current

5.3. TPG

0x020A: test_pattern_mode [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:4]		Reserved	0000b	Next
B[3:0]	test_pattern _mode	Test pattern mode 0 – no pattern(default) 1 – solid color 2 – 100% color bars 3 – fade to grey color bars 4 – PN9 5 – horizontal gradient pattern 6 – vertical gradient pattern 7 – check board 8 – slant pattern 9 – resolution pattern 10 ~ 15 - Reserved	0000b	

0x0202: tpg_width_h [default=0x0A, r/w]

Bit	Function	Description	Default	Renewal Frame
B[3:0]	tpg_width_h	Image width replace register	0000_1010b	Current

0x0203: tpg_width_l [default=0x30, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	tpg_width_l	Image width replace register	0011_0000b	Current

0x0204: tpg_height_h [default=0x07, r/w]

Bit	Function	Description	Default	Renewal Frame
B[3:0]	tpg_height_h	Image heigth replace register	0000_0111b	Current

0x0205: tpg_height_l [default=0xA8, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	tpg_height_l	Image heigth replace register	1010_1000b	Current

0x020C: test_data_red_h [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	test_data_red_h	The test data used to replace red pixel data (high byte [15:8])	0000_0000b	Next

0x020D: test_data_red_l [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	test_data_red_l	The test data used to replace red pixel data (low byte [7:0])	0000_0000b	Next

0x020E: test_data_greenR_h [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	test_data_greenR_h	The test data used to replace greenR pixel data (high byte [15:8])	0000_0000b	Next

0x020F: test_data_ greenR_l [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	test_data_ greenR_l	The test data used to replace greenR pixel data (low byte [7:0])	0000_0000b	Next

0x0210: test_data_blue_h [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	test_data_blue_h	The test data used to replace blue pixel data (high byte [15:8])	0000_0000b	Next

0x0211: test_data_blue_l [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	test_data_blue_l	The test data used to replace blue pixel data (low byte [7:0])	0000_0000b	Next

0x0212: test_data_greenB_h [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	test_data_greenB_h	The test data used to replace greenB pixel data (high byte [15:8])	0000_0000b	Next

0x0213: test_data_greenB_l [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	test_data_greenB_l	The test data used to replace greenB pixel data (low byte [7:0])	0000_0000b	Next

5.4. Digital Gain

0x0078: digital_gain_gr_h [default=0x02, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:5]	digital_gain_gr_h	Reserved	000b	Next
B[4:0]		Digital gain for Gr channel (high byte [12:8])	0_0010b	

0x0079: digital_gain_gr_l [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	digital_gain_gr_l	Digital gain for Gr channel (low byte [7:0])	0000_0000b	Next

0x007A: digital_gain_gb_h [default=0x02, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:5]	digital_gain_gb_h	Reserved	000b	Next
B[4:0]		Digital gain for Gb channel (high byte [12:8])	0_0010b	

0x007B: digital_gain_gb_l [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	digital_gain_gb_l	Digital gain for Gb channel (low byte [7:0])	0000_0000b	Next

0x007C: digital_gain_r_h [default=0x02, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:5]	digital_gain_r_h	Reserved	000b	Next
B[4:0]		Digital gain for R channel (high byte [12:8])	0_0010b	

0x007D: digital_gain_r_l [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	digital_gain_r_l	Digital gain for R channel (low byte [7:0])	0000_0000b	Next

0x007E: digital_gain_b_h [default=0x02, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:5]	digital_gain_b_h	Reserved	000b	Next
B[4:0]		Digital gain for B channel (high byte [12:8])	0_0010b	

0x007F: digital_gain_b_l [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	digital_gain_b_l	Digital gain for B channel (low byte [7:0])	0000_0000b	Next

5.5. FORMATTER

0x0804: X_START_H [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	x_start_h	Column start pixel	0000_0000b	Next

0x0805: X_START_L [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	x_start_l	Column start pixel	0000_0000b	Next

5.6. Windowing

0x0A12: x_output_size_h [default=0x0C, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	x_output_size_h	Formatter column output size (MSB)	0000_1100b	Next

0x0A13: x_output_size_l [default=0xD0, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	x_output_size_l	Formatter column output size (LSB)	1101_0000b	Next

0x0A14: y_output_size_h [default=0x09, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	y_output_size_h	Formatter row output size (MSB)	0000_1001b	Next

0x0A15: y_output_size_l [default=0xA0, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	y_output_size_l	Formatter row output size (LSB)	1010_0000b	Next

5.7. MIPI

0x0902: MIPI_tx_op_mode [default=0xC3, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:6]	Lane Mode	MIPI lane mode 00 : 1 lane mode 01 : 2 lane mode 11 : 4 lane mode	11b	Current
B[5]	Data Format	MIPI data format 0 : RAW10 mode 1 : RAW8 mode	0b	
B[4]	Line synchronization	Line synchronization enable 1 : MIPI line start/end packet on 0 : MIPI line start/end packet off	0b	
B[3]	MIPI line number	MIPI line number enable 1 : MIPI line number on 0 : MIPI line number off	0b	
B[2]	MIPI frame number	MIPI frame number enable 1 : MIPI frame number on 0 : MIPI frame number off	0b	
B[1]	MIPI clock mode	MIPI clock mode selection 0:non-continuous clock mode 1:continuous clock mode	1b	
B[0]	MIPI frame number	MIPI frame count reset 0 : MIPI frame count reset off 1 : MIPI frame count reset on	1b	

0x0915: tlpx [default=0x05, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	tlpx	Tlpx is the length of any Low-Power state period	0000_0101b	Current

0x0916: tclk_prepare [default=0x05, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	tclk_prepare	Tclk prepare is the time to drive LP-00 to prepare for HS clock transmission.	0000_0101b	Current

0x0917: tclk_zero [default=0x1A, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	tclk_zero	Tclk zero is the time for lead HS-0 drive period before starting clock	0001_1010b	Current

0x0919: ths_prepare [default=0x05, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	ths_prepare	Ths prepare is the time to drive LP-00 before starting the HS transmission on a Data Lane.	0000_0101b	Current

0x091A: ths_zero [default=0x0A, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	ths_zero	Ths zero minimum is the time to send HS-0, i.e. turn on the line termination and drive the interconnect with the HS driver, prior to sending the SoT Sync sequence	0000_1010b	Current

0x091B: ths_trail [default=0x09, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	ths_trail	Ths trail is the time the transmitter must drive the flipped last data bit after sending the last payload data bit of a HS transmission burst. This time is required by the receiver to determine EoT.	0000_1001b	Current

0x091C: tclk_post [default=0x0D, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	tclk_post	Time that the transmitter shall continue sending HS clock after the last associated data lane has transitioned to LP mode. Host will control that suitable value is used	0000_1101b	Current

0x091D: tclk_trail_min [default=0x08, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	Tclk_trail_min	Tclk trail minimum is the time to drive HS differential state after last layload clock bit of a HS transmission burst.	0000_1000b	Current

5.8. ISP Common

0x0A00: mode_sel [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:1]		Reserved	0000_000b	Current
B[0]	mode_sel	1 – streaming 0 – sw_standby	0b	

0x0A02: fast_standby_mode [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:1]		Reserved	0000_000b	Current
B[0]	fast_standby_ mode	1 – fast standby mode (enable mode change from streaming mode to sw standby mode at line blank) 0 – sw_standby	0b	

0x0A04: isp_en_h [default=0x01, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:1]		Reserved	0000_000b	Current
B[0]	mipi enable	MIPI enable	1b	

0x0A05: isp_en_l [default=0x40, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7]		Reserved	0b	Current
B[6]	fmt enable	Formatter enable	1b	
B[5]	hbin enable	Horizontal binning enable	0b	
B[4]	lsc enable	Lens shading correction enable	0b	
B[3]	dga enable	Digital gain enable	0b	
B[2]		Reserved	0b	
B[1]	adpc enable	adpc enable	0b	
B[0]	tpg enable	Test pattern generation enable	0b	

0x0A10: data_pedestal [default=0x40, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	data_pedestal	data pedestal value	0100_0000b	Current

0x0A1A: pedestal_en [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:4]	-	Reserved	0000b	Current
B[3]	DGA Pedestal_en	DGA Pedestal enble	0b	
B[2]	LSC Pedestal_en	LSC Pedestal enble	0b	
B[1:0]		Reserved	00b	

5.9. Bayer Scaler (Horizontal)

0x0A22: hbin_mode [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:2]		Reserved	0000_00b	Next
B[1:0]	hbin_mode	Horizontal Binning Mode 10 : 1/4 Horizontal binning 01 : 1/2 Horizontal binning 00 : Bypass	00b	

5.10. PLL

0x0F32: pll_cfg_ramp1_h [default=0x07, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:4]		Reserved	0000b	Current
B[3:0]	pll_cfg_ramp1	PLL prediv ramp	0111b	

0x0F33: pll_cfg_ramp1_l [default=0x50, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	pll_cfg_ramp1	PLL mdiv ramp	0101_0000b	Current

0x0F34: pll_cfg_ramp2_h [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]		Reserved	0000_0000b	Current

0x0F35: pll_cfg_ramp2_l [default=0x24, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7]		Reserved	0b	Current
B[6:5]	pll_cfg_ramp2	PLL_ramp_clk_div	01b	
B[4:3]	pll_cfg_ramp2	PLL_vt_sys_clk_div2	00b	
B[2:0]	pll_cfg_ramp2	PLL_vt_sys_clk_div1	100b	

0x0F38: pll_cfg_mipi1_h [default=0x02, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:4]		Reserved	0000b	Current
B[3:0]	pll_cfg_mipi1	PLL_prediv_mipi	0010b	

0x0F39: pll_cfg_mipi1_l [default=0x5A, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	pll_cfg_mipi1	PLL_mdiv_mipi	0101_1010b	Current

0x0F2A: pll_cfg_mipi2_h [default=0x41, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7]		Reserved	0b	Current
B[6]	pll_cfg_mipi2	PLL_mipi_d_byte_clk_sel	1b	

B[5]	pll_cfg_mipi2	PLL_mipi_ramp_div_en	0b	
B[4:3]	pll_cfg_mipi2	PLL_mipi_clk_div2	00b	
B[2:0]	pll_cfg_mipi2	PLL_mipi_clk_div1	001b	

0x0F2B: pll_cfg_mipi2_l [default=0x24, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:5]	pll_cfg_mipi2	PLL_mipi_ramp_clk_div	001b	Current
B[4:3]	pll_cfg_mipi2	PLL_mipi_vt_sys_clk_div2	00b	
B[2:0]	pll_cfg_mipi2	PLL_mipi_vt_sys_clk_div1	100b	

5.11. BLC

0x0C00: blc_ctl0 [default=0x91, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:1]		Reserved	1001_000b	Current
B[0]	en_blc	BLC enable	1b	

0x0C01: blc_ctl1 [default=0x50, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:1]		Reserved	0101_000b	Current
B[0]	en_blc_hdr	BLC HDR enable	0b	

5.12. PAD

0x0D00: drvst_fsync [default=0x07, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:3]		Reserved	0000_0b	Current
B[2:0]	drvst_fsync	driving strength of FSYNC IO.	111b	

0x0D01: drvst_sda [default=0x07, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:3]		Reserved	0000_0b	Current
B[2:0]	drvst_sda	driving strength of SDA IO	111b	

0x0D02: drvst_strobe [default=0x07, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:3]		Reserved	0000_0b	Current
B[2:0]	drvst_strobe	driving strength of STROBE	111b	

5.13. SMU

0x0F00: rst_cfg1 [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:1]		Reserved	0000_000b	Current
B[0]	rst_cfg1	System software reset	0b	

0x0F02: pll_cfg1 [default=0x00, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:1]		Reserved	0000_000b	Current
B[0]	pll_cfg1	Pll enable	0b	

0x0F14: sensor_id [default=0x20, r/w]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	sensor_id	I2C slave address 0x20 @ 7bit 0x40 @ 8bit	0010_0000b	Current

0x0F16: model_id_l [default=0x46, r/o]

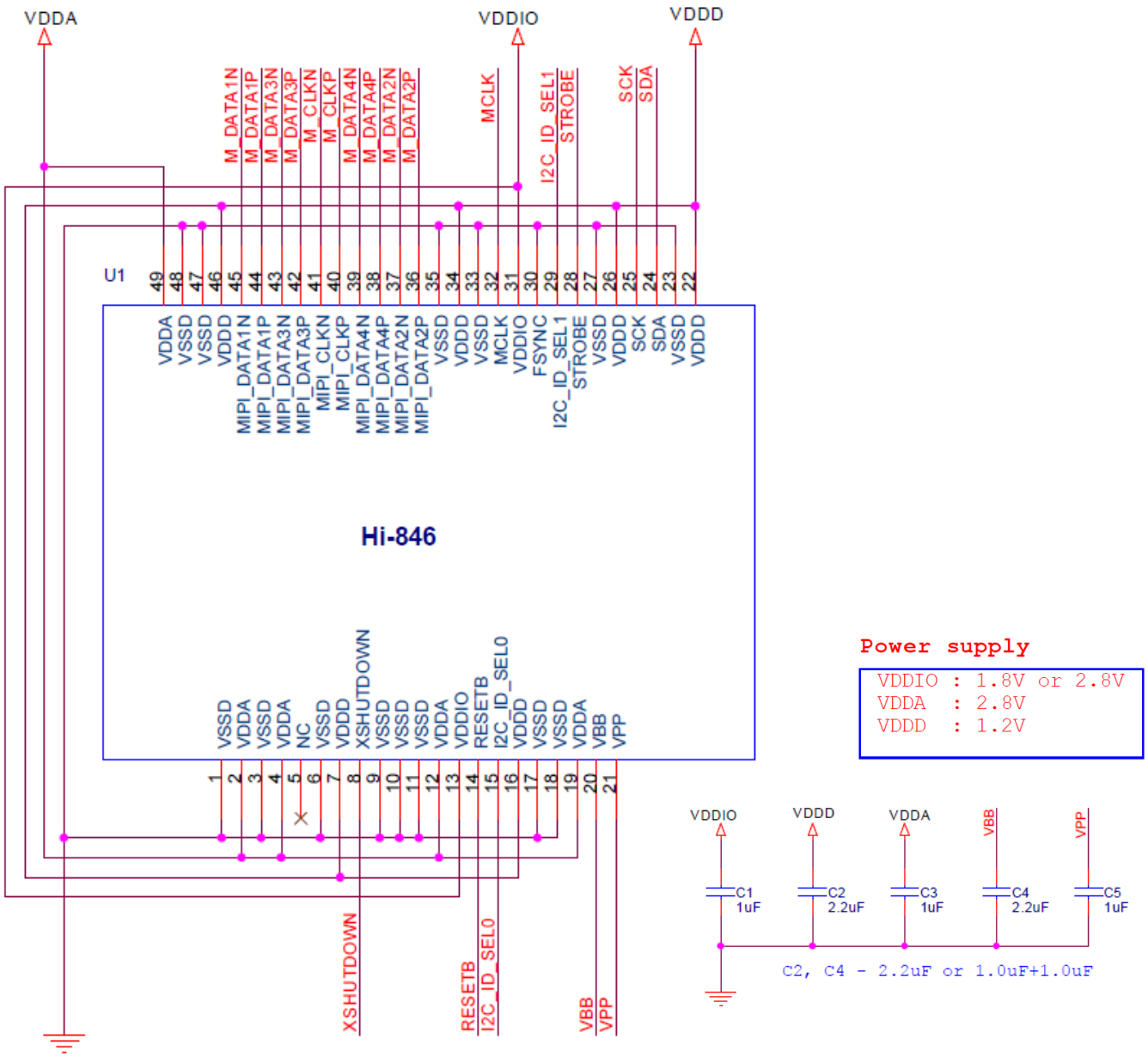
Bit	Function	Description	Default	Renewal Frame
B[7:0]	model_id_l	Sensor model ID lower byte	0100_0110b	RO

0x0F17: model_id_h [default=0x08, r/o]

Bit	Function	Description	Default	Renewal Frame
B[7:0]	model_id_h	Sensor model ID higher byte	0000_1000b	RO

6. Reference Module Schematic

<Figure 26. Module Schematic>



I2C Slave address select

PAD	Input	I2C Salve address
#15(I2C_ID_SEL0) #29(I2C_ID_SEL1)	Low(GND) Low(GND)	W-0x40@8bit R-0x41@8bit
#15(I2C_ID_SEL0) #29(I2C_ID_SEL1)	Low(GND) High(VDDIO)	W-0x44@8bit R-0x45@8bit
#15(I2C_ID_SEL0) #29(I2C_ID_SEL1)	High(VDDIO) Low(GND)	W-0x42@8bit R-0x43@8bit
#15(I2C_ID_SEL0) #29(I2C_ID_SEL1)	High(VDDIO) High(VDDIO)	W-0x46@8bit R-0x47@8bit

Sensor control

PAD	Normal control	X-Shutdown control
XSHUTDOWN (PAD #8)	Connect to AP GPIO	Connect to AP GPIO
RESETB (PAD #14)	Connect to AP GPIO	Connect to VDDIO

Note

STROBE(PAD #28) - If unused, this pad should be unconnected

FSYNC(PAD #30) - If unused, this pad should be tied to VSSD(GND)

7. Spectral Response

To be determined.