Mitigation of performance variability induced by Checkpoint-Restart using DVFS

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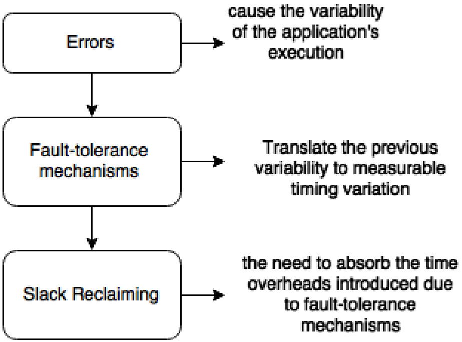
Urgency for slack Reclaiming


Errors
cause the variability of the application's execution
Fault-tolerance mechanisms
Translate the previous variability to measurable timing variation
Slack Reclaiming
the need to absorb the time overheads introduced due to fault-tolerance mechanisms

- Reliability Availability Serviceability (RAS) mechanisms
- Fault-tolerance mechanisms produce the idea of Reliability Wall [42]
- Darpa, Perfect project [16]

Error Profilling

Two types of errors are taken into account [32, 33]:

- Silent Data Corruptions (SDC), where erroneous outputs are generated. Data corruption may not manifest as failure and the application continues its execution
- Detected Unrecoverable Errors (DUE), the application is either terminated or blocked.

Errors are expressed by Mean Time to Failure (MTTF) and Failures in Time (FIT).

Operation of Checkpoint Restart

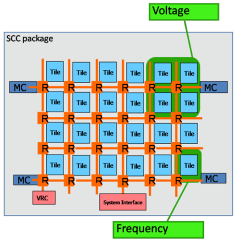
Checkpoint/Restart enables fault-tolerance in a system.

- Stores snapshots of the system or application state (system and application level C/R)
- After failure, operation can be restarted from a previous checkpoint
- C/R can be facilitated in distributed systems through system coordination [41]
- Available tools implementing the C/R technique [12, 31]

Playing with power on CPU

- Sprinting (pushing the TDP) [35, 36]
  - frequency sprinting
  - parallel sprinting
  - both parallel and frequency sprinting
- Boosting (respecting the TDP)
  - Intel Turbo Boost [14]
- DVFS (using the manufacturer defined P-states)

Target Platforms



The Single-Chip Cloud Computer (SCC) [6, 5]:

- Voltage and frequency islands
- 48 homogenuous cores
- `/shared` directory between SCC cores and MCPC

x86 commercial platform:

- Intel(R) Core(TM) i7 2630QM Sandy-bridge
- quad core processor with two simultaneous multi-threading (SMT) contexts per core
- acpi-cpufreq driver

Voltage and Frequency relation

Voltage regulators keep voltages within the desired range

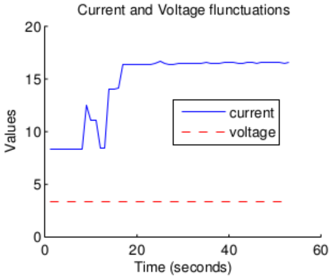
- off-chip
- on-chip

Opperating Performance Point List depict the connection between frequency and voltage

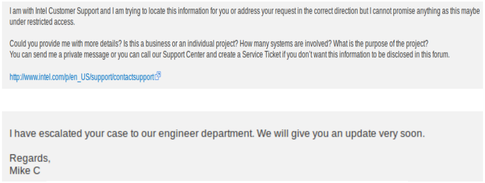
Measuring Energy consumption

For the SCC platform

- we use *sccBmc -c status* to read voltage and current
- we integrate using trapezoidal rule to calculate the Energy consumption



For the x86 platform in discussion with Intel engineers

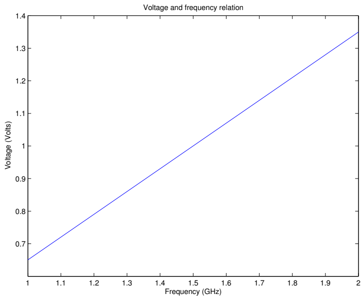

I am with Intel Customer Support and I am trying to locate this information for you or address your request in the correct direction but I cannot promise anything as this maybe under restricted access.

Could you provide me with more details? Is this a business or an individual project? How many systems are involved? What is the purpose of the project?
You can send me a private message or you can call our Support Center and create a Service Ticket if you don't want this information to be disclosed in this forum.

http://www.intel.com/p/en_US/support/contactsupport

I have escalated your case to our engineer department. We will give you an update very soon.

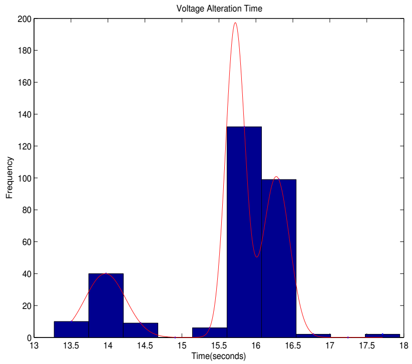
Regards,
Mike C



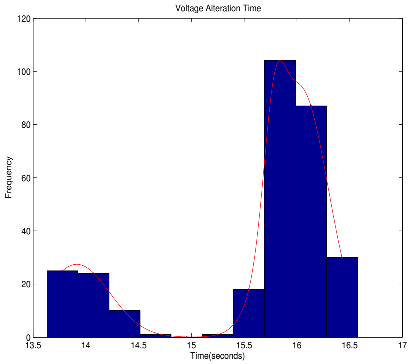
SCC DVFS and overheads

RCCE library provides `RCCE_iset_power()`

From 533 MHz to 800 MHz

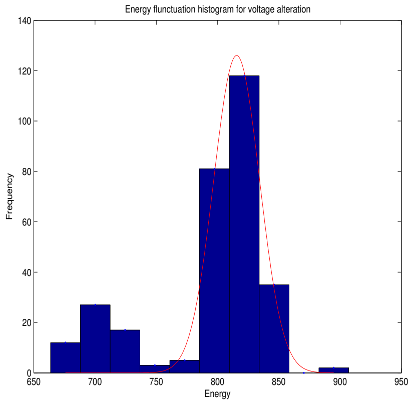


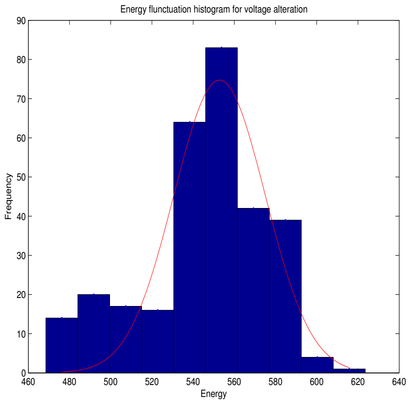
From 800 MHz to 533 MHz



From 533 MHz to 800 MHz

From 800 MHz to 533 MHz





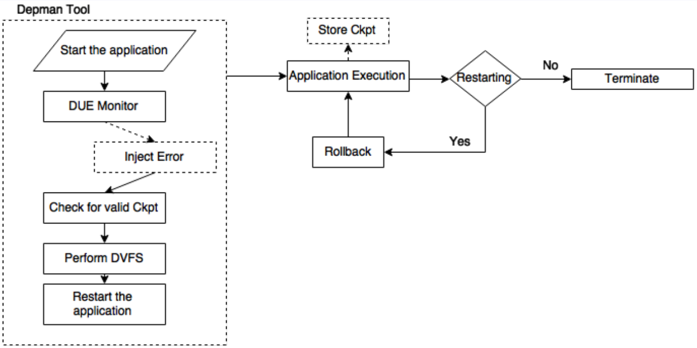
x86 DVFS

CPUfreq governors:

- Performance
- Powersave
- Ondemand
- Conservative
- Userspace, the one used for our scheme

Alterations are performed by changing the `/sys/devices/system/cpu/cpu*/cpufreq` filesystem.
`scaling_setspeed` file is responsible for frequency changes
`cpufrequtils` is used for easier frequency transitions.
Transition latency is about 10 $\mu seconds$

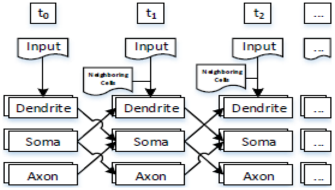
Depman Operation ([31])



Diagnostics: Depman is capable of detecting DUE errors by parsing the application's stdout.
Self Injection: The self injection module induce errors to the execution of the application, with a Weibull distributed probability of

$$P_s = 1 - e^{-\Delta t / MTTF} \tag{1}$$

Target Application and C/R procedure



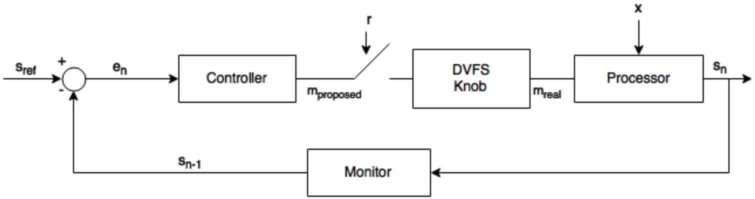
Our target application is the Infoli simulator [15], implementing data parallelism, based on the Hodgkin-Huxley model [24]. We use double buffered checkpoint files to save the application state, which contain:

- simulation step
- the number of cells
- the number of cores
- soma,dentrite,axon compartments

The Restart procedure consists of:

- the restoration of data from checkpoint files
- finding maximum simulation step to restart
- performing output reconstruction if needed

DVFS module



DVFS module work as a Finite-State Machine (FSM). PID control implementations have been proposed [37]

s	application slack
m	frequency multiplier
x	timing noise
r	number of errors per DVFS change
e_n	$s_{\mathtt{ref}} - s_{\mathtt{n-1}}$

Timing Noise Quantification

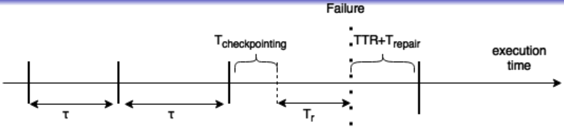
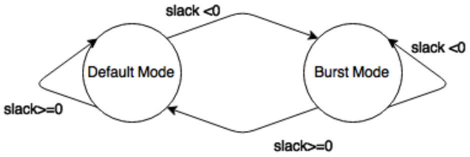


Figure: Modelling the Checkpoint cycle

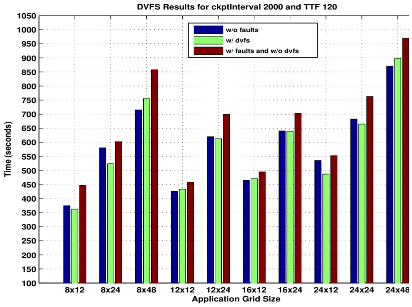
τ is the Checkpoint Interval

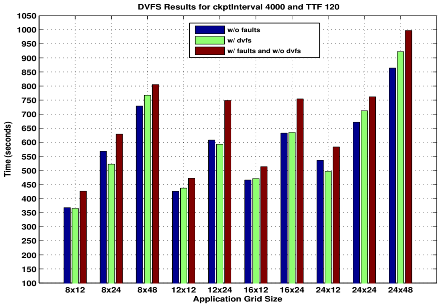
- Rollback Time (T_r)
- Time to Restart (TTR)
- Repair Time (T_{repair})
- Checkpoint Time ($T_{\text{checkpointing}}$)

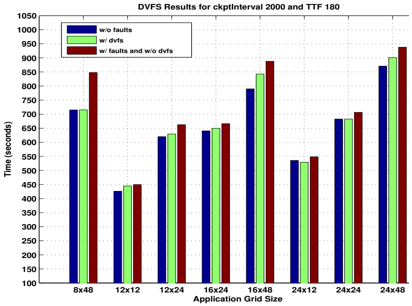
SCC implementation

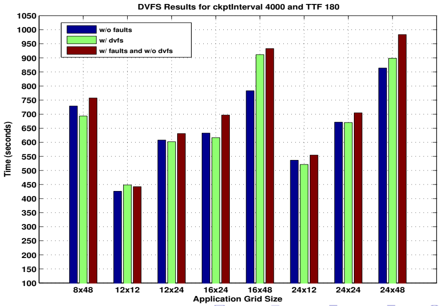


$$\begin{aligned} s_{new} &= s_{previous} - timeOverheads + \\ &+ \underbrace{(lastTTF \times curFreq - lastTTF \times defFreq)}_{\text{depicts the time overhead that has been reclaimed}} \end{aligned} \tag{2}$$


DVFS Results for ckptInterval 2000 and TTF 120
w/o faults
w/ dvfs
w/ faults and w/o dvfs
Time (seconds)
Application Grid Size
8x12
8x24
8x48
12x12
12x24
16x12
16x24
24x12
24x24
24x48


DVFS Results for ckptInterval 4000 and TTF 120
w/o faults
w/ dvfs
w/ faults and w/o dvfs
Time (seconds)
Application Grid Size
8x12
8x24
8x48
12x12
12x24
16x12
16x24
24x12
24x24
24x48


DVFS Results for ckptInterval 2000 and TTF 180
w/o faults
w/ dvfs
w/ faults and w/o dvfs
Time (seconds)
Application Grid Size
8x48
12x12
12x24
16x24
16x48
24x12
24x24
24x48


DVFS Results for ckptInterval 4000 and TTF 180
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Time (seconds)
Application Grid Size
8x48
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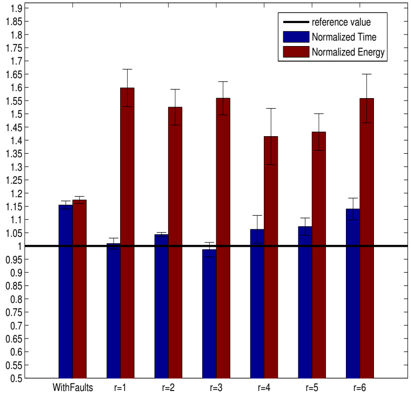
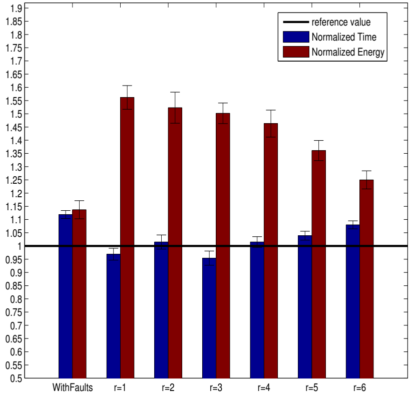
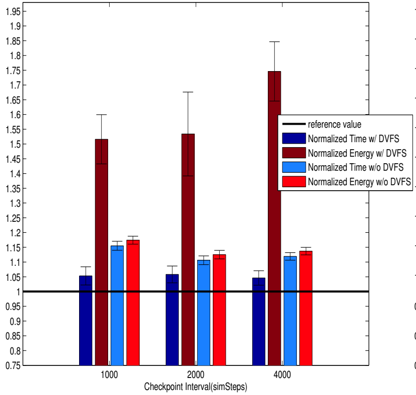


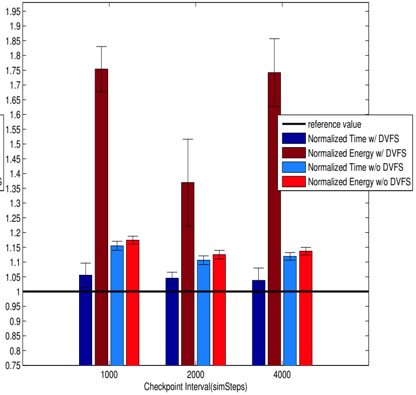


ckptInt=1000 ckptInt=4000

SCC Results, TTF: 122 sec, Time Reference: 823 seconds and Energy Reference: 29210 Joules



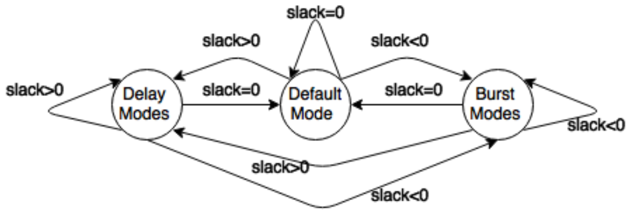
r=1



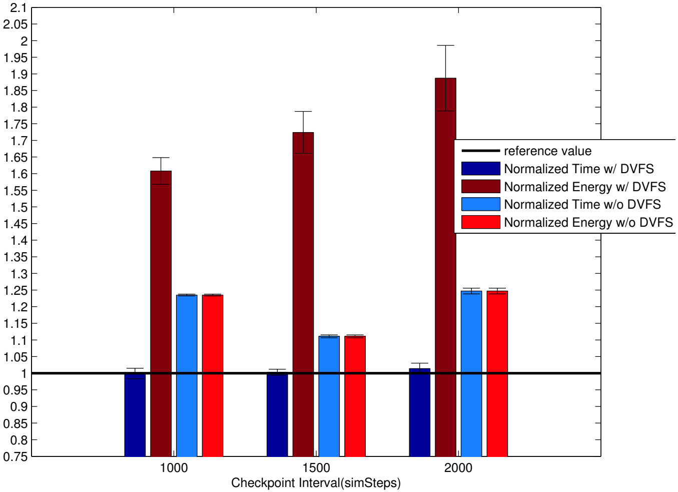
r=3

SCC Results, Weibull distributed TTF, Time Reference: 823 seconds and Energy Reference: 29210 Joules

x86 First Implementation

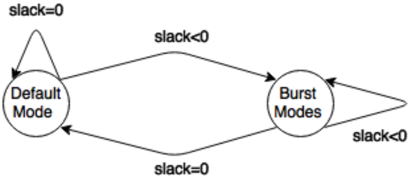


$$newFreq = \frac{-s + defFreq \times MTTF}{MTTF} \tag{3}$$

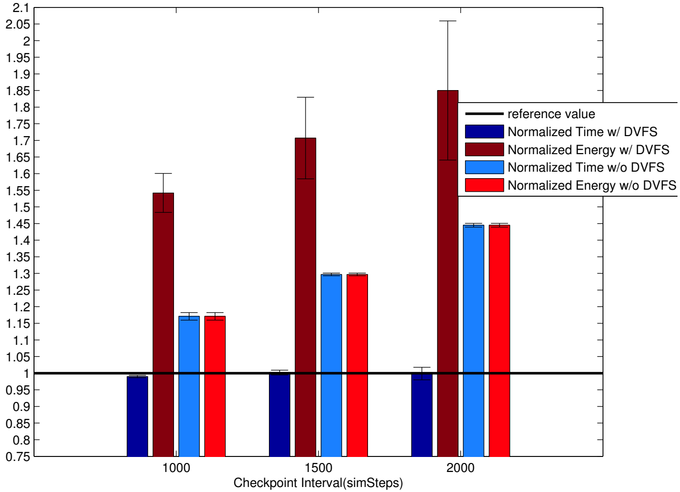


Weibull distributed TTF, Time Reference: 578 seconds and Energy normalized, based on $P \propto f \times V_{dd}^2$

x86 Second Implementation



$$reclaimingTime = \frac{-s}{determinedFreq - defFreq} \tag{4}$$



Weibull distributed TTF, Time Reference: 494 seconds and Energy

Energy normalized, based on P $\propto$ f $\times V_{dd}^2$

Conclusions

- Depman is operating on any platform and can be easily adjusted to any application
- Our scheme needs no additional run time parameters as it can estimate the total time overheads on the fly and perform the available countermeasures
- It seems that the DVFS module is capable of absorbing the time overheads introduced by the C/R procedure
- The additional feature of dependable performance comes at an energy cost

Future Work

- Adopt parallel sprinting besides DVFS
- Use Depman as a main component for distributed systems C/R and synchronization
- Export the DVFS module as a library used by programmers
- Adopt DVFS techniques by web-servers to improve responsiveness
- Modify Depman from the fail-stop model, as to react to multiple events

Acknowledgements

I would like to personally thank Professor D.Soudris and Phd candidate D.Rodopoulos for their guidance and support throughout our cooperation.

Thank you all for your attention!

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