Altera Innovators Day 2025 Update

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***Abstract*—Altera Innovators Day 2025 introduced production-ready Agilex 5 and 3 devices, with new high-density D-Series Agilex 5 FPGAs, Quartus 25.3 enhancements with Visual Designer and Nios-V debug, and FPGA AI Suite 25.3 featuring DDR-Free inference for faster, memory-efficient edge performance.**

Altera Innovators Day 2025

Altera Innovators Day 2025 served as a event for engineers, developers, and partners to explore the latest advancements in the company's FPGA products and development tools. The event highlighted how Altera's renewed independence and focus on user experience are shaping the future of their FPGA development. I had the opportunity to attend technical sessions, live demonstrations, and collaborative discussions as the conference emphasized Altera's vision of simplifying FPGA adoption and accelerating innovation, particularly in AI-driven applications. I was grateful to participate as a content creator and to represent the educational, hobbyist, and open-source FPGA communities.

Agilex FPGA Update

Altera emphasized its FPGA performance and power efficiency relative to the current market, highlighting bold claims that the latest Agilex devices can achieve fabric frequencies approaching 600 MHz [1], [2]. Equally notable was the company's confirmation that the Agilex 5 and Agilex 3 families have entered production, marking the completion of the first generation of Agilex FPGAs. It is encouraging to see Altera's return to more accessible, low-cost product lines. I hope this direction sparks renewed interest in education, research, and hobbyist development. Finally, Altera introduced the new "big" Agilex 5 D-Series devices [3], featuring up to 1.6 million logic elements and expanded DDR5 and LPDDR5 interfaces. These high-density FPGAs are intended to handle larger applications such as CNN models, and take full advantage of Altera's new Tensor DSPs for AI acceleration.

Partner Development Boards

Altera's partner ecosystem offers a variety of development platforms that make the Agilex™ family accessible across a broad range of performance and cost tiers. Some of the platforms I am interested in are summarized here.

The **Arrow AXE5-Falcon Development Kit** (Figure 1) features an Agilex 5 E-Series SoC with integrated ARM cores, DDR memory, and HDMI connectivity [4]. It uses a compact Raspberry Pi-style form factor and should support standard Pi HATs, though it doesn't seem to include a PCIe connector.

Terasic's Agilex 3 boards, including the Atum A3 Nano and DE23-Lite, focus on compact and educational applications [5]. These platforms combine small board footprints with HDMI output, SDRAM, and USB-Blaster III connectivity, offering a balanced and cost-effective entry point for FPGA learning and experimentation.

Trenz Electronic's TEI0187 module provides a system-on-module approach [6]. It integrates an Agilex 5 E-Series FPGA within a 5.2×7.6 cm package, optimized for integration into custom carrier boards and space-constrained embedded designs.

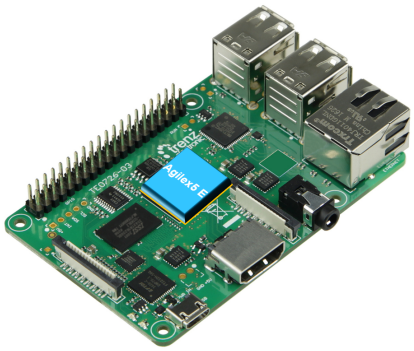

Fig. 1. Arrow AXE5-Falcon Development Kit [4].

Quartus Prime 25.3 Update

Altera's Quartus® Prime 25.3 release delivers one of the most substantial toolchain updates in recent years, introducing major enhancements in design visualization and debugging efficiency [7].

A key highlight is the new **Visual Designer Studio**, which provides an intuitive block-diagram environment with integrated Avalon and AXI interface support, along with seamless integration for custom HDL IP cores (see Figure 2). This environment enables faster deployment of both vendor and user-defined IP, supporting complex data processing pipelines.

Another major improvement is the addition of SignalTap support for the **Nios-V** soft processor. Developers can now perform real-time debugging—single stepping, breakpoints, and register inspection—directly within the Quartus environment, greatly simplifying firmware and hardware co-debug workflows. I look forward to exploring how these updates improve system bring-up speed and plan to attempt another "Hello World" speedrun on the Nios-V using the new design and debug tools.

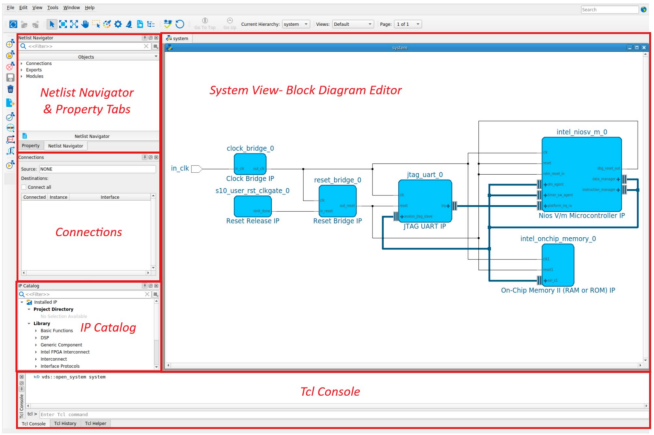

Fig. 2. New Quartus Prime 25.3 Visualizer interface (hierarchical and timing view).

FPGA AI Suite 25.3 Update

With the 25.3 release, Altera's FPGA AI Suite introduces a new feature called **DDR-Free mode**, which leverages on-chip memory resources to eliminate reliance on external DDR interfaces, enabling faster model switching, lower latency, and improved inference efficiency. In one demonstration, a ResNet-50 workload achieved a 27 % increase in frames per second when executed on an Agilex device under DDR-Free mode. The update also adds production support for Agilex 3 devices and includes a hostless JTAG example design for the Agilex C-Series development kit. The FPGA AI Suite is now bundled as an optional component within the Quartus installer and offers deeper integration with the Visual Designer Studio environment [8]. With DDR-Free inference and on-chip memory acceleration now possible, it raises an exciting question—what level of AI model complexity could realistically fit and run efficiently on a compact, edge-oriented Agilex 3 FPGA?

Conclusion

Looking ahead, I am particularly interested in how Altera will expand support for PCIe DMA across the Agilex 5 and Agilex 3 families. I plan to demonstrate a software-defined PCIe endpoint using the Nios-V soft processor paired with a Raspberry Pi host, showcasing the growing accessibility of FPGA-based acceleration. In parallel, I aim to explore JTAG-driven fault injection as a means to evaluate radiation hardness-by-design techniques within Agilex devices.

Building on the new FPGA architectures and toolchain enhancements introduced at Altera Innovators Day 2025, especially with the Quartus 25.3 release and the FPGA AI Suite 25.3 updates. I hope to see continued progress in documentation, step-by-step tutorials, and robust IP examples. Such resources will be essential for helping developers fully exploit the potential of these next-generation Agilex platforms across research, education, and embedded AI applications.

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