


# ECO-CHIP: Estimation of Carbon Footprint of Chiplet-based Architectures for Sustainable VLSI

Chetan Choppali Sudarshan, Nikhil Matkar, Sarma Vrudhula, Sachin S. Sapatnekar, Vidya A. Chhabria

HPCA 2024

# Agenda

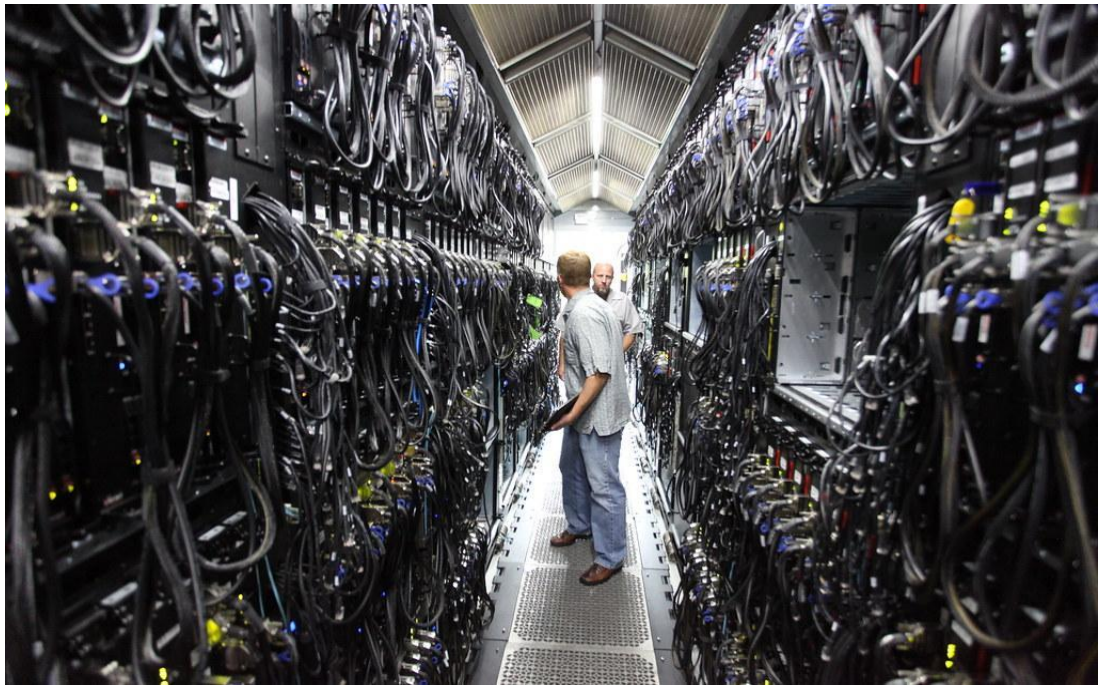
- Introduction
- Prior work
  - Architectural carbon footprint modeling (ACT)
- ECO-CHIP
  - HI Pathway to sustainability
  - Framework
  - ECO-CHIP carbon footprint models
  - Key takeaways
- Conclusion

# Agenda

- **Introduction**
- Prior work
  - Architectural carbon footprint modeling (ACT)
- ECO-CHIP
  - HI Pathway to sustainability
  - Framework
  - ECO-CHIP carbon footprint models
  - Key takeaways
- Conclusion

# Information and Computing Technology (ICT)

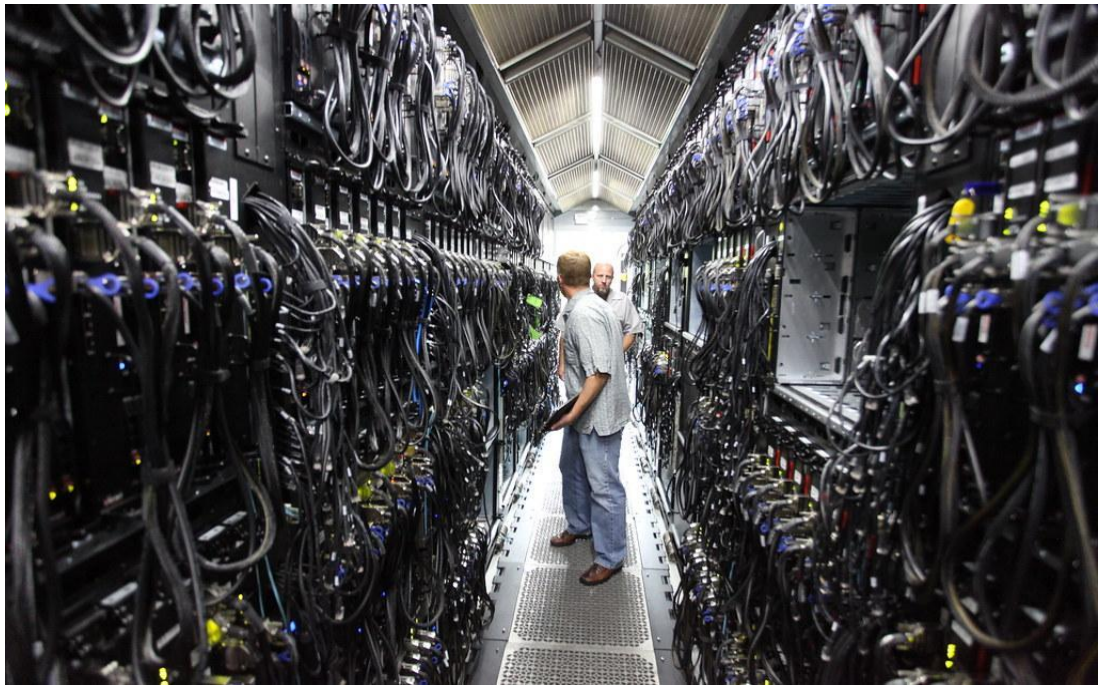
## Data Center and Networks



## User devices

# Information and Computing Technology (ICT)

## Data Center and Networks

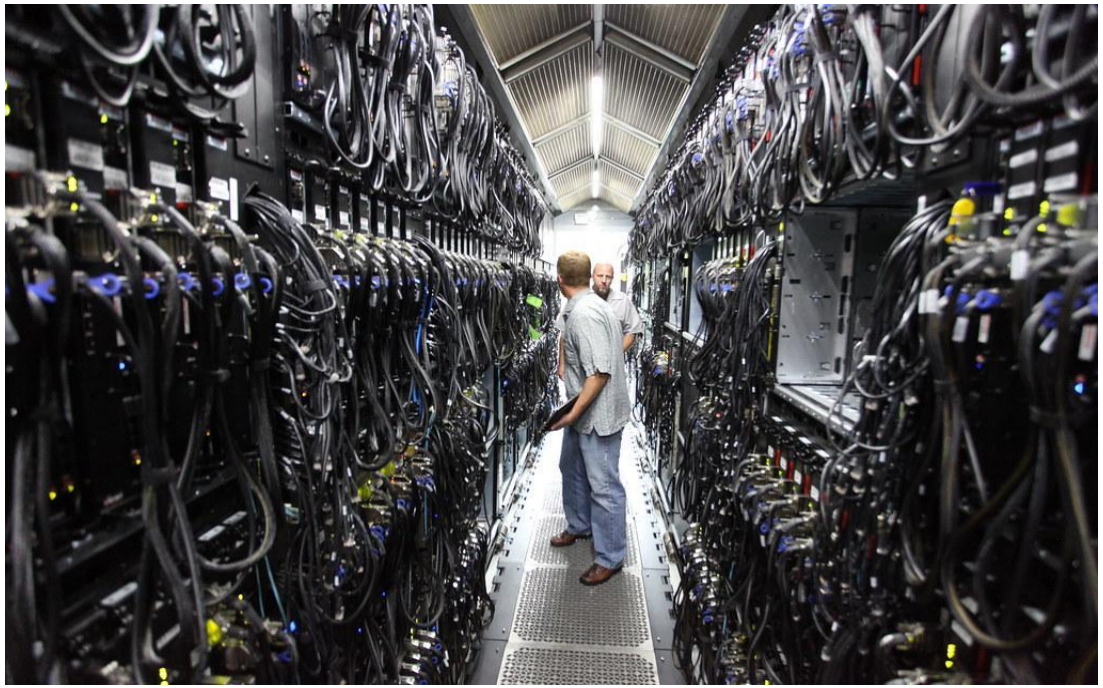


## User devices


- ICT contributes to 3-4% of the total world carbon footprint (CFP) Source : C. Freitag et al., Patterns 2021
- Need for sector-wide regulations

# Information and Computing Technology (ICT)

## Data Center and Networks



## User devices


- ICT contributes to 3-4% of the total world carbon footprint (CFP) Source : C. Freitag et al., Patterns 2021
- Need for sector-wide regulations

# Industry and government interest

PRESS RELEASE
July 21, 2020

**Apple commits to be 100 percent carbon neutral for its supply chain and products by 2030**

**Intel Vows to Reach Net-Zero Greenhouse Gas Emissions by 2040, Shaping a Greener Tech Industry**

by ESG News • November 23, 2023 Share:

# Industry and government interest

PRESS RELEASE
July 21, 2020

## Apple commits to be 100 percent carbon neutral for its supply chain and products by 2030

## Intel Vows to Reach Net-Zero Greenhouse Gas Emissions by 2040, Shaping a Greener Tech Industry

by ESG News • November 23, 2023 Share:

U.S. National Science Foundation

Find Funding & Apply Manage Your Award Focu


Home / Funding at NSF / Funding Search / Design for Environmental Sustainability in Computing (DESC)

**Important information for proposers**
All proposals must be submitted in accordance with the requirements specified in this funding opportunity and in the NSF Proposal & Award Policies & Procedures Guide (PAPPG) that is in effect..

Supports foundational research addressing the substantial environmental impacts of computing. Projects should surpass studies of energy efficiency alone, pursuing dramatic improvements to overall sustainability.

NSF 22-060

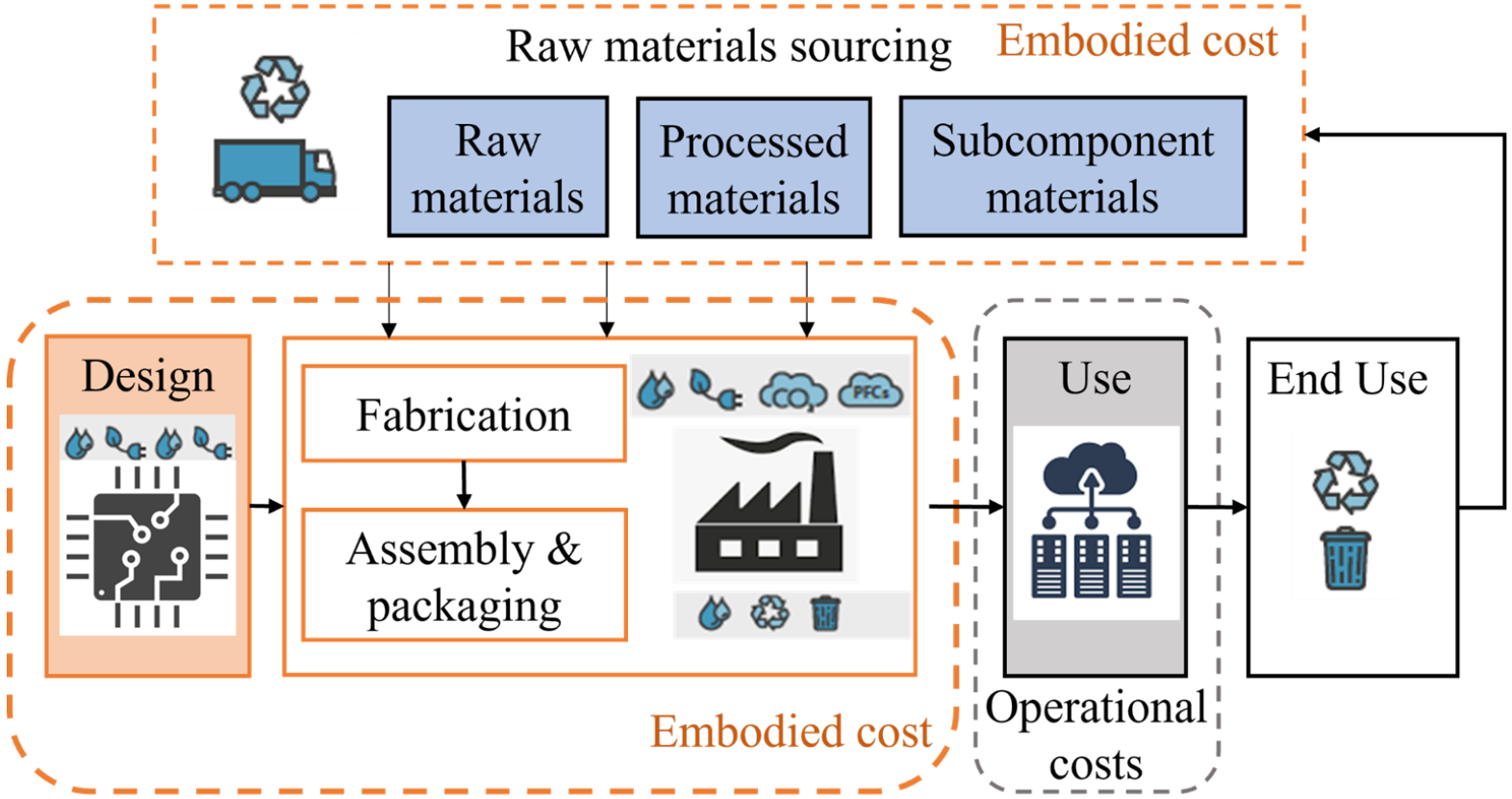
### Dear Colleague Letter: Design for Sustainability in Computing

March 15, 2022

Dear Colleagues:

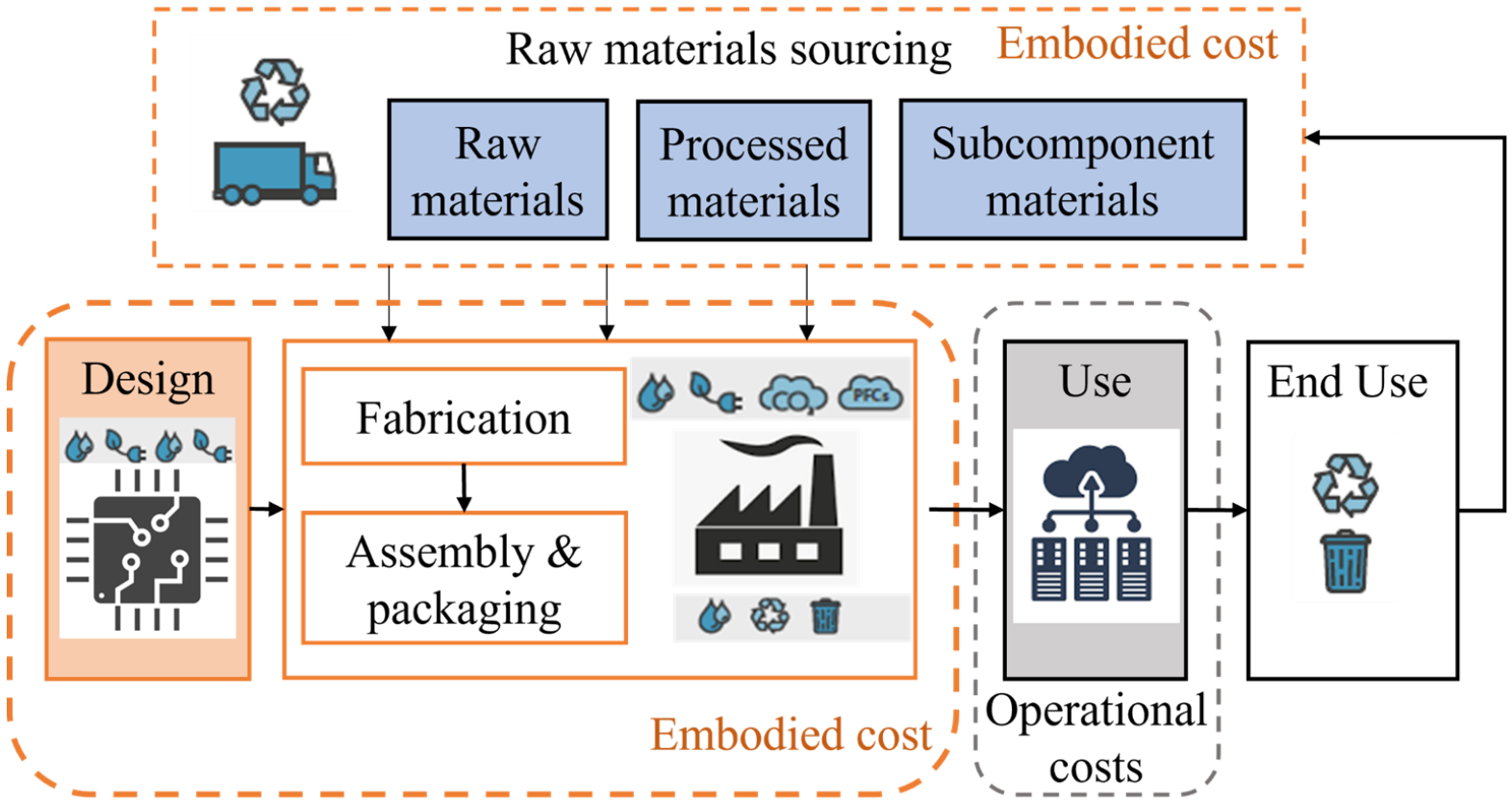
Environmental impacts of computing technologies extend well beyond their energy consumption and require a holistic focus on broader sustainability. Negative impacts of greenhouse gas emissions, depletion of rare earth elements, and e-waste are exacerbated by the proliferation of computing throughout society and treatment of computing systems as disposable commodities with planned obsolescence. Furthermore, environmental concerns range from the better-known carbon footprint from energy consumption (e.g., cloud) to equally important concerns of embodied carbon[1], generation of methane, carcinogens, volatile organic compounds, and eutrophication, among others. Widespread use of compute intensive techniques (e.g., blockchain and artificial intelligence), handling and moving massive amounts of data, the rollout of next generation

# Silicon lifecycle and sources of carbon



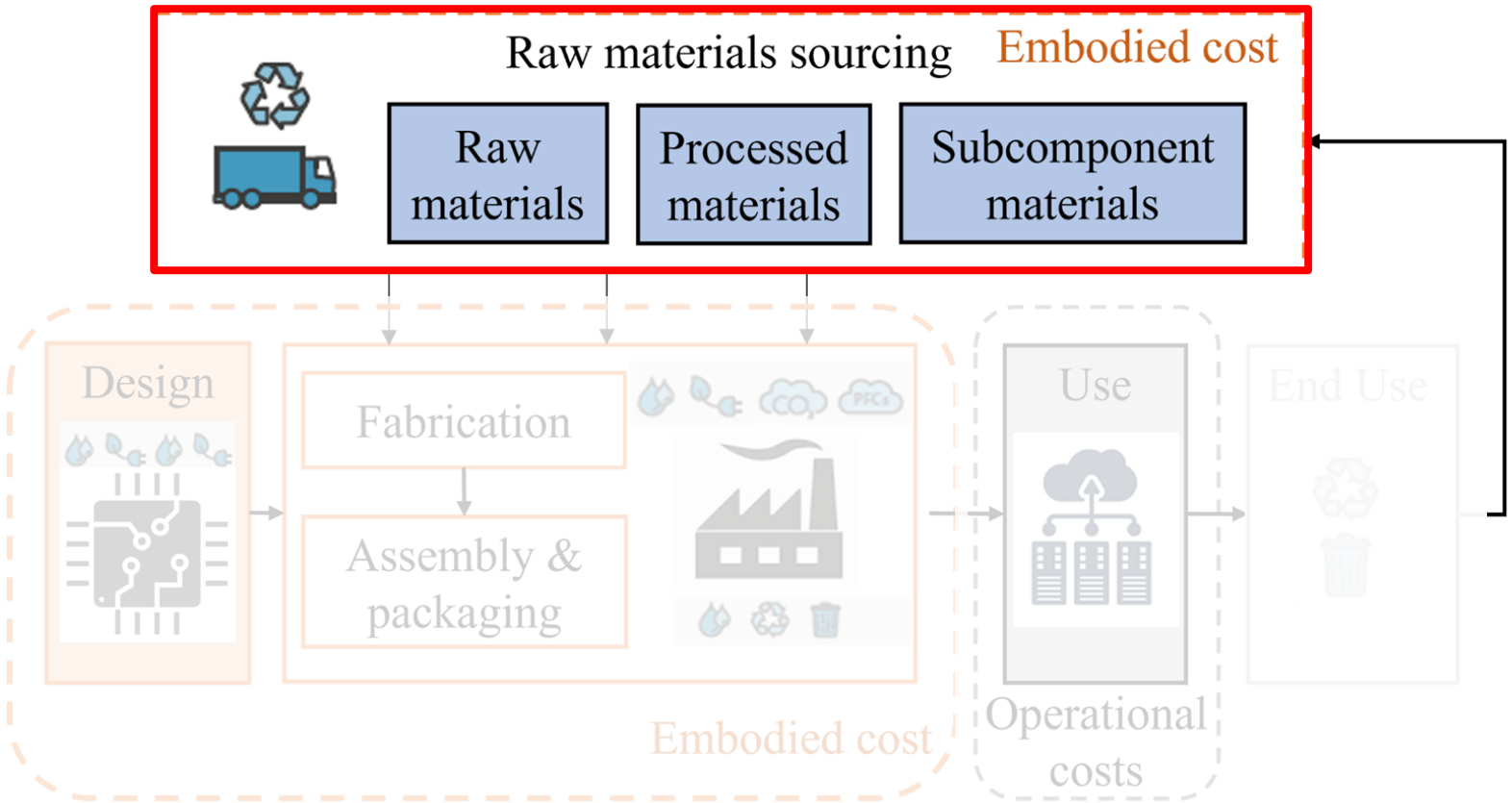
# Silicon lifecycle and sources of carbon

- Embodied carbon footprint (CFP)
  - Raw material CFP
  - Design CFP
  - Manufacturing and packaging CFP
- Operational CFP
  - CFP from end-user



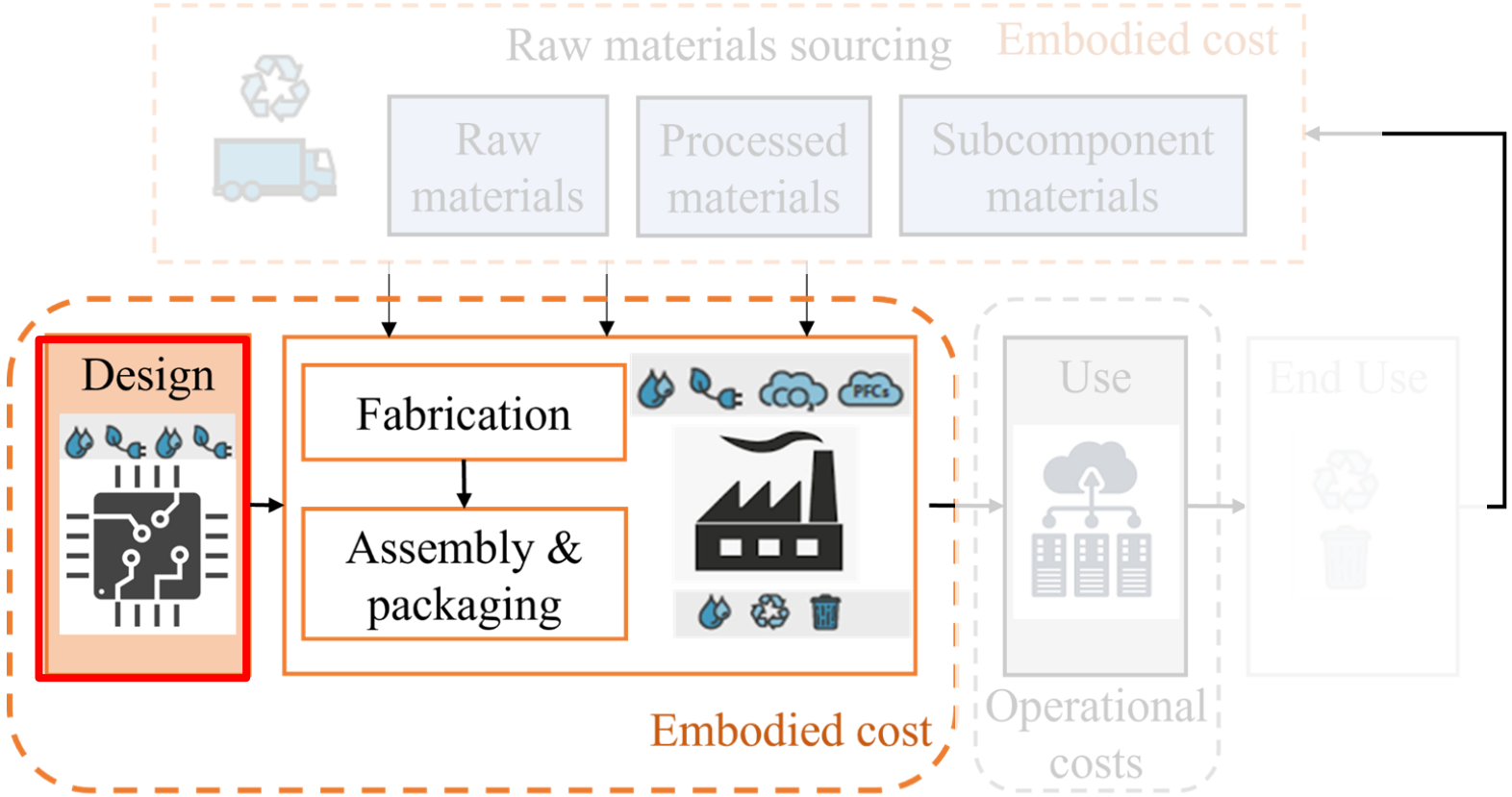
# Silicon lifecycle and sources of carbon

- Embodied carbon footprint (CFP)
  - Raw material CFP
  - Design CFP
  - Manufacturing and packaging CFP
- Operational CFP
  - CFP from end-user



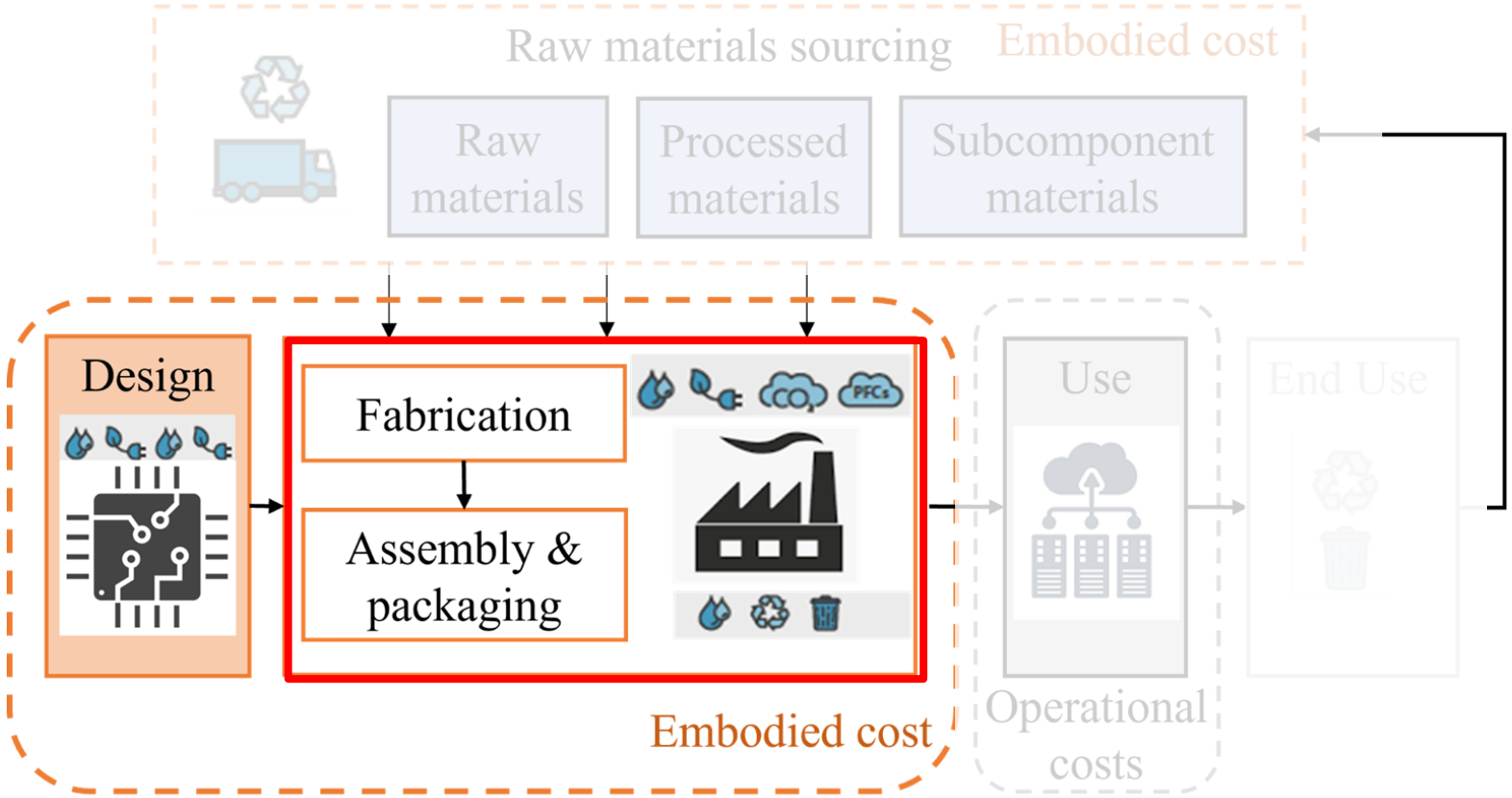
# Silicon lifecycle and sources of carbon

- Embodied carbon footprint (CFP)
  - Raw material CFP
  - Design CFP
  - Manufacturing and packaging CFP
- Operational CFP
  - CFP from end-user



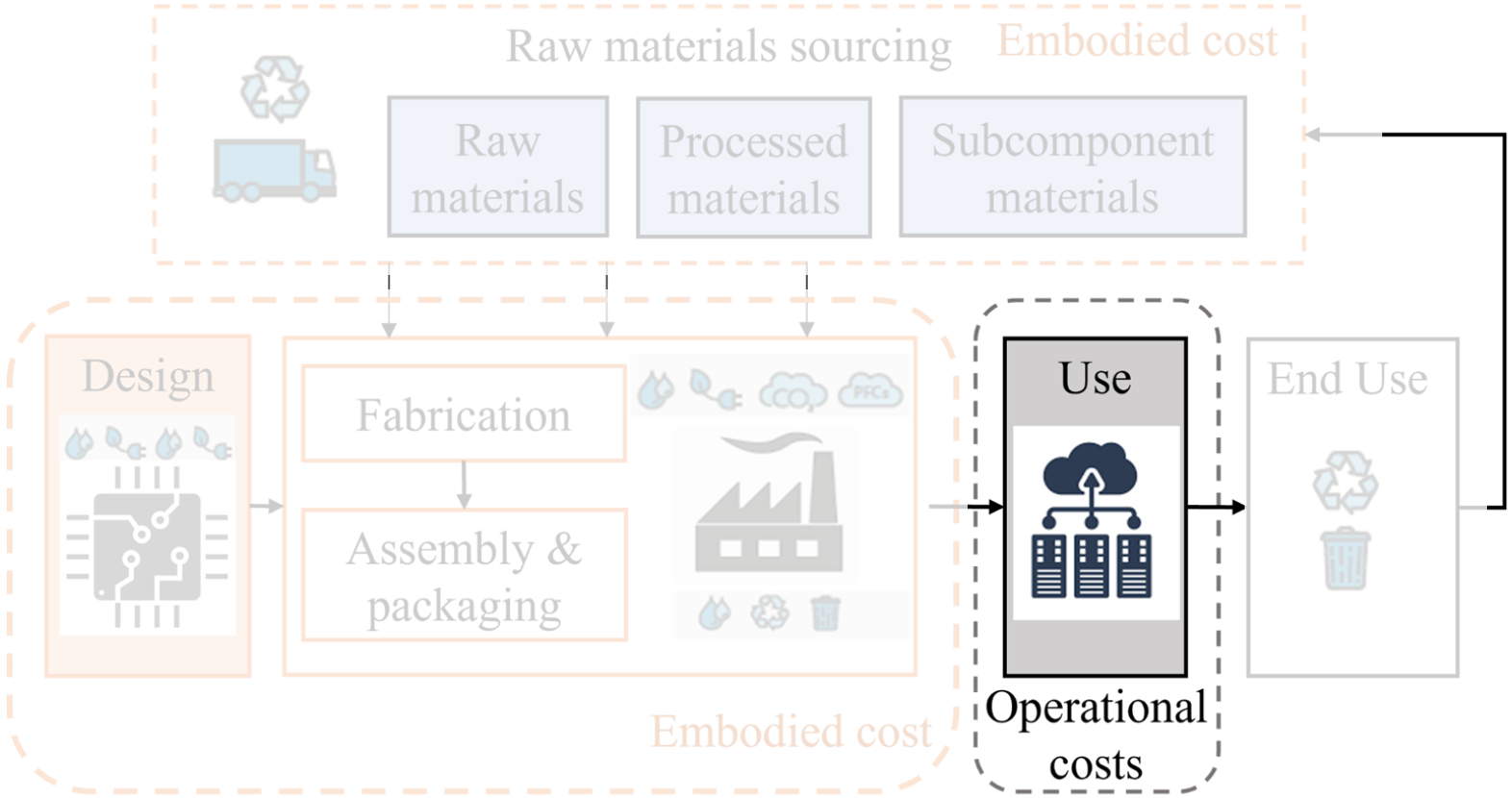
# Silicon lifecycle and sources of carbon

- Embodied carbon footprint (CFP)
  - Raw material CFP
  - Design CFP
  - Manufacturing and packaging CFP
- Operational CFP
  - CFP from end-user



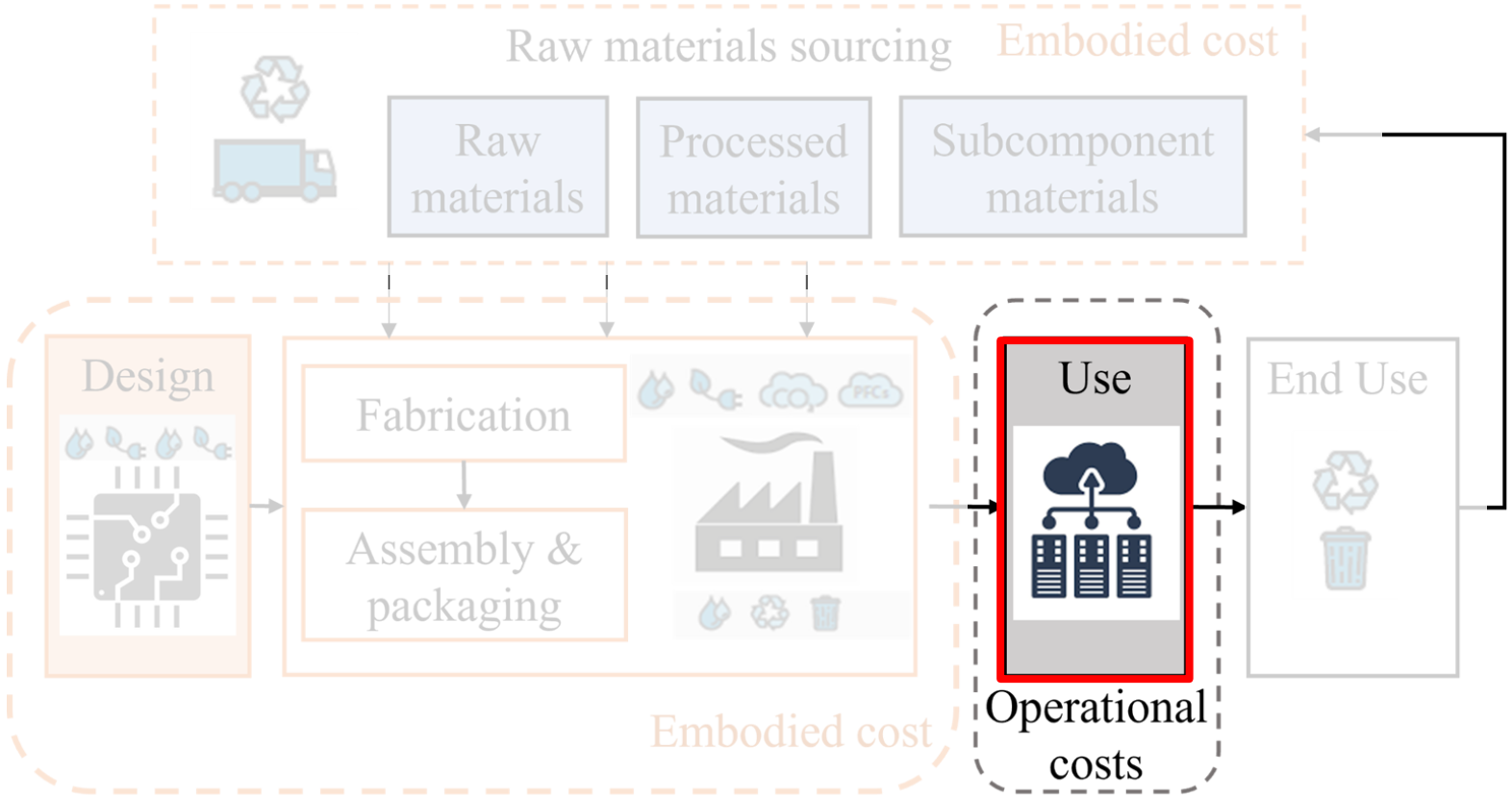
# Silicon lifecycle and sources of carbon

- Embodied carbon footprint (CFP)
  - Raw material CFP
  - Design CFP
  - Manufacturing and packaging CFP
- Operational CFP
  - CFP from end-user



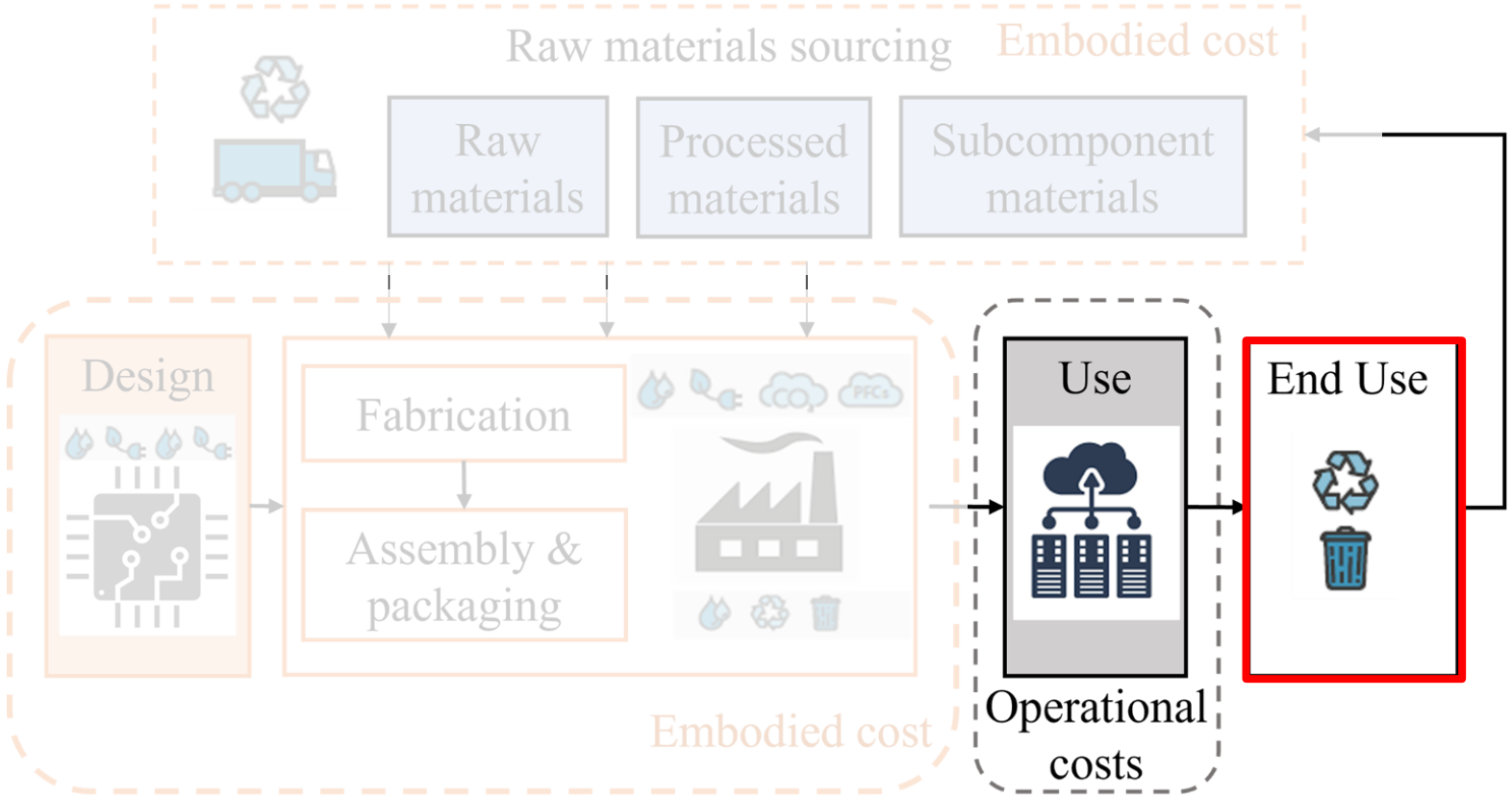
# Silicon lifecycle and sources of carbon

- Embodied carbon footprint (CFP)
  - Raw material CFP
  - Design CFP
  - Manufacturing and packaging CFP
- Operational CFP
  - CFP from end-user

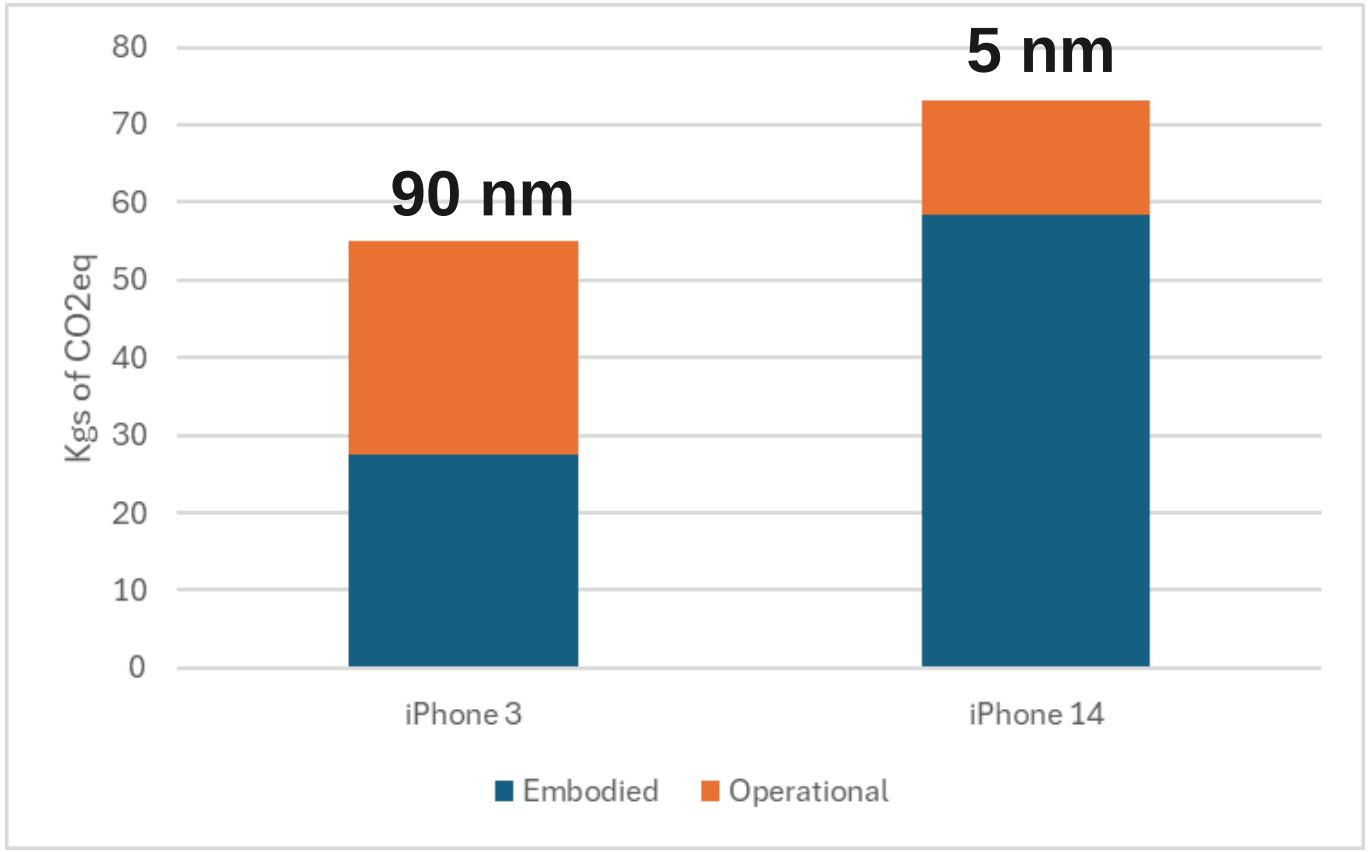


# Silicon lifecycle and sources of carbon

- Embodied carbon footprint (CFP)
  - Raw material CFP
  - Design CFP
  - Manufacturing and packaging CFP
- Operational CFP
  - CFP from end-user



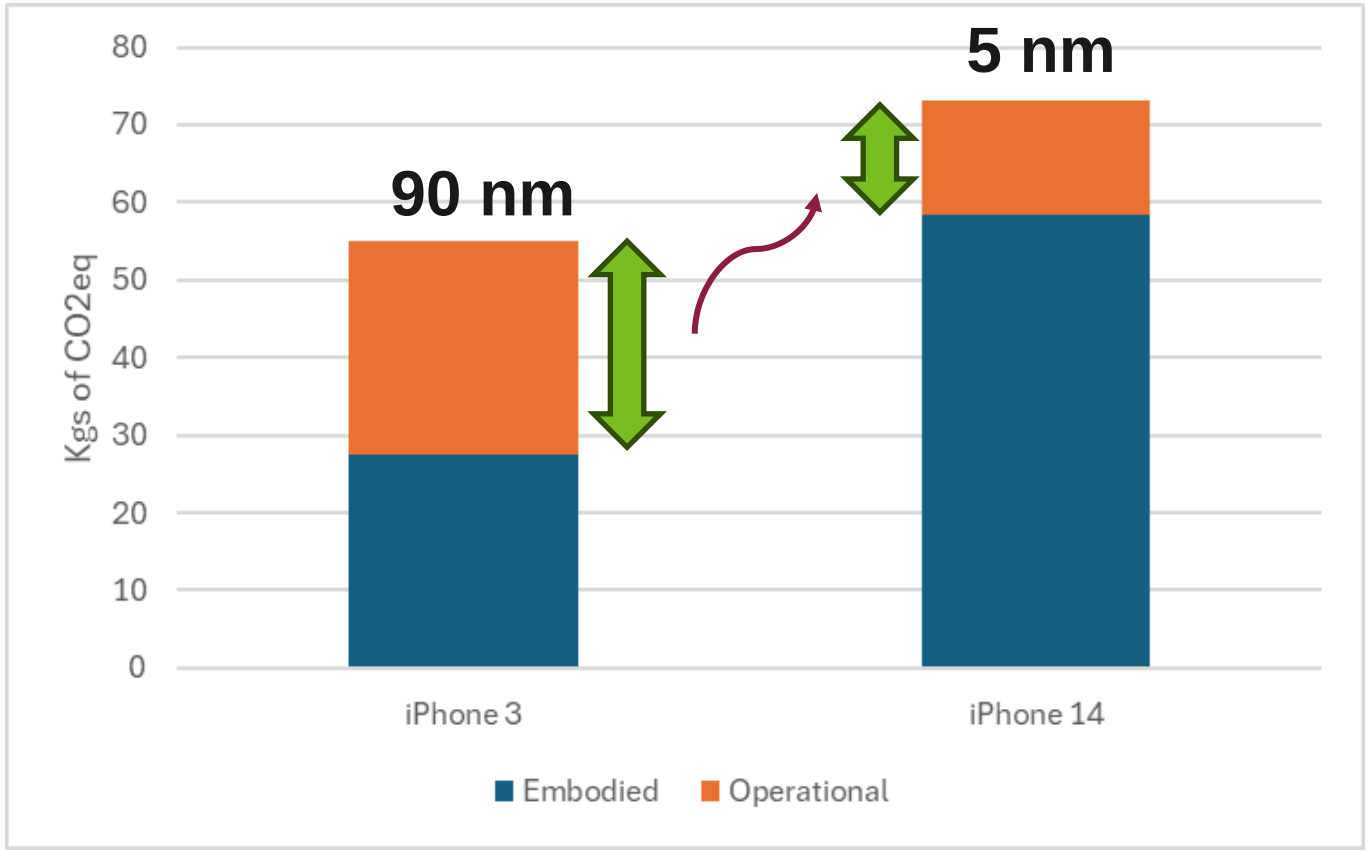
# Challenges and demands




Source : Apple sustainability reports

# Challenges and demands

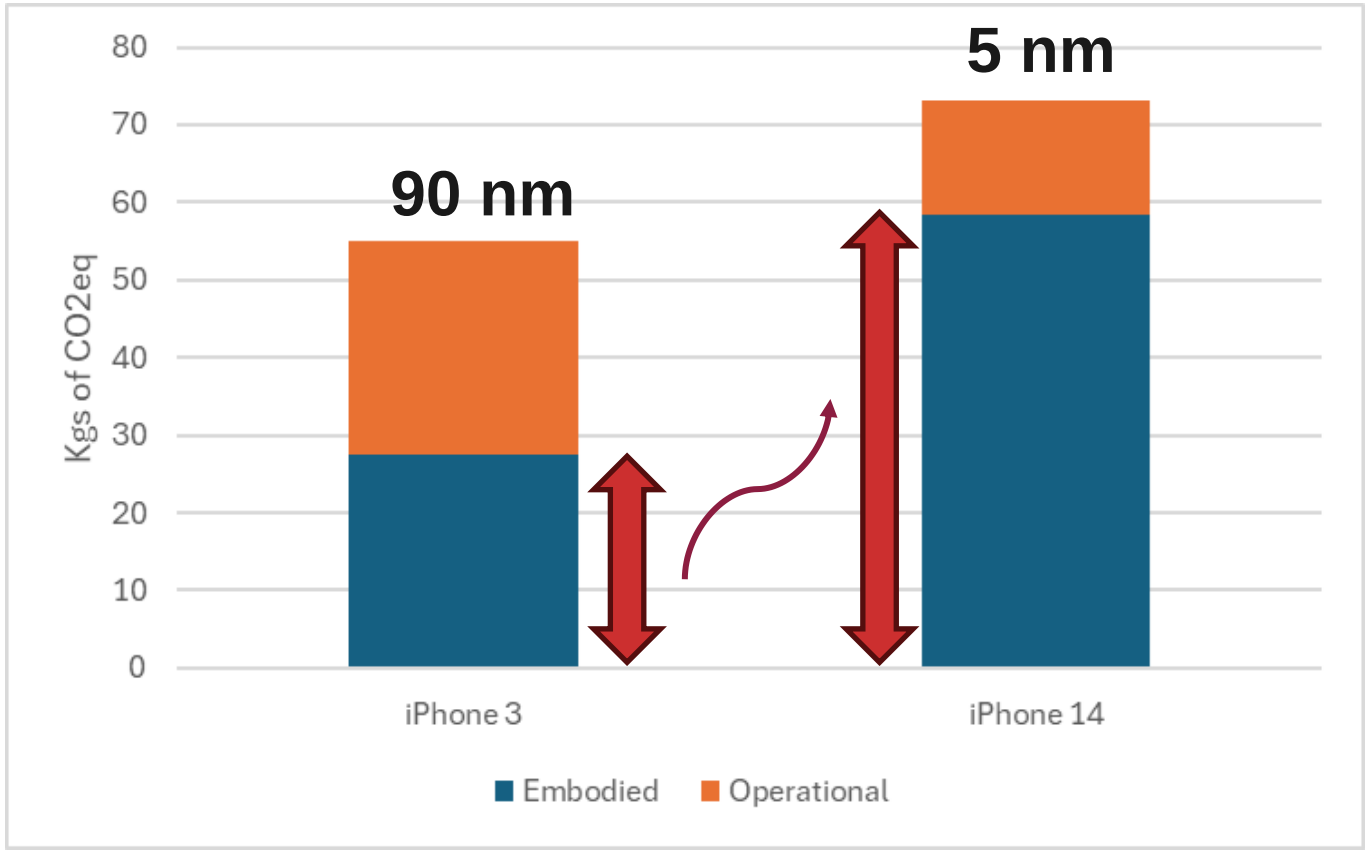
- Efficiency optimization
  - Operational CFP drops 46%
- Rising embodied carbon
  - Embodied CFP increases 110%




Source : Apple sustainability reports

# Challenges and demands

- Efficiency optimization
  - Operational CFP drops 46%
- Rising embodied carbon
  - Embodied CFP increases 110%




Source : Apple sustainability reports

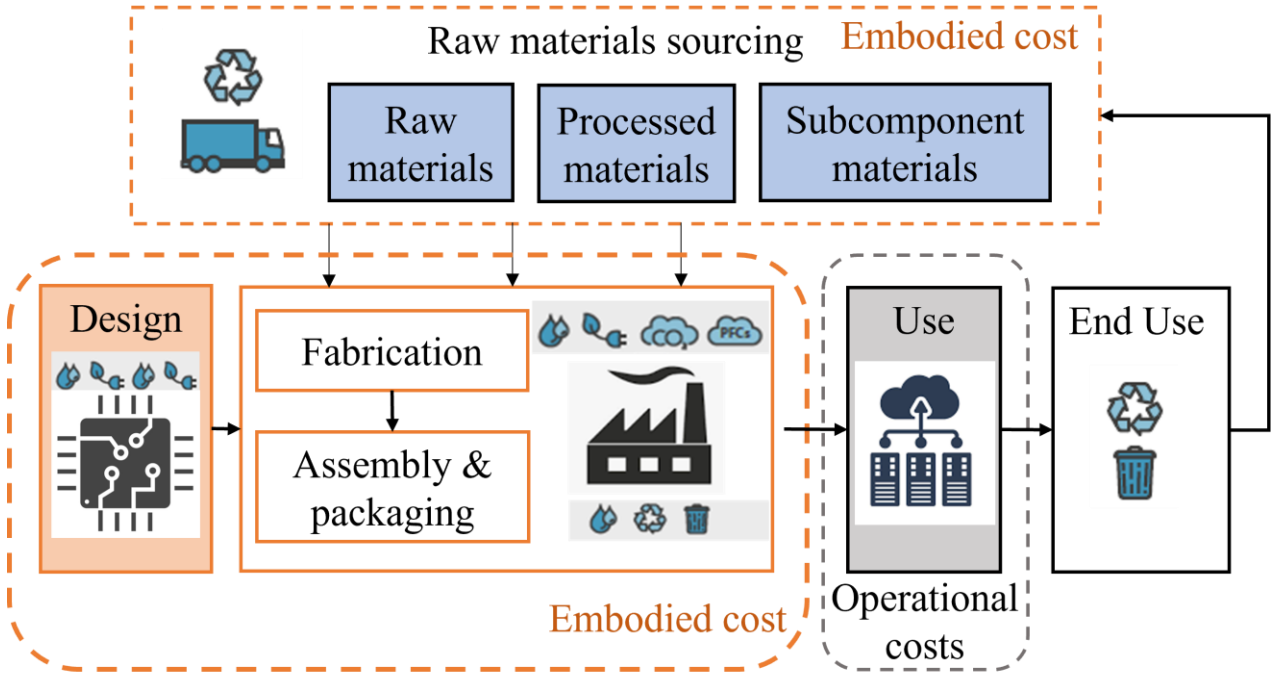
# Agenda

- Introduction
- **Prior work**
  - **Architectural carbon footprint modeling (ACT)**
- ECO-CHIP
  - HI Pathway to sustainability
  - Framework
  - ECO-CHIP CFP models
  - Key takeaways
- Conclusion

# Prior work

## Architectural Carbon Model Tool (ACT)

- ISCA 2022
- Carbon-aware exploration framework
- Architectural model estimating embodied carbon
- Based on industry reports

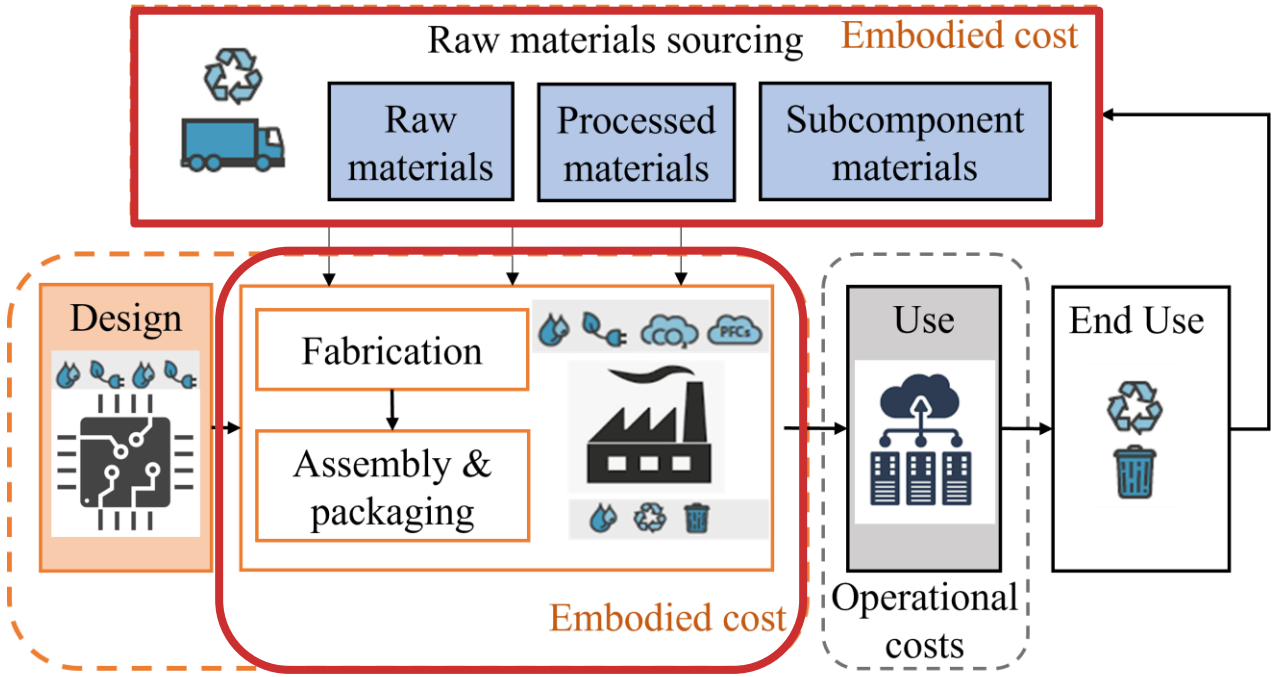



Udit Gupta, Mariam Elgamal, Gage Hills, Gu-Yeon Wei, Hsien-Hsin S. Lee, David Brooks, and Carole-Jean Wu. 2022. ACT: designing sustainable computer systems with an architectural carbon modeling tool. In Proceedings of the 49th Annual International Symposium on Computer Architecture (ISCA '22)

# Prior work

## Architectural Carbon Model Tool (ACT)

- ISCA 2022
- Carbon-aware exploration framework
- Architectural model estimating embodied carbon
- Based on industry reports

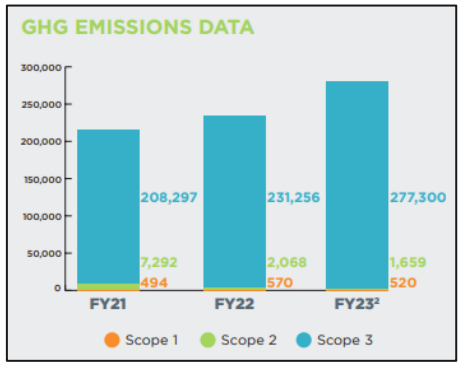


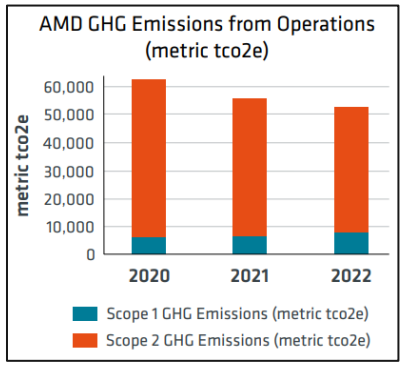

Udit Gupta, Mariam Elgamal, Gage Hills, Gu-Yeon Wei, Hsien-Hsin S. Lee, David Brooks, and Carole-Jean Wu. 2022. ACT: designing sustainable computer systems with an architectural carbon modeling tool. In Proceedings of the 49th Annual International Symposium on Computer Architecture (ISCA '22)

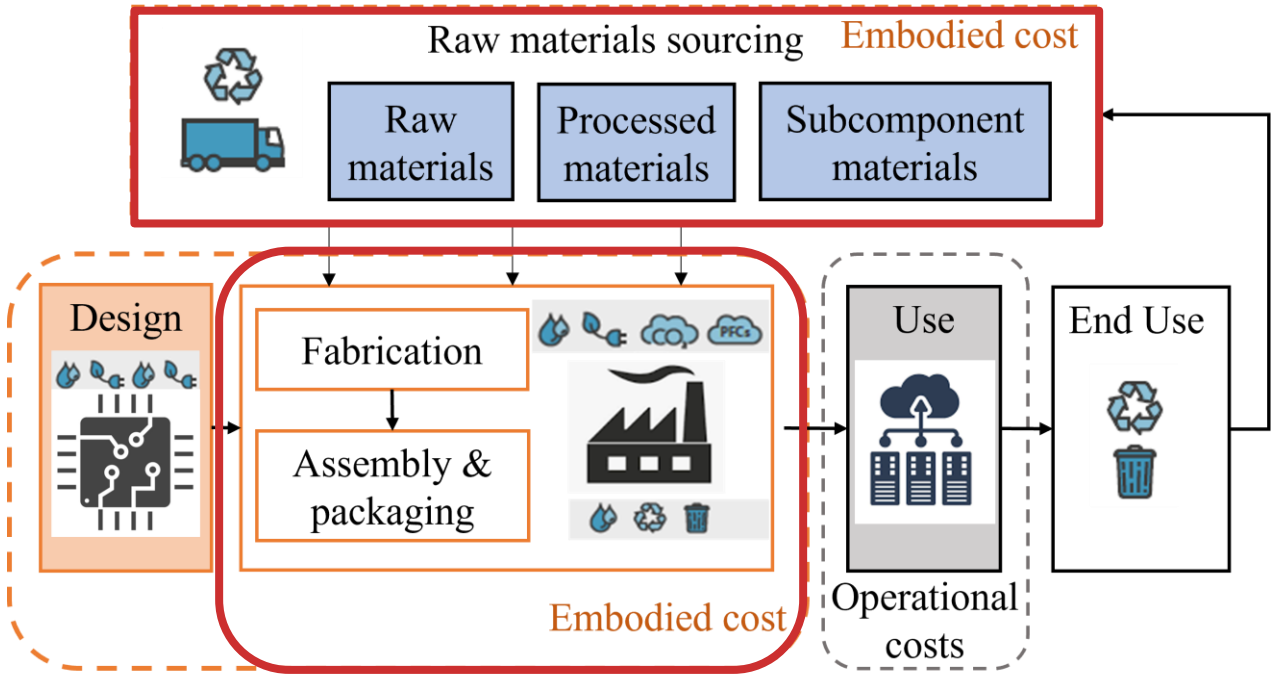
# Prior work

## Architectural Carbon Model Tool (ACT)

- ISCA 2022
- Carbon-aware exploration framework
- Architectural model estimating embodied carbon
- Based on industry reports




Udit Gupta, Mariam Elgamal, Gage Hills, Gu-Yeon Wei, Hsien-Hsin S. Lee, David Brooks, and Carole-Jean Wu. 2022. ACT: designing sustainable computer systems with an architectural carbon modeling tool. In Proceedings of the 49th Annual International Symposium on Computer Architecture (ISCA '22)

# This work: Our approach to sustainable computing

3R’s for sustainability

- Reduce
- Reuse
- Recycle

# This work: Our approach to sustainable computing

3R’s for sustainability

- Reduce
- Reuse
- Recycle

# This work: Our approach to sustainable computing

3R’s for sustainability

- Reduce
- Reuse
- Recycle


**Our approach**

# This work: Our approach to sustainable computing

3R's for sustainability

- Reduce
- Reuse
- Recycle

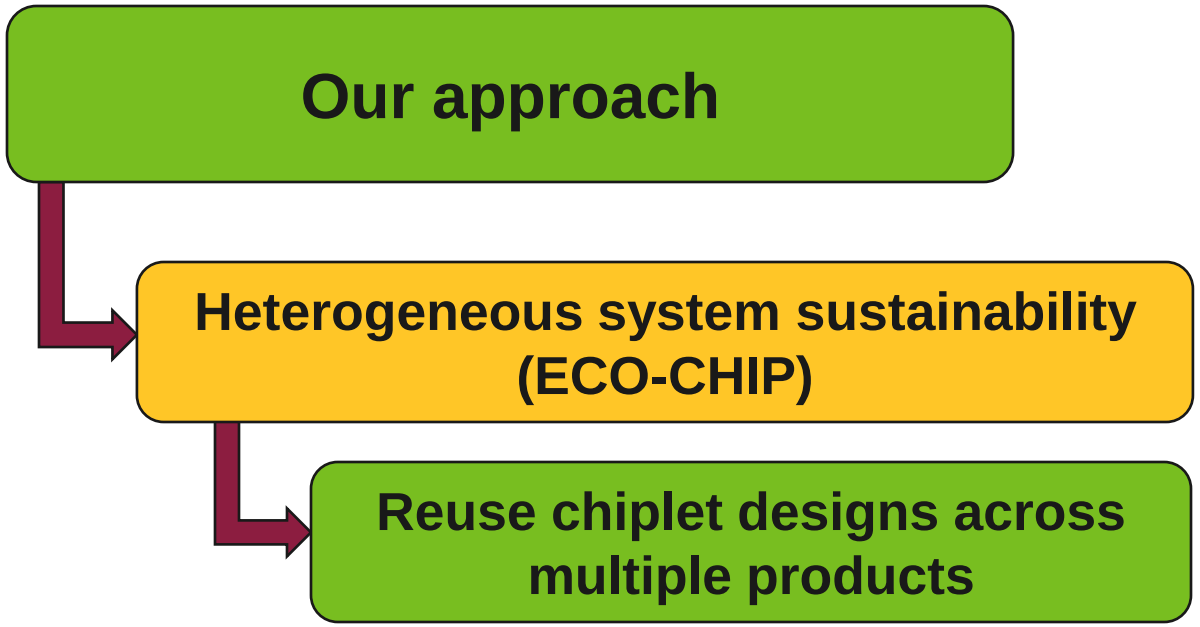

**Our approach**

**Heterogeneous system sustainability (ECO-CHIP)**

# This work: Our approach to sustainable computing

3R's for sustainability

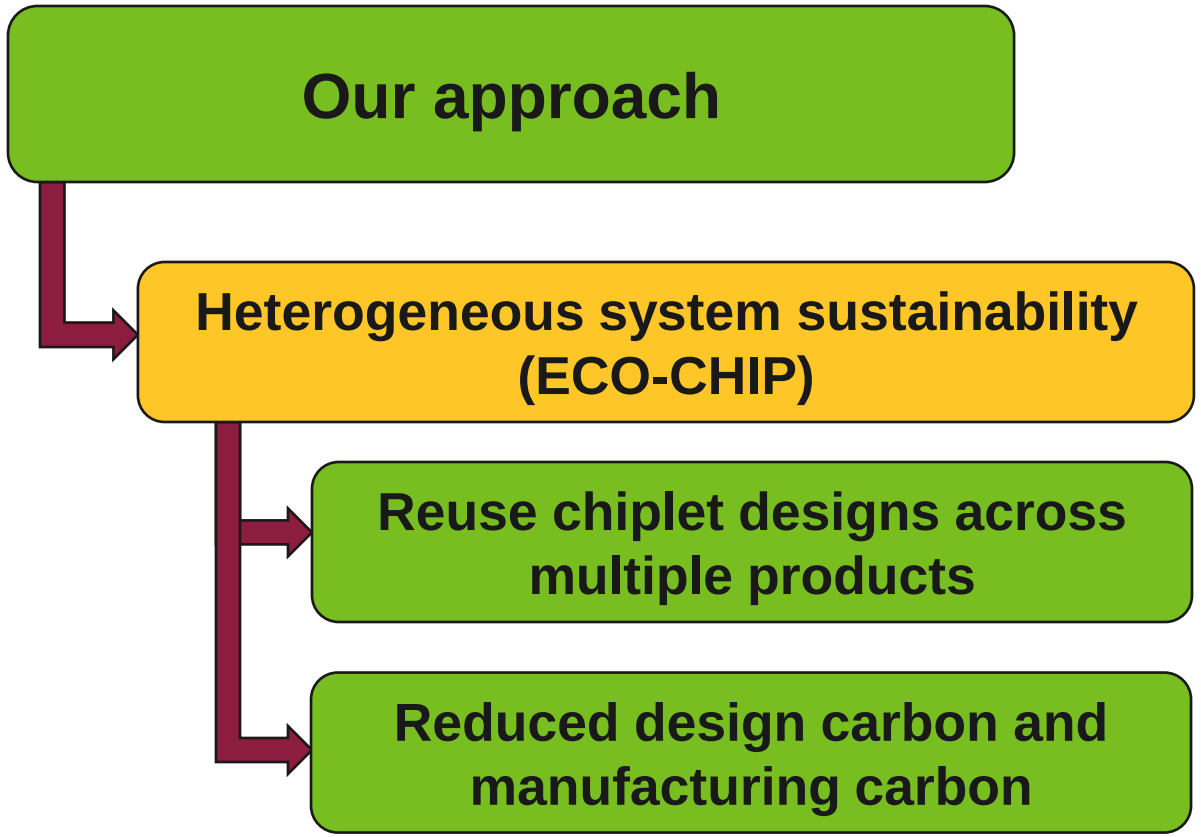
- Reduce
- Reuse
- Recycle

# This work: Our approach to sustainable computing

3R's for sustainability

- Reduce
- Reuse
- Recycle

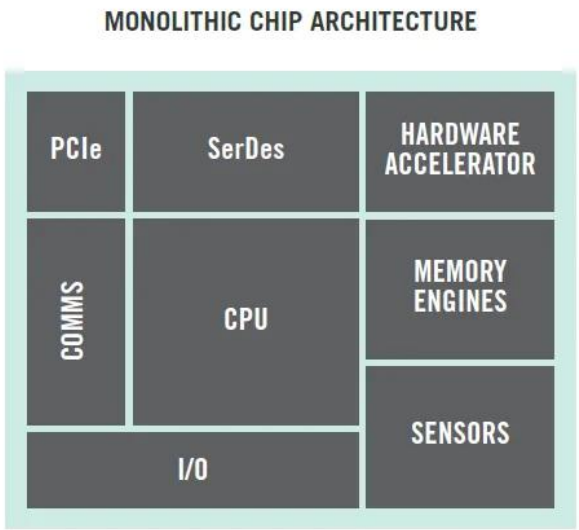



# Agenda

- Introduction
- Prior work
  - Architectural carbon footprint modeling (ACT)
- **ECO-CHIP**
  - **HI Pathway to sustainability**
  - Framework
  - ECO-CHIP CFP models
  - Key takeaways
- Conclusion

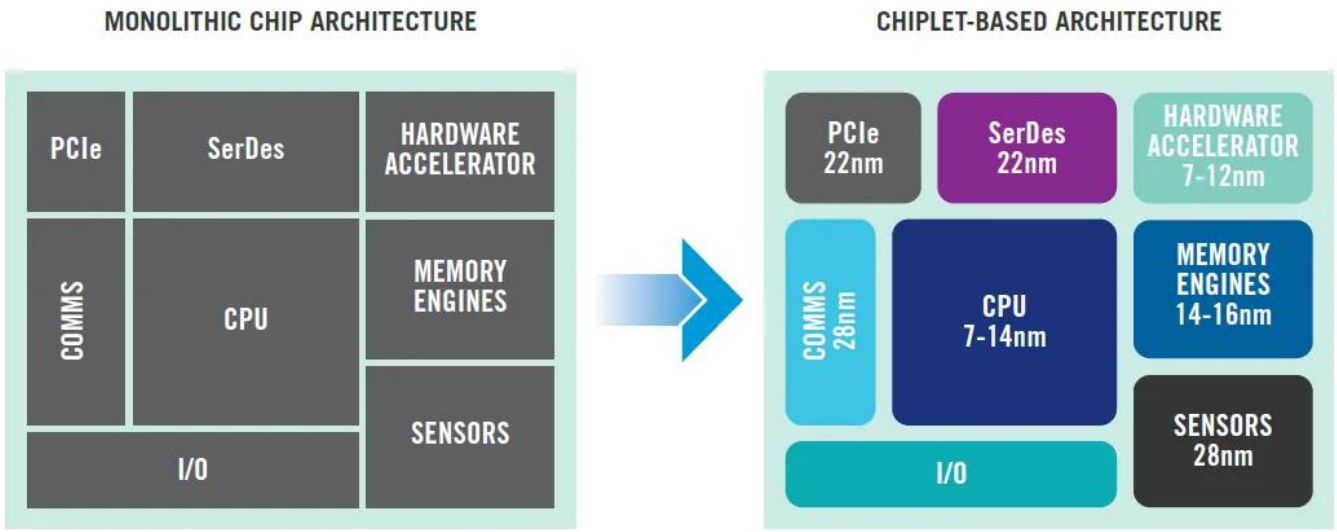
# Heterogeneous Integration (HI)

- Large SoCs are at reticle limit



# Heterogeneous Integration (HI)

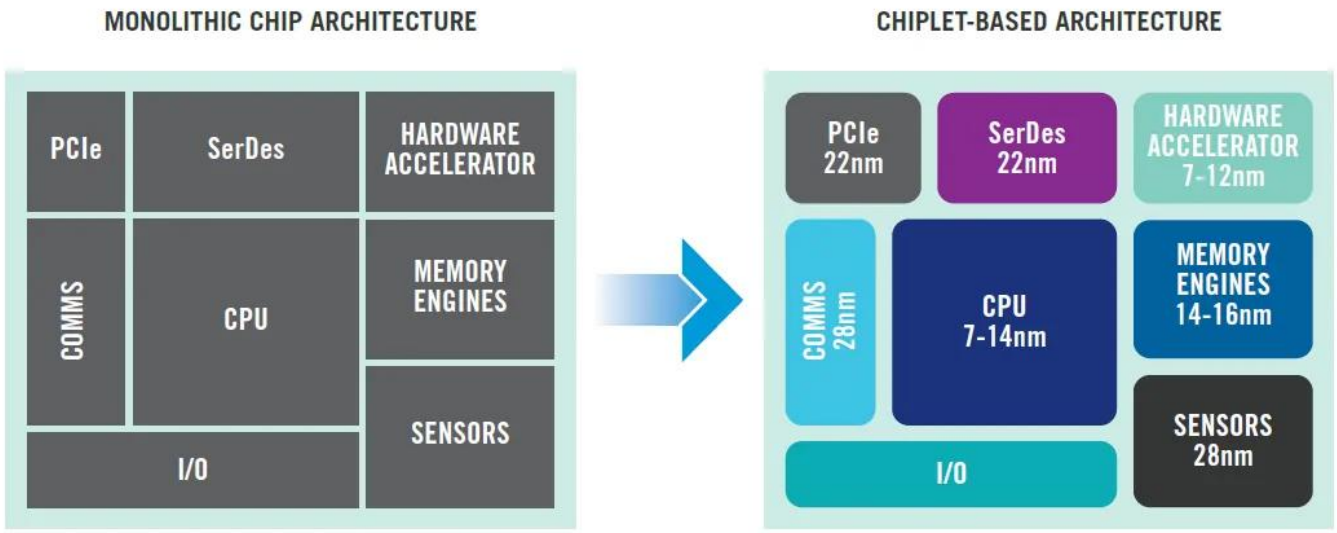
- Large SoCs are at reticle limit
- To reduce costs and sustain Moore's law HI enables two or more dies manufactured individually and integrated into a single package



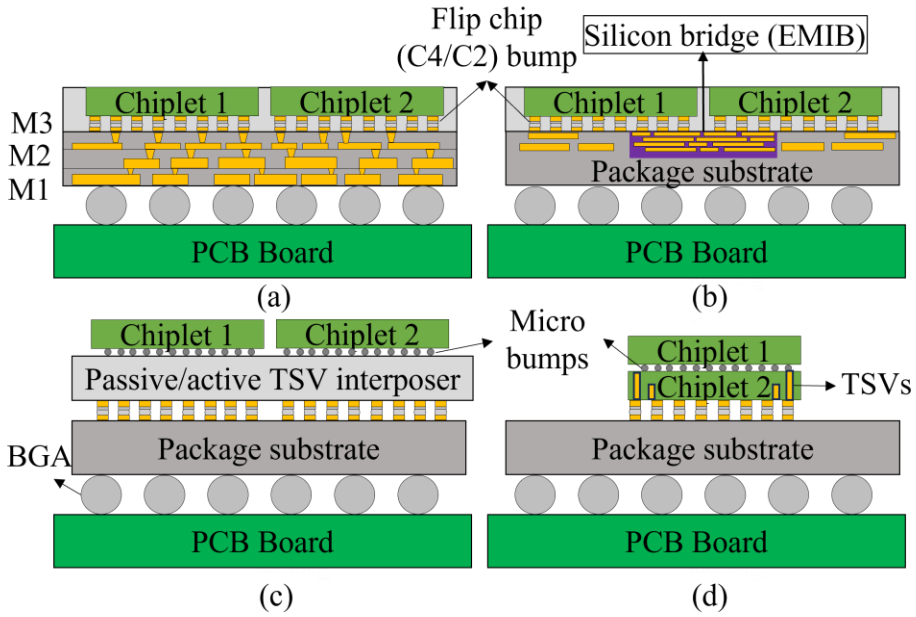

Source : Lawrence Lundy-Bryan FRSA, LinkedIn post

# Heterogeneous Integration (HI)

- Large SoCs are at reticle limit
- To reduce costs and sustain Moore's law HI enables two or more dies manufactured individually and integrated into a single package
- The key enabler for heterogeneous integration are advanced packaging techniques



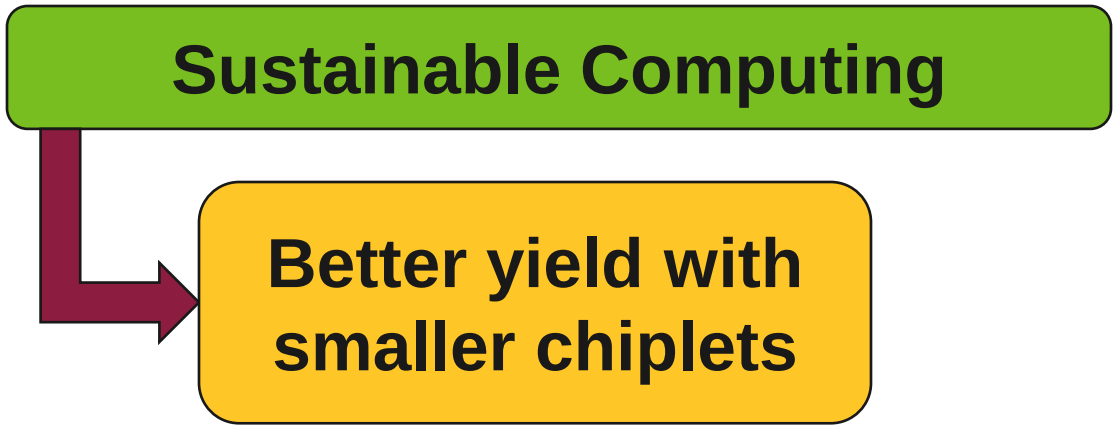

Source : Lawrence Lundy-Bryan FRSA, LinkedIn post



# HI as a path towards sustainable computing

**Sustainable Computing**

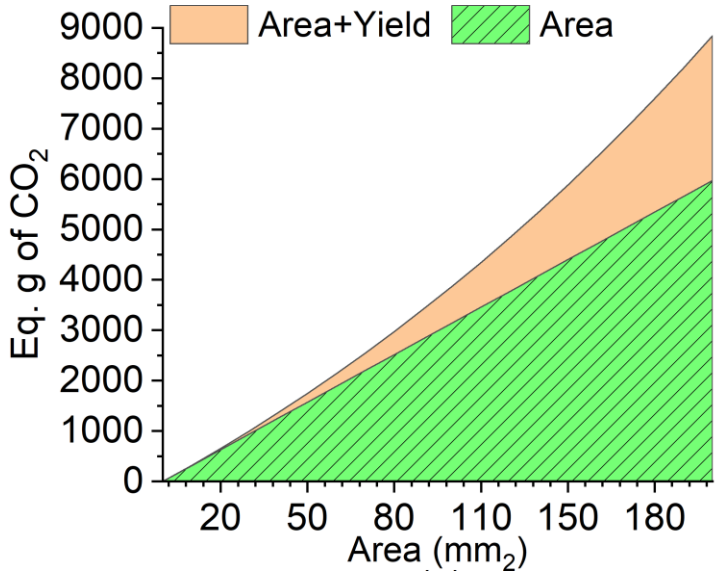
# HI as a path towards sustainable computing

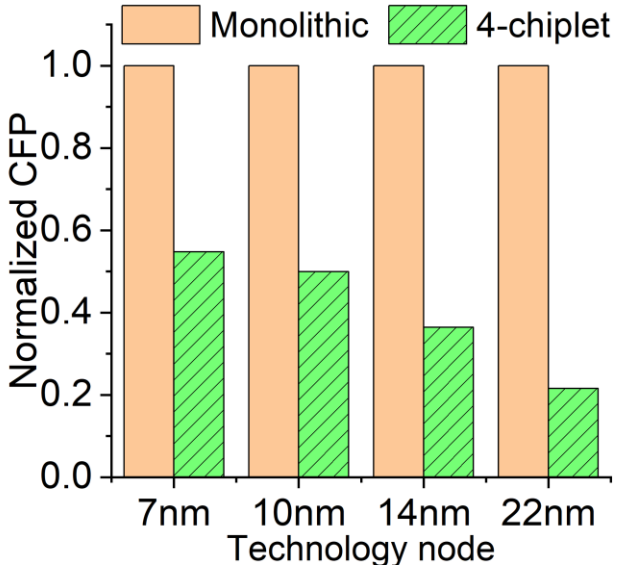


# HI as a path towards sustainable computing

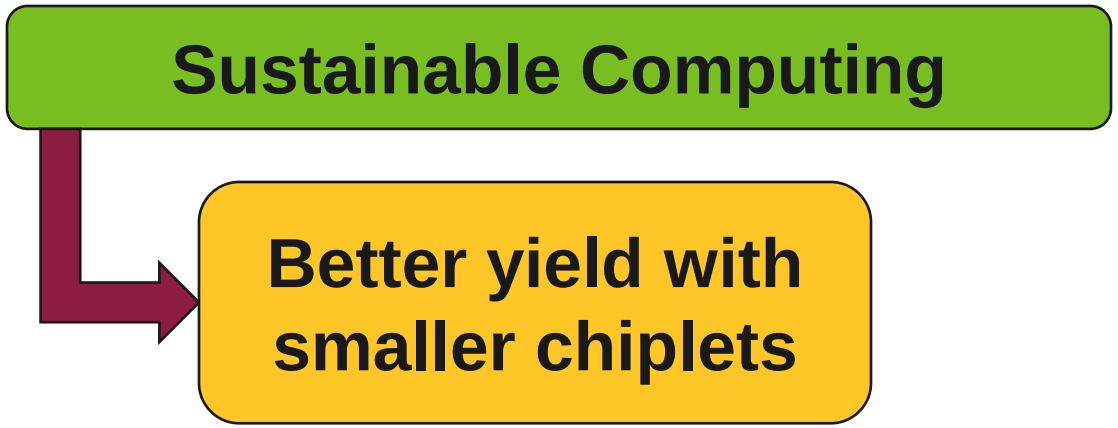
**Sustainable Computing**

**Better yield with smaller chiplets**

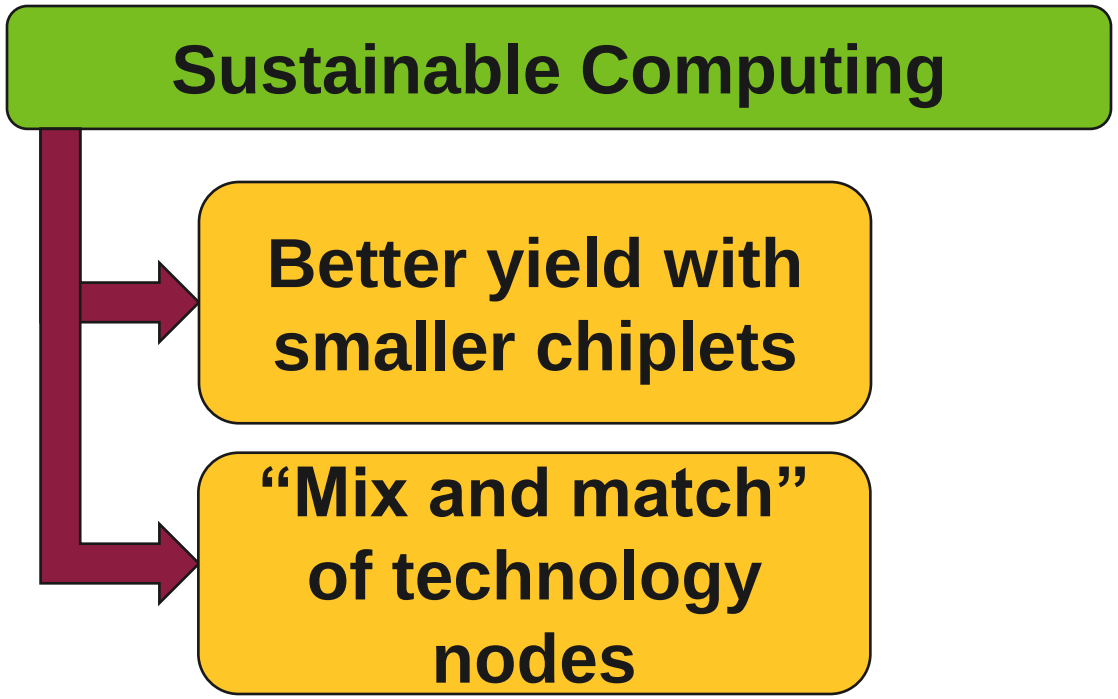


# HI as a path towards sustainable computing



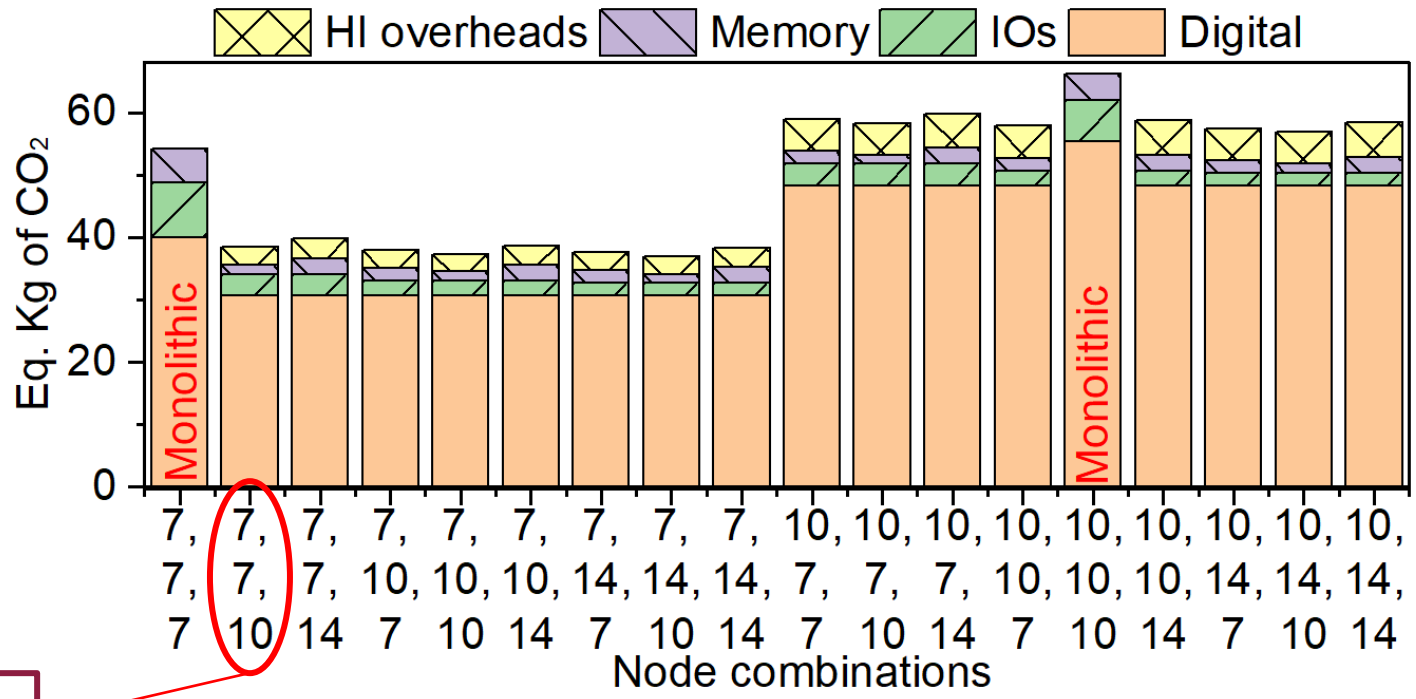
# HI as a path towards sustainable computing



# HI as a path towards sustainable computing

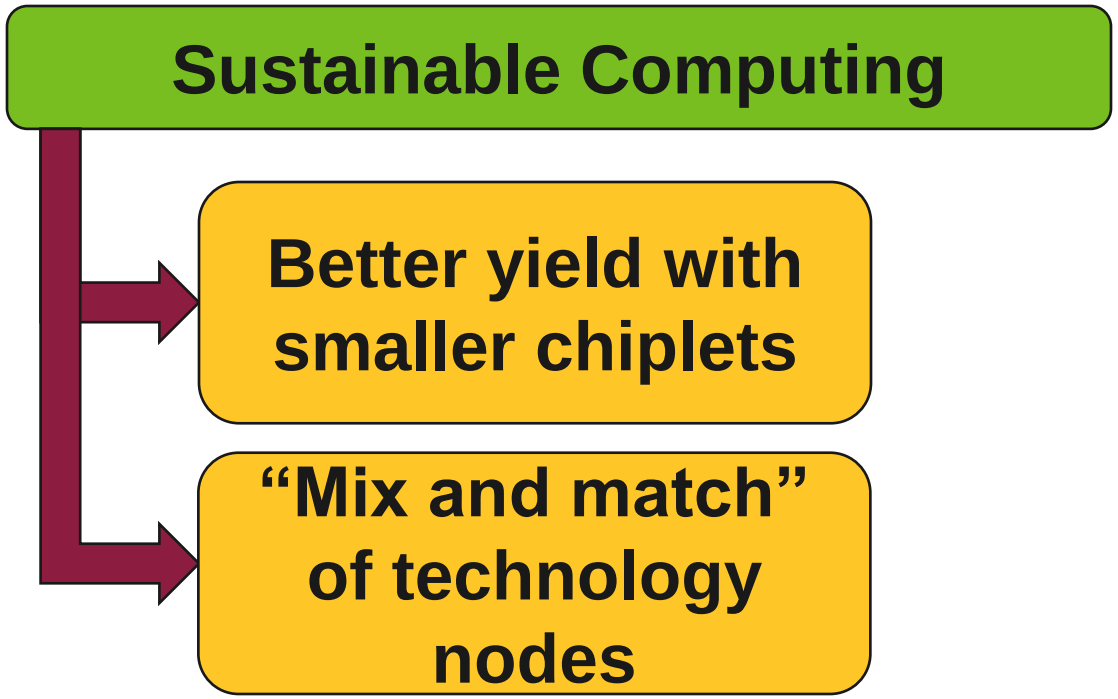
**Sustainable Computing**

- **Better yield with smaller chiplets**
- **"Mix and match" of technology nodes**

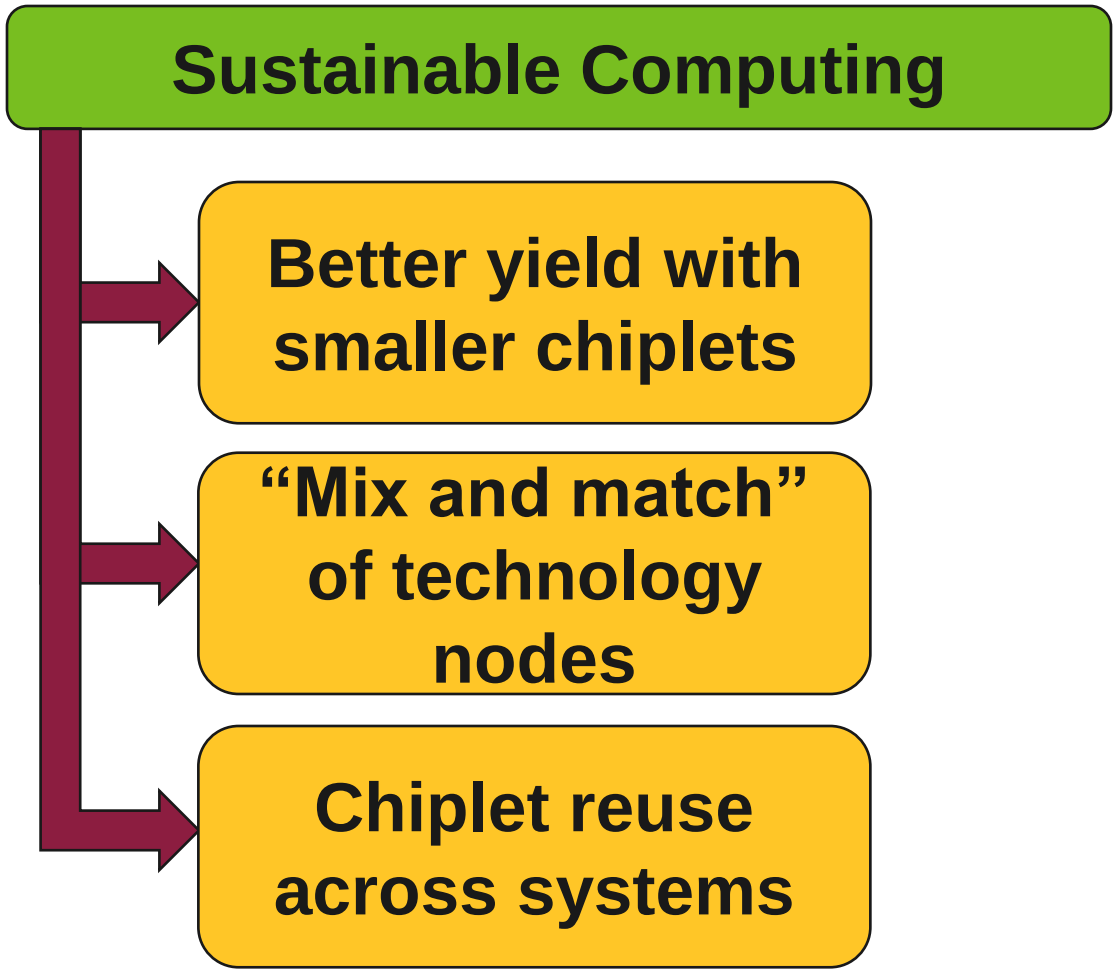



**7,7,10 => 7nm Logic**
**7nm IOs**
**10nm Memory**
**7,7,7 => Monolithic on 7nm**

# HI as a path towards sustainable computing



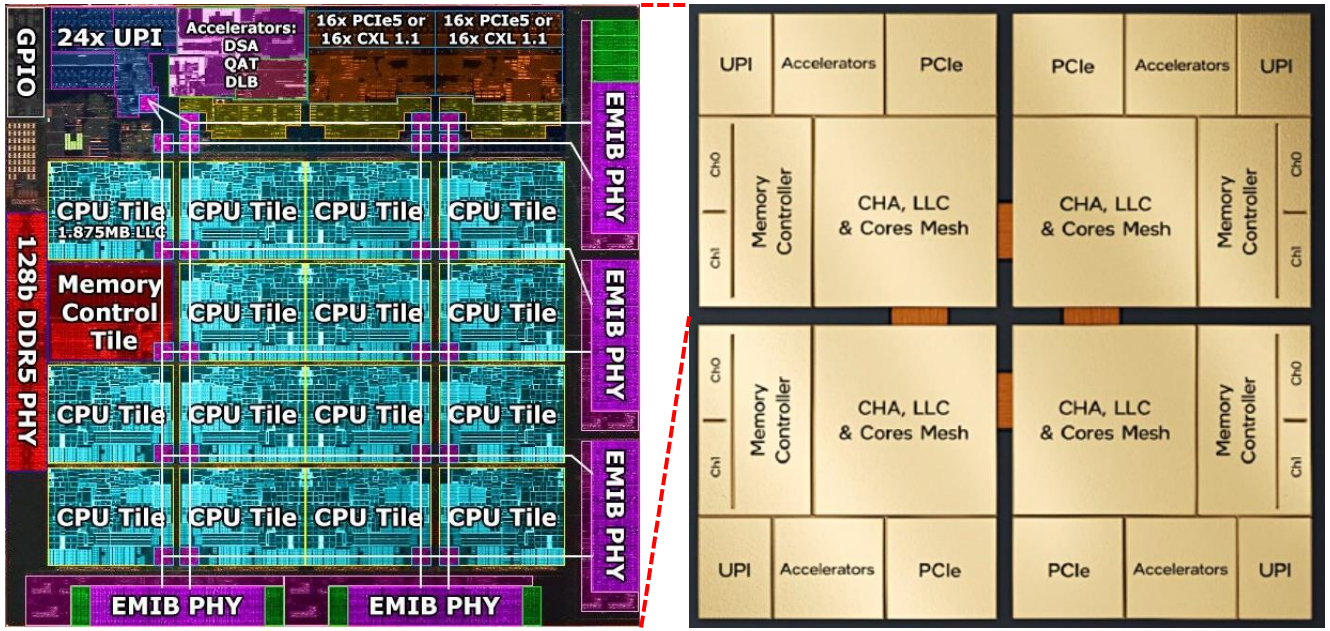
# HI as a path towards sustainable computing



# HI as a path towards sustainable computing

**Sustainable Computing**

- **Better yield with smaller chiplets**
- **“Mix and match” of technology nodes**
- **Chiplet reuse across systems**

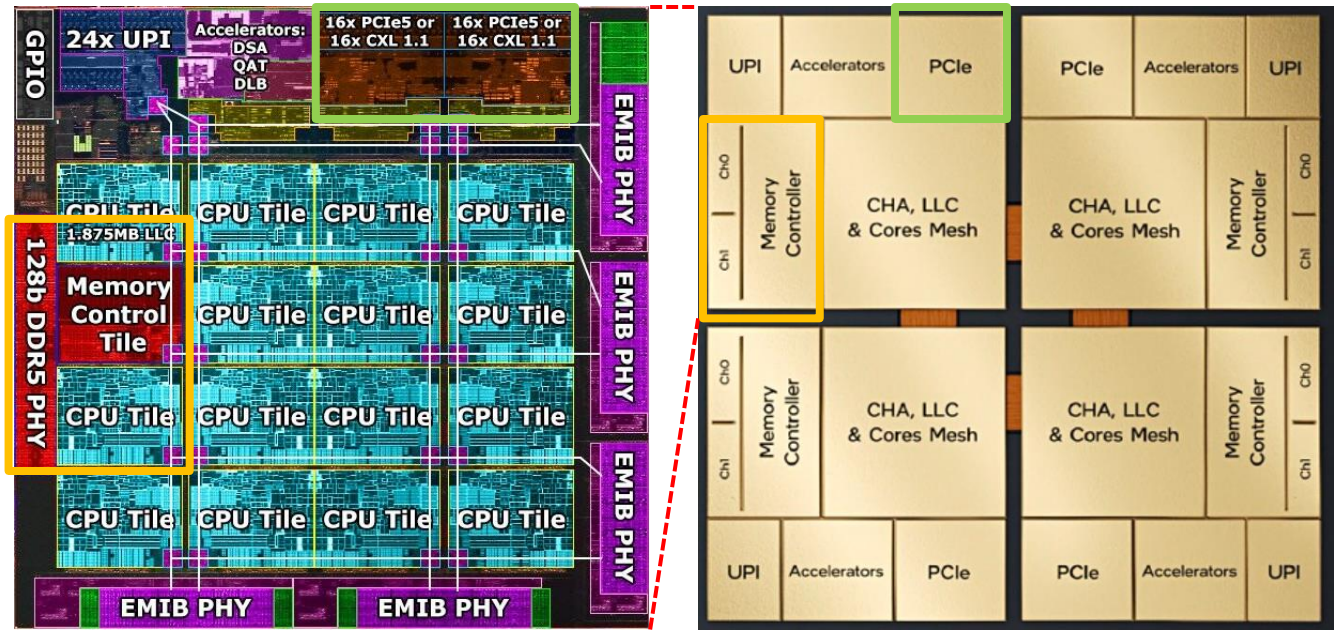



Source : Intel, Screenhacker

# HI as a path towards sustainable computing

**Sustainable Computing**

- **Better yield with smaller chiplets**
- **“Mix and match” of technology nodes**
- **Chiplet reuse across systems**



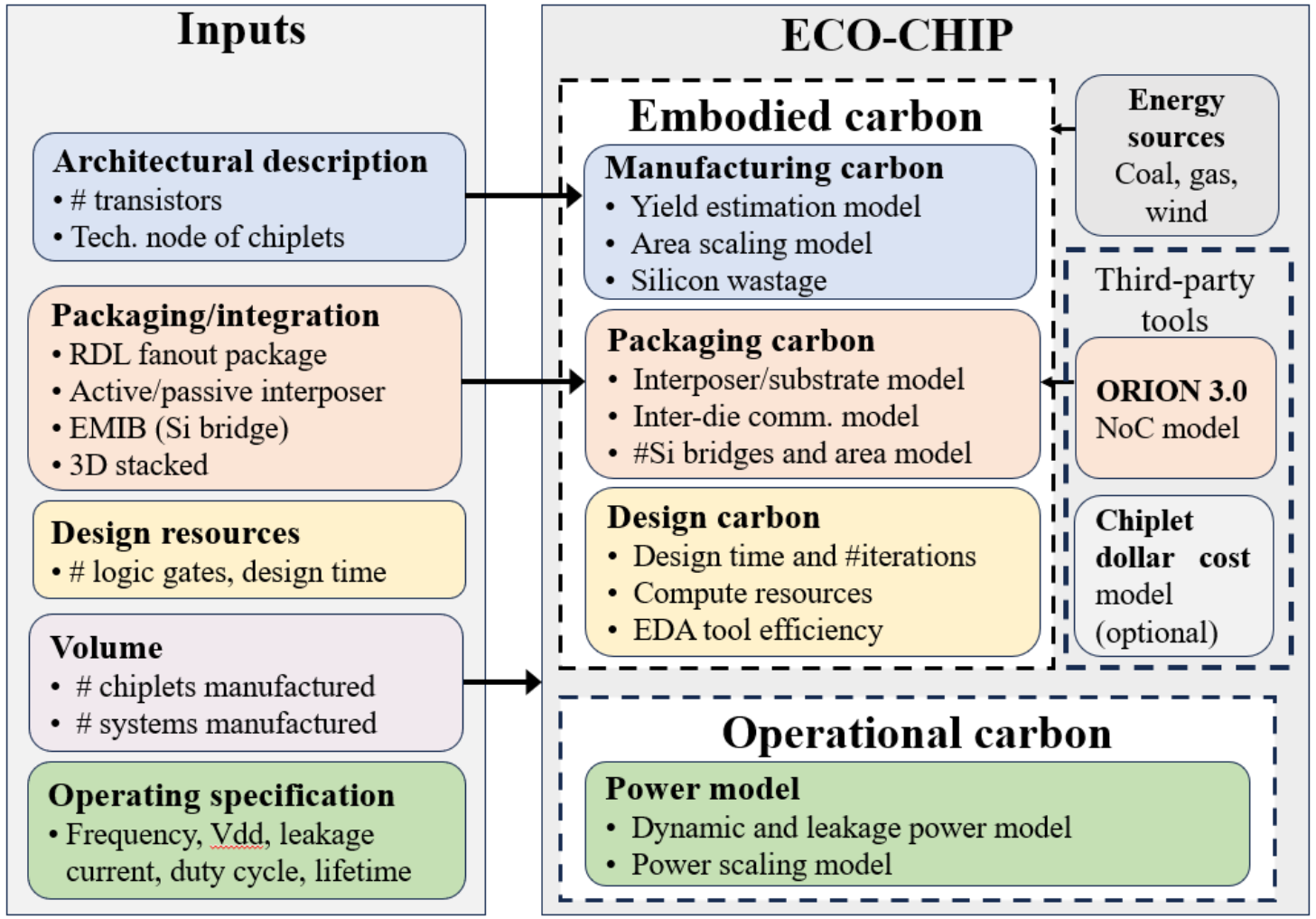

Source : Intel, Screenhacker

# Agenda

- Introduction
- Prior work
  - Architectural carbon footprint modeling (ACT)
- **ECO-CHIP**
  - HI Pathway to sustainability
  - **Framework**
  - ECO-CHIP CFP models
  - Key takeaways
- Conclusion

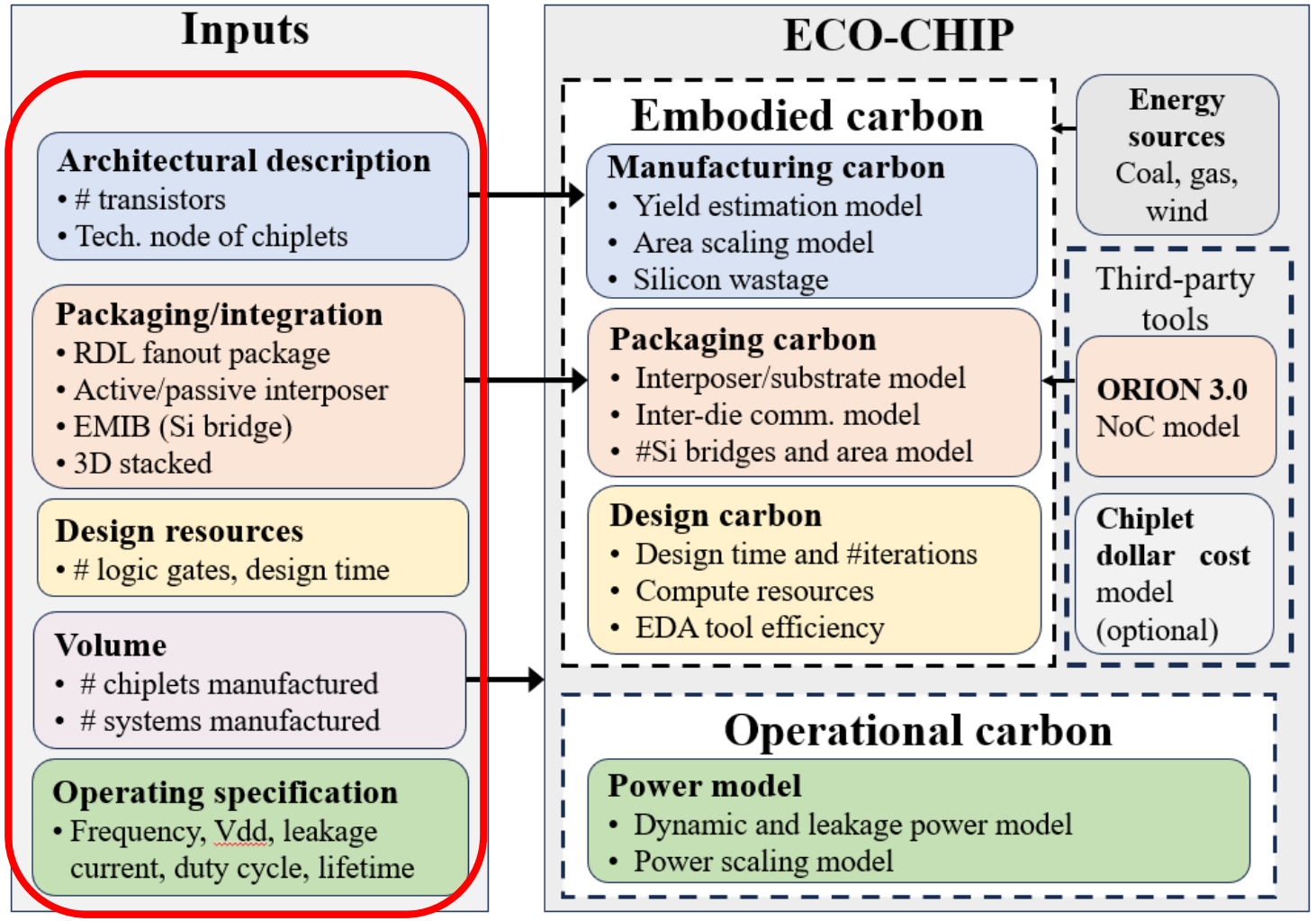
# ECO-CHIP framework

- Architecture parameter inputs
- Estimates embodied CFP
  - Manufacturing
  - Packaging
  - Design
- Operational CFP
- Integrate with third-party tools



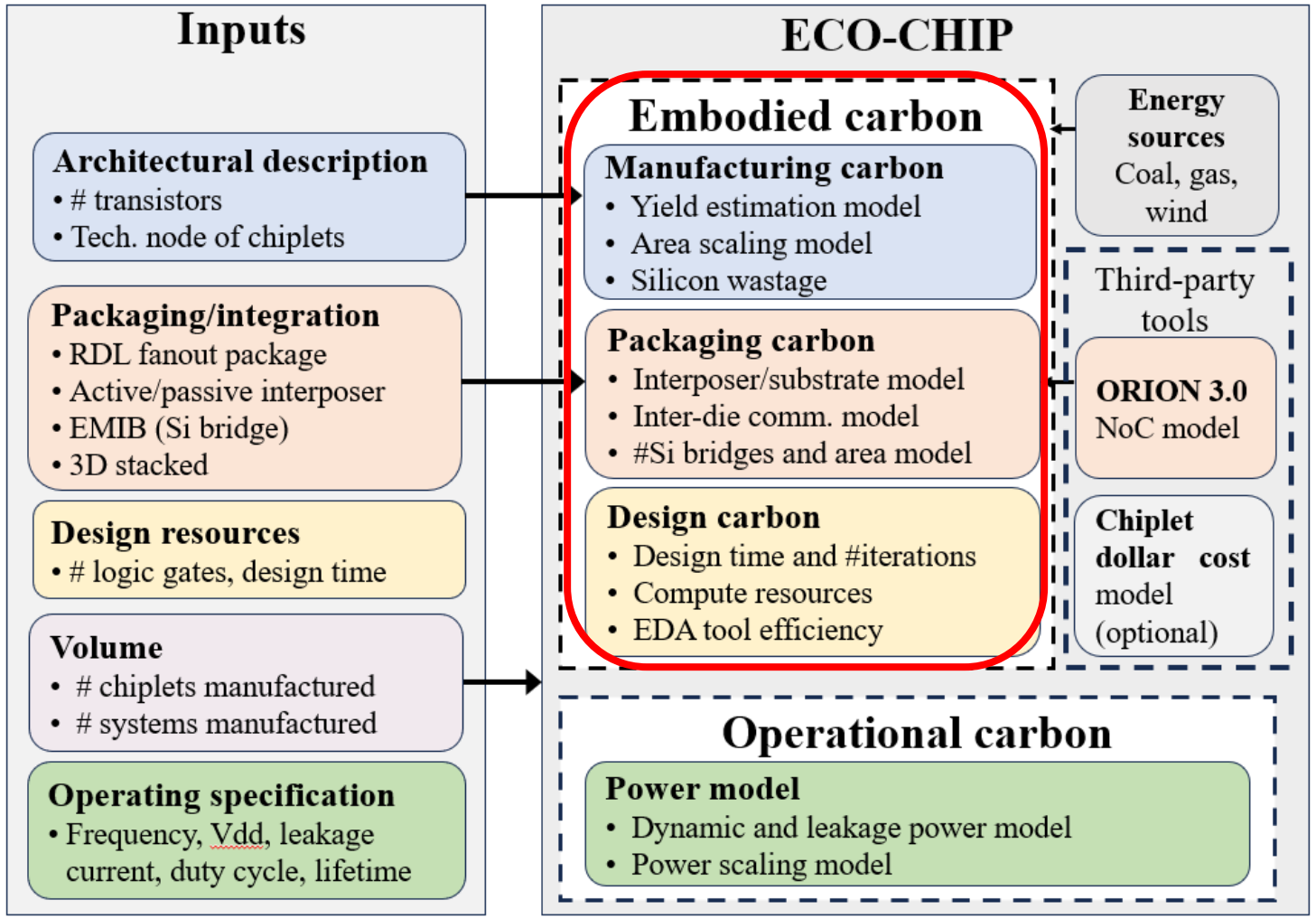
# ECO-CHIP framework

- Architecture parameter inputs
- Estimates embodied CFP
  - Manufacturing
  - Packaging
  - Design
- Operational CFP
- Integrate with third-party tools



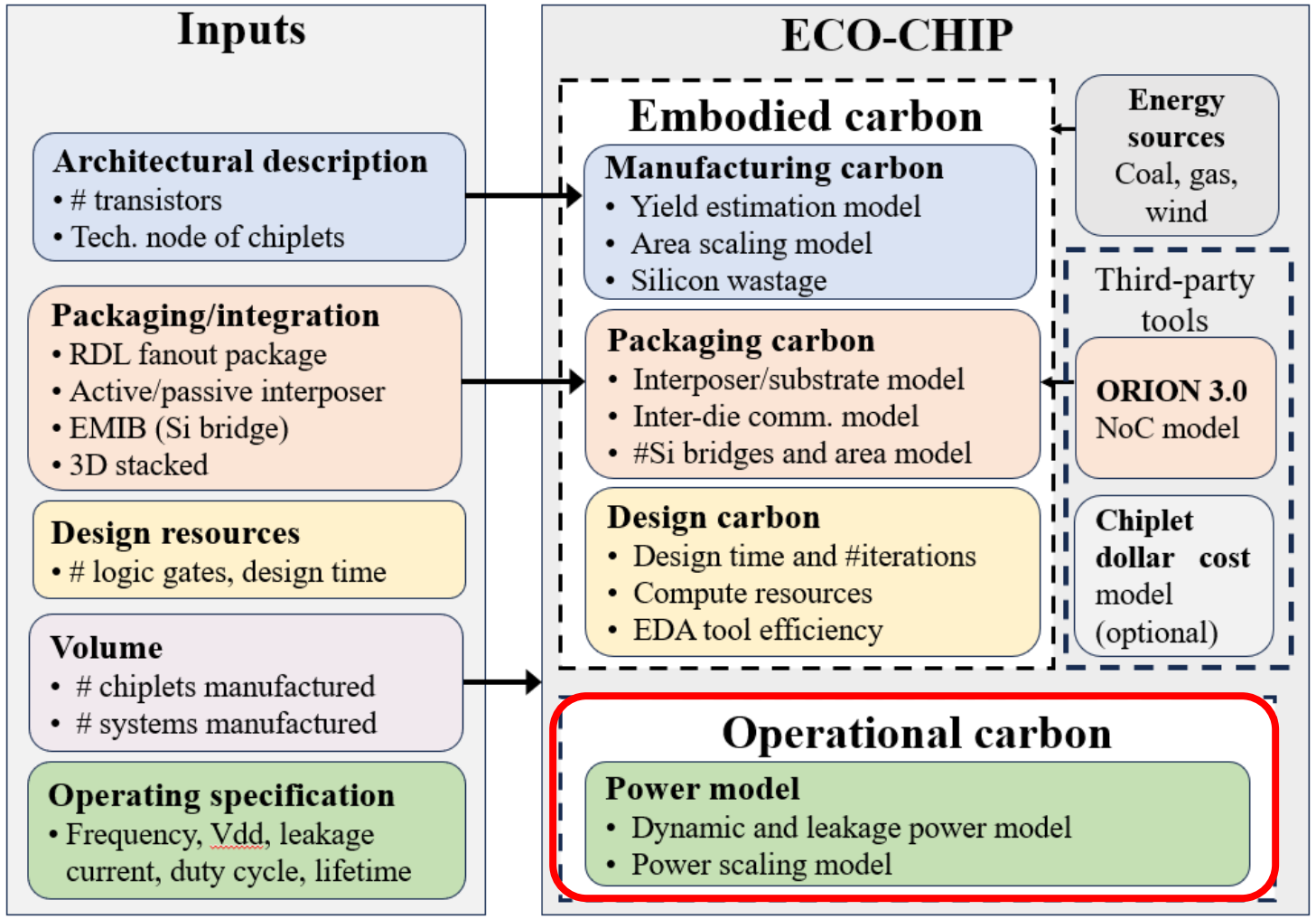
# ECO-CHIP framework

- Architecture parameter inputs
- Estimates embodied CFP
  - Manufacturing
  - Packaging
  - Design
- Operational CFP
- Integrate with third-party tools



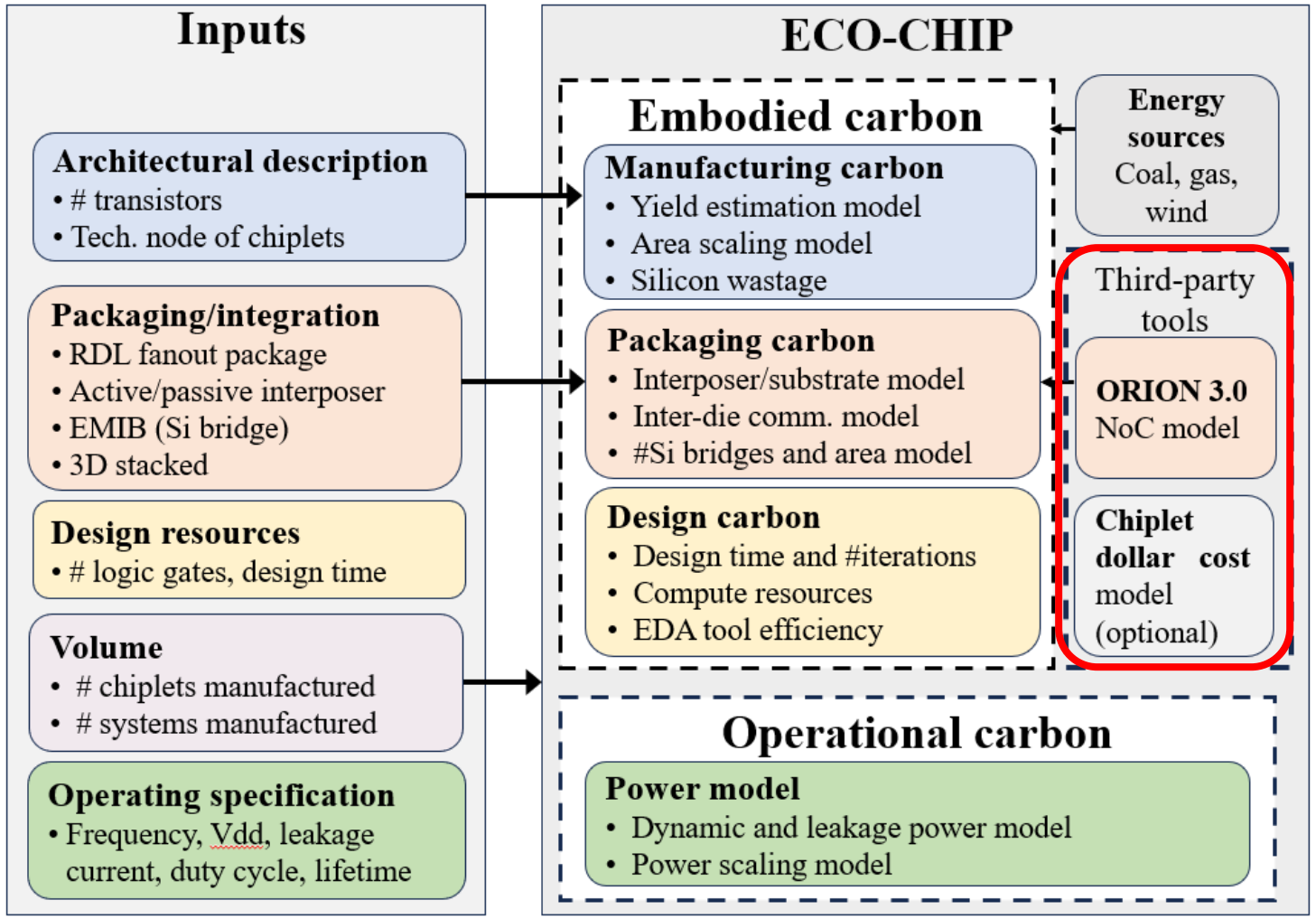
# ECO-CHIP framework

- Architecture parameter inputs
- Estimates embodied CFP
  - Manufacturing
  - Packaging
  - Design
- Operational CFP
- Integrate with third-party tools



# ECO-CHIP framework

- Architecture parameter inputs
- Estimates embodied CFP
  - Manufacturing
  - Packaging
  - Design
- Operational CFP
- Integrate with third-party tools



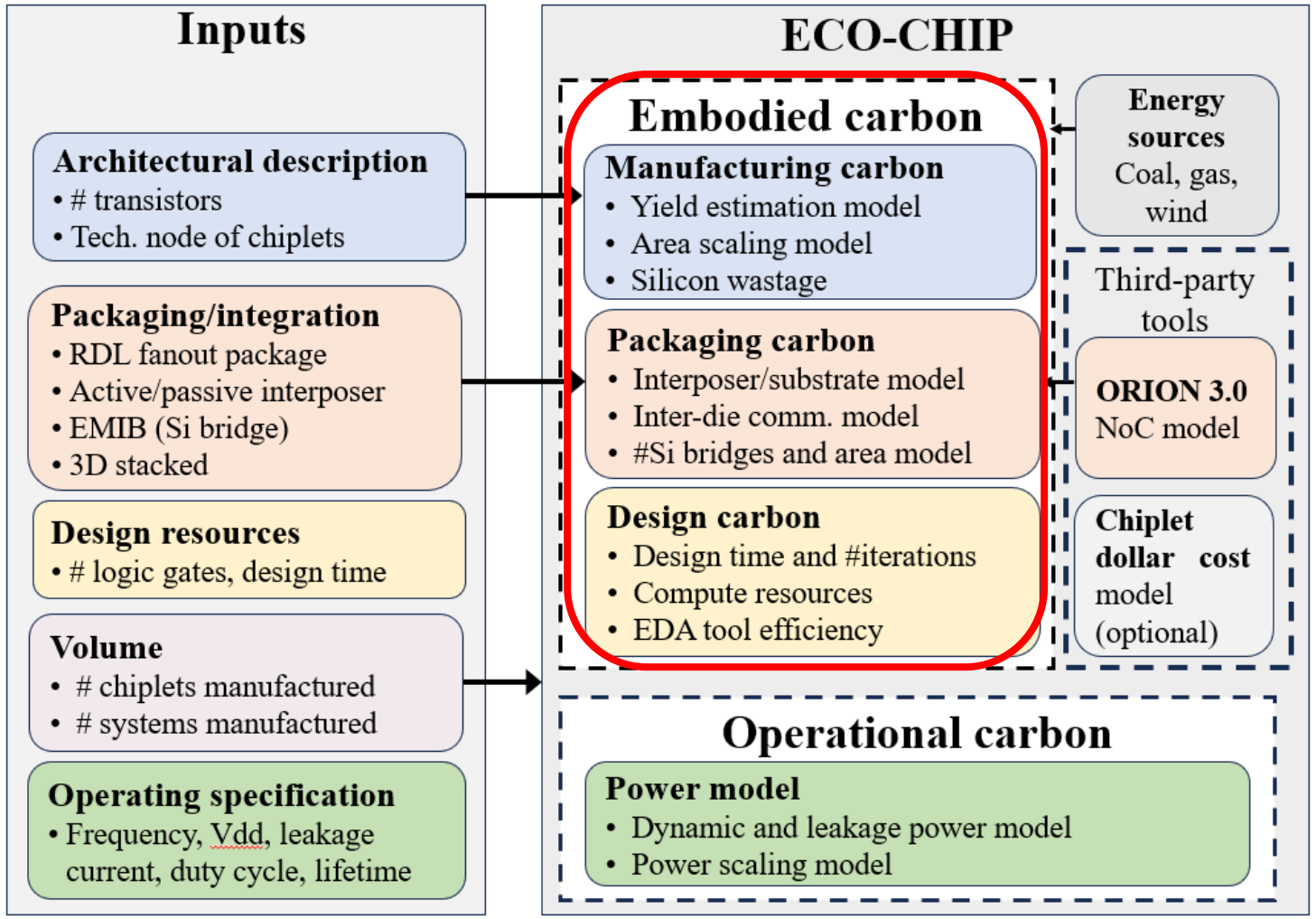
# ECO-CHIP framework

Total carbon is given by the sum of operational carbon across the lifetime of the chip and the embodied carbon

$$C_{tot} = C_{emb} + lifetime \times C_{op}$$

$$C_{emb} = C_{mfg} + C_{HI} + C_{des}$$

$C_{emb}$ - Embodied carbon
$C_{mfg}$ - Manufacturing carbon
$C_{des}$ - Design carbon
$C_{HI}$ - Carbon from HI (advanced packaging and area overheads)



# ECO-CHIP framework

Total carbon is given by the sum of operational carbon across the lifetime of the chip and the embodied carbon

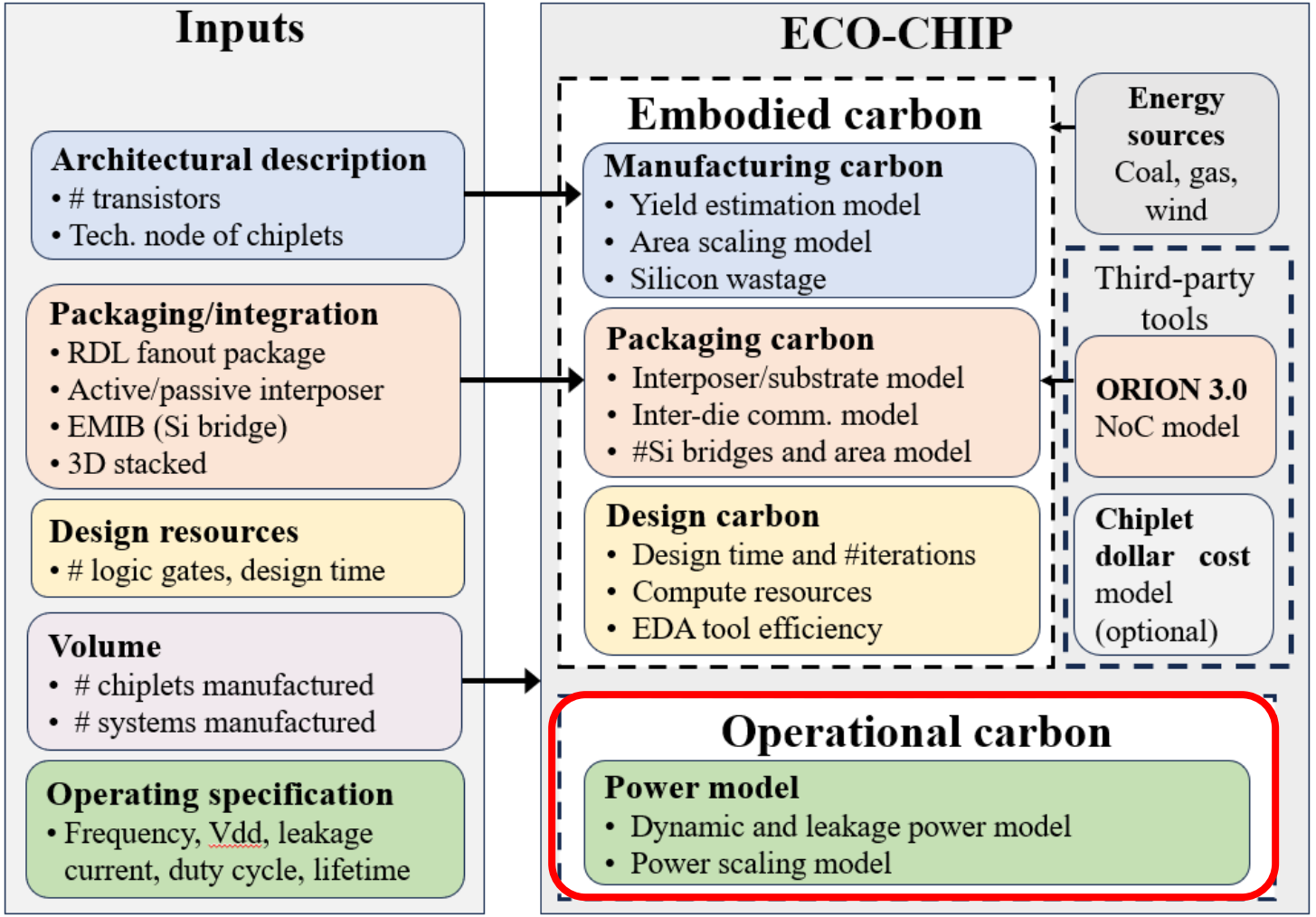
$$C_{tot} = C_{emb} + lifetime \times C_{op}$$

$$C_{op} = C_{src,use} \times E_{use}$$

$C_{op}$ - Operational carbon

$C_{src,use}$-Carbon intensity of energy source

$E_{use}$ - Energy spend during usage



# Agenda

- Introduction
- Prior work
  - Architectural carbon footprint modeling (ACT)
- **ECO-CHIP**
  - HI Pathway to sustainability
  - Framework
  - **ECO-CHIP CFP models**
  - Key takeaways
- Conclusion

# Embodied carbon: Manufacturing

The manufacturing carbon for a die depends on its area, and amortized wasted area on the wafer

# Embodied carbon: Manufacturing

The manufacturing carbon for a die depends on its area, and amortized wasted area on the wafer

$$C_{mfg} = CFPA \times (Die\ area + Wasted\ area)$$

$$CFPA = \frac{(\eta_{fab} \times C_{mfg} \times E_{mfg} + C_{gas} + C_{material})}{Yield}$$

$\eta_{fab}$ - Energy efficiency of lithography tools

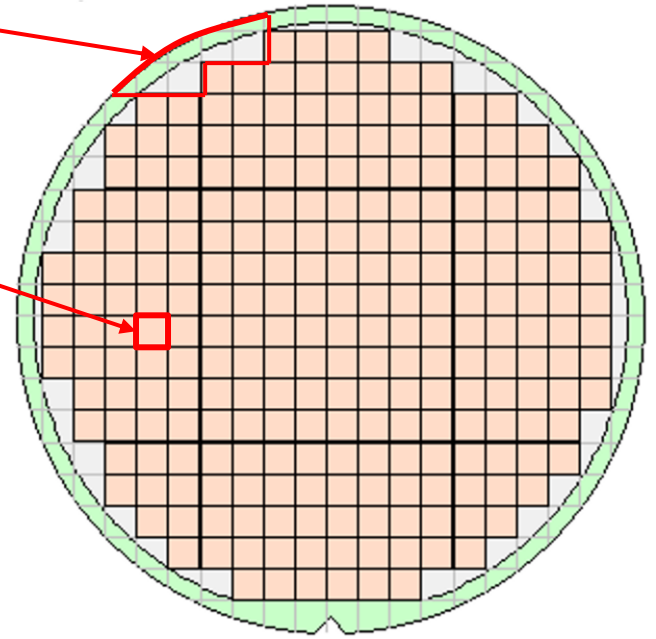
$EPA$ - Energy consumed during manufacturing

$C_{gas}$ - CFP from green house gas emission

$C_{material}$ - CFP from sourcing the materials for fabrication

$Yield$ - Yield of design for particular process node

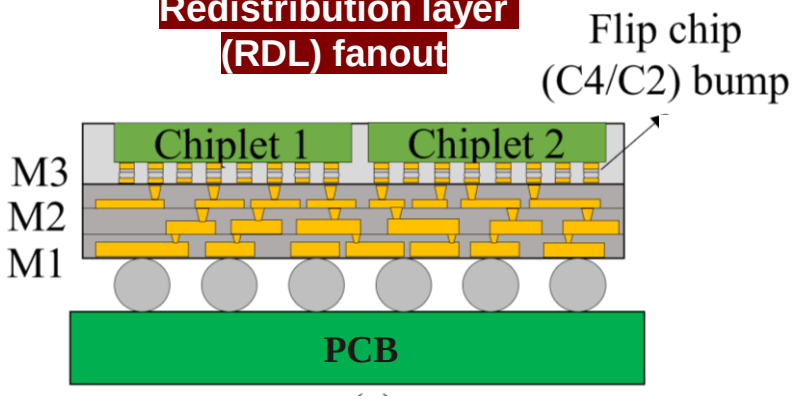
ACT (prior work)



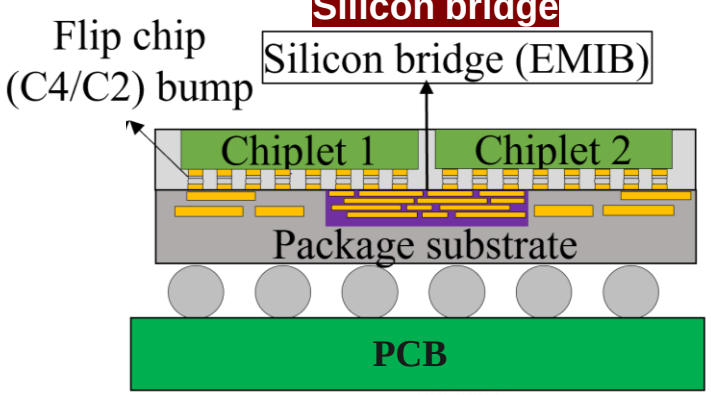
Enhanced the manufacturing carbon model from ACT to include area-dependent yield and efficiency of fabrication tools

# Embodied carbon: HI overheads

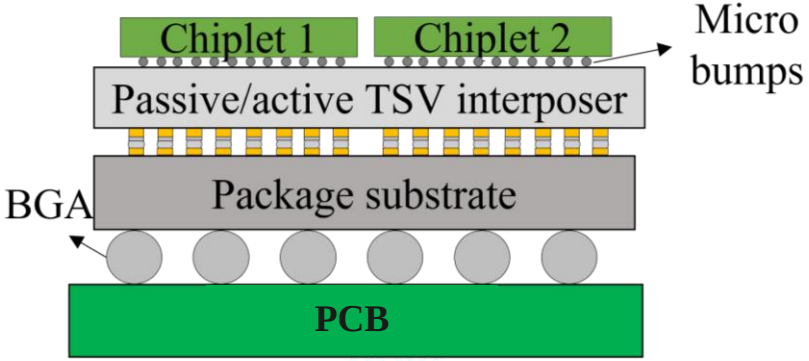
**Redistribution layer (RDL) fanout**



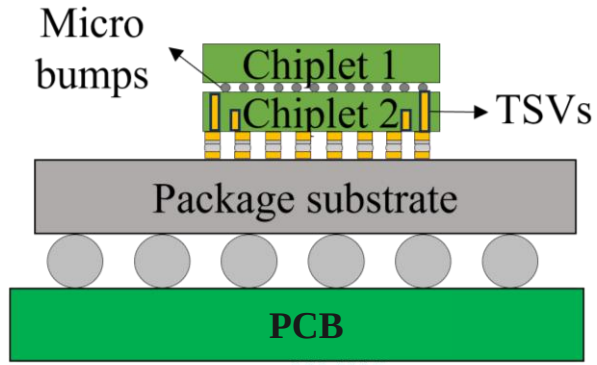

**Silicon bridge**




**Passive/active interposer package**

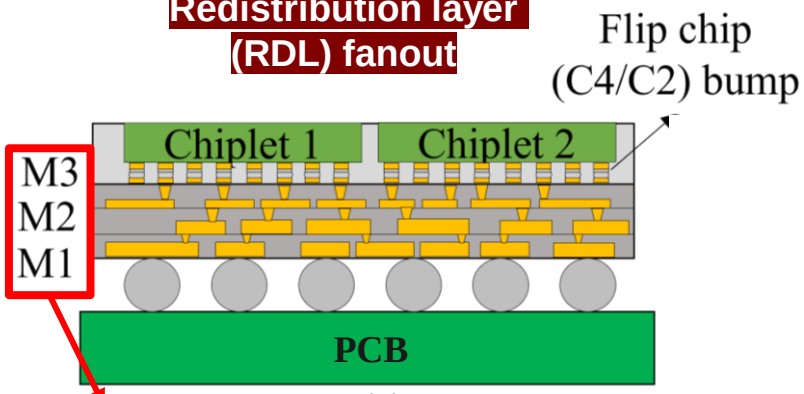



**3D chiplet stacking**



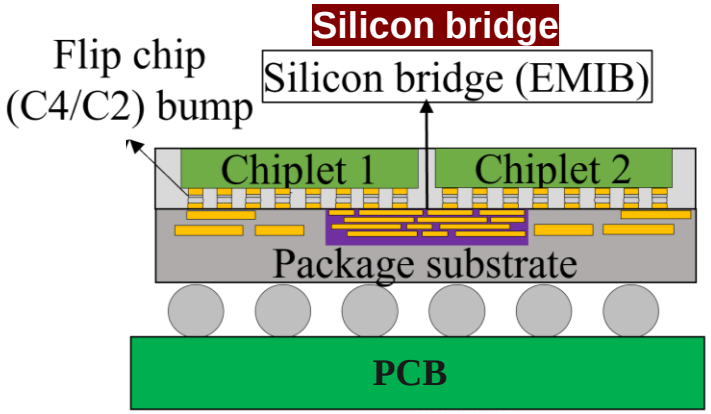
# Embodied carbon: HI overheads

**Redistribution layer (RDL) fanout**

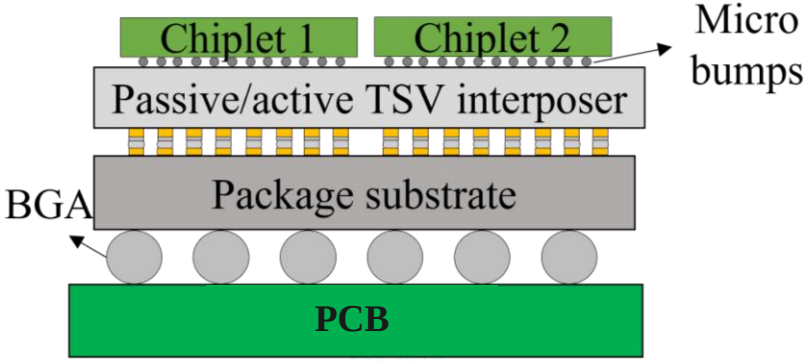



$$C_{RDL} = \frac{L_{RDL} \times EPLA_{RDL} \times C_{pkg} \times A_{package}}{Yield(RDL)}$$

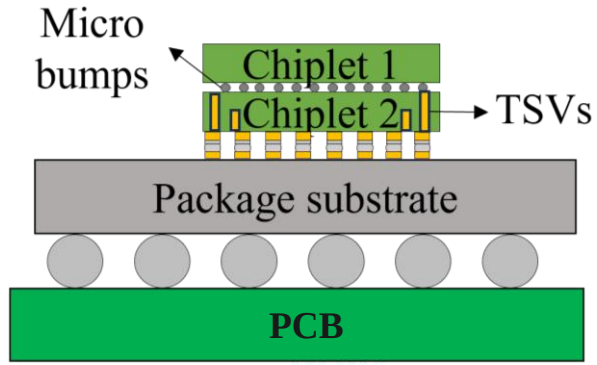
**Silicon bridge**




**Passive/active interposer package**



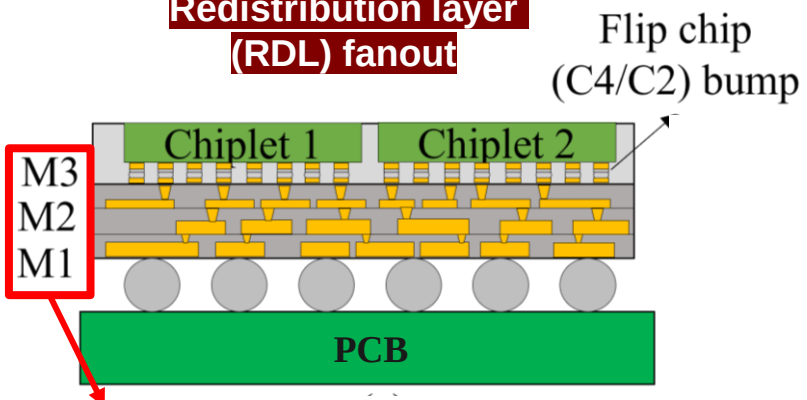

**3D chiplet stacking**




EPLA → Energy per unit area per layer

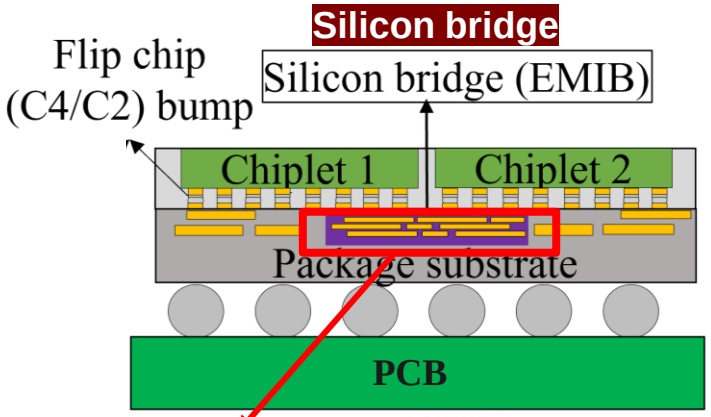
# Embodied carbon: HI overheads

**Redistribution layer (RDL) fanout**



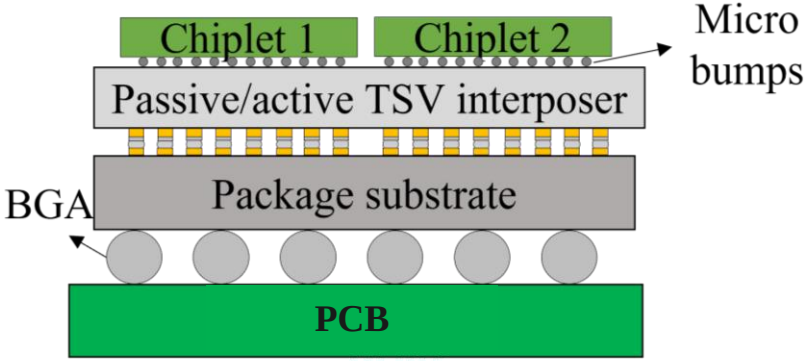

$$C_{RDL} = \frac{L_{RDL} \times EPLA_{RDL} \times C_{pkg} \times A_{package}}{Yield(RDL)}$$

**Silicon bridge**

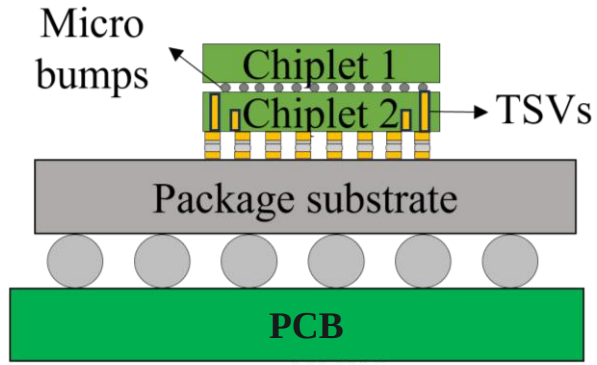



$$C_{bridge} = \frac{N_{bridge} \times L_{bridge} \times EPLA_{bridge} \times C_{pkg} \times A_{bridge}}{Yield(bridge)}$$

**Passive/active interposer package**



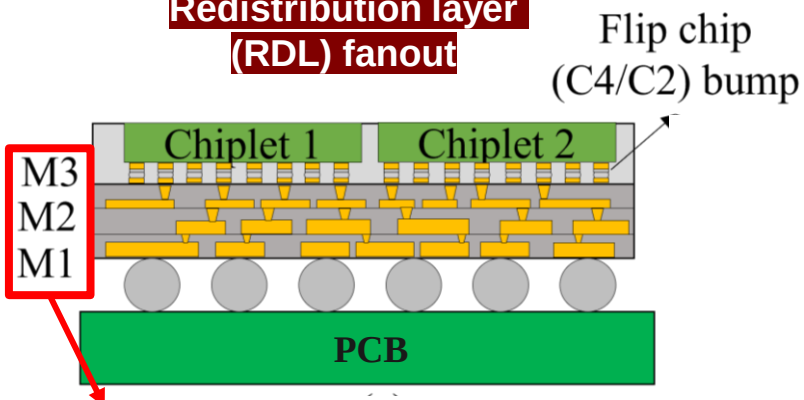

**3D chiplet stacking**




EPLA → Energy per unit area per layer

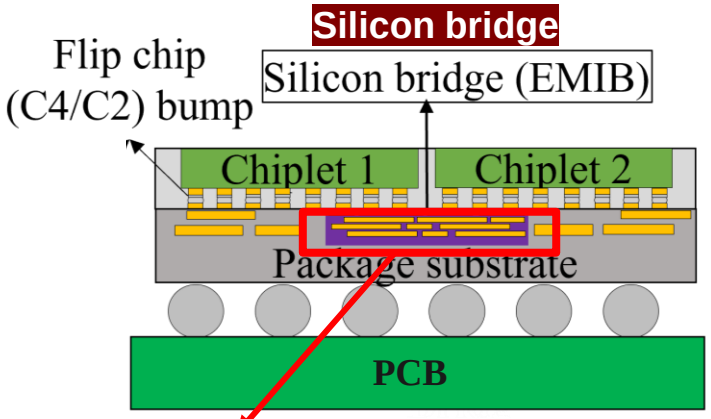
# Embodied carbon: HI overheads

**Redistribution layer (RDL) fanout**



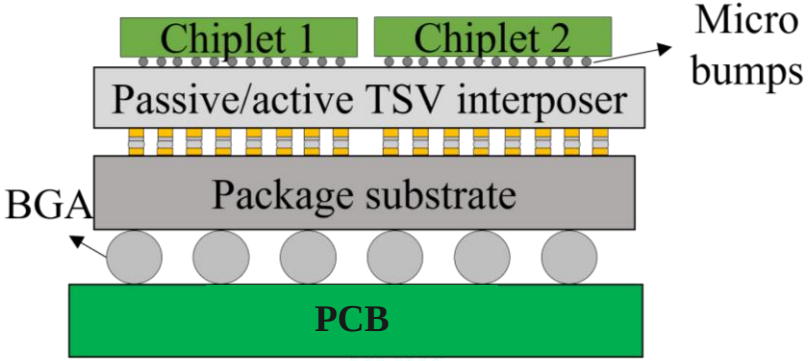

$$C_{RDL} = \frac{L_{RDL} \times EPLA_{RDL} \times C_{pkg} \times A_{package}}{Yield(RDL)}$$

**Silicon bridge**



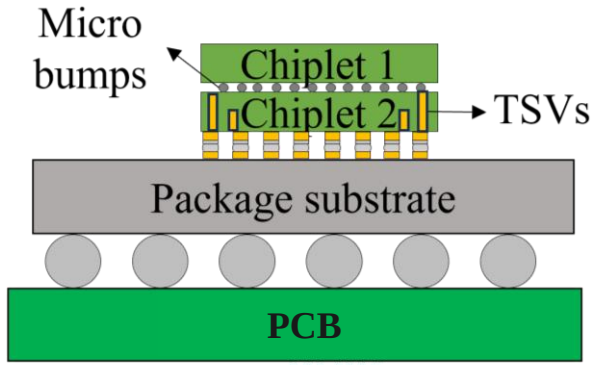

$$C_{bridge} = \frac{N_{bridge} \times L_{bridge} \times EPLA_{bridge} \times C_{pkg} \times A_{bridge}}{Yield(bridge)}$$

**Passive/active interposer package**




Modeled as an additional die

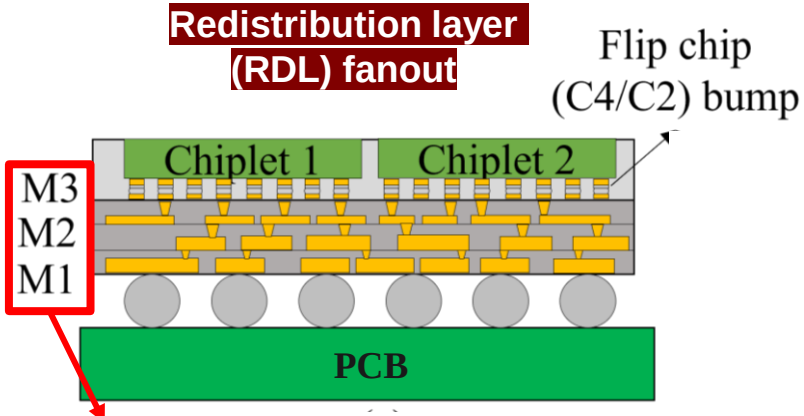
**3D chiplet stacking**




EPLA → Energy per unit area per layer

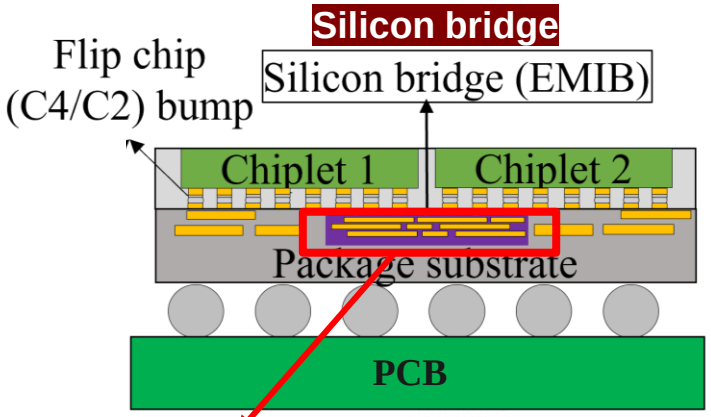
# Embodied carbon: HI overheads

**Redistribution layer (RDL) fanout**



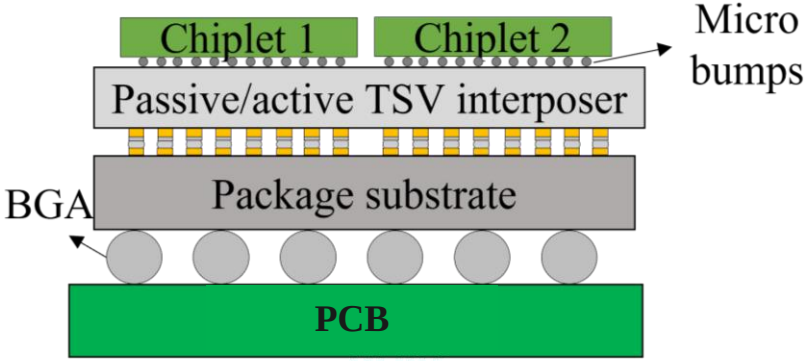

$$C_{RDL} = \frac{L_{RDL} \times EPLA_{RDL} \times C_{pkg} \times A_{package}}{Yield(RDL)}$$

**Silicon bridge**



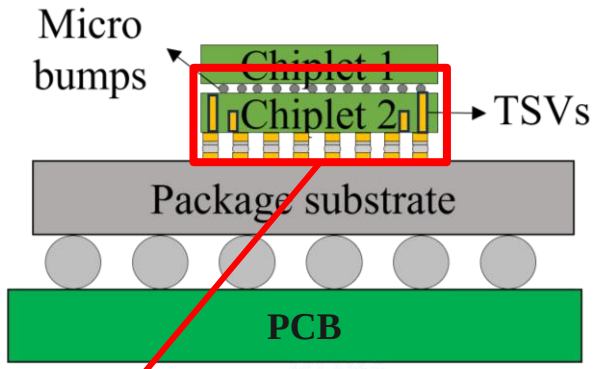

$$C_{bridge} = \frac{N_{bridge} \times L_{bridge} \times EPLA_{bridge} \times C_{pkg} \times A_{bridge}}{Yield(bridge)}$$

**Passive/active interposer package**




Modeled as an additional die

**3D chiplet stacking**




$$C_{3D} = \frac{N_{TSV,bump,bond} \times EPLA_{TSV,bump,bond} \times C_{pkg}}{Yield(3D)}$$

EPLA → Energy per unit area per layer

# Embodied carbon: Design carbon

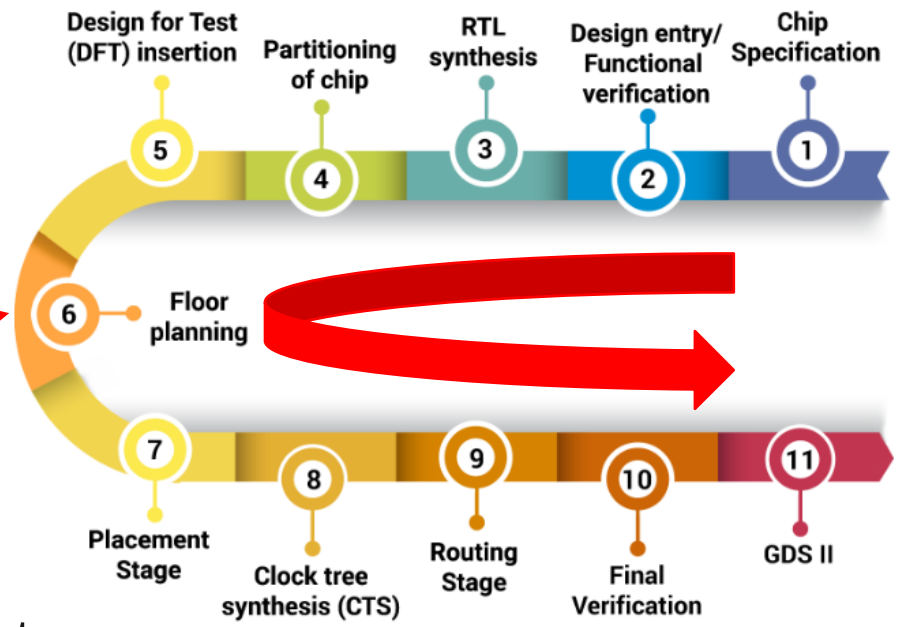
Design carbon of the system is the sum of:

- Design carbon of all chiplets amortized across the number of chiplets manufactured (design reuse)
- Design carbon of the overhead of integrating amortized across the number of systems packaged

The design carbon of a single chiplet is:

$$C_{des} = t_{des} \times P_{des} \times C_{src}$$

$$t_{des} = \frac{t_{verif} + (t_{SP\&R} + t_{analyze}) \times N_{des}}{\eta_{EDA}}$$




Source: eInfochips

$t_{verif,i}$ - Compute time for verification
$t_{SP\&R,i}$ - Computing time for single synthesis, place, and route
$t_{analyze,i}$ - Compute time for all simulation analysis
$N_{des}$ - Number of design iterations
$\eta_{EDA}$ - EDA tool productivity

# Agenda

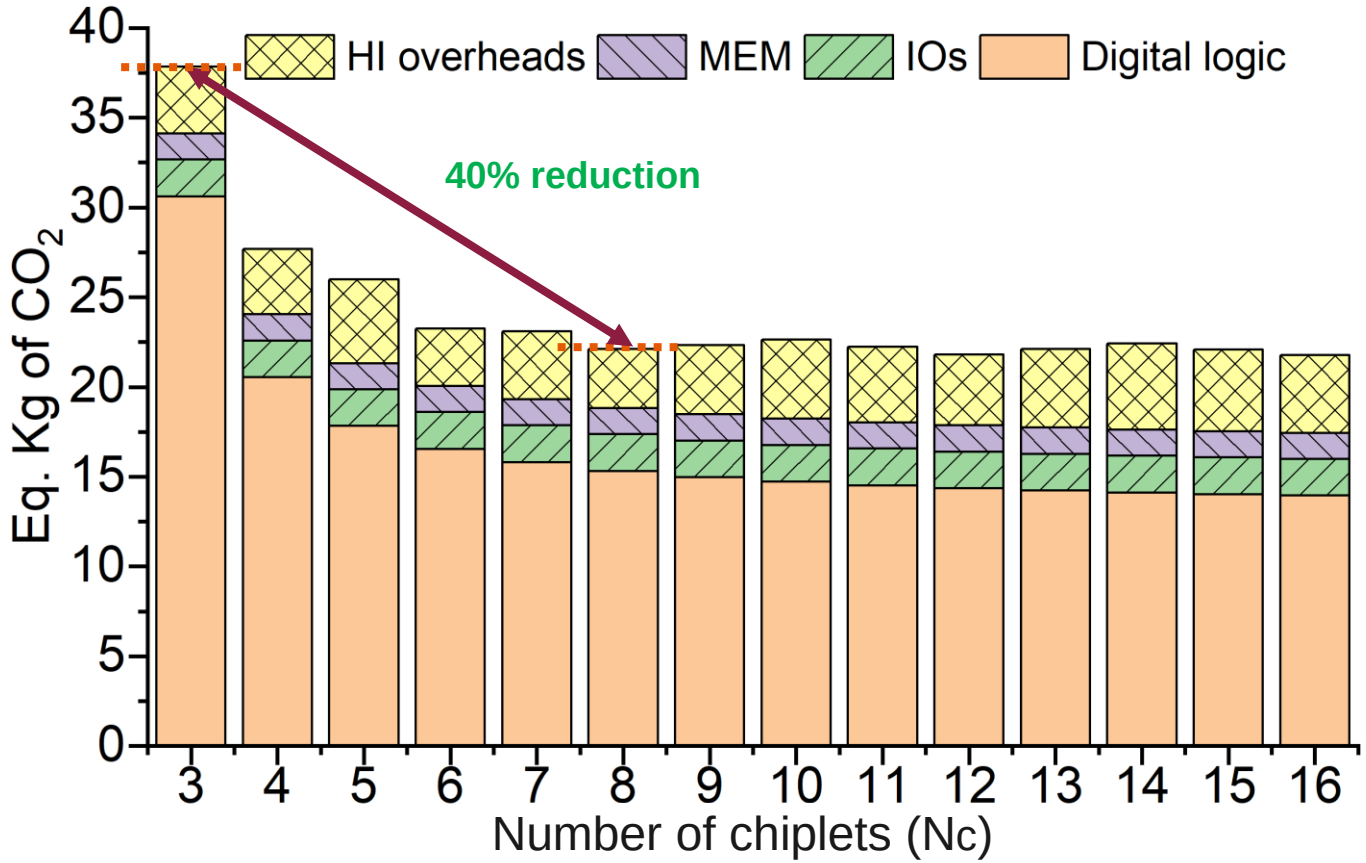
- Introduction
- Prior work
  - Architectural carbon footprint modeling (ACT)
- **ECO-CHIP**
  - HI Pathway to sustainability
  - Framework
  - ECO-CHIP CFP models
  - **Key takeaways**
- Conclusion

# ECO-CHIP results: Key takeaways

- Disaggregation to chiplets helps in lowering the overall CFP by 40%

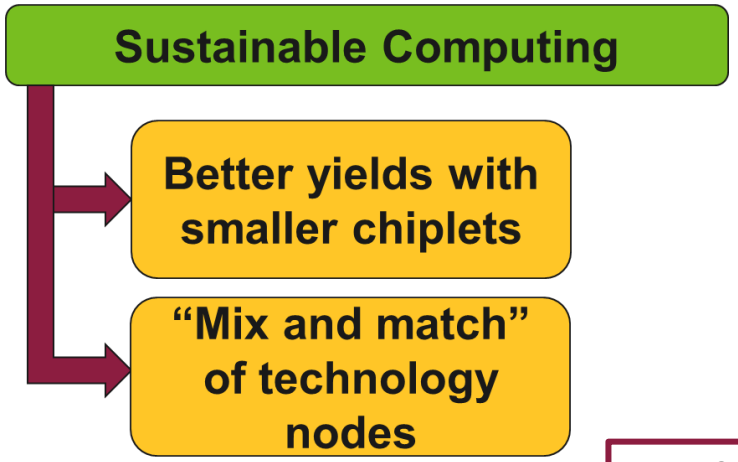
**Sustainable Computing**

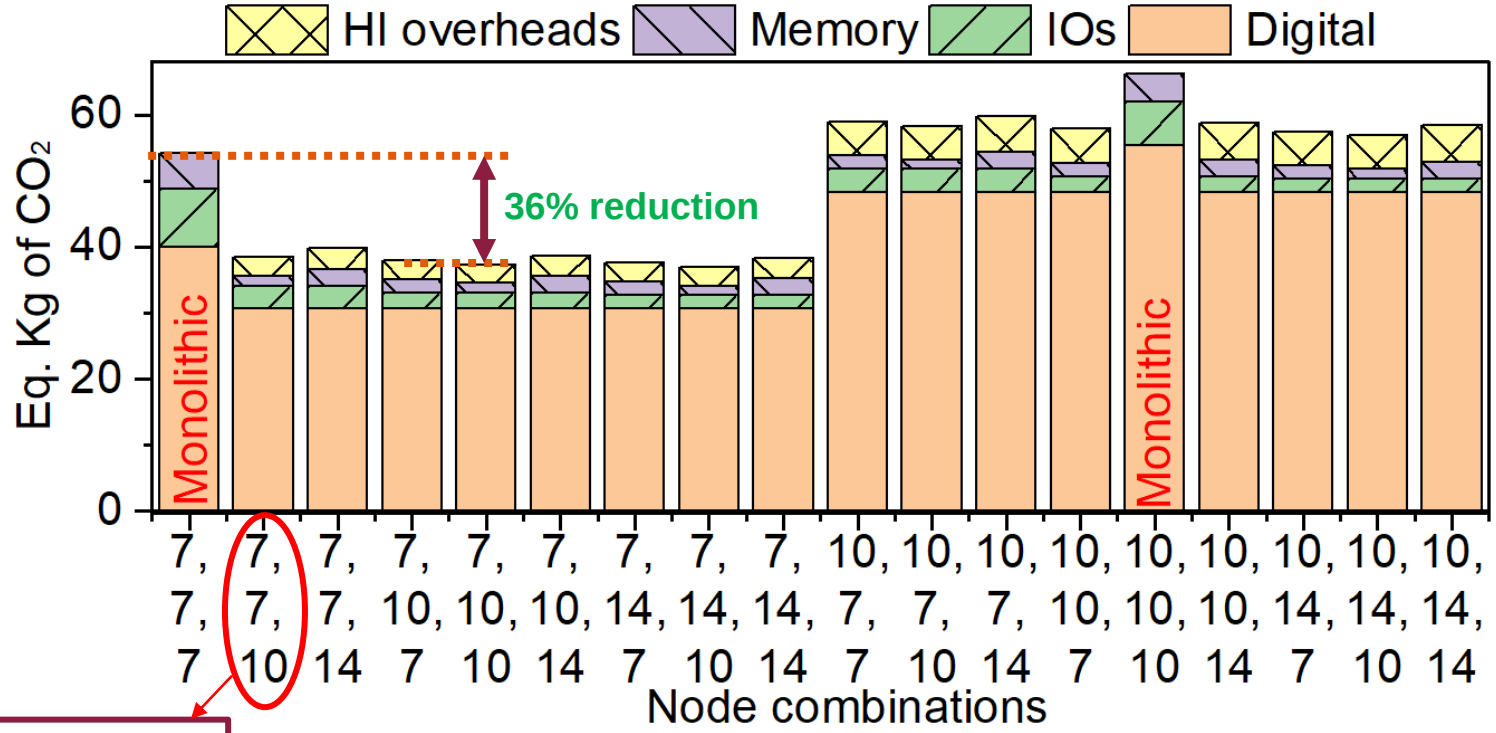
**Better yields with smaller chiplets**



# ECO-CHIP results: Key takeaways

- Disaggregation to chiplets helps in lowering the overall CFP by 40%
- Technology mix and match can help reduce overall CFP by 36%

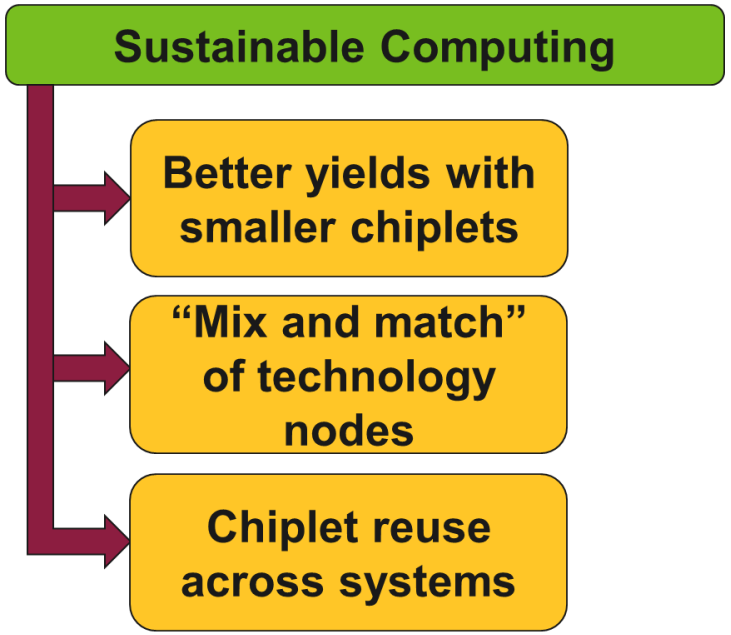


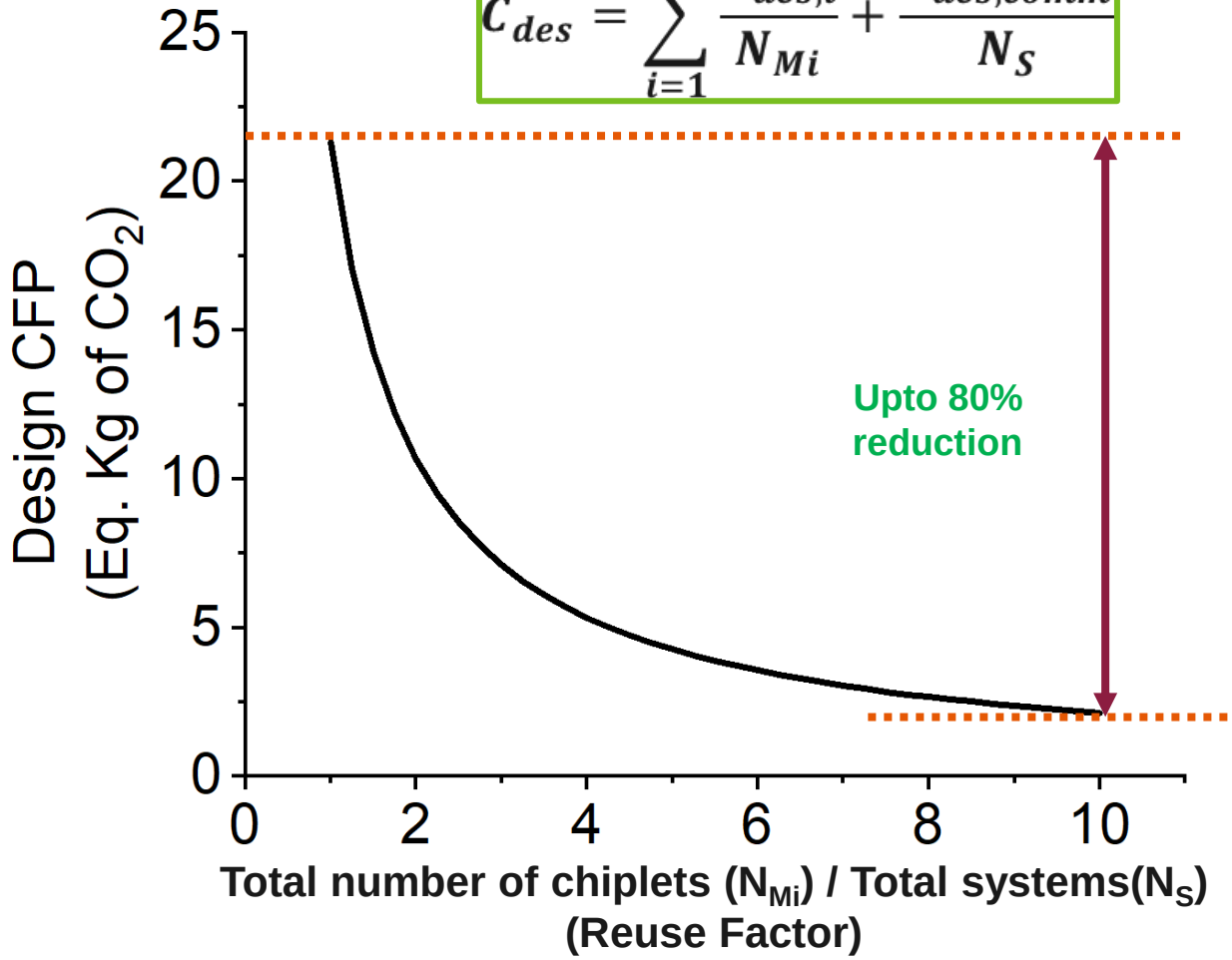

7,7,10 => 7nm Logic
7nm IOs
10nm Memory
7,7,7 => Monolithic on 7nm

# ECO-CHIP results: Key takeaways

- Disaggregation to chiplets helps in lowering the overall CFP by 40%
- Technology mix and match can help reduce overall CFP by 36%
- Amortizing the design CFP across multiple systems can reduce design CFP by 80%

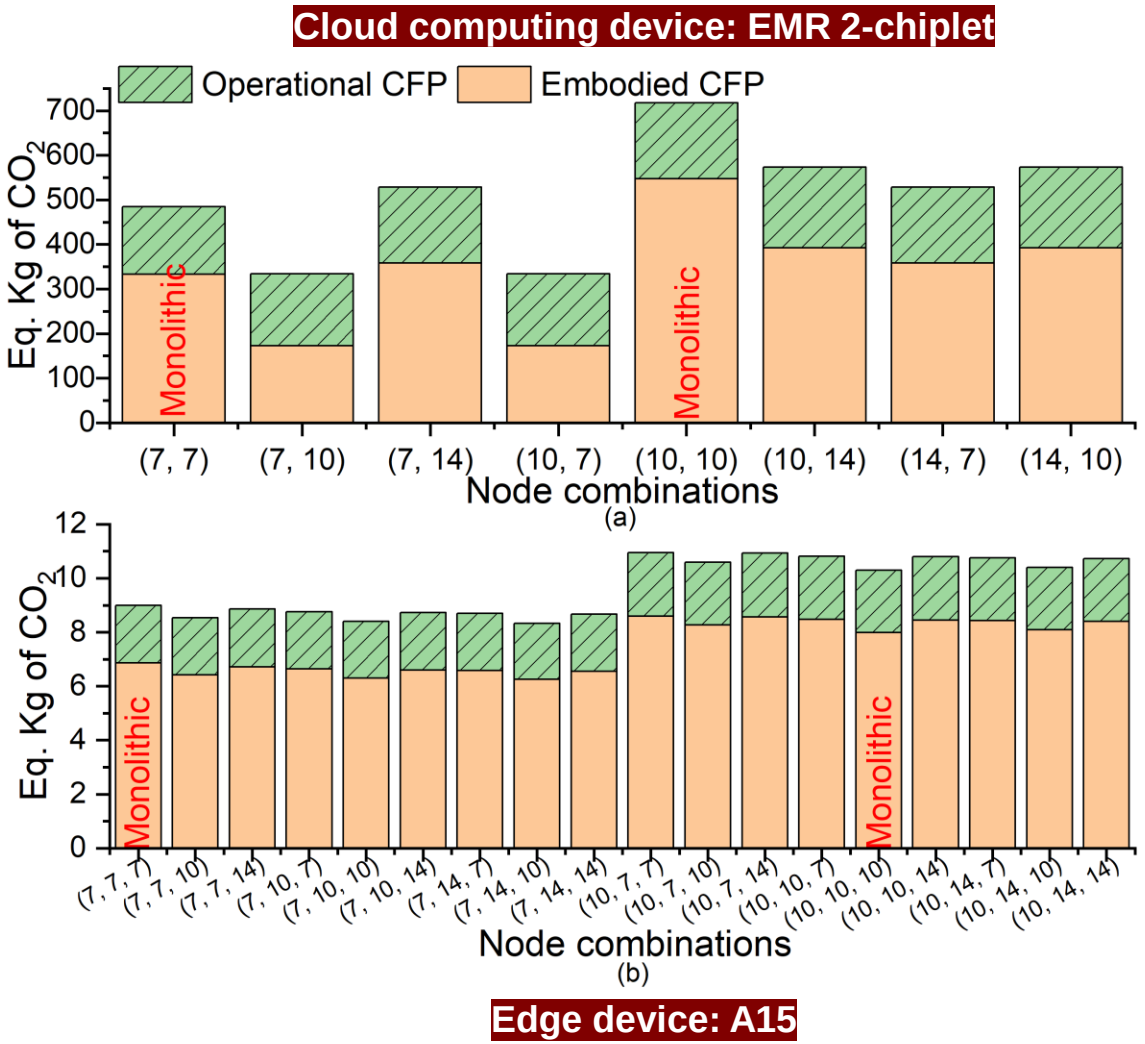



$$C_{des} = \sum_{i=1}^{Nc} \frac{C_{des,i}}{N_{Mi}} + \frac{C_{des,comm}}{N_S}$$



# ECO-CHIP results: Key takeaways

- Disaggregation to chiplets helps in lowering the overall CFP by 40%
- Technology mix and match can help reduce overall CFP by 36%
- Amortizing the design CFP across multiple systems can reduce design CFP by 80%
- Edge devices
  - $C_{emb}$ dominates, $C_{op}$ already low
  - Disaggregation helps lower $C_{emb}$
- Cloud computing devices
  - Higher $C_{op}$ / $C_{emb}$ ratio
  - Disaggregation helps lower $C_{emb}$

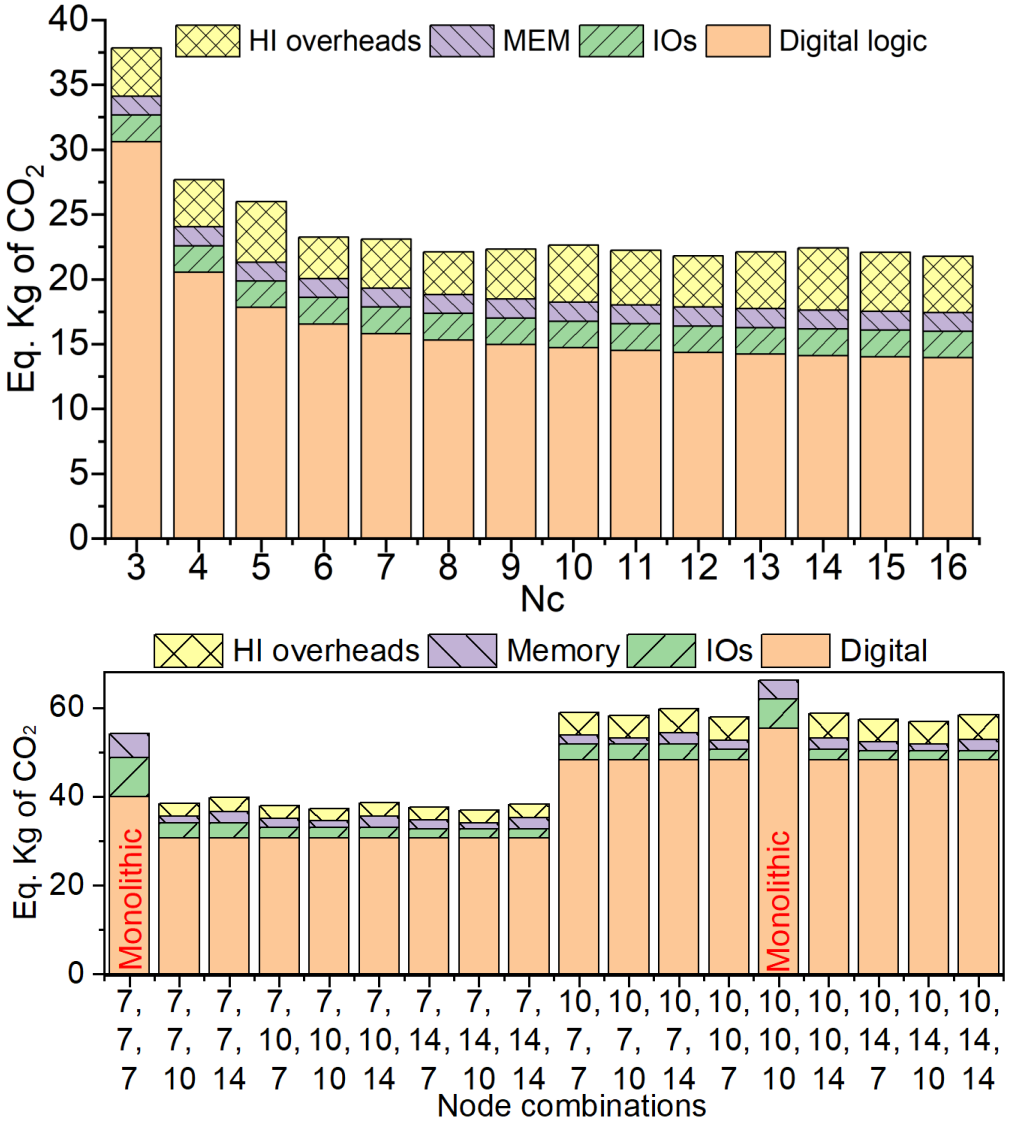


# Agenda

- Introduction
- Prior work
  - Architectural carbon footprint modeling (ACT)
- ECO-CHIP
  - HI Pathway to sustainability
  - Framework
  - ECO-CHIP CFP models
  - Key takeaways
- **Conclusion**

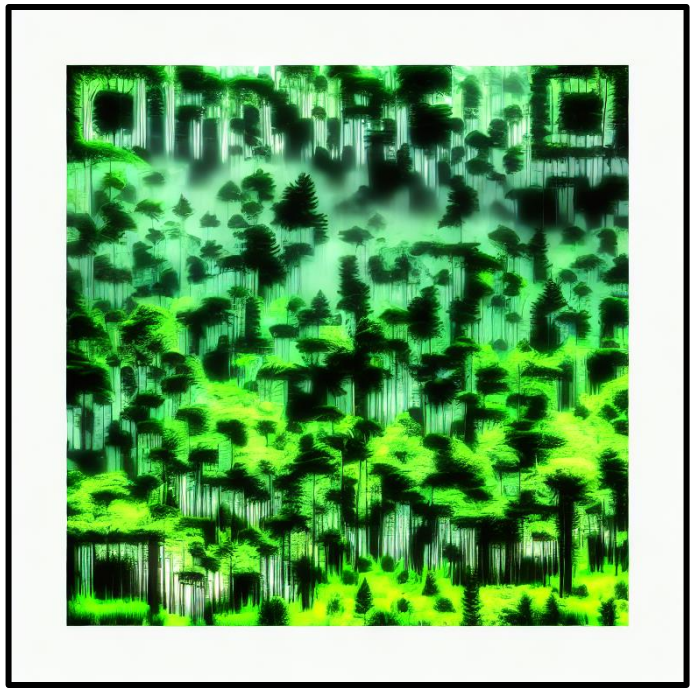
# Conclusion

- Key contributions
  - Develop ECO-CHIP for heterogeneous systems
    - Model yield variations across multiple technology nodes for CFP analysis
    - CFP modeling for design
    - CFP of advanced packing architecture was modeled
  - HI systems are pathways to sustainable computing
    - Moving to chiplet-based design reduced CFP by **40%**
    - Can reduce up to **80%** of design CFP by amortizing and increasing the reuse factor
    - Chiplet and technology space exploration can reduce the overall CFP by **36%**



# ECO-CHIP GitHub repository

- **We have open-sourced ECO-CHIP for broader access and awareness within the research community**



**Scan QR code for ECO-CHIP**

**https://github.com/ASU-VDA-Lab/ECO-CHIP**

README BSD-3-Clause license

## ECO-CHIP : Estimation of Carbon Footprint of Chiplet-based Architectures for Sustainable VLSI

[paper]

Carbon footprint estimator for heterogenous chiplet-based systems. ECO-CHIP is an analysis tool that analyzes the operational and embodied CFP (design, manufacturing, and packaging). The tool supports the following HI and packaging architectures: RDL fanout, silicon bridge-based, passive and active interposer, and 3D integration. The tool evaluates the crucial package/assembly carbon emissions essential for HI systems, considering size, yield, and assembly process. In addition, it also estimates design CFP.

No packages published
Publish your first package

Contributors 2

VidyaChhabria

ChetanSudarshan Chetan Sudarshan

Languages

Python 100.0%

Suggested workflows

Published November 10, 2023 | Version v2

Software Open

ECO-CHIP: Estimation of Carbon Footprint of Chiplet-based Architectures for Sustainable VLSI: HPCA 2024 Artifact Evaluation

Choppali Sudarshan, Chetan[1]; Matkar, Nikhil[1]; Vrudhula, Sarma[1]; Sapatnekar, Sachin[2]; Chhabria, Vidya[1]

Hide affiliations

1. ROR Arizona State University
2. ROR University of Minnesota

91 VIEWS 9 DOWNLOADS

Show more details

Versions

Version v2 Nov 10, 2023
10.5281/zenodo.10223759

# Thank you!!