

Crowd Supply

Course Workbook 1

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About this Workbook

This workbook is designed to be used in conjunction with the Crowd Supply lab one workshop.

The contents of this workbook are created by Adiuvo Engineering & Training, Ltd.

If you have any questions about the contents, or need assistance, please contact Adam Taylor at adam@adiuvoengineering.com.

Pre-Lab

Workshop Prerequisites

Required Hardware

The following hardware is required to complete this series of labs

1. Digilent [Basys3 Development board](#)

Downloads and Installations

Step 1 – Download and install the following at least one day prior to the workshop. This may take a significant amount of time and drive space.

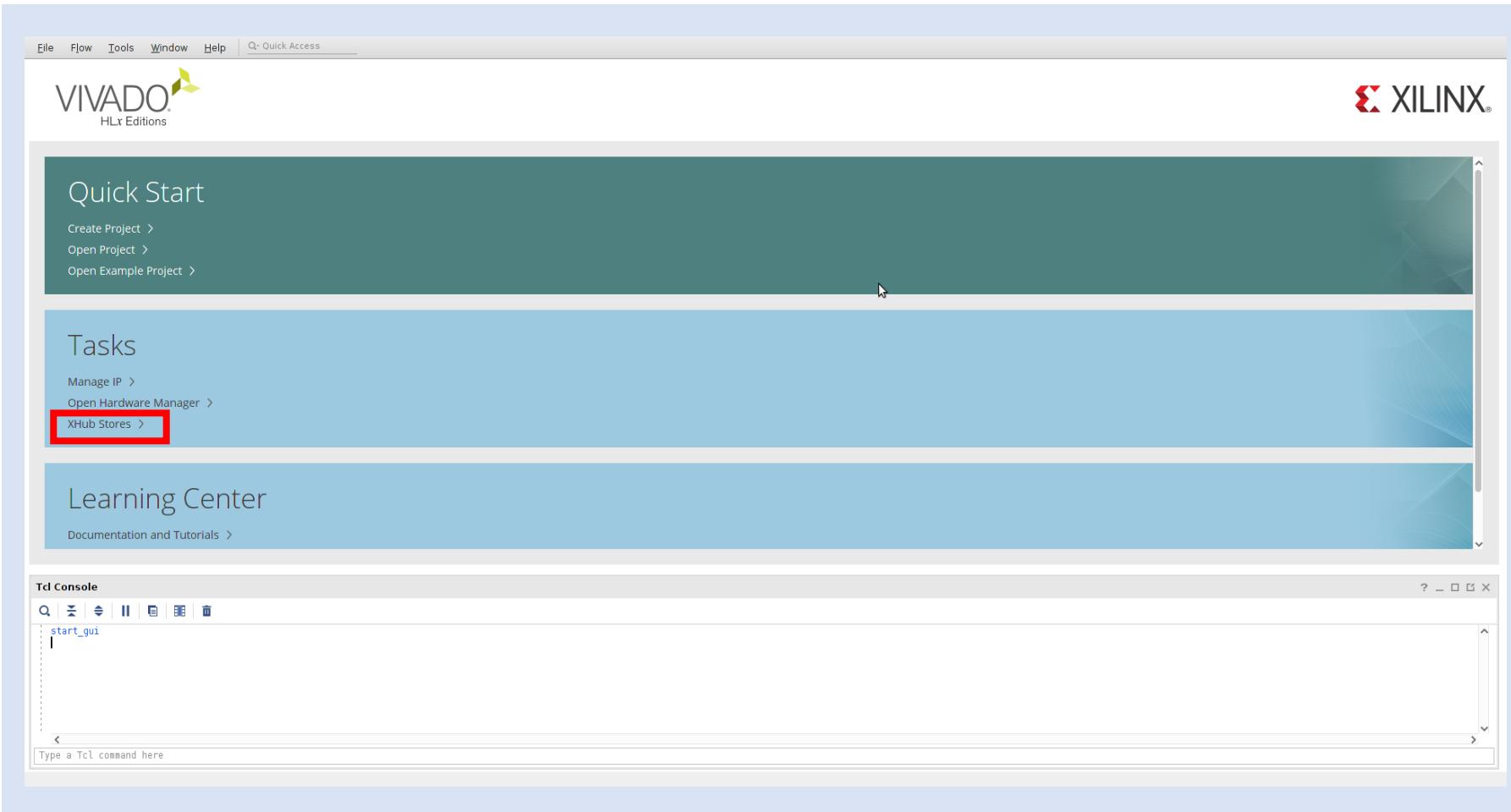
Vitis 2020.2 – Includes Vivado	Download
Source Project Files	Download

Lab

Creating Pong on the Basys3

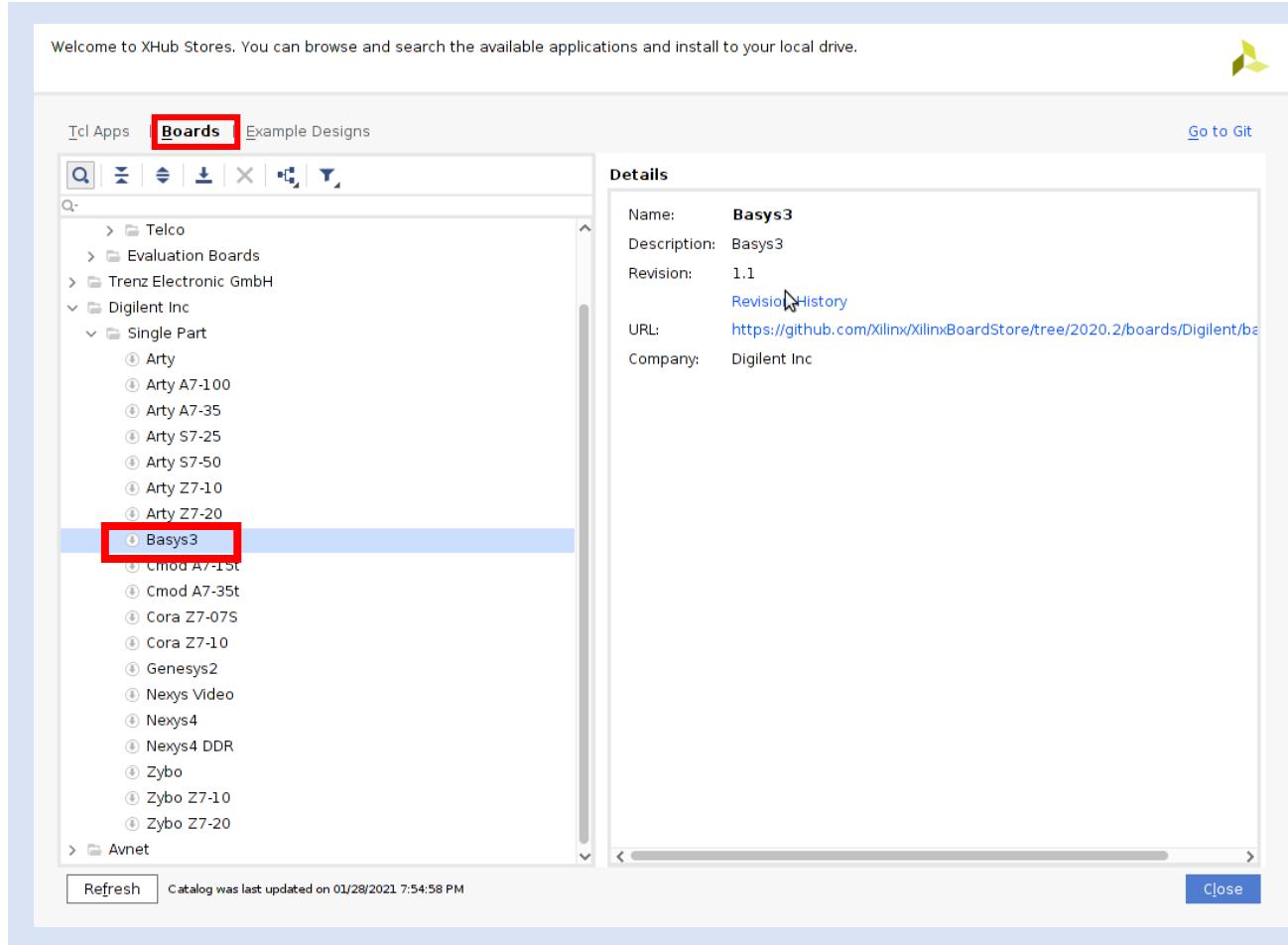
Crowd Supply: Lab One

Step 1 – Open Vivado 2020.2. Under “Tasks”, open “XHub Stores”



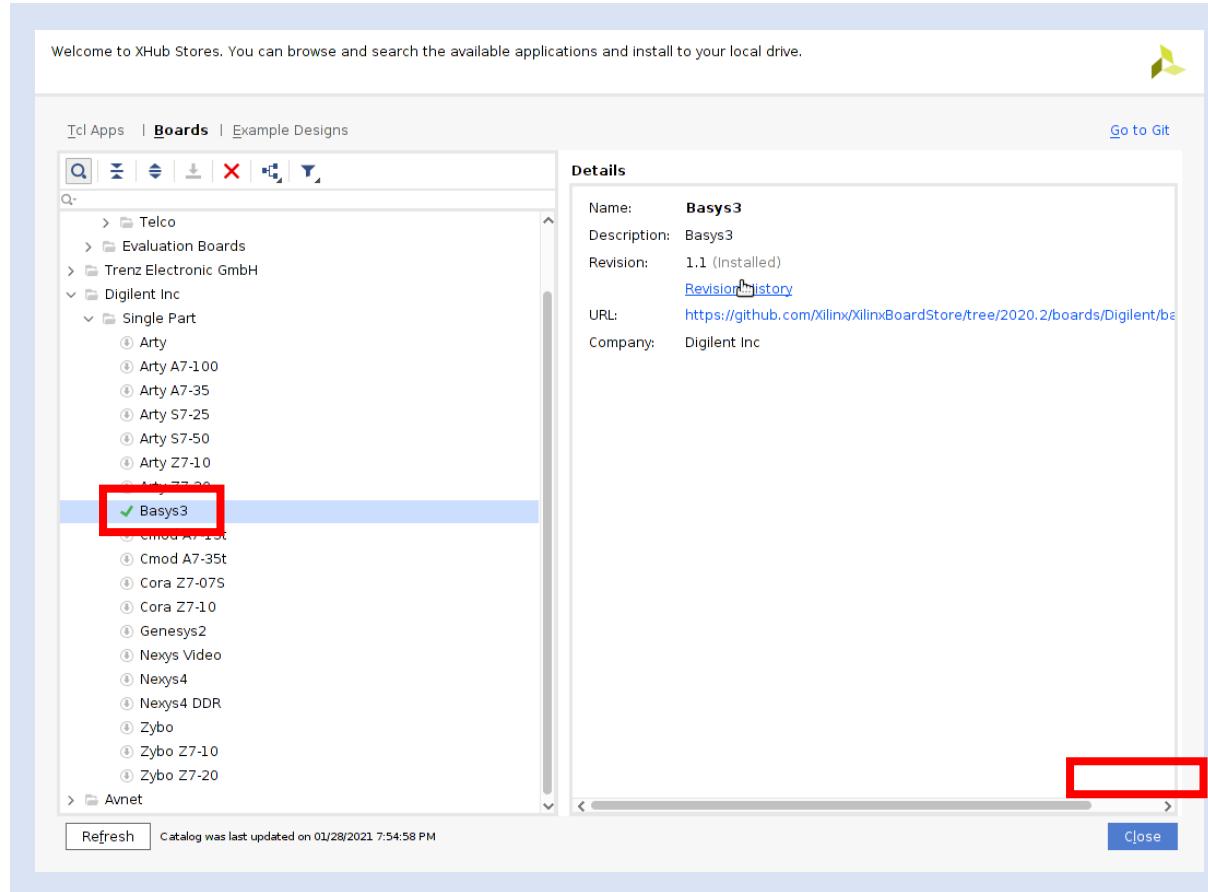
Crowd Supply: Lab One

Step 2 – In the XHub Store, navigate to the “Boards” tab and search for the “Basys3”. Right-click “Basys3” and select “Install”.



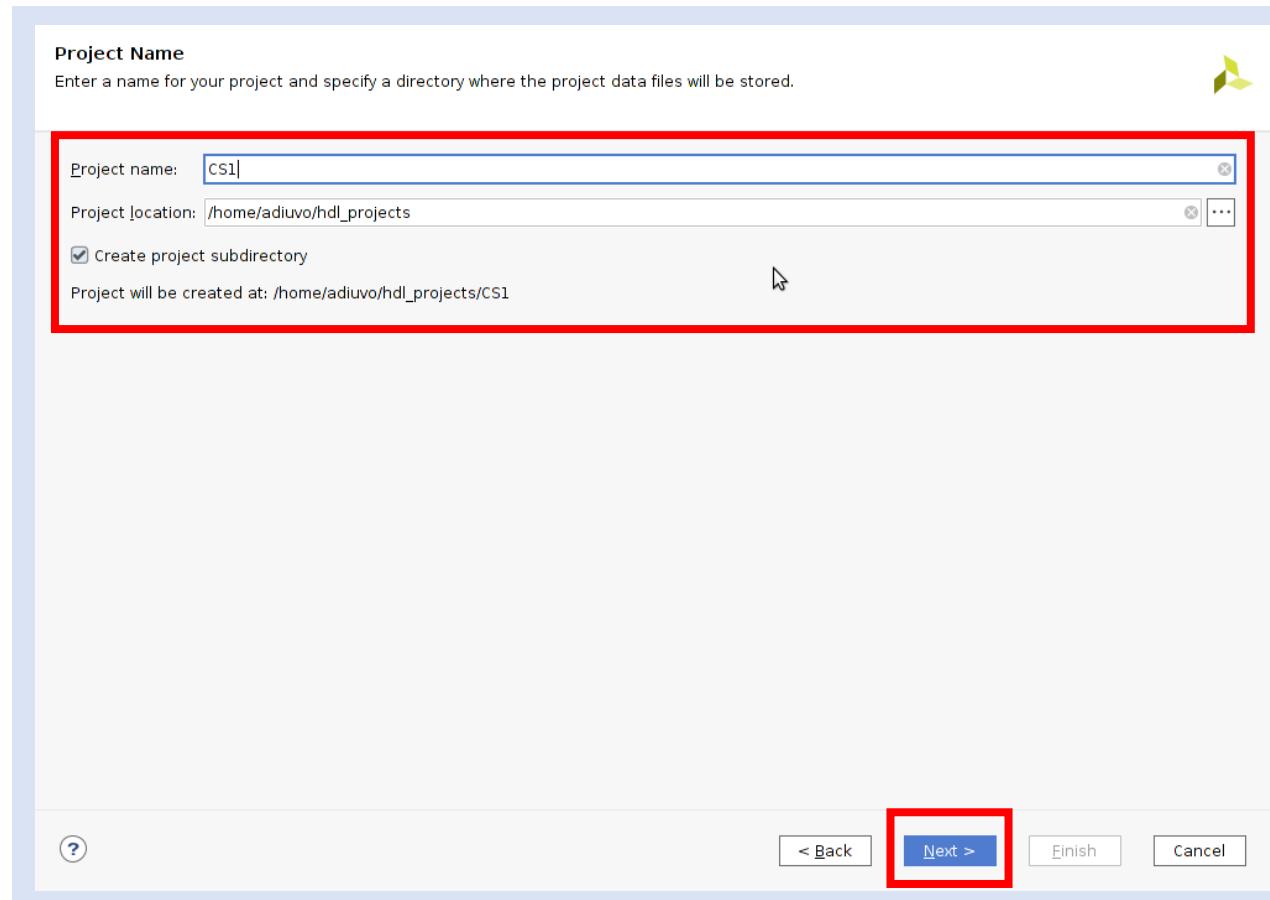
Crowd Supply: Lab One

Step 3 – When the Basys3 board is installed, a green check will appear next to the board. Click “Close” to return to the Vivado start page.



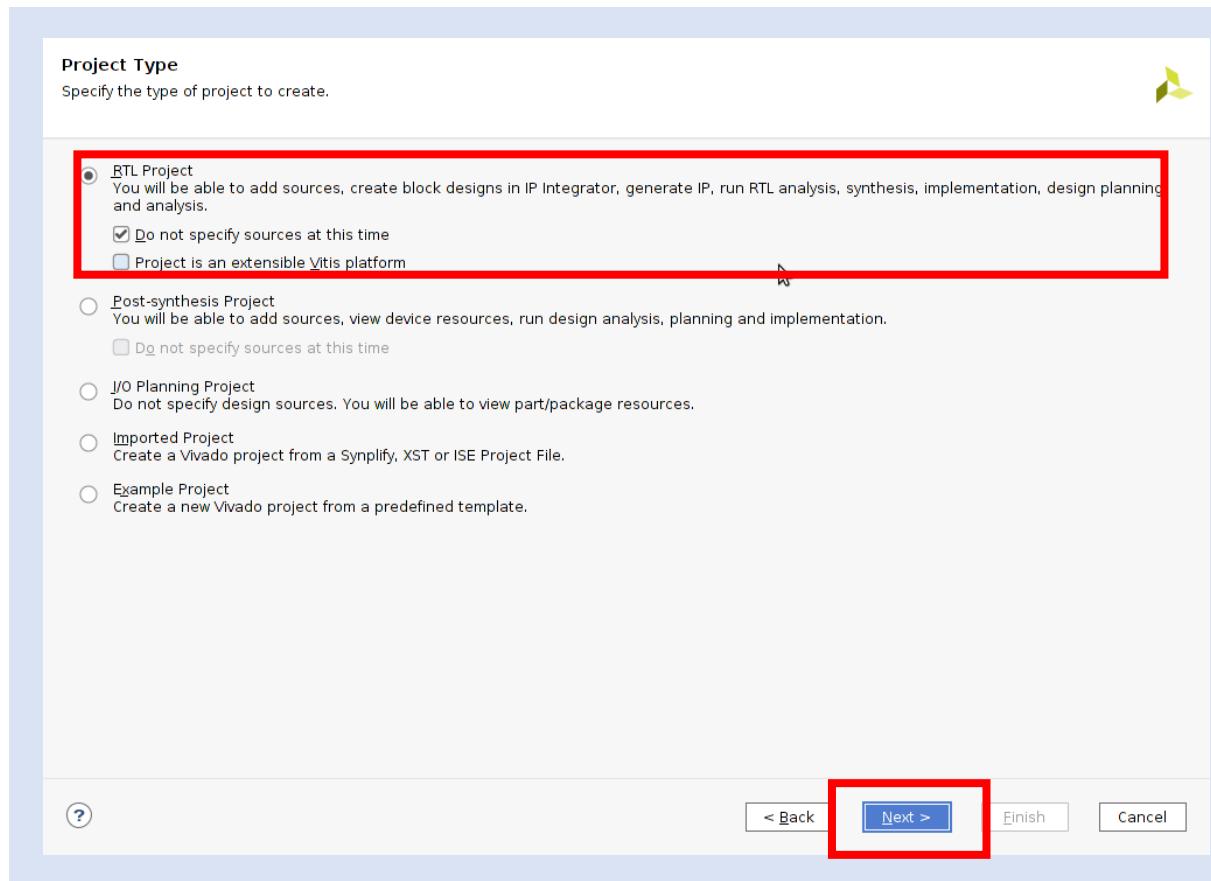
Crowd Supply: Lab One

Step 4 – Under “Quick Start”, select “Create Project”. When prompted, enter a project name (e.g. “CS1”) and location for the project folder. Click “Next”.



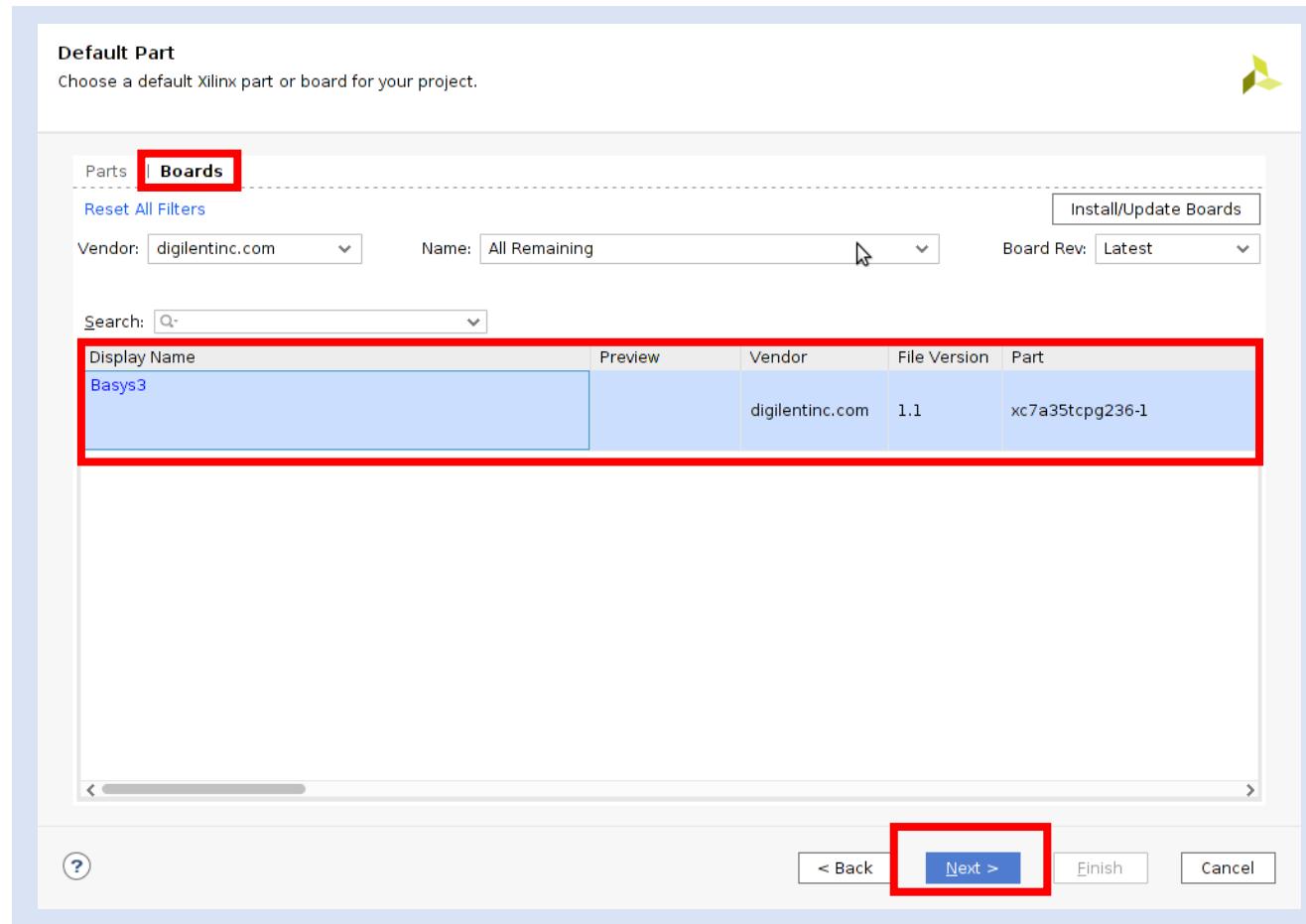
Crowd Supply: Lab One

Step 5 – “RTL Project” and check “Do no specify sources at this time”. Click “Next”.



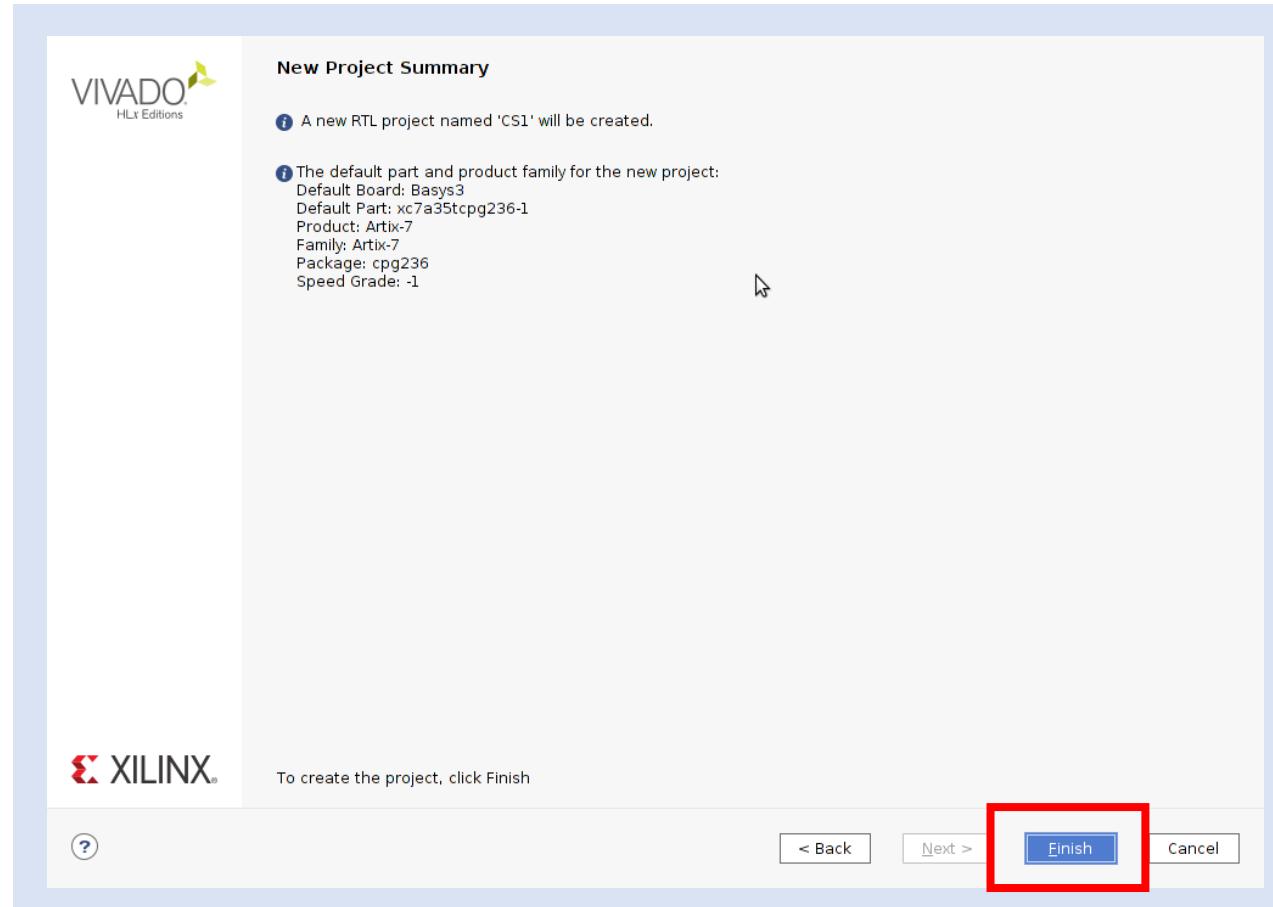
Crowd Supply: Lab One

Step 6 –In the “Boards” tab, select the Basys3 board (the selection will turn blue). Click “Next”.



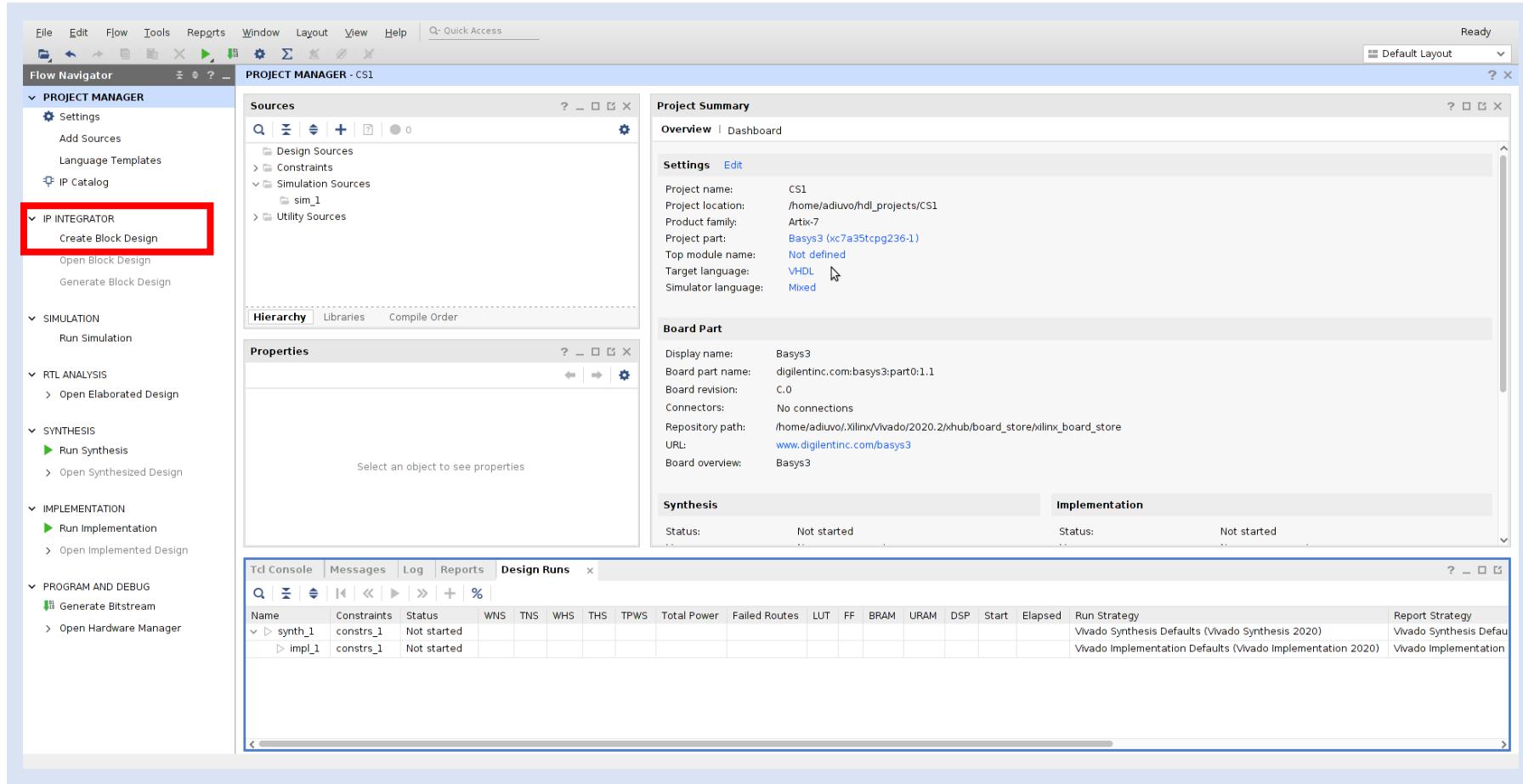
Crowd Supply: Lab One

Step 7 – Review the project summary page and click “Finish”.



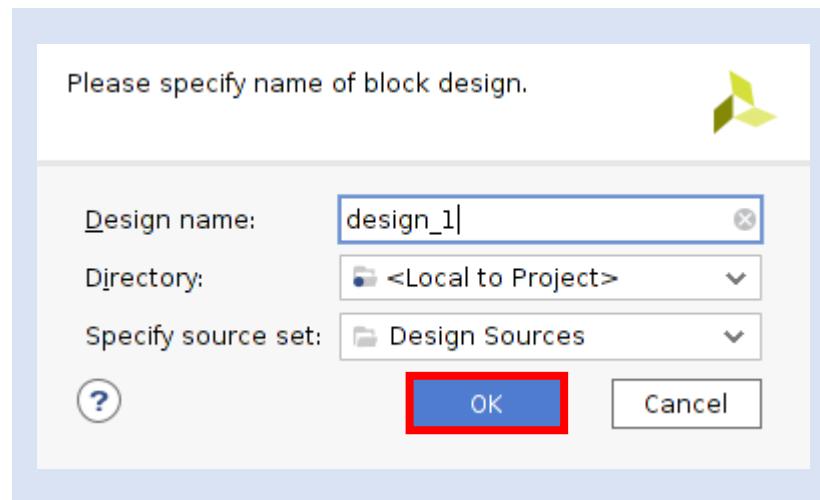
Crowd Supply: Lab One

Step 8 –The open project should appear as below. In Flow Navigator > IP Integrator, select “Create Block Design”.



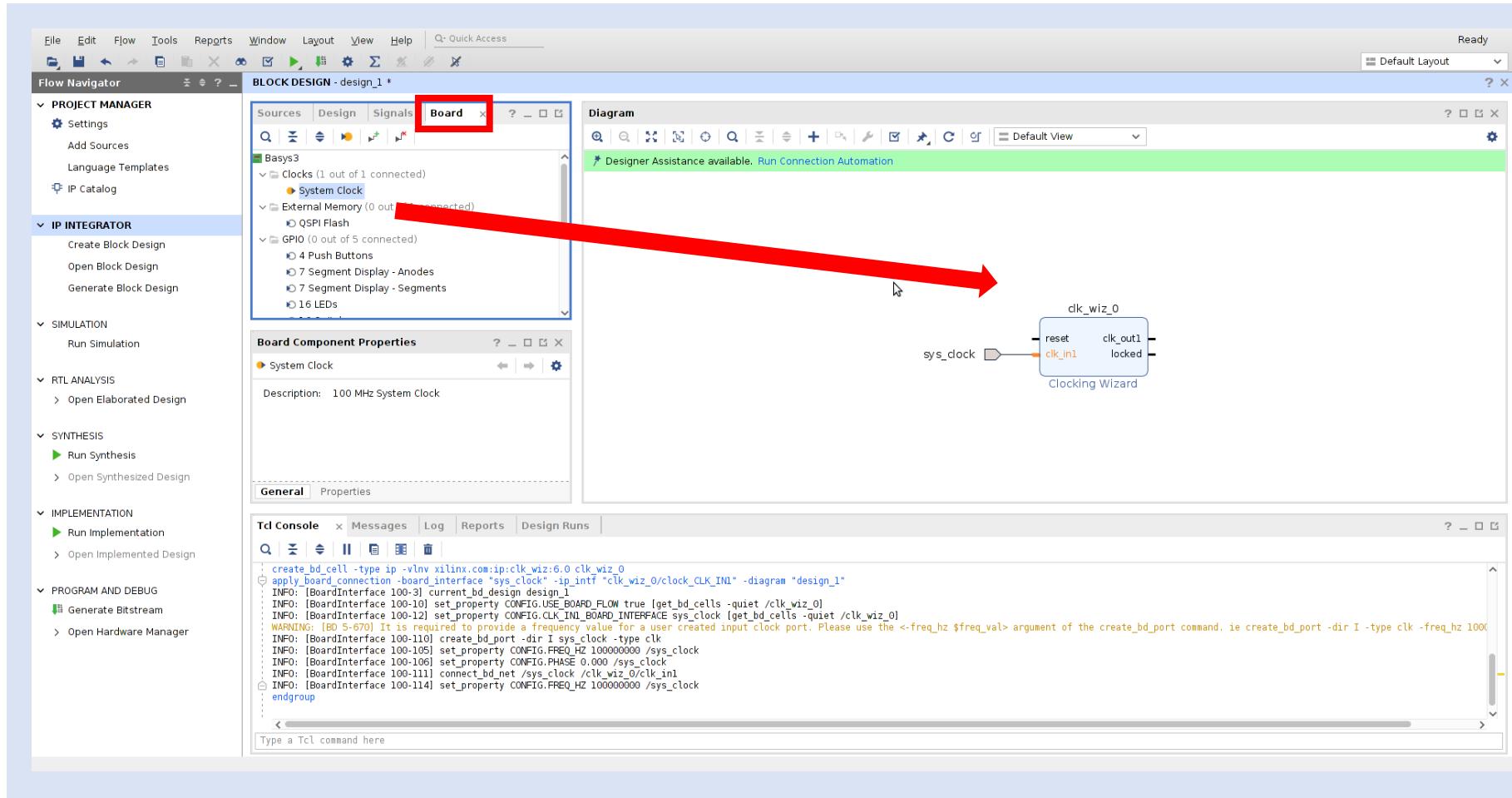
Crowd Supply: Lab One

Step 9 – Leave the defaults in the dialogue box which appears. Click “OK”



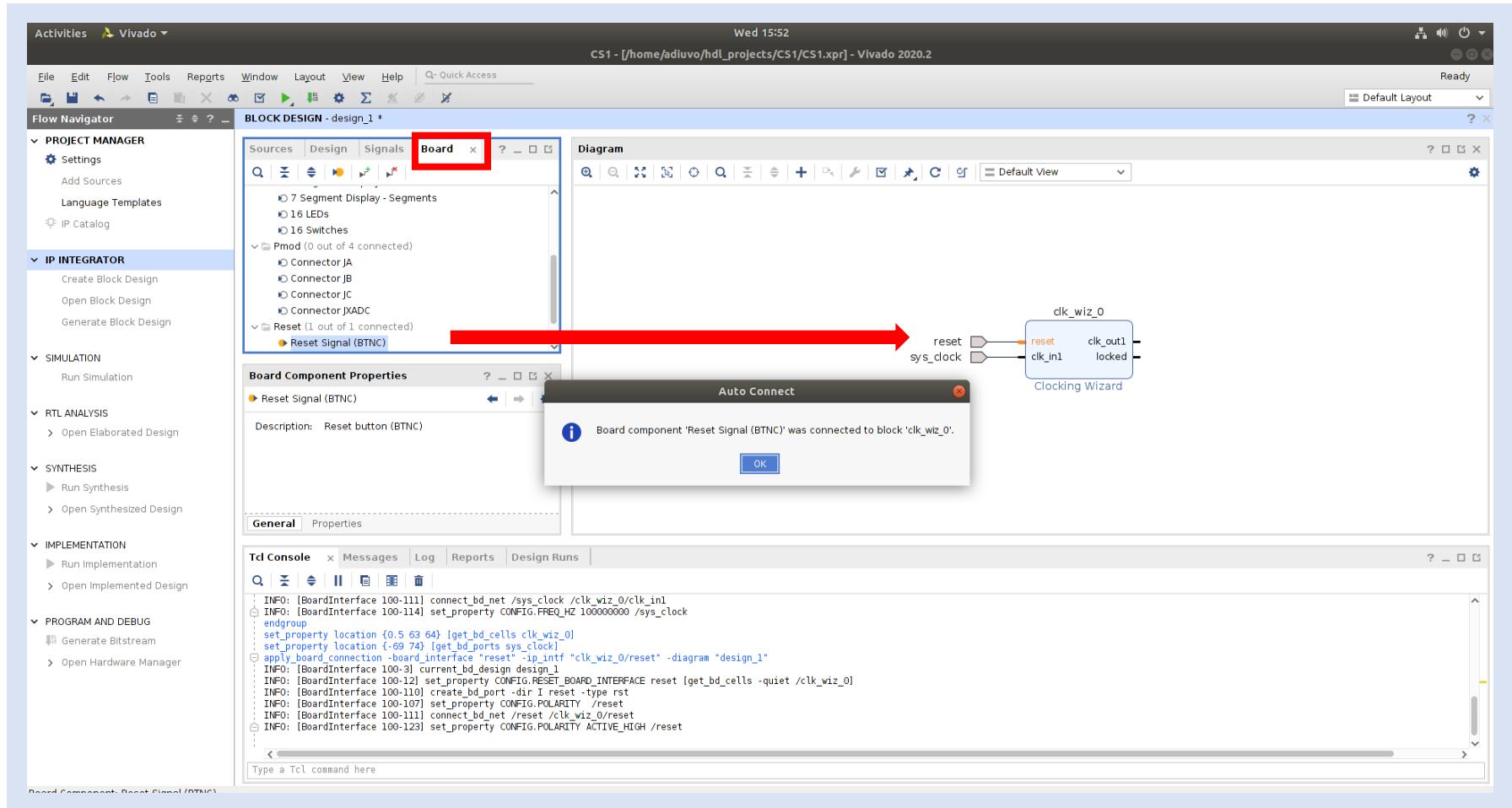
Crowd Supply: Lab One

Step 10 – Once the Block Design is created, select the Board tab and drag the system clock onto the block design. The block will appear in the diagram as shown below.



Crowd Supply: Lab One

Step 11 – From the Board tab, drag the Reset signal on to the reset pin of the clock wizard. After placement, the reset will appear external as shown below.

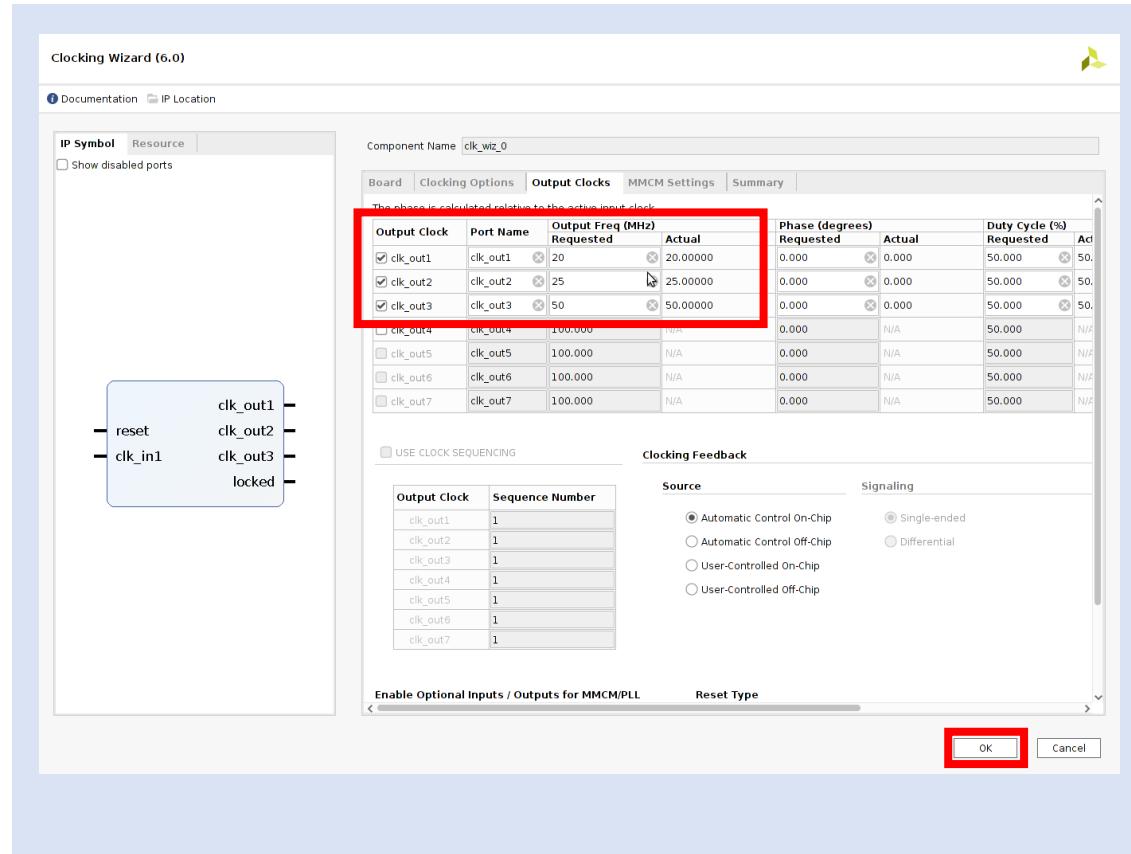


Crowd Supply: Lab One

Step 12 – Double click on the clock wizard block to open its customization menu. Check output clocks clk_out1, clk_out2, and clk_out 3 and set output frequency as shown below:

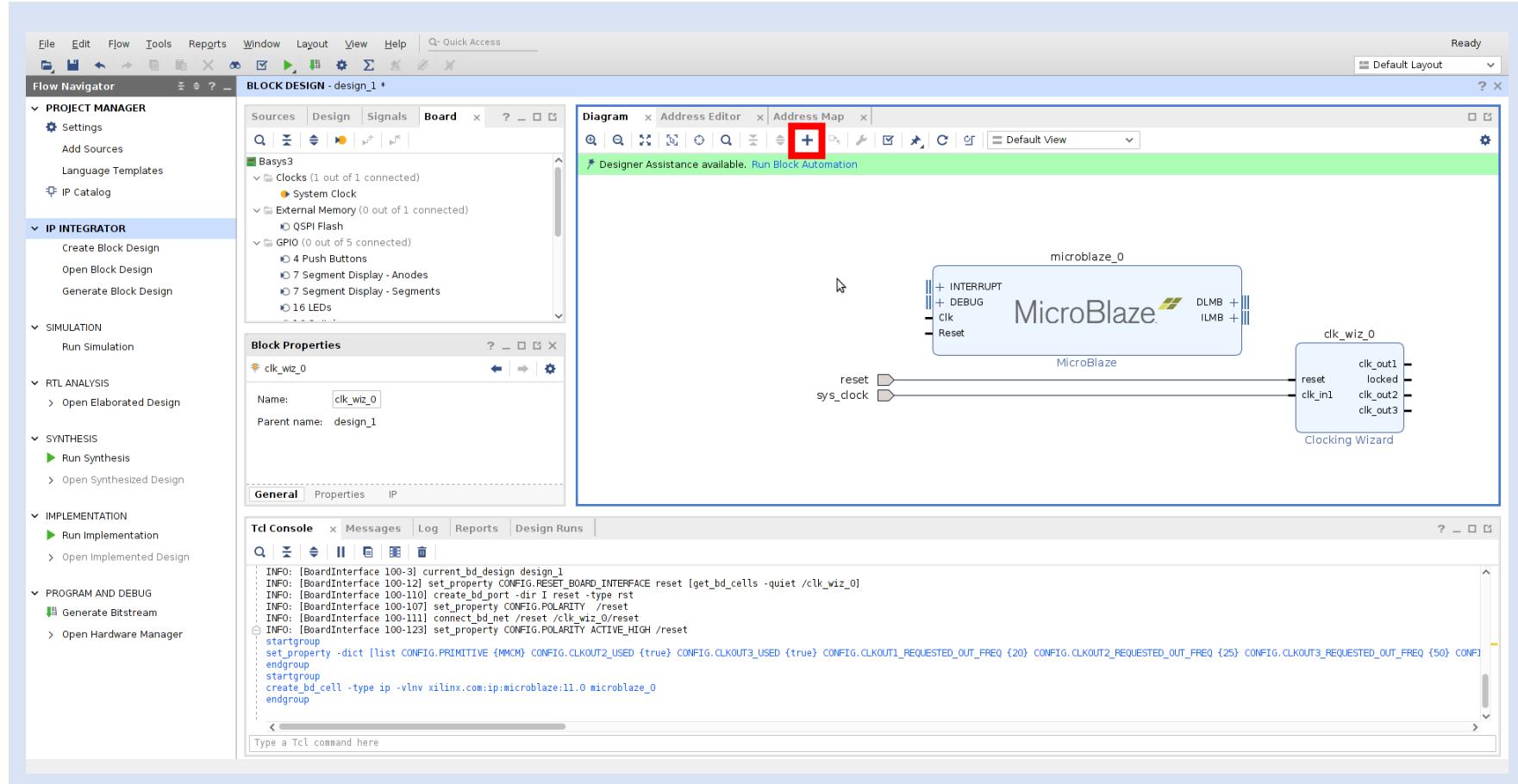
CLK1 = 20 MHz, CLK2 = 25MHz, CLK3 = 50MHz

Click “OK” to confirm settings and return to block diagram.



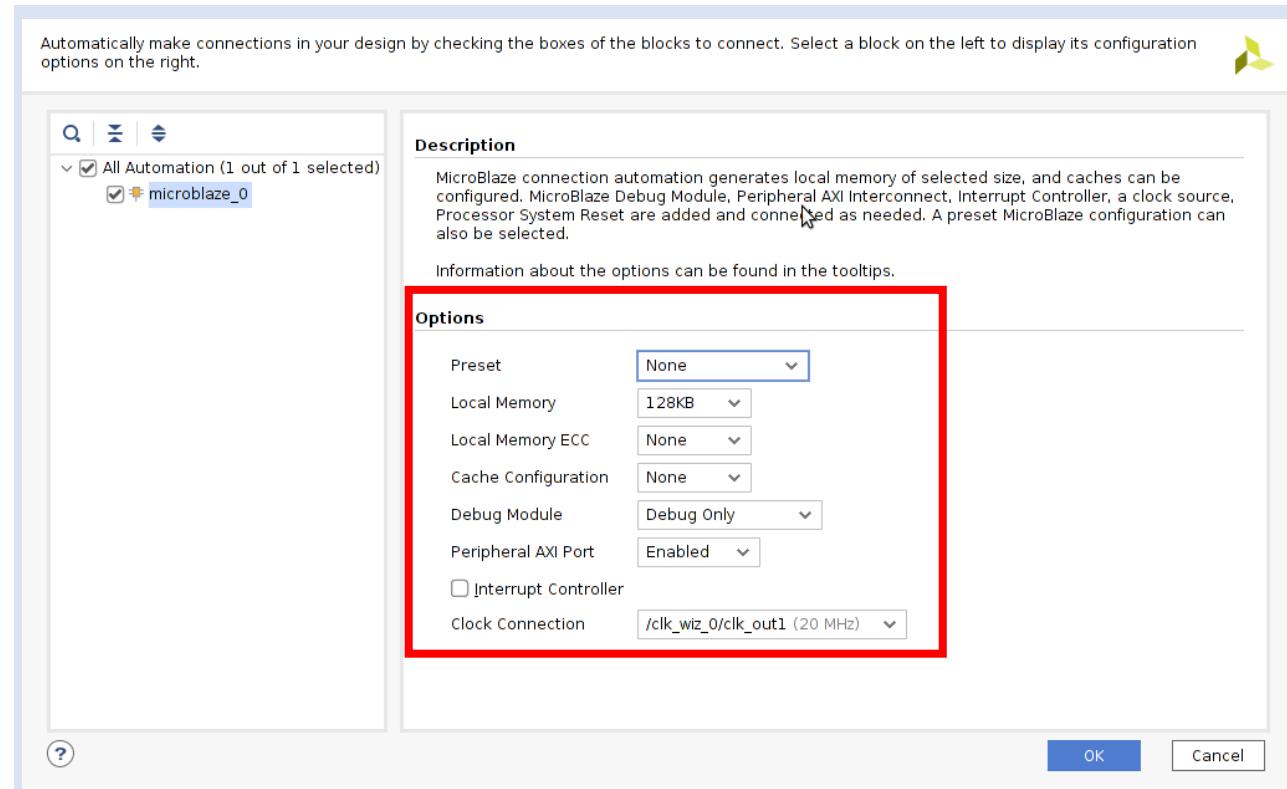
Crowd Supply: Lab One

Step 13 – Click on the + symbol and add a *MicroBlaze* IP block to the block design.



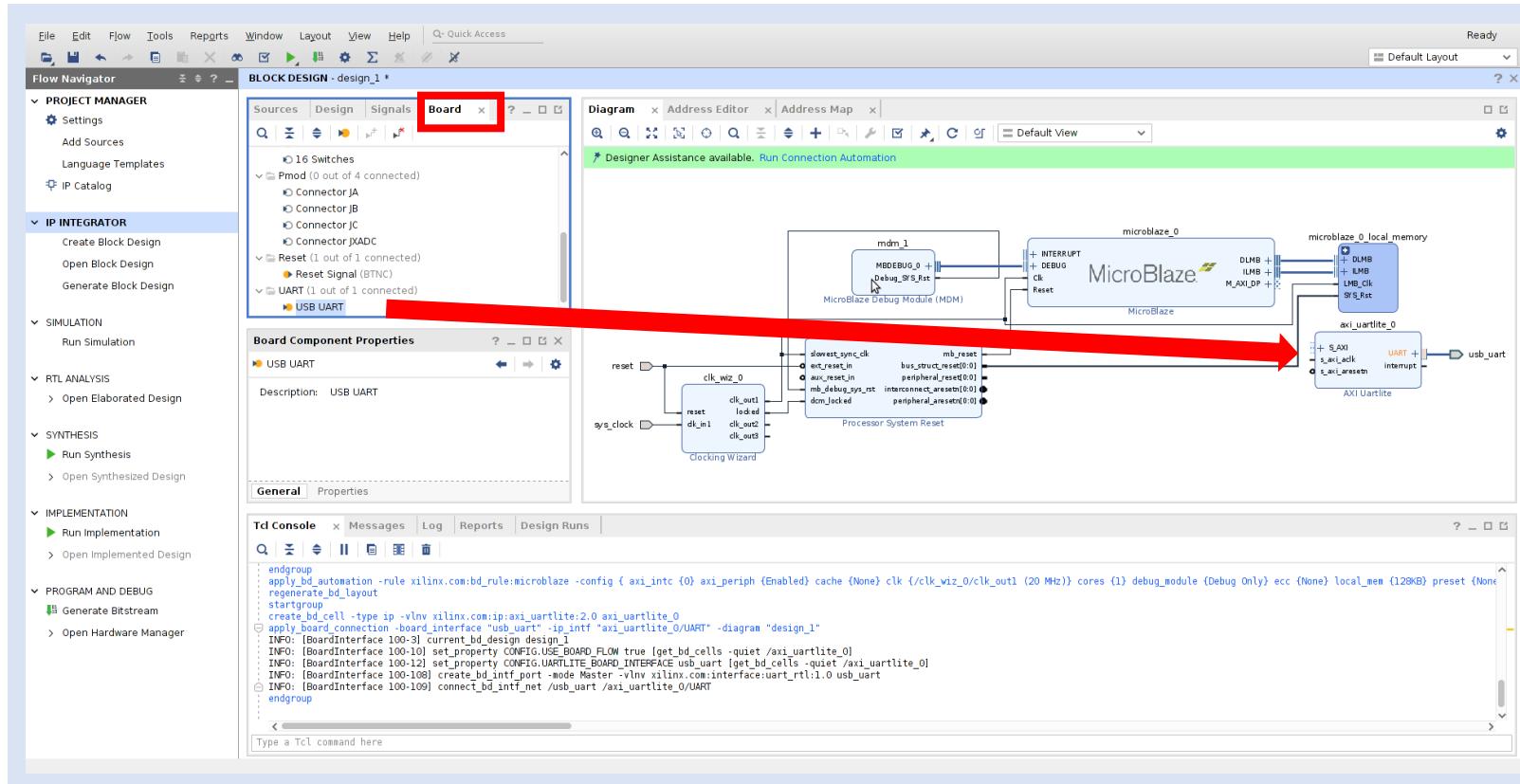
Crowd Supply: Lab One

Step 14 – Run Block Automation from the Designer Assistance suggestion, or by right-clicking the block diagram and selecting “Run Block Automation”. Select the MicroBlaze in the menu, set the local memory to 128KB and set the Peripheral AXI Port to enabled.



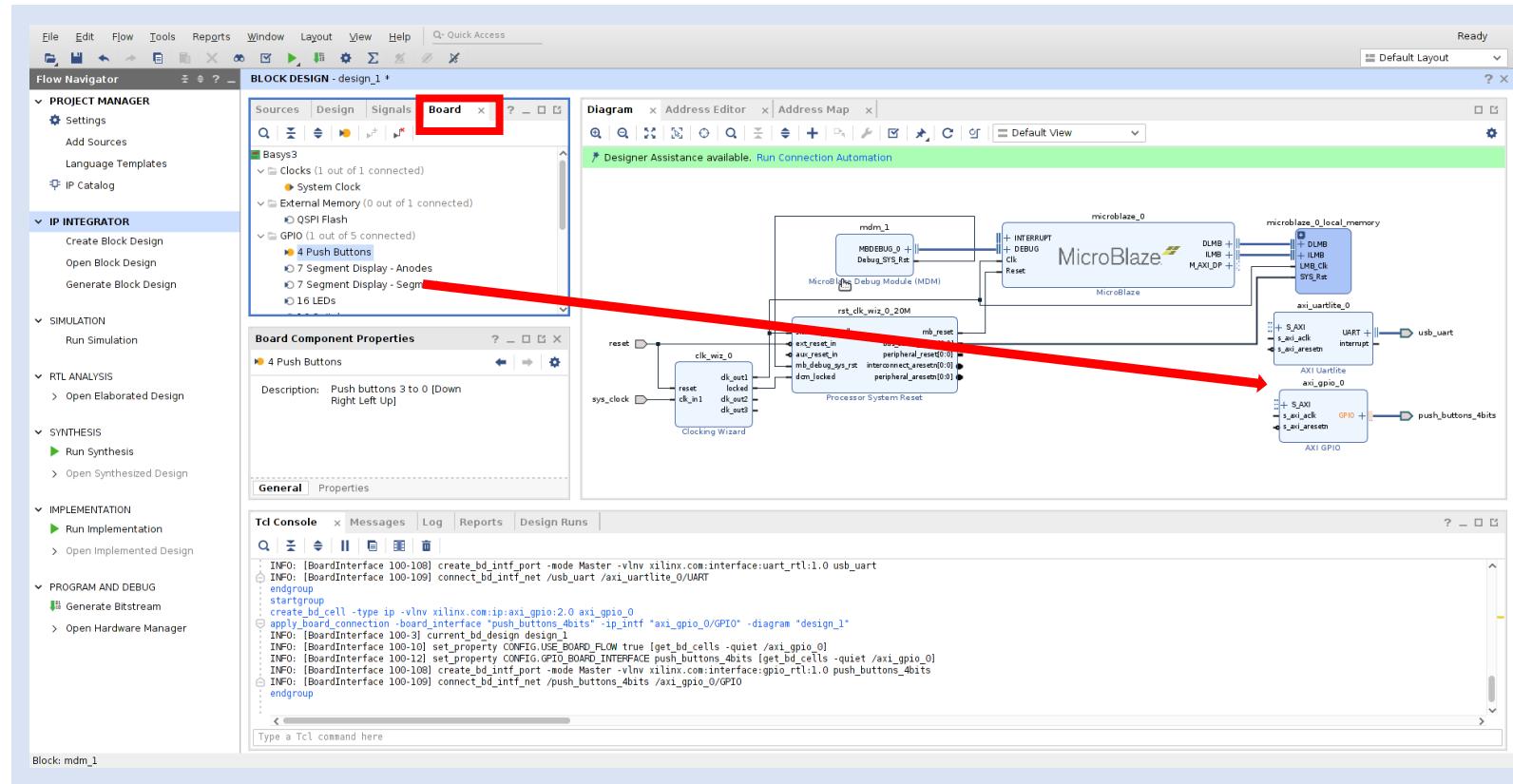
Crowd Supply: Lab One

Step 15 – This will create the MicroBlaze System as shown below. From the Board tab, drag the USB UART onto the block design. This will create the AXI UartLite block as shown below.



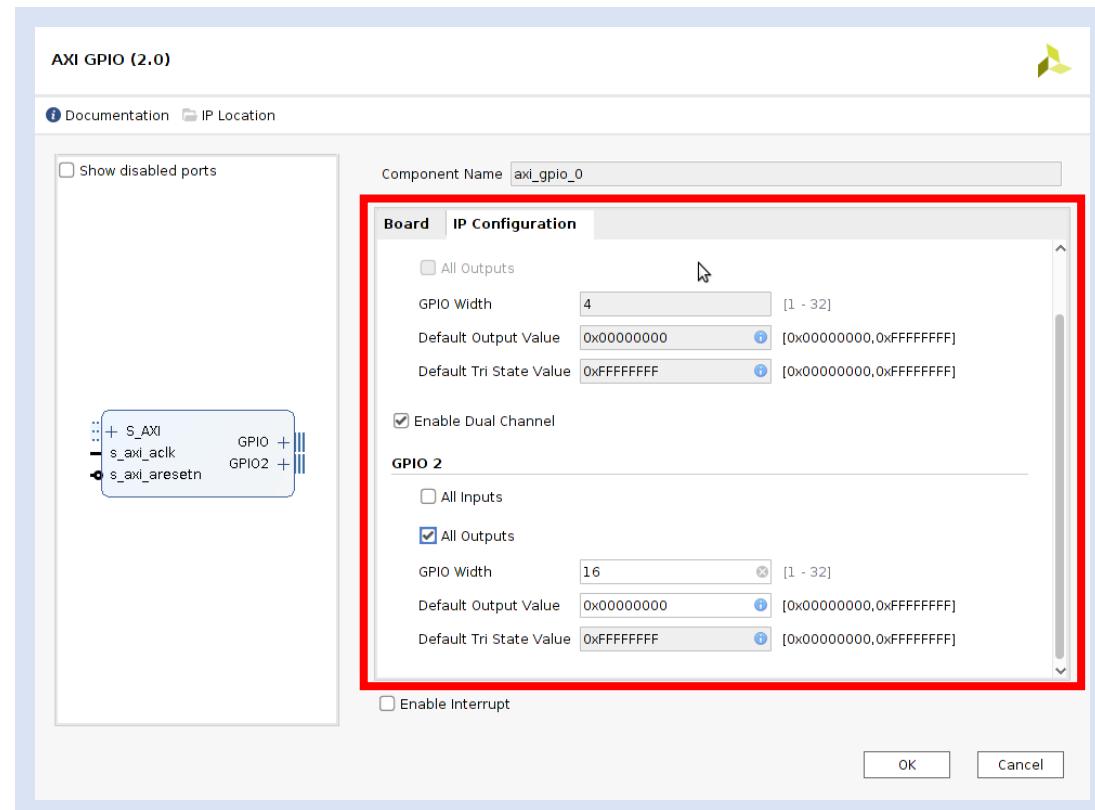
Crowd Supply: Lab One

Step 16 – From the Board tab drag and drop the 4 Push Buttons onto block diagram. This will create the AXI GPIO block as shown below.



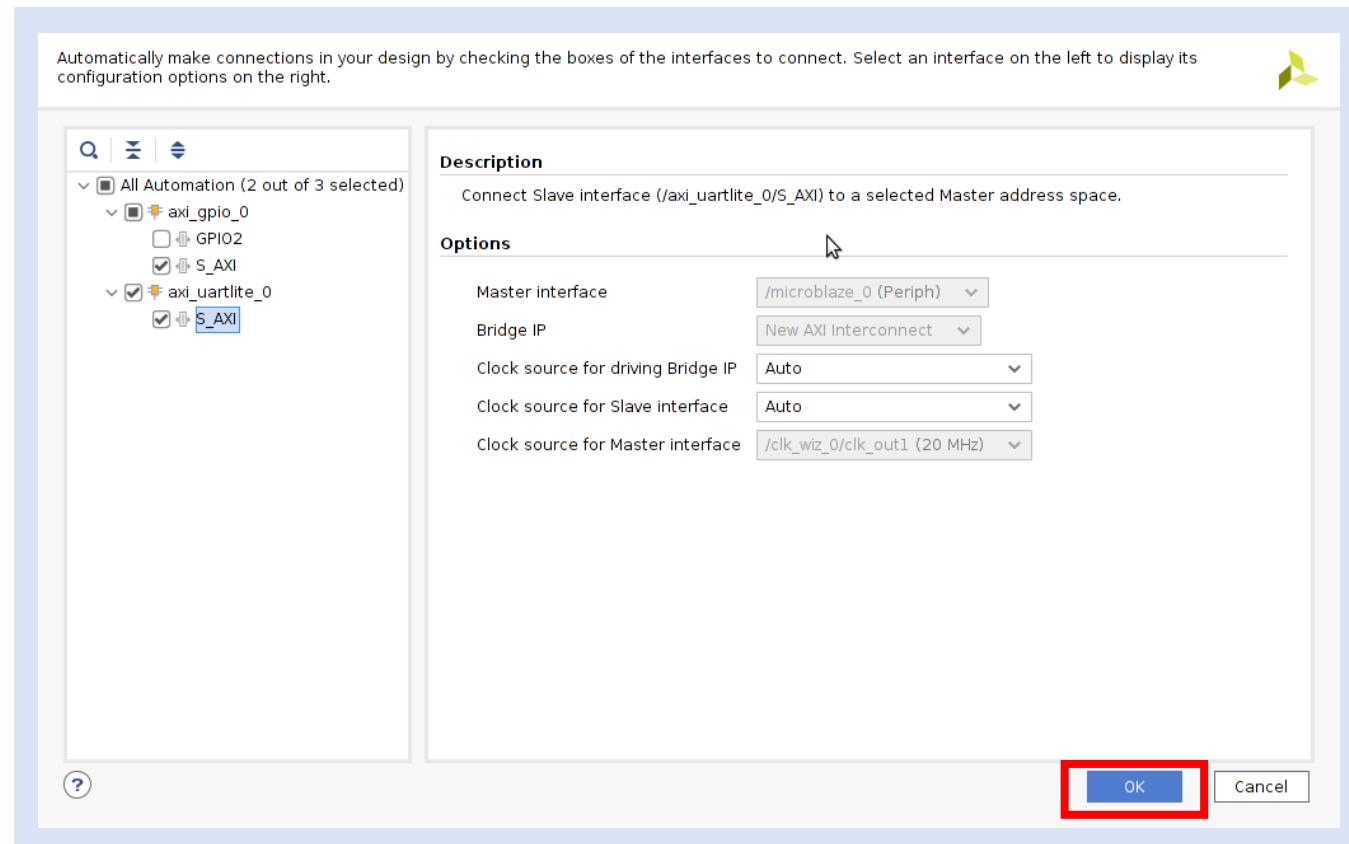
Crowd Supply: Lab One

Step 17 – Double-click on the AXI GPIO IP Block and in the IP Reconfiguration tab and customize the second channel as below (All Outputs, GPIO Width set to 16 bits).



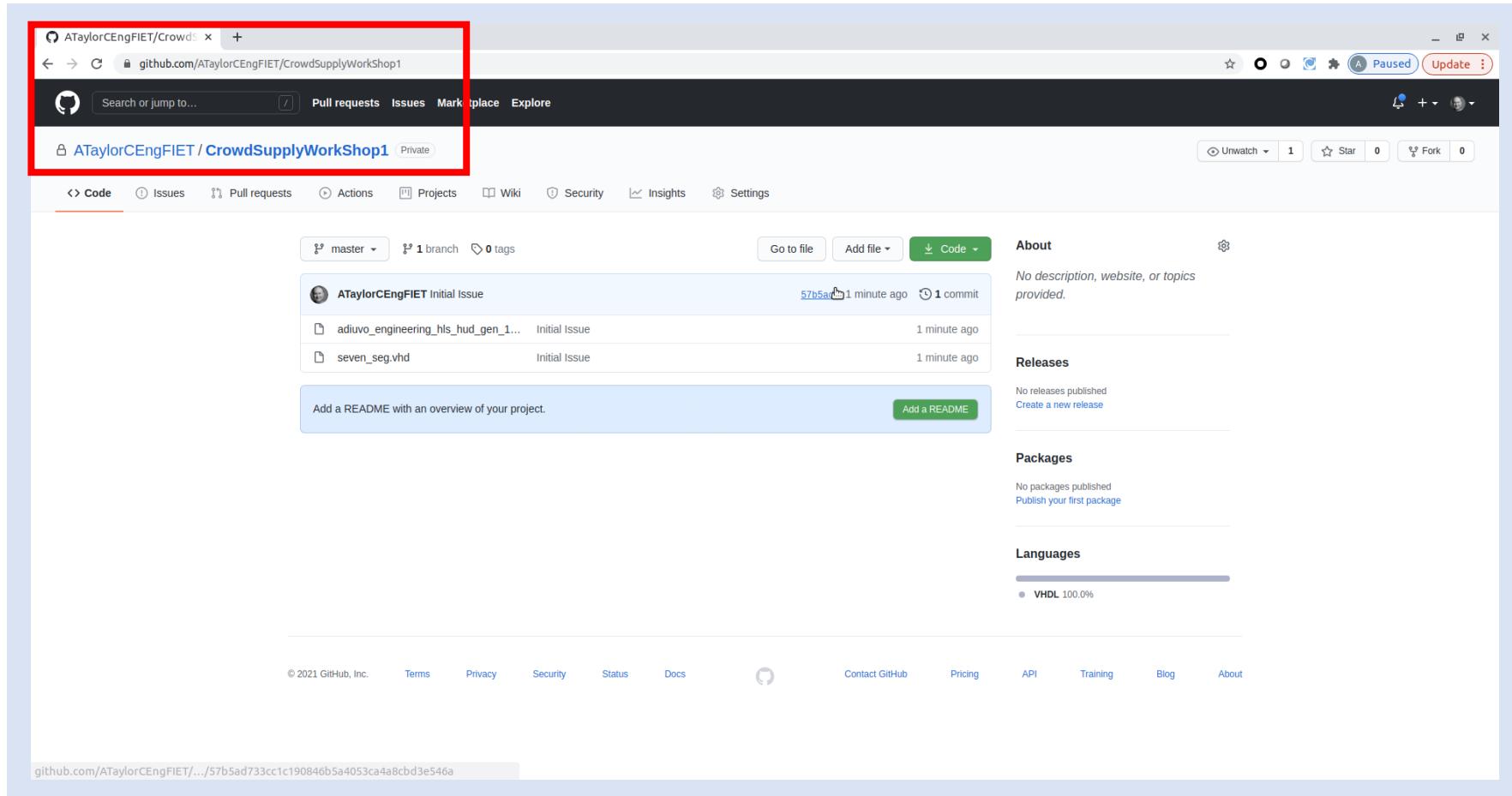
Crowd Supply: Lab One

Step 18 – Run Block Automation and select the AXI GPIO S_AXI and AXI UARTLite S_AXI interfaces in the left menu. Click “OK”.



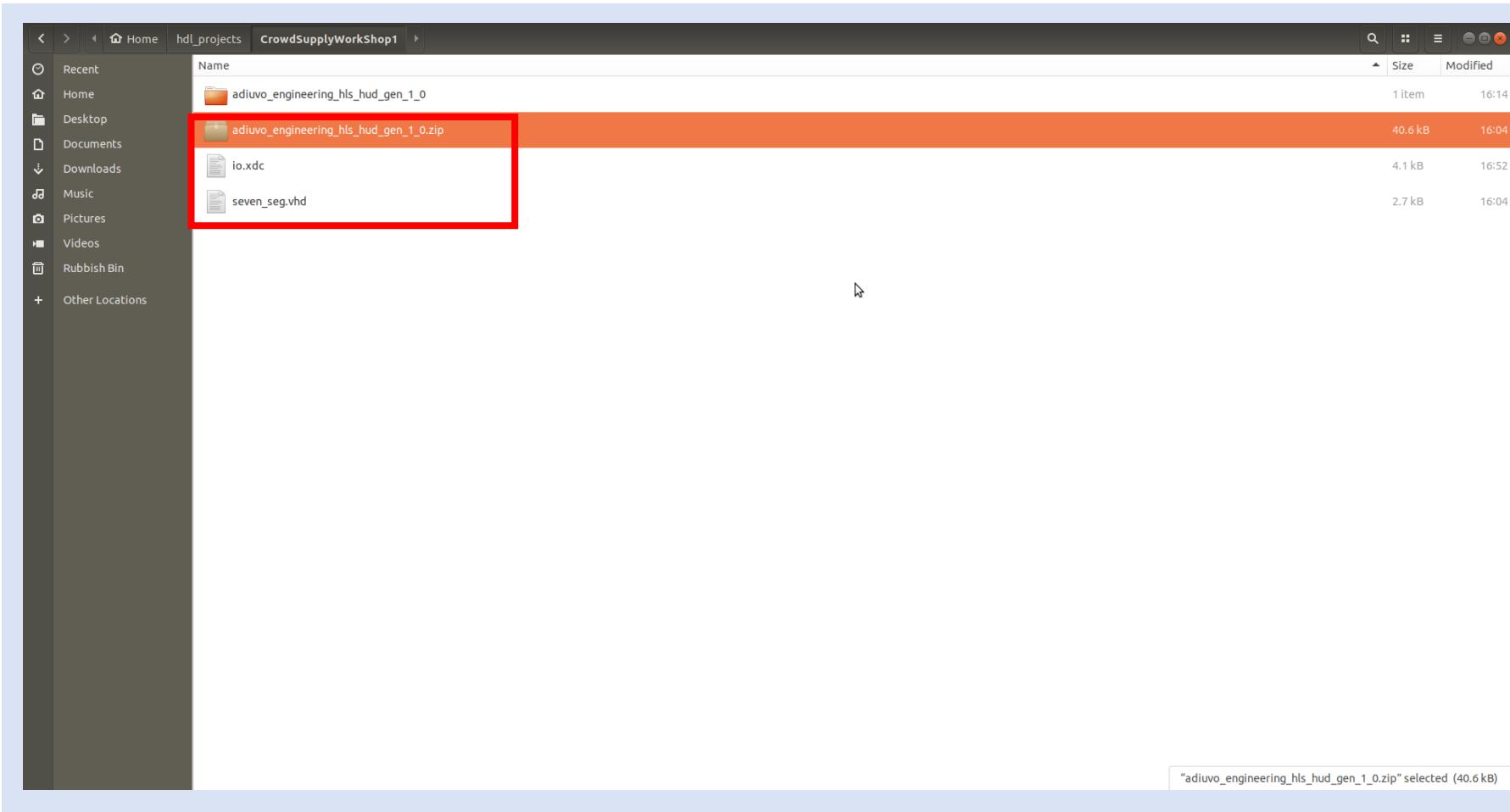
Crowd Supply: Lab One

Step 19 – If you haven't already, open a web browser and clone the IP files from the GitHub for this lab here: <https://github.com/ATaylorCEngFIET/CrowdSupplyWorkShop1>



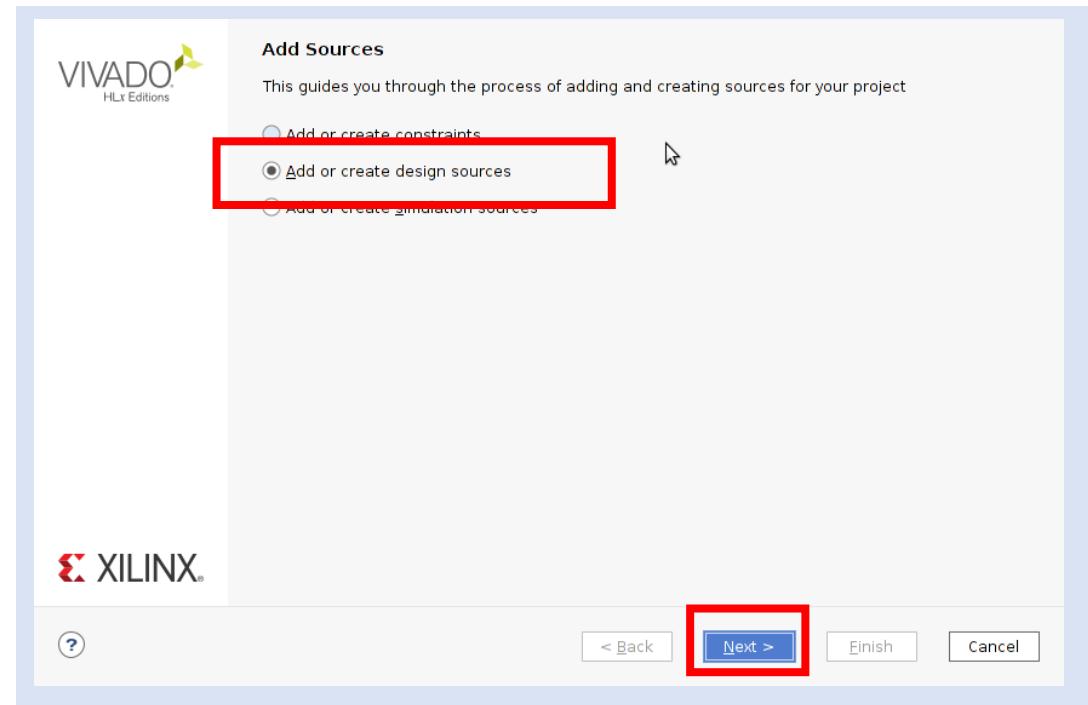
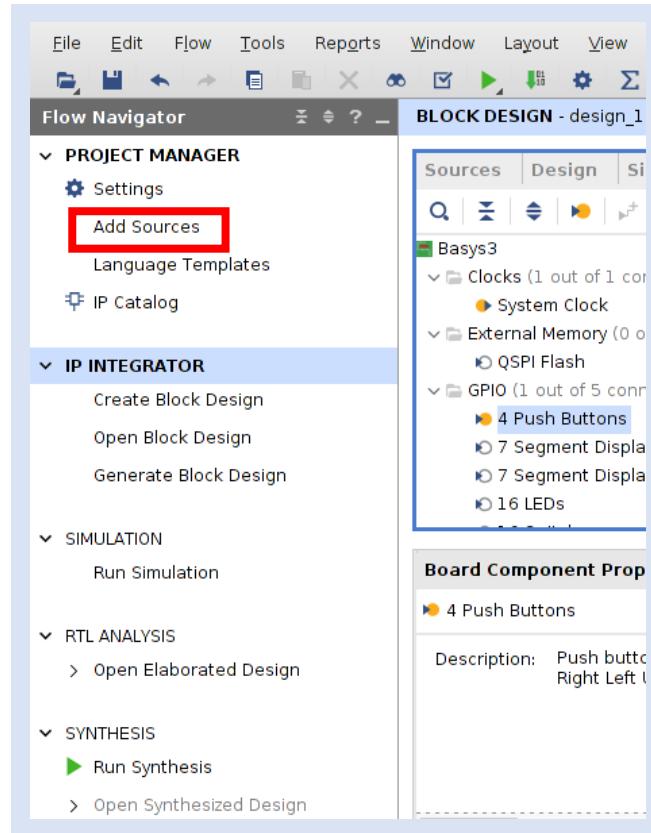
Crowd Supply: Lab One

Step 20 – This will clone three files: one RTL (.vhd) file, a constraints (.xdc) file, and an HLS IP core.



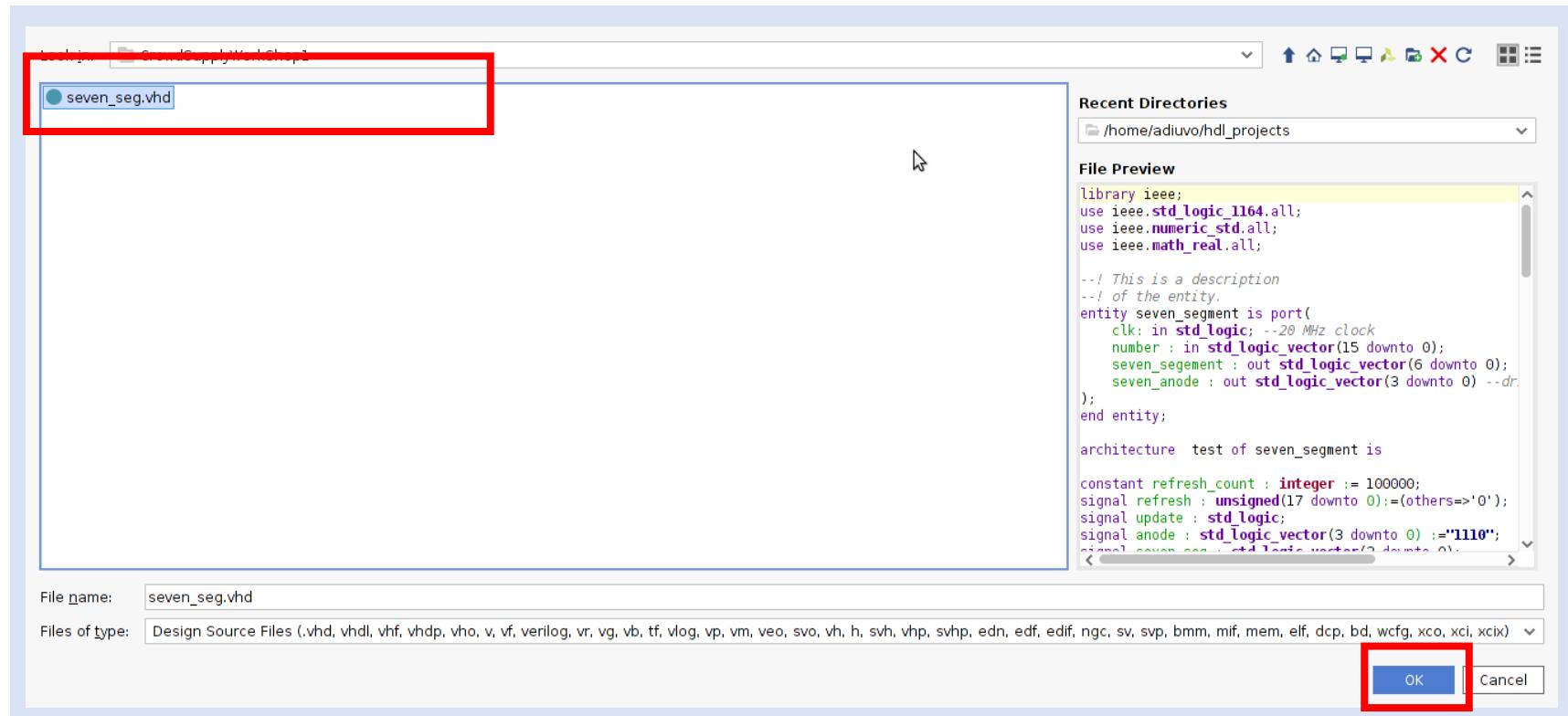
Crowd Supply: Lab One

Step 21 – C Under the Flow Navigator > Project Manager tab in Vivado, select “Add Sources”. In the next window, select “Add or create design sources” and click “Next”.



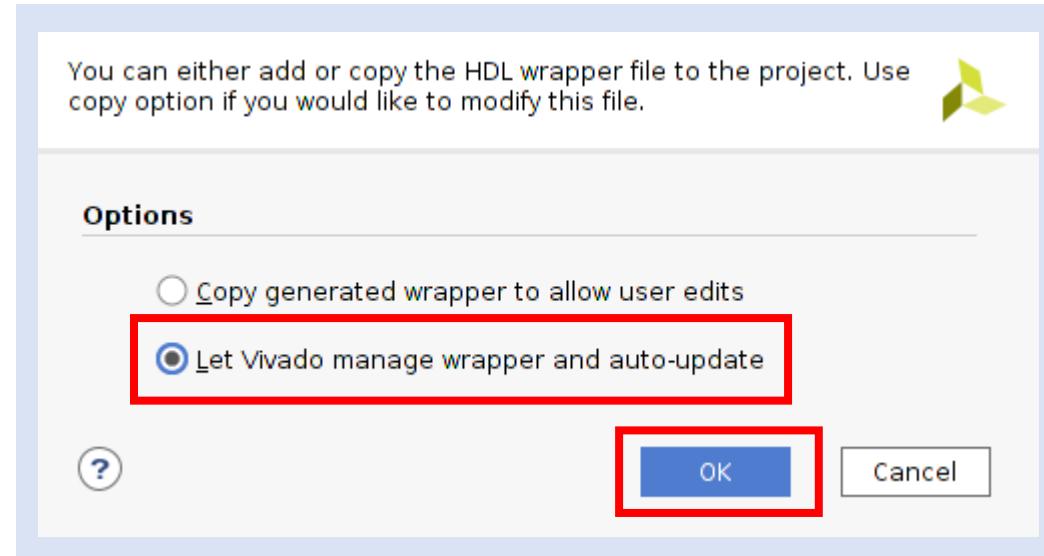
Crowd Supply: Lab One

Step 22 – In the location where you have saved the files from GitHub, select seven_seg.vhd and select “OK” to add the source.



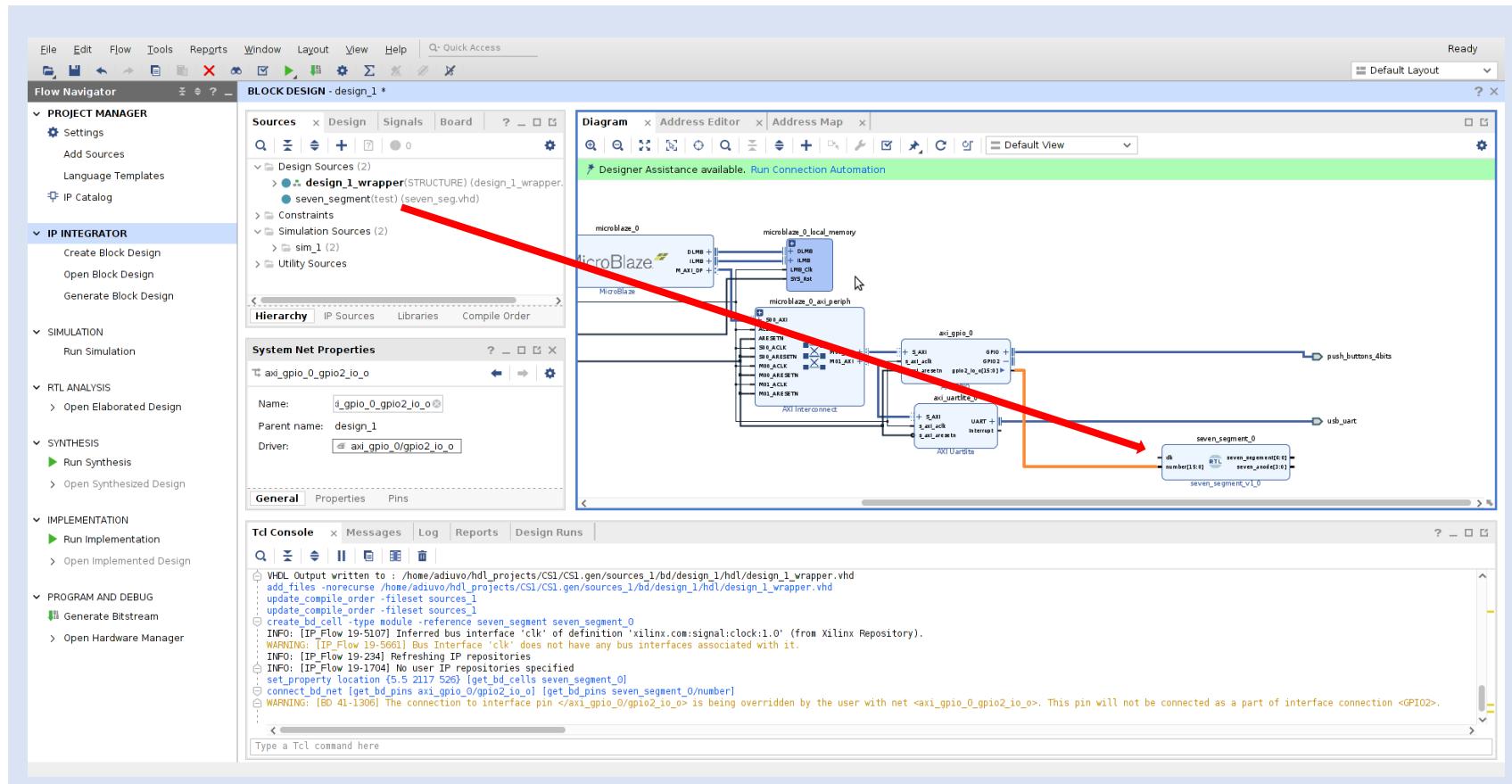
Crowd Supply: Lab One

Step 23 – Under the Sources tab in Vivado, right-click your block design (e.g., design_1.bd) and select “Create HDL Wrapper”. Select “Let Vivado manage wrapper and auto-update” in next window. Click “OK”. This will create [name of design]_wrapper.hdl under the Sources tab.



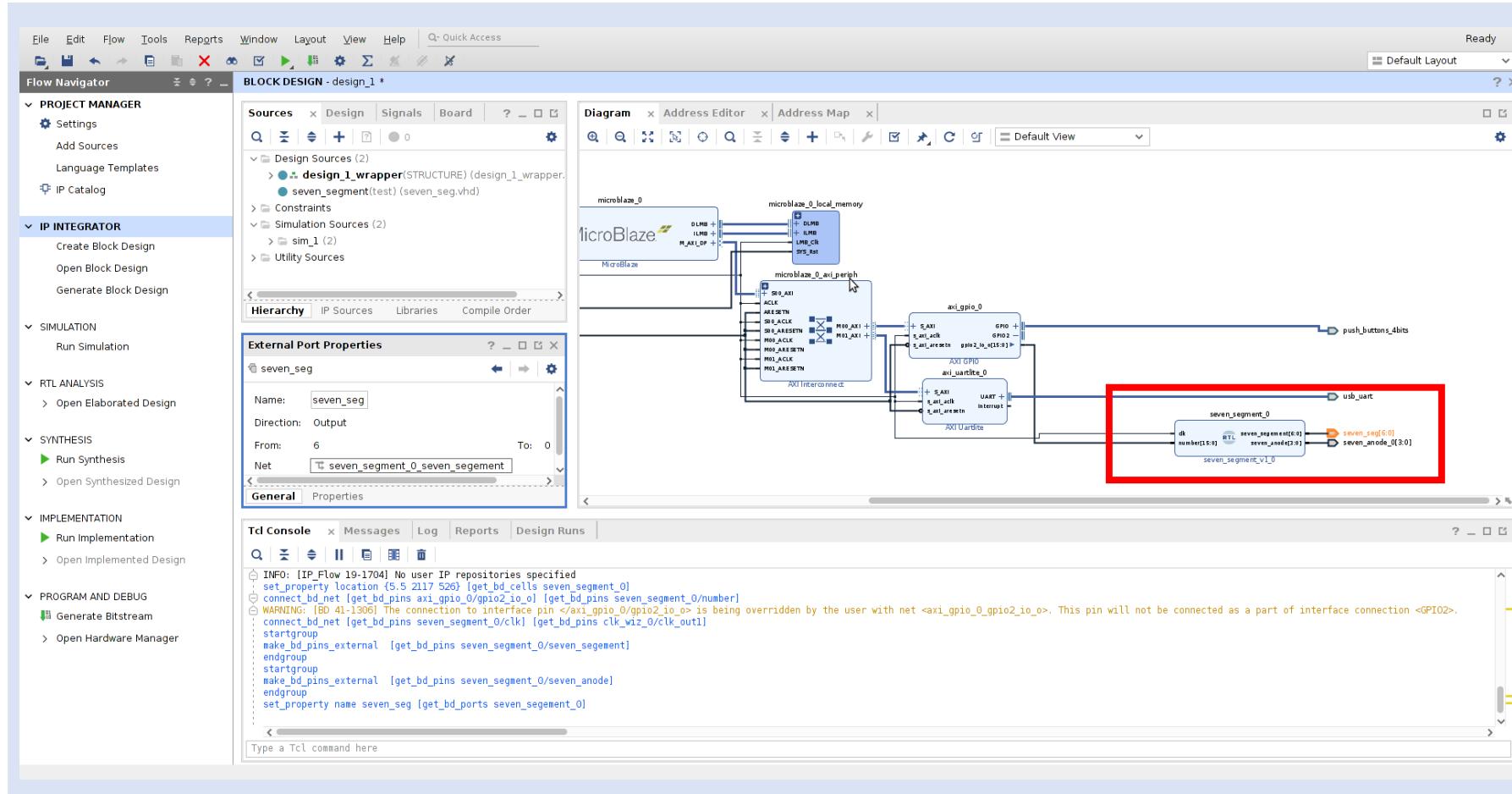
Crowd Supply: Lab One

Step 24 – From the Design Sources dropdown under Sources, drag the seven_segment RTL block onto the block diagram. Connect the second output port from the GPIO IP to the input of the seven_segment input as below. (You may have to expand “GPIO2” with “+” on the GPIO IP block to display the output port.)



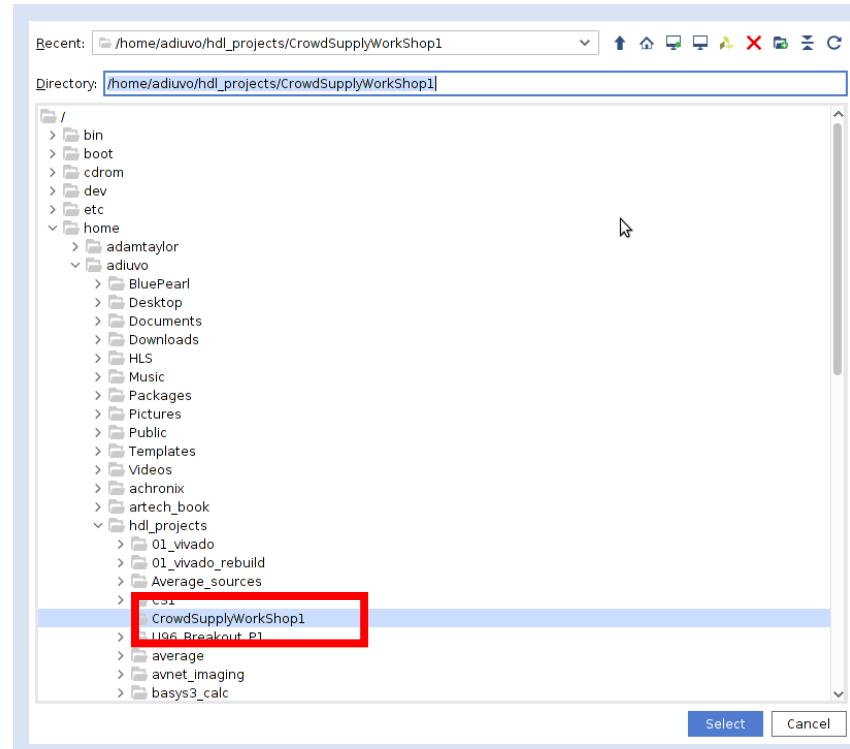
Crowd Supply: Lab One

Step 25 – Connect clk on the seven_segment block to clk_1 (20 MHZ) of the clock wizard. Make the two ports (seven_segment and seven_anode) external by right-clicking each port and selecting “Make External”. Name them seven_seg & seven_seg_led_an respectively.



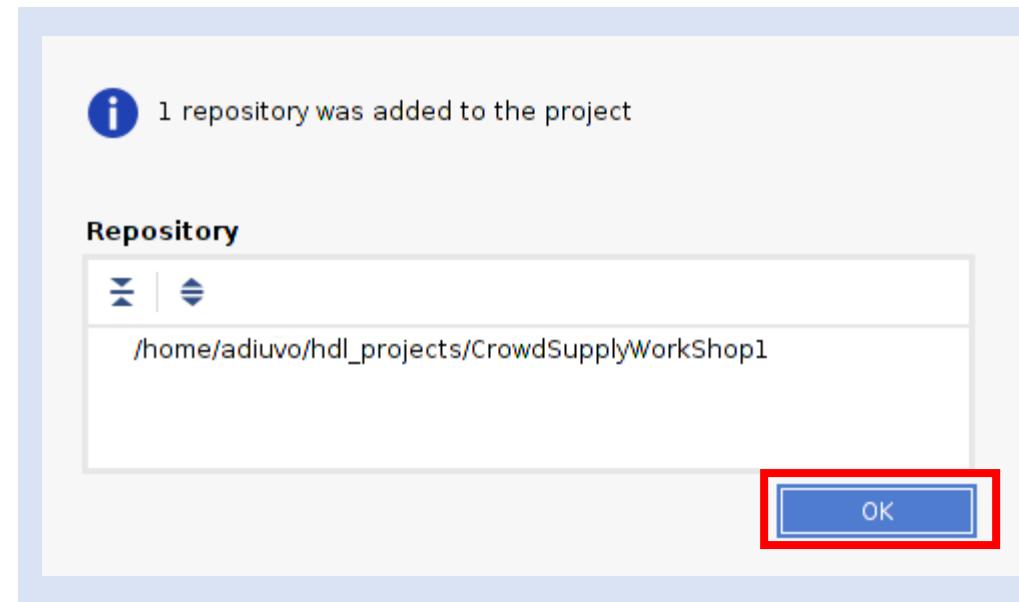
Crowd Supply: Lab One

Step 26 – Add a new repository to the IP library by navigating as follows: Project Manager > Settings > Project Settings > IP > repository > “+”. Select the cloned repository as your directory.



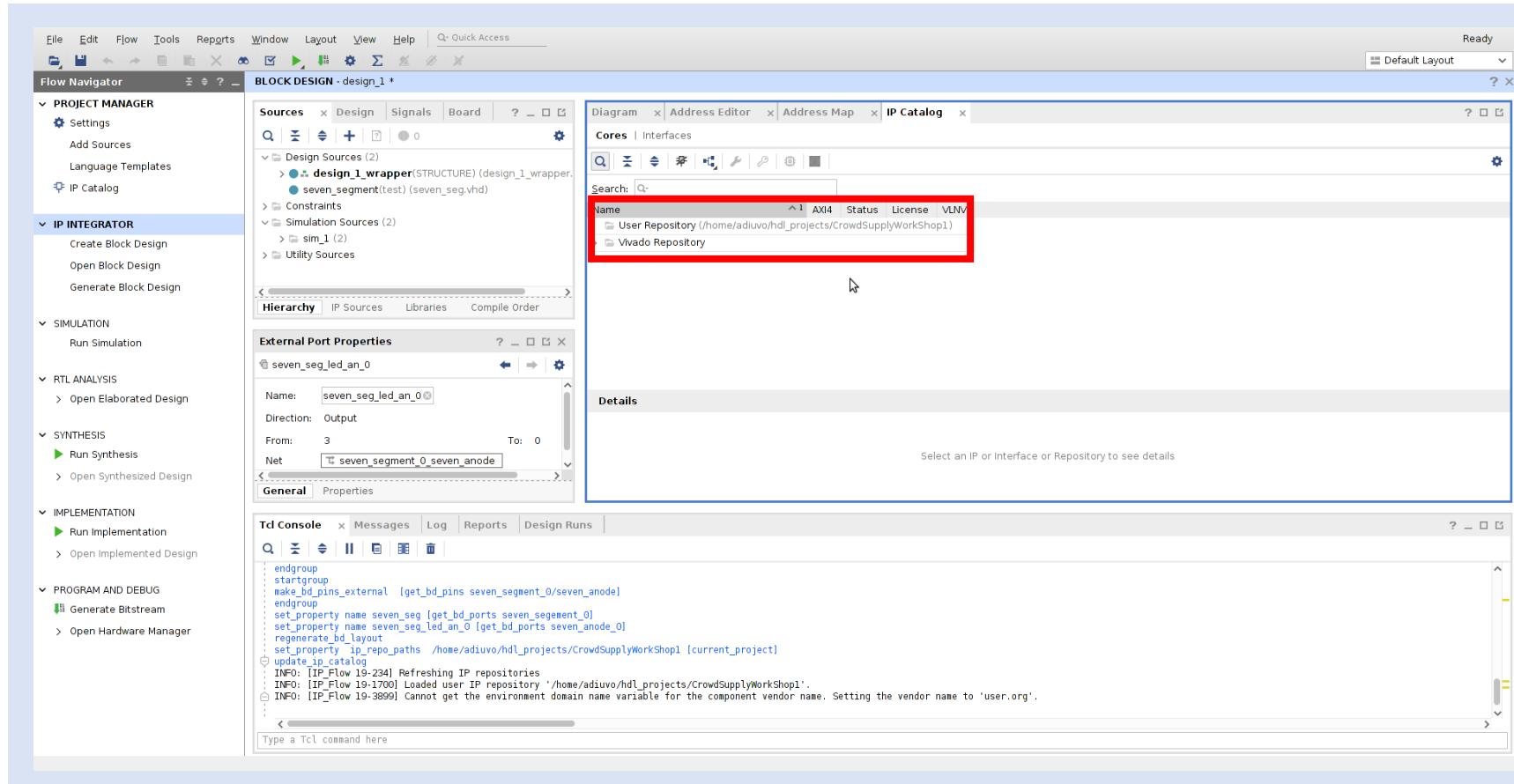
Crowd Supply: Lab One

Step 27 – This will add one repository to the project as shown by the dialogue below. Click “OK” to exit this window, and then again to exit the settings window.



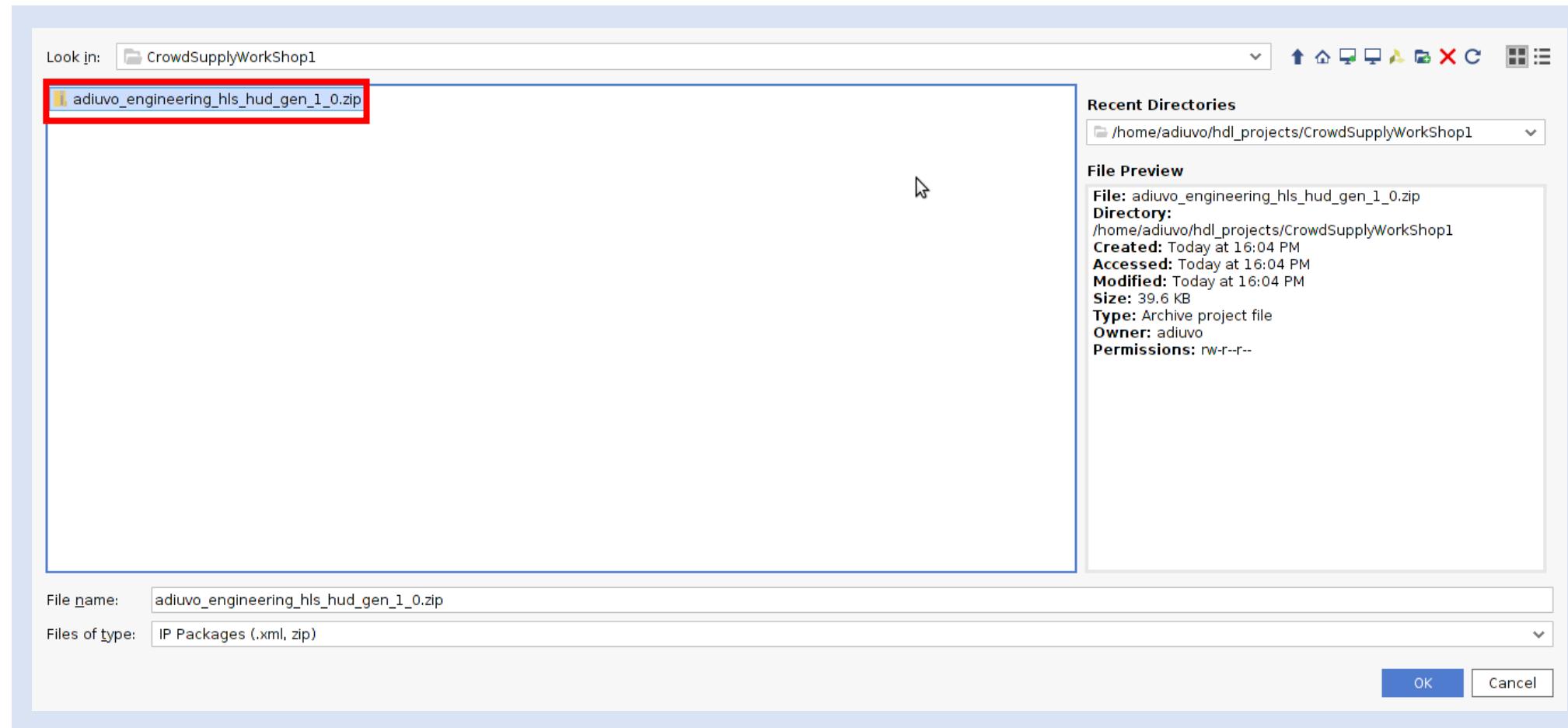
Crowd Supply: Lab One

Step 28 – Under the newly opened IP Catalog tab, right-click on the User Repository (which was just added) and select “Add IP to Repository”.



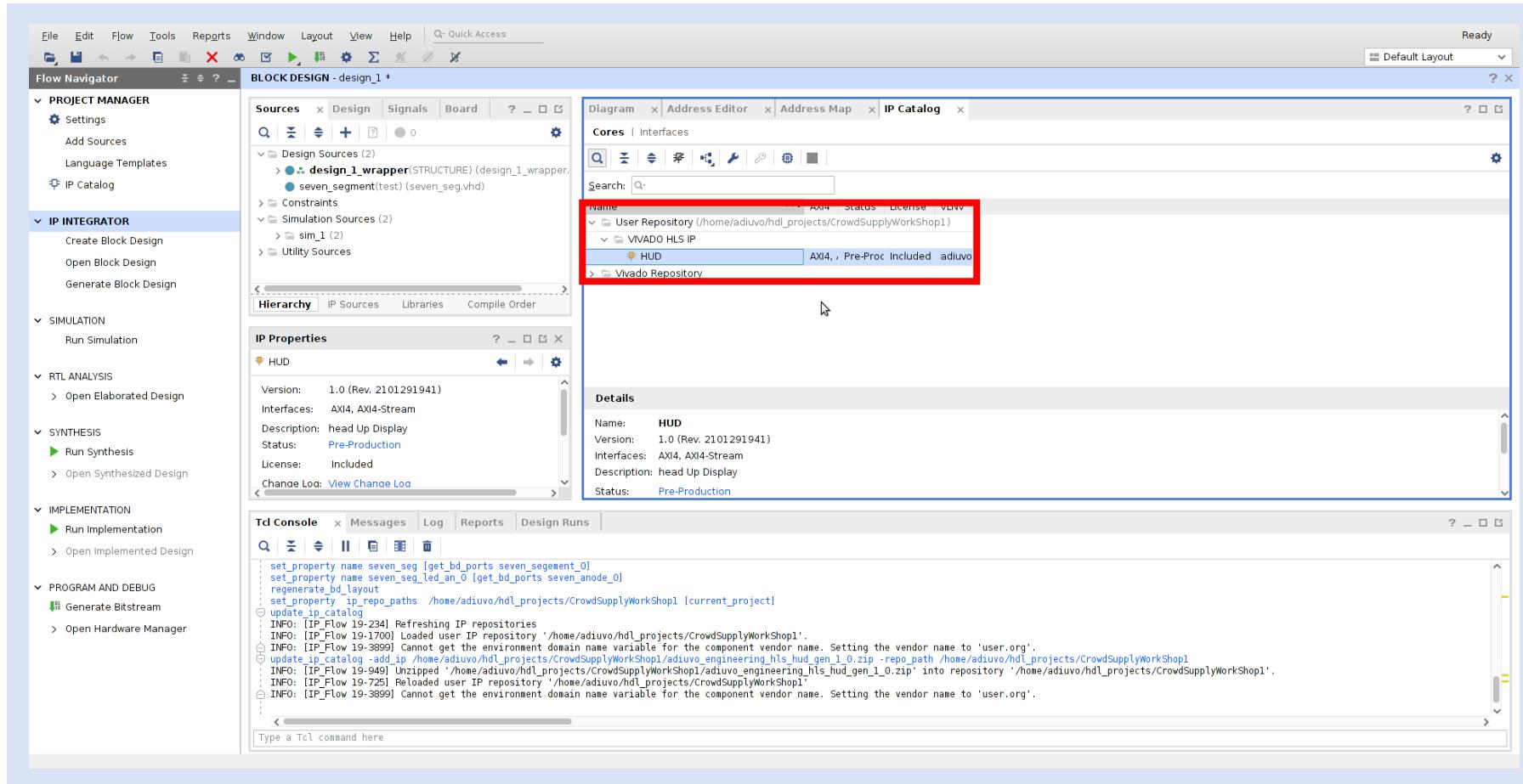
Crowd Supply: Lab One

Step 29 – In the new window, select the .zip in the cloned directory. Click “OK”.



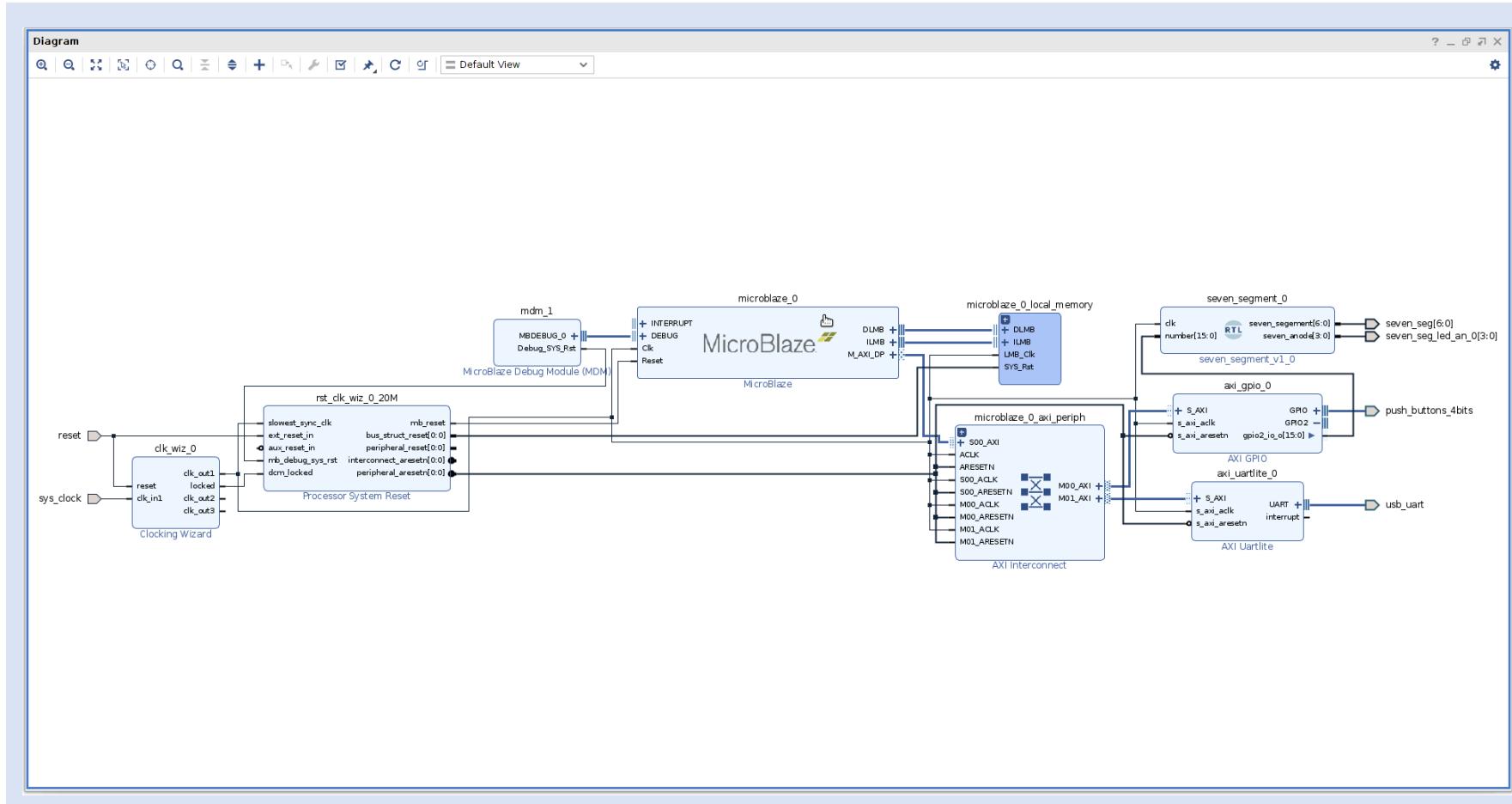
Crowd Supply: Lab One

Step 30 – Under the User Repository dropdown, you should now see the HUD IP block.



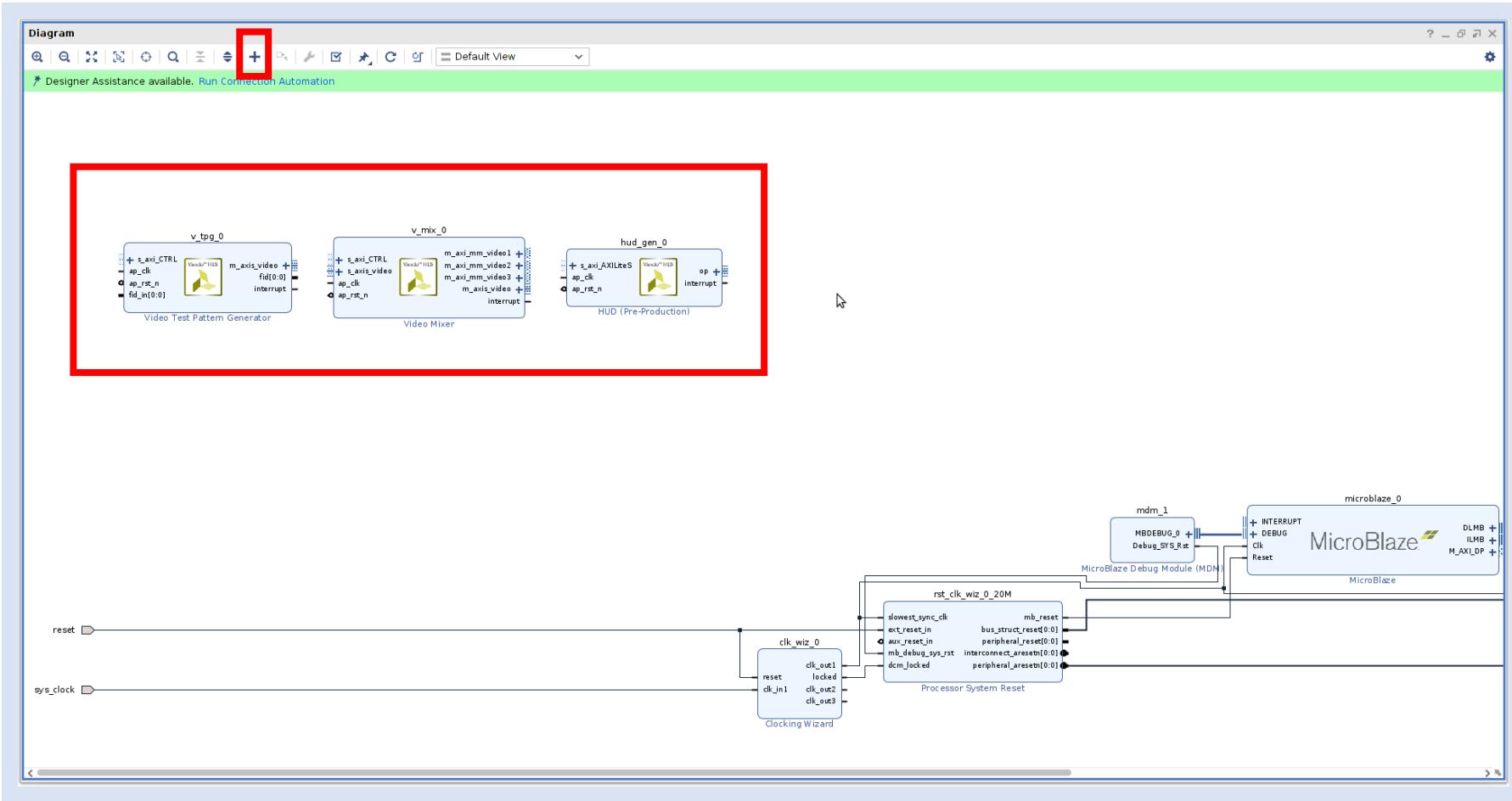
Crowd Supply: Lab One

Step 31 – Float the block diagram by clicking the right-most icon in the top left corner of the diagram tab and maximize the window.



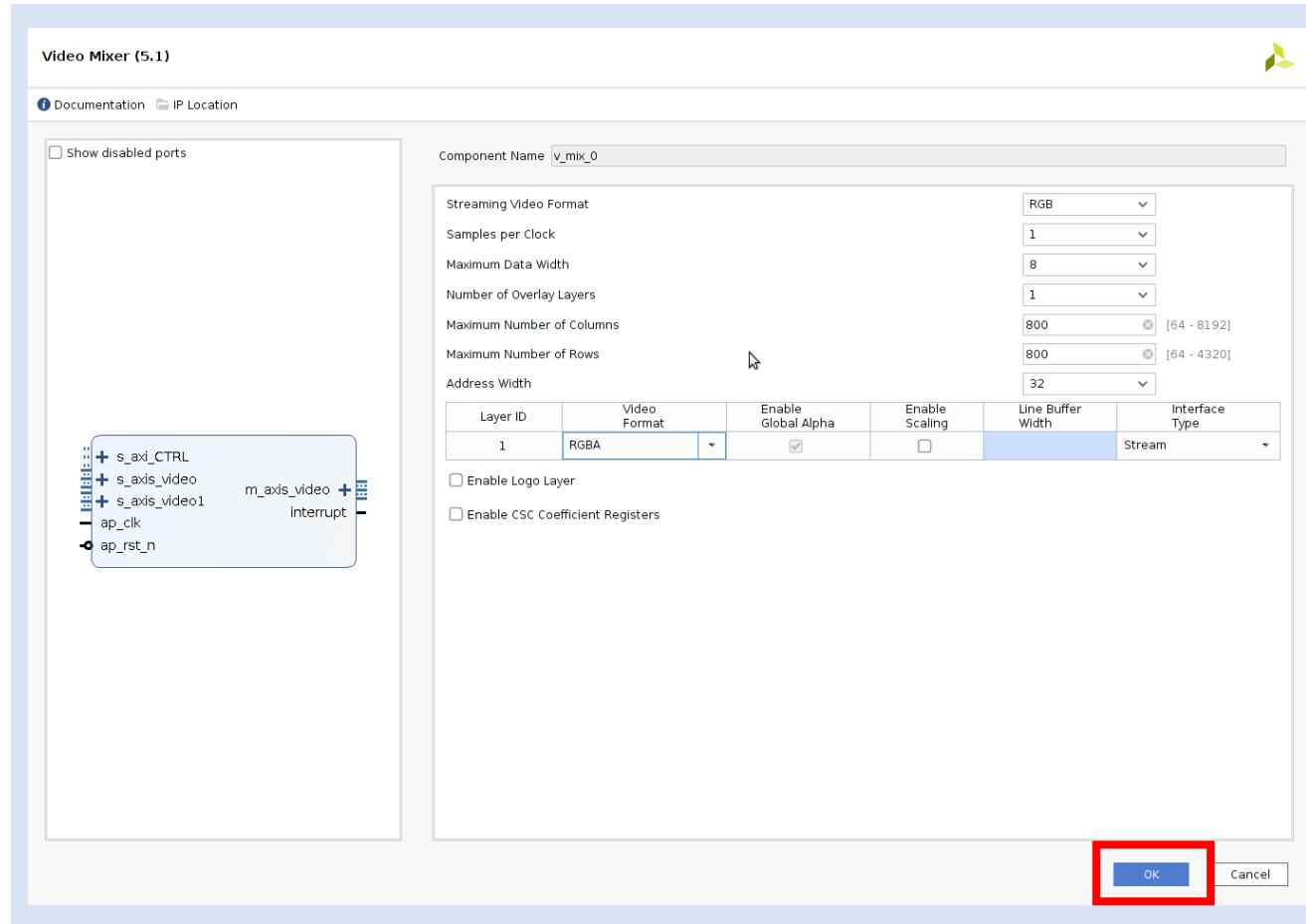
Crowd Supply: Lab One

Step 32 – Add the following IP to the diagram: “Video Test Pattern Generator”, “Video Mixer”, and “HUD”.



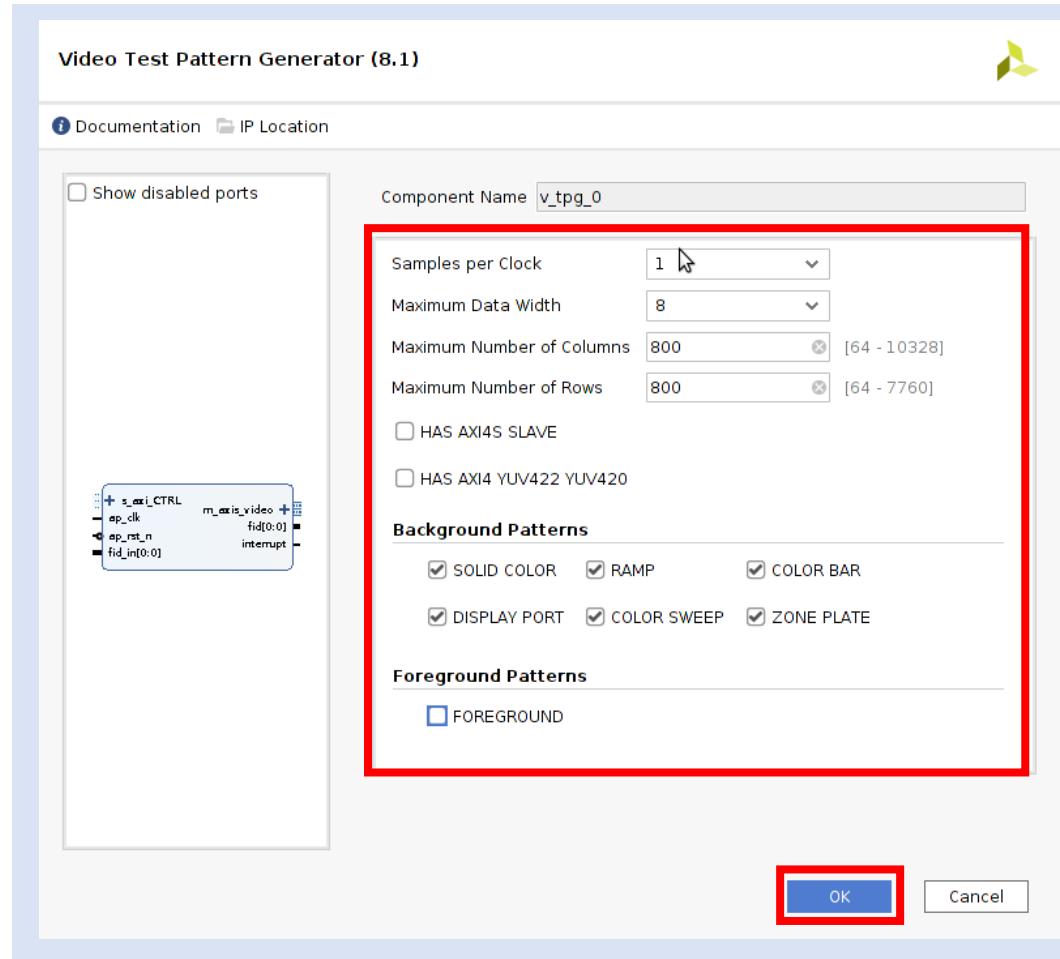
Crowd Supply: Lab One

Step 33 – Double click on the Video Mixer block and configure it as below



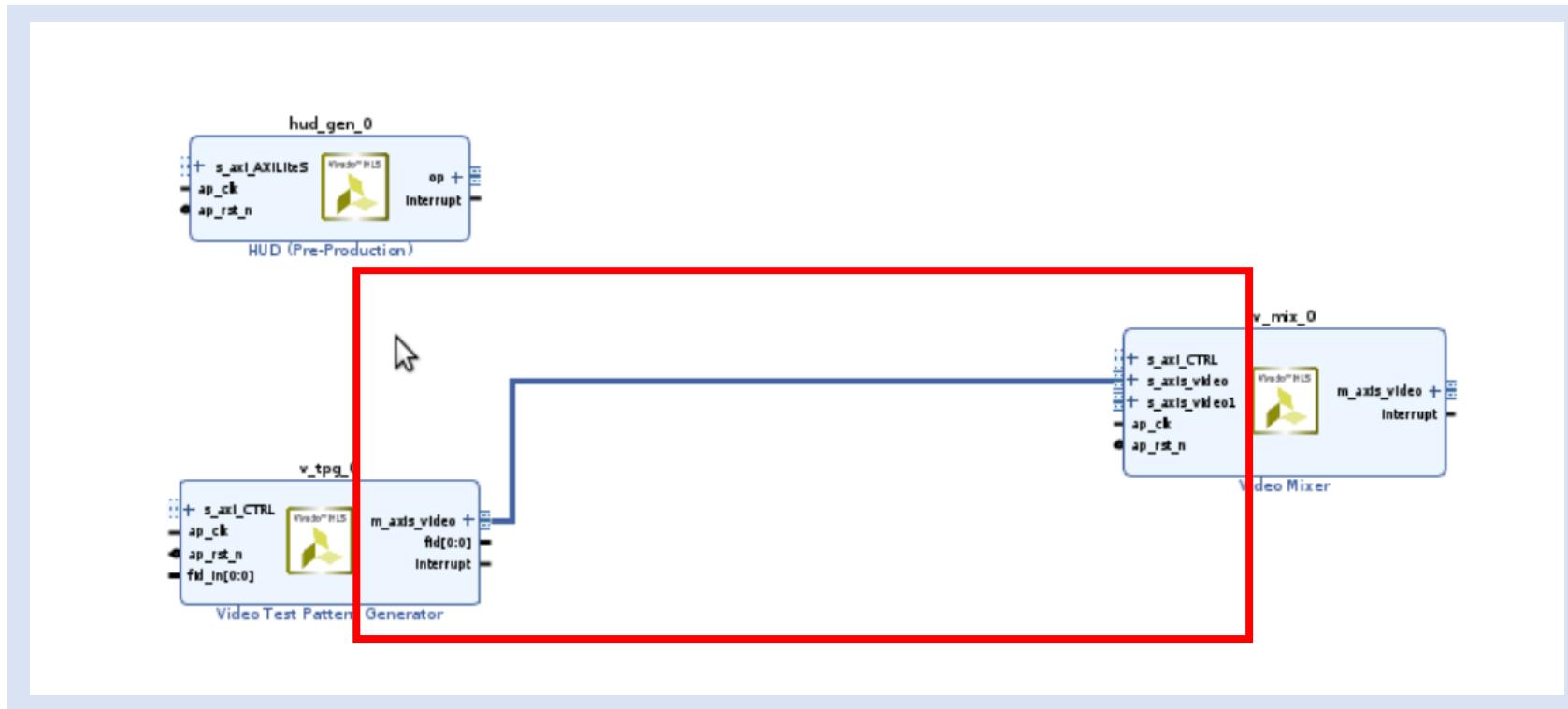
Crowd Supply: Lab One

Step 34 – Double click on the Test Pattern Generator block and configure it as below



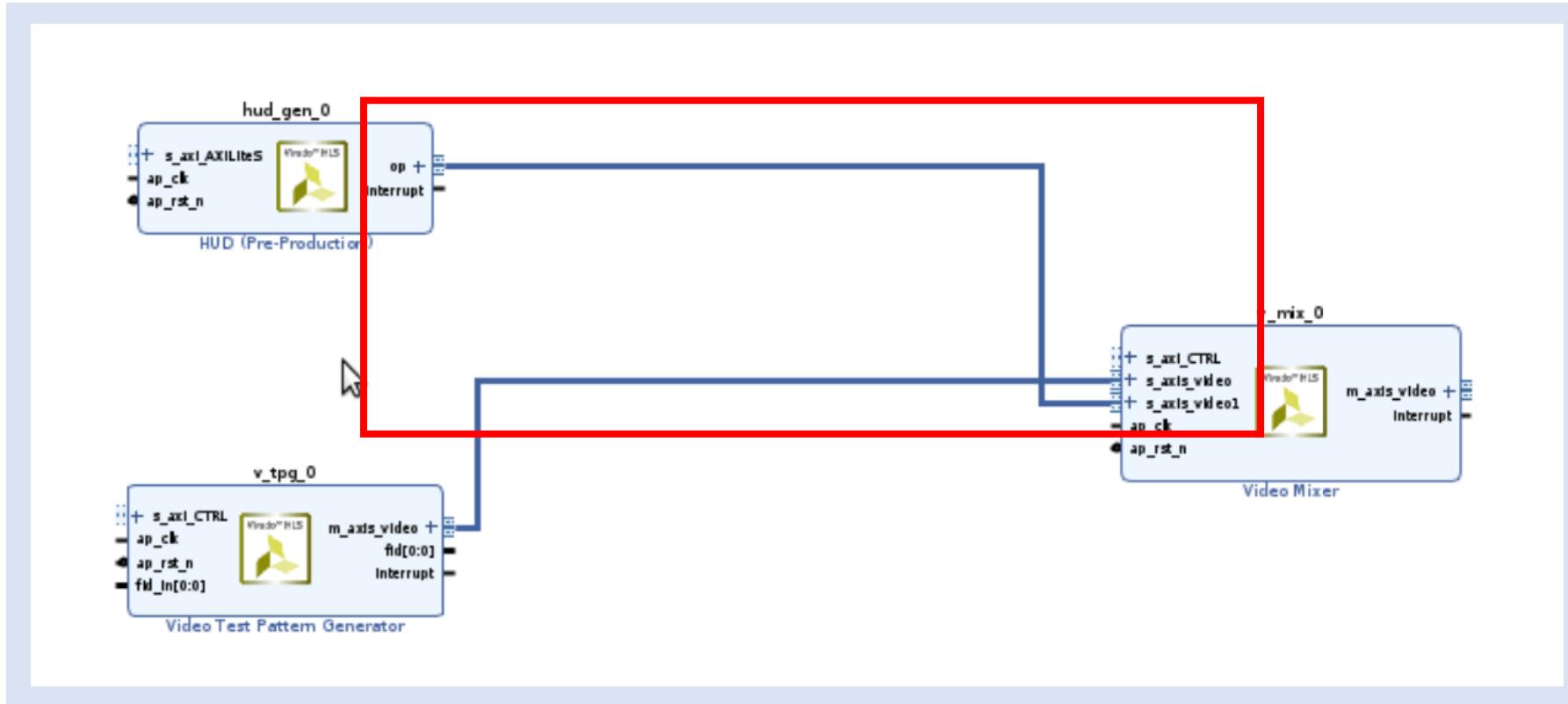
Crowd Supply: Lab One

Step 35 – Connect the Test Pattern Generator block to the Video Mixer block as shown below.



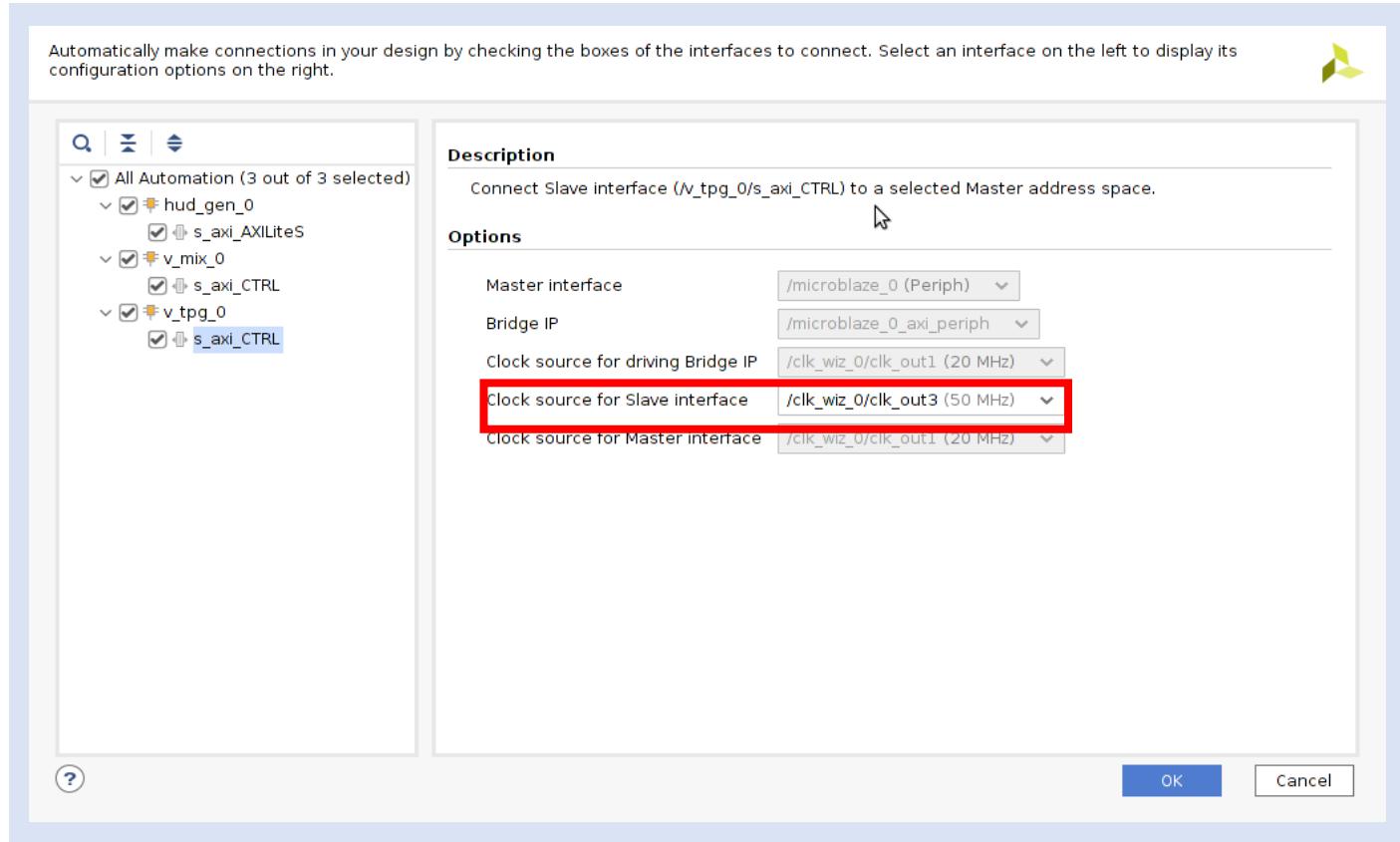
Crowd Supply: Lab One

Step 36 – Connect the HUD IP to the Video Mixer block as shown below.



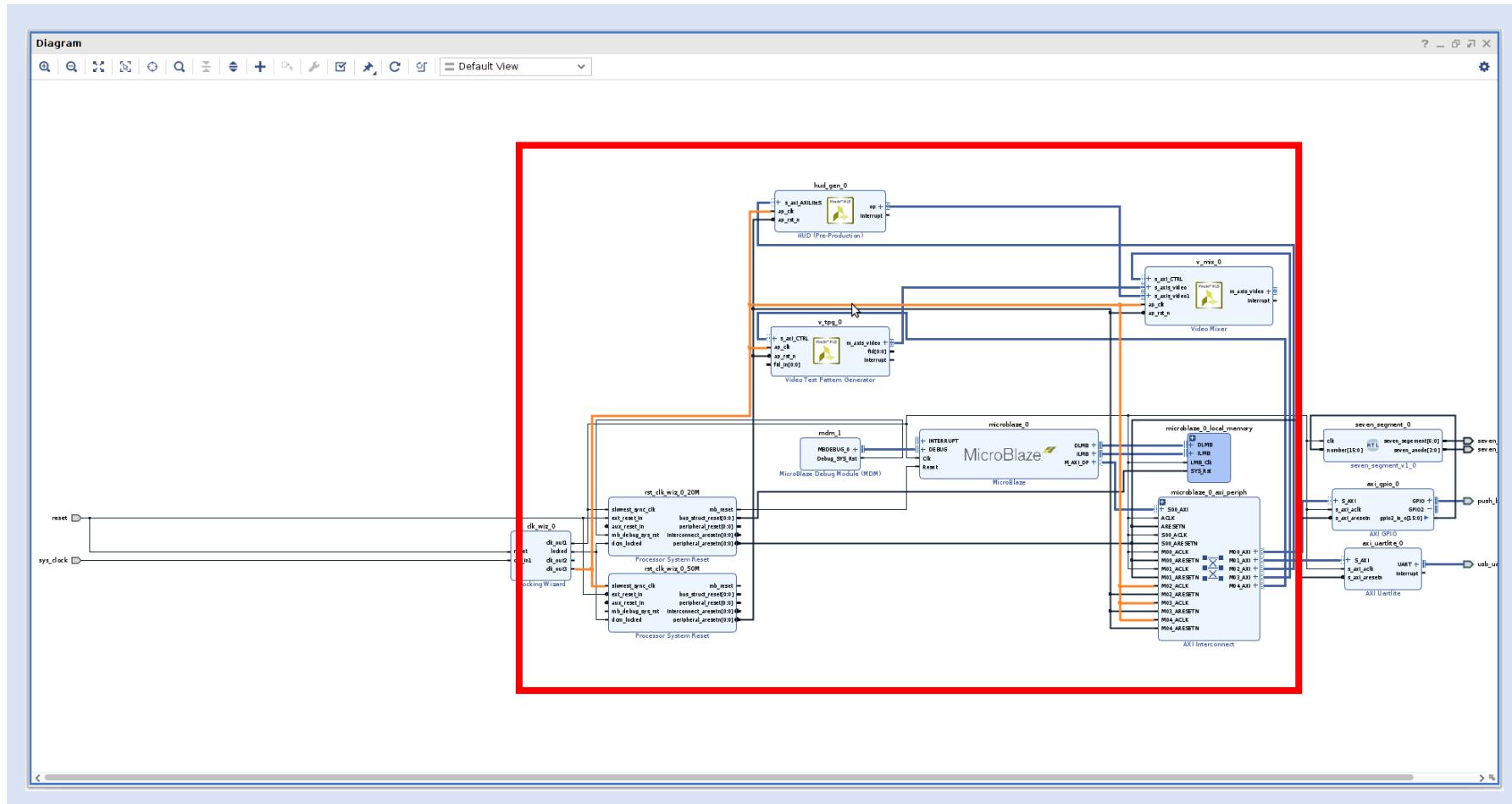
Crowd Supply: Lab One

Step 37 – Run the connection automation and for all three modules. Before clicking “OK”, set clock source for all s_axi interfaces to clk_out3 (50 MHz).



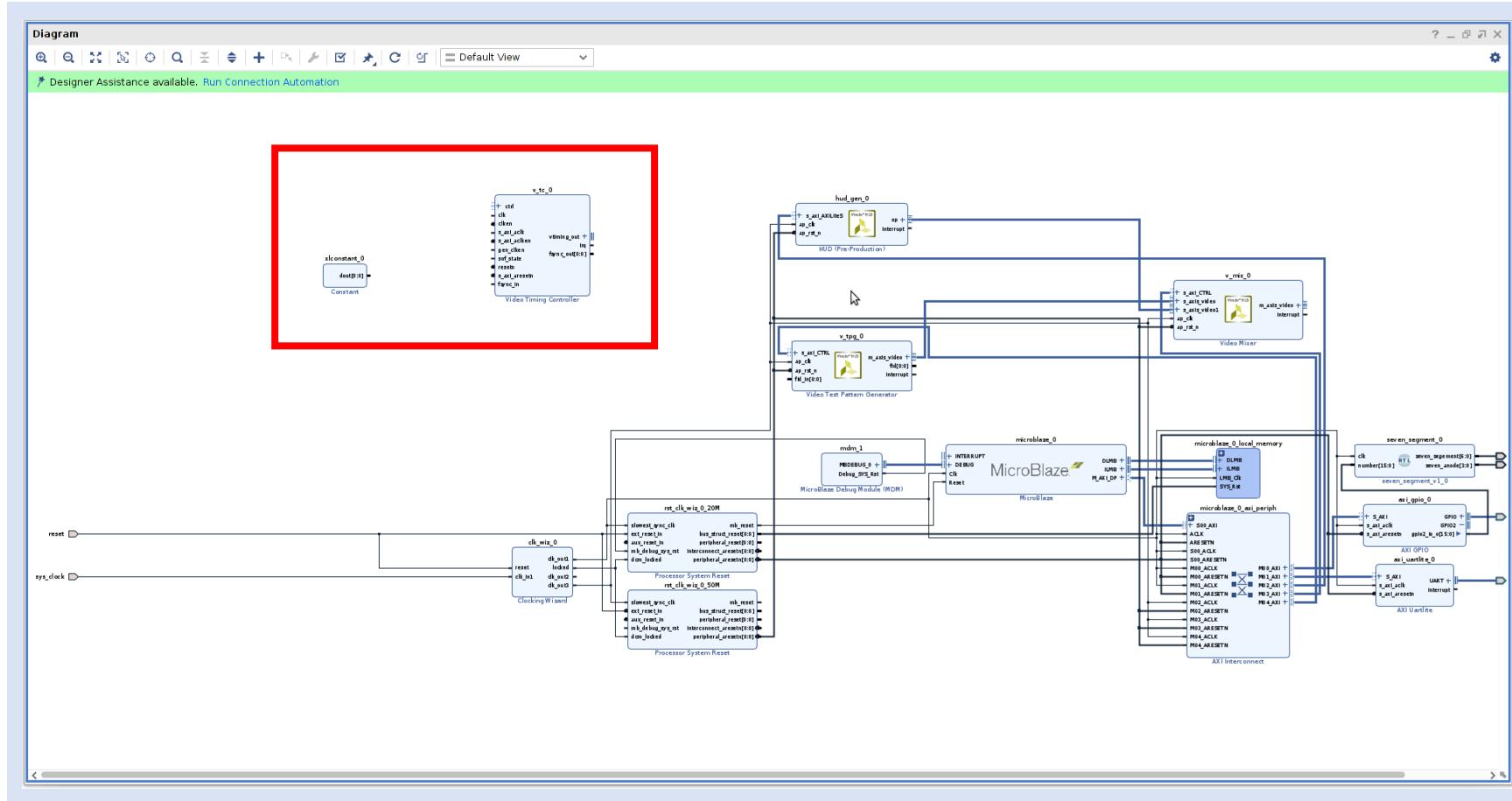
Crowd Supply: Lab One

Step 38 – Check that the clocks for the HUD, Video TPG, and Video Mixer IP are connected to the 50 MHz clock network (clk_out3).



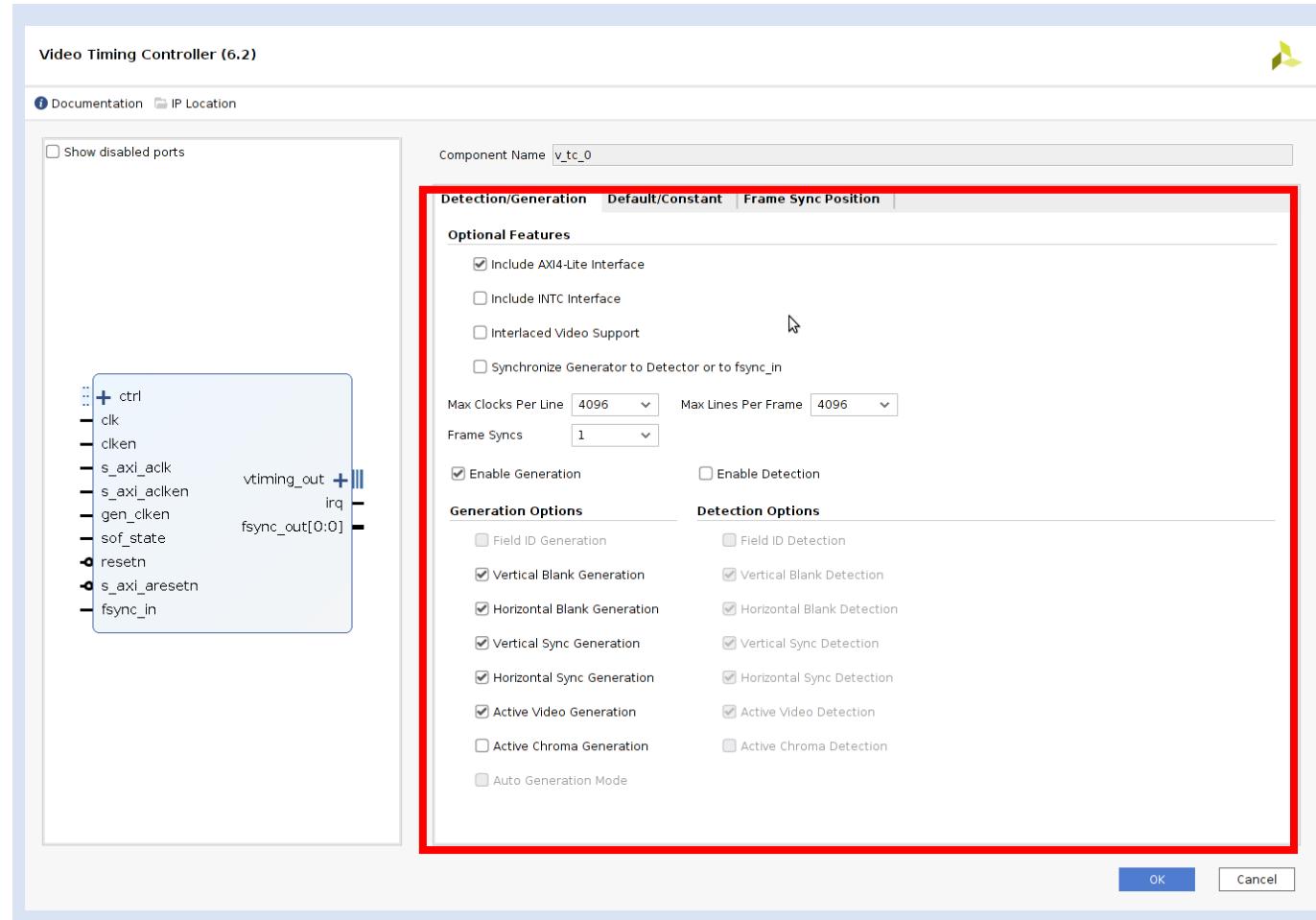
Crowd Supply: Lab One

Step 39 – Add the following blocks to the diagram: “Video Timing Controller” and “Constant”



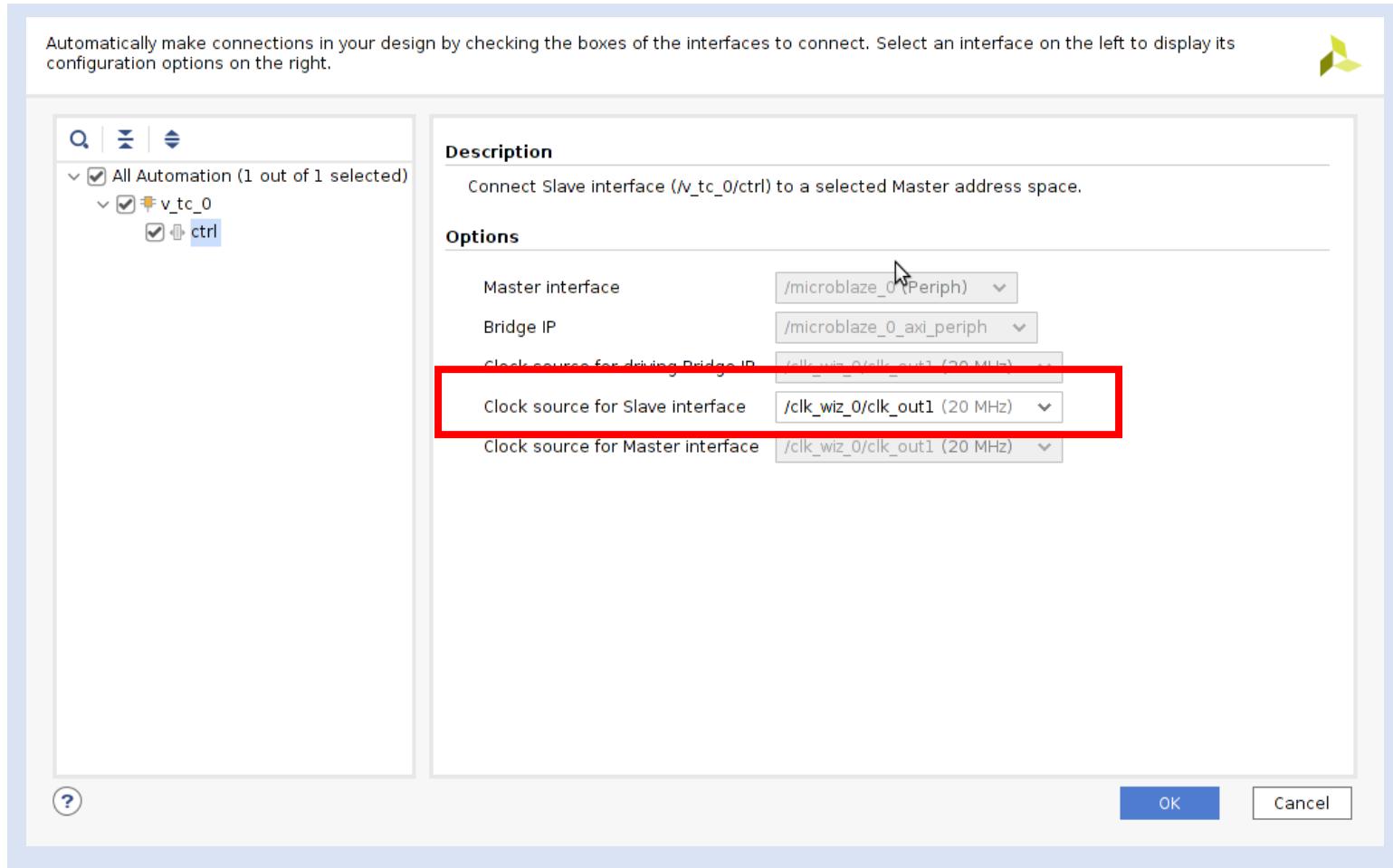
Crowd Supply: Lab One

Step 40 – Double-click the Video Timing Controller on it to recustomize as shown below.



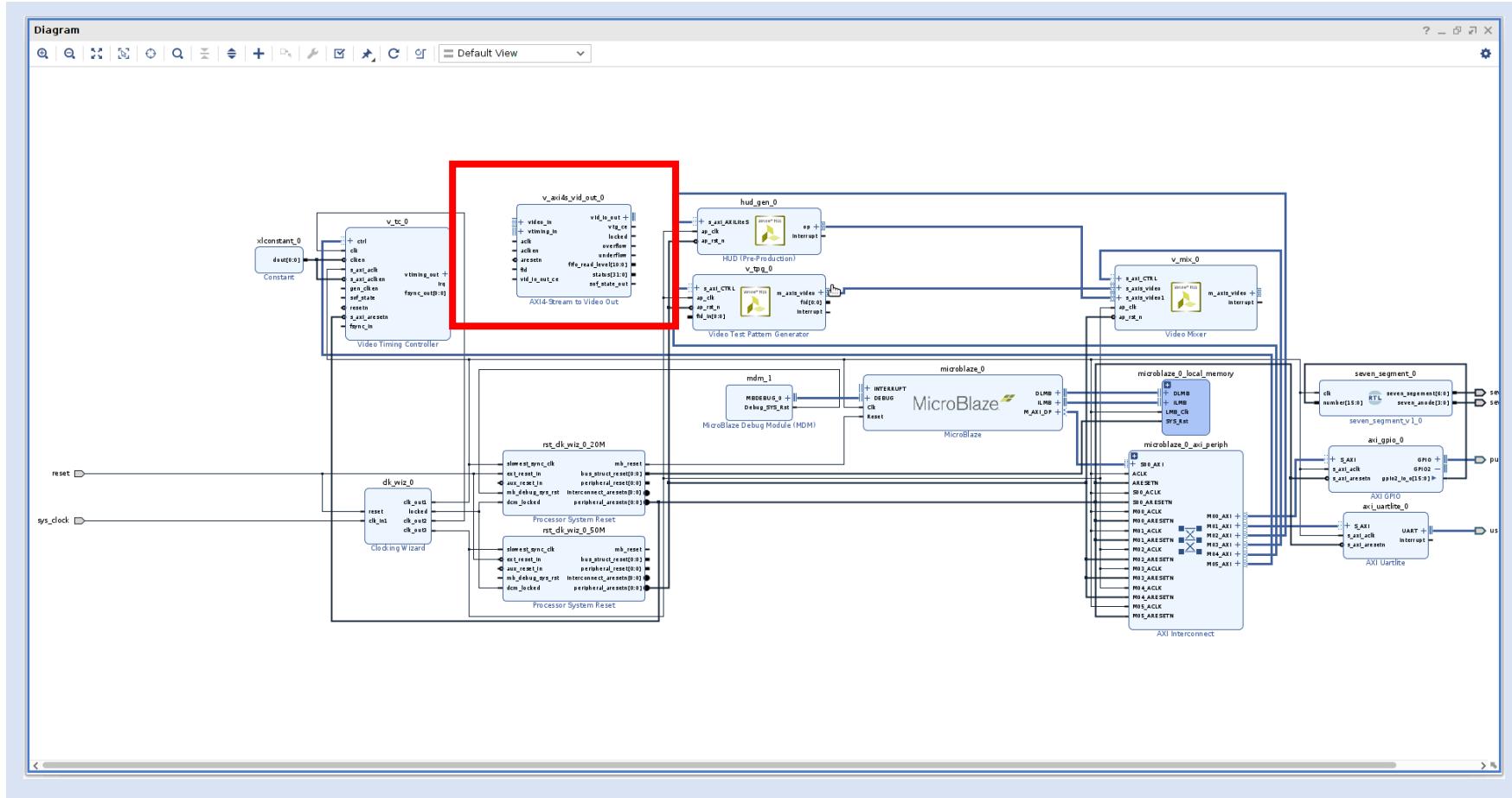
Crowd Supply: Lab One

Step 41 – Run the connection automation to connect the VTC into the AXI Network. Before clicking “OK”, ensure “ctrl” is selected and the clock source for the interface is set to clk_out1 (20 MHz).



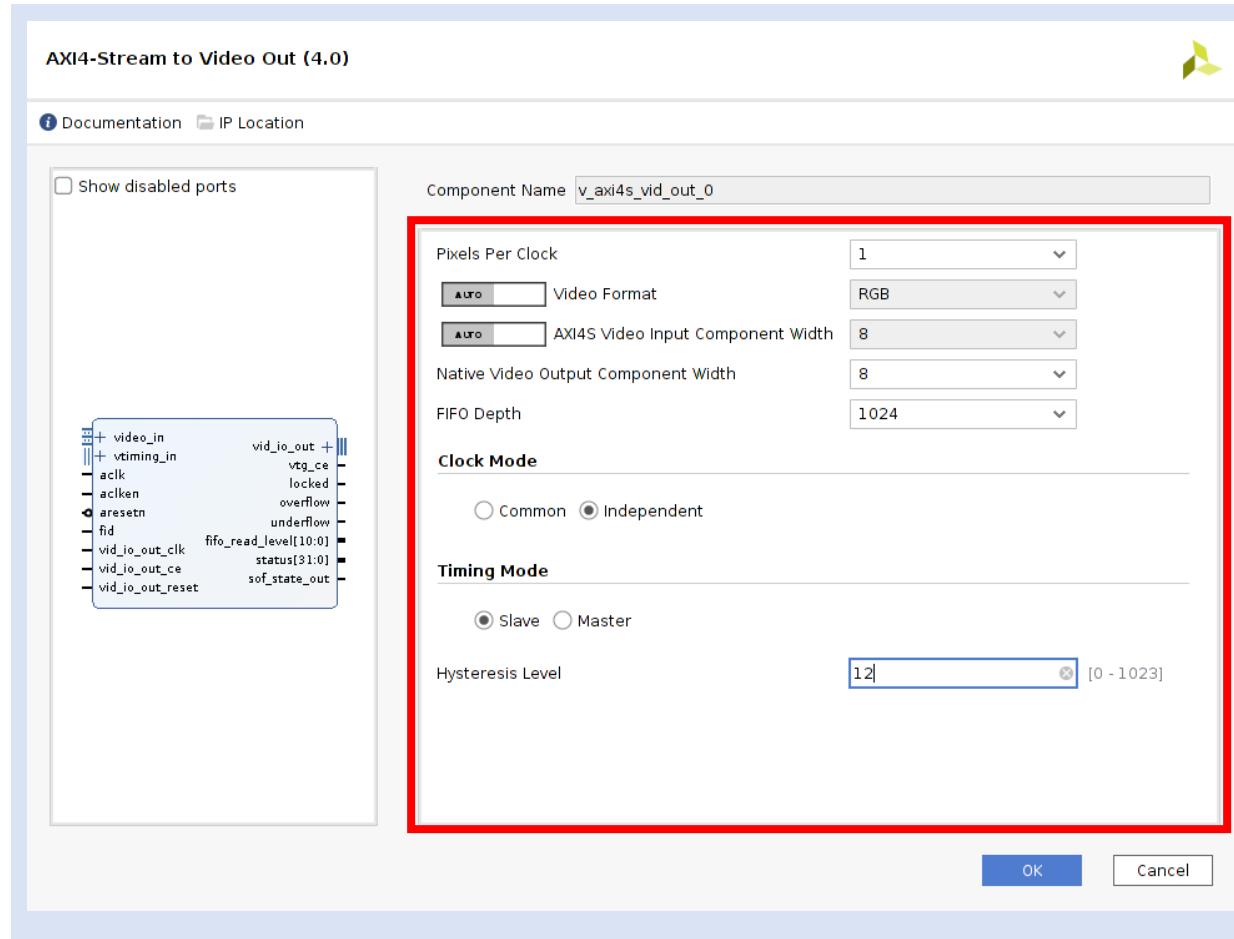
Crowd Supply: Lab One

Step 42 – Add a “AXI Stream to Video Out” IP block to the diagram.



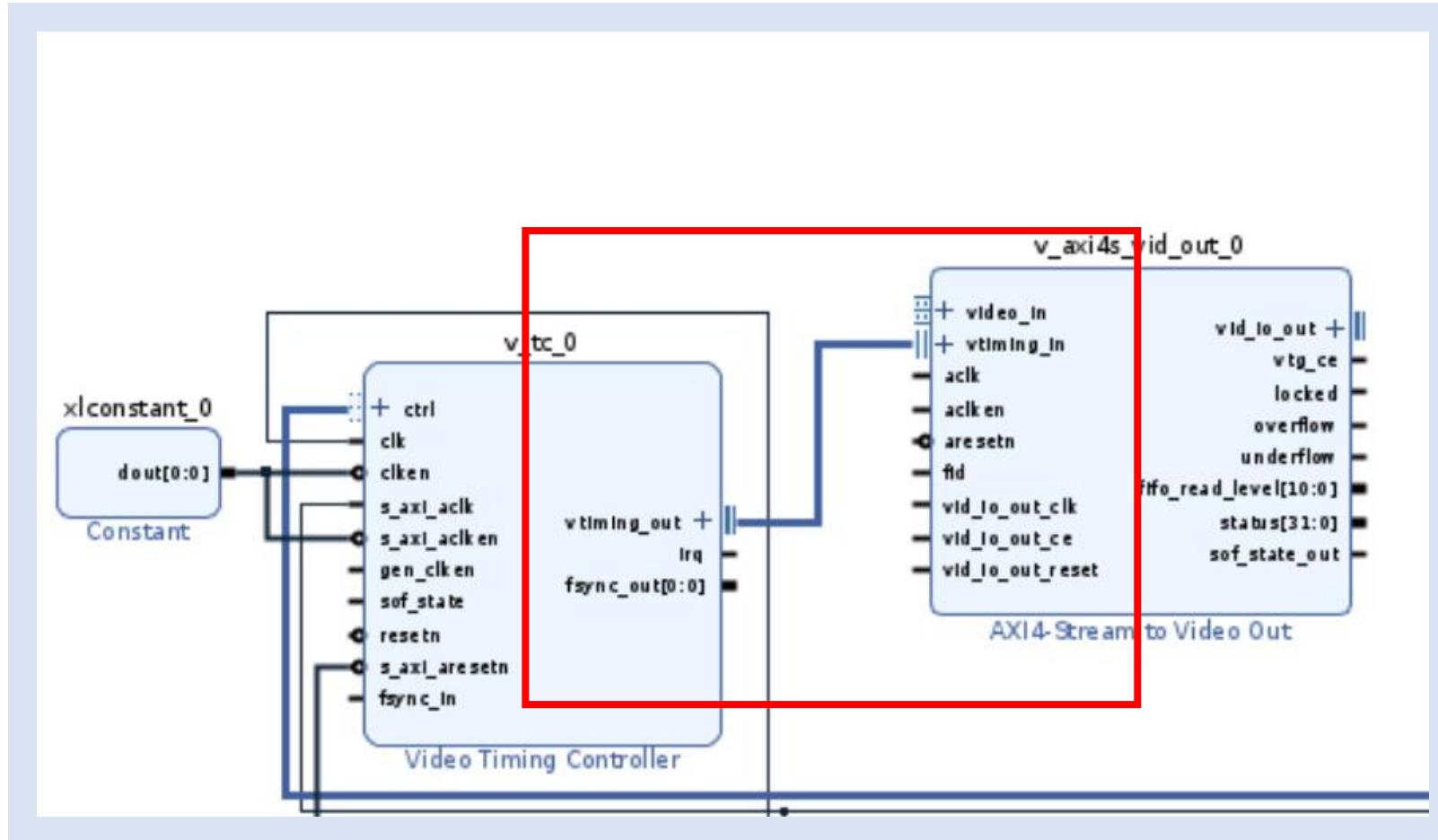
Crowd Supply: Lab One

Step 43 – Double-click the AXI4-Stream to Video Out block to recustomize as shown below.



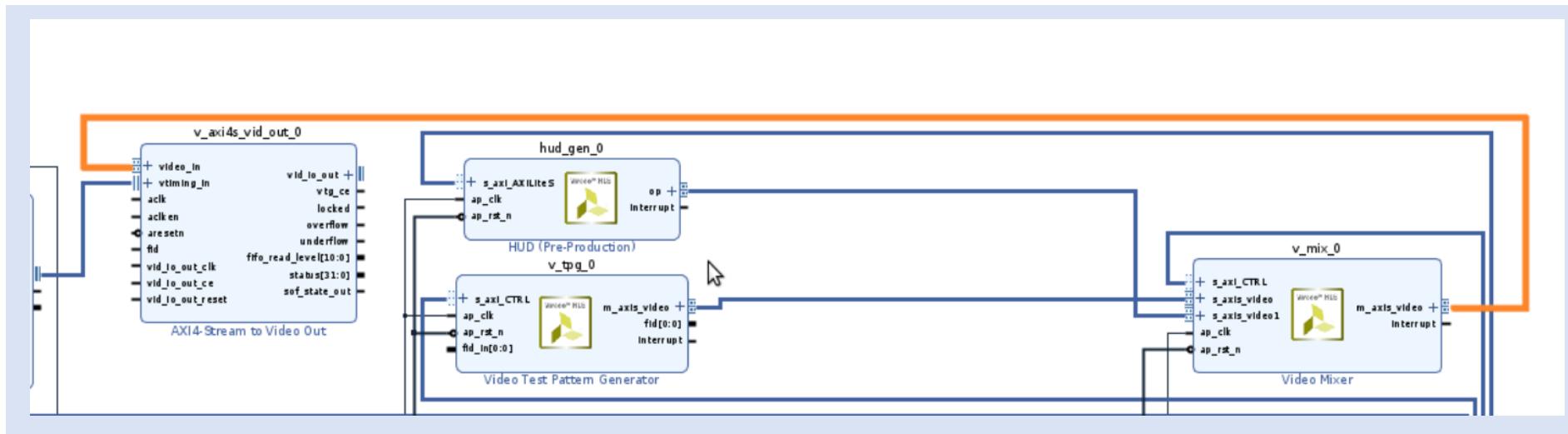
Crowd Supply: Lab One

Step 44 – Connect the vtiming_out port of the VTC to the vtiming_in port of the AXIS Vid Out IP as shown below.



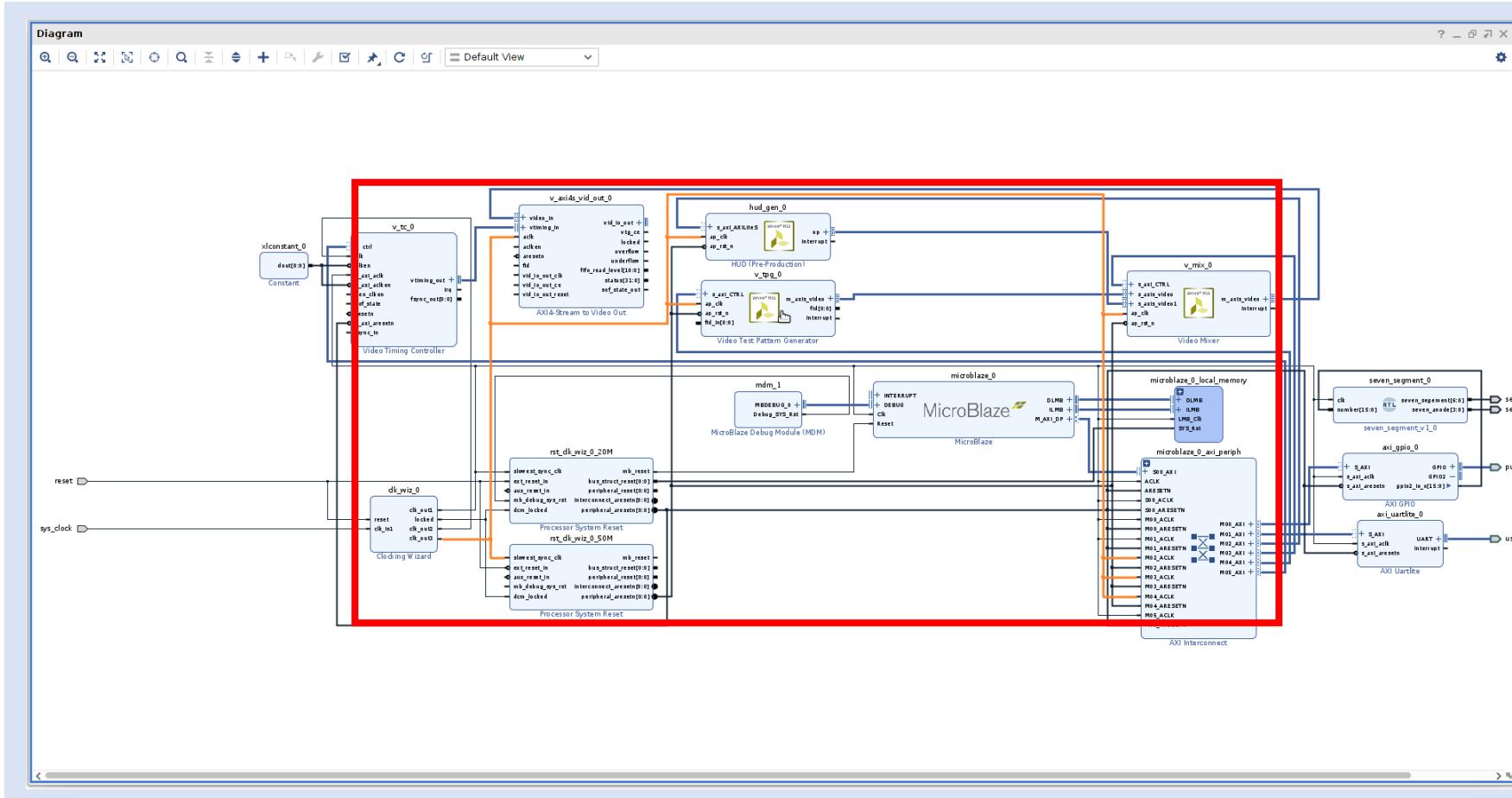
Crowd Supply: Lab One

Step 45 – Connect the output of the Video Mixer to the AXIS Vid Out input as shown below.



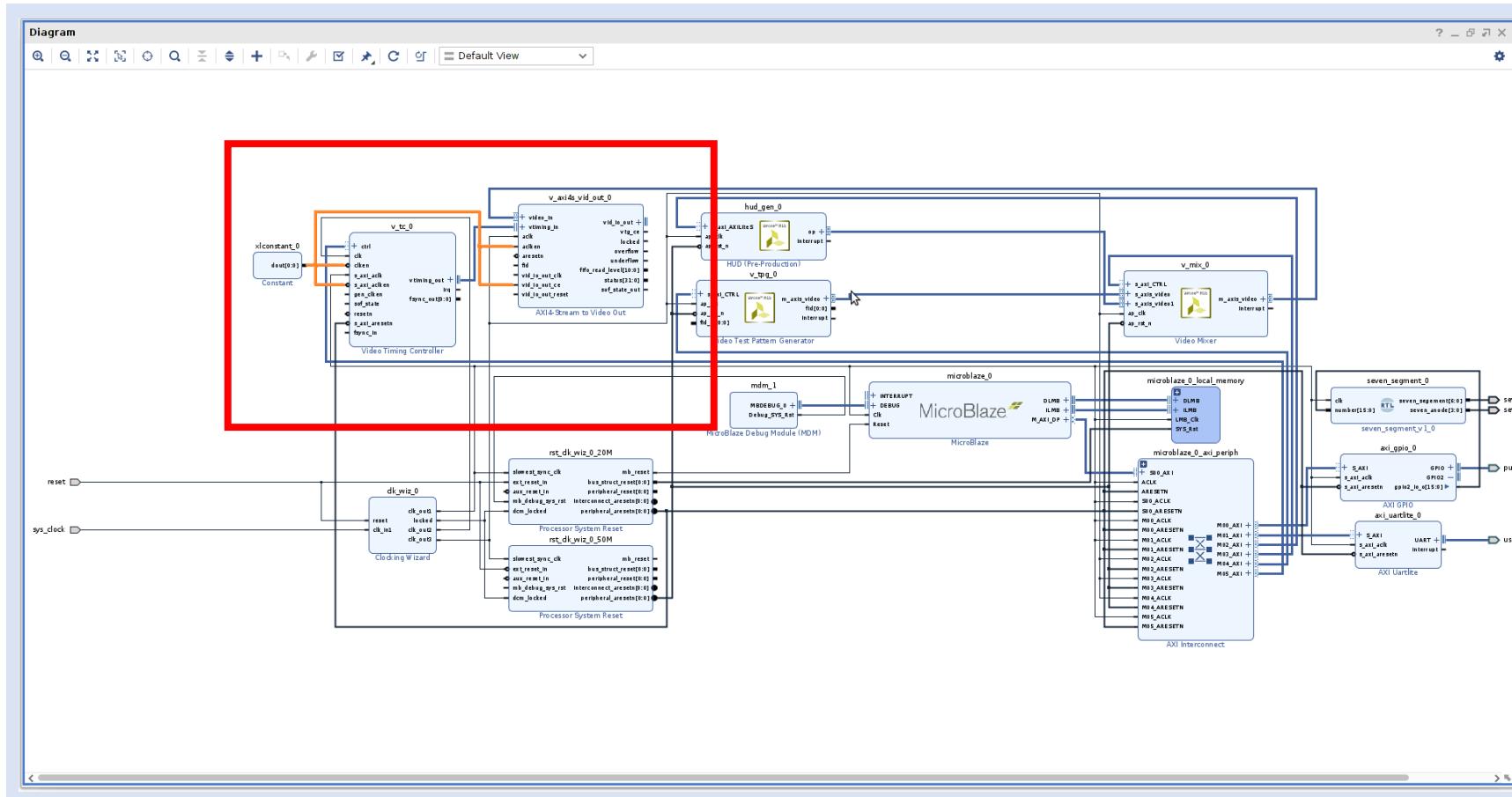
Crowd Supply: Lab One

Step 46 – Connect the aclk port of the AXIS Vid Out block to clk_out3 (50 MHz).



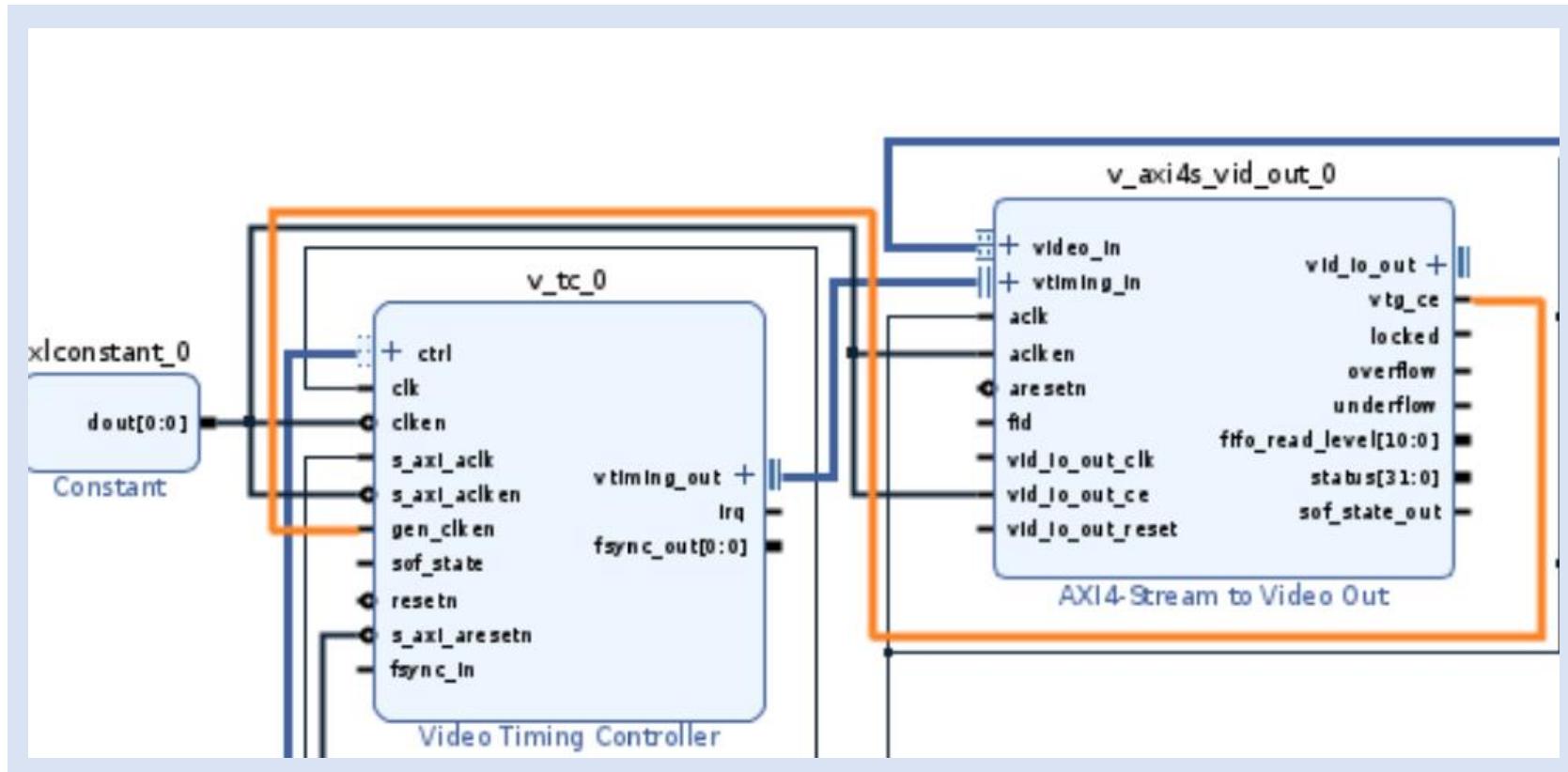
Crowd Supply: Lab One

Step 47 – Connect the Constant block to the 4 following ports as shown below: clk_en (VTC), s_axi_aclken (VTC), aclken (AXIS Vid Out), vid_io_out_ce (AXIS Vid Out)



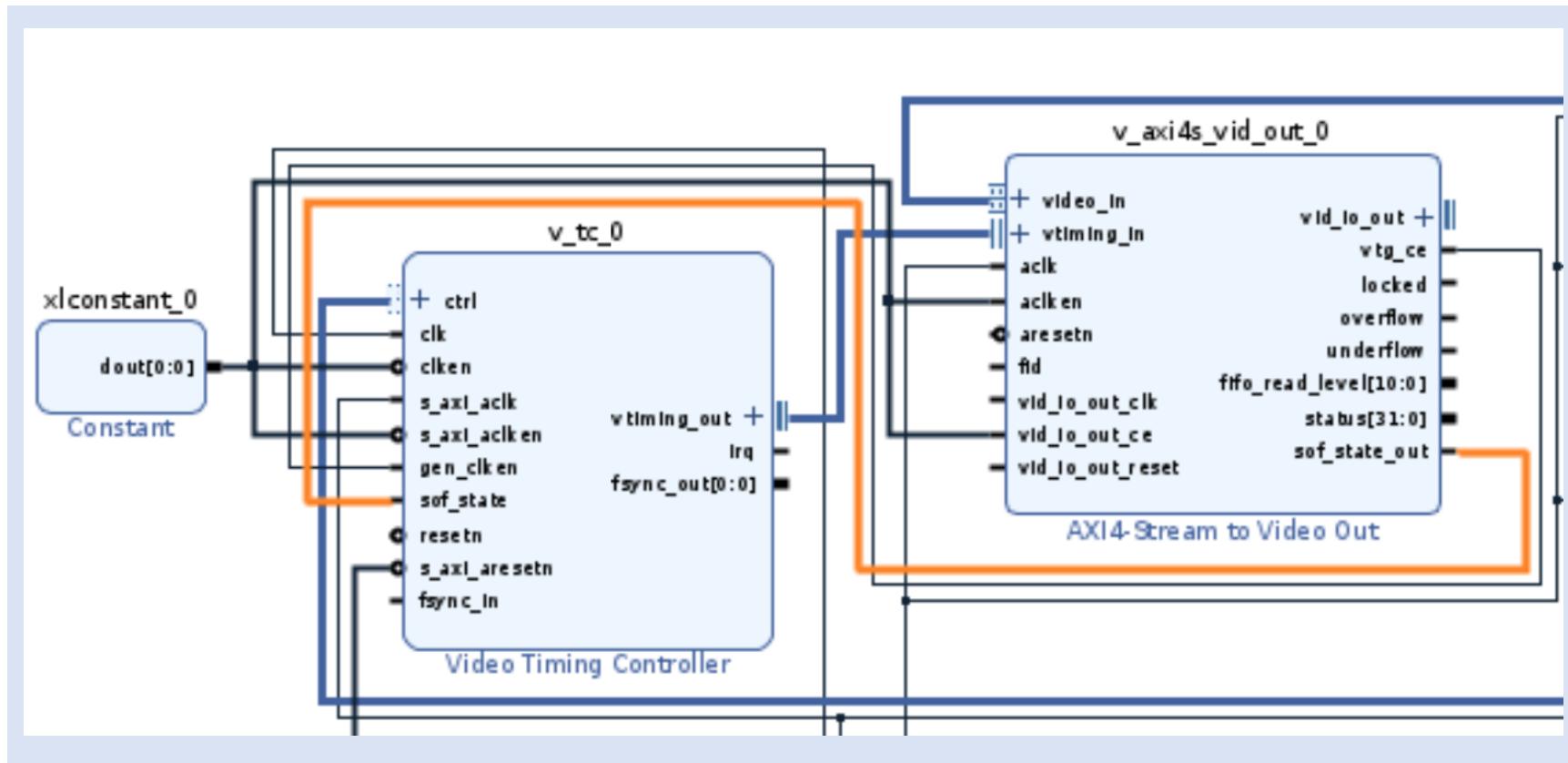
Crowd Supply: Lab One

Step 48 – Connect vtg_ce (AXIS Vid Out) to gen_clken (VTC)



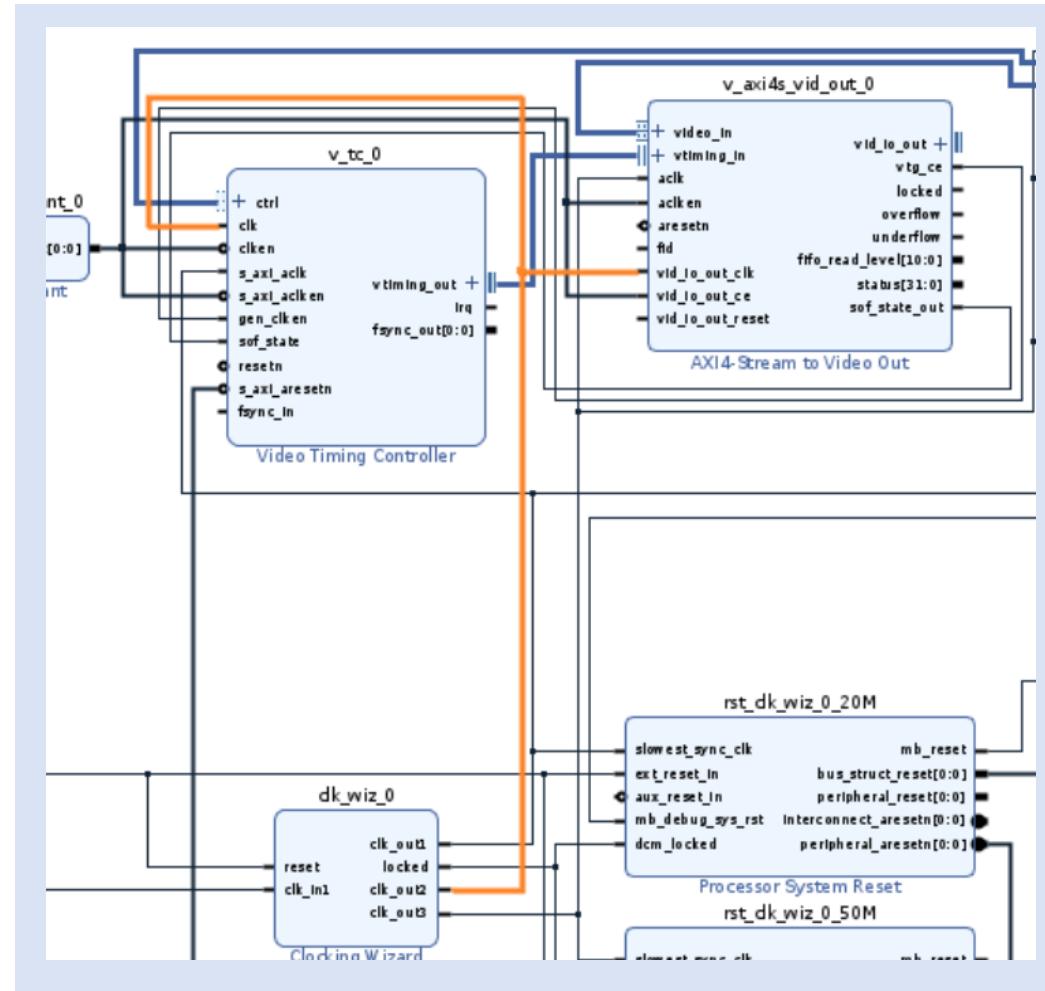
Crowd Supply: Lab One

Step 49 – Connect sof_state_out (AXIS Vid Out) to sof_state (VTC)



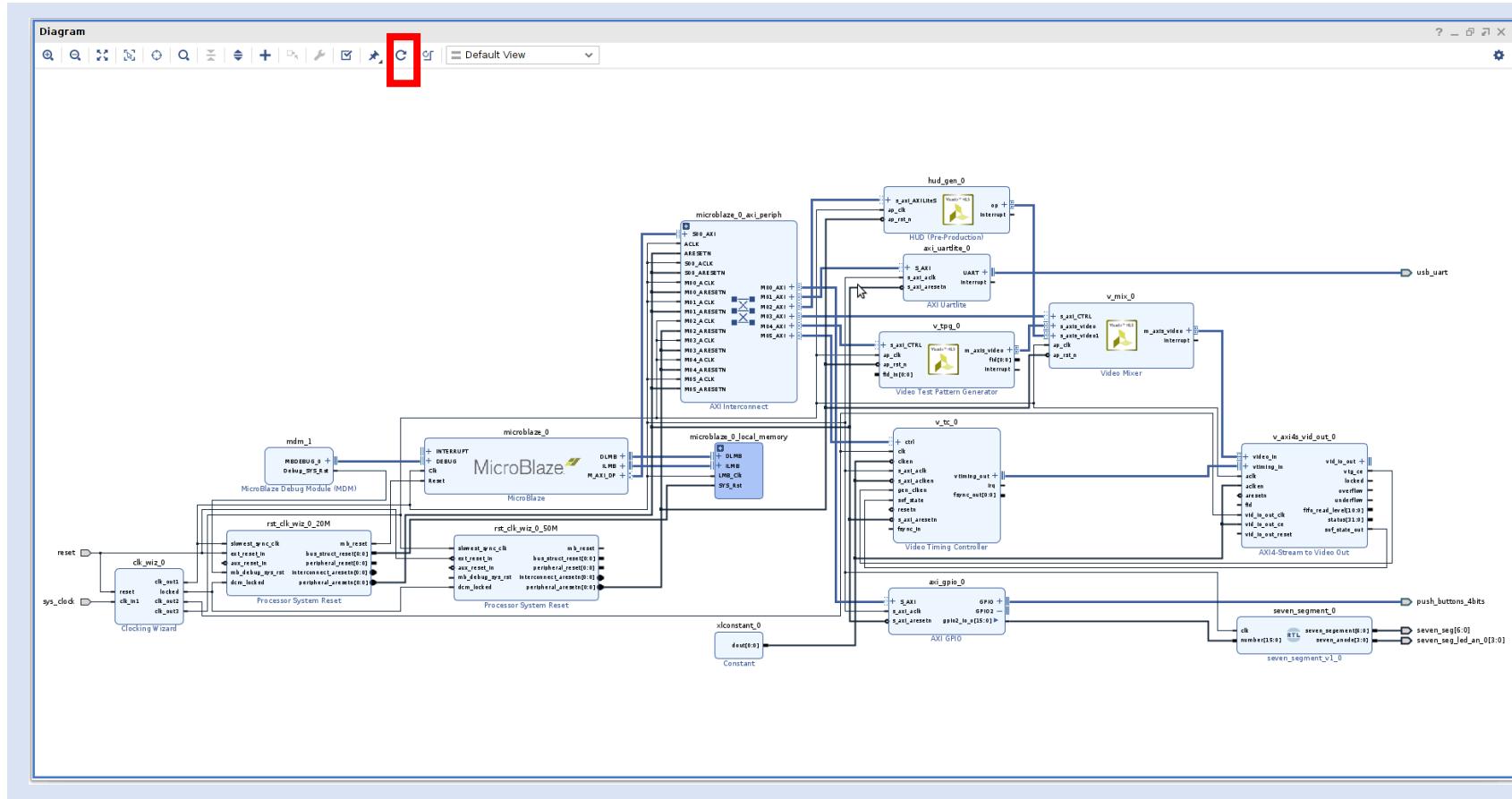
Crowd Supply: Lab One

Step 50 – Connect clk_out2 (25MHz) to clk (VTC) and vid_io_out_clk (AXI4S Vid Out)



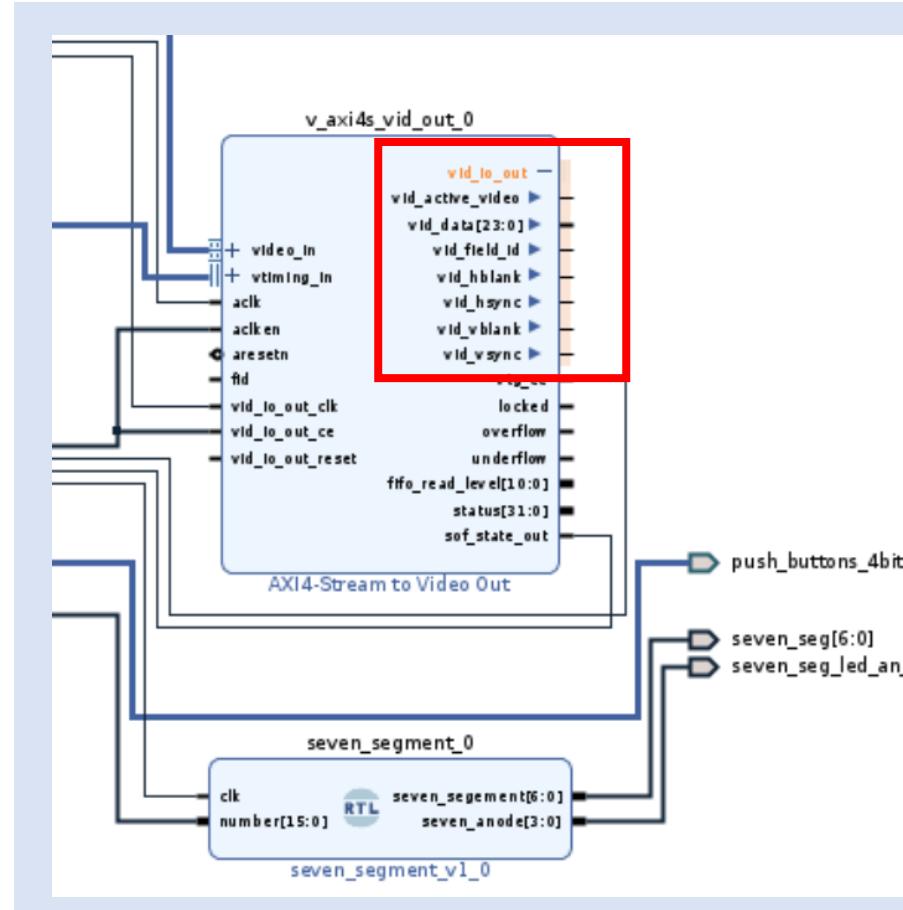
Crowd Supply: Lab One

Step 51 – Click on the regenerate layout icon to make the diagram more understandable.



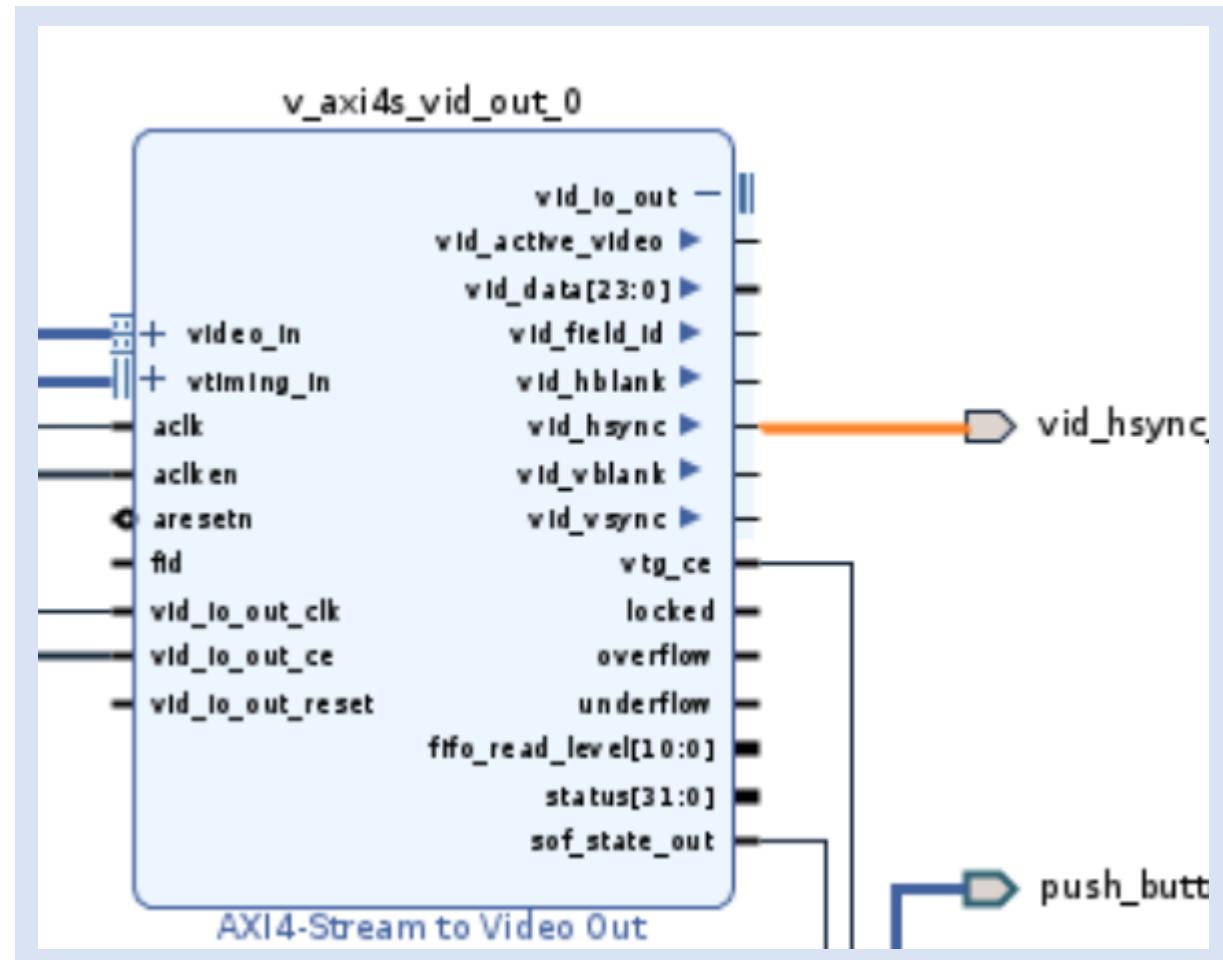
Crowd Supply: Lab One

Step 52 – Expand vid_io_out on the AXIS Video Out block



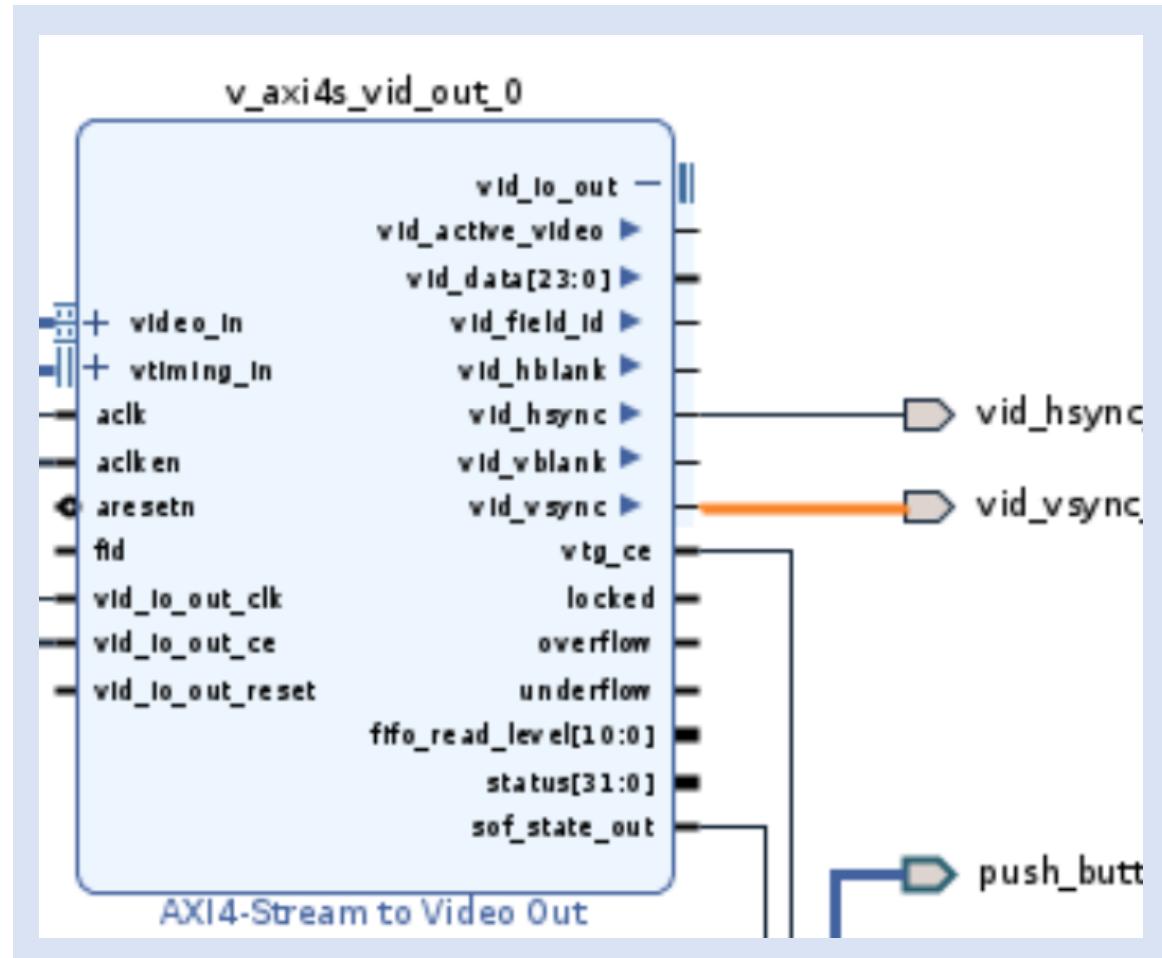
Crowd Supply: Lab One

Step 53 – Make vid_hsync (AXI Vid Out) external and rename it **Hsync. (Warning: External port names are case sensitive. Copy names exactly as shown in instructions as IO standards are set in constraints using port names.)**



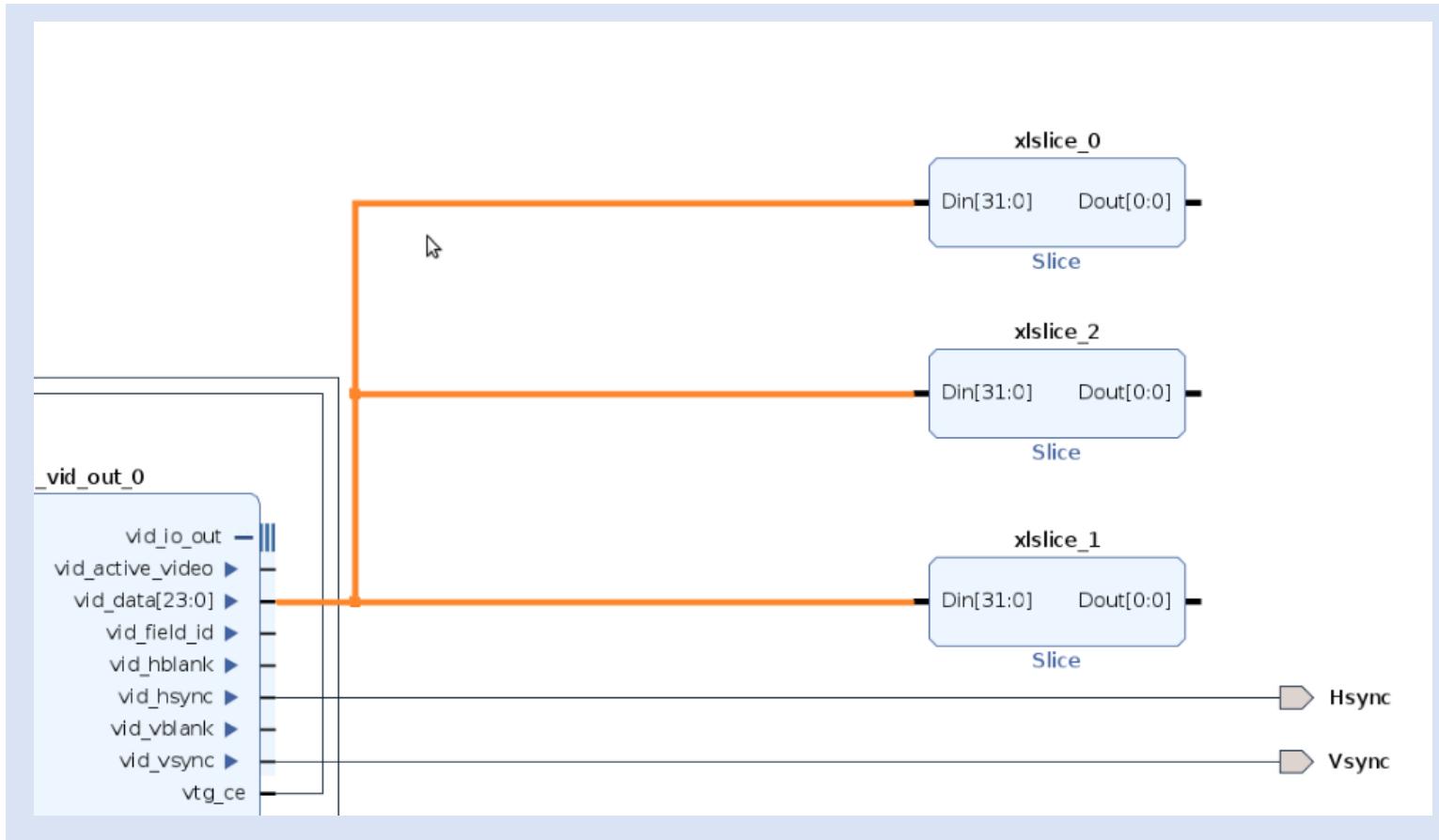
Crowd Supply: Lab One

Step 54 – Make vid_vsync (AXIS Vid Out) external and re-name it **Vsync**.



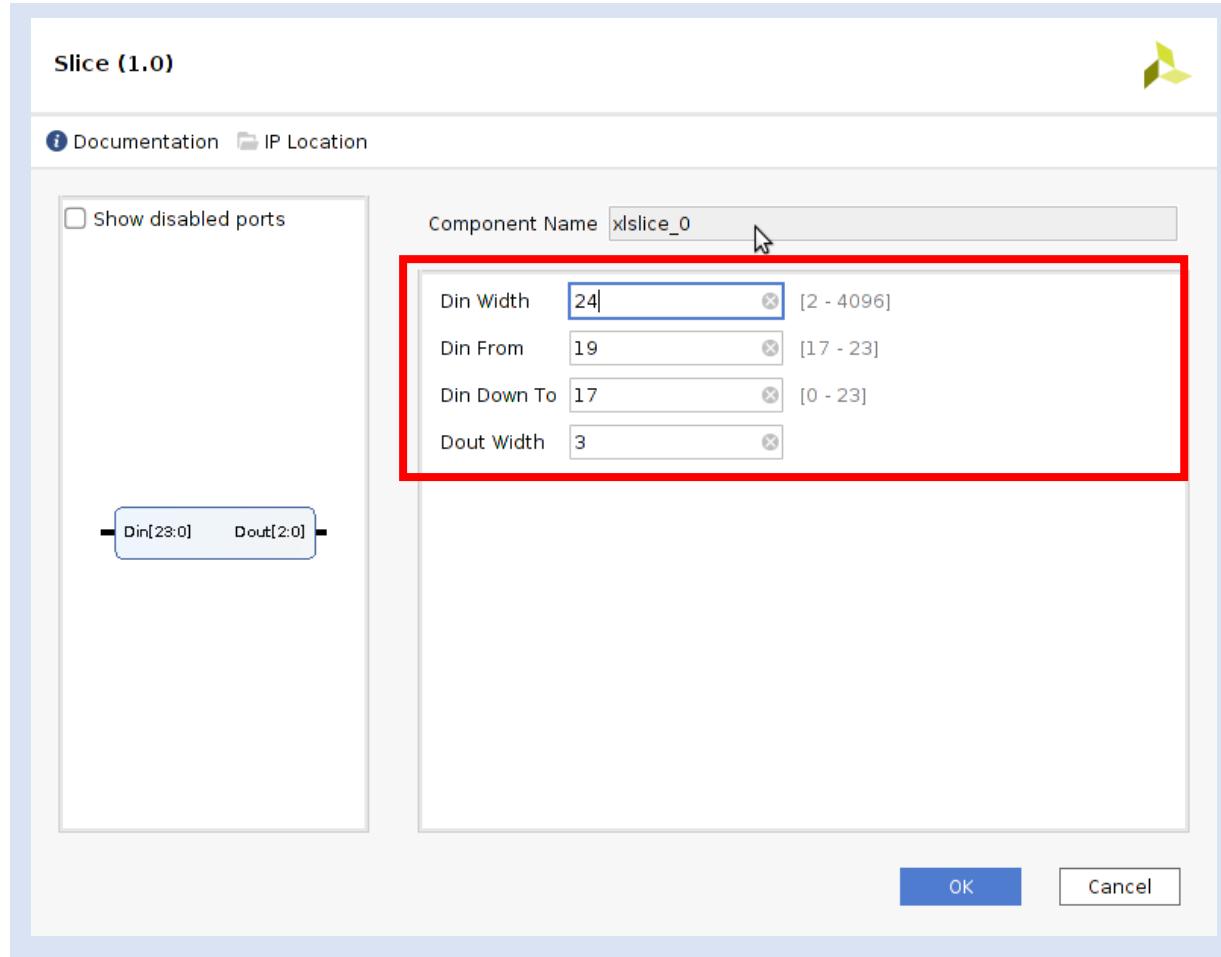
Crowd Supply: Lab One

Step 55 – Add in three “Slice” IP blocks and connect them to the vid_data output (AXIS Vid Out)



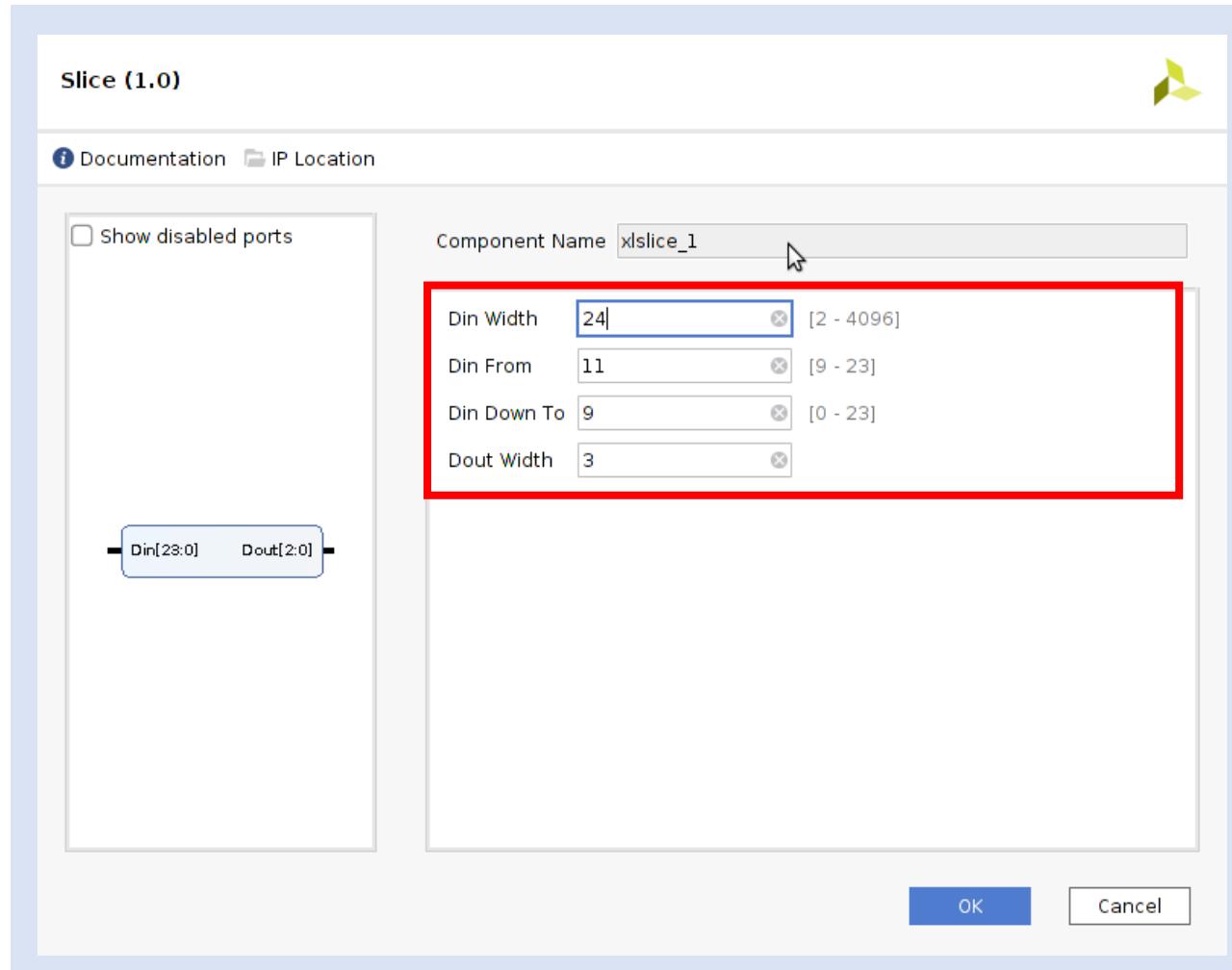
Crowd Supply: Lab One

Step 56 – Re-customize Slice 0 with the settings as below



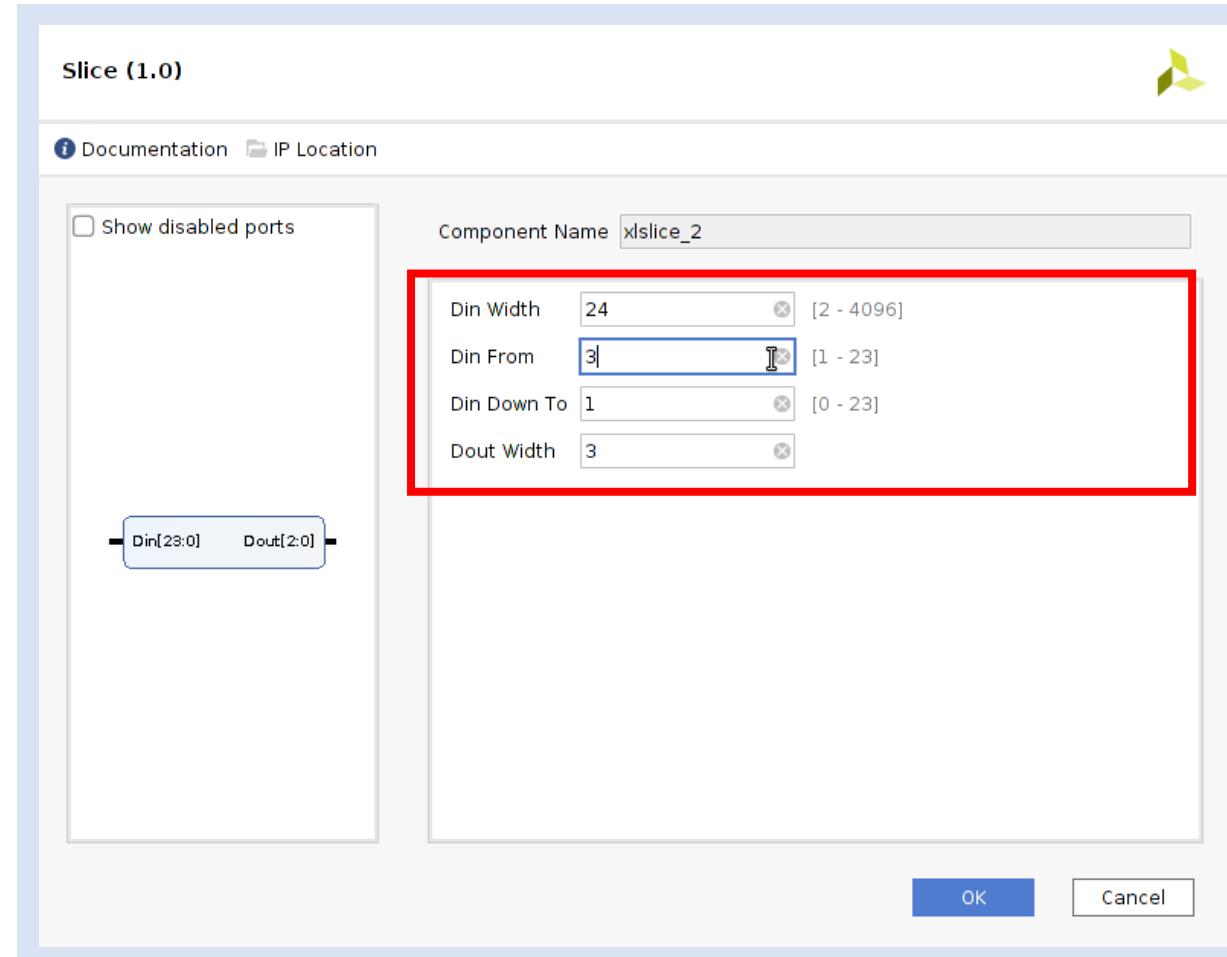
Crowd Supply: Lab One

Step 57 – Re-customize Slice 1 with the settings as below



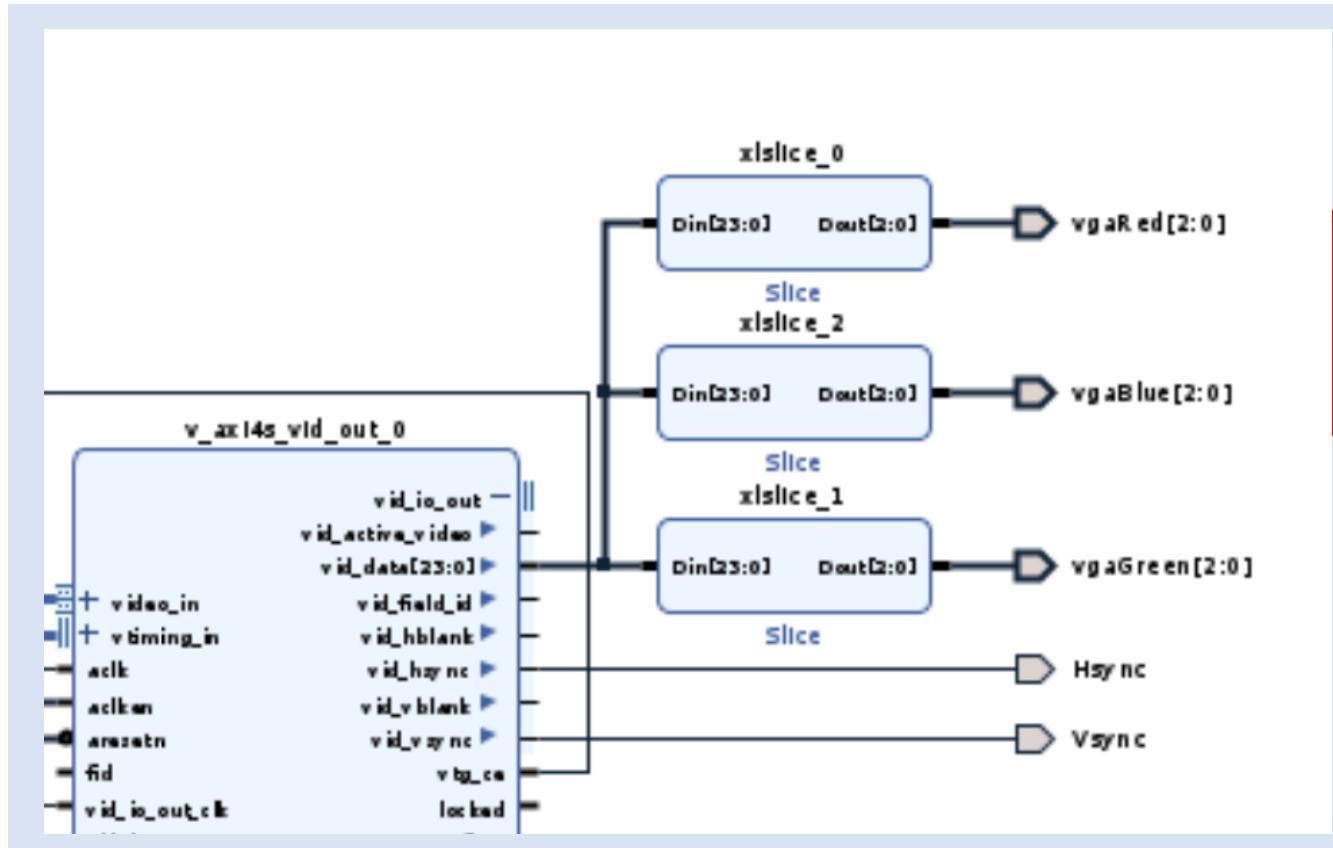
Crowd Supply: Lab One

Step 58 – Re-customize Slice 2 with the settings as below



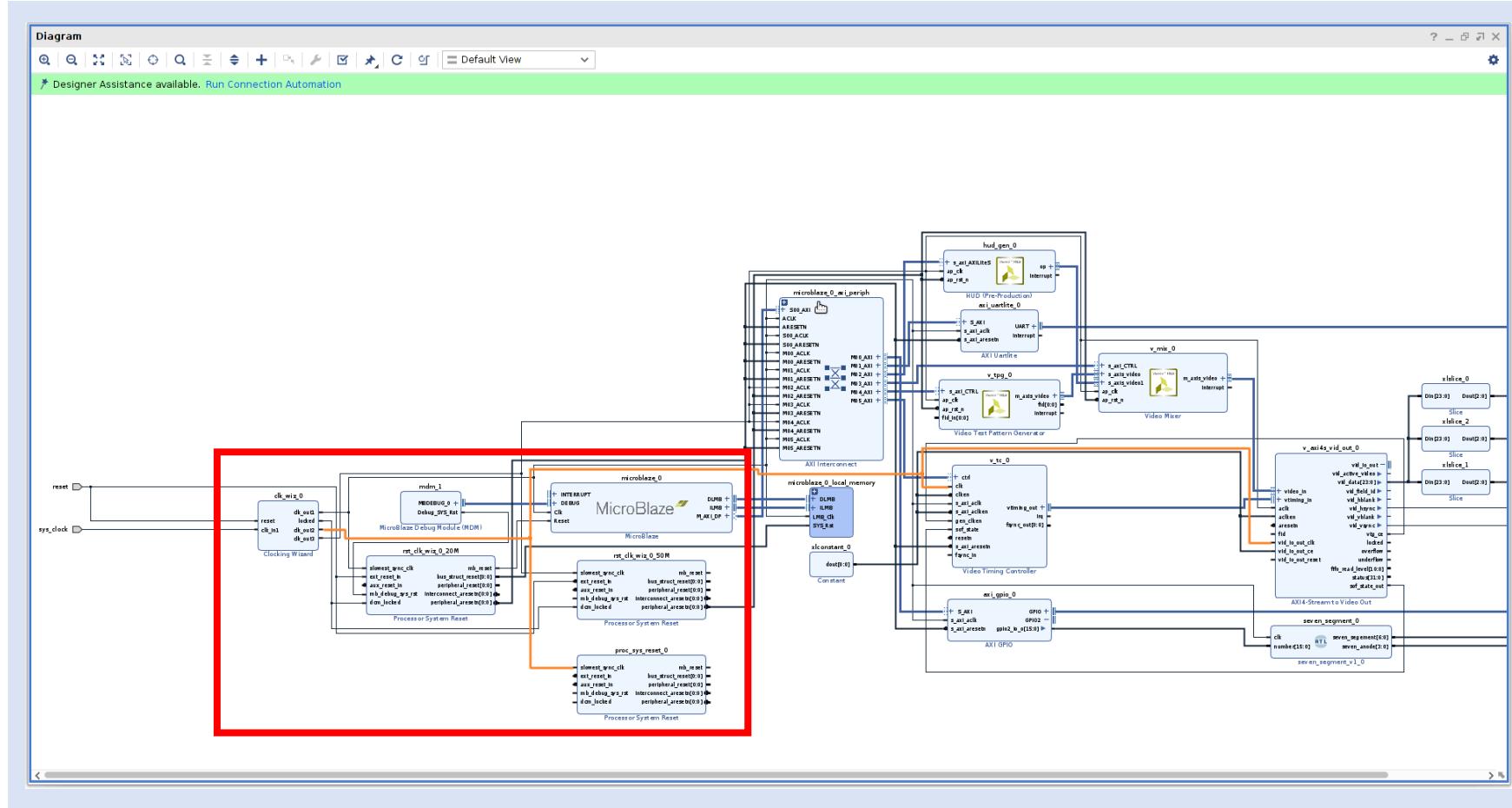
Crowd Supply: Lab One

Step 59 – Make the three slice output ports external. Name them as follows: Slice0 > vgaRed, Slice1 > vgaBlue, Slice2 > vgaGreen



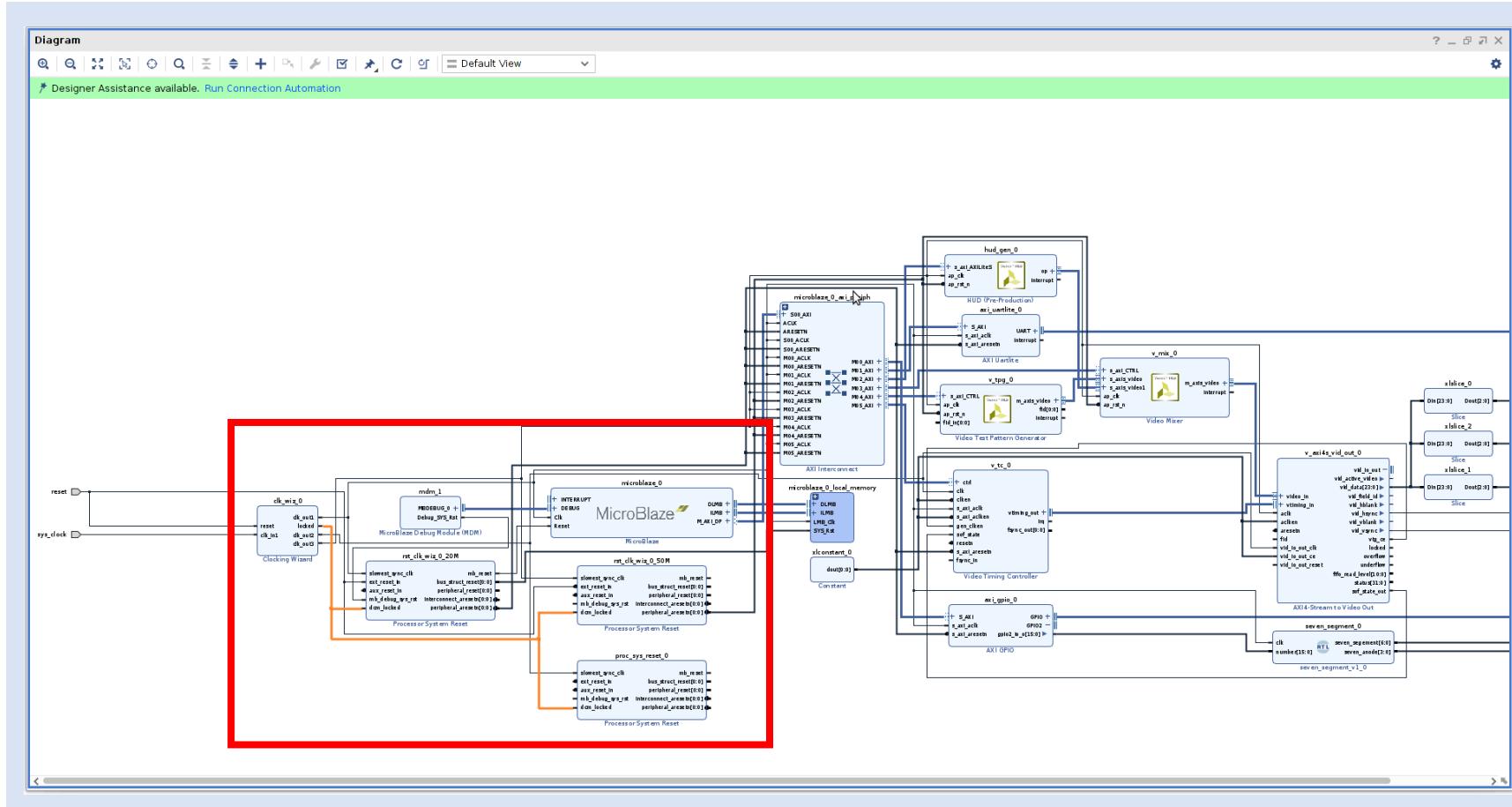
Crowd Supply: Lab One

Step 60 – Add in a new Processor System Reset block. Connect its clock input to clk_out2 (25 MHz).



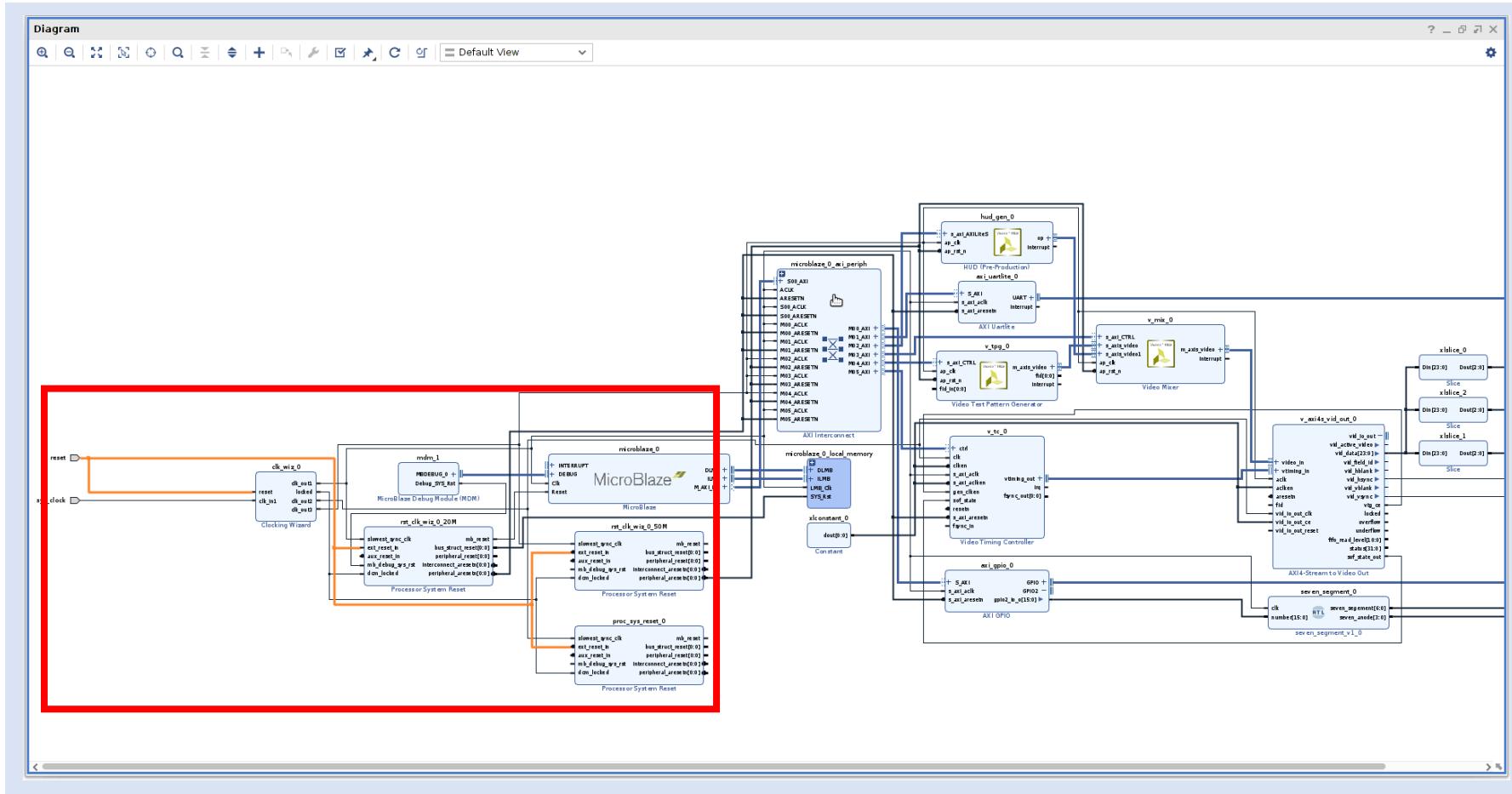
Crowd Supply: Lab One

Step 61 – Connect dcm_locked signal (PSR) to locked (clock wizard).



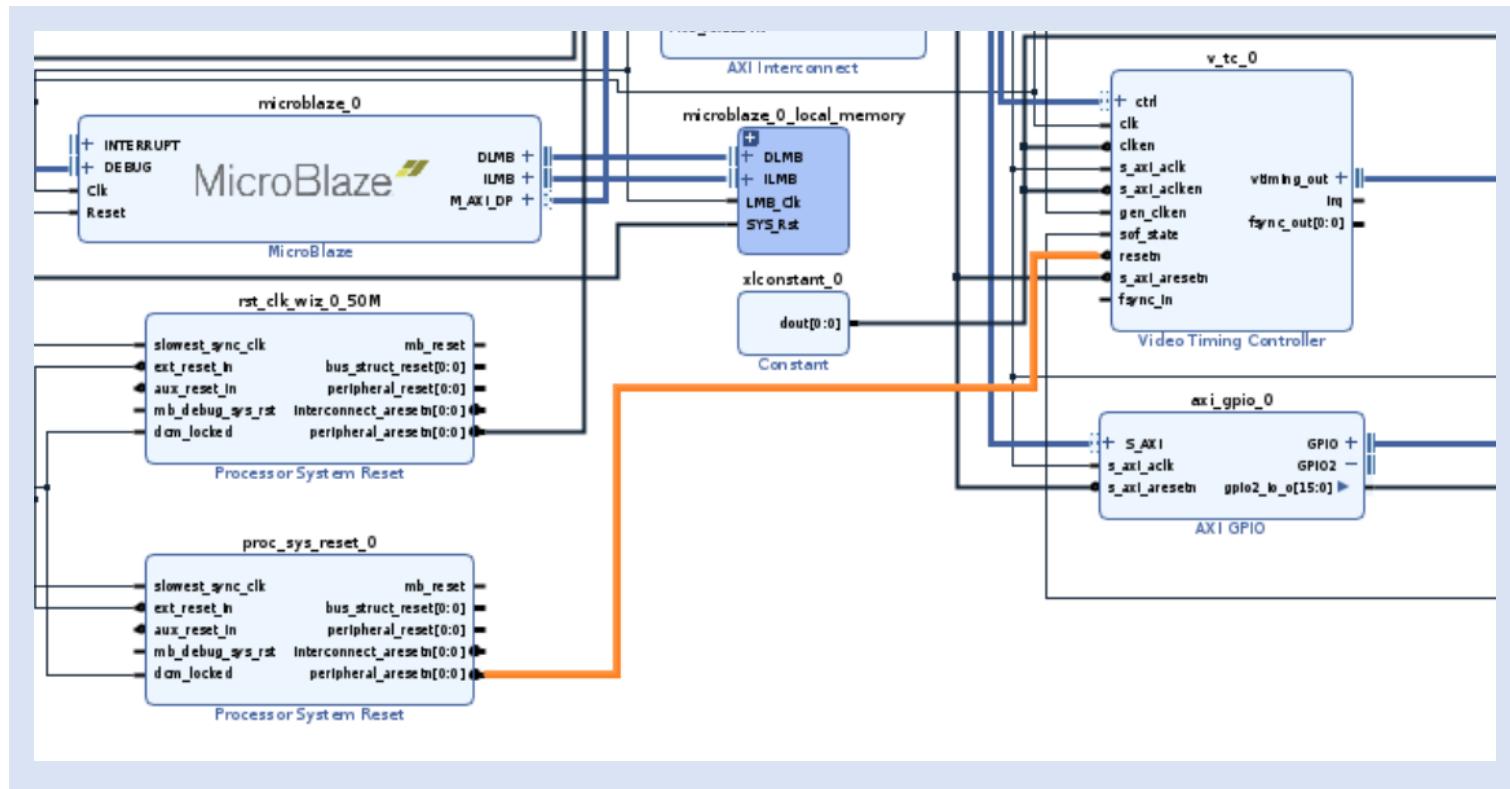
Crowd Supply: Lab One

Step 62 – Connect reset (clock wizard) to ext_reset_in (PSR).



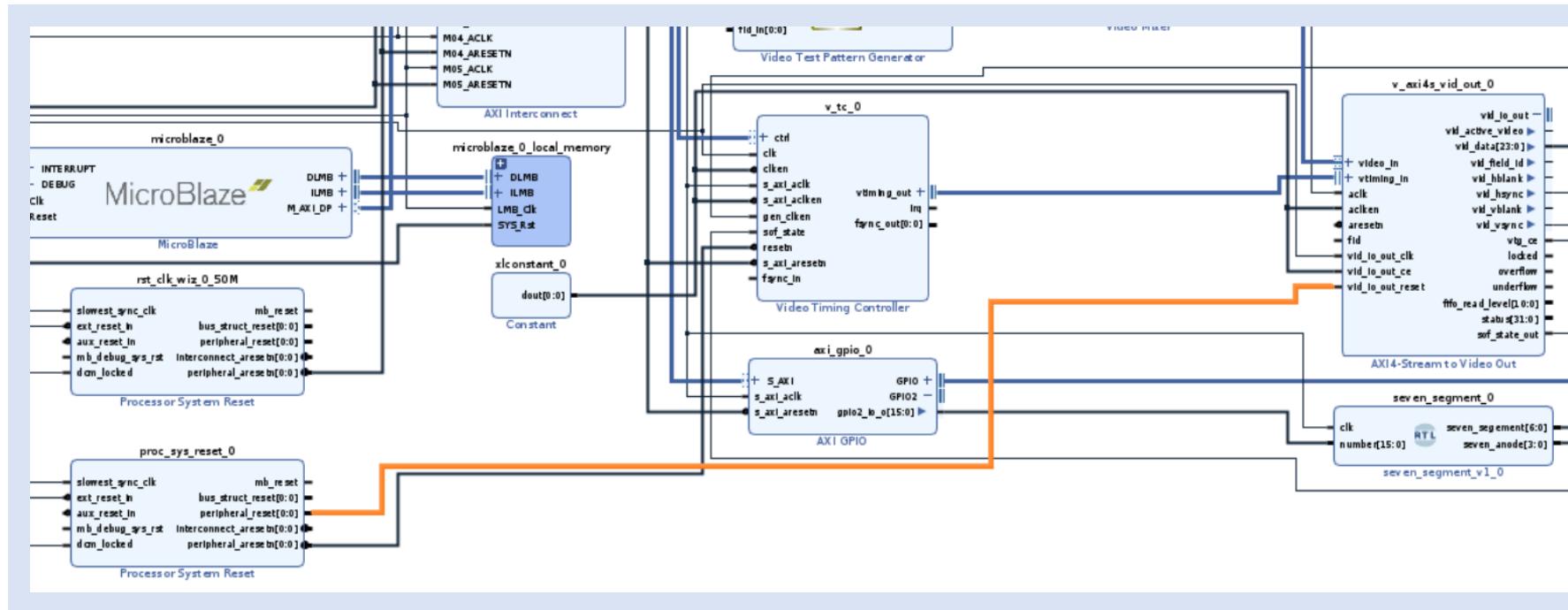
Crowd Supply: Lab One

Step 63 – Connect peripheral_aresetn (PSR) to resetn (VTC).



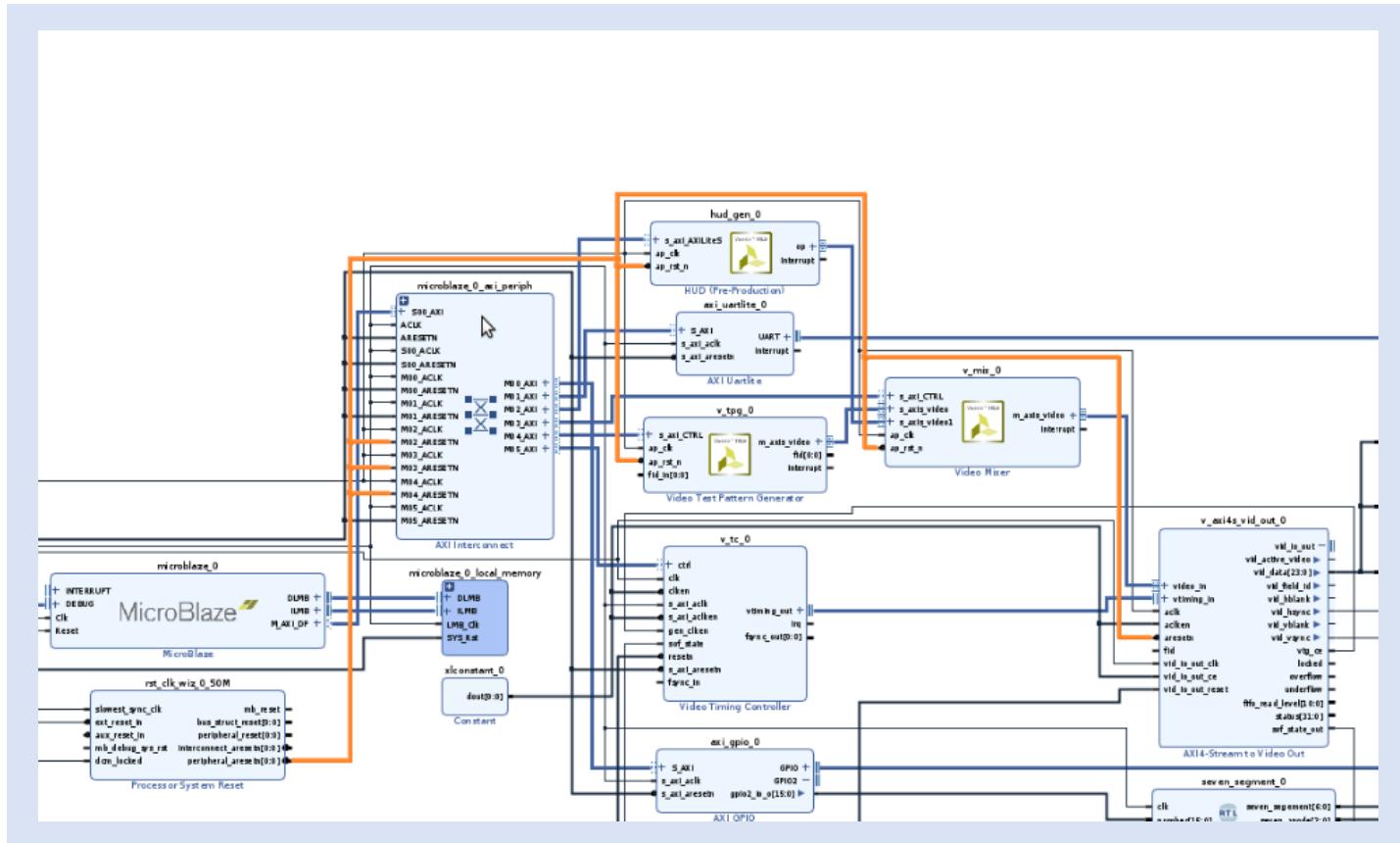
Crowd Supply: Lab One

Step 64 – Connect peripheral_areset (PSR) to vid_in_out_reset (AXIS Video Out).



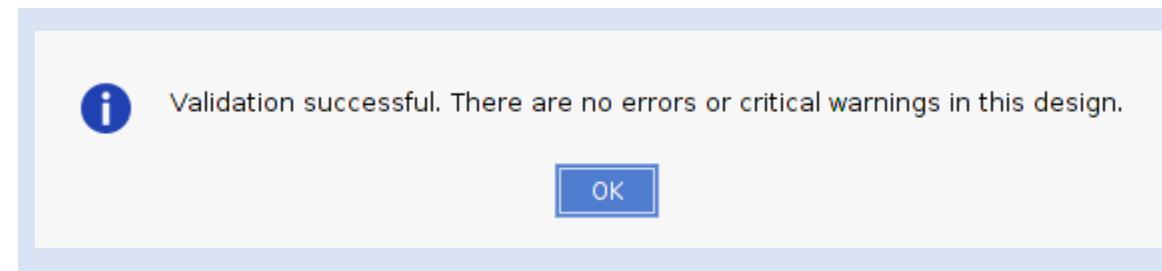
Crowd Supply: Lab One

Step 65 – Connect the peripheral_areset from the reset block associated with clk_out3 (50 MHz) to aresetn (AXIS Vid Out).



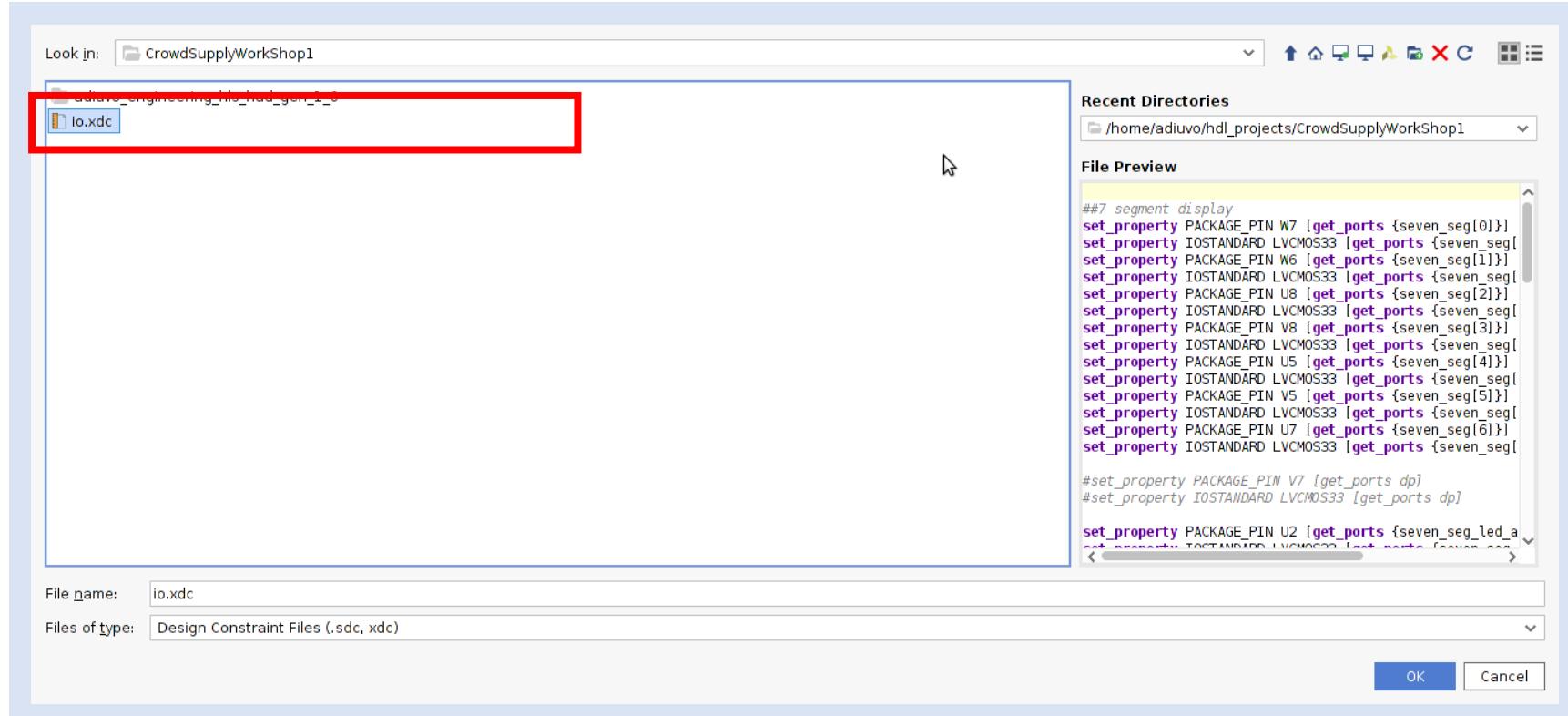
Crowd Supply: Lab One

Step 66 – Validate the design by right-clicking anywhere in the diagram and selecting “Validate Design”. We should see no errors or warnings.



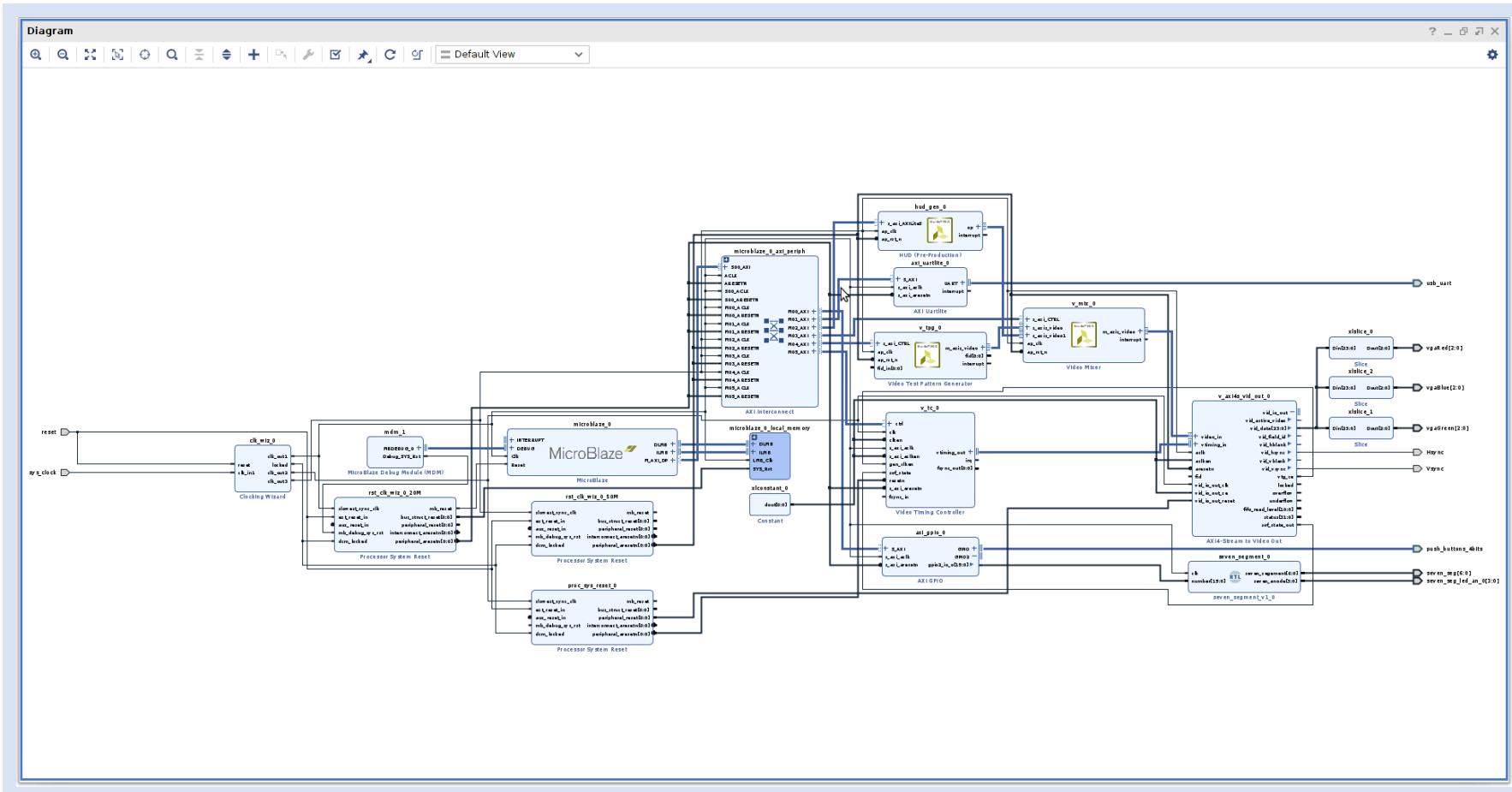
Crowd Supply: Lab One

Step 67 – Add in a new source through the Project Manager dropdown; select “Add or create constraints” when prompted. Select the .xdc file from the cloned directory as shown below and click “OK”.



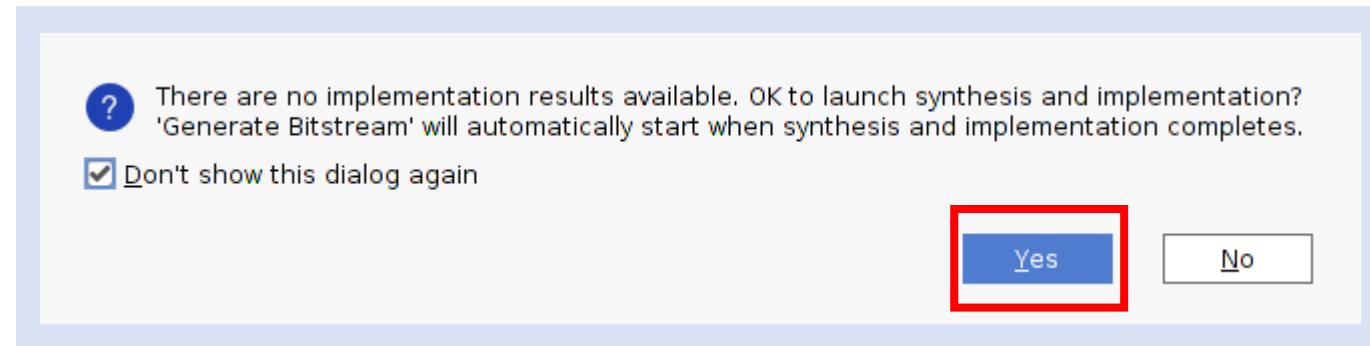
Crowd Supply: Lab One

Step 68 – The final block design should look as below.



Crowd Supply: Lab One

Step 69 – Under Flow Navigator > Program and Debug, select “Generate Bitstream”. Click “Yes” if given the dialogue below.



Crowd Supply: Lab One

Step 70 –Configure runs as below and select “OK”. This may take some time—the status of synthesis and implementation runs preceding bitstream generation can be monitored under the “Design Runs” tab.

