Aalto University
School of Electrical
Engineering

Module 2

Switched-Mode Conversion: Full Bridge and Unipolar PWM

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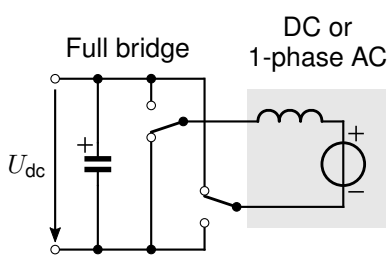
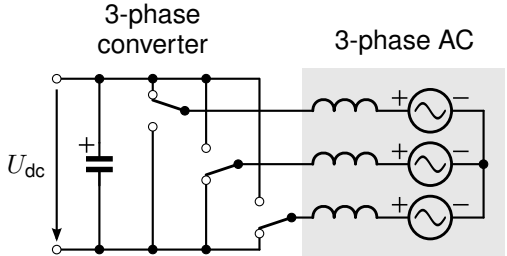
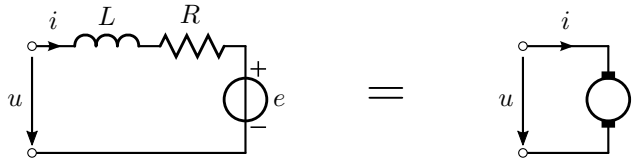
Full Bridge is Similar to 3-Phase Converter





Symbol Used for the Load



Outline

Full Bridge

Unipolar Pulse-Width Modulation

Synchronous Sampling and PWM Update Delay

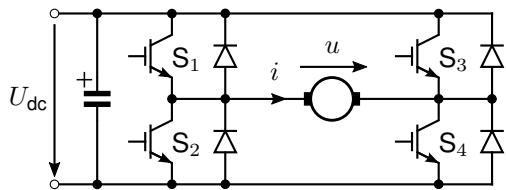
Full Bridge

S_1 and S_4 switched ON: $u = U_{dc}$

S_2 and S_3 switched ON: $u = -U_{dc}$

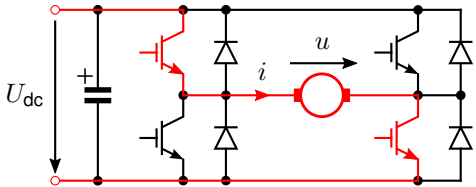
S_1 and S_3 switched ON: $u = 0$

S_2 and S_4 switched ON: $u = 0$

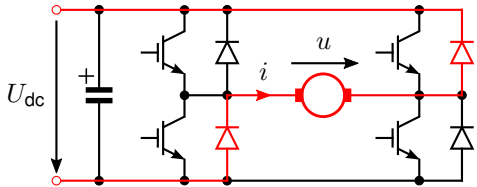


Operation Modes

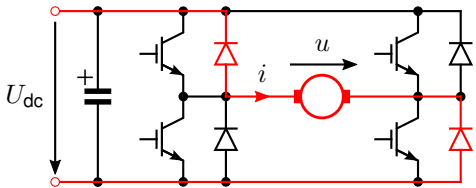
Only Nonzero Voltage Switching States Are Shown



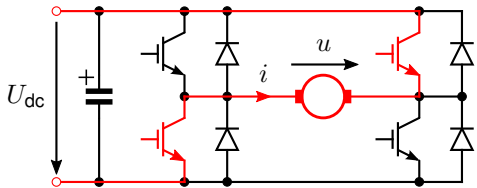
$u = U_{dc}, \quad i > 0$



$u = -U_{dc}, \quad i > 0$



$u = U_{dc}, \quad i < 0$

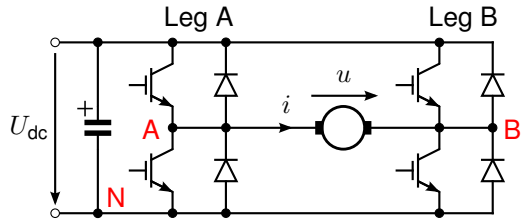


$u = -U_{dc}, \quad i < 0$

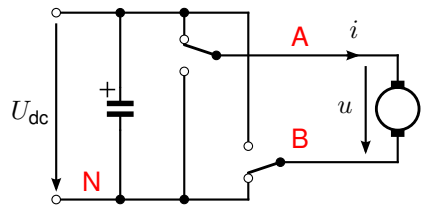
Notation of Potentials and Voltages

- Legs can be modelled as bi-positional switches
- Negative DC-bus potential N
- u_{AN} is the voltage between potentials A and N
- u_{BN} is the voltage between potentials B and N
- Converter output voltage

$$u = u_{\mathrm{AN}} - u_{\mathrm{BN}}$$



Circuit diagram



Equivalent circuit

Switching States of the Bi-Positional Switches

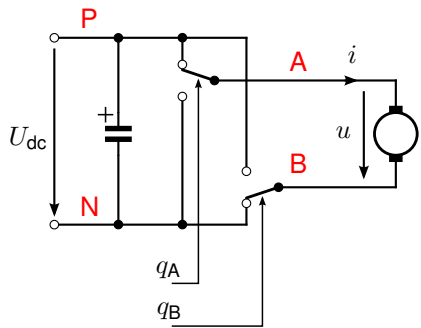
- Switching state q
  - $q = 0$ if the switch is connected to N
  - $q = 1$ if the switch is connected to P
- Pole voltages

$$u_{\mathrm{AN}} = q_{\mathrm{A}} U_{\mathrm{dc}} \qquad u_{\mathrm{BN}} = q_{\mathrm{B}} U_{\mathrm{dc}}$$

- Converter output voltage

$$u = (q_{\mathrm{A}} - q_{\mathrm{B}}) U_{\mathrm{dc}}$$

- Figure: $q_{\mathrm{A}} = 1$ and $q_{\mathrm{B}} = 0$, giving $u = U_{\mathrm{dc}}$



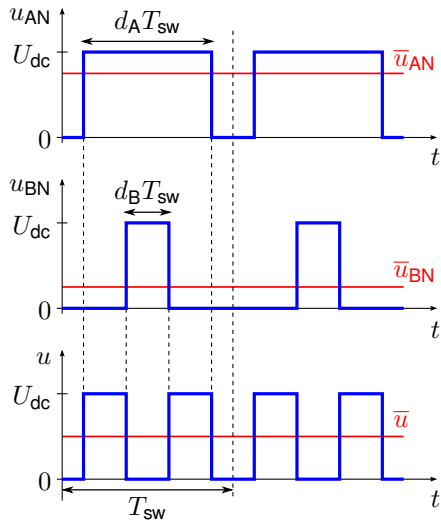
Switching-Cycle Averaged Quantities

- Average pole voltage over T_{sw}

$$\overline{u}_{\mathrm{AN}} = \frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}} u_{\mathrm{AN}} \mathrm{d}t = d_{\mathrm{A}} U_{\mathrm{dc}}$$

- Average voltage $\overline{u}_{\mathrm{BN}}$ is obtained similarly
- Average output voltage

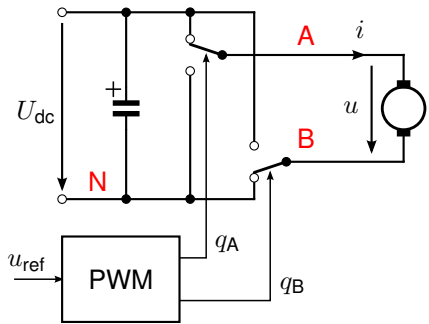
$$\overline{u} = (d_{\mathrm{A}} - d_{\mathrm{B}}) U_{\mathrm{dc}}$$



Outline

Pulse-Width Modulation

- PWM generates the control signals q_A and q_B for the power switches
- Goal: switching-cycle averaged voltage $\overline{u}$ equals the reference voltage u_{ref}
- Various PWM methods exist: they all give $\overline{u} = u_{ref}$ but produce different pulse patterns
- Unipolar PWM will be considered in the following



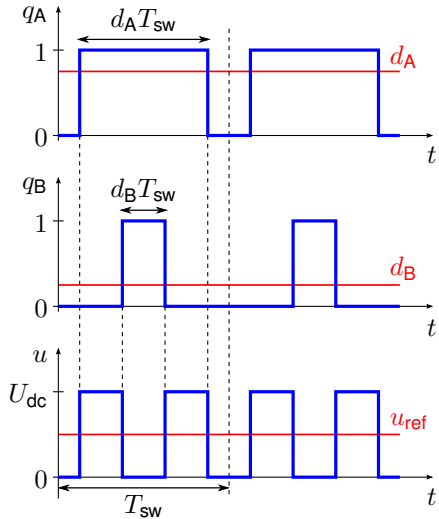
Duty Cycles

- Conditions $\overline{u}_{\mathrm{a}} = u_{\mathrm{a,ref}}$ and $d_{\mathrm{A}} + d_{\mathrm{B}} = 1$ lead to the duty cycles

$$d_{\mathrm{A}} = \frac{1}{2}\left(1 + \frac{u_{\mathrm{ref}}}{U_{\mathrm{dc}}}\right)$$

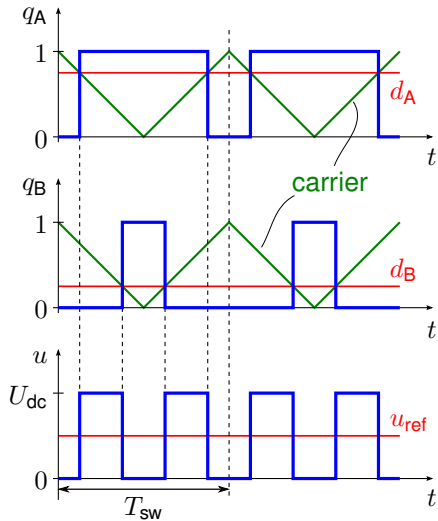
$$d_{\mathrm{B}} = \frac{1}{2}\left(1 - \frac{u_{\mathrm{ref}}}{U_{\mathrm{dc}}}\right)$$

- Example in the figure: $u_{\mathrm{ref}} = 0.5 U_{\mathrm{dc}}$
- What are the duty cycles d_{A} and d_{B}?
- How to generate the control signals q_{A} and q_{B}?



Carrier Comparison

- Carrier comparison is often used for generating the control signals
  - Triangular carrier with the period T_{sw}
  - Magnitude varies between 0 and 1
- If d is higher than the carrier, then $q = 1$ (otherwise $q = 0$)
- Same carrier for both d_{A} and d_{B}
- Next slide: step change in the voltage reference ($-0.5U_{\text{dc}} \rightarrow 0.75U_{\text{dc}}$)

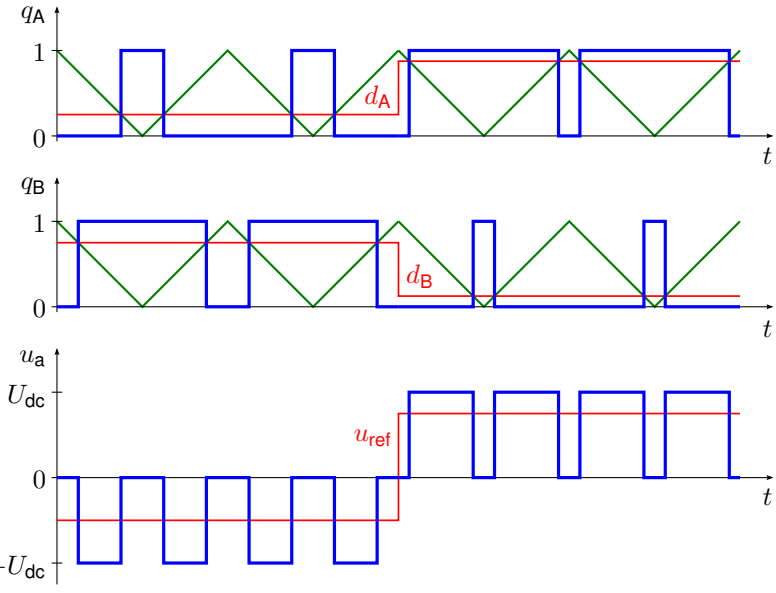


There are various ways to scale the carrier waveform and the reference quantities. Using the carrier varying between 0 and 1 together with the duty cycle references is convenient in digital implementation.

$$d_\mathrm{A} = \frac{1}{2}\left(1 + \frac{u_\mathrm{ref}}{U_\mathrm{dc}}\right)$$

$$d_\mathrm{B} = \frac{1}{2}\left(1 - \frac{u_\mathrm{ref}}{U_\mathrm{dc}}\right)$$

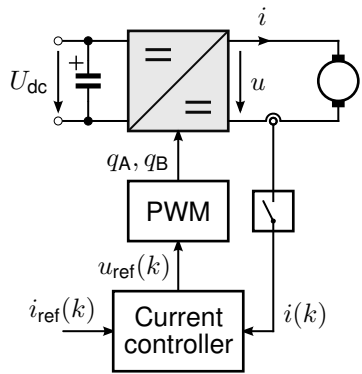
$$\overline{u} = (d_\mathrm{A} - d_\mathrm{B})U_\mathrm{dc}$$



Outline

Digital Control System

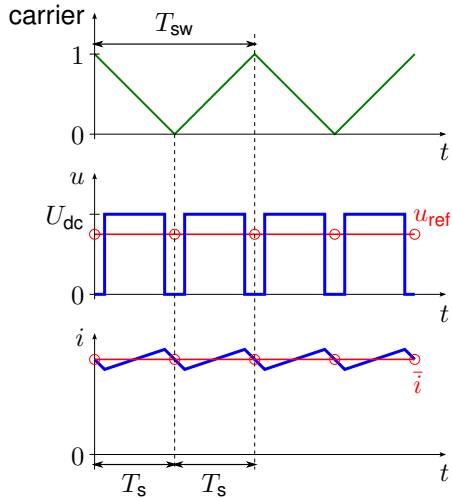
- Current is measured for the feedback of the current controller
- Sampling is synchronized with the PWM
- Synchronized sampling effectively removes the switching ripple from the samples



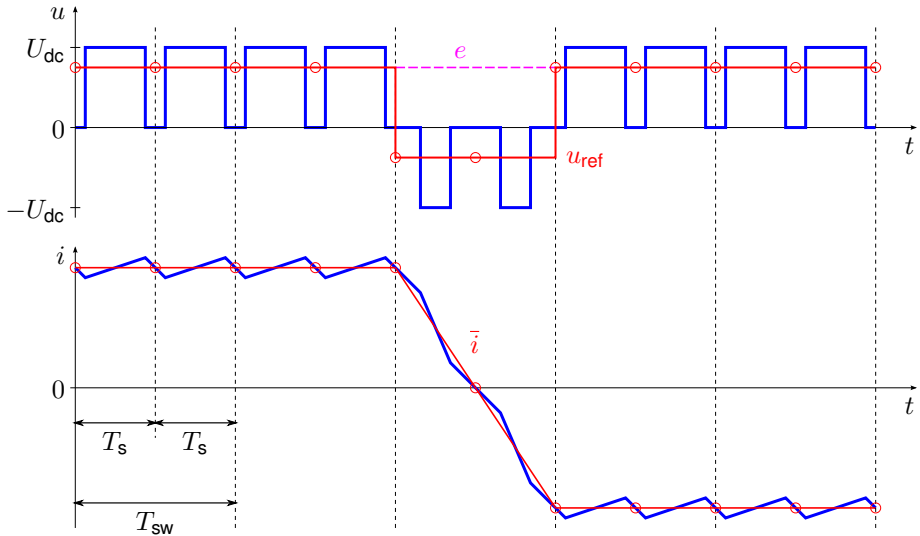
Synchronous Sampling

- Voltage reference u_{ref} can be updated in the beginning and in the middle of the carrier (marked with the circles)
- Current samples (circles) can be taken at these same time instants
- Next slide: Current response is governed by

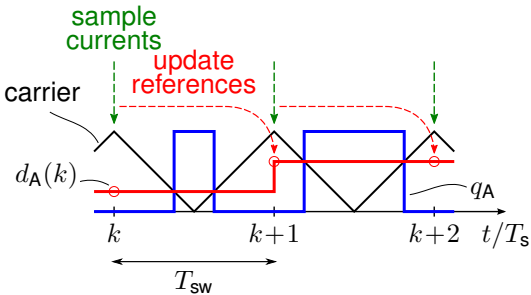
$$L\frac{\mathrm{d}i}{\mathrm{d}t} = u - e$$



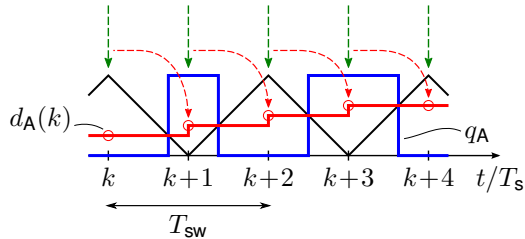
Different variants of sampling synchronized with the PWM exist, while only one is presented here. Furthermore, it can be noticed that actually four current samples per carrier period could be taken without the current ripple in the case of the unipolar PWM.


u
U_{dc}
0
$-U_{dc}$
e
u_{ref}
t
i
$\bar{i}$
0
t
T_s
T_s
T_{sw}

Computational Delay in the PWM Update



Single-update PWM



Double-update PWM

- Duty ratios d_A and d_B are updated simultaneously (only d_A is shown)
- Computing new voltage (duty ratio) reference takes a finite time
- References calculated using the current samples at k will be applied at $k+1$
- This computational delay cannot be avoided in practice