Southern Illinois University
Department of Electrical and Computer Engineering

ASIC Design Final Project

Implementation of ANN to predict Handwritten Digits

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In this project, we implement a 3 layer artificial neural network to recognize the handwritten digits correctly. The input are 8*8 pixel images with each pixel ranging from -0.5 to 0.5. These values are represented by 8-bit fixed point 2's complementary numbers with 7 fractional bits.

1. **MAC**
   The first part of the project involved in design of MAC(Multiplier and Accumulator Circuit). The block diagram of MAC circuit is presented in figure 1. The module

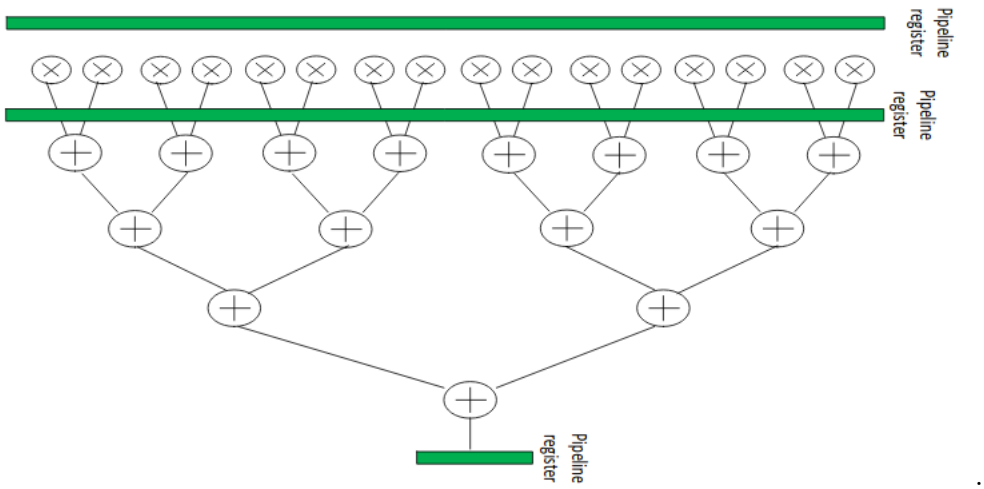

Figure 1: MAC block diagram

computes

$$y = \sum_{i=1}^{16} w_i.x_i \tag{1}$$

where w_i and x_i are 8-bit fixed point numbers.

The schematic of designed MAC module is in figure 2. We have used pipeline register and on running the synthesis using timing constraint with clock period 10 ns, the Worst Negative slack is 12.601 ns for the hold time satisfies with Worst Hold Slack of 0.511 ns.

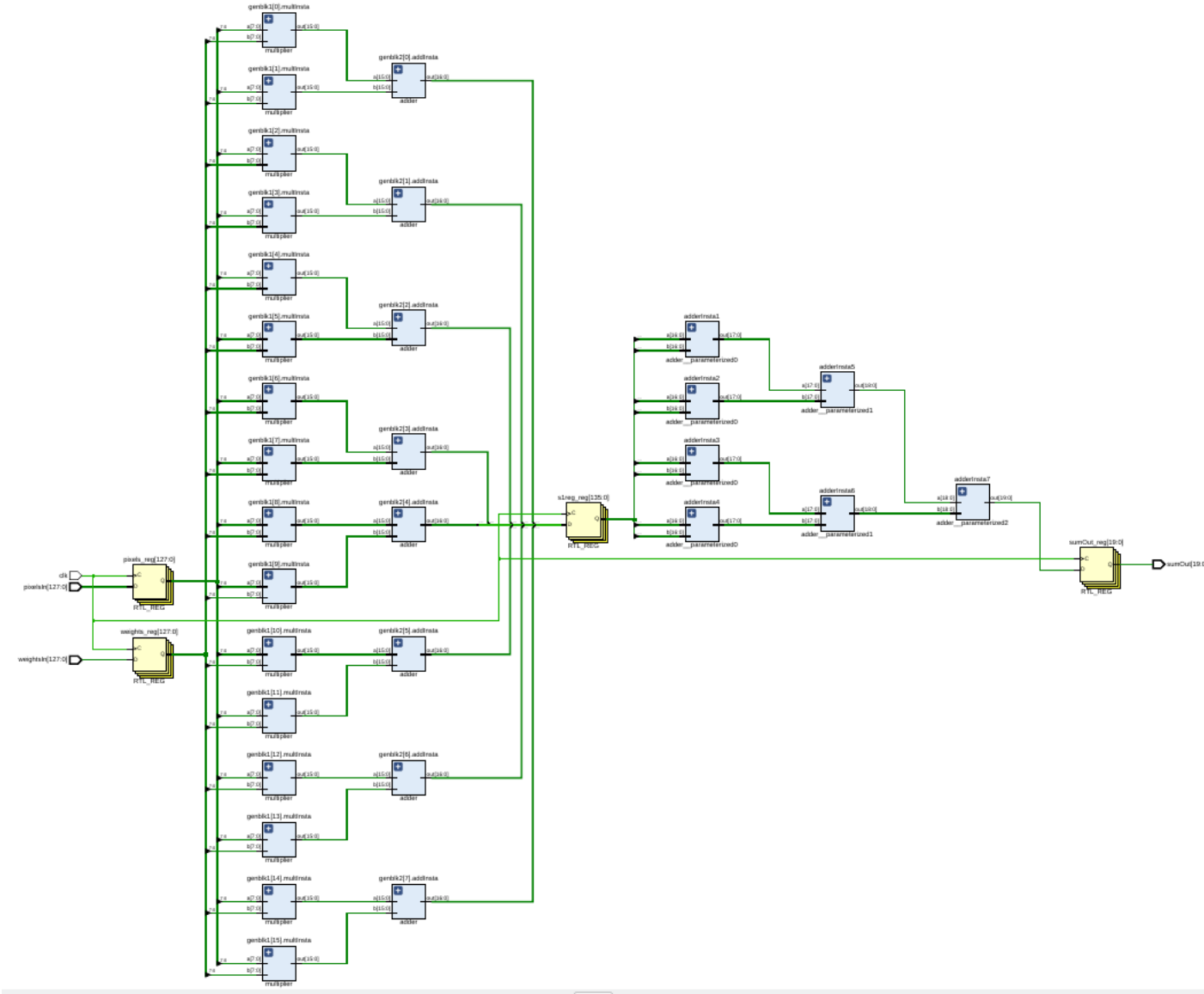

Figure 2: MAC block diagram

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	12.601 ns	Worst Hold Slack (WHS):	0.511 ns	Worst Pulse Width Slack (WPWS):	9.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	156	Total Number of Endpoints:	156	Total Number of Endpoints:	413

All user specified timing constraints are met.

Figure 3: Timing Summary

2. **ACC**
   The MAC module does computation for 16 multiplications and adds them together. Since we need to add 64 multiplications to get output of the hidden node, we need to use MAC module for 4 clock cycles. In first clock cycle, we add the bias. The

weighted sum performed by ACC module is

$$y = \sum_{i=1}^{N} w_i.x_i + b_i \tag{2}$$

After that, we add for 3 clock cycles. The Accumulator schematic is shown in figure 4. An FSM is designed to control the accumulator and a MUX is used to either select bias or the previous accumulator value to be added to the input.

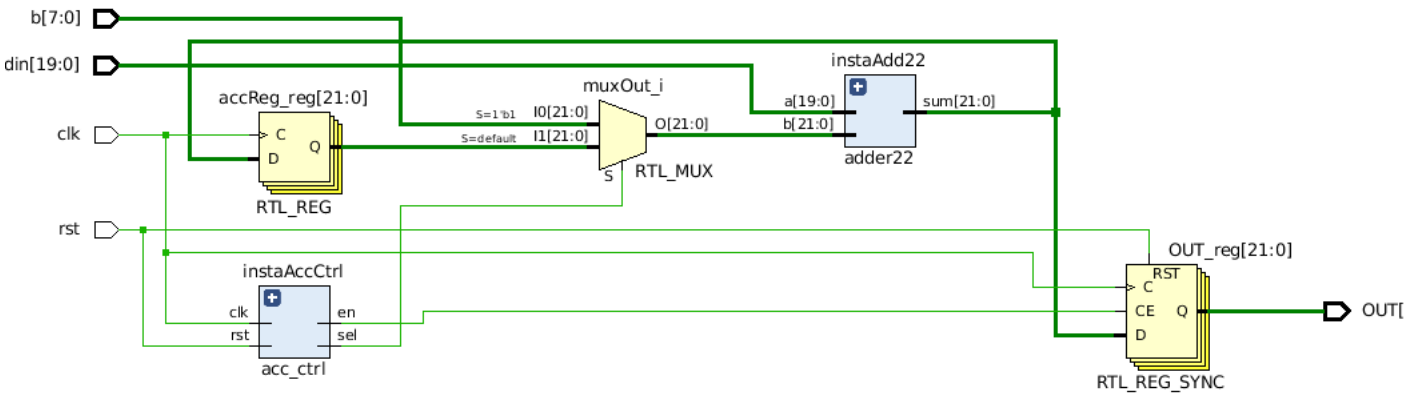

Figure 4: ACC Schematic

3. **MAC_ACC**
We now connect the MAC and ACC modules together to form a MAC_ACC module. The schematic of MAC_ACC module is in figure 5.

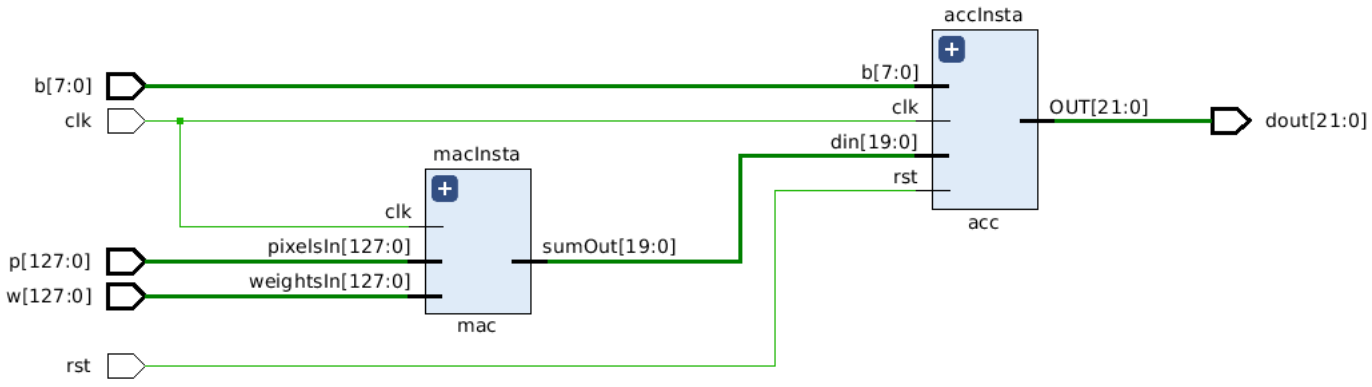

Figure 5: MAC_ACC Schematic

4. **Sigmoid_func**
We created a sigmoid_func module. The sigmoid_func module consists of sig-

moid_IP and the IP wrapper. The sigmoid IP is an activation function that computes

$$f(y) = \frac{1}{1 + e^{-y}} - 0.5 \tag{3}$$

The IP wrapper module takes the 22 bit output of MAC_ACC module and generates signals ovf and sign. These signals are fed to the sigmoid_IP and the activation function generates a 8-bit output. Figure 6 shows the schematic view of Sigmoid_IP.

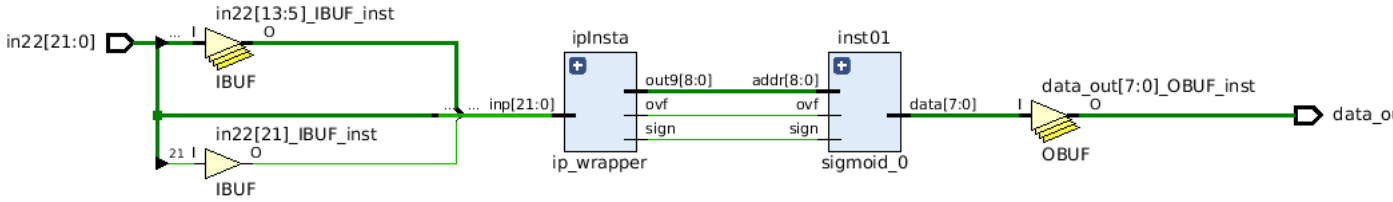

Figure 6: Sigmoid_IP Schematic

5. **node_func**
   Finally, we create a module to contain together the MAC_ACC and sigmoid_func modules together. We write a testbench to read the weights and pixels from the file. Then we provide these as input to the node_func module. As seen in schematic 7, Inside node_func module, MAC_ACC module takes pixel, weights, bias, clk and rst as input and outputs a 22 bit weighted sum. This sum is taken by sigmoidFunc as input and the sigmoid activation function gives final output for that particular hidden node.

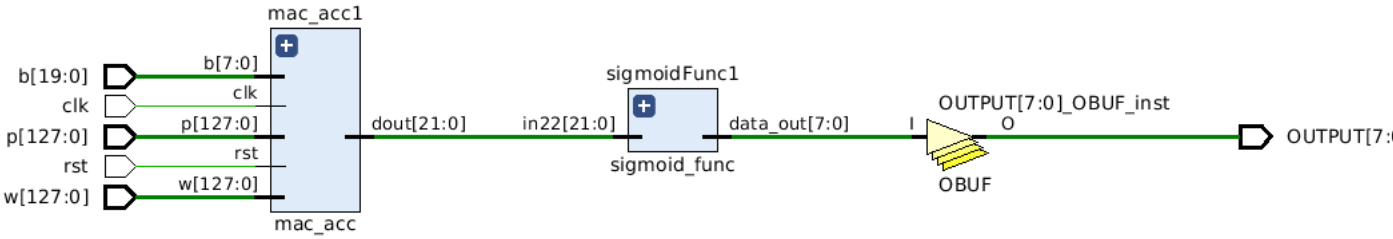

Figure 7: node_func schematic

On behavioral simulation, post-synthesis functional and post-synthesis timing simulation, we obtain the correct waveform and the final outputs are also correct. The two waveform are shown in figure 8, 9 and 10. The timing report in figure 11 also shows that no timing constraints are violated.

Figure 8: Behavioral Simulation

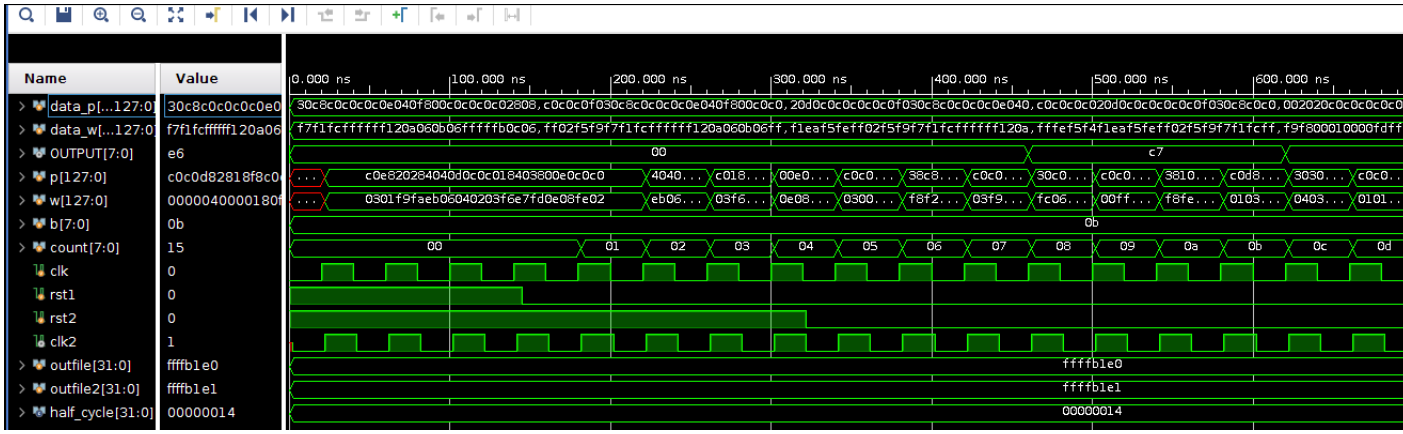

Figure 9: Post Synthesis Functional Simulation

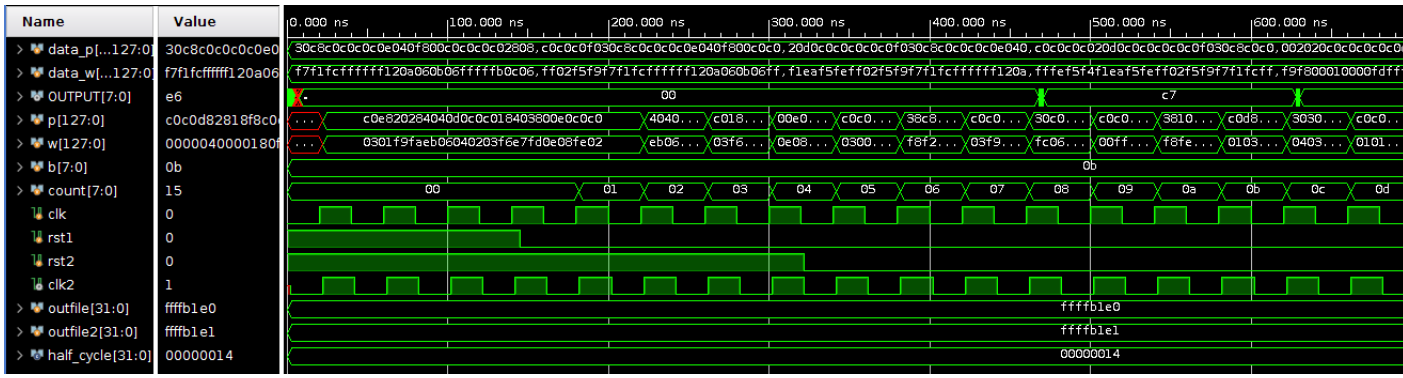

Figure 10: Post Synthesis Timing Simulation

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	12.601 ns	Worst Hold Slack (WHS):	0.154 ns	Worst Pulse Width Slack (WPWS):	9.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	216	Total Number of Endpoints:	216	Total Number of Endpoints:	456

All user specified timing constraints are met.

Figure 11: Timing Report