Synthesis Report

Mon Dec 4 16:58:47 2017

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Release 14.7 - xst P.20131013 (nt)
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--> Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 3.00 secs
Total CPU time to Xst completion: 2.71 secs

--> Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 3.00 secs
Total CPU time to Xst completion: 2.71 secs

--> Reading design: MIPS.prj
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=========================================================================
*                     Synthesis Options Summary                         *
=========================================================================
---- Source Parameters
Input File Name                    : "MIPS.prj"
Ignore Synthesis Constraint File   : NO
---- Target Parameters
Output File Name                   : "MIPS"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324
---- Source Options
Top Module Name                    : MIPS
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No
---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES
---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5
=========================================================================
=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Analyzing Verilog file "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\muxes.v" into library work
Parsing module .
Parsing module .
Parsing module .
Parsing module .
Parsing module .
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Parsing module .
Analyzing Verilog file "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\memory.v" into library work
Parsing module .
Parsing module .
Analyzing Verilog file "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\fetch.v" into library work
Parsing module .
Parsing module .
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Parsing module .
Analyzing Verilog file "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\excuetion.v" into library work
Parsing module .
Parsing module .
Analyzing Verilog file "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\decode.v" into library work
Parsing module .
Parsing module .
Parsing module .
Analyzing Verilog file "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" into library work
Parsing module .
=========================================================================
*                          HDL Elaboration                              *
=========================================================================
Elaborating module .
WARNING:HDLCompiler:1127 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" Line 118: Assignment to MEMWBrs ignored, since the identifier is never used
Elaborating module .
Elaborating module .
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Elaborating module .
Elaborating module .
Elaborating module .
Elaborating module .
WARNING:HDLCompiler:1127 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" Line 170: Assignment to shamt ignored, since the identifier is never used
Elaborating module .
Elaborating module .
Elaborating module .
Elaborating module .
WARNING:HDLCompiler:1127 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" Line 171: Assignment to zeroflag ignored, since the identifier is never used
Elaborating module .
Elaborating module .
Elaborating module .
Elaborating module .
=========================================================================
*                           HDL Synthesis                               *
=========================================================================
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v".
INFO:Xst:3210 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 170: Output port  of the instance  is unconnected or connected to loadless signal.
INFO:Xst:3210 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 170: Output port  of the instance  is unconnected or connected to loadless signal.
INFO:Xst:3210 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 170: Output port  of the instance  is unconnected or connected to loadless signal.
INFO:Xst:3210 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 170: Output port  of the instance  is unconnected or connected to loadless signal.
INFO:Xst:3210 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 171: Output port  of the instance  is unconnected or connected to loadless signal.
    Found 32-bit register for signal .
    Found 32-bit register for signal .
    Found 32-bit register for signal .
    Found 12-bit register for signal .
    Found 5-bit register for signal .
    Found 5-bit register for signal .
    Found 5-bit register for signal .
    Found 32-bit register for signal .
    Found 12-bit register for signal .
    Found 32-bit register for signal .
    Found 32-bit register for signal .
    Found 5-bit register for signal .
    Found 5-bit register for signal .
    Found 1-bit register for signal .
    Found 5-bit register for signal .
    Found 32-bit register for signal .
    Found 32-bit register for signal .
    Found 3-bit register for signal .
    Found 5-bit register for signal .
    Found 1-bit register for signal .
    Found 32-bit register for signal .
    Found 5-bit comparator equal for signal  created at line 148
    Found 5-bit comparator equal for signal  created at line 149
    Found 5-bit comparator equal for signal  created at line 151
    Found 5-bit comparator equal for signal  created at line 152
    Found 5-bit comparator equal for signal  created at line 154
    Found 1-bit comparator equal for signal  created at line 154
    Found 5-bit comparator equal for signal  created at line 156
    Found 5-bit comparator equal for signal  created at line 156
    Found 5-bit comparator equal for signal  created at line 157
    Found 5-bit comparator equal for signal  created at line 157
    Found 5-bit comparator equal for signal  created at line 158
    Found 5-bit comparator equal for signal  created at line 158
    Found 5-bit comparator equal for signal  created at line 163
    Found 5-bit comparator equal for signal  created at line 164
    Found 5-bit comparator equal for signal  created at line 166
    Found 5-bit comparator equal for signal  created at line 167
    Summary:
         inferred 352 D-type flip-flop(s).
         inferred  16 Comparator(s).
         inferred   4 Multiplexer(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\fetch.v".
    Summary:
         no macro.
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\fetch.v".
    Found 32-bit register for signal .
    Found 32-bit adder for signal  created at line 21.
    Found 32-bit adder for signal  created at line 29.
    Summary:
         inferred   1 Adder/Subtractor(s).
         inferred  32 D-type flip-flop(s).
         inferred   1 Multiplexer(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\fetch.v".
        MemDepth = 255
WARNING:Xst:647 - Input > is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block ar
WARNING:Xst:647 - Input > is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block ar
WARNING:Xst:653 - Signal  is used but never assigned. This sourceless signal will be automatically connected to value GND.
    Found 256x32-bit single-port Read Only RAM  for signal .
    Found 32-bit register for signal .
    Summary:
         inferred   1 RAM(s).
         inferred  32 D-type flip-flop(s).
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Unit  synthesized.
WARNING:Xst:2972 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\decode.v" line 231. All outputs of instance  of block  are unconnected in block . Underlying l
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\decode.v".
WARNING:Xst:653 - Signal  is used but never assigned. This sourceless signal will be automatically connected to value GND.
    Found 32-bit adder for signal  created at line 204.
    Summary:
         inferred   1 Adder/Subtractor(s).
         inferred   1 Multiplexer(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\decode.v".
WARNING:Xst:647 - Input  is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block anc
WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in
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WARNING:Xst:737 - Found 1-bit latch for signal >. Latches may be generated from incomplete case or if statements. We do not recommend the use of latches in
    Summary:
         inferred  12 Latch(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\decode.v".
        zero = 5'b00000
        at = 5'b00001
        v0 = 5'b00010
        v1 = 5'b00011
        a0 = 5'b00100
        a1 = 5'b00101
        a2 = 5'b00110
        a3 = 5'b00111
        t0 = 5'b01000
        t1 = 5'b01001
        t2 = 5'b01010
        t3 = 5'b01011
        t4 = 5'b01100
        t5 = 5'b01101
        t6 = 5'b01110
        t7 = 5'b01111
        s0 = 5'b10000
        s1 = 5'b10001
        s2 = 5'b10010
        s3 = 5'b10011
        s4 = 5'b10100
        s5 = 5'b10101
        s6 = 5'b10110
        s7 = 5'b10111
        t8 = 5'b11000
        t9 = 5'b11001
        k0 = 5'b11010
        k1 = 5'b11011
        gp = 5'b11100
        sp = 5'b11101
        fp = 5'b11110
        ra = 5'b11111
    Found 1-bit register for signal .
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    Found 32-bit adder for signal  created at line 67.
    Found 32-bit 32-to-1 multiplexer for signal  created at line 10.
    Found 32-bit 32-to-1 multiplexer for signal  created at line 11.
    Found 1-bit tristate buffer for signal  created at line 67
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    Found 1-bit tristate buffer for signal  created at line 67
    Summary:
         inferred   1 Adder/Subtractor(s).
         inferred 1024 D-type flip-flop(s).
         inferred   2 Multiplexer(s).
         inferred  64 Tristate(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\muxes.v".
    Found 32-bit 4-to-1 multiplexer for signal  created at line 11.
    Summary:
         inferred   1 Multiplexer(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\muxes.v".
    Summary:
         inferred   1 Multiplexer(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\excuetion.v".
    Summary:
         no macro.
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\muxes.v".
    Summary:
         inferred   1 Multiplexer(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\muxes.v".
    Summary:
         inferred   1 Multiplexer(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\excuetion.v".
    Found 32-bit subtractor for signal  created at line 14.
    Found 32-bit adder for signal  created at line 13.
    Found 32-bit shifter logical left for signal  created at line 17
    Found 32-bit shifter logical right for signal  created at line 18
    Found 32-bit shifter arithmetic right for signal  created at line 19
    Found 32-bit 13-to-1 multiplexer for signal  created at line 3.
    Found 32-bit comparator greater for signal  created at line 20
    Found 32-bit comparator greater for signal  created at line 21
    Found 1-bit comparator equal for signal  created at line 27
    Found 1-bit comparator not equal for signal  created at line 27
    Summary:
         inferred   2 Adder/Subtractor(s).
         inferred   4 Comparator(s).
         inferred  13 Multiplexer(s).
         inferred   3 Combinational logic shifter(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\memory.v".
WARNING:Xst:647 - Input  is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block anc
    Summary:
         no macro.
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\memory.v".
        MemDepth = 255
WARNING:Xst:647 - Input > is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block ar
    Found 256x32-bit single-port RAM  for signal .
    Found 32-bit register for signal .
    Summary:
         inferred   1 RAM(s).
         inferred  32 D-type flip-flop(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\muxes.v".
```

```
    Summary:
         inferred   2 Multiplexer(s).
Unit  synthesized.
Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\muxes.v".
    Summary:
         inferred   1 Multiplexer(s).
Unit  synthesized.
=========================================================================
HDL Synthesis Report
Macro Statistics
# RAMs                                                 : 2
 256x32-bit single-port RAM                            : 1
 256x32-bit single-port Read Only RAM                  : 1
# Adders/Subtractors                                   : 5
 32-bit adder                                          : 4
 32-bit subtractor                                     : 1
# Registers                                            : 56
 1-bit register                                        : 2
 12-bit register                                       : 2
 3-bit register                                        : 1
 32-bit register                                       : 44
 5-bit register                                        : 7
# Latches                                              : 12
 1-bit latch                                           : 12
# Comparators                                          : 20
 1-bit comparator equal                                : 2
 1-bit comparator not equal                            : 1
 32-bit comparator greater                             : 2
 5-bit comparator equal                                : 15
# Multiplexers                                         : 32
 12-bit 2-to-1 multiplexer                             : 1
 2-bit 2-to-1 multiplexer                              : 4
 32-bit 2-to-1 multiplexer                             : 21
 32-bit 32-to-1 multiplexer                            : 2
 32-bit 4-to-1 multiplexer                             : 3
 5-bit 2-to-1 multiplexer                              : 1
# Logic shifters                                       : 3
 32-bit shifter arithmetic right                       : 1
 32-bit shifter logical left                           : 1
 32-bit shifter logical right                          : 1
# Tristates                                            : 64
 1-bit tristate buffer                                 : 64
# Xors                                                 : 1
 32-bit xor2                                           : 1
=========================================================================
INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic operations in this design can share the same physical resources for reduc
=========================================================================
*                        Advanced HDL Synthesis                          *
=========================================================================
INFO:Xst:2261 - The FF/Latch  in Unit  is equivalent to the following FF/Latch, which will be removed :
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization process.
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WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization process.
WARNING:Xst:2677 - Node  of sequential type is unconnected in block .
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WARNING:Xst:2677 - Node  of sequential type is unconnected in block .
WARNING:Xst:2677 - Node  of sequential type is unconnected in block .
Synthesizing (advanced) Unit .
INFO:Xst:3226 - The RAM  will be implemented as a BLOCK RAM, absorbing the following register(s):
    -----------------------------------------------------------------------
    | ram_type           | Block                                |          |
    -----------------------------------------------------------------------
    | Port A                                                               |
    |     aspect ratio   | 256-word x 32-bit                    |          |
    |     mode           | write-first                          |          |
    |     clkA           | connected to signal            | rise     |
    |     weA            | connected to signal            | high     |
    |     addrA          | connected to signal > |          |
    |     diA            | connected to signal            |          |
    |     doA            | connected to signal         |          |
    |     doregrstA      | connected to internal node          | high     |
    | reset value        | 00000000000000000000000000000000                |
    -----------------------------------------------------------------------
    | optimization       | speed                                |          |
    -----------------------------------------------------------------------
```

```
Unit  synthesized (advanced).
WARNING:Xst:2677 - Node  of sequential type is unconnected in block .
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WARNING:Xst:2677 - Node  of sequential type is unconnected in block .
=========================================================================
Advanced HDL Synthesis Report
Macro Statistics
# RAMs                                                 : 2
 256x32-bit single-port block Read Only RAM            : 1
 256x32-bit single-port distributed RAM                : 1
# Adders/Subtractors                                   : 5
 32-bit adder                                          : 4
 32-bit subtractor                                     : 1
# Registers                                            : 1398
 Flip-Flops                                            : 1398
# Comparators                                          : 20
 1-bit comparator equal                                : 2
 1-bit comparator not equal                            : 1
 32-bit comparator greater                             : 2
 5-bit comparator equal                                : 15
# Multiplexers                                         : 125
 1-bit 2-to-1 multiplexer                              : 32
 1-bit 32-to-1 multiplexer                             : 64
 12-bit 2-to-1 multiplexer                             : 1
 2-bit 2-to-1 multiplexer                              : 4
 32-bit 2-to-1 multiplexer                             : 20
 32-bit 4-to-1 multiplexer                             : 3
 5-bit 2-to-1 multiplexer                              : 1
# Logic shifters                                       : 3
 32-bit shifter arithmetic right                       : 1
 32-bit shifter logical left                           : 1
 32-bit shifter logical right                          : 1
# Xors                                                 : 1
 32-bit xor2                                           : 1
=========================================================================
=========================================================================
*                          Low Level Synthesis                          *
=========================================================================
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization process.
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WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization process.
INFO:Xst:2261 - The FF/Latch  in Unit  is equivalent to the following FF/Latch, which will be removed :
INFO:Xst:2261 - The FF/Latch  in Unit  is equivalent to the following FF/Latch, which will be removed :
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INFO:Xst:2261 - The FF/Latch  in Unit  is equivalent to the following FF/Latch, which will be removed :
INFO:Xst:2261 - The FF/Latch  in Unit  is equivalent to the following 17 FFs/Latches, which will be removed :
WARNING:Xst:2170 - Unit MIPS : the following signal(s) form a combinatorial loop: ControlLines[2]_GND_1_o_AND_21_o, ForwardE<0>, ForwardD<0>, ControlLines[2
Optimizing unit  ...
Optimizing unit  ...
Optimizing unit  ...
Optimizing unit  ...
WARNING:Xst:1710 - FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during the optimization process.
WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during
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WARNING:Xst:1895 - Due to other FF/Latch trimming, FF/Latch  (without init value) has a constant value of 0 in block . This FF/Latch will be trimmed during
Optimizing unit  ...
WARNING:Xst:2677 - Node  of sequential type is unconnected in block .
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INFO:Xst:2261 - The FF/Latch  in Unit  is equivalent to the following FF/Latch, which will be removed :
INFO:Xst:2261 - The FF/Latch  in Unit  is equivalent to the following FF/Latch, which will be removed :
INFO:Xst:2261 - The FF/Latch  in Unit  is equivalent to the following FF/Latch, which will be removed :
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block MIPS, actual ratio is 4.
Final Macro Processing ...
=========================================================================
Final Register Report
Macro Statistics
# Registers                                            : 1262
 Flip-Flops                                            : 1262
=========================================================================
=========================================================================
*                            Partition Report                           *
=========================================================================
Partition Implementation Status
-------------------------------
  No Partitions were found in this design.
-------------------------------
=========================================================================
*                             Design Summary                            *
=========================================================================
Top Level Output File Name         : MIPS.ngc
Primitive and Black Box Usage:
------------------------------
# BELS                             : 1769
#      GND                         : 1
#      INV                         : 10
#      LUT2                        : 49
#      LUT3                        : 128
#      LUT4                        : 109
#      LUT5                        : 207
#      LUT6                        : 1005
#      MUXCY                       : 110
#      MUXF7                       : 69
#      VCC                         : 1
#      XORCY                       : 80
# FlipFlops/Latches                : 1273
#      FD                          : 254
#      FDE                         : 16
#      FDE_1                       : 992
#      LD                          : 11
# RAMS                             : 33
#      RAM256X1S                   : 32
#      RAMB18E1                    : 1
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 128
#      OBUF                        : 128
Device utilization summary:
---------------------------
Selected Device : 7a100tcsg324-3
```

```
Slice Logic Utilization:
 Number of Slice Registers:            1273  out of  126800     1%
 Number of Slice LUTs:                 1636  out of  63400     2%
    Number used as Logic:              1508  out of  63400     2%
    Number used as Memory:              128  out of  19000     0%
       Number used as RAM:              128
Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:   2712
   Number with an unused Flip Flop:    1439  out of   2712    53%
   Number with an unused LUT:          1076  out of   2712    39%
   Number of fully used LUT-FF pairs:   197  out of   2712     7%
   Number of unique control sets:        35
IO Utilization:
 Number of IOs:                        129
 Number of bonded IOBs:                129  out of    210    61%
Specific Feature Utilization:
 Number of Block RAM/FIFO:               1  out of    135     0%
    Number using Block RAM only:         1
 Number of BUFG/BUFGCTRLs:               1  out of     32     3%
---------------------------
Partition Resource Summary:
---------------------------
  No Partitions were found in this design.
---------------------------
=========================================================================
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.
Clock Information:
------------------
-----------------------------------------------------------------------------------+--------------------------------+-------+
Clock Signal                                                                       | Clock buffer(FF name)          | Load  |
-----------------------------------------------------------------------------------+--------------------------------+-------+
Clk                                                                                | BUFGP                          | 1295  |
Dec/CU/Opcode[5]_GND_6_o_Select_37_o(Dec/CU/Opcode[5]_GND_6_o_Select_37_o4:O)| NONE(*)(Dec/CU/ControlLines_0)| 11    |
-----------------------------------------------------------------------------------+--------------------------------+-------+
(*) This 1 clock signal(s) are generated by combinatorial logic,
and XST is not able to identify which are the primary clock signals.
Please use the CLOCK_SIGNAL constraint to specify the clock signal(s) generated by combinatorial logic.
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources. Please use the buffer_type constraint in c
Asynchronous Control Signals Information:
-----------------------------------------
----------------------------------+----------------------------------------+-------+
Control Signal                    | Buffer(FF name)                        | Load  |
----------------------------------+----------------------------------------+-------+
N1(XST_GND:G)                     | NONE(Fetch/MyInst/Mram_InstructionMem1)| 2     |
----------------------------------+----------------------------------------+-------+
Timing Summary:
---------------
Speed Grade: -3
   Minimum period: 6.349ns (Maximum Frequency: 157.515MHz)
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: 5.893ns
   Maximum combinational path delay: No path found
Timing Details:
---------------
All values displayed in nanoseconds (ns)
=========================================================================
Timing constraint: Default period analysis for Clock 'Clk'
  Clock period: 6.349ns (frequency: 157.515MHz)
  Total number of paths / destination ports: 1511362 / 2610
-------------------------------------------------------------------------
Delay:               3.174ns (Levels of Logic = 12)
  Source:            Dec/RegFile/Registers_ff_925_2 (FF)
  Destination:       Fetch/PC1/OutputAddress_9 (FF)
  Source Clock:      Clk falling
  Destination Clock: Clk rising
  Data Path: Dec/RegFile/Registers_ff_925_2 to Fetch/PC1/OutputAddress_9
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDE_1:C->Q            2   0.364   0.516  Dec/RegFile/Registers_ff_925_2 (Dec/RegFile/Registers_ff_925_2)
     LUT5:I2->O            1   0.097   0.556  Dec/RegFile/mux22_9 (Dec/RegFile/mux22_9)
     LUT6:I2->O            1   0.097   0.000  Dec/RegFile/mux22_3 (Dec/RegFile/mux22_3)
     MUXF7:I1->O           2   0.279   0.299  Dec/RegFile/mux22_2_f7 (Dec/RegFile/ReadData1<2>1)
     LUT6:I5->O            1   0.097   0.000  Fetch/PC1/Mmux_OutputAddress[31]_InputAddress[31]_mux_6_OUT_rs_lut<2> (Fetch/PC1/Mmux_OutputAddress[31]_InputA
     MUXCY:S->O            1   0.353   0.000  Fetch/PC1/Mmux_OutputAddress[31]_InputAddress[31]_mux_6_OUT_rs_cy<2> (Fetch/PC1/Mmux_OutputAddress[31]_InputAc
     MUXCY:CI->O           1   0.023   0.000  Fetch/PC1/Mmux_OutputAddress[31]_InputAddress[31]_mux_6_OUT_rs_cy<3> (Fetch/PC1/Mmux_OutputAddress[31]_InputAc
     MUXCY:CI->O           1   0.023   0.000  Fetch/PC1/Mmux_OutputAddress[31]_InputAddress[31]_mux_6_OUT_rs_cy<4> (Fetch/PC1/Mmux_OutputAddress[31]_InputAc
     MUXCY:CI->O           1   0.023   0.000  Fetch/PC1/Mmux_OutputAddress[31]_InputAddress[31]_mux_6_OUT_rs_cy<5> (Fetch/PC1/Mmux_OutputAddress[31]_InputAc
     MUXCY:CI->O           1   0.023   0.000  Fetch/PC1/Mmux_OutputAddress[31]_InputAddress[31]_mux_6_OUT_rs_cy<6> (Fetch/PC1/Mmux_OutputAddress[31]_InputAc
     MUXCY:CI->O           1   0.023   0.000  Fetch/PC1/Mmux_OutputAddress[31]_InputAddress[31]_mux_6_OUT_rs_cy<7> (Fetch/PC1/Mmux_OutputAddress[31]_InputAc
     MUXCY:CI->O           0   0.023   0.000  Fetch/PC1/Mmux_OutputAddress[31]_InputAddress[31]_mux_6_OUT_rs_cy<8> (Fetch/PC1/Mmux_OutputAddress[31]_InputAc
     XORCY:CI->O           1   0.370   0.000  Fetch/PC1/Mmux_OutputAddress[31]_InputAddress[31]_mux_6_OUT_rs_xor<9> (Fetch/PC1/OutputAddress[31]_InputAddres
     FDE:D                     0.008          Fetch/PC1/OutputAddress_9
    ----------------------------------------
    Total                      3.174ns (1.803ns logic, 1.371ns route)
                                       (56.8% logic, 43.2% route)
=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'Clk'
  Total number of paths / destination ports: 1364364 / 128
-------------------------------------------------------------------------
Offset:              5.893ns (Levels of Logic = 29)
  Source:            IDEXrs_4 (FF)
  Destination:       ALUresult<31> (PAD)
  Source Clock:      Clk rising
  Data Path: IDEXrs_4 to ALUresult<31>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               3   0.361   0.693  IDEXrs_4 (IDEXrs_4)
     LUT5:I0->O            1   0.097   0.295  GND_1_o_EXEMEMWriteReg[4]_AND_4_o1 (GND_1_o_EXEMEMWriteReg[4]_AND_4_o1)
     LUT3:I2->O           13   0.097   0.435  GND_1_o_EXEMEMWriteReg[4]_AND_4_o2 (GND_1_o_EXEMEMWriteReg[4]_AND_4_o2)
     LUT6:I4->O           20   0.097   0.383  GND_1_o_EXEMEMWriteReg[4]_AND_4_o3 (GND_1_o_EXEMEMWriteReg[4]_AND_4_o)
     LUT6:I5->O            8   0.097   0.328  ForwardAmux/Mmux_WriteData4 (ForwardAout<12>)
     LUT4:I3->O            1   0.097   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_lut<12> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_lut<12>)
     MUXCY:S->O            1   0.353   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<12> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<12>)
     MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<13> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<13>)
     MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<14> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<14>)
```

```
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<15> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<15>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<16> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<16>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<17> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<17>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<18> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<18>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<19> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<19>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<20> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<20>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<21> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<21>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<22> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<22>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<23> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<23>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<24> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<24>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<25> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<25>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<26> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<26>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<27> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<27>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<28> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<28>)
    MUXCY:CI->O           1   0.023   0.000  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<29> (Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_cy<29>)
    XORCY:CI->O           2   0.370   0.299  Exexcution/MyALU/Msub_A[31]_B[31]_sub_4_OUT_xor<30> (Exexcution/MyALU/A[31]_B[31]_sub_4_OUT<30>)
    LUT6:I5->O            1   0.097   0.000  Exexcution/MyALU/Mmux_Result1_rs_lut<30> (Exexcution/MyALU/Mmux_Result1_rs_lut<30>)
    MUXCY:S->O            0   0.353   0.000  Exexcution/MyALU/Mmux_Result1_rs_cy<30> (Exexcution/MyALU/Mmux_Result1_rs_cy<30>)
    XORCY:CI->O           2   0.370   0.299  Exexcution/MyALU/Mmux_Result1_rs_xor<31> (Exexcution/MyALU/Mmux_Result1_split<31>)
    LUT6:I5->O            2   0.097   0.283  Exexcution/MyALU/Mmux_Result12487 (ALUresult_31_OBUF)
    OBUF:I->O                 0.000          ALUresult_31_OBUF (ALUresult<31>)
    ----------------------------------------
    Total                     5.893ns (2.877ns logic, 3.016ns route)
                                      (48.8% logic, 51.2% route)
==========================================================================
Cross Clock Domains Report:
--------------------------
Clock to Setup on destination clock Clk
---------------------------------+---------+---------+---------+---------+
                                 | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock                     |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------------------------+---------+---------+---------+---------+
Clk                              |    5.618|    3.174|    2.554|         |
Dec/CU/Opcode[5]_GND_6_o_Select_37_o|         |    4.175|         |         |
---------------------------------+---------+---------+---------+---------+
Clock to Setup on destination clock Dec/CU/Opcode[5]_GND_6_o_Select_37_o
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
Clk            |         |         |    3.237|         |
---------------+---------+---------+---------+---------+
==========================================================================
Total REAL time to Xst completion: 25.00 secs
Total CPU time to Xst completion: 25.26 secs

-->
Total memory usage is 335132 kilobytes
Number of errors   :    0 (   0 filtered)
Number of warnings :  188 (   0 filtered)
Number of infos    :   18 (   0 filtered)
```