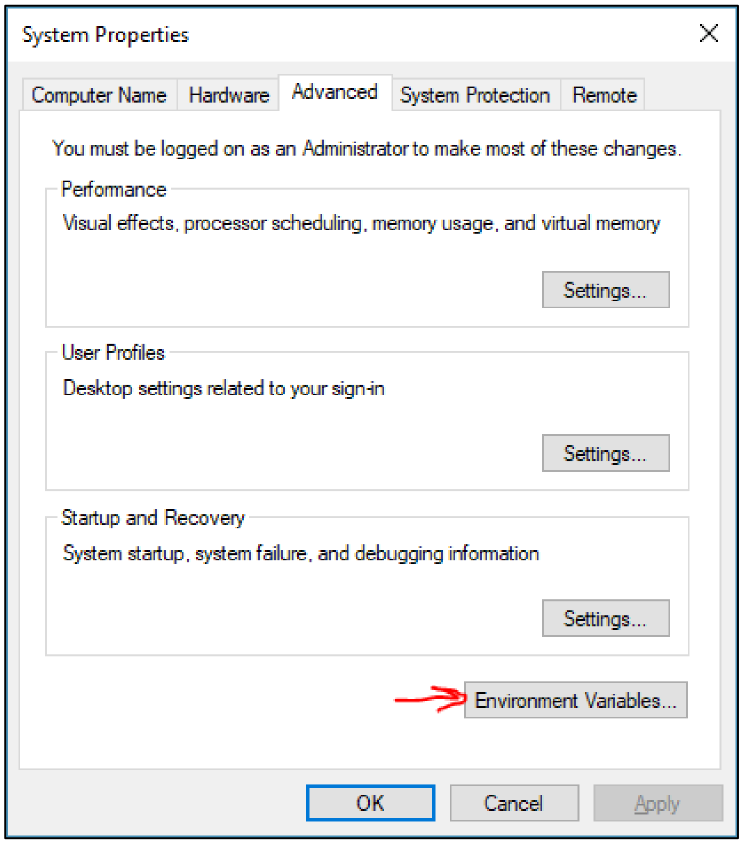
Preface:

This GUI is used for creating input files for our MIPS Verilog project such as instruction memory, data memory and register file. The app is integrated with iVerilog to simulate the Verilog modules and show output results. It is also can be used on Windows and Linux operating systems.

Prerequisites:

For Windows:

- Python 2.7: Please note that it won't work with Python 3
- iVeriliog 10.0 or later: After this modify the environment variables by selecting **System** from the **Control Panel**, selecting **Advanced system settings**, and clicking **Environment Variables**.
  Edit **Path** system variable by creating new system variable with iVerilog path for example, "C:\iverilog\bin" without quotations.

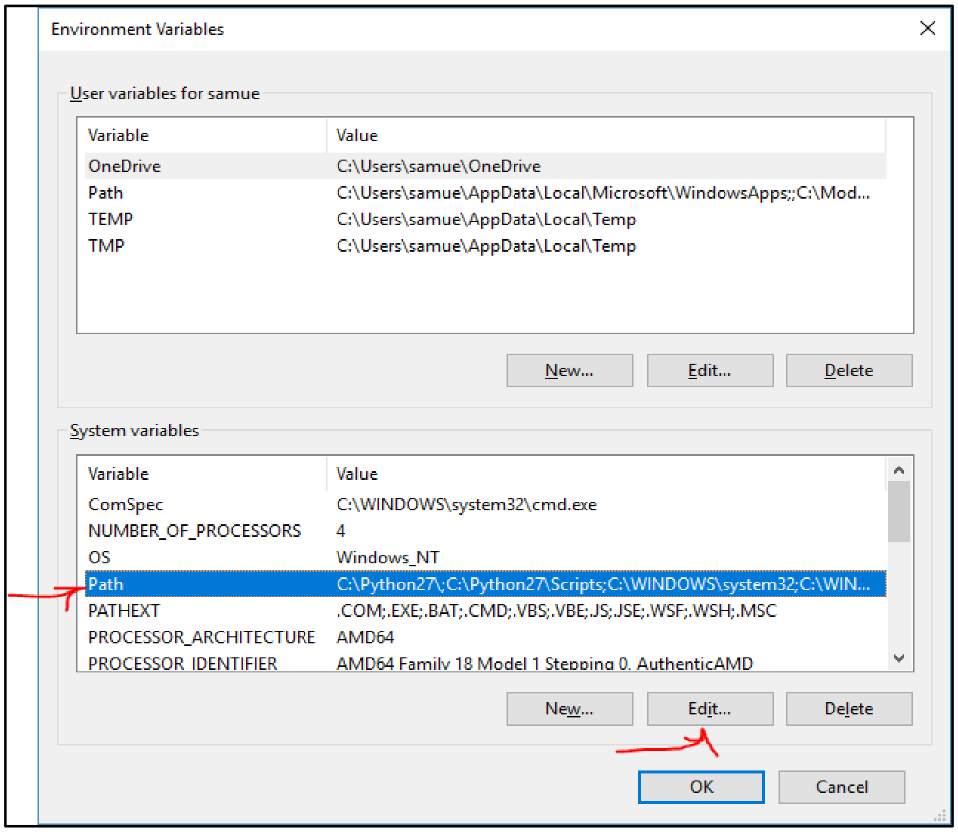

System Properties

You must be logged on as an Administrator to make most of these changes.

Performance
Visual effects, processor scheduling, memory usage, and virtual memory

User Profiles
Desktop settings related to your sign-in

Startup and Recovery
System startup, system failure, and debugging information



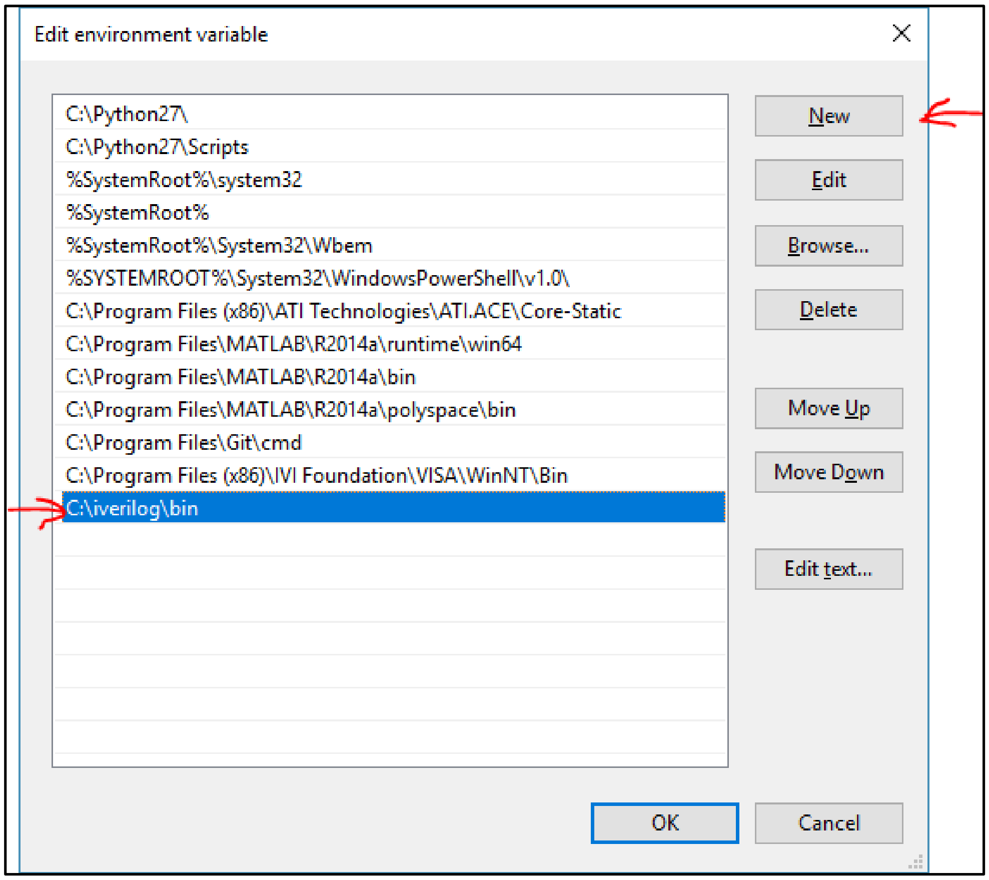
Environment Variables

User variables for samue

Variable	Value
OneDrive	C:\Users\samue\OneDrive
Path	C:\Users\samue\AppData\Local\Microsoft\WindowsApps;;C:\Mod...
TEMP	C:\Users\samue\AppData\Local\Temp
TMP	C:\Users\samue\AppData\Local\Temp

System variables

Variable	Value
ComSpec	C:\WINDOWS\system32\cmd.exe
NUMBER_OF_PROCESSORS	4
OS	Windows_NT
Path	C:\Python27\;C:\Python27\Scripts;C:\WINDOWS\system32;C:\WIN...
PATHEXT	.COM;.EXE;.BAT;.CMD;.VBS;.VBE;.JS;.JSE;.WSF;.WSH;.MSC
PROCESSOR_ARCHITECTURE	AMD64
PROCESSOR_IDENTIFIER	AMD64 Family 18 Model 1 Stepping 0, AuthenticAMD



Edit environment variable

```
C:\Python27\
C:\Python27\Scripts
%SystemRoot%\system32
%SystemRoot%
%SystemRoot%\System32\Wbem
%SYSTEMROOT%\System32\WindowsPowerShell\v1.0\
C:\Program Files (x86)\ATI Technologies\ATI.ACE\Core-Static
C:\Program Files\MATLAB\R2014a\runtime\win64
C:\Program Files\MATLAB\R2014a\bin
C:\Program Files\MATLAB\R2014a\polyspace\bin
C:\Program Files\Git\cmd
C:\Program Files (x86)\IVI Foundation\VISA\WinNT\Bin
C:\iverilog\bin
```

To run: Double click on **assembler.py** or using Windows power shell command python2 assembler.py

For Linux:

- Python 2.7:
  $ sudo apt-get install python2.7
  Please note that it won't work with Python 3
- iVeriliog :
  $sudo apt-get install iverilog

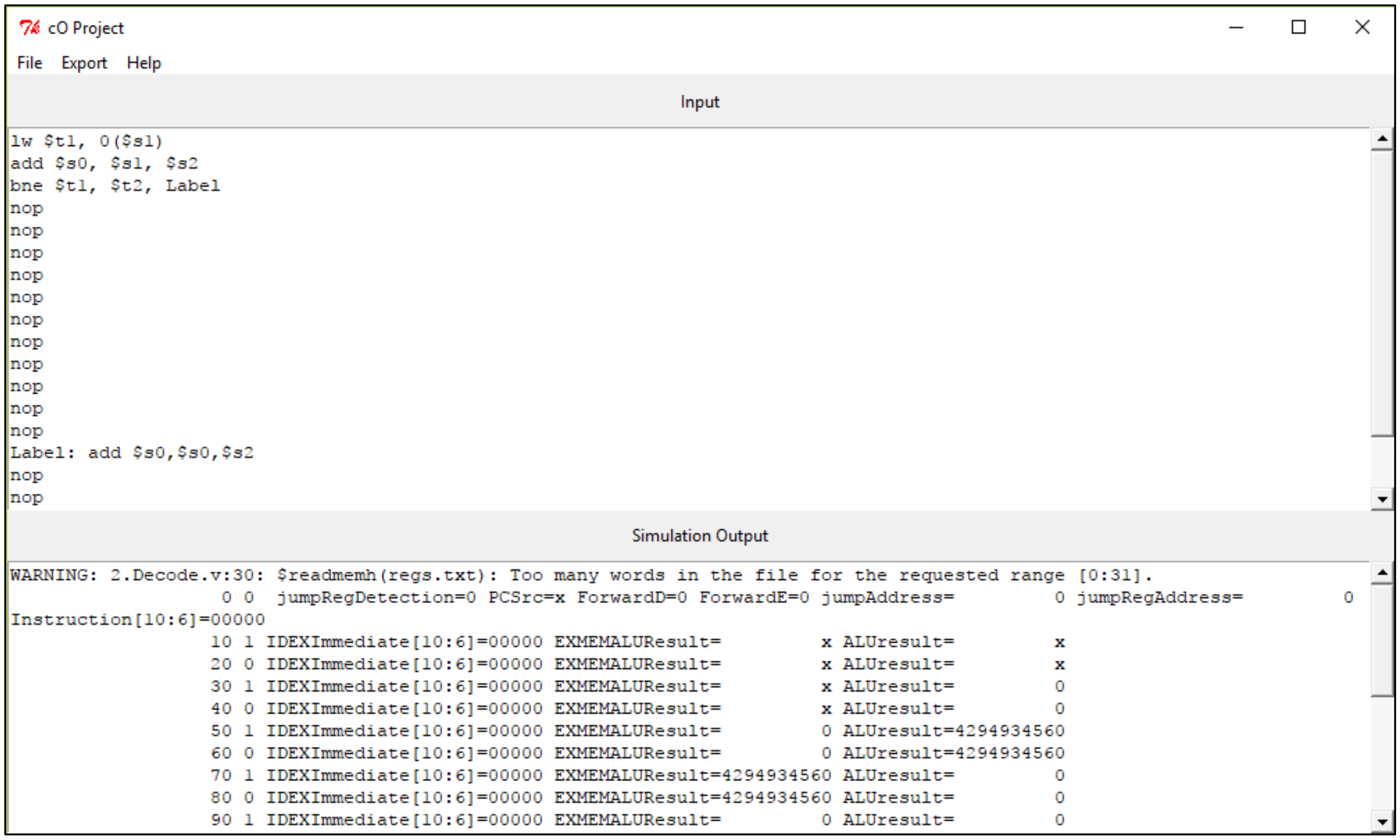
To run:

$ python2 assembler.py

Usage:

- put the Verilog project files "*.v" files in the path of GUI
- Open an existing *.asm or *.txt file or use the input field editor.
- Then from **Export** menu:
- **Instruction memory** that will create a inst_mem.txt file with instructions machine code.
- **Register file** that will create a regs.txt file contain Regfile data.
- **Data memory** that will create a data_mem.txt file with contain DataMem data.
- The previous files are in hexadecimal and will be created in the same path of *.v files, please don't rename any of the as they will be used in Verilog modules
- From **File** menu -> **Execute** to start simulation and monitor the simulation outputs.
- You can also export the machine code to other destinations from **Export -> Machine code**.
- You can also save the input field contents in *.asm and *.txt extensions.

The expected output after enter an assembly code followed by filling the memories files will be:



```
lw $t1, 0($s1)
add $s0, $s1, $s2
bne $t1, $t2, Label
nop
nop
nop
nop
nop
nop
nop
nop
nop
nop
nop
Label: add $s0,$s0,$s2
nop
nop
```

```
WARNING: 2.Decode.v:30: $readmemh(regs.txt): Too many words in the file for the requested range [0:31].
                   0 0  jumpRegDetection=0 PCSrc=x ForwardD=0 ForwardE=0 jumpAddress=         0 jumpRegAddress=         0
Instruction[10:6]=00000
                  10 1  IDEXImmediate[10:6]=00000 EXMEMALUResult=         x ALUresult=         x
                  20 0  IDEXImmediate[10:6]=00000 EXMEMALUResult=         x ALUresult=         x
                  30 1  IDEXImmediate[10:6]=00000 EXMEMALUResult=         x ALUresult=         0
                  40 0  IDEXImmediate[10:6]=00000 EXMEMALUResult=         x ALUresult=         0
                  50 1  IDEXImmediate[10:6]=00000 EXMEMALUResult=         0 ALUresult=4294934560
                  60 0  IDEXImmediate[10:6]=00000 EXMEMALUResult=         0 ALUresult=4294934560
                  70 1  IDEXImmediate[10:6]=00000 EXMEMALUResult=4294934560 ALUresult=         0
                  80 0  IDEXImmediate[10:6]=00000 EXMEMALUResult=4294934560 ALUresult=         0
                  90 1  IDEXImmediate[10:6]=00000 EXMEMALUResult=         0 ALUresult=         0
```