Synthesis Report

Mon Dec 4 15:09:03 2017

```
Release 14.7 - xst P.20131013 (nt)
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--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.10 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.10 secs

--> Reading design: MIPS_TB.prj

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=========================================================================
*                     Synthesis Options Summary                         *
=========================================================================
---- Source Parameters
Input File Name                    : "MIPS_TB.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "MIPS_TB"
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324

---- Source Options
Top Module Name                    : MIPS_TB
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                            HDL Parsing                                *
=========================================================================
Analyzing Verilog file "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\muxes.v" into library work
Parsing module .
Parsing module .
Parsing module .
Parsing module .
Parsing module .
Parsing module .
Parsing module .
Analyzing Verilog file "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\memory.v" into library work
Parsing module .
Parsing module .
Analyzing Verilog file "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\fetch.v" into library work
Parsing module .
Parsing module .
Parsing module .
Analyzing Verilog file "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\excuetion.v" into library work
Parsing module .
Parsing module .
Analyzing Verilog file "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\decode.v" into library work
Parsing module .
Parsing module .
Parsing module .
Analyzing Verilog file "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" into library work
Parsing module .
Parsing module .
```

```
=========================================================================
*                         HDL Elaboration                               *
=========================================================================

Elaborating module .

Elaborating module .
WARNING:HDLCompiler:1127 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" Line 118: Assignment to MEMWBrs ignored, since the identifier is never used

Elaborating module .

Elaborating module .

Elaborating module .

Elaborating module .

Elaborating module .

Elaborating module .

Elaborating module .

Elaborating module .
WARNING:HDLCompiler:1127 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" Line 170: Assignment to shamt ignored, since the identifier is never used

Elaborating module .

Elaborating module .

Elaborating module .

Elaborating module .
WARNING:HDLCompiler:1127 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" Line 171: Assignment to zeroflag ignored, since the identifier is never used

Elaborating module .

Elaborating module .

Elaborating module .

Elaborating module .
WARNING:Xst:2972 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 169. All outputs of instance  of block  are unconnected in block . Underlying logic will be removed.
WARNING:Xst:2972 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 170. All outputs of instance  of block  are unconnected in block . Underlying logic will be removed.
WARNING:Xst:2972 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 171. All outputs of instance  of block  are unconnected in block . Underlying logic will be removed.
WARNING:Xst:2972 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 172. All outputs of instance  of block  are unconnected in block . Underlying logic will be removed.
WARNING:Xst:2972 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 174. All outputs of instance  of block  are unconnected in block . Underlying logic will be removed.
WARNING:Xst:2972 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 176. All outputs of instance  of block  are unconnected in block . Underlying logic will be removed.
WARNING:Xst:2972 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 177. All outputs of instance  of block  are unconnected in block . Underlying logic will be removed.
WARNING:Xst:2972 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 178. All outputs of instance  of block  are unconnected in block . Underlying logic will be removed.
WARNING:Xst:2972 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 180. All outputs of instance  of block  are unconnected in block . Underlying logic will be removed.
WARNING:Xst:2972 - "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v" line 193. All outputs of instance  of block  are unconnected in block . Underlying logic will be removed.

=========================================================================
*                           HDL Synthesis                               *
=========================================================================

Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\mips.v".
    Summary:
        no macro.
Unit  synthesized.

Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\fetch.v".
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
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    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Summary:
        inferred  32 D-type flip-flop(s).
Unit  synthesized.

Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\fetch.v".
        MemDepth = 255
WARNING:Xst:647 - Input > is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.
WARNING:Xst:647 - Input > is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.
WARNING:Xst:653 - Signal  is used but never assigned. This sourceless signal will be automatically connected to value GND.
    Found 256x32-bit single-port Read Only RAM  for signal .
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
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    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
```

```
    Found 1-bit register for signal >.
    Summary:
        inferred   1 RAM(s).
        inferred  32 D-type flip-flop(s).
Unit  synthesized.

Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\decode.v".
WARNING:Xst:647 - Input  is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.
    Summary:
        no macro.
Unit  synthesized.

Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\decode.v".
        zero = 5'b00000
        at = 5'b00001
        v0 = 5'b00010
        v1 = 5'b00011
        a0 = 5'b00100
        a1 = 5'b00101
        a2 = 5'b00110
        a3 = 5'b00111
        t0 = 5'b01000
        t1 = 5'b01001
        t2 = 5'b01010
        t3 = 5'b01011
        t4 = 5'b01100
        t5 = 5'b01101
        t6 = 5'b01110
        t7 = 5'b01111
        s0 = 5'b10000
        s1 = 5'b10001
        s2 = 5'b10010
        s3 = 5'b10011
        s4 = 5'b10100
        s5 = 5'b10101
        s6 = 5'b10110
        s7 = 5'b10111
        t8 = 5'b11000
        t9 = 5'b11001
        k0 = 5'b11010
        k1 = 5'b11011
        gp = 5'b11100
        sp = 5'b11101
        fp = 5'b11110
        ra = 5'b11111
    Summary:
        no macro.
Unit  synthesized.

Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\muxes.v".
    Summary:
        no macro.
Unit  synthesized.

Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\muxes.v".
    Summary:
        no macro.
Unit  synthesized.

Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\muxes.v".
    Summary:
        no macro.
Unit  synthesized.

Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\muxes.v".
    Summary:
        no macro.
Unit  synthesized.

Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\excuetion.v".
    Summary:
        no macro.
Unit  synthesized.

Synthesizing Unit .
    Related source file is "C:\Users\Diaa_Ahmed\Documents\xlinx\mips1\memory.v".
        MemDepth = 255
WARNING:Xst:647 - Input > is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.
    Found 256x32-bit single-port RAM  for signal .
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
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    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Found 1-bit register for signal >.
    Summary:
        inferred   1 RAM(s).
        inferred  32 D-type flip-flop(s).
Unit  synthesized.

=========================================================================
HDL Synthesis Report

Found no macro
=========================================================================

=========================================================================
*                        Advanced HDL Synthesis                         *
=========================================================================


=========================================================================
Advanced HDL Synthesis Report

Found no macro
=========================================================================
```

```
=========================================================================
*                      Low Level Synthesis                              *
=========================================================================

Optimizing unit  ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block MIPS_TB, actual ratio is 0.

Final Macro Processing ...

=========================================================================
Final Register Report

Found no macro
=========================================================================

=========================================================================
*                         Partition Report                              *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
*                           Design Summary                              *
=========================================================================

Top Level Output File Name         : MIPS_TB.ngc

Primitive and Black Box Usage:
------------------------------

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:      0
   Number with an unused Flip Flop:       0  out of      0
   Number with an unused LUT:             0  out of      0
   Number of fully used LUT-FF pairs:     0  out of      0
   Number of unique control sets:         0

IO Utilization:
 Number of IOs:                           0
 Number of bonded IOBs:                   0  out of    210     0%

Specific Feature Utilization:

----------------------------
Partition Resource Summary:
----------------------------

  No Partitions were found in this design.

----------------------------


=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
-----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================

Cross Clock Domains Report:
---------------------------

=========================================================================


Total REAL time to Xst completion: 7.00 secs
Total CPU time to Xst completion: 7.10 secs

-->

Total memory usage is 370524 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :   18 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```