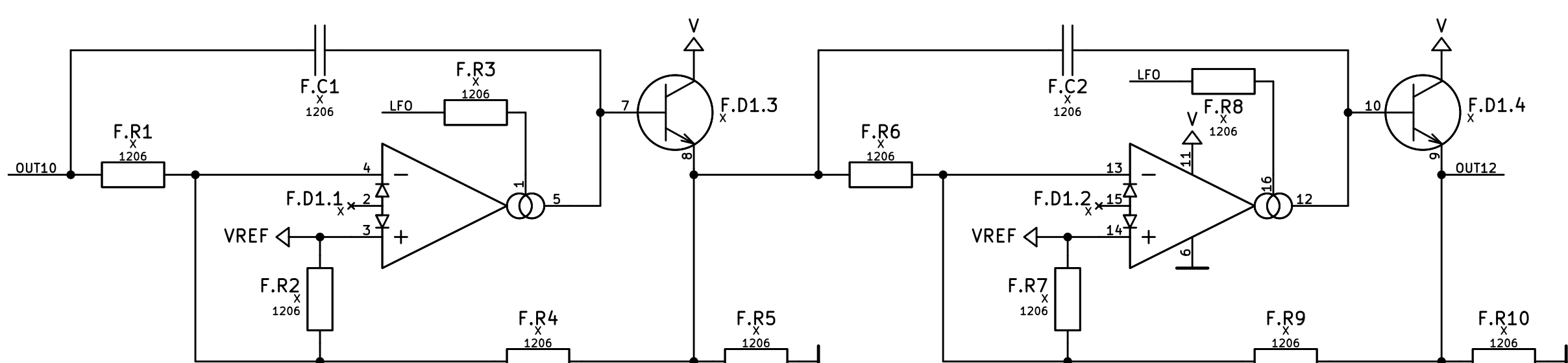
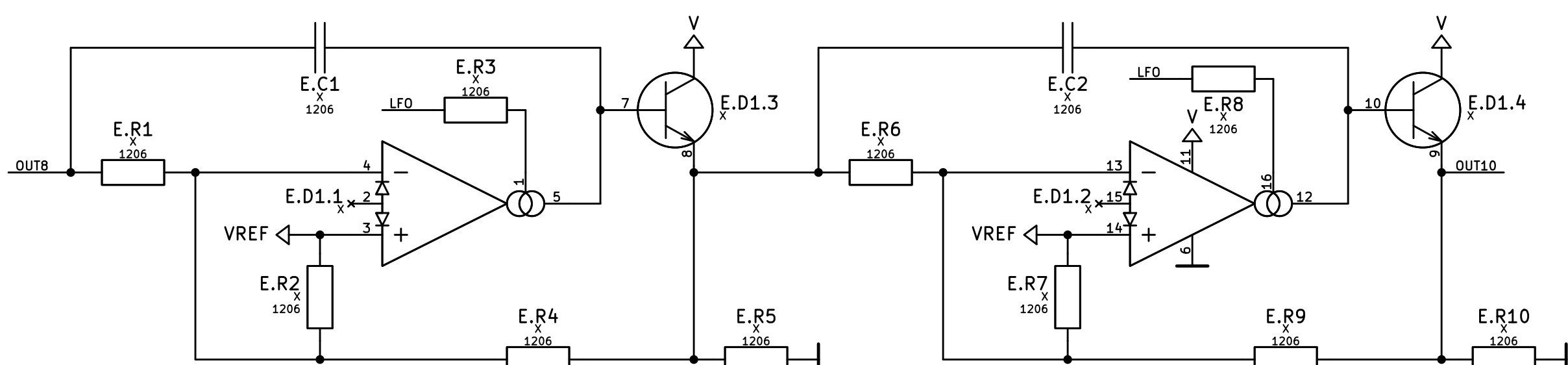
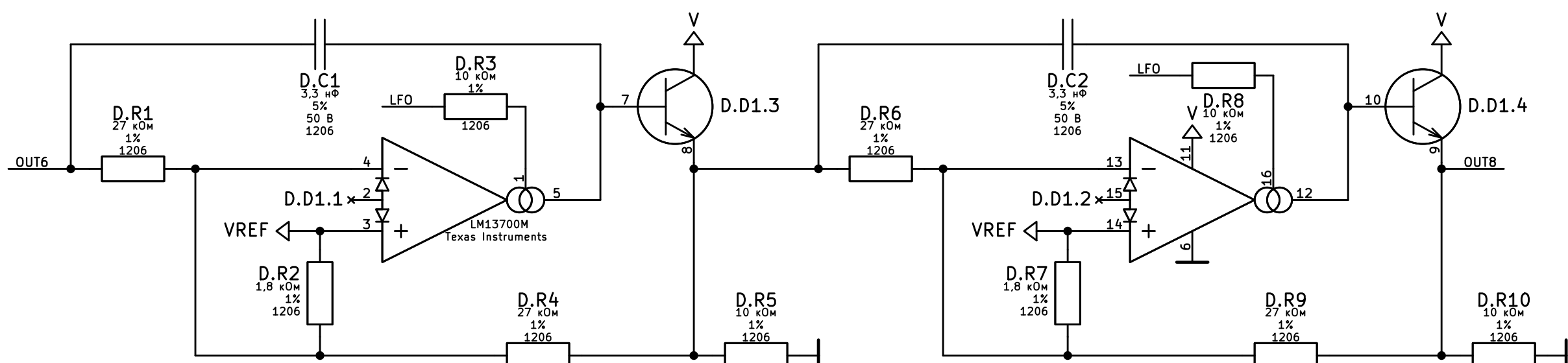
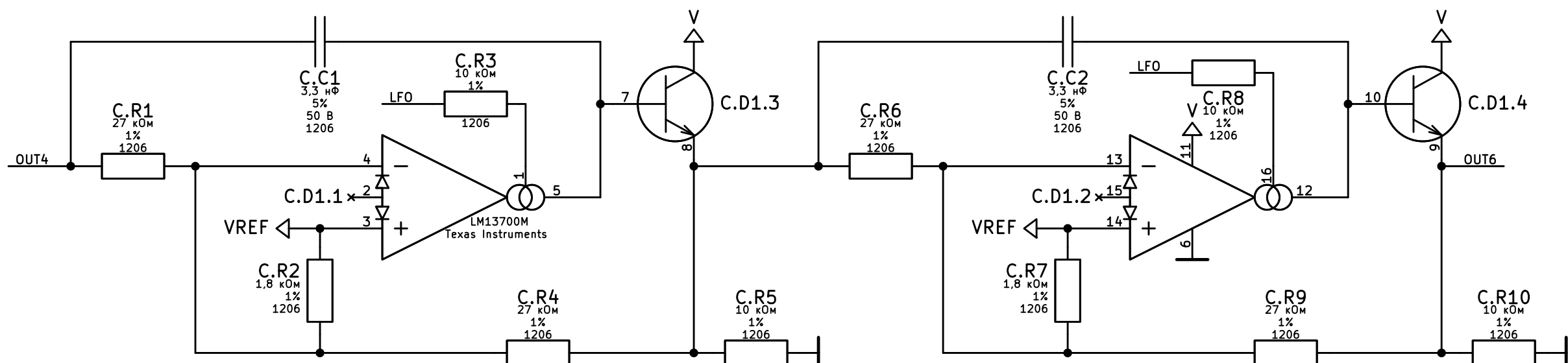
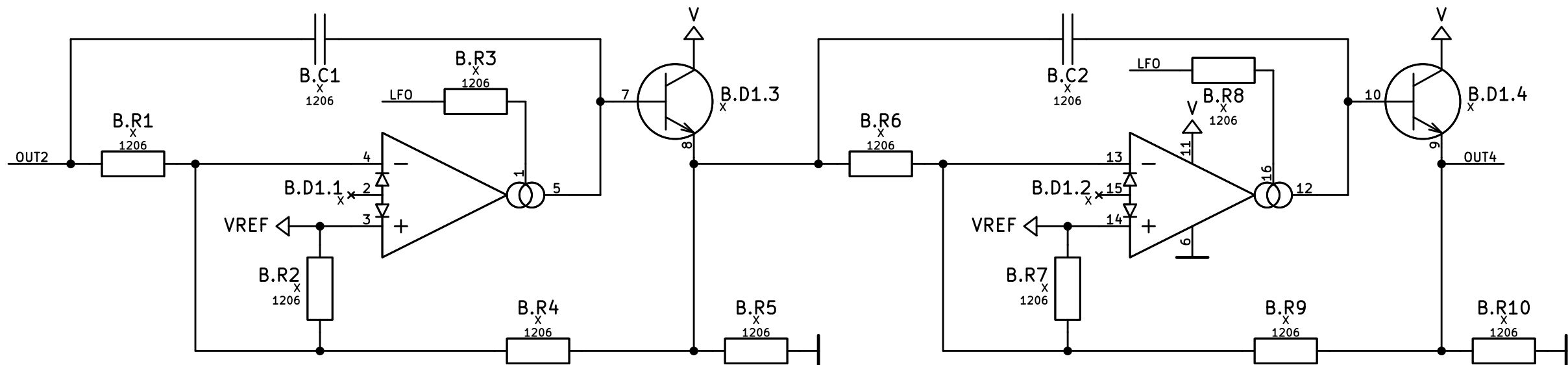


The second stage consists of two differential pairs, A.D1.3 and A.D1.4, each with a current mirror load (A.R3, A.R4 and A.R8, A.R9) and a load capacitor (A.C1, A.C2). The output of the first differential pair is connected to the input of the second differential pair via a current mirror (A.R6). The output of the second differential pair is connected to the output of the first differential pair via a current mirror (A.R10). The output of the second differential pair is also connected to the output of the first differential pair via a current mirror (A.R10).

[illegible][illegible]

The schematic diagram illustrates the RPB1.1 SPEED circuit. It features several key components and connections:

- Input Stage:** The input signal, labeled SA3-COM2, passes through a 1206 ohm resistor (L.J1) and a 470 nF capacitor (L.C1). It then splits to the non-inverting input (pin 2) of the first op-amp (L.D1.1) and through a 360 kOhm resistor (L.R1) to the inverting input (pin 3).
- Feedback and Biasing:** The non-inverting input (pin 2) is also biased via a CTSMO-C capacitor and a 360 kOhm resistor (L.R2) to ground. The inverting input (pin 3) is biased via a 360 kOhm resistor (L.R5) to ground.
- Op-Amp L.D1.1:** An RC4558B op-amp from Texas Instruments, configured as a voltage follower (LFO-SQR), with its output (pin 1) connected to its inverting input (pin 3).
- Control and Timing:** The output of L.D1.1 is connected to the RPB1.1 SPEED IC (pin 0, 1206 ohm resistor L.R4) and the inverting input (pin 5) of the second op-amp (L.D1.2). The RPB1.1 SPEED IC is a 500 kOhm (B) R15K1-L20KC from Song Hual Electric.
- Op-Amp L.D1.2:** Another RC4558B op-amp configured as a voltage follower (LFO-AUTO), with its output (pin 7) connected to its inverting input (pin 5).
- Output and Biasing:** The output of L.D1.2 is connected to the non-inverting input (pin 6) of the third op-amp (L.D1.1) and through a 10 kOhm resistor (L.R8) to the inverting input (pin 3). The non-inverting input (pin 6) is also biased via a CTSMO-C capacitor and a 360 kOhm resistor (L.R9) to ground. The inverting input (pin 3) is biased via a 10 kOhm resistor (L.R10) to ground.
- Final Output:** The output of the third op-amp (L.D1.1) is connected to the LFO-AUTO output (pin 7) and through a 10 kOhm resistor (L.R10) to the inverting input (pin 3).
- Other Components:** The circuit includes several other resistors (L.R3, L.R6, L.R7, L.R9, L.R10) and capacitors (L.C2, L.C3, L.C4, L.C5, L.C6, L.C7, L.C8) for timing and biasing purposes.

The timing diagram illustrates the relationship between various input and output signals of the J1206 device. The horizontal axis represents time. The signals shown are:

- TP1**: Input signal, shown as a square wave.
- TP2**: Input signal, shown as a square wave.
- TP3**: Input signal, shown as a square wave.
- TP4**: Input signal, shown as a square wave.
- V**: Input signal, shown as a square wave.
- VREF**: Input signal, shown as a square wave.
- IN**: Input signal, shown as a square wave.
- CIR-IN**: Input signal, shown as a square wave.
- TP6**: Output signal, labeled **DRY**, shown as a square wave.
- TP7**: Output signal, labeled **LFO-SQR**, shown as a square wave.
- TP8**: Output signal, labeled **LFO-AUTO**, shown as a square wave.
- TP9**: Output signal, labeled **LFO-MANUAL**, shown as a square wave.
- TP10**: Output signal, labeled **OUT**, shown as a square wave.

The diagram also includes two blocks labeled **J1206** and **J2206**, which represent the device's internal logic. The **J1206** block is connected to the **IN** and **CIR-IN** signals, and its output is connected to the **TP6** signal. The **J2206** block is connected to the **TP7**, **TP8**, and **TP9** signals, and its output is connected to the **TP10** signal.

The schematic diagram illustrates the input stage of the ADXL045. It features a differential input structure with two op-amp inputs, 6 and 7. Input 6 is connected to a network of resistors (OM.R1, OM.R2, OM.R3, OM.R4) and a capacitor (OM.C1). Input 7 is connected to a network of resistors (OM.R5, OM.R6, OM.R7, OM.R8, OM.R9) and a capacitor (OM.C1). The output of the op-amp is connected to the RPB2.1 and RPB2.3 comparators. The diagram also shows the connection to the RPB2.1 and RPB2.3 comparators, which are used for signal processing.

[illegible]

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<http://github.com/Adept666>
Salty Phaser [REV1B]
 Sheet: /
 File: TKN-1.23.B-1.sch
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| Size: A1 | Date: 2024-01-07 | Rev: 1B |
| KiCad E.D.A. | kiCad 5.1.12-84ad8e8a8692ubuntu20.04.1 | Id: 1/1 |