## Reporte de practica 5

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#### Marzo 2020

## 1. Código C++

```
* Alumno: Gonzalez Pardo Adrian
   * Grupo: 3CV8
   * Practica 5
   * Desarrollado para Linux por el define de colores
   */
7 #include <bits/stdc++.h>
8 using namespace std;
10 #define KNRM
                 "\x1B[0m"
11 #define KRED
                 "\x1B[31m"
12 #define KGRN
                 "\x1B[32m"
13 #define KYEL
                 "\x1B[33m"
14 #define KBLU
                 "\x1B[34m"
15 #define KMAG
                 "\x1B[35m"
                 "\x1B[36m"
16 #define KCYN
17 #define KWHT
                 "\x1B[37m"
18 #define BRED
                 "\x1B[91m"
19 #define BGRN
                 "\x1B[92m"
20 #define BYEL
                 "\x1B[93m"
21 #define BBLU
                 "\x1B[94m"
22 #define BMAG
                 "\x1B[95m"
23 #define BCYN
                 "\x1B[96m"
24 #define BWHT
                 "\x1B[97m"
25
  class registros{
26
    private:
      short banco[16], writeData, writeReg, readData1, readData2, shamt;
      bool WR, SHE, DIR, CLR;
    public:
30
      /* Constructor */
      archivoRegistros(){
        srand(time(NULL));
      /* Getters and Setters */
36
      short getWriteReg(){return this->writeReg;}
```

```
short getWriteData(){return this->writeData;}
short getReadData1(){return this->readData1;}
short getReadData2(){return this->readData2;}
short getShamt(){return this->shamt;}
bool isWR(){return this->WR;}
bool isSHE(){return this->SHE;}
bool isDIR(){return this->DIR;}
bool isCLR(){return this->CLR;}
void setWriteReg(short writeReg){this->writeReg=writeReg;}
void setWriteData(short writeData){this->writeData=writeData;}
void setReadData1(short readData1){this->readData1=readData1;}
void setReadData2(short readData2){this->readData2=readData2;}
void setShamt(short shamt){this->shamt=shamt;}
void setWR(bool WR){this->WR=WR;}
void setSHE(bool SHE){this->SHE=SHE;}
void setDIR(bool DIR){this->DIR=DIR;}
void setCLR(bool CLR){this->CLR=CLR;}
/* Set banco with random number between -32768 to 32767 */
void set(){
  for(short i=0; i<16; i++) {</pre>
    /* Limite positivo 32767
     * Limite negativo -32768 */
    *(banco+i)=(rand()\%65536)-32768;
  }
}
/* Validation function */
bool isInReg(short reg){
  return (reg<0 || reg>16);
}
bool isReg(short reg){
  return (reg > 0 & & reg < 16);</pre>
```

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```
91
92
       /* Get banco data */
       void get(){
          for(short i=0; i<16; i++){</pre>
94
            cout << "Registro["<<i<<"] :=> "<<banco[i]<<"\n";
95
96
       }
97
98
99
       /* Operaciones del banco de registros */
100
       void operacionSincrona(short writeData, short writeReg,
            short readReg1, short readReg2, short shamt,
            bool WR, bool SHE, bool DIR,
            bool CLR) {
104
          setWR(WR);
105
          setSHE(SHE);
106
          setDIR(DIR);
          setCLR(CLR);
108
          setWriteReg(writeReg);
109
          setWriteData(writeData);
          setShamt(shamt);
111
          if(getWriteReg()<0 || getWriteReg()>16){
            cout << BRED << "Fuera del limite de registros \n" << KNRM;</pre>
113
            return;
114
          }
          if(getWriteData() <-32768 || getWriteData() > 32767) {
117
            cout << BRED << "Valor mayor a un Slit16 \n" << KNRM;</pre>
118
            return;
119
          }
120
121
          if(isInReg(readReg1)){
123
            cout << BRED << "Reg1 fuera del limite de registros \n" << KNRM;</pre>
            return;
124
          }
126
          if (isInReg(readReg2)){
127
            cout << BRED << "Reg2 fuera del limite de registros \n" << KNRM;</pre>
128
            return;
129
          }
130
          if(isInReg(getShamt())){
            cout << BRED << "Shamt fuera del limite de registros \n" << KNRM;</pre>
            return;
134
          }
          setReadData1(banco[readReg1]);
          setReadData2(banco[readReg2]);
138
139
          if(isCLR()){
            operacionAsincrona(isCLR());
140
            return;
141
          }else if(isWR() && !isSHE()){
142
            *(banco+getWriteReg())=getWriteData();
143
```

```
144
            return;
145
         }else if(isWR() && isSHE() && !isDIR()){
            *(banco+getWriteReg())=(*(banco+readReg1)>>getShamt()) & 0
146
      x0000ffff;
            return:
147
         }else if(isWR() && isSHE() && isDIR()){
148
            *(banco+getWriteReg())=(*(banco+readReg1)<<getShamt()) & 0
149
      x0000ffff;
           return;
         }
151
       }
153
       /* Operacion que manda a O todo el banco de registros */
154
       void operacionAsincrona(bool CLR){
         for(short i=0; i<16; i++){</pre>
156
            *(banco+i)=0;
         }
         get();
159
       }
161
       /* Operacion que muestra Registros */
162
       void operacionAsincrona(bool CLR, short readReg1, short readReg2){
163
         setCLR(CLR);
164
         if(isCLR()){
165
            operacionAsincrona(isCLR());
166
         }
167
         if(isReg(readReg1)){
168
            cout < BGRN < "Registro[" < readReg1 < < "] :=> " < banco[readReg1] < < "\n"
169
      << KNRM;
         }
170
         if (isReg(readReg2)){
171
            cout << BYEL << "Registro[" << readReg 2 << "] :=> " << banco[readReg 2] << "\n"
      << KNRM;
         }
174
       }
176 };
177
178 int main(void) {
     registros r;
179
     cout << BBLU << "Inicializacion \n";
180
     r.set();
181
     r.get();
182
     cout << BCYN << "\n\t\t(Operacion 1)\n\toperacionAsincrona(1) <==> RESET\n";
183
     r.operacionAsincrona(1);
184
     cout << KGRN << "\n\t\t(Operacion 2)\n\tBANCO[1]=89 <==> operacionSincrona
186
      (89,1,0,0,0,1,0,0,0)\n";
     r.operacionSincrona(89,1,0,0,0,1,0,0,0);
187
     r.get();
188
189
     cout << KCYN << "\n\t\t(Operacion 3)\n\tBANCO[2]=72 <==> operacionSincrona
190
      (72,2,0,0,0,1,0,0,0)\n";
```

```
r.operacionSincrona(72,2,0,0,0,1,0,0,0);
191
192
     r.get();
193
     cout << KGRN << "\n\t\t(Operacion 4)\n\tBANCO[3]=123 <==> operacionSincrona
194
      (123,3,0,0,0,1,0,0,0) \n";
     r.operacionSincrona(123,3,0,0,0,1,0,0,0);
196
     r.get();
197
     cout << KYEL << "\n\t\t(Operacion 5)\n\tBANCO[4]=53 <==> operacionSincrona
198
      (53,4,0,0,0,1,0,0,0) \n";
     r.operacionSincrona(53,4,0,0,0,1,0,0,0);
199
     r.get();
200
201
     cout << BMAG << "\n\t\t(Operacion 6)\n\tREAD BANCO[1] & BANCO[2]\n";</pre>
202
     r.operacionAsincrona(0,1,2);
203
204
     cout << KMAG << "\n\t\t(Operacion 7)\n\tREAD BANCO[3] & BANCO[4]\n";</pre>
205
     r.operacionAsincrona(0,3,4);
206
207
     cout << BBLU << "\n\t\t(Operacion 8)\n\tBANCO[2] = BANCO[1] << 3 <==>
208
      operacionSincrona(0,2,1,0,3,1,1,1,0)\n";
     r.operacionSincrona(0,2,1,0,3,1,1,1,0);
     r.get();
211
     cout << KYEL << "\n\t\t(Operacion 9)\n\tBANCO[4] = BANCO[3] >> 5 <==>
212
      operacionSincrona(0,4,3,0,5,1,1,0,0)\n";
     r.operacionSincrona(0,4,3,0,5,1,1,0,0);
213
     r.get();
214
215
     cout << KGRN << "\n\t\t(Operacion 10)\n\tREAD BANCO[1] & BANCO[2]\n";</pre>
     r.operacionAsincrona(0,1,2);
217
218
     cout << KYEL << "\n\t\t(Operacion 11)\n\tREAD BANCO[3] & BANCO[4]\n";</pre>
219
     r.operacionAsincrona(0,3,4);
220
221
     cout << KBLU << "\n\t\t(Operacion 12)\n\tget()\n";</pre>
222
     r.get();
223
     cout << BCYN << "\n\t\t(Operacion 13)\n\toperacionAsincrona(1) <==> RESET\n"
225
     r.operacionAsincrona(1);
226
227
     cout << KNRM << endl;</pre>
228
229
     return 0;
230 }
```

Código fuente de archivo de registros

### 2. Captura de simulaciones

```
Inicializacion
Registro[0] :=> -12667
Registro[1] :=> -3213
Registro[2] :=> 15915
Registro[3] :=> -26708
Registro[4] :=> 8324
Registro[5] :=> -1511
Registro[6] :=> -31770
Registro[7]
           :=> -16905
Registro[8] :=> -1648
Registro[9] :=> 7047
Registro[10] :=> 21355
Registro[11] :=> -8001
Registro[12]
             :=> -7134
Registro[13] :=> 32000
Registro[14]
            :=> -16773
Registro[15] :=> -18843
```

Figura 0: Inicialización del programa con números random

```
(Operacion 1)
        operacionAsincrona(1) <==> RESET
Registro[0] :=> 0
Registro[1] :=> 0
Registro[2] :=> 0
Registro[3]
           :=> 0
Registro[4] :=> 0
Registro[5] :=> 0
Registro[6] :=> 0
Registro[7]
           :=> 0
Registro[8] :=> 0
Registro[9] :=> 0
Registro[10] :=> 0
Registro[11]
Registro[12] :=> 0
Registro[13] :=> 0
Registro[14] :=> 0
Registro[15] :=> 0
```

Figura 1: Operación 1 Reset"

```
(Operacion 2)
        BANCO[1]=89 <==> operacionSincrona(89,1,0,0,0,1,0,0,0)
Registro[0]
                                           breakatwhitespace=false
Registro[1]
                89
                                           breaklines=true,
Reaistro[2]
                                            captionpos=b,
Registro[3]
Registro[4]
Registro[5]
Registro[6]
                                           numbersep=5pt,
Registro[7]
Registro[8]
Registro[9]
Registro[10]
Registro[11]
Registro[12]
Registro[13]
Registro[14]
Registro[15]
```

Figura 2: Operación 2 "Banco[1]=89"

```
(Operacion 3)
        BANCO[2]=72 <==> operacionSincrona(72,2,0,0,0,1,0,0,0)
Registro[0]
Registro[1]
            :=> 89
Registro[2]
            :=> 72
Registro[3]
Registro[4]
Registro[5]
                                           keepspaces=true,
Registro[6]
Registro[7]
Registro[8]
                                           numbersep=5pt,
Registro[9] :=> 0
Registro[10]
Registro[11]
Registro[12]
                                           showtabs=false,
Registro[13] :=> 0
Registro[14]
Registro[15]
```

Figura 3: Operación 3 "Banco[2]=72"

```
(Operacion 4)

BANCO[3]=123 <==> operacionSincrona(123,3,0,0,0,1,0,0,0)

Registro[0] :=> 0

Registro[1] :=> 89

Registro[2] :=> 72

Registro[3] :=> 123

Registro[4] :=> 0

Registro[5] :=> 0

Registro[6] :=> 0

Registro[7] :=> 0

Registro[8] :=> 0

Registro[9] :=> 0

Registro[10] :=> 0
```

Figura 4: Operación 4 "Banco[3]=123"

Figura 5: Operación 5 "Banco[4]=53"

```
(Operacion 6)

READ BANCO[1] & BANCO[2]

Registro[1] :=> 89

Registro[2] :=> 72
```

Figura 6: Operación 6 READ Banco[1] & Banco[2]"

```
(Operacion 7) 35 brea brea (Operacion 7) 35 brea (Operacion 7) 35 brea (Operacion 7) 36 capt (Operacion 7) 36 capt (Operacion 7) 37 keep (Operacion 7) 38 operacion 7) 35 operacion 7) 35 operacion 7) 36 operacion 7) 37 operacion 7) 37 operacion 7) 38 oper
```

Figura 7: Operación 7 READ Banco[3] & Banco[4]"

```
(Operacion 8)
        BANCO[2]=BANCO[1]<<3<==> operacionSincrona(0,2,1,0,3,1,1,1,0)
Registro[0] :=> 0
Registro[1] :=> 89
Registro[2] :=> 712
Registro[3] :=> 123
Registro[4] :=> 53
Registro[5] :=> 0
Registro[6] :=> 0
Registro[7] :=> 0
Registro[8] :=> 0
Registro[9] :=> 0
Registro[10] :=> 0
Registro[11]
Registro[12]
Registro[13]
                                     \newcommand\tab[1][1cm]{\hspace*{#1}}
Registro[14] :=> 0
Registro[15] :=> 0
```

Figura 8: Operación 8 "Banco[2]=Banco[1]<<3"

```
(Operacion 9)

BANCO[4]=BANCO[3] >> 5 <=> OperacionSincrona(0,4,3,0,5,1,1,0,0)

Registro[0] :=> 0

Registro[1] :=> 89

Registro[2] :=> 712

Registro[3] :=> 123

Registro[4] :=> 3

Registro[5] :=> 0

Registro[6] :=> 0

Registro[7] :=> 0

Registro[8] :=> 0

Registro[9] :=> 0

Registro[10] :=> 0

Registro[11] :=> 0

Registro[12] :=> 0

Registro[13] :=> 0

Registro[13] :=> 0

Registro[14] :=> 0

Registro[15] :=> 0

Registro[15
```

Figura 9: Operación 9 "Banco[4]=Banco[3]>>5"

```
(Operacion 10)

READ BANCO[1] & BANCO[2] 47 \autho

Registro[1] :=> 89 48 \date{

Registro[2] :=> 712 49

50 \title
```

Figura 10: Operación 10 READ Banco[1] & Banco[2]"

```
(Operacion 11)

READ BANCO[3] & BANCO[4]

Registro[3] :=> 123

Registro[4] :=> 3
```

Figura 11: Operación 11 READ Banco[3] & Banco[4]"

```
get()

Registro[0] :=> 0

Registro[1] :=> 89

Registro[2] :=> 712

Registro[3] :=> 123

Registro[4] :=> 0

Registro[5] :=> 0

Registro[6] :=> 0

Registro[7] :=> 0

Registro[8] :=> 0

Registro[9] :=> 0

Registro[10] :=> 0

Registro[11] :=> 0

Registro[12] :=> 0

Registro[13] :=> 0

Registro[13] :=> 0

Registro[14] :=> 0

Registro[15] :=> 0

Regi
```

Figura 12: Operación 12 "GET()"

```
(Operacion 13)
        operacionAsincrona(1) <==> RESET
Registro[0] :=> 0
Registro[1] :=> 0
Registro[2] :=>
Registro[3]
Registro[4] :=> 0
Registro[5] :=> 0
Registro[6] :=> 0
Registro[7]
Registro[8] :=> 0
Registro[9] :=> 0
Registro[10] :=> 0
Registro[11]
Registro[12]
Registro[13]
Registro[14] :=> 0
Registro[15] :=> 0
```

Figura 13: Operación 13 Reset"