Reporte de practica 5

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1. Código C++

```
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   * Grupo: 3CV8
   * Practica 5
   */
6 #include <bits/stdc++.h>
 using namespace std;
9 #define KNRM
                 "\x1B[0m"
10 #define KRED
                 "\x1B[31m"
11 #define KGRN
                 "\x1B[32m"
12 #define KYEL
                 "\x1B[33m"
13 #define KBLU
                 "\x1B[34m"
14 #define KMAG
                 "\x1B[35m"
15 #define KCYN
                 "\x1B[36m"
16 #define KWHT
                 "\x1B[37m"
17 #define BRED
                 "\x1B[91m"
18 #define BGRN
                 "\x1B[92m"
19 #define BYEL
                 "\x1B[93m"
20 #define BBLU
                 "\x1B[94m"
21 #define BMAG
                 "\x1B[95m"
22 #define BCYN
                 "\x1B[96m"
 #define BWHT
                 "\x1B[97m"
25 class registros{
    private:
26
      int banco[16], writeData, writeReg, readData1, readData2, shamt;
      bool WR, SHE, DIR, CLR;
    public:
      /* Constructor */
30
      registros(){
        srand(time(NULL));
33
      /* Getters and Setters */
      int getWriteReg(){return this->writeReg;}
36
```

```
int getWriteData(){return this->writeData;}
      int getReadData1(){return this->readData1;}
      int getReadData2(){return this->readData2;}
      int getShamt(){return this->shamt;}
      bool isWR(){return this->WR;}
46
      bool isSHE(){return this->SHE;}
49
      bool isDIR(){return this->DIR:}
50
      bool isCLR(){return this->CLR;}
      void setWriteReg(int writeReg) { this -> writeReg = writeReg; }
      void setWriteData(int writeData){this->writeData=writeData;}
      void setReadData1(int readData1){this->readData1=readData1;}
      void setReadData2(int readData2){this->readData2=readData2;}
      void setShamt(int shamt){this->shamt=shamt;}
      void setWR(bool WR){this->WR=WR;}
      void setSHE(bool SHE){this->SHE=SHE;}
66
      void setDIR(bool DIR){this->DIR=DIR;}
      void setCLR(bool CLR){this->CLR=CLR;}
70
      /* Set banco with random number between -32768 to 32767 */
      void set(){
        for(int i=0; i<16; i++) {</pre>
          /* Limite positivo 32767
           * Limite negativo -32768 */
          *(banco+i)=(rand()\%65536)-32768;
        }
      }
80
      /* Validation function */
      bool isInReg(int reg){
        return (reg<0 || reg>16);
      }
86
      bool isReg(int reg){
        return (reg > 0 & & reg < 16);</pre>
```

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81

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84

85

87

89

```
/* Get banco data */
91
92
       void get(){
          for(int i=0; i<16; i++){</pre>
93
            cout << "Registro["<<i<<"] :=> "<<banco[i]<<"\n";
94
          }
95
       }
96
97
98
       /* Operaciones del banco de registros */
99
       void operacionSincrona(int writeData,int writeReg,
100
            int readReg1,int readReg2,int shamt,
            bool WR, bool SHE, bool DIR,
            bool CLR) {
          setWR(WR);
104
          setSHE(SHE);
105
          setDIR(DIR);
106
          setCLR(CLR);
          setWriteReg(writeReg);
108
          setWriteData(writeData);
109
          setShamt(shamt);
          if(getWriteReg()<0 || getWriteReg()>16){
111
            cout << BRED << "Fuera del limite de registros \n" << KNRM;</pre>
            return;
113
          }
114
          if (getWriteData() <-32768 || getWriteData() > 32767) {
            cout << BRED << "Valor mayor a un Slit16 \n" << KNRM;</pre>
117
            return;
118
          }
119
          if (isInReg(readReg1)){
121
            cout << BRED << "Reg1 fuera del limite de registros \n" << KNRM;</pre>
123
            return;
          }
124
          if(isInReg(readReg2)){
126
            cout << BRED << "Reg2 fuera del limite de registros \n" << KNRM;</pre>
127
            return;
          }
129
130
          if(isInReg(getShamt())){
            cout << BRED << "Shamt fuera del limite de registros \n" << KNRM;</pre>
            return;
134
135
          setReadData1(banco[readReg1]);
          setReadData2(banco[readReg2]);
          if(isCLR()){
138
139
            operacionAsincrona(isCLR());
            return;
140
          }else if(isWR() && !isSHE()){
141
            *(banco+getWriteReg())=getWriteData();
142
143
            return;
```

```
}else if(isWR() && isSHE() && !isDIR()){
144
            *(banco+getWriteReg())=(*(banco+readReg1)>>getShamt()) & 0
145
      x0000ffff;
           return;
146
         }else if(isWR() && isSHE() && isDIR()){
147
            *(banco+getWriteReg())=(*(banco+readReg1)<<getShamt()) & 0
148
      x0000ffff;
           return;
149
         }
       }
151
       /* Operacion que manda a O todo el banco de registros */
153
       void operacionAsincrona(bool CLR){
154
         for(int i=0; i<16; i++){</pre>
            *(banco+i)=0;
156
         get();
       }
159
       /* Operacion que muestra Registros */
161
       void operacionAsincrona(bool CLR, int readReg1, int readReg2){
162
         setCLR(CLR);
163
         if(isCLR()){
164
            operacionAsincrona(isCLR());
165
166
         if(isReg(readReg1)){
167
            cout << BGRN << "Registro [" << readReg1 << "] :=> " << banco [readReg1] << "\n"
      << KNRM:
         }
         if(isReg(readReg2)){
            cout << BYEL << "Registro[" << readReg2 << "] :=> " << banco[readReg2] << "\n"
      << KNRM;
         }
173
       }
174
175 };
176
int main(void) {
     registros r;
178
     cout << BBLU << "Inicializacion \n";</pre>
179
     r.set();
180
     r.get();
181
     cout << BCYN << "\n\t\t(Operacion 1)\n\toperacionAsincrona(1) <==> RESET\n";
182
     r.operacionAsincrona(1);
183
184
     cout << KGRN << "\n\t\t(Operacion 2)\n\tBANCO[1]=89 <==> operacionSincrona
      (89,1,0,0,0,1,0,0,0) \n";
     r.operacionSincrona(89,1,0,0,0,1,0,0,0);
186
     r.get();
187
188
     cout << KCYN << "\n\t\t(Operacion 3)\n\tBANCO[2]=72 <==> operacionSincrona
189
      (72,2,0,0,0,1,0,0,0)\n";
     r.operacionSincrona(72,2,0,0,0,1,0,0,0);
```

```
r.get();
191
192
     cout << KGRN << "\n\t\t(Operacion 4)\n\tBANCO[3]=123 <==> operacionSincrona
193
      (123,3,0,0,0,1,0,0,0) \n";
     r.operacionSincrona(123,3,0,0,0,1,0,0,0);
194
     r.get();
195
196
     cout << KYEL << "\n\t\t(Operacion 5)\n\tBANCO[4]=53 <==> operacionSincrona
197
      (53,4,0,0,0,1,0,0,0)\n";
     r.operacionSincrona(53,4,0,0,0,1,0,0,0);
198
     r.get();
199
200
     cout << BMAG << "\n\t\t(Operacion 6)\n\tREAD BANCO[1] & BANCO[2]\n";</pre>
201
     r.operacionAsincrona(0,1,2);
202
203
     cout << KMAG << "\n\t\t(Operacion 7)\n\tREAD BANCO[3] & BANCO[4]\n";</pre>
204
     r.operacionAsincrona(0,3,4);
205
206
     cout << BBLU << "\n\t\t(Operacion 8)\n\tBANCO[2] = BANCO[1] << 3 <==>
207
      operacionSincrona(0,2,1,0,3,1,1,1,0)\n";
     r.operacionSincrona(0,2,1,0,3,1,1,1,0);
208
209
     r.get();
210
     cout << KYEL << "\n\t\t(Operacion 9)\n\tBANCO[4] = BANCO[3] >> 5 <==>
211
      operacionSincrona(0,4,3,0,5,1,1,0,0)\n";
     r.operacionSincrona(0,4,3,0,5,1,1,0,0);
212
     r.get();
213
214
     cout << KGRN << "\n\t\t(Operacion 10)\n\tREAD BANCO[1] & BANCO[2]\n";</pre>
215
     r.operacionAsincrona(0,1,2);
217
     cout << KYEL << "\n\t\t(Operacion 11)\n\tREAD BANCO[3] & BANCO[4]\n";</pre>
218
219
     r.operacionAsincrona(0,3,4);
220
     cout << KBLU << "\n\t\t(Operacion 12)\n\tget()\n";</pre>
221
     r.get();
222
223
     cout << BCYN << "\n\t\t(Operacion 13)\n\toperacionAsincrona(1) <==> RESET\n"
224
     r.operacionAsincrona(1);
225
     cout << KNRM << endl;</pre>
227
     return 0;
228
229 }
```

Código fuente de archivo de registros

2. Captura de simulaciones

```
Inicializacion
Registro[0] :=> -12667
Registro[1] :=> -3213
Registro[2] :=> 15915
Registro[3] :=> -26708
Registro[4] :=> 8324
Registro[5] :=> -1511
Registro[6] :=> -31770
Registro[7]
           :=> -16905
Registro[8] :=> -1648
Registro[9] :=> 7047
Registro[10] :=> 21355
Registro[11] :=> -8001
Registro[12]
             :=> -7134
Registro[13] :=> 32000
Registro[14]
            :=> -16773
Registro[15] :=> -18843
```

Figura 0: Inicialización del programa con números random

```
(Operacion 1)
        operacionAsincrona(1) <==> RESET
Registro[0] :=> 0
Registro[1] :=> 0
Registro[2] :=> 0
Registro[3]
           :=> 0
Registro[4] :=> 0
Registro[5] :=> 0
Registro[6] :=> 0
Registro[7]
           :=> 0
Registro[8] :=> 0
Registro[9] :=> 0
Registro[10] :=> 0
Registro[11]
Registro[12] :=> 0
Registro[13] :=> 0
Registro[14] :=> 0
Registro[15] :=> 0
```

Figura 1: Operación 1 Reset"

```
(Operacion 2)
        BANCO[1]=89 <==> operacionSincrona(89,1,0,0,0,1,0,0,0)
Registro[0]
                                           breakatwhitespace=false
Registro[1]
                89
                                           breaklines=true,
Reaistro[2]
                                            captionpos=b,
Registro[3]
Registro[4]
Registro[5]
Registro[6]
                                           numbersep=5pt,
Registro[7]
Registro[8]
Registro[9]
Registro[10]
Registro[11]
Registro[12]
Registro[13]
Registro[14]
Registro[15]
```

Figura 2: Operación 2 "Banco[1]=89"

```
(Operacion 3)
        BANCO[2]=72 <==> operacionSincrona(72,2,0,0,0,1,0,0,0)
Registro[0]
Registro[1]
            :=> 89
Registro[2]
            :=> 72
Registro[3]
Registro[4]
Registro[5]
                                           keepspaces=true,
Registro[6]
Registro[7]
Registro[8]
                                           numbersep=5pt,
Registro[9] :=> 0
Registro[10]
Registro[11]
Registro[12]
                                           showtabs=false,
Registro[13] :=> 0
Registro[14]
Registro[15]
```

Figura 3: Operación 3 "Banco[2]=72"

```
(Operacion 4)

BANCO[3]=123 <==> operacionSincrona(123,3,0,0,0,1,0,0,0)

Registro[0] :=> 0

Registro[1] :=> 89

Registro[2] :=> 72

Registro[3] :=> 123

Registro[4] :=> 0

Registro[5] :=> 0

Registro[6]:=> 0

Registro[7] :=> 0

Registro[8] :=> 0

Registro[9]:=> 0

Registro[10] :=> 0

R
```

Figura 4: Operación 4 "Banco[3]=123"

Figura 5: Operación 5 "Banco[4]=53"

```
(Operacion 6)

READ BANCO[1] & BANCO[2]

Registro[1] :=> 89

Registro[2] :=> 72
```

Figura 6: Operación 6 READ Banco[1] & Banco[2]"

```
(Operacion 7) 35 brea brea (Operacion 7) 35 brea (Operacion 7) 35 brea (Operacion 7) 36 capt (Operacion 7) 36 capt (Operacion 7) 37 keep (Operacion 7) 38 operacion 7) 35 operacion 7) 35 operacion 7) 36 operacion 7) 37 operacion 7) 37 operacion 7) 38 oper
```

Figura 7: Operación 7 READ Banco[3] & Banco[4]"

```
(Operacion 8)
        BANCO[2]=BANCO[1]<<3<==> operacionSincrona(0,2,1,0,3,1,1,1,0)
Registro[0] :=> 0
Registro[1] :=> 89
Registro[2] :=> 712
Registro[3] :=> 123
Registro[4] :=> 53
Registro[5] :=> 0
Registro[6] :=> 0
Registro[7] :=> 0
Registro[8] :=> 0
Registro[9] :=> 0
Registro[10] :=> 0
Registro[11]
Registro[12]
Registro[13]
                                     \newcommand\tab[1][1cm]{\hspace*{#1}}
Registro[14] :=> 0
Registro[15] :=> 0
```

Figura 8: Operación 8 "Banco[2]=Banco[1]<<3"

```
(Operacion 9)

BANCO[4]=BANCO[3] >> 5 <=> OperacionSincrona(0,4,3,0,5,1,1,0,0)

Registro[0] :=> 0

Registro[1] :=> 89

Registro[2] :=> 712

Registro[3] :=> 123

Registro[4] :=> 3

Registro[5] :=> 0

Registro[6] :=> 0

Registro[7] :=> 0

Registro[8] :=> 0

Registro[9] :=> 0

Registro[10] :=> 0

Registro[11] :=> 0

Registro[12] :=> 0

Registro[13] :=> 0

Registro[13] :=> 0

Registro[14] :=> 0

Registro[15] :=> 0

Registro[15
```

Figura 9: Operación 9 "Banco[4]=Banco[3]>>5"

```
(Operacion 10)

READ BANCO[1] & BANCO[2] 47 \autho

Registro[1] :=> 89 48 \date{

Registro[2] :=> 712 49

50 \title
```

Figura 10: Operación 10 READ Banco[1] & Banco[2]"

```
(Operacion 11)

READ BANCO[3] & BANCO[4]

Registro[3] :=> 123

Registro[4] :=> 3
```

Figura 11: Operación 11 READ Banco[3] & Banco[4]"

```
get()

Registro[0] :=> 0

Registro[1] :=> 89

Registro[2] :=> 712

Registro[3] :=> 123

Registro[4] :=> 0

Registro[5] :=> 0

Registro[6] :=> 0

Registro[7] :=> 0

Registro[8] :=> 0

Registro[9] :=> 0

Registro[10] :=> 0

Registro[11] :=> 0

Registro[12] :=> 0

Registro[13] :=> 0

Registro[13] :=> 0

Registro[14] :=> 0

Registro[15] :=> 0

Regi
```

Figura 12: Operación 12 "GET()"

```
(Operacion 13)
        operacionAsincrona(1) <==> RESET
Registro[0] :=> 0
Registro[1] :=> 0
Registro[2] :=>
Registro[3]
Registro[4] :=> 0
Registro[5] :=> 0
Registro[6] :=> 0
Registro[7]
Registro[8] :=> 0
Registro[9] :=> 0
Registro[10] :=> 0
Registro[11]
Registro[12]
Registro[13]
Registro[14] :=> 0
Registro[15] :=> 0
```

Figura 13: Operación 13 Reset"