R-I-J TİPİ KOMUTLAR

	6-bit	5-bit	5-bit	5-bit	5-bit	5-bit
LW	op	rs	rt	immediate		
SW	op	rs	rt	immediate		
ADD	op	rs	rt	rd	0	func
SUB	op	rs	rt	rd	0	func
BEQ	op	rs	rt	immediate		
J	op		address			

KOMUTLARIN ALU DEĞERLERİ

Operation	RegDst	RegWrite	ALUSrc	ALUOp	MemWrite	MemRead	MemToReg
add	1	1	0	010	0	0	0
sub	1	1	0	110	0	0	0
and	1	1	0	000	0	0	0
or	1	1	0	001	0	0	0
slt	1	1	0	111	0	0	0
lw	0	1	1	010	0	1	1
sw	X	0	1	010	1	0	X
beq	X	0	0	110	0	0	X

The Five Cycles of MIPS

(Instruction Fetch)

    IR:= Memory[PC]

    PC:= PC+4

(Instruction decode and Register fetch)

    A:= Reg[IR[25:21]], B:=Reg[IR[20:16]]

    ALUout := PC + sign-extend(IR[15:0]]

(Execute|Memory address|Branch completion)

    Memory reference: ALUout:= A+ IR[15:0]

    R-type (ALU): ALUout:= A op B

    Branch: if A=B then PC := ALUout

(Memory access | R-type completion)

    LW: MDR:= Memory[ALUout]

    SW: Memory[ALUout]:= B

    R-type: Reg[IR[15:11]]:= ALUout

(Writeback)

    LW: Reg[[20:16]]:= MDR

5 AŞAMA ÜZERİNDE

Break datapath into 5 stages

❑ Each stage has its own functional units.

❑ Each stage can execute in 2ns
  – Just like the multi-cycle implementation