PAR – 2^{nd} In-Term Exam – Course 2017/18-Q1
January 10th, 2018

Problem 1 (4 points) Consider the following sequential C code for reversing the order of a vector of data items and doing some computation on them:

```
int * array; // pointer to start of array
int N; // length of array, assumed to be multiple of the number of processors

void swap (int i, int j) {
    int tmp = array[i]; array[i] = array[j]; array[j] = tmp;
}

void reverse ( ) {
    for (int i = 0; i < N/2; i++) swap (i, N - 1 - i);
}

void compute ( ) {
    for (int i = 0; i < N; i++) array[i] = foo(array[i], i);
}

void main( ) {
    reverse( );
    compute( );
}
```

We ask you:

1. Implement, using OpenMP, a parallel version for function `compute` that follows a *block-cyclic geometric data decomposition* for the *output* vector `array`. Decide the minimum value for the block size that better exploits data locality (assuming that cache lines are 32 bytes long and integers occupy 4 bytes). **Important:** You are **NOT ALLOWED to use the `for`** clause in your parallel version.

2. Draw the *geometric data decomposition* for the *output* vector `array` that would be implemented with the (incomplete) parallel version for function `reverse` that is given below:

```
void reverse ( ) {
    int P = ...;  // number of threads executing this function
    int id = ...; // identifier of the thread executing this instance (0 .. P-1)

    int segmentLength = N / ( 2 * P );
    int segmentStart = id * segmentLength;
    for (int i = segmentStart; i < segmentStart + segmentLength; i++)
        swap (i , N - 1 - i);
}
```

Complete the parallel code with the appropriate OpenMP pragmas and invocations to intrinsic functions.

3. Finally, implement a new parallel version for function `compute` that follows the same *output geometric data decomposition* that has been specified above in function `reverse`.

Problem 2 (2 points) Given the following sequential code in C that counts the number of times each key in a set of keys (contained in vector `keys`) appears in a vector `DBin`:

```
#define DBsize 1048576
#define nkeys 128 // much larger than the number of processors

int main() {
    double DBin[DBsize];
    double keys[nkeys];
    unsigned int counter[nkeys];

    getkeys(keys, nkeys);      // get keys
    initialize(DBin, DBsize);  // initialize elements in DBin

    #pragma omp parallel
    for (unsigned int i = 0; i < DBsize; i++)
        #pragma omp for schedule(static, 1)
        for (unsigned int k = 0; k < nkeys; k++)
            if (DBin[i] == keys[k]) counter[k]++;
}
```

Does the proposed parallelisation strategy suffer from false sharing? Justify your answer and in affirmative case propose two alternative solutions that eliminate the false sharing issue:

Notes: 1) Assume that vectors `keys` and `counter` start at the beginning of a cache line; 2) cache lines are 32 bytes long; and 3) `double` and `int` data elements occupy 8 and 4 bytes, respectively.

Problem 3 (4 points) Given a NUMA system with 2 nodes, each node with 2 cores (each with its own local cache memory), which implements a write–invalidate coherence scheme based on directories among NUMA Nodes and MSI snoopy within each NUMA Node. Assume that the following code is executed on 3 cores of that system:

```
// In cores 0 and 1 (NUMA Node 0)          // In core 2 (NUMA Node 1)
count = 0;
flag = 1;                                  ...
#pragma omp parallel for                   tmp = ll(flag);
for (i = 0; i < 4; i++)                lock: while (!(sc(1, flag) && tmp==0))
    #pragma omp atomic                         tmp = ll(flag);
    count++;                               ...
flag = 0;
```

Assumptions: 1) variables `i` and `tmp` are stored in two registers in the register file of each core; variables `count` and `flag` are stored in the same memory line, mapped in NUMA Node 1; 2) local cache memories are initially empty; 3) the atomic pragma does not imply additional memory accesses; and 4) the execution of `ll` (load linked) implies a $BusRd$ and $RdReq$, `sc` (store conditional) implies a single $BusRdX$ and $WrReq$, and the increment ++ implies a $BusRdX$ and $WrReq$, if any of them is necessary.

We ask you to complete the following table with the actions that occur (*NUMA transactions* and *Bus transactions*) and changes in the state of caches and directories to maintain memory coherency, assuming the temporal ordering of memory instructions shown in the same table.

SURNAME:

NAME:

Time	NUMA Node 0						NUMA Node 1							
	Core 0		Core 1		Bus transactions	NUMA transactions	Core 2		Core 3	Bus transactions	NUMA transactions			
	Inst.	Cache state flag/count	Inst.	Cache state flag/count			Inst.	Cache state flag/count	Not used			Directory state flag / count	Sharers list 1	0
0	**count=0**													
1	**Flag=1**													
2	**count++**													
3			**count++**											
4							**ll flag**							
5	**count++**													
6							**sc 1, flag**							
7							**ll flag**							
8			**count++**											
9							**sc 1, flag**							
10	**flag=0**													
11							**ll flag**							
12							**sc 1, flag**							

(1) Cache line state: M (modified), S (shared) or I (invalid)

(2) Coherence commands inside NUMA node: BusRd, BusRdX and Flush

(3): Line state in node memory: M (modified), S (shared) or U (uncached)

(4) Coherence commands between NUMA nodes: RdReq, WrReq, Dreply, Fetch and Invalidate