ECE 538: VLSI System Testing
Spring 2019

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Homework 1

Assigned: January 22, 2019; Due: January 31, 2019

Instructions:
You are required to work on the homework on your own. If you think a question has several interpretations, make reasonable assumptions and state them clearly. Please be neat and legible. Show all work in order to receive partial credit.

Problem 1 (5 points) [SSL faults in irredundant circuits]: Prove that no SSL fault in a single-output, irredundant circuit can complement the function *z* implemented by the fault-free circuit.

Problem 2 (5 points) Textbook Problem 4.8 (Page 79).

Problem 3 (10 points) Textbook Problem 4.5 (Page 79).

Problem 4 (10 points) [Fault modeling]: This concerns the effects of physical faults on the circuit shown below (Fig. 1).
(a) Suppose that a manufacturing defect creates a short-circuit joining points e and g. Determine the resulting function z_{f1} realized by the circuit, and show it on a truth table. Can this physical fault be modeled by logical fault?
(b) Suppose that the IC was dropped during a wild student party, breaking the connection marked g in the figure. Determine the resulting function z_{f2} realized by the circuit, and show it on the same truth table. Once again, can this physical fault be modeled by logical fault?

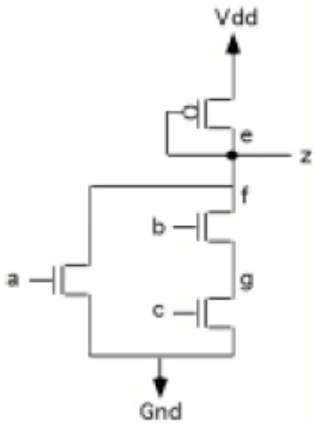

Fig. 1: Schematic to be used for Problem 4.

Problem 5 (10 points) [Stuck-open faults]:
Fig. 2 shows the switch level design of a complementary CMOS gate. The line marked by X is broken. How many test patterns are required to detect this fault? Identify these patterns. Is your *robust*, i.e., valid under any condition? Explain.

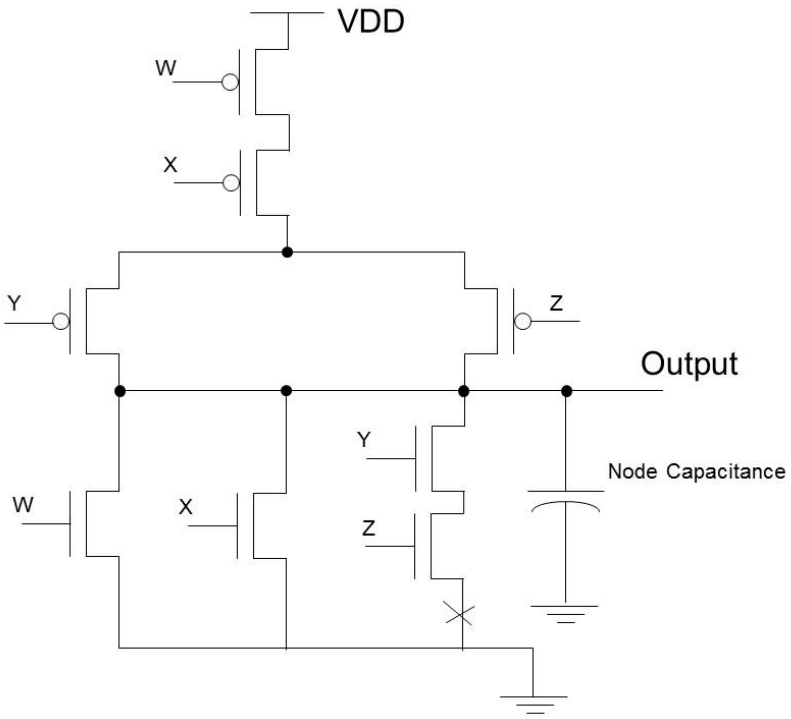

Fig. 2: Figure for Problem 5.

Problem 6 (10 points) [Logic simulation]: It is proposed to augment the standard 3-valued logic based on {0,1,X} by a fourth value X*, where X* stands for the complement of X. Write a brief note evaluating the usefulness of the resulting 4-valued algebra in logic simulation. Illustrate of your argument(s) with a simple concrete example.

Problem 7 (10 points) [Logic simulation]: An inertial delay element responds only to input changes that persist for a minimum time T_{id}. Input pulses of width less than T_{id} are filtered out, but of width more than Tid are transmitted, with a pure delay of T_{id}. Many CAD systems do not allow a designer to assign an inertial delay value to a gate. We can, however, construct a "workaround" model for an inertial delay from a pure delay and some zero-delay combinational logic, as shown below. Determine a suitable logic circuit for C, and briefly explain how it works.