ECE 538: VLSI System Testing
Solutions to Homework 2

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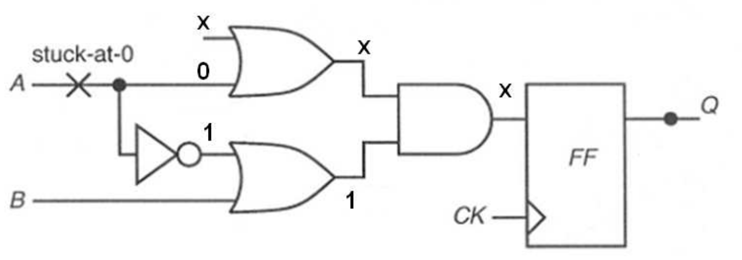
Problem 4.2:

In the fault-free case, we can initialize $Q = 1$ by setting $A = 1$ and $B = 1$ independently of the previous FF state.

In the faulty case, the FF will latch an "X" for any input combination:

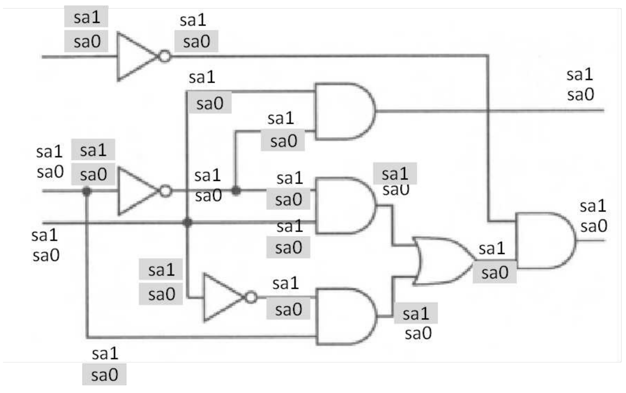


Therefore, the faulty circuit cannot be initialized. Other faults that will prevent initialization:

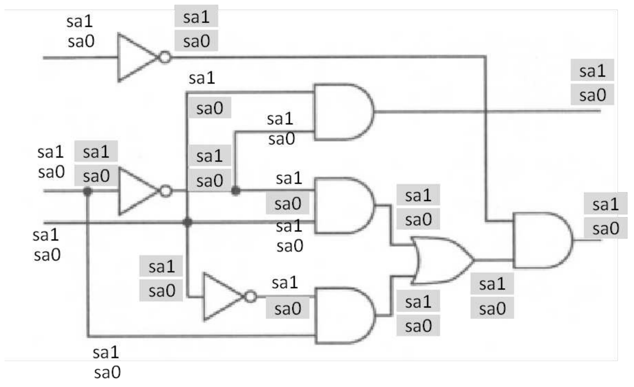
- If CK is stuck-at-0 or stuck-at-1, the FF will keep "X"
- If one of the input or the output of the AND gate is stuck-at-0, the FF cannot be initialized $Q = 1$

Problem 4.11:

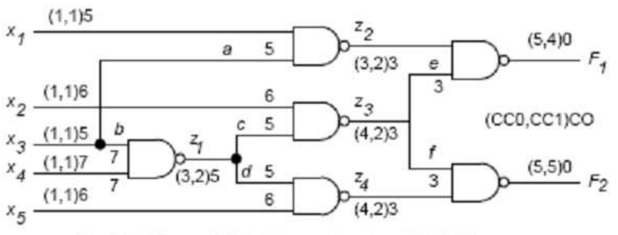
(a) 18
(b) 20/36



(c) 15/36



Problem 6.4:

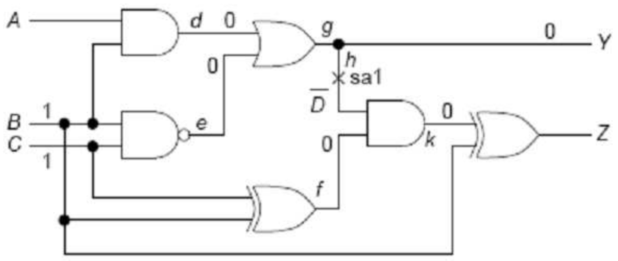


Circuit of Figure 6.22 with combinational SCOAP measures.

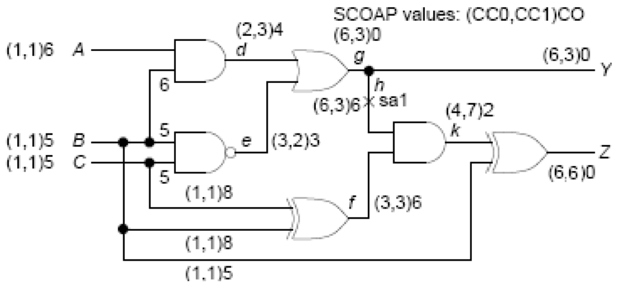
Problem 7.3:
We level order the signals and proceed as follows:

Step no.	Action	A	B	C	d	e	f	g	Y	h	k	Z	D front.	Impl. stack
1	Fault Activation							0	0	$\overline{D}$			k	$g=0$
	Immediate impl.				0	0		0	0	$\overline{D}$			k	$g=0$
	Immediate impl.		1	1	0	0		0	0	$\overline{D}$			k	$g=0$
	Immediate impl.		1	1	0	0	0	0	0	$\overline{D}$			k	$g=0$
	Immediate impl.		1	1	0	0	0	0	0	$\overline{D}$	0		ϕ	$g=0$
	Immediate impl.		1	1	0	0	0	0	0	$\overline{D}$	0	1	ϕ	$g=0$

The fault redundant because the D-frontier disappeared. No backtracks. Signals are shown in the following figure.



Problem 7.5:
The figure below shows the SCOAP testability measures used for guiding PODEM.



The steps of the PODEM algorithms are recorded in the following table:

Step No.	Objec-tive	Action	Imp. stack	A	B	C	d	e	f	g	h	k	Y	Z	D front.	X path
				Implied signal values												
1	$g=0$	Backtrace	$B=1$		1										ϕ	ok
2	$g=0$	Backtrace	$C=1$ $B=1$		1	1		0	0			0		1	ϕ	none
3	$g=0$	Backtrack	$C=0$ $B=1$		1	0		1	1	1	1	1	1	0	ϕ	none
4	$g=0$	Backtrack	$B=0$		0		0	1		1	1		1		ϕ	none
5	$g=0$	Backtrack	Empty													
Algorithm termination: Objective g=0 is impossible; fault h s-a-1 is redundant.																

Explanation: an X-path is a path from the fault site to a PO, such that the signals on it are either faulty states or undetermined. An "ok" for X-path in the table means that one or more such paths exist. Having no X-path is a reason for *backtrack* because its existence is a necessary condition for the detection of the fault. When a series of backtracks leads to an *empty* stack, it indicates that the objective $g = 0$ is impossible. As a result, **the fault h s-a-1 cannot be activated and, hence, it is redundant.** Three backtracks.

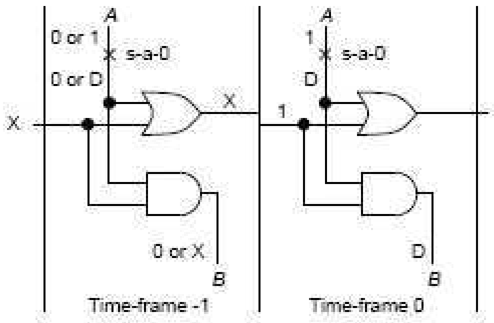
8.5

For test generation with the five-valued algebra, we use the following steps (also see the illustration):

Step 1: Place a D at the output B in time-frame 0.

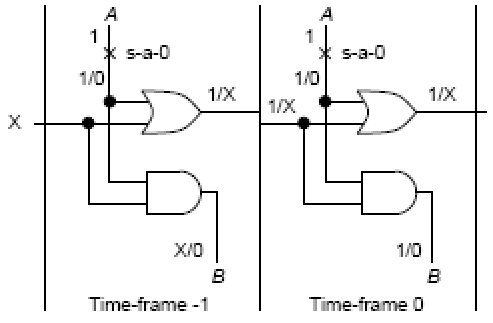
Step 2: This can only be justified by either DD or D1 input to the AND gate in time-frame 0. DD is not possible due to the state input being X in the time-frame -1. We place D1 by applying $A = 1$ and assuming that a state 1 can be justified.

Step 3: Any input, 0 or 1, as shown in the figure, produces a state output X from time-frame -1. Thus, the faulty circuit cannot be initialized to any known state, including the 1 needed for the test. **Hence, it is impossible to find a test by the 5-valued algebra.**



Test generation attempted with 5-valued algebra.

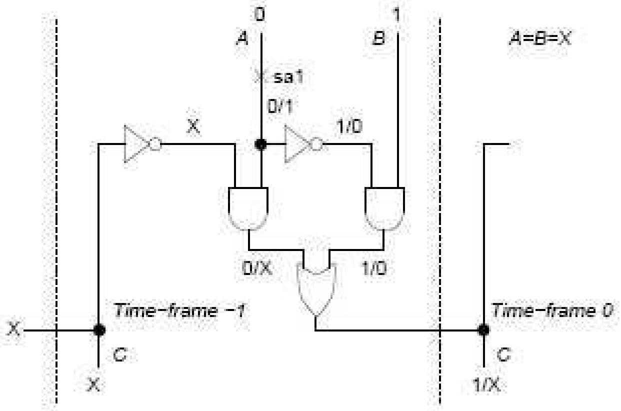
Following similar steps with the nine-valued algebra (see illustration below), we find that two 1's at A detect the fault at B as 1/0 in time-frame 0. Notice that the fault is detected although the faulty circuit is never initialized.

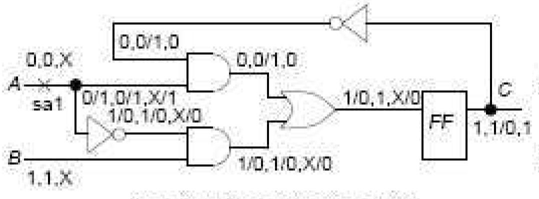


Test generation with 9-valued algebra.

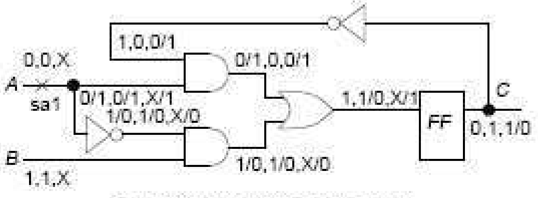
8.6 Initialization fault

The following figure illustrates the time-frame expansion procedure of generating a vector, $A = 0,\ B = 1$, which starting from the unknown state detects the fault A s-a-1 as $1/X$. After the application of the input vector, the flip-flop is clocked before the output can be observed. Even if we add more vectors to the test sequence, the faulty circuit output will not become deterministic. This is because the faulty circuit is not initializable. The fault is only potentially detectable.





Test simulation with initial state 1.



Test simulation with initial state 0.

Note: Some test generators will find the potential detection test of the above type. Others will consider the fault untestable (conservative approach.) Most fault simulators will find the fault potentially detectable. Interestingly, the two test simulation scenarios in the figure show that the fault is definitely detectable, though the detection requires multiple observations. If we assume the initial state to be 1 then the fault is detected as 1/0 after the application of the first clock. However, this output will be 1 (same as the correct output) if the initial state was 0. In this case, repeating the same vector and clocking once again will produce a 1/0 output. A conventional fault simulator will not report such detection because it does not enumerate the possible initial state scenarios. For such multiple observation tests see reference [525] of the book.

8.7

The *note* in the solution of Problem 8.6 explains the operation of a multiple observation test. Besides simulation, a multiple observation test can also be derived by the following procedure.

An observable state variable, which cannot be initialized in the faulty circuit but must be observed for fault detection, is represented symbolically by a Boolean variable s. Inversion of s is $\overline{s}$. A test sequence is derived such that any one of the following pairs of outputs is produced:

- $0/s$ and $0/\overline{s}$
- $1/s$ and $1/\overline{s}$
- $0/s$ and $1/s$
- $0/\overline{s}$ and $1/\overline{s}$

We notice that irrespective of the value the uninitialized state variable assumes, one element in each test output pair will provide definite fault detection. For example, the outputs produced by the test (A, B) = (0,1), (0,1) of Problem 8.6 are $1/\overline{s}$ and $1/s$, respectively, which agree with the second pair given above.

When the feedback in the circuit of Figure 8.25 (see page 250 of the book) has no inversion, a test sequence (A, B) = (0,0), (0,1) will produce outputs $0/s$ and $1/s$. This is a multiple observation test. Details on multiple observation tests may be found in reference [525] cited in the book.

Problem 4
There are some parameters to be chosen when running the Fastscan to generate stuck-at test patterns.
1. N-detection

Students can choose different n-detection patterns in the DOFILE using the following command. For an ordinary stuck-at test pattern generation, n = 1.

Command for one-detection : set fault type stuck -DEtections 1
Command for 15-detection : set fault type stuck -DEtections 15

2. Compression of test patterns

Under one-detection (n = 1), students can choose whether compressing the test patterns or not by using the following command. This command cannot be run when multiple-detection is enabled (n > 1).

Command : compress patterns -multiple_detection -reset_au

3. For a circuit, the fault coverage remains the same with or without using N-detection and test-pattern compression. The CPU time needed and the number of patterns generated may vary depending on the parameter selection.

Following is the statistics for c7552 and s38417.

Statistics report for c7552 (one-detection, with compression of test patterns)

```
-------------------------------------------
                                      #faults     #faults
fault class                             (coll.)     (total)
----------------------      -------      -------
```

```
FU (full)                        7550       19946
-----------------------    -------    -------
DS (det_simulation)              7419       19643
TI (tied)                           4          20
RE (redundant)                    127         283
-----------------------    -------    -------
test_coverage                 100.00%     100.00%
fault_coverage                 98.26%      98.48%
atpg_effectiveness            100.00%     100.00%
-------------------------------------------
#test_patterns                              145
#simulated_patterns                         145
CPU_time (secs)                             4.6
-------------------------------------------
```

Statistics report for c7552 (one-detection, no compression of test patterns)

```
-------------------------------------------
                                #faults     #faults
fault class                      (coll.)     (total)
-----------------------    -------    -------
FU (full)                        7550       19946
-----------------------    -------    -------
DS (det_simulation)              7419       19643
TI (tied)                           4          20
RE (redundant)                    127         283
-----------------------    -------    -------
test_coverage                 100.00%     100.00%
fault_coverage                 98.26%      98.48%
atpg_effectiveness            100.00%     100.00%
-------------------------------------------
#test_patterns                              199
#simulated_patterns                         256
CPU_time (secs)                             4.5
-------------------------------------------
```

Statistics report for c7552 (15-detection, no compression of test patterns)

```
-------------------------------------------
                                #faults     #faults
fault class                      (coll.)     (total)
-----------------------    -------    -------
FU (full)                        7550       19946
-----------------------    -------    -------
DS (det_simulation)              7419       19643
TI (tied)                           4          20
RE (redundant)                    127         283
-----------------------    -------    -------
test_coverage                 100.00%     100.00%
fault_coverage                 98.26%      98.48%
atpg_effectiveness            100.00%     100.00%
-------------------------------------------
#test_patterns                             2020
#simulated_patterns                        2752
CPU_time (secs)                            10.0
```

```
-----------------------------------------
```

Statistics report for s38417 (one-detection, with compression of test patterns)

```
-----------------------------------------
                                  #faults    #faults
fault class                        (coll.)    (total)
----------------------   -------   -------
FU (full)                        32741      81956
----------------------   -------   -------
DS (det_simulation)              29254      75291
DI (det_implication)                 7         11
UU (unused)                       3128       6256
RE (redundant)                     140        186
AU (atpg_untestable)               212        212
----------------------   -------   -------
test_coverage                   99.28%     99.72%
fault_coverage                  89.37%     91.88%
atpg_effectiveness             100.00%    100.00%
-----------------------------------------
#test_patterns                                207
#simulated_patterns                           210
CPU_time (secs)                               2.5
-----------------------------------------
```

Statistics report for s38417 (one-detection, no compression of test patterns)

```
-----------------------------------------
                                  #faults    #faults
fault class                        (coll.)    (total)
----------------------   -------   -------
FU (full)                        32741      81956
----------------------   -------   -------
DS (det_simulation)              29254      75291
DI (det_implication)                 7         11
UU (unused)                       3128       6256
RE (redundant)                     140        186
AU (atpg_untestable)               212        212
----------------------   -------   -------
test_coverage                   99.28%     99.72%
fault_coverage                  89.37%     91.88%
atpg_effectiveness             100.00%    100.00%
-----------------------------------------
#test_patterns                                210
#simulated_patterns                           256
CPU_time (secs)                               2.1
-----------------------------------------
```

Statistics report (15-detection, no compression of test patterns)

```
-----------------------------------------
                                  #faults    #faults
fault class                        (coll.)    (total)
```

```
-----------------------   -------   -------
FU (full)                   32741     81956
-----------------------   -------   -------
DS (det_simulation)         29254     75291
DI (det_implication)            7        11
UU (unused)                  3128      6256
RE (redundant)                140       186
AU (atpg_untestable)          212       212
-----------------------   -------   -------
test_coverage              99.28%    99.72%
fault_coverage             89.37%    91.88%
atpg_effectiveness        100.00%   100.00%
-------------------------------------------
#test_patterns                         1878
#simulated_patterns                    2944
CPU_time (secs)                         8.3
-------------------------------------------
```