ECE 538: VLSI System Testing
Spring 2019

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Homework 3

Assigned: February 21, 2019

Due: March 7, 2019 (start of class)

Instructions:
You are required to work on the homework on your own. If you think a question has several interpretations, make reasonable assumptions and state them clearly. Please be neat and legible. Show all work in order to receive partial credit.

Problem 1 (5 + 5 + 5 = 15 points) [Scan testing]

(a) Derive a formula for the testing time (in clock cycles) for a full-scan circuit with n flip-flops, m scan chains, and p test patterns. Ignore the functional inputs and outputs. Determine the test time in milliseconds for the following typical values of the above parameters: n = 100,000; m = 512; $p = 10^6$. Assume a clock frequency of 100 MHz (for both scan shifting and response capture).

(b) Next, derive a formula for the test time for a set of p 2-pattern transition fault vector pairs. Choose a test application scheme from the ones discussed in class. Calculate the numerical value for the testing time for the above parameters. Assume in addition that the response capture clock frequency is 1 GHz.

(c) Imagine yourself as a test engineer at a leading semiconductor company. Your manager wants you to reduce the scan test time for an integrated circuit, which has a single long scan chain, by a factor of 10. However, the designers are reluctant to add additional scan pins by implementing ten scan chains. What alternative techniques can you and the designers explore to reduce test time? Discuss some techniques that you can use to trade-off fault coverage with the testing time.

Problem 2 (5 + 10 = 15 points) [BIST: LFSR/MISR as Pattern Generators]:

(a) Textbook, Problem 15.4 (Page 544)

(b) Textbook, Problem 15.8 (Page 544)

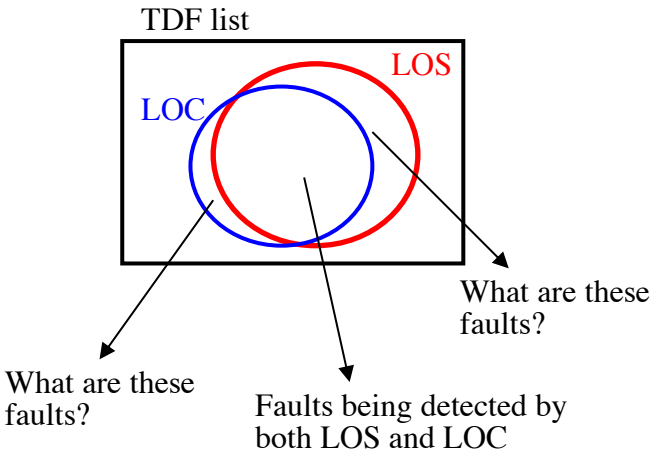
Problem 3 (10+10 = 20 points) [BIST: LFSR/MISR as Signature Registers]:

(a) Textbook, Problem 15.14, 15.15, 15.16 (pp. 545-546)

(b) Textbook, Problem 15.19 (Page 546)

Problem 4 (10 points) [Delay fault testing]

The figure below shows a Venn diagram of fault sets for two transition delay fault (TDF) test methods, i.e., launch-off-shift (LOS) and launch-off-capture (LOC). As seen, there are some faults that are being detected using both LOS and LOC methods. However, there are some other faults that are detected using LOS but not with LOC and vice versa.



Explain what these faults are and why the two methods are incapable of detecting them. What method do you recommend to detect all such faults?