ECE 538: VLSI System Testing

Assignment 4

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Duke Community Standard

By submitting this LaTeX document, I affirm that

1. I have adhered to the Duke Community Standard in completing this assignment.

Problem 1 Path Delay and Small Delay Defect Testing using Synopsys TetraMax:

a. Path Delay Faults

(i)

Number of Critical Paths	50	100	150	200	250	300
Total Faults	50	100	150	200	250	300
Detected	44	82	123	128	129	128
Test Coverage	88.00%	82.00%	82.00%	64.00%	51.60%	42.67%
Patterns	9	18	19	19	19	18
CPU Time	0.02	0.02	0.03	0.02	0.03	0.05

Table 1: Results for path-delay faults, 0.15ns clock period

(ii)

Number of Critical Paths	50	100	150	200	250	300
Total Faults	50	100	150	200	250	300
Detected	44	82	123	128	129	128
Test Coverage	88.00%	82.00%	82.00%	64.00%	51.60%	42.67%
Patterns	9	18	19	18	19	18
CPU Time	0.01	0.03	0.03	0.03	0.03	0.04

Table 2: Results for path-delay faults, 0.10ns clock period

The fault coverage for the 0.15ns/0.10ns path delay fault simulations were exactly the same. Having the same total faults, detected faults, and fault coverage means that— from one timing to the next— no additional delay faults were found on the critical paths tested (i.e., the paths not detected in the 0.15ns simulation had significant enough slack to also not be detected in the 0.10ns simulation). Between simulations, there was one more pattern for the 200 critical path simulation with 0.15ns clock than 0.10ns clock. This means that with the faster clock, fewer patterns were necessary to sensitize a delay long enough to detect. The CPU times were roughly the same for each simulation.

b. Small Delay Defects

(i)

Slack	10%	15%	20%	25%	30%
Total Faults	4094	4094	4094	4094	4094
Detected	3994	3994	3994	3994	3994
Delay Effectiveness	0.11ns(55.17%)	0.165ns(30.75%)	0.22ns(50.08%)	0.275ns(49.82%)	0.33ns(53.68%)
SDQL	6289088.50	6126893.50	5438607.50	4897204.50	4477742.50
CPU Time	0.07	0.07	0.07	0.08	0.08

Table 3: Results for small delay defects, 1.1ns clock period

(ii)

Slack	10%	15%	20%	25%	30%
Total Faults	4094	4094	4094	4094	4094
Detected	3994	3994	3994	3994	3994
Delay Effectiveness	0.12ns(6.64%)	0.18ns(49.23%)	0.24ns(25.95%)	0.30ns(44.24%)	0.36ns(49.65%)
SDQL	5756102.00	5206344.50	5301291.50	4501716.00	4122875.25
CPU Time	0.08	0.06	0.07	0.07	0.08

Table 4: Results for small delay defects, 1.2ns clock period

The delay-effectiveness for almost all simulations using 1.2ns clock period (with the sole exception of 15% slack) was much lower than for the 1.1ns clock period simulations of the same slack-percentage. This means that fewer of the small delay defects could be detected in a circuit with a higher clock period. This is potentially because the small delay defects for a higher clock period (but with same percentage slack) have a longer path to sensitize— so fewer tests will be able to do so. The SDQL values for the 1.1ns simulations are relatively higher than those for their 1.2ns simulation counterparts. This is most-likely the case because of the delay-defect distribution (i.e., there are more small-delay defects that with little slack when the clock period is relatively smaller). The CPU times stayed relatively the same.

(iii)

Slack	10%	15%	20%	25%	30%
Total Faults	4094	4094	4094	4094	4094
Detected	3994	3994	3994	3994	3994
Delay Effectiveness	0.10ns(44.24%)	0.15ns(45.63%)	0.20ns(50.85%)	0.25ns(51.03%)	0.30ns(58.95%)
SDQL	6445672.00	5683769.50	5567790.00	5023122.00	4668992.50
CPU Time	0.07	0.08	0.08	0.08	0.08

Table 5: Results for small delay defects, 1.0ns clock period