ECE 538: VLSI System Testing
Spring 2019

Krish Chakrabarty

Homework 2

Assigned: February 5, 2019

Due: February 19, 2019 (start of class)

Instructions:
You are required to work on the homework on your own. If you think a question has several interpretations, make reasonable assumptions and state them clearly. Please be neat and legible. Show all work in order to receive partial credit.

Problem 1 (10 points) [Fault modeling and fault analysis]:
(a) Textbook problem 4.2 (page 79)
(d) Textbook problem 4.11 (page 80)

Problem 2 (20 points) [Testability measures and combinational test generation]:
(a) Textbook, problem 6.4 (page 151)
(b) Textbook, problem 7.3 (page 207)
(c) Textbook, problem 7.5 (pp. 207-208)

Problem 3 (20 points) [Sequential circuit test generation]:
(d) Textbook, problem 8.5 (page 250)
(e) Textbook, problem 8.6 (page 250)
(f) Textbook, problem 8.7 (page 250)

Problem 4 (10 points) [ATPG using Mentor Graphics Fastscan]: Use Fastscan to generate stuck-at test patterns for benchmark circuits c7552 and s38417. Please go through the Fastscan tutorial posted on the website. You can download Verilog files from:
http://www.ee.duke.edu/~krish/teaching/ECE269/c7552.v
http://www.ee.duke.edu/~krish/teaching/ECE269/s38417.v
Present your results in the form of a screen dump as shown in the tutorial. List the fault coverage obtained, CPU time needed, and the number of patterns generated.