Hardware Design and Implementation of Digital Pulse Processor using FPGA

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Abstract - *A new data acquisition (DAQ) system was developed to fulfill the requirements of the X-ray spectrometer, providing high-resolution spectroscopy at very high-count rate. This system is based on FPGA, able to perform real time algorithm for data reduction and digital pulse processing. The DAQ system consists of digital filter, edge detector, energy resolver and so on. The main filter is based on the conventional digital time-invariant trapezoidal shaper operating. The DAQ system is implemented by Altera FPGA Cyclone III. Our proposed design is solved the previous design problem that baseline is increased gradually.*

Keywords: Digital Pulse Processing, FPGA, Digital Spectroscopy, XRF, USB

1 Introduction

European Union (EU) were fermented the RoHS directive since July 2006. According to this rule, if it contains more than standard concentration, the electrical and electronic equipment does not sell them in the European market[1],[2]. And so "IEC 62321 RoHS Test Method" has been adopted analytical method such as XRF, AAS, ICP-OES, ICP-MS, GC-MS, so on. AAS, ICP-OES, ICP-MS, GC-MS methods are as accurate and precise analysis is possible[3]~[5].

But these methods contain disadvantages that are complexity of pre-processing. The sample preprocessing comes some errors and time consuming. Also preprocessing is drawback the requiring skills. XRF is provided poor precision compare to AAS, ICP-OES, ICP-MS, GC-MS. But XRF is not limited time, place and size of sample. XRF has some advantages. These are that fast time to analyze the various elements and simple preprocessing or preprocessing process can be measured non-destructively. Portable XRF limits of the place, nor the size of the samples are less affected and proficiency. Portable XRF market will be increased gradually. In this study, DAQ system has been implemented for obtaining spectral data. XRF system has been implemented by the Altera FPGA Cyclone III. It operates 25MHz. ADC is 14 bits resolution. To improve the compatibility, external I/O uses USB interface.

2 Hardware Structure

Many DAQ systems have been developed based on the gamma-ray[6]~[9]. But in this paper, system is based on X-ray. DAQ system's hardware architecture is proposed as shown in Fig. 1. The system through input of the ADC(resolution 14bits) was connected directly to the FPGA.

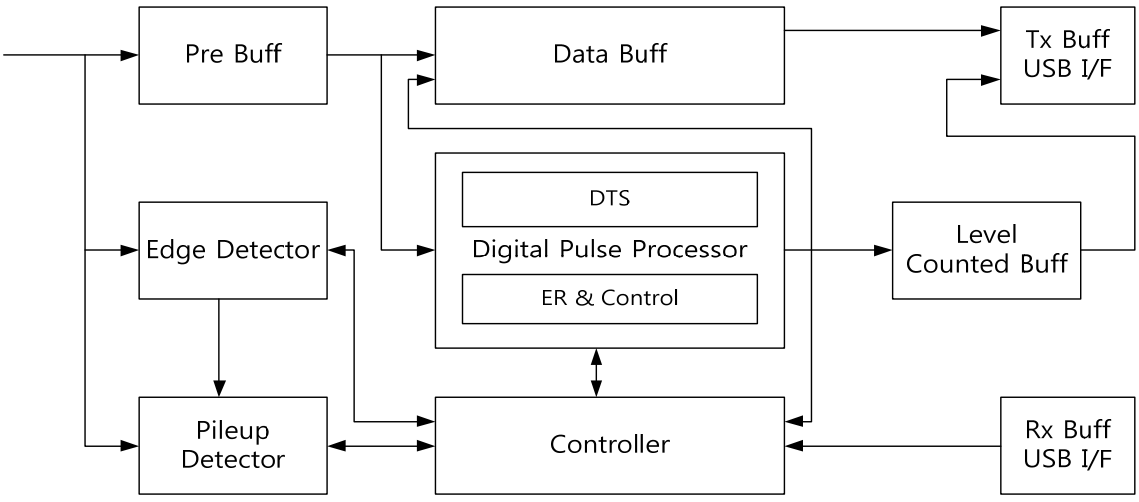


Figure 1. DAQ system Block Diagram

From the ADC input data temporarily stored at the pre-buffer. In the same time to determine whether the data is validated. Depending on the results validity of the data, the temporarily data is stored in the Data Buffer. The stored data is able to transfer to another device, or to calculate the time constant of the pulse data.

Hardware configuration is divided into three major blocks. First part is peak detecting part. It is to search the amplitude and position of the peak. Second part is DPP(Digital Pulse Processing) part. In this part, we calculate the maximum value of the pulse.

This value is flat-top. spectrum data is obtained by the DPP. The last part is controller part. Controller block consists of the register, external I/O interface, counter and memory controller.

3 Hardware Structure

Peak detecting part, as shown in Fig 1, is composed of edge detector and pileup detector. Edge detector is to detect the pulse from ADC input data. And pileup detector is to decide block through input pulse data.

To obtain spectral data, Digital Pulse Processor calculates the maximum of input pulse data. In this paper, to distinguish input pulse data from ADC, edge detector is designed based on the differentiator.

It is continuously monitoring and detecting pulse data. And it judges validity of the data using generated pulse interval or time constant.

3.1 Edge Detector

Edge Detector is to detect the pulse and to calculate the difference between the input data. Differential pulse occurs when the value is changed sharply. But also noise suddenly changes the derivative. We must remove the noise effect. So, We adapt two method.

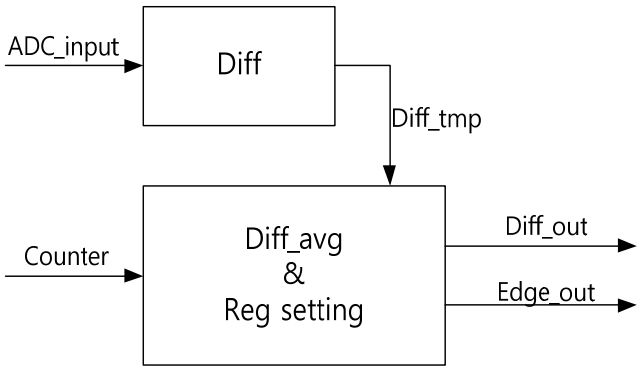


Figure 2. Design of Edge Detector

- First step, when the pulse occurs, the differential value is more than a certain threshold.
- Second step, if pulse is generated, we calculate weighted averages using the around differential value.
- Conventional methods used in the differential, using data from multiple channels and found the pulse. But our design is used just a single channel data. Previously method use the gamma-ray, but proposed design is used X-ray.
- Fig 2 is block diagram of the Edge Detector. Hardware blocks compose of 'Diff' and 'Diff_avg' blocks. Diff block is calculated differential value from input data. Diff_avg block is compared pulse conditions.

3.2 Pileup Detector

Spectral data can be obtained from the DAQ system. When the pulse occurs, spectrum data is generated. However, sometimes overlapping pulses can be generated.

The pileup is that multiple pulse are generated overlapping in a set of data. If pulse contains overlapping, it is difficult to obtain the correct peaks of the multiple pulses.

At this reason, hardware designer does not use the overlapping pulse data. They only use the correct input data. In this paper, pileup detector module was designed by Edge Detector(ED) and Counter.

The pileup generates when the pulse is detected several times by the ED. Then this block performs initialization of each register and the input data set removal.

Fig 3 is pileup detector's block diagram. Hardware design is very simply. But this module strongly detects the pileup. F/F is reset when counter is reached control value

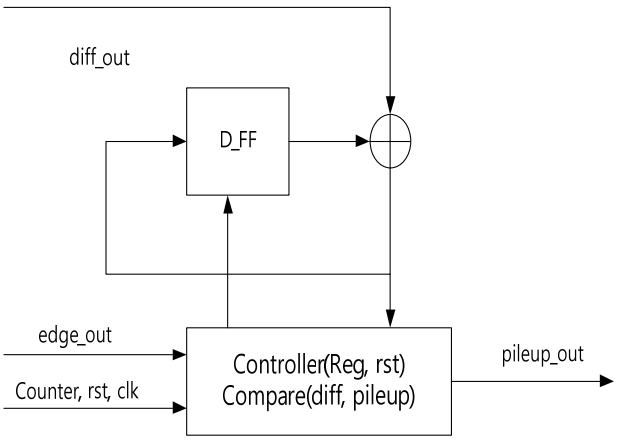


Figure 3. Design of Pileup Detector

4 Digital Pulse Processor

Spectral data can be obtained by the Edge Detector and Pileup Detector modules. Digital Trapezoidal Shaper(DTS) calculates flat-top value using pre-buffer data. At that time, calculated float-top value is the maximum of the pulse.

Flat-top value means spectrum level. Spectral data is consisted of counted value the spectrum level. XRF system uses the spectral data. Our design is used DTS to calculate the level of the pulse. Also, Energy Resolver is applied to remove the baseline.

4.1 Digital Trapezoidal Shaper(DTS)

Many algorithms have been developed to calculate the peak of pulse data[10]~[14]. In this paper, we adapted trapezoidal algorithm. This algorithm finds maximum of pulse using flat-top. Trapezoidal function was implemented according to the following formula:

$$d_n^{k,l}(t) = v_n(t) - v_n(t-k) - v_n(t-l) + v_n(t-k-l) \quad (1)$$

$$p_n(t) = p(t-1) + \sum_{i=0}^{n} d_i^{k,l}(t) \quad (2)$$

$$r_n(t) = p_n(t) + M * d_i^{k,l}(t) \quad (3)$$

$$S_n(t) = S(t-1) + \sum_{i=0}^{n} r_i \quad (4)$$

- DTS module basically consists of adder, subtracter and two kinds of shift register.

- Equation (1), input data delayed k and l clocks then calculate result of adder and subtracter operation.

- These results fed into the high pass filter to remove the pole-zero cancelation, eq (2).

- The pulse energy is calculated using M value that reflects pulse of time constant, eq (3).

- Finally, the spectrum data obtained from flat-top.

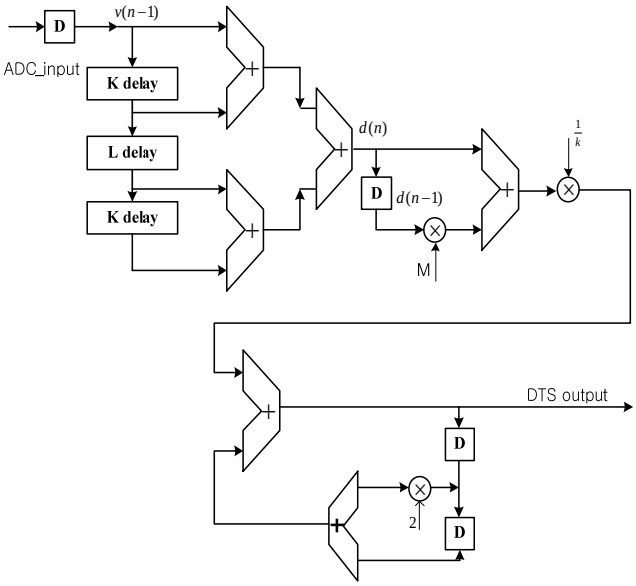


Figure 4. Hardware Design of DTS

- Figure 4 is hardware architecture of DTS. It consists of some shift register, delay and Arithmetic and Logic Unit(adder and subtracter).

4.2 Energy Resolver

In the previous method[15], result of DPP continuously increases such as step function. It is that baseline is not reset because of continuous input.

In this paper, we proposed baseline reset method. This method calculates baseline during detected pulse data before(using the average of the input data).

Proposed method is very simple and DTS module configuration can be applied in real time. Figure 5 is block diagram of energy resolver. It is very simple. And it will be applied real time system.

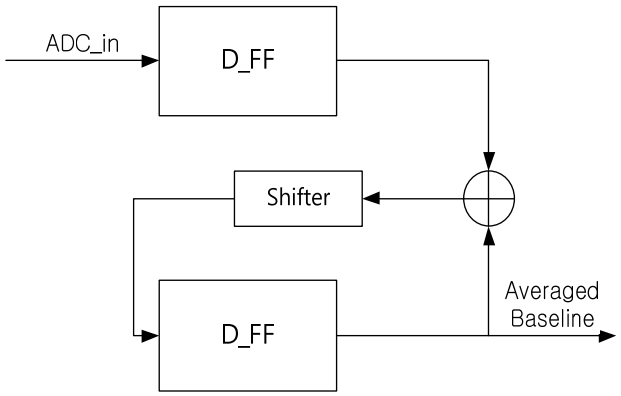


Figure 5. Block Diagram of Energy Resolver

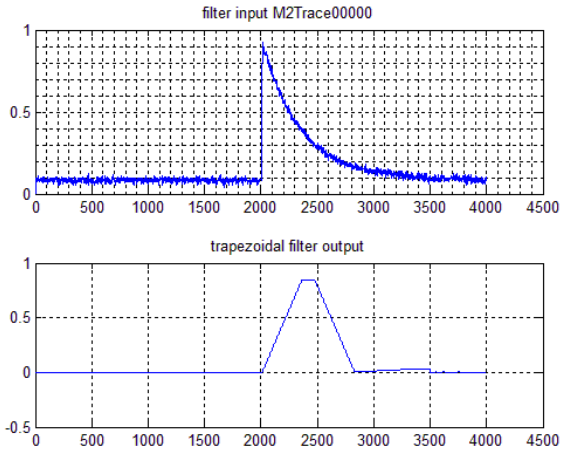


Figure 6. Auctual input and DTS output

5 Control & Extensional I/O

The controller was implemented based on the counter. Differential signal was used as interrupts. For example, pileup generates if additional differential signal is detected during the edge detector generating signals. In addition, ED is detected exceeded at least 24 samples to improve the accuracy of Energy Resolver. XRF system uses DTS operation results that collected during sample period time. Actually, component analysis is done using external devices such as PC, DSP, Embedded system. We were considering USB interface for convenience connection. In this paper, the data set consists of 1000 samples. Figure 6 is DTS resulting waveform using Matlab simulation.

6 Experiment Result

In this paper, we proposed hardware architecture of DAQ system. It is synthesized using Quartus II and simulated by ModelSim 6.5b[16]. DAQ system is implemented using Alter FPGA Cyclone III. Also, we adapts external I/O interface USB. We will be expected that helps to ensure the scalability and versatility. Figure 7 is simulation results of each hardware blocks.

6.1 Edge Detector & Pileup Detector

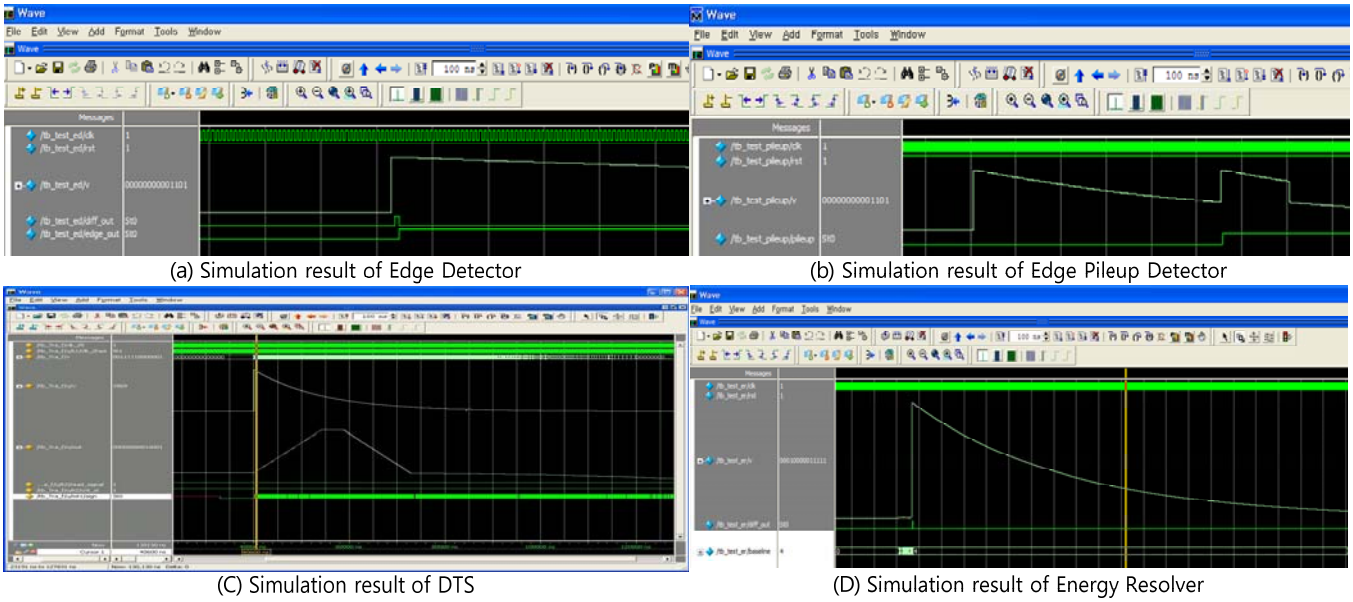
Edge Detector simulation result is Fig.7.(a). In the middle of graph, amplitude of the input signal is changing rapidly. Accordingly, differential signal occurs. Then ED signal is maintained until the end of processing or pileup detecting.

Pileup detector simulation result is Fig.7.(b). As shown in fig.7. pulse is overlapped. As a result, Pileup detecting signal created. In the proposed design, counter continues to operate until it reaches the set value. Then ED, Pileup, ER module turns initial value.

6.2 DTS & Energy Resolver

DTS simulation result is Fig.7.(c). Result of DTS is the flat-top. As you know from the simulation results, flat-top is related the time constant.

Energy resolver simulation result is Fig.7.(d). Pulse occurs, then data occurred prior to calculate the energy resolver(ER). ER pulse is detected, current value is maintained. After processing of the data set, ER is initialized.



(a) Simulation result of Edge Detector

(b) Simulation result of Edge Pileup Detector

(C) Simulation result of DTS

(D) Simulation result of Energy Resolver

Figure 7 Simulation Results of the each Blocks

7 Conclusions

DAQ system was designed and implemented using Alter Cyclone III FPGA. It synthesis of Quartus II[16] and simulates using ModelSim. Our design is operating at 25MHz.

Previous design using gamma-ray had been serious problem. That is continuously increase baseline. To remove this problem, we add reset block. When processing a set of data, the baseline was used to reset the registers.

Also we calculate average of input data is detected pulse before. Our design is very simple and powerful. To improve the compatibility, external I/O uses USB interface.

Acknowledgment

This research was financially supported by the Ministry of Education, Science Technology (MEST) and National Research Foundation of Korea(NRF) through the Human Resource Training Project for Regional Innovation.

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