

Tutorial 6

CACHES

CS3021 Computer Architecture

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1 Q1.

1.1 (i)

tag	4 word 16 bytes			
000,220,110,008	0000,2200,1100,0080	0004,2204,1104,0084	0008, 2208,1108,0088	000C,220C,110C,008C
001,339	0010,3390	0014,3394	0018,3398	001C,339C
002,00A	0020,00A0	0024,00A4	0028,00A8	002C,00AC
113,00B	1130,00B0	1134,00B4	1138,00B8	113C,00BC
004	0040	0044	0048	004C
00D	00D0	00D4	00D8	00DC
00E, 006	00E0,0060	00E4,0064	00E8,0068	00EC,OO6C
007	0070	0074	0078	007C

address set hit/miss 0000 0 M 0004 0 H 000c 0 M 00d0 5 M 00e0 6 M 1130 3 M 0028 2 M 113c 3 H 2204 0 H 0010 1 M 0020 2 H 0040 4 M 2208 0 M 0040 4 M 2208 0 M 0008 0 M 0008 0 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 00b0 3 M 1100 0 M 0028 2	1.1		1
0004 0 H 000c 0 H 2200 0 M 00d0 5 M 00e0 6 M 1130 3 M 0028 2 M 113c 3 H 2204 0 H 0010 1 M 0020 2 H 0040 4 M 2208 0 M 0008 0 M 0008 0 M 0000 2 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M			,
000c 0 H 2200 0 M 00d0 5 M 00e0 6 M 1130 3 M 0028 2 M 113c 3 H 2204 0 H 0010 1 M 0020 2 H 0004 0 M 0040 4 M 2208 0 M 0008 0 M 0008 0 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H			
2200 0 M 00d0 5 M 00e0 6 M 1130 3 M 0028 2 M 113c 3 H 2204 0 H 0010 1 M 0020 2 H 0004 0 M 0040 4 M 2208 0 M 0008 0 M 0008 0 M 0000 2 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H		-	
00d0 5 M 00e0 6 M 1130 3 M 0028 2 M 113c 3 H 2204 0 H 0010 1 M 0020 2 H 0004 0 M 0040 4 M 2208 0 M 0008 0 M 0008 0 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 0084 0 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M			
00e0 6 M 1130 3 M 0028 2 M 113c 3 H 2204 0 H 0010 1 M 0020 2 H 0004 0 M 0040 4 M 2208 0 M 0008 0 M 0008 0 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M			
1130 3 M 0028 2 M 113c 3 H 2204 0 H 0010 1 M 0020 2 H 0004 0 M 0040 4 M 2208 0 M 0008 0 M 0000 2 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 0084 0 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M			
0028 2 M 113c 3 H 2204 0 H 0010 1 M 0020 2 H 0004 0 M 0040 4 M 2208 0 M 0008 0 M 0000 2 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 000c 0 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M			
113c 3 H 2204 0 H 0010 1 M 0020 2 H 0004 0 M 0040 4 M 2208 0 M 0008 0 M 0000 2 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 000c 0 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	1130		
2204 0 H 0010 1 M 0020 2 H 0004 0 M 0040 4 M 2208 0 M 0008 0 M 0000 2 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M			
0010 1 M 0020 2 H 0004 0 M 0040 4 M 2208 0 M 0008 0 M 0008 0 M 0000 2 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 000c 0 M 3390 1 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	113c	3	
0020 2 H 0004 0 M 0040 4 M 2208 0 M 0008 0 M 0000 2 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 0084 0 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	2204	0	
0004 0 M 0040 4 M 2208 0 M 0008 0 M 0000 2 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 000c 0 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	0010		M
0040 4 M 2208 0 M 0008 0 M 00a0 2 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 000c 0 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	0020	2	Н
2208 0 M 0008 0 M 00a0 2 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 000c 0 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	0004	0	M
0008 0 M 00a0 2 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 000c 0 M 0390 1 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	0040	4	M
00a0 2 M 0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 000c 0 M 3390 1 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	2208	0	M
0004 0 H 1104 0 M 0028 2 M 000c 0 M 0084 0 M 000c 0 M 3390 1 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	0008	0	M
1104 0 M 0028 2 M 000c 0 M 0084 0 M 000c 0 M 03390 1 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	00a0	2	M
0028 2 M 000c 0 M 0084 0 M 000c 0 M 3390 1 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	0004	0	H
000c 0 M 0084 0 M 000c 0 M 3390 1 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	1104	0	M
0084 0 M 000c 0 M 3390 1 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	0028	2	M
000c 0 M 3390 1 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	000c	0	M
3390 1 M 00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	0084	0	M
00b0 3 M 1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	000c	0	M
1100 0 M 0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	3390	1	M
0028 2 H 0064 6 M 0070 7 M 00d0 5 H 0008 0 M	00b0	3	M
0064 6 M 0070 7 M 00d0 5 H 0008 0 M	1100	0	M
0070 7 M 00d0 5 H 0008 0 M	0028	2	Н
00d0 5 H 0008 0 M	0064	6	M
0008 0 M	0070	7	M
	00d0	5	Н
3394 1 H	0008	0	M
	3394	1	Н

1.2 (ii)

Table 1: 128 byte 2-way cache with 16 bytes per line (L = 16, N = 4, K=2)

, , , , , , , , , , , , , , , , , , ,											
tag k=0	tag k=1	4 word 16 bytes				4 word 16 bytes					
000,004,008	220	0000	0044	0008	000c	2200	2204	2208	220c		
	110	0040	0044	0048	004c						
		0080	0084	0088	008c	1100	1104	1108	110c		
00d,339	001	00d0	00d4	00d8	00dc	0010	0014	0018	001c		
		3390	3394	3398	339c						
00e,00a	002,006	00e0	00e4	00e8	00ec	0020	0024	0028	002c		
		00a0	00a4	00a8	00ac	0060	0064	0068	006c		
113,007	00b	1130	1134	1138	113c	00b0	00b4	00b8	00bc		
		0070	0074	0078	007c						

	Addre	ess Format
address	set	hit/miss
0000	0	M
0004	0	H
000c	0	H
2200	0	M
00d0	1	M
00e0	2	M
1130	3	M
0028	2	M
113c	3	H
2204	0	Н
0010	1	M
0020	2	Н
0004	0	Н
0040	0	M
2208	0	M
0008	0	M
00a0	0	M
0004	0	Н
1104	2	M
0028	0	Н
000c	0	H
0084	0	M
000c	0	Н
3390	1	M
00b0	3	M
1100	0	M
0028	2	Н
0064	2	M
0070	3	M
00d0	1	M
0008	0	Н
3394	1	H

13 hits

1.3 (iii)

tag 1	tag 2	tag 3	tag 4	4 word 16 bytes			

Table 3: Address Format s set hit/miss hits/caddress hits/c-misses 0000 0 Μ 0004 0 Н 000cΗ 0 hit 2200 0 Μ Μ 00d01 00e0 0 Μ 1130 Μ 1 0028 0 Μ 113c Η 1 hit 2204 0 Η hit 0010 Μ 1 0020 Η 0 0004 Η 0 0040 0 Μ 2208 0 Η hit 0008 0 Η hit 00a0 0 Μ 0004 0 Η Μ 1104 0 Μ 0028 0 000c0 Η hit 0084 Μ 0 Н 000c 0 hit 3390 1 Μ 00b0 1 Μ Η 1100 0 hit 0028 0 Η hit 0064 0 Μ 0070 Μ 1 00d01 Μ

Η

Н

0

1

hit

hit

0008

3394

tag1	tag2	tag3	tag4	tag5	tag6	tag7	tag8				

Т	able 4	: Address	Format
address	set	hit/miss	hit/ c-misses
0000	0	M	compulsory
0004	0	Н	hit
000c	0	Н	hit
2200	0	M	compulsory
00d0	0	M	compulsory
00e0	0	M	compulsory
1130	0	M	compulsory
0028	0	M	compulsory
113c	0	Н	hit
2204	0	H	hit
0010	1	M	compulsory
0020	0	H	hit
0004	0	H	hit
0040	0	M	compulsory
2208	0	H	hit
0008	0	H	hit
00a0	0	M	compulsory
0004	0	H	hit
1104	0	M	compulsory
0028	0	H	hit
000c	0	H	hit
0084	0	M	compulsory
000c	0	H	hit
3390	0	M	compulsory
00b0	0	M	compulsory
1100	0	Н	hit
0028	0	H	hit
0064	0	M	compulsory
0070	0	M	compulsory
00d0	0	M	capacity
0008	0	H	hit
3394	0	Н	hit

16 hits

2 Q2.

Determine the number of compulsory, capacity and conflict misses for each cache organization in Q1. done in the q1 tables

3 Q3.

Write a program (in C, C++, Java,) to solve Q1. Make sure you can create a generalized cache object with parameters L, K and N. Hand in a copy of your source code and evidence that your program works.

4 Q4.

FOR AN EXTRA 5 MARKS modify your program to simulate a pseudo LRU replacement policy. What are the hit rates for the cache organizations specified in Q1?