

# TOSHIBA MOS MEMORY PRODUCTS

2,048 WORD x 8 BIT STATIC RAM

TMM2016AP-90 TMM2016AP-12  
TMM2016AP-10 TMM2016AP-15

## DESCRIPTION

The TMM2016AP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 90ns/100ns/120ns/150ns and maximum operating current of 80mA/65mA/65mA/65mA. When  $\overline{CS}$  is a logical

high, the device is placed in a low power standby mode in which maximum standby current is 7mA. Thus the TMM2016AP is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2016AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

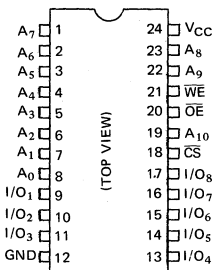
## FEATURES

### • Access Time and Current

Parameter Part Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2016AP-90	90ns	80mA	7mA
TMM2016AP-10	100ns	65mA	7mA
TMM2016AP-12	120ns	65mA	7mA
TMM2016AP-15	150ns	65mA	7mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature:  $\overline{CS}$
- Output Buffer Control:  $\overline{OE}$
- Three Stage Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs protected: All inputs have protection against static charge.

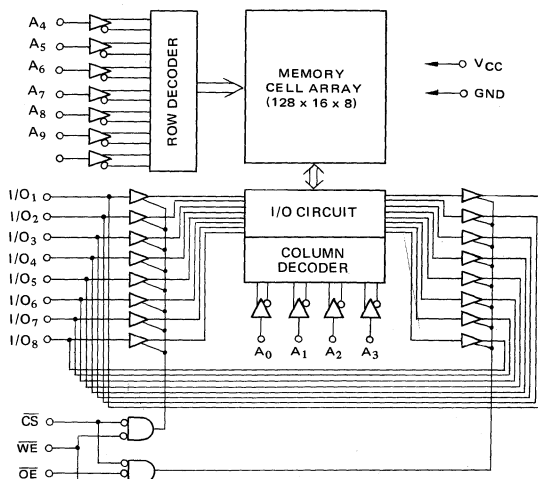
## PIN CONNECTION



## PIN NAMES

SYMBOL	NAME
$A_0 \sim A_3$	Column Address Inputs
$A_4 \sim A_{10}$	Row Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{OE}$	Output Enable Input
$V_{CC}$	Power (5V)
GND	Ground

## BLOCK DIAGRAM



## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
$V_{CC}$	Power Supply Voltage	$-0.5 \sim 7.0$	V
$V_{IN}, V_{OUT}$	Input/Output Voltage	$-0.5 \sim 7.0$	V
$T_{opr.}$	Operating Temperature	$0 \sim 70$	$^{\circ}\text{C}$
$T_{stg.}$	Storage Temperature	$-55 \sim 150$	$^{\circ}\text{C}$
$T_{solder}$	Soldering Temperature • Time	$260 \cdot 10$	$^{\circ}\text{C} \cdot \text{sec}$
$P_D$	Power Dissipation ( $T_a = 70^{\circ}\text{C}$ )	1.0	W

## D.C. RECOMMENDED OPERATING CONDITIONS ( $T_a = 0 \sim 70^{\circ}\text{C}$ )

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{IH}$	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
$V_{IL}$	Input Low Voltage	-0.5	—	0.8	V
$V_{CC}$	Supply Voltage	4.5	5.0	5.5	V

## D.C. CHARACTERISTICS ( $T_a = 0 \sim 70^{\circ}\text{C}$ , $V_{CC} = 5.0\text{V} \pm 10\%$ )

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{IL}$	Input Leakage Current	$V_{IN} = 0\text{V} \sim 5.5\text{V}$	-10	—	10	$\mu\text{A}$
$V_{OH}$	Output High Voltage	$I_{OUT} = -1.0\text{mA}$	2.4	—	—	V
$V_{OL}$	Output Low Voltage	$I_{OUT} = 2.1\text{mA}$	—	—	0.4	V
$I_{LO}$	Output Leakage Current	$\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ , $V_{OUT} = 0\text{V} \sim 5.5\text{V}$	-10	—	10	$\mu\text{A}$
$I_{SBP}$	Peak Power-on Current	$\overline{CS} = V_{CC}$ , $I_{OUT} = 0\text{mA}$	—	—	30	mA
$I_{SB}$	Standby Current	$\overline{CS} = V_{IH}$ , $I_{OUT} = 0\text{mA}$	—	—	7	mA
$I_{CC1}$	Operating Current TMM2016AP-10/-12/-15	$\overline{CS} = V_{IL}$ , $I_{OUT} = 0\text{mA}$	—	—	65	mA
$I_{CC2}$	Operating Current TMM2016AP-90	$\overline{CS} = V_{IL}$ , $I_{OUT} = 0\text{mA}$	—	—	80	mA

## CAPACITANCE\* ( $T_a = 25^{\circ}\text{C}$ , $f = 1.0\text{MHz}$ )

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = \text{A.C. Ground}$	5	pF
$C_{OUT}$	Output Capacitance	$V_{IN} = \text{A.C. Ground}$	10	pF

\* Note: This parameter is periodically sampled and is not 100% tested.

**A.C. CHARACTERISTICS ( $T_a = 0 \sim 70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ )**
**READ CYCLE**

SYMBOL	PARAMETER	TMM2016AP-90		TMM2016AP-10		TMM2016AP-12		TMM2016AP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{RC}$	Read Cycle Time	90	—	100	—	120	—	150	—	ns
$t_{ACC}$	Address Access Time	—	90	—	100	—	120	—	150	ns
$t_{CO}$	Chip Select Access Time	—	90	—	100	—	120	—	150	ns
$t_{OE}$	Output Enable Time	—	35	—	35	—	50	—	55	ns
$t_{OH}$	Output Data Hold Time from Address Change	10	—	10	—	10	—	10	—	ns
$t_{CLZ}$	Output in Low-Z from $\overline{CS}$	10	—	10	—	10	—	10	—	ns
$t_{CHZ}$	Output in High-Z from $\overline{CS}$	—	40	—	40	—	40	—	55	ns
$t_{OLZ}$	Output in Low-Z from $\overline{OE}$	5	—	5	—	5	—	5	—	ns
$t_{OHZ}$	Output in High-Z from $\overline{OE}$	—	35	—	35	—	35	—	50	ns
$t_{PU}$	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
$t_{PD}$	Chip Deselection to Power Down Time	—	50	—	50	—	60	—	60	ns

**WRITE CYCLE**

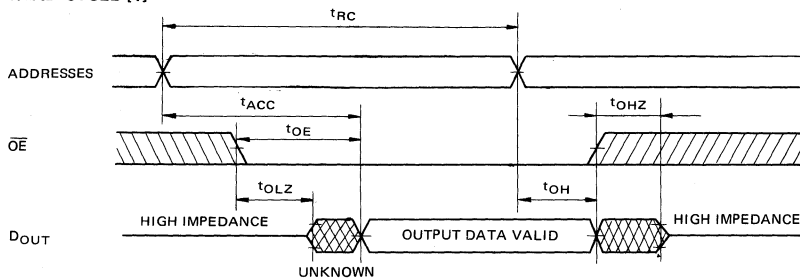
SYMBOL	PARAMETER	TMM2016AP-90		TMM2016AP-10		TMM2016AP-12		TMM2016AP-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{WC}$	Write Cycle Time	90	—	100	—	120	—	150	—	ns
$t_{CW}$	Chip Selection to End of Write	70	—	80	—	100	—	120	—	ns
$t_{AS}$	Address Set up Time	20	—	20	—	20	—	20	—	ns
$t_{WP}$	Write Pulse Width	60	—	70	—	85	—	100	—	ns
$t_{WR}$	Write Recovery Time	0	—	0	—	0	—	0	—	ns
$t_{DS}$	Data Set up Time	35	—	40	—	50	—	60	—	ns
$t_{DH}$	Data Hold Time	0	—	0	—	0	—	0	—	ns
$t_{WLZ}$	Output in Low-Z from $\overline{WE}$	5	—	5	—	5	—	5	—	ns
$t_{WHZ}$	Output in High-Z from $\overline{WE}$	—	25	—	30	—	35	—	50	ns

**A.C. TEST CONDITIONS**

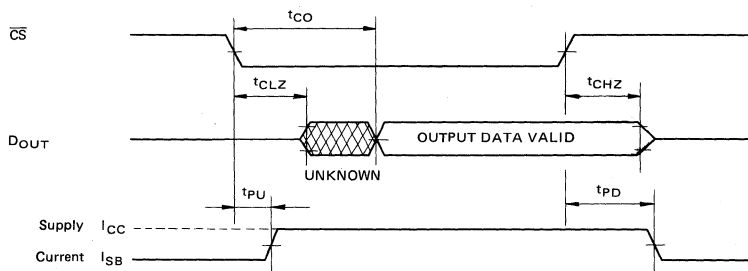
Input Pulse Levels	0 ~ 3.5V
Input Rise and Fall Time	10 ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & $C_L = 100\text{pF}$

## TIMING WAVEFORMS

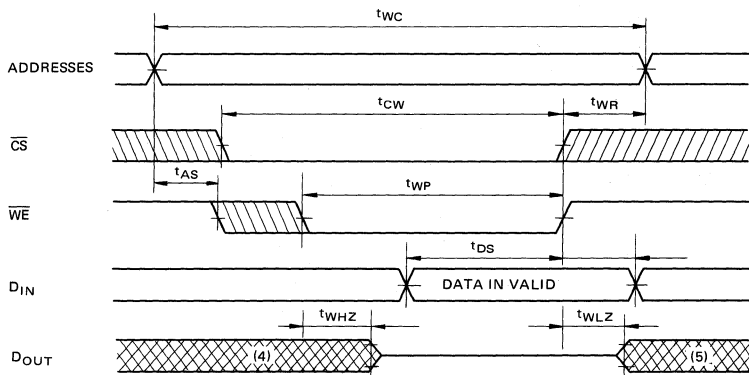
(A) READ CYCLE [1] <sup>(1)</sup>



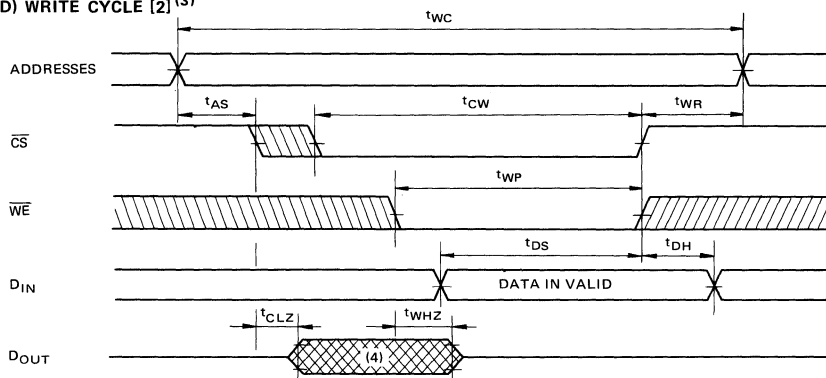
(B) READ CYCLE [2] <sup>(1)(2)</sup>



(C) WRITE CYCLE [1] <sup>(3)</sup>



## (D) WRITE CYCLE [2] <sup>(3)</sup>



Note: (1) The  $\overline{WE}$  is high for read cycle.

Device is continuously selected,  $\overline{CS} = V_{IL}$  in read cycle [1].

(2) All address are valid prior to or simultaneously with  $\overline{CS}$  transitions.

(3) A write occurs during the overlap of low  $\overline{CS}$  and low  $\overline{WE}$ .

The  $t_{CW}$  is specified as the time from the chip selection to end of write in write cycle, and the  $t_{WP}$  is specified as the overlap time of low  $\overline{CS}$  and low  $\overline{WE}$ .

$\overline{OE}$  is allowed to be low or high level in write cycle.

If the  $\overline{OE}$  is high, the output buffers remain in a high impedance state in this period.

(4) If the  $\overline{CS}$  low transition occurs simultaneously with or latter to the  $\overline{WE}$  low transition, the output buffers remain in a high impedance state in this period.

(5) If the  $\overline{CS}$  high transition occurs simultaneously with  $\overline{WE}$  high transition, the output buffers remain in a high impedance state in this period.

These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A)  $t_{CLZ}, t_{OLZ}, t_{WLZ}$  ..... Output Enable Time

(B)  $t_{CHZ}, t_{OHZ}, t_{WHZ}$  ..... Output Disable Time

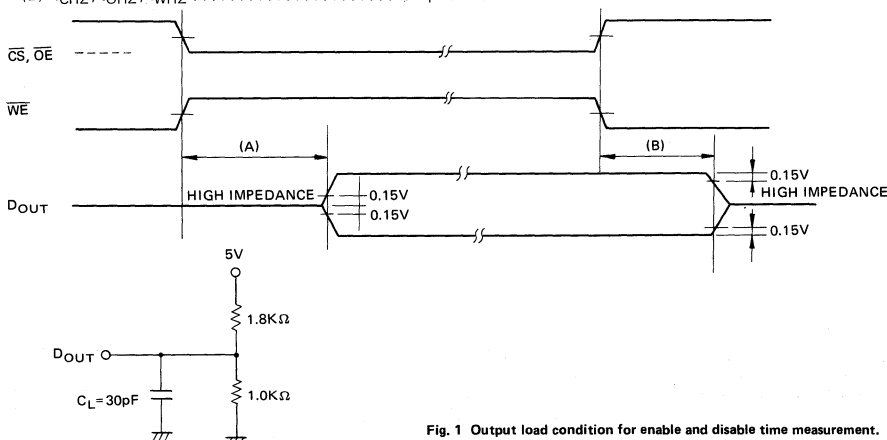
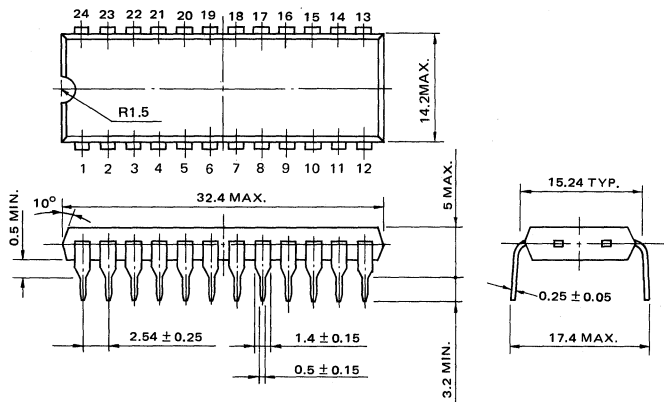


Fig. 1 Output load condition for enable and disable time measurement.

## OUTLINE DRAWINGS

Unit: mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 24 leads.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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