

COMPUTER ENGINEERING DEPARTMENT

SUBJECT: MICROPROCESSOR

COURSE: T.E.

Year: 2020-2021

Semester: V

DEPT: Computer Engineering

SUBJECT CODE: CSC501

EXAMINATION DATE: 07/01/2021

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MICROPROCESSOR ANSWER SHEET

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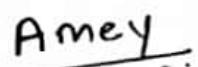
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Date : 07/01/2021

Day : THURSDAY

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Q2.

A. Explain the use of BHE and AO in 8086 based system.

BHE

- BHE stands for Bus High Enable. It is available at pin 34 and used to indicate the transfer of data using data bus D8 - D15. This signal is low during the first clock cycle, thereafter it is active.

AO.

- AO is analogous to BHE for the lower byte of data bus, pins D0 - D7. AO bit is low during T1 state when a byte is to be transferred on the lower portion of the bus in memory or I/O operation. 8-bit oriented devices tied to the lower half word normally use AO to condition chip select function.

Q.2.

B. List and explain any 5 assembler directive

Ans:

Assembly language consists of 2 types of statements

- (1) Executable statements
- (2) Assembler directive

Assembler directives are classified in

- (1) Simplified segment directive
- (2) Data Allocation Directive
- (3) Segment Directive
- (4) Macro related directive
- (5) Code label directive
- (6) scope directive
- (7) listing Control directive
- (8) Miscellaneous directive

① Code.

- This indicates the assemble of the start of the code segment
- The CS register is initialized to such a value that it should point to the location in the beginning along with SS.

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② Data

- This indicates the assembler of the start of data segment.
- The DS register is initialized to such a value that it should point to this location in the beginning.

③ Model

- It is used to indicate the memory requirement of the program.

④ Stack

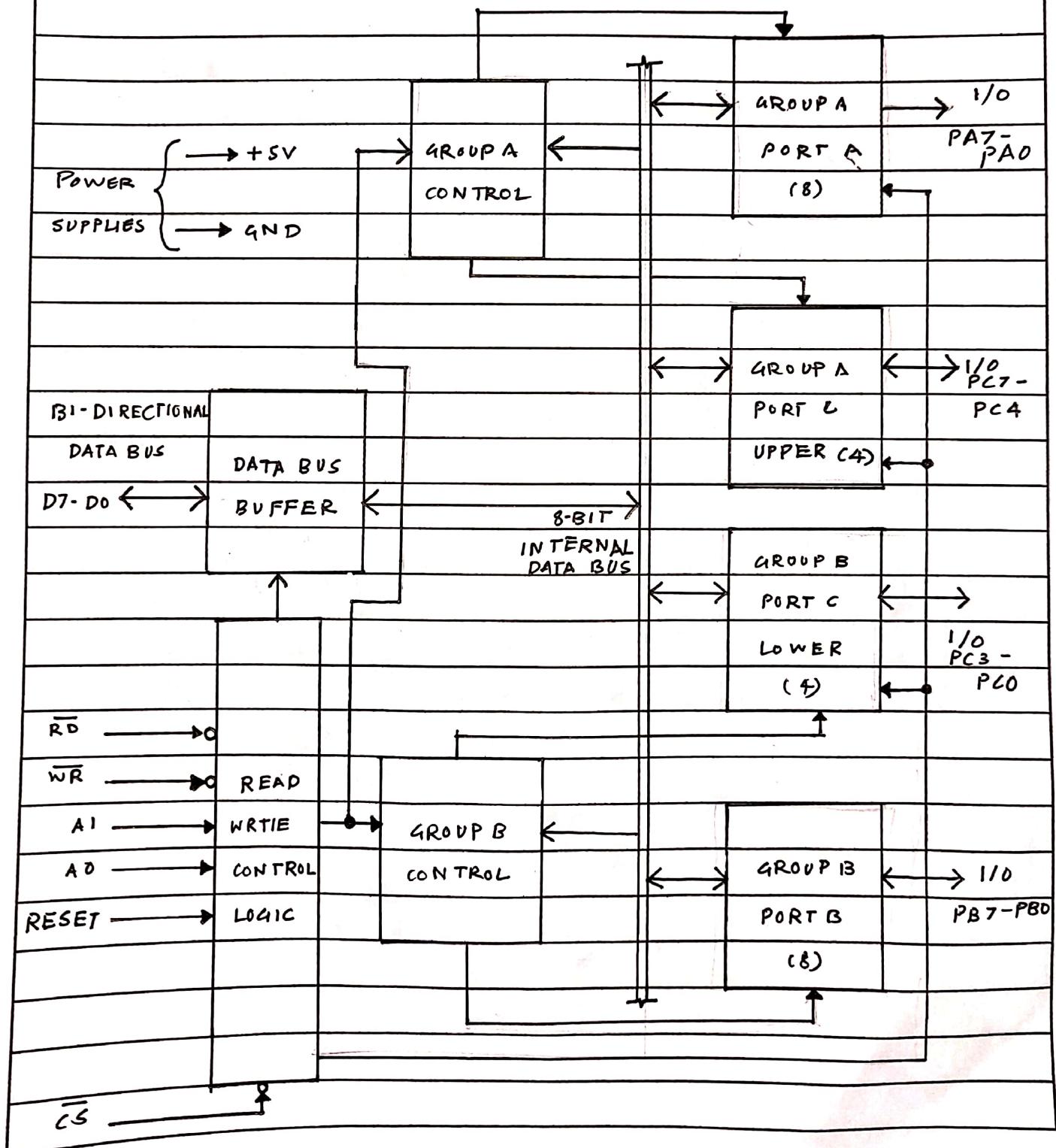
- This indicates the assembler of the start of stack segment.
- The SS register is initialized to such a value that it should point to this location in the beginning.

⑤ EQU - Equate

- EQU stands for Equel or EQUATE.
- It is used to assign a value to a variable or constant.

Q.2.

D Explain mode 2 of 8255 with diagram



- Two modes of 8255.

① Bit Set Reset (BSR) Mode

② Input / Output Mode

① BSR Mode

- This mode is used to set or reset the bits of the port C only. For BSR mode always D7 will be 0. The Control register looks like this.

Bits	D7	D6	D5	D4	D3	D2	D1	DO
Values	0		X		PC bit number		0 or 1	

- The (D3, D2, D1) will be 000 to 111.

In this mode, it affects only one bit of port C at a time. When user set the bit, it remains set until user unset it. The user needs to load the bit program pattern in control register to change the bit.

② IO Mode

- This mode is selected when the D7 bit of the control register is 1.

- This mode has 3 modes.

① Mode 0

② Mode 1

③ Mode 3

Mode 0 - Simple or basic IO mode

- In this mode all of the ports A, B, C can be used as IO mode.

The Outputs are latched. The mode has interrupt handling capability.

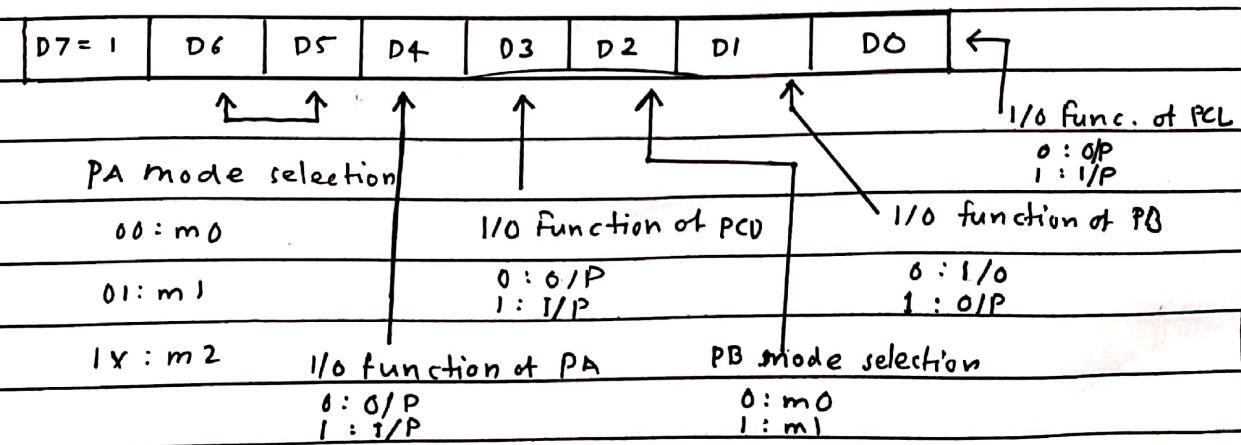
Mode 1 - Handshake IO.

- In this mode the port A and port B can be used as IO ports. The Port C are used for handshaking.

In this mode, the inputs and outputs are latched. This mode has interrupt handling capability.

Mode 3 - Bidirectional IO

- In this mode only port A can work and port B can either be in Mode 0 or mode 1. Port C used for handshaking. In this mode, inputs and outputs are latched.



Q.2.E. Real address mode & Protected address mode

Real Address Mode	Protected Address Mode
① Real mode is also called as Real address mode. It is default operating mode on Reset.	① Protected mode may only be entered after the system software sets up several descriptor tables and enables P.T bit in CR0.
② Its main function is to initialize 80386 for protected mode operation.	② It allows system to utilize features such as virtual memory, segmentation, paging, etc..
③ In real mode of 80386 can access all the registers.	③ segment selection - segment descriptor can be accessed
④ 80386 can directly address upto 1 MB of memory	④ 80386 can access $2^{32} = 4 \text{ GB}$ of memory unit with 32 bit addressing.

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⑤ 80386 register begins its execution in real mode.

⑤ PF bit of CR0 registers must be set

⑥ To leave the real mode and enter protected mode the PF bit of CR0 must be set

⑥ Whenever processor wants to return to real mode the users can clear the PE bit in CR0

Q.2.

F. Floating pipeline stages used in pentium processor

Ans:

- Floating point unit is heavily pipelined hence allowing several instructions to be executed simultaneously under certain conditions
- Most of the floating point instructions have to be the "U" pipeline only and cannot be paired with integer instructions
- The first 4 stages of floating point pipelines are shared with integer pipeline units.
- 4 stages

(1) Prefetch

(2) Instruction decode 1 (D1)

(3) Instruction decode 2 (D2)

(4) Execution stage

- Floating point F1 (Execution):

It reads the information from registers / memory and move them into FP register.

It is also converted to FP format.

- FP E2:

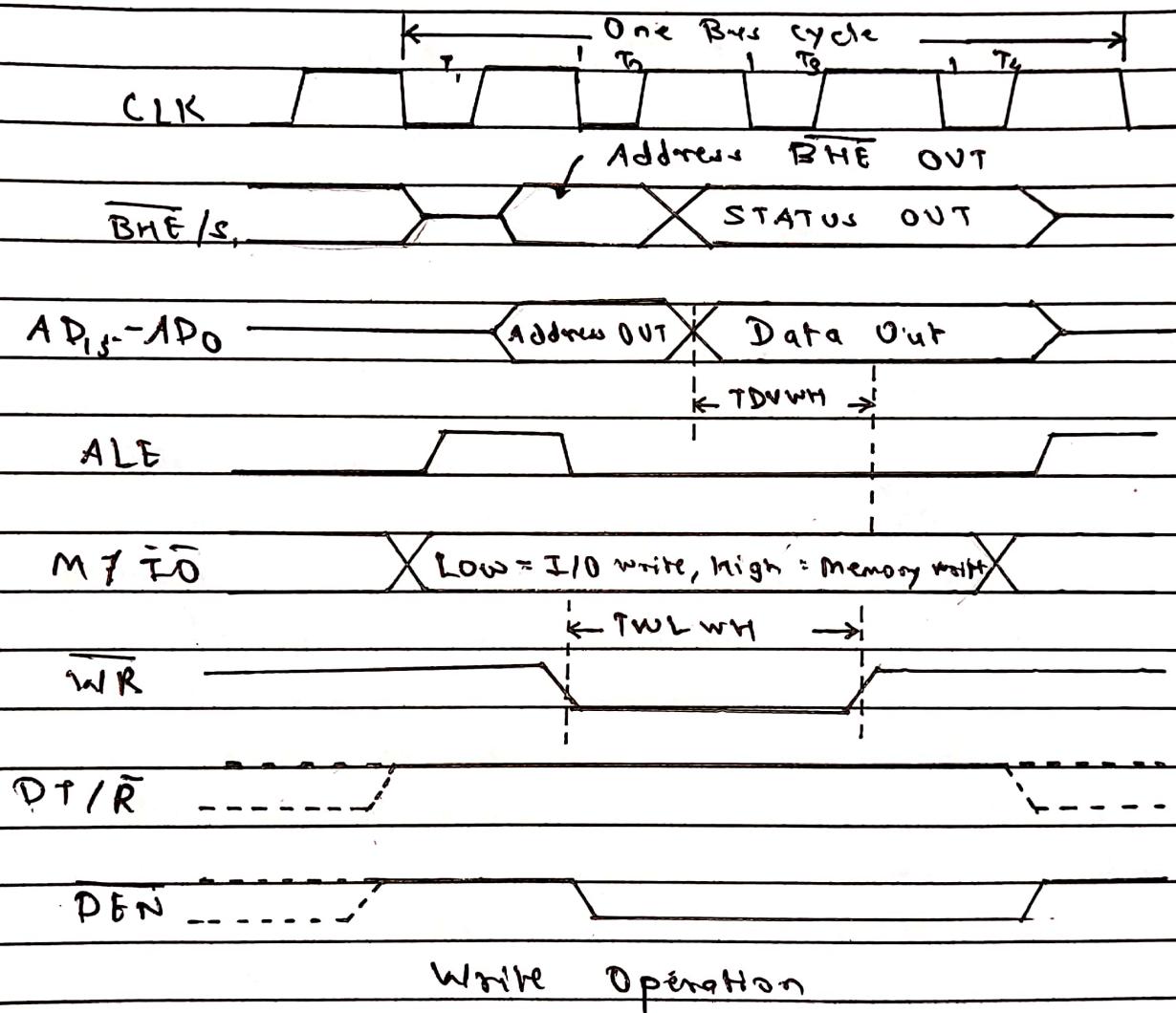
In this stage, the FP operation is performed

- Write FP results

In this stage the result is rounded off and written in targeted FP register.

Q.3

A. Draw and explain timing diagram for write operation in minimum mode of 8086.



The timing diagram for write operation in minimum mode is shown in figure

- When processor is ready to initiate the bus cycle it applies a pulse to ALE during T₁. Before the trailing edge of ALE, the address, BHE, M/I/O, DEN and DT/R must be stable, i.e. DEN = high and DT/R = 0 for input or DT/R = 1 for output.
- At the trailing edge of ALE, ICs 74LS373 or 8282 latch the address.
- During T₂ the address signals are disabled and S3-S7 ale available on AD16 / S3-APlg/S6 and BHE/S7. Also DEN is lowered to enable transceiver.
- In case of input operation, RD is activated during T₂ and ADO to AD15 go in high impedance preparing for input.
- If memory or IO interface can perform the transfer immediately there are no wait states and data is output on the bus during T₃.
- After the data is accepted by the processor, RD is raised high at beginning of T₄. Upon detecting this transaction during T₄ the memory or IO devices will disable its data signal. For an output operation, Processor applies WR = 0 and then the data on the data bus during T₂. In T₄, WR is raised high and data signals are disabled.

- For either input or output operation, DEN is raised during T4 to disable the transceiver. Also M/I/O is set according to the next T1 state. Thus length of bus cycle in 8086 is four clock cycle.
- If the bus is to be inactive after completion of bus cycle, then the gap between the successive cycles is filled by ideal state clock cycles.
- When the memory or I/O device is not able to respond quickly during transfer, wait states (T_w) are inserted between T3 and T4 by disabling the READY.

Q.3

B. Assembly language program for 8086 to check the given string of 10 characters represents palindrome.

Ans:

Data Segment

str1 db 'ABCDEEDCBA', '\$'

strlen1 dw \$ - str1

strrev db 20 dup ('')

str-palin db 'String is not palindrome.', '\$'

Data Ends

Code segment

Assume cs: code, ds: data

Begin

mov ax, data

mov ds, ax

mov es, ax

mov cx, strlen1

add cx, -2

lea si, str1

lea di, strrev

add si, strlen1

add si, -2

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L1 :

mov al, [si]

mov [di], al

dec si

inc di

loop L1

mov al, [si]

mov [di], al

inc di

mov d1, '\' \$ \'

mov [di], d1

mov cx, strlen1

,

Palin - check :

lea si, str1

lea di, strrev

repe cmpsb

jne Not-Palin

Palin :

mov ah, 09h

lea dx, str-palin

int 21h

jmp Exit

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Not - Palin :

mov ah, 09h

lea dx, str-not-palin
int 21h

Exit :

mov ax, 4C00h
int 21h

Code ends

End Begin