

# Quiz Microprocessor

Total points **10/10** ?

Solve all Questions

Email address \*

ameythakur@ternaengg.ac.in

Class : TE B DiV

✗ Name of Student \*

AMEY THAKUR

✗

Correct answer

Correct Answer

✗ Roll No \*

50

✗

Correct answer

Correct Answer



✓ 1. In 8086, Example for Non maskable interrupts are \_\_\_\_\_.

1/1

☒ a) TRAP



☐ b) RST6.5

☐ c) INTR

☐ d) RST6.6

☐ Other: \_\_\_\_\_

✓ 2. In 8086 microprocessor one of the following statements is not true?

1/1

☐ a) coprocessor is interfaced in max mode

☒ b) coprocessor is interfaced in min mode



☐ c) I/O can be interfaced in max / min mode

☐ d) supports pipelining

✓ 3. Which group of instructions do not affect the flags?

1/1

☐ a) Arithmetic operations

☐ b) Logic operation

☒ c) Data transfer operations



☐ d) Branch operations



✓ 4. Which of the following is not an 8086/8088 general-purpose register? \* 1/1

- ☐ a) Code segment (CS)
- ☒ b) Data segment (DS) ✓
- ☐ c) Stack segment (SS)
- ☐ d) Address segment (AS)

✓ 5. The 80386DX is a processor that supports 1/1

- ☐ a) 8-bit data operand
- ☐ b) 16-bit data operand
- ☐ c) 32-bit data operand
- ☒ d) all of the mentioned ✓

✓ 6. The memory management of 80386 supports 1/1

- ☐ a) virtual memory
- ☐ b) paging
- ☐ c) four levels of protection
- ☒ d) all of the mentioned ✓

☐ Other: .....



✓ 7. The 80386 enables itself to organize the available physical memory into 1/1 pages, which is known as

☐ a) segmentation

☒ b) paging ✓

☐ c) memory division

☐ d) none of the mentioned

✓ 8. The instructions that pass through the fetch, decode and execution stages sequentially is known as 1/1

☐ a) sequential instruction

☐ b) sequence of fetch, decode and execution

☒ c) linear instruction sequencing ✓

☐ d) non-linear instruction sequencing

✓ 9. The execution in which the consecutive instruction execution in a sequential flow is hampered is 1/1

☐ a) speculative execution

☒ b) out of turn execution ✓

☐ c) dual independent bus

☐ d) multiple branch prediction



✓ 10. The unit that accepts the sequence of instructions from the instruction cache as input is

1/1

☒ a) fetch-decode unit



☐ b) dispatch-execute unit

☐ c) retire unit

☐ d) none

This form was created inside of Terna.

Google Forms

