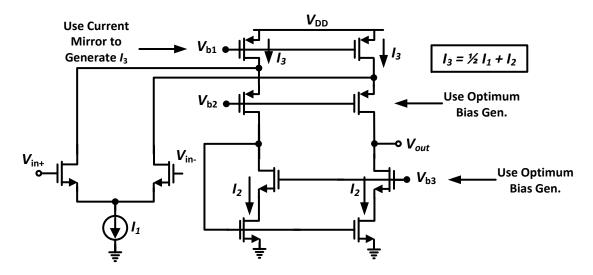
CMOS Operational Amplifier Design

I. Design

The purpose of this project is to design and simulate a folded-cascode operational amplifier used as a buffer.



II. Specifications

You are required to design the single-ended single-stage op-amp shown such that:

- $V_{\rm DD}$ = 3.3V (use **HG devices** with thick oxide and thus will not breakdown for high voltage)
- $V_{\text{inCM}} = V_{\text{DD}} / 2$ (input common-mode voltage)
- $A_{DC} > 55$ dB (DC differential gain)
- GBW > 100 MHz for a load capacitance of C_L =2pF
- Slew Rate $> 100 \text{ V/}\mu\text{sec}$
- Output Swing $> 1.5 V_{pp}$ (Definition of swing is when the DC-gain drops by 10dB)
- Input referred thermal noise density $< 10nV/\sqrt{Hz}$ (Ignore 1/f noise)
- $PM > 60^{\circ}$
- Minimize power consumption
- Do not use ideal current sources (assume that you have only one current source of $25\mu A$ coming from V_{DD}). Use biasing circuit to generate I_1 and optimum bias for V_{b1} , V_{b2} , and V_{b3} .
- Design all current mirrors to provide close to optimum compliance voltage (to obtain maximum output swing). BUT Adjust V_{DS} of any transistor in the current mirror (or current source) to $(V_{eff} + 100 \text{mV})$ in order to improve r_o of this transistor.

III. Simulations

- Simulate the circuit (DC analysis save operating point, AC analysis)
 - Print all transistor operating point information (DC)
 - Plot the gain and phase versus frequency (AC). Show open-loop gain and PM
 - Plot the common-mode rejection ratio (CMRR)
 - Plot the power supply rejection ratio (PSRR)
- Place the op-amp in a unity feedback (**Buffer**) configuration:
 - Simulate stability using STB analysis and IPROBE
 - Plot STB gain and phase versus frequency (AC) and calculate open-loop gain and PM
 - What is the difference between those results and previous open-loop AC results?
 - Plot the DC-gain versus V_{out} (report when DC-gain drops by 10dB to verify specifications)
 - Plot the closed-loop (CL) frequency response. What is A_{CL} and BW_{CL} (comment)?
 - Simulate input-referred noise and tabulate top 4 contributors @10MHz (comment).
 - Simulate the slew rate and verify the specifications.
 - Apply a sine input signal of 1V_{pp} @10MHz and plot V_{out} (add proper input DC value).
 Plot DFT (in dB) and calculate harmonic distortion HD2, HD3, and THD (comment).
 - Plot V_{out} for a small step input of 100mV (add proper input DC value). Calculate the fractional gain error (FGE) and 1% settling time (compare with hand analysis).

IV. Assessment

- The total grade of this project is **5 points**.
- The project can be done by group of 4 students (or less).
- You are required to deliver a report that contains:
 - 1. **Schematic diagrams** (snapshots from Cadence showing dimensions and values)
 - 2. **Design procedure** (hand calculations)
 - 3. **Simulation results** (snapshots from Cadence)
 - 4. **Discussion** of your results and conclusions
- Any missing item from the **4 items above will be penalized in the report grading.** Please be aware that 'bad' presentation (report document, figures, etc.) of your work is going to affect your grade.
- Report size shouldn't exceed 15 pages. A 0.5 point will be deducted for each extra page.
- Deadline to submit the project report (delivered to Eng. Basem Abdelaziz) is <u>12/22/2020</u>.
- Any copied reports or groups more than 4 will be given Zero.