وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog IC Design
Lab 07
gm/ID Design Methodology

Intended Learning Objectives

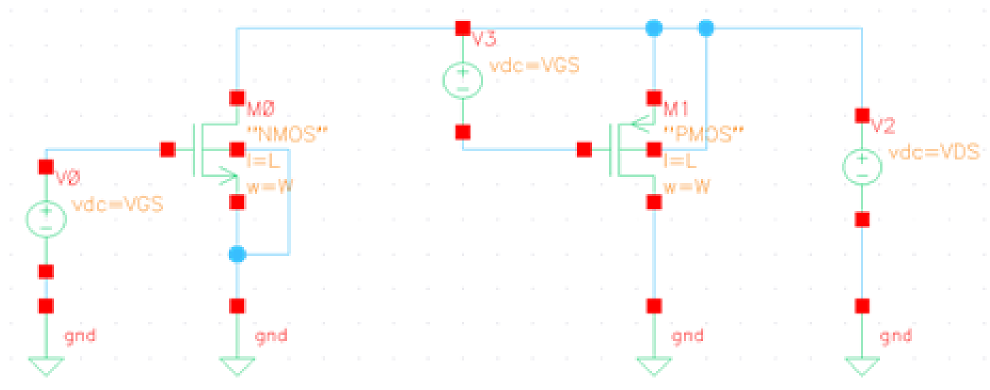
In this lab you will:

- Design and simulate a 5T OTA.
- Learn how to generate and use gm/ID design curves.
- Learn how to simulate the open-loop characteristics of the 5T OTA.
- Learn how to simulate the closed-loop characteristics of the 5T OTA.

PART 1: gm/ID Design Curves

Use the following sweep ranges to characterize NMOS and PMOS transistors.

- W = 10um
- L = 0.2um:0.2um:5um → **parametric sweep**
- VGS ≈ (VTH-100m):5m:(VTH+VDD/3) → **DC sweep**
- VDS = VDD/3



Export simulation results to a csv file then import it in MATLAB.

→ Cadence Hint: In order to save OP point parameters vs DC sweep variable, create an empty text file and write the following statement (without quotes): "save *:oppoint sigtype=dev". Add this text file in adexl (Setup -> Model Libraries). If you are using SPICE models (e.g., Arizona PTM models) you need to add this statement at the beginning of the text file to switch back to Spectre (without quotes): "simulator lang = spectre".

Plot the following design charts vs gm/ID for both PMOS and NMOS[1]:

1) gm*ro
2) ID/W
3) gm/Cgg
4) VGS

PART 2: OTA Design

Use gm/ID methodology to design a diff input SE output operational transconductance amplifier (OTA) that achieves the following specs. Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec), but design your own current mirror.

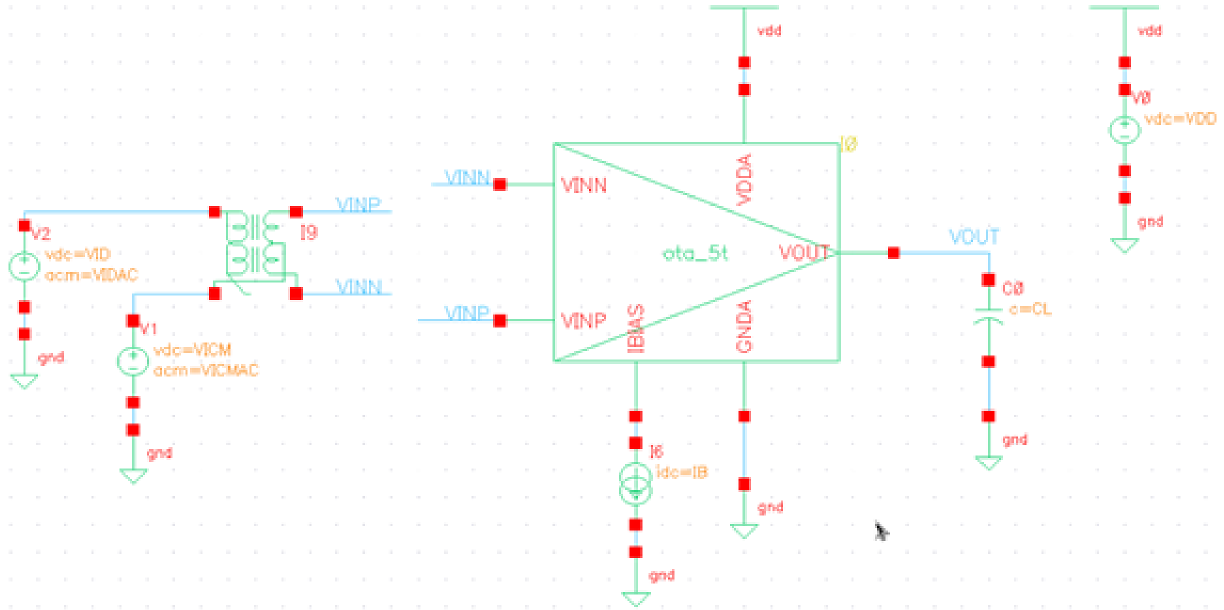
Technology	0.13um CMOS	0.18um CMOS
Supply voltage	1.2V	1.8V
Load	5pF	5pF
Open loop DC voltage gain	>= 34dB	>= 34dB
CMRR @ DC	>= 74dB	>= 74dB
Phase margin	>= 70º	>= 70º
OTA current consumption	<= 20uA	<= 20uA
CM input range – low	<= 0.6V	<= 0.8V
CM input range – high	>= 1V	>= 1.5V
GBW	>= 5MHz	>= 5MHz

Report the following:

1) Detailed design procedure and hand analysis. You need to explain why you chose the architecture that you implemented.
2) A table showing W, L, g_m, I_D, g_m/I_D, $vdsat$, $V_{ov} = V_{GS} - V_{TH}$, and $V^* = 2I_D/g_m$ of all transistors (as calculated from gm/ID curves).

[1] While viewing MATLAB figure, use "View -> Plot Browser" to view the legend and enable or disable curves. While using the data cursor, right click on the cursor and select "Selection Style -> Mouse Position".

PART 3: Open-Loop OTA Simulation[2]



Create a testbench as shown above. Note that IDC connection (sinking or sourcing) in the test bench may be different from the one shown above depending on the type of your input pair (PMOS/NMOS). Report the following:

1) Schematic of the OTA with DC node voltages clearly annotated.
   - Use VICM at the middle of the CMIR.
   - Is the current (and gm) in the input pair **exactly** equal?
   - What is DC voltage at VOUT? Why?
2) Diff small signal ccs:
   - Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
   - Set VIDAC = 1 and VICMAC = 0.
   - Use VICM at the middle of the CMIR.

➔ Cadence Hint: Use Cadence calculator expressions to calculate circuit parameters (Ao, Ao in dB, BW, GBW, UGF). You may use Cadence calculator to create other useful expressions.

Name	Type	Expression/Signal/File
Ao	expr	ymax(mag(VF("/VOUT")))
Ao_dB	expr	dB20(ymax(mag(VF("/VOUT"))))
BW	expr	bandwidth(VF("/VOUT") 3 "low")
fu	expr	unityGainFreq(VF("/VOUT"))
GBW	expr	(Ao * BW)

- Plot diff gain (in dB) vs frequency.
- Compare simulation results with hand calculations in a table.

[2] An OTA can be simulated without closing the loop if it is perfectly matched (zero offset voltage). For this 5T OTA in open loop, the output node DC level will follow the diode connected node. For two-stage OTA, the systematic offset voltage may drive the output to one of the rails. Also, when simulating mismatch (Monte Carlo simulation), open-loop simulation cannot be used. You must close the loop in the cases of random and systematic offset, so that the offset voltage is automatically adjusted by the feedback action and the dc bias is correctly set.

3) CM small signal ccs:

- Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
- Set VICMAC = 1 and VIDAC = 0.
- Use VICM at the middle of the CMIR.
- Plot CM gain in dB vs frequency.
- Compare simulation results with hand calculations in a table.
- (Optional) Avcm vs VICM:
    - Use **parametric** sweep (**not DC sweep**) for VICM = CMIR-low:10m:CMIR-high.
    - Plot CM gain at 1Hz in dB vs VICM.

    ➔ Cadence Hint: Instead of using parametric sweep, a better alternative in Cadence is to use AC sweep but sweep a design variable (VICM) instead of sweeping the frequency. The frequency is set at 1 Hz (or any other small value) to get the low frequency gain (DC gain).
    - Justify the results.

4) CMRR:

➔ Cadence Hint: In Mentor Pyxis you have to get Avd and Avcm from two independent simulation runs (we cannot run both simultaneously because we have single ended output, thus we cannot differentiate between diff and CM signals at the output). But for Cadence Virtuoso you should use XF analysis (1Hz:10Gz, logarithmic, 10 points/decade) because you need to calculate the transfer function between multiple inputs and a single output.

➔ Cadence Hint: Access XF analysis results from the results browser or from adexl results tab (Right Click -> Direct Plot -> Main Form). You may use this expression in the calculator to plot the CMRR: dB20(mag(getData("/V2" ?result "xf"))) - dB20(mag(getData("/V1" ?result "xf"))) .

- Use VICM at the middle of the CMIR.
- Plot CMRR in dB vs frequency at VICM at the middle of the CMIR.
- Compare simulation results with hand calculations in a table.
- (Optional) CMRR vs VICM:
    - Use **parametric** sweep (**not DC sweep**) for VICM = CMIR-low:10m:CMIR-high.
    - Plot CMRR at 1Hz in dB vs VICM.

    ➔ Cadence Hint: Instead of using parametric sweep, a better alternative in Cadence is to use AC sweep but sweep a design variable (VICM) instead of sweeping the frequency. The frequency is set at 1 Hz (or any other small value) to get the low frequency gain (DC gain).
    - Justify the results.

5) Diff large signal ccs:

- Use VICM at the middle of the CMIR.
- Use DC sweep (**not parametric sweep**) VID = -VDD:1m:VDD. You must use a small step (1mV) because the gain region is very small (steep slope).
- Plot VOUT vs VID.

- From the plot, what is the value of Vout at VID = 0? Why?
- Plot the derivative of VOUT vs VID. Compare the peak with Avd.

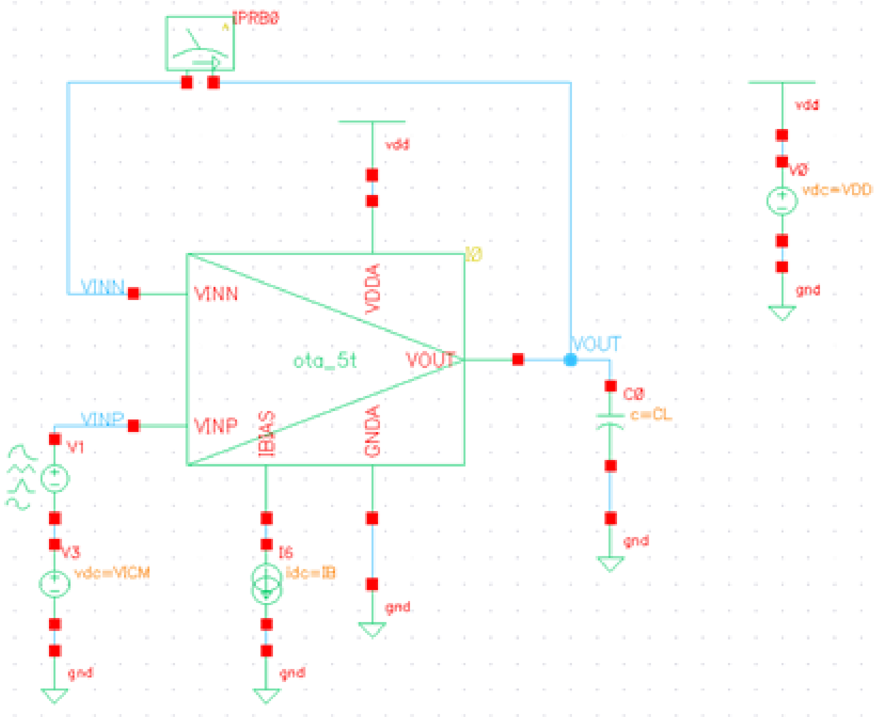
6) CM large signal ccs (region vs VICM):
   - Use **DC sweep** (not parametric sweep) VICM = 0:10m:VDD.
   - Plot "region" OP parameter vs VICM for the input pair and the tail current source (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown). Plot the results overlaid on the results of the previous method (10% reduction of GBW).
   - Plot "region" OP parameter vs VICM for the input pair and the tail current source.
   - Find the CM input range (CMIR). Compare with hand analysis in a table.
   - Note that the drawback of this method is that the "region" parameter cannot be experimentally measured in the lab.
7) (Optional) CM large signal ccs (GBW vs VICM):
   - Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
   - Set VIDAC = 1 and VICMAC = 0.
   - Use **parametric** sweep (**not DC sweep**) VICM = 0:10m:VDD.
   - Plot GBW vs VICM. Plot the results overlaid on the results of the previous method (region parameter).

➔ Cadence Hint: Instead of using parametric sweep, a better alternative in Cadence is to use AC sweep but sweep a design variable (VICM) instead of sweeping the frequency. The frequency is set at 1 Hz (or any other small value) to get the low frequency gain (DC gain).

   - Annotate the CM input range. Calculate the input range as the range over which the GBW is within 90% of the max GBW, i.e., 10% reduction in GBW[3].

[3] If you are using NMOS input pair, body effect may cause CMIR to extend till VDD (why?).

PART 4: Closed-Loop OTA Simulation



Create a testbench as shown above. Report the following:

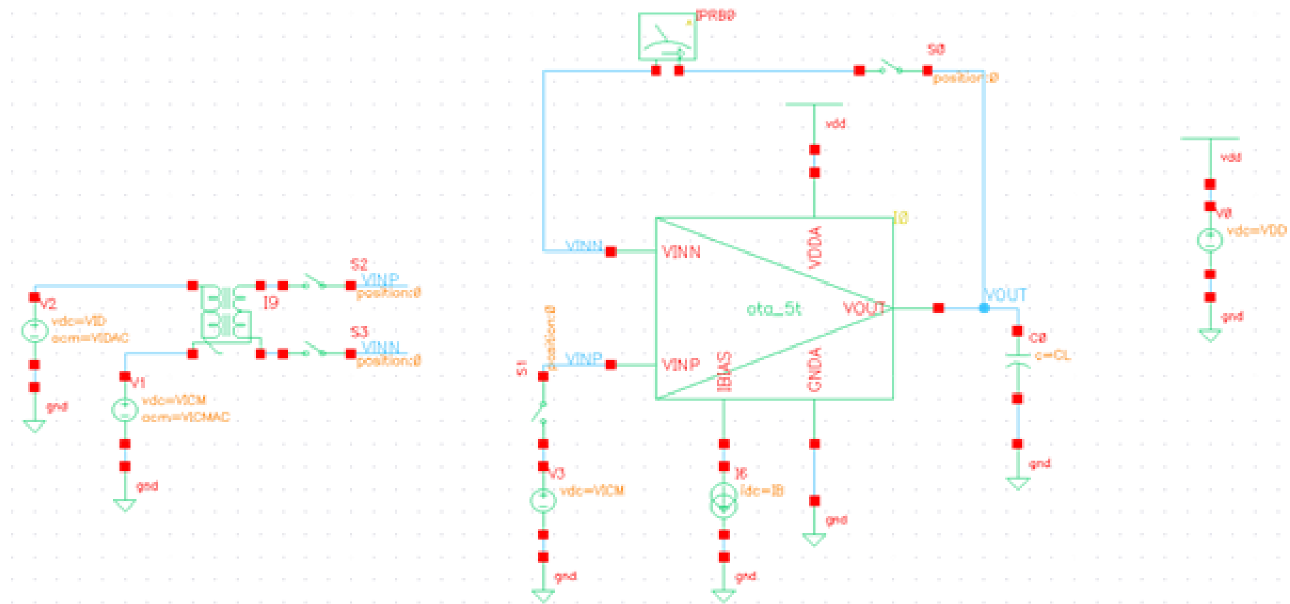
1) Schematic of the OTA with DC OP point clearly annotated in unity gain buffer configuration. Use VIN = CMIR-low + 50mV.
   - Is the current (and gm) in the input pair exactly equal[4]? Why?
   - Calculate the mismatch in I_D and gm.
2) Loop gain:
   - Use STB analysis (1Hz:10Gz, logarithmic, 10 points/decade) in unity gain buffer configuration.
   - Use VICM at the middle of the CMIR.
   - Plot loop gain in dB and phase vs frequency.

➔ Cadence Hint: Access STB analysis results from the results browser or from adexl results tab (Right Click in adexl Results tab-> Direct Plot -> Main Form).

   - Compare DC gain and GBW with those obtained from open-loop simulation. Comment
   - Compare simulation results with hand calculations in a table.

[4] For the case of the OTA in closed-loop unity-gain buffer connection, the output will follow the input. The output voltage deviates from its CM level (the voltage at the mirror node for the 5T OTA) in order to match the input voltage. Since the gain is finite, there will be a non-zero differential input voltage that will cause an imbalance between the two sides of the differential pair. This imbalance behaves exactly like mismatch. To avoid this imbalance, we may close the loop using Vin equal to the voltage at the mirror node. Any other Vin will introduce mismatch between the gm's of the input pair, and you will have to use Avcm and CMRR equations that consider mismatch.

PART 5 (optional): Effect of Mismatch on CMRR



Copy your testbench in a new cell and modify the new schematic as shown above. Switches with different AC/DC setting are added in order to connect the feedback loop in DC and break it in AC. The DC OP point is set by the unity gain feedback buffer connection, while the AC stimulus is set by the balun. Note that the DC feedback loop will introduce mismatch in the input pair (why?). We will study the effect of mismatch on Avcm and CMRR. Report the following:

1) CM small signal ccs:
   - Use AC analysis (at 1Hz, no frequency sweep). Keep OP simulation enabled because we will plot gm.
   - Set VICMAC = 1 and VIDAC = 0.
   - Use **parametric** sweep (**not DC sweep**) for VIN = CMIR-low:10m:CMIR-high.
   - Plot gm of the input pair overlaid vs VICM.
   - The two gm's intersect (are equal) at a specific VIN. Why? What is Avcm at this value.
   - Plot CM gain at 1Hz in dB vs VIN. Extract it in Measures as shown below.
   - Add a cursor for Avcm @ VIN = CMIR-low + 50mV. Compare simulation results with hand calculations in a table (Hint: use A_{vCM} formula that considers gm mismatch).
2) CMRR:

➔ Cadence Hint: In Mentor Pyxis you have to get Avd and Avcm from two independent simulation runs (we cannot run both simultaneously because we have single ended output, thus we cannot differentiate between diff and CM signals at the output). But for Cadence Virtuoso you should use XF analysis (1Hz:10Gz, logarithmic, 10 points/decade) because you need to calculate the transfer function between multiple inputs and a single output.

- Extract Avd and Avcm at 1Hz vs VIN from two AC simulations as in the previous step (note that we cannot run both simultaneously because we have single ended output, thus we cannot differentiate between diff and CM signals at the output).
- Use **parametric** sweep (**not DC sweep**) for VIN = CMIR-low:10m:CMIR-high.
- Plot CMRR in dB vs VIN.
- Add a cursor for CMRR @ VIN = CMIR-low + 50mV. Compare simulation results with hand calculations in a table (Hint: use CMRR formula that considers gm mismatch).

Lab Summary

- In Part 1 you learned:
  - How to generate and use gm/ID design curves.
- In Part 2 you learned:
  - meeting desired specifications.
- In Part 3 you learned:
  - How to simulate the small-signal differential gain of a 5T OTA in open-loop configuration.
  - How to simulate the small-signal common-mode gain of a 5T OTA in open-loop configuration.
  - How to simulate the large-signal differential characteristics of a 5T OTA in open-loop configuration.
  - How to simulate the large-signal common-mode characteristics of a 5T OTA in open-loop configuration.
- In Part 4 you learned:
  - How to simulate the small-signal differential gain of a 5T OTA in closed-loop configuration.
  - How to simulate the small-signal common-mode gain of a 5T OTA in closed-loop configuration.
  - How to simulate the large-signal differential characteristics of a 5T OTA in closed-loop configuration.
  - How to simulate the large-signal common-mode characteristics of a 5T OTA in closed-loop configuration.
- In Part 5 you learned:
  - How to simulate the effect of mismatches on the characteristics of a 5T OTA.

Acknowledgements

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