## 19 February 2019 1440 عمادى الثانية 1440

## وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا هَلِيلًا

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## **Analog IC Design**

### **OTA Simulation Tutorial**

In this tutorial we will simulate an OTA that was designed using gm/ID methodology.

Note that this tutorial was done using AMS 0.18um technology. Your technology may be different, so library/instance/parameter names may be different.

# Part 1: Design Charts

#### **Creating Design Library**

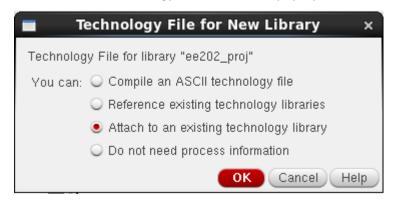
From library manager create new library.



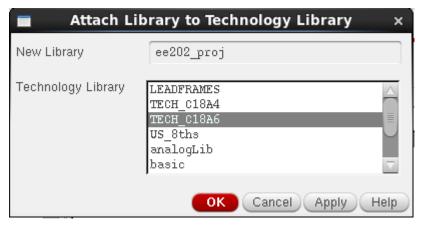
Give your lib a name.



Attach it to our technology (note that some pop-up windows may appear in the background).

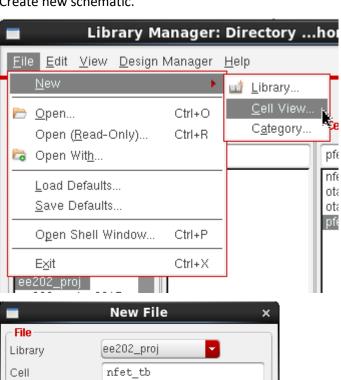


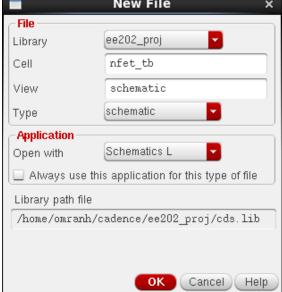
The below snapshot applies for AMS 0.18 technology. Your technology may be different. This step is important only if you will be doing layout.



### **Creating Design Charts**

Create new schematic.

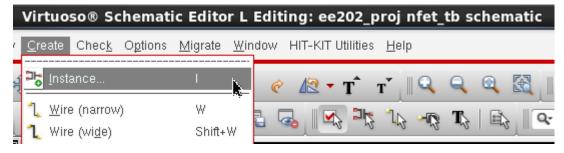




If you receive messages like the below just click always.



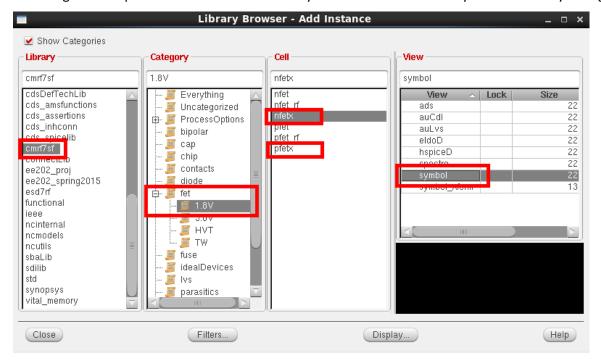
Add instance (you can use the hot-key 'i').



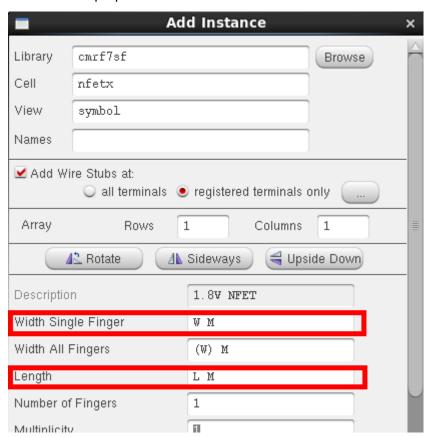
#### Browse.



The design kit components are in "cmrf7sf" library. These are the FETs that you will be always using.



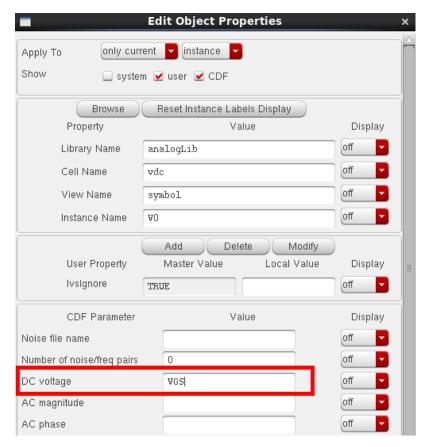
You can make properties as variables.



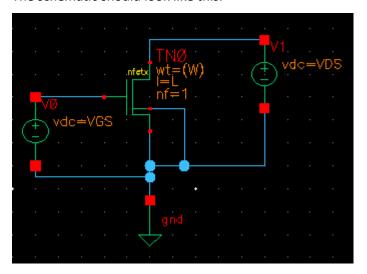
Sources, resistors, capacitors, gnd, etc., are in analogLib library.

Add DC voltage source.

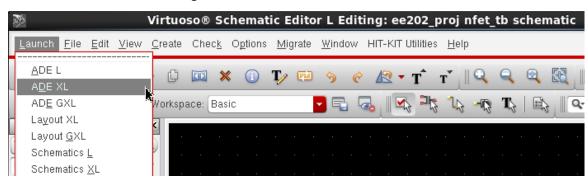




The schematic should look like this.



Launch adexl to start simulating.



For the first time you create new view. After that you open the existing view.

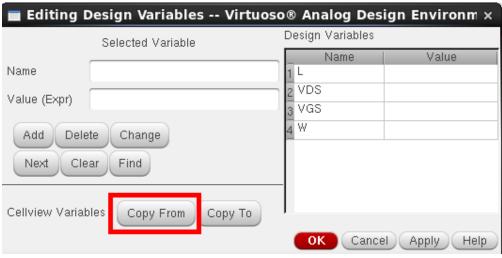


Add test.



Copy variables from the schematic.

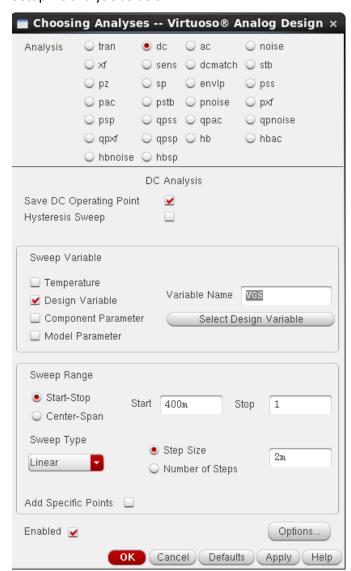




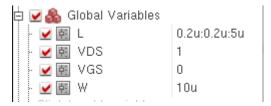
#### Add analysis.



Setup DC analysis as below.



Setup the global variables as below.



You need to tell Cadence that you want to save some transistor parameters (gm, gds, etc.) So you need to add a text file to your model libraries.



Create a text file, add the lines below in it, and then add it to model libraries as below.

save \*:gm sigtype=dev

save \*:gds sigtype=dev

save \*:id sigtype=dev

save \*:cgg sigtype=dev

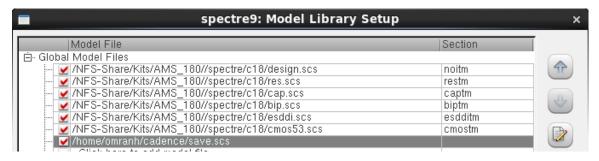
save \*:cgs sigtype=dev

save \*:gmoverid sigtype=dev

save \*:vgs sigtype=dev

save \*:vth sigtype=dev

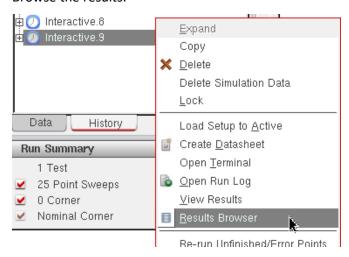
#### save \*:vdsat sigtype=dev



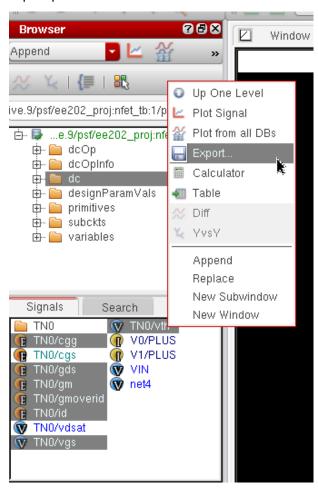
#### Run your simulation.



#### Browse the results.



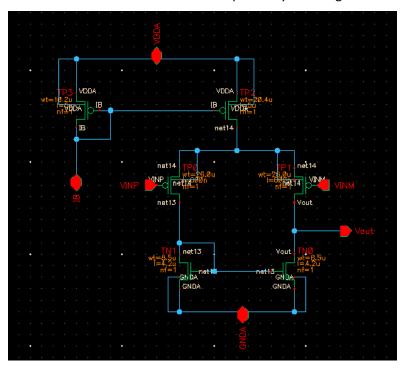
Export parameters to csv file.



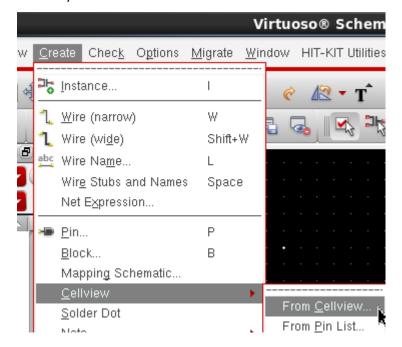
Use MATLAB to plot the design curves. A sample MATLAB code is available on Canvas.

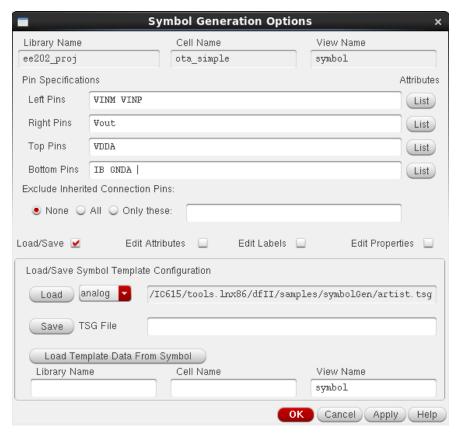
# Part 2: OTA Simulation

Draw the schematic as below. Create pins for your design.

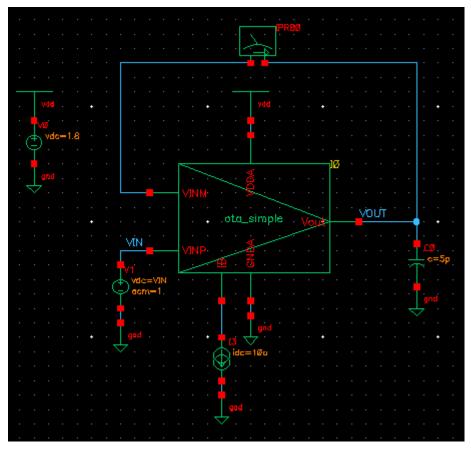


Create symbol view to use it in the test bench.



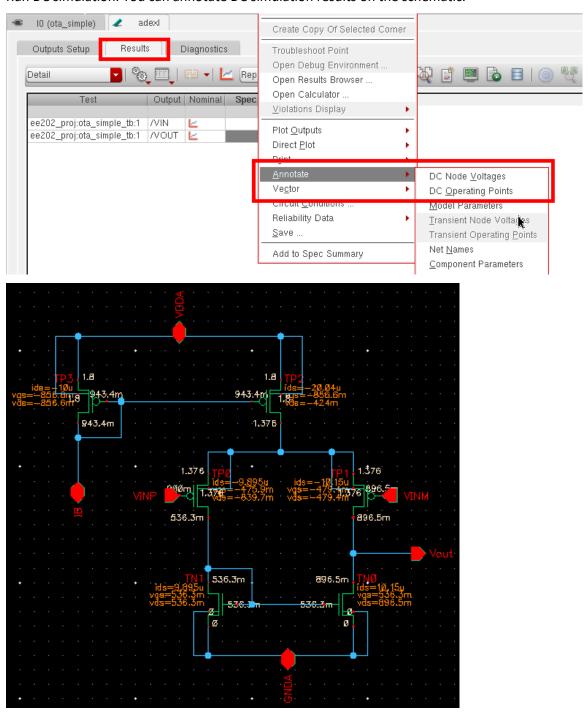


Create new schematic for the test bench. Draw the test bench as below.



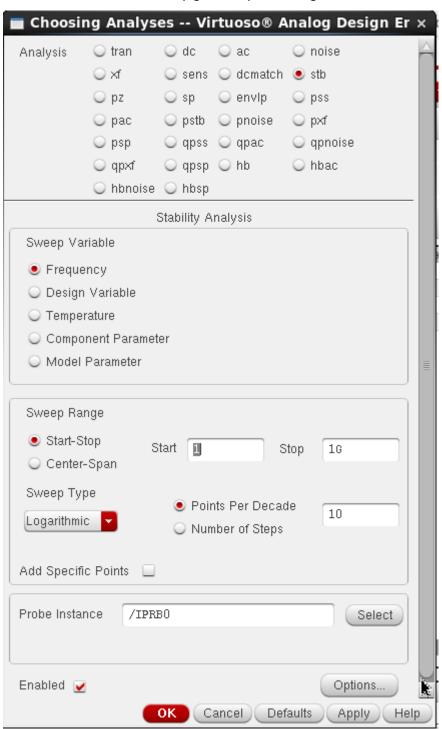
**DC Simulation** 

#### Run DC simulation. You can annotate DC simulation results on the schematic.

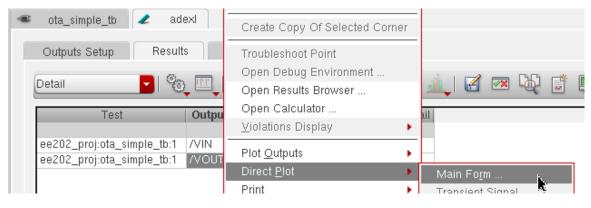


**STB Simulation** 

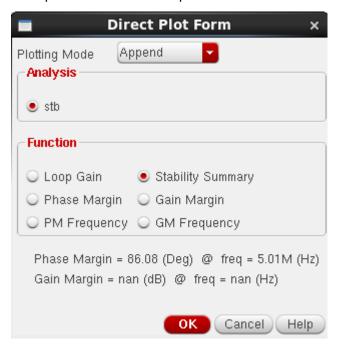
Run STB simulation to find loop gain and phase margin.



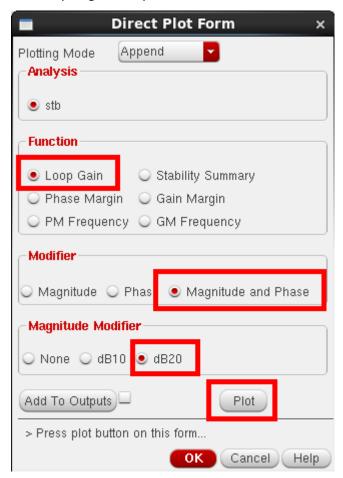
Use "Main Form" to plot STB simulation results.



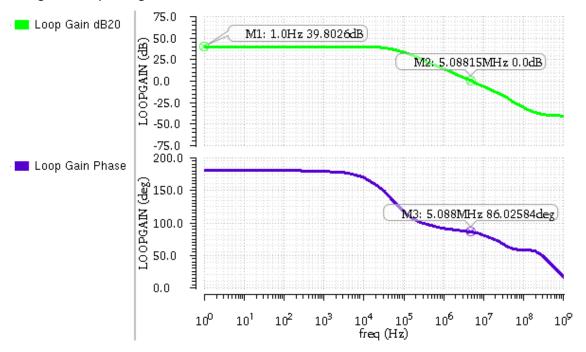
All important results can be plotted from here.



You can plot gain and phase as below.



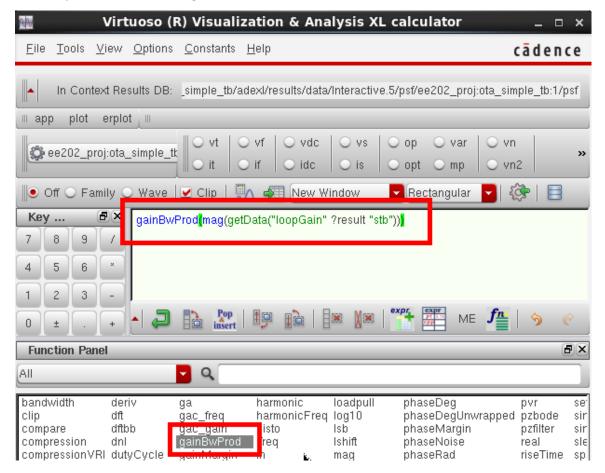
Make sure you annotate the plots using markers (m). Invert the colors in any image editor to avoid black background in printing.

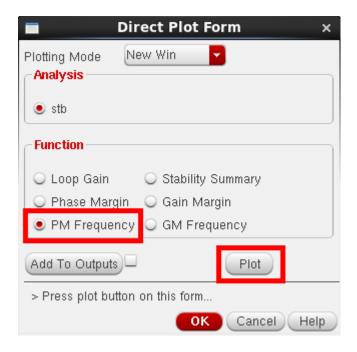


To get input range you need to sweep VIN.

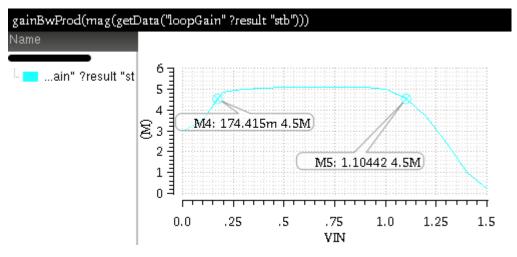


You can plot GBW vs VIN using calculator. You can also use the "Main Form" as before.



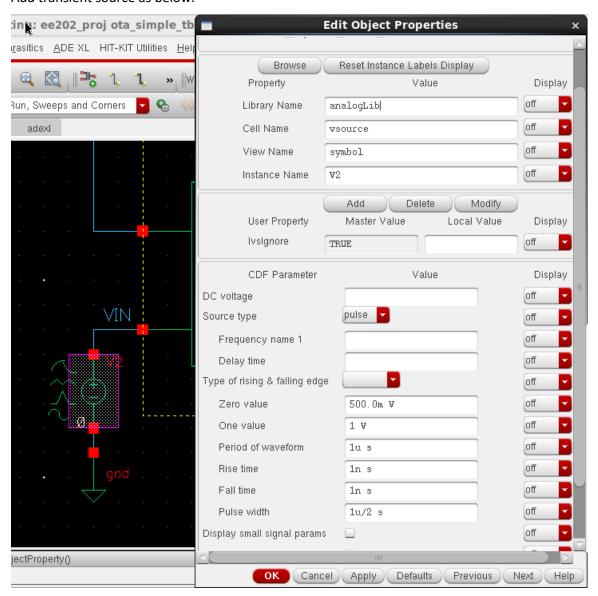


This plot shows GBW vs VIN.

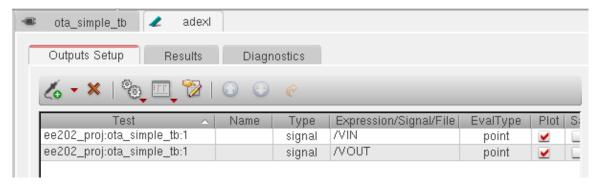


**Transient Simulation** 

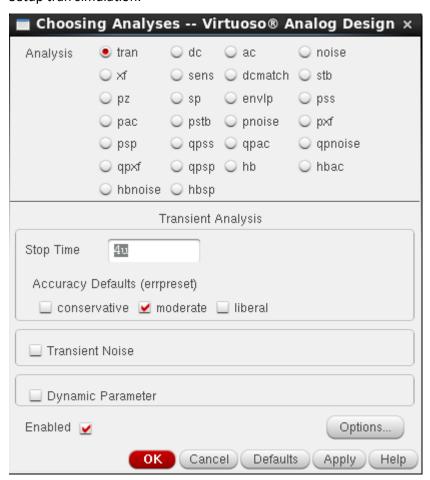
#### Add transient source as below.



#### Select the signals to be plotted.



Setup tran simulation.



Run the simulation and plot the results. Use (a,b) marker to calculate the slew rate.

