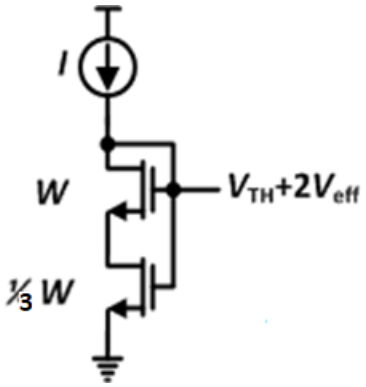
Problem Set #2: Advanced Current Mirrors

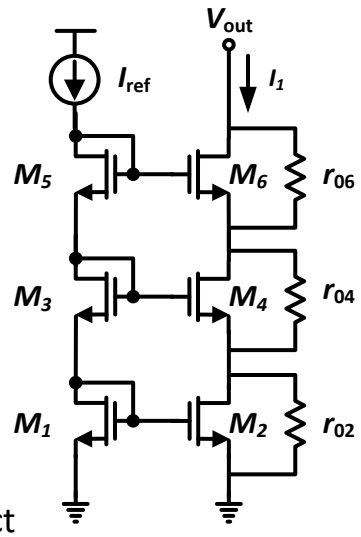
Problem (1)

The circuit shown is used to bias a low-voltage (high-swing) cascode current mirror. Show that the dimension of the bottom transistor (W/3) is proper to obtain the required bias voltage.



Problem (2)

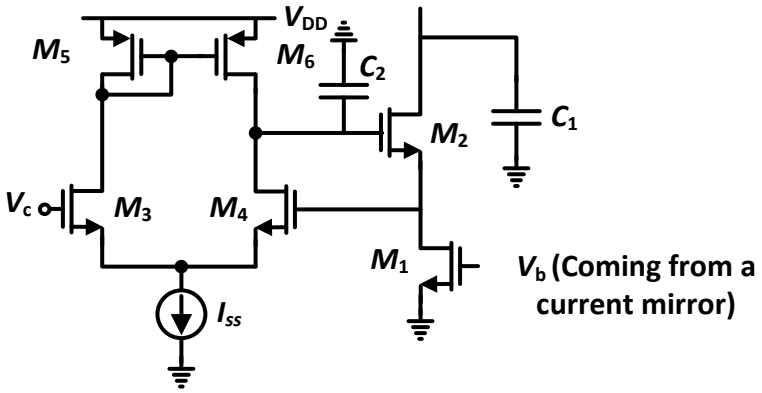
I. For the current mirror circuit shown, assume all transistors are identical. Find:
   A. R_{out}.
   B. Compliance voltage of the current source.
   C. Assuming random mismatches between transistors find $\frac{\Delta I_1}{I_{ref}}$ in terms of the offset voltage between matched transistors (v_{os}) and overdrive voltages (V_{eff}). Consider only the transistor pair that contributes most to the current mismatch and ignore channel length modulation for all transistors). Discuss the effect on the current mismatch due to mismatches in all 3 pairs separate (M1-M2 , M3-M4 and M5-M6)



Problem (3)

In the shown circuit (called self-regulated current source):

1- Find R_{out} at DC.
2- Find the compliance voltage of the current source.
3- Find V_c for optimum compliance voltage.
4- Given the capacitors shown, find $Z_{out}(f)$



* Assume an ideal current source I_{SS} (can accept negative voltage on its upper terminal)

Problem (4)

For the Wilson current mirror shown:

1) Find an expression for $V_{compliance}$ and R_{out}
2) Does the current mirror suffer from systematic offset? Explain