وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog IC Design – Cadence Tools
Lab 02
Common Source Amplifier

Intended Learning Objectives

In this lab you will:

- Design and simulate a common-source amplifier.
- Learn how to generate and use design charts.
- Investigate gain non-linearity; the variation of the gain with input signal amplitude.
- Study the maximum gain attainable for a resistive-loaded CS amplifier and the effect of supply scaling on max gain.
- Learn how to use feedback to reduce non-linearity (gain linearization).

PART 1: Sizing Chart

1) We would like to design a resistive loaded CS amplifier that meets the specifications below. The design process involves selecting the sizing of the transistor (W and L), the bias point (V_{GS}), and the resistive load (R_D).

Spec	0.13um CMOS	0.18um CMOS
DC Gain	-5	-8
Supply	$1.2V$	$1.8V$
Current consumption	$100\mu A$	$100\mu A$

2) The first design decision is to choose L. Since there is not spec on bandwidth (speed), we may choose a relatively long L to provide large r_o and avoid short channel effects. Note that r_o appears in parallel with R_D. Assume we will choose $L = 2\mu m$.
3) We can show that the gain is given by

$$|A_v| \approx g_m R_D = \frac{2I_D}{V_{ov}} \times R_D = \frac{2V_{R_D}}{V_{ov}}$$

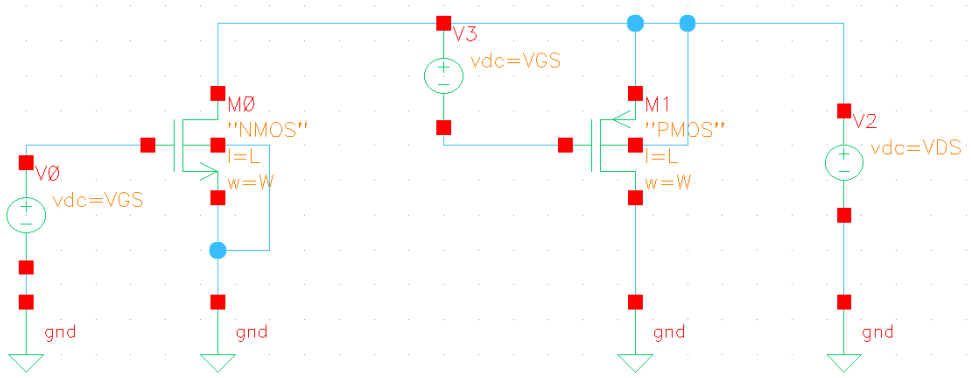
Interestingly, the gain only depends on the voltage drop across V_{R_D} and V_{ov}. However, to derive this expression we used $g_m = \frac{2I_D}{V_{ov}}$ which is based on the square-law. For a real MOSFET, if we compute V_{ov} and $\frac{2I_D}{g_m}$ they will not be equal. Let's define a new parameter called V-star (V^*) which is calculated from actual simulation data using the formula

$$V^* = \frac{2I_D}{g_m} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

For a square-law device, $V^* = V_{ov}$, however, for a real MOSFET they are not equal. The actual gain is now given by

$$|A_v| \approx \frac{2V_{R_D}}{V^*}$$

4) The choice of V_{R_D} is constrained by the output signal swing. Since we usually want to provide large output swing, we choose the common-mode (CM) output level (DC output level) around $V_{DD}/2$. Thus, although increasing V_{R_D} increases the gain, but the choice is limited by the supply voltage which is aggressively scaled down in modern technologies. That's one reason it is difficult to get high gain in modern technologies. Assuming CM output = $V_{R_D} = V_{DD}/2$ and given the DC bias current, determine the value of R_D. Again, it is interesting to note that although the gain equals $g_m R_D$, it actually does not depend on R_D itself, but on the voltage drop across it, i.e., the product $I_D \times R_D$.
5) Given A_v and V_{R_D}, calculate the required V^* (again note that $V^* \neq V_{ov}$ for a real MOSFET). Let's name this value V_Q^*.
6) The remaining variable in the design is to calculate W. Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation. Create a testbench for NMOS and PMOS characterization (we will use the PMOS later in Part 2 of this lab). Use $W = 10\mu m$ (we will understand why shortly) and $L = 2\mu m$ (the same L that we chose before).

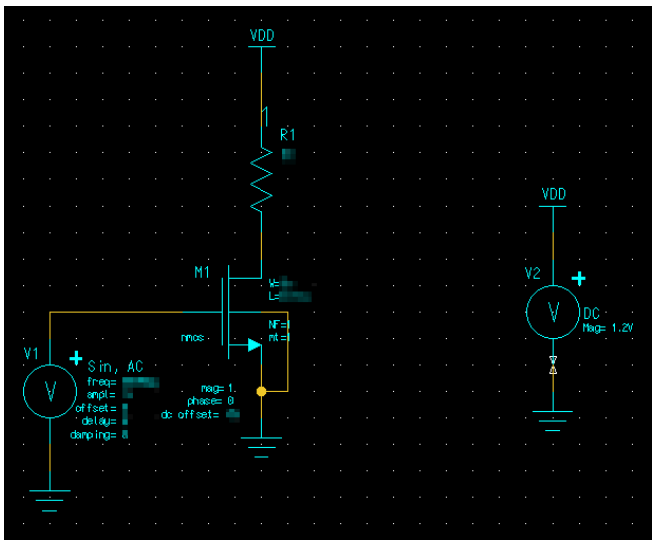


7) Sweep VGS from 0 to $\approx V_{TH} + 0.4V$ with 10mV step. Set $V_{DS} = V_{DD}/2$.
8) We want to compare $V^* = 2I_D/g_m$ and $V_{ov} = V_{GS} - V_{TH}$ by plotting them overlaid. Use the calculator to create expressions for V^* and V_{ov}. Export the expressions to adexl.
9) Plot V^* and V_{ov} overlaid vs VGS. Make sure the y-axis of both curves has the same range. You will notice that in the region of moderate inversion, V^* and V_{ov} are relatively close to each other (i.e., square-law is relatively valid). For strong inversion (large V_{ov}) or weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square-law (although we are using $L = 2\mu m$).
10) On the V^* and V_{ov} chart locate the point at which $V^* = V_Q^*$. Find the corresponding V_{ovQ} and V_{GSQ}.
11) Plot I_D, g_m, and g_{ds} vs V_{GS}. Find their values at V_{GSQ}. Let's name these values I_{DX}, g_{mX}, and g_{dsX}.
12) Now back to the assumption that we made that $W = 10\mu m$. This is not the actual value that we will use for our design. But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be $I_{DQ} = 100\mu A$ as given in the specs. Calculate W as shown below.

W	I_D
$10\mu m$	I_{DX} @V_Q^* (from the chart)
?	$I_{DQ} = 100\mu A$ (from the specs)

13) Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as V_{ov} is constant. On the other hand, $r_o = 1/g_{ds}$ is **inversely** proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross-multiplication) and double check that $A_v = -g_m(R_D||r_o)$ meet the required gain spec.

PART 2: CS Amplifier



1. OP and AC Analysis

1) Create a testbench for the resistive loaded CS amplifier using the V_{GSQ}, R_D, L, and W that you got from the previous part.
2) Simulate the DC OP. Add a monitor for M1 (from DCOP/TRAN) to show the key OP parameters. Compare the results with the results you obtained in Part 1. Since we used chart-based design, the results should agree well.
   ➔ Cadence Hint: The "region" meaning is as follows: (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown).
3) Compare r_o and R_D. Is the assumption of ignoring r_o justified in this case? Do you expect the assumption to remain justified if we use min L?
4) Calculate the intrinsic gain of the transistor.
5) Calculate the amplifier gain analytically. What is the relation $(\ll, <, \approx, >, \gg)$ between the amplifier gain and the intrinsic gain?
6) Create a new simulation configuration and run AC analysis (from 1Hz to 1GHz). Report the gain vs frequency. Annotate the DC gain and make sure it meets the spec.

2. Gain Non-Linearity

1) Create a new simulation configuration. Perform a DC sweep for the input voltage from 0 to V_{DD} with 2mV step.
2) Report VOUT vs VIN. Is the relation linear? Why?
3) Calculate the derivative of VOUT using calculator. Plot the derivative vs VIN. The derivative is itself the small signal gain. Is the gain linear (independent of the input)? Why?
4) Set the properties of the voltage source to apply a transient stimulus (sine wave of 1kHz frequency and 10mV amplitude superimposed on the DC input voltage).
5) Create a new simulation configuration. Run transient simulation for 2ms. Plot gm vs time. Does gm vary with the input signal? What does that mean?
   ➔ Cadence Hint: In order to save gm vs time, create an empty text file and write the following statement: save *:gm sigtype=dev. Add this text file in the model libraries. Enable DC simulation.
6) Is this amplifier linear? Comment.

3. [Optional] Maximum Gain

1) We want to investigate the variation of gain vs RD. We will use AC analysis to calculate the small signal gain. Set the source AC magnitude = 1. Note that AC analysis is a linear analysis, so we use a

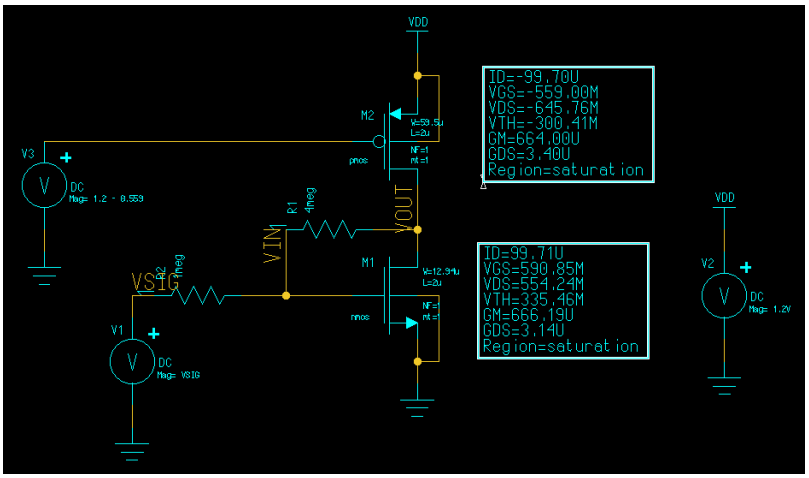
magnitude of one such that the output is itself the gain. Keep the DC value of VGS constant at the DC value you selected in Part 1.

2) Set AC simulation to sweep design variable (RD from ¼ the value you selected in Part 1 to 4 times the value you selected in Part 1). Set the AC simulation frequency at 1 Hz (single frequency point). The purpose of the AC analysis here is just to get the small signal gain and not to investigate the frequency response.
3) Use the calculator to plot the gain vs RD.
4) You will find that the gain increases with RD and then decreases with RD. Justify this behavior.
5) What is the value of RD that gives the highest gain? What is the highest gain?
6) Analytically calculate the value of RD that gives the highest gain and the highest gain using the expressions in Part 1. Compare simulation and analysis results.
7) What is the available signal swing at the point of maximum gain?
8) Is scaling down the supply voltage good for gain? Comment.

4. [Optional] Gain Linearization (feedback)

1) We will use feedback to improve the gain non-linearity. We will study feedback in more details later.
2) Create a new schematic. You may copy instances from the old schematic to the new schematic by opening them as multiple tabs inside the same Pyxis Schematic window.
3) Replace the resistive load with a PMOS current source (active load) as shown below. Create a sizing chart for the PMOS similar to what we did for NMOS in Part 1 using $L = 2\mu m$ and $W = 10\mu m$ (you may use the same test bench used in Part 1). From the chart, assuming V_Q^* similar to NMOS, determine V_{GSQ} and I_{DX}. Using ratio and proportion (cross-multiplication) determine W similar to Part 1. Note that the PMOS load must have the same bias current as the NMOS input device.

W	I_D
$\mathbf{10\mu m}$	I_{DX} @V_Q^* (from the chart)
?	$I_{DQ} = 100\mu A$ (from the specs)



4) Add two resistors: input resistor (R_{in}) = 1M and feedback resistor (R_f). Choose R_f to give a voltage gain approximately equal to $R_f/R_{in} = |A_v|$ as given in the specs.
5) Perform a DC sweep for the input voltage (VSIG) from 0 to V_{DD} with 2mV step.
6) Report VIN and VOUT vs VSIG (overlaid). At what voltage do the two curves cross? Why?
Hint: Compare this voltage to VGS of M1. The center value of the amplification region is itself VGS of M1. At this point VOUT is also equal to VIN because no current flows in the two resistors.
7) Is VOUT vs VSIG linear? Why?

8) Calculate the derivative of VOUT. The derivative is itself the small signal gain. Is the gain linear (independent of the input)? Why?
9) What is value of VIN in the part where the gain is linear?
10) Analytically calculate the DC input range over which the gain is linear. Compare your analysis with the simulation result.
Hint: When VSIG deviates from V_{GS1} current flows and VOUT deviates. The amplifier fails when M1 or M2 gets out of saturation ($V_{DS} < V^*$). You can get the input range by dividing the output range by the gain $\approx \frac{V_{DD}-2V^*}{4}$.

Lab Summary

In Part 1 you learned:

- How to generate and use design charts for NMOS and PMOS transistors.
- How to design a resistive-loaded common-source amplifier.
- How the overdrive voltage of a MOS transistor deviates from the square law in different regions of operation.

In Part 2 you learned:

- How to do ac and DC simulations of a CS amplifier.
- How the gain of an amplifier changes with the input signal amplitude.
- How to get the maximum attainable gain of a CS amplifier by changing the load resistor.
- How to use feedback resistors to reduce gain non-linearity.

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