وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog IC Design – Cadence Tools
Lab 03
Cascode Amplifier

Intended Learning Objectives

In this lab you will:

- Design and simulate a cascode amplifier.
- Learn how to generate and use design charts.
- Study the biasing of the cascode amplifier.
- Investigate the gain, the bandwidth, and the GBW of a cascode amplifier.

Part 1: Sizing Chart

1) We can show that the intrinsic gain of a MOSFET is given by

$$|A_v| \approx g_m r_o = \frac{2I_D}{V_{ov}} \times \frac{V_A}{I_D} = \frac{2V_A}{V_{ov}}$$

Interestingly, the gain only depends on λ and V_{ov}. However, to derive this expression we used $g_m = \frac{2I_D}{V_{ov}}$ which is based on the square-law. For a real MOSFET, if we compute V_{ov} and $\frac{2I_D}{g_m}$ they will not be equal. Let's define a new parameter called V-star (V^*) which is calculated from actual simulation data using the formula

$$V^* = \frac{2I_D}{g_m} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

For a square-law device, $V^* = V_{ov}$, however, for a real MOSFET they are not equal. The actual gain is now given by

$$|A_v| \approx \frac{2V_A}{V^*}$$

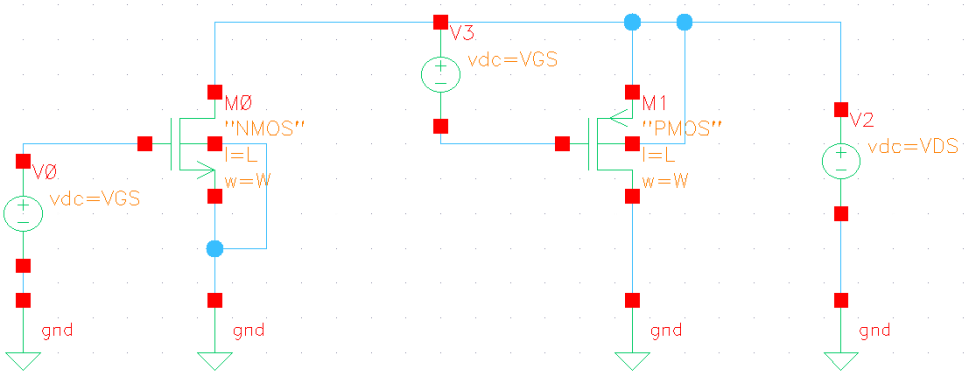
The lower the V^* the higher the gain, but the larger the area and the lower the speed. An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200mV$.

2) We want to design CS and cascode amplifiers with the parameters below.

Parameter	0.13um CMOS	0.18um CMOS
L[1]	$0.5\mu m$	$0.5\mu m$
V^*	$200mV$	$200mV$
Supply	$1.2V$	$1.8V$
Current consumption	$20\mu A$	$20\mu A$

3) The remaining variable in the design is to calculate W. Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation. Create a testbench for NMOS transistor as shown below (we will use NMOS only in this lab). Use $W = 10\mu m$ (we will understand why shortly) and $L = 0.5\mu m$ (the same L selected before).

[1] A relatively small L is necessary for Part 3 to make sure that Cgd is not negligible compared to Cgs.



4) Sweep VGS from 0 to $\approx V_{TH} + 0.4V$ with 10mV step. Set $V_{DS} = V_{DD}/2$.
5) We want to compare $V^* = 2I_D/g_m$ and $V_{ov} = V_{GS} - V_{TH}$ by plotting them overlaid. Use the calculator to create expressions for V^* and V_{ov}. You can save the expressions to reuse them later.
6) Plot V^* and V_{ov} overlaid vs VGS. Make sure the y-axis of both curves has the same range. From the chart, you will notice that in the region of moderate inversion, V^* and V_{ov} are relatively close to each other (i.e., square-law is relatively valid). For strong inversion (large V_{ov}) or weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square-law.
7) An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200mV$. On the V^* and V_{ov} chart locate the point at which $V^* = 200mV$. Find the corresponding V_{ovQ} and V_{GSQ}.
8) Plot I_D, g_m, and g_{ds} vs V_{GS}. Find their values at V_{GSQ}. Let's name these values I_{DX}, g_{mX}, and g_{dsX}.
9) Now back to the assumption that we made that $W = 10\mu m$. This is not the actual value that we will use for our design. But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be $I_{DQ} = 20\mu A$ as given in the specs. Calculate W as shown below.

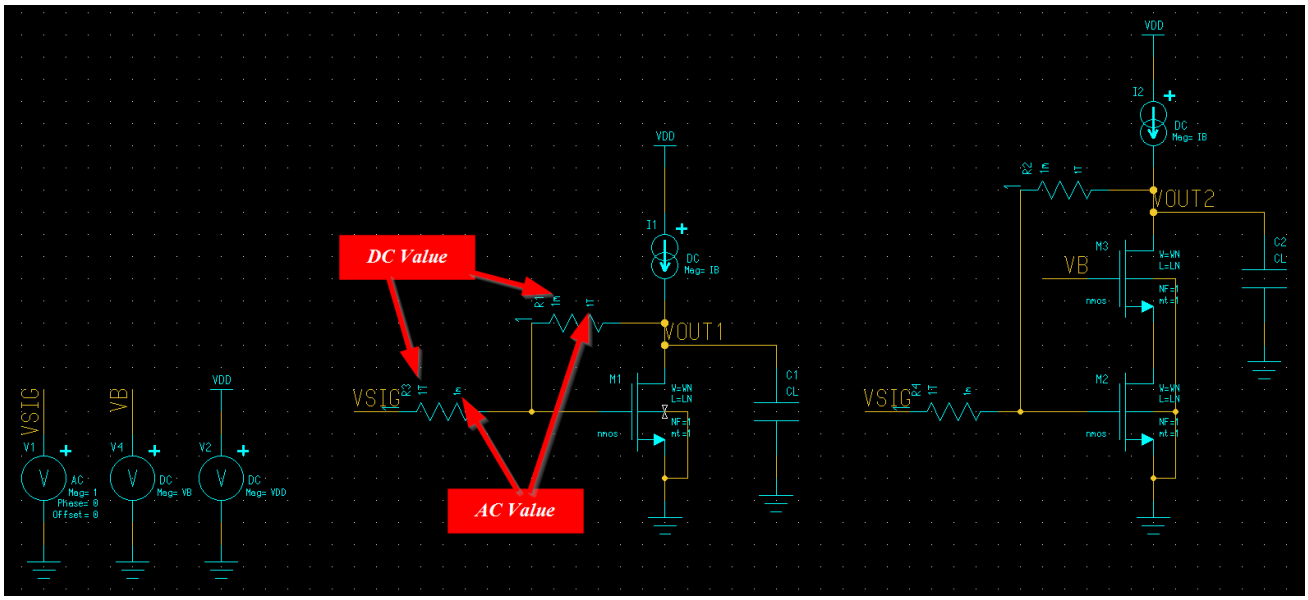
W	I_D
$\mathbf{10\mu m}$	I_{DX} @V_Q^* (from the chart)
?	$I_{DQ} = 20\mu A$ (from the specs)

10) Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as V_{ov} is constant. On the other hand, $r_o = 1/g_{ds}$ is **inversely** proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross-multiplication).

PART 2: Cascode for Gain

1. OP Analysis

1) Create a new cell and schematic. Construct the circuit shown below. Use $I_B = 20\mu A$, $L = 0.5\mu m$, W as selected in Part 1, and $C_L = 1pF$.



2) Choose V_B (the cascode device bias voltage) such that M3 has $V_{DS} \approx V^* + 100mV$ (you may sweep VB and plot VDS vs VB to help you choose a good value for VB).
3) We need to bias transistors in saturation; however, the output node is a high impedance node; thus, it is difficult to control its DC voltage. As a workaround in simulation, we use a feedback loop and resistors with different resistances in DC/AC to change the circuit connections in DC/AC simulations (use the AC property in ideal_resistor). The input transistor is diode connected for DC simulation (always in saturation), while in AC simulation the feedback is disconnected and the AC input source is connected. Set the feedback resistance $1m\Omega$ DC and $1T\Omega$ AC and set the source resistance oppositely. We will study how to do biasing practically later in this course inshaAllah.
4) Simulate the DC OP point of the above CS and cascode amplifiers. Report a snapshot showing the following parameters for M1, M2 and M3 in addition to DC node voltages clearly annotated.

ID
VGS
VDS
VTH
VDSAT
GM
GDS
GMB
CDB
CGD
CGS
CSB
Region

"vdsat" is the minimum drain-source voltage required to bias the transistor in saturation. It is equal to V_{ov} for a square-law device. It is also referred to as "vdss" (drain-source saturation voltage).
5) Check that all transistors operate in saturation.
6) Do all transistors have the same vth? Why?
7) What is the relation $(\ll, <, =, >, \gg)$ between gm and gds?
8) What is the relation $(\ll, <, =, >, \gg)$ between gm and gmb?
9) What is the relation $(\ll, <, =, >, \gg)$ between cgs and cgd?
10) What is the relation $(\ll, <, =, >, \gg)$ between csb and cdb?

2. AC Analysis

1) Create a new simulation configuration. Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.
2) Use calculator to create expressions for circuit parameters (DC gain, BW, GBW, and UGF) and export them to adexl.
   ➔ Cadence Hint: Use the following expressions in the calculator, and send them to adexl to quickly calculate circuit parameters.

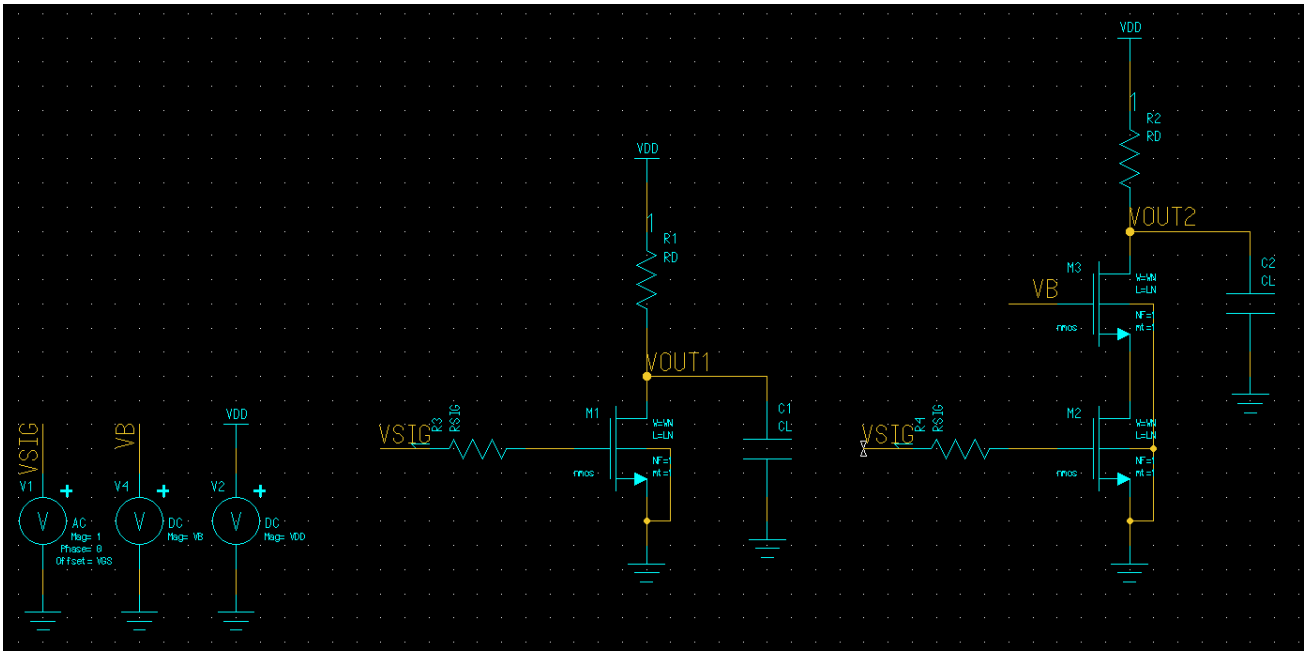
Type	Expression/Signal/File	EvalType	Plot
expr	dB20(VF("/vout1"))	point	☑
expr	ymax(dB20(VF("/vout1")))	point	☑
expr	ymax(mag(VF("/vout1")))	point	☑
expr	bandwidth(VF("/vout1") 3 "low")	point	☑
expr	gainBwProd(VF("/vout1"))	point	☑
expr	dB20(VF("/vout2"))	point	☑
expr	ymax(dB20(VF("/vout2")))	point	☑
expr	ymax(mag(VF("/vout2")))	point	☑
expr	bandwidth(VF("/vout2") 3 "low")	point	☑
expr	gainBwProd(VF("/vout2"))	point	☑

3) Report the Bode plot (magnitude) of CS and cascode **appended on the same plot**.
4) Using small signal parameters from OP simulation, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.
5) Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis.
6) Comment on the results.

PART 3 [Optional]: Cascode for BW

1. OP Analysis

1) Create a new cell and schematic. Copy the old schematic instances to the new one. Make the following modifications: remove the feedback resistance, set $C_L = 1fF$, replace the current source with a resistor RD, make the signal source resistance $= 10M\Omega$ (remove the AC value). Set VGS of the input device as calculated in Part 1.



2) Calculate R_D analytically such that the voltage drop on it is $\approx V_{DD}/2$ (the current remains roughly the same as in Part 2 because we are using the same VGS).
3) Note that the DC voltage of the output node is set by the resistance (R_D); thus, we don't need a feedback loop as in the previous case.
4) Simulate the DC OP point of the new CS and cascode amplifiers. Add monitors and report a snapshot showing the following parameters for M1, M2 and M3 in addition to DC node voltages clearly annotated.

ID
VGS
VDS
VTH
VDSAT
GM
GDS
GMB
CDB
CGD
CGS
CSB
Region

5) Check that all transistors operate in saturation.

2. AC Analysis

1) Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.
2) Use calculator to create expressions for circuit parameters (DC gain, BW, GBW, and UGF) and export them to adexl.
3) Report the Bode plot (magnitude) of CS and cascode **appended on the same plot**.
4) Using small signal parameters from OP simulation, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.
5) Report a table comparing the DC gain, BW, UGF, and GBW of both circuits from simulation and hand analysis. Comment on the results.

Lab Summary

In Part 1 you learned:

- How to generate and use design charts for NMOS and PMOS transistors.
- How to design common-source and cascode amplifiers.

In Part 2 you learned:

- How to do ac and DC simulations of a cascode amplifier with current-source load.
- How the gain of a cascode amplifier with current-source load changes with frequency.
- How to simulate the gain, the bandwidth and the GBW of a cascode amplifier with current-source load.

In Part 3 you learned:

- How to do ac and DC simulations of a cascode amplifier with resistive load.
- How the gain of a cascode amplifier with resistive load changes with frequency.
- How to simulate the gain, the bandwidth and the GBW of a cascode amplifier with resistive load.

Acknowledgements

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