

Analog IC Design**Lab 04****Common Drain Frequency Response****Intended Learning Objectives**

In this lab you will:

- Design and simulate a common-drain amplifier.
- Learn how to generate and use design charts.
- Learn how to do ac, DC, and transient simulations of a CD amplifier.
- Investigate the ringing and peaking problem in a capacitive-loaded CD amplifier with a large signal source resistance (R_{sig}) and learn how to solve it.
- Use PMOS input transistor to avoid body effect in a CD amplifier.

Part 1: Sizing Chart

- 1) We can show that the intrinsic gain of a MOSFET is given by

$$|A_v| \approx g_m r_o = \frac{2I_D}{V_{ov}} \times \frac{1}{\lambda I_D} = \frac{2}{\lambda V_{ov}}$$

Interestingly, the gain only depends on λ and V_{ov} . However, to derive this expression we used $g_m = \frac{2I_D}{V_{ov}}$ which is based on the square-law. For a real MOSFET, if we compute V_{ov} and $\frac{2I_D}{g_m}$ they will not be equal. Let's define a new parameter called V-star (V^*) which is calculated from actual simulation data using the formula

$$V^* = \frac{2I_D}{g_m} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

For a square-law device, $V^* = V_{ov}$, however, for a real MOSFET they are not equal. The actual gain is now given by

$$|A_v| \approx \frac{2}{\lambda V^*}$$

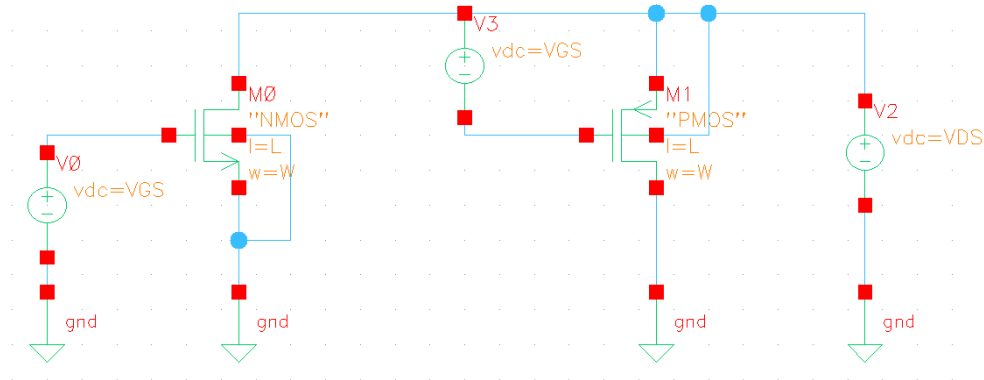
The lower the V^* the higher the gain, but the larger the area and the lower the speed. An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200mV$.

- 2) We want to design a CD amplifier with the parameters below.

Parameter	0.13um CMOS	0.18um CMOS
Input transistor	PMOS	PMOS
L	$1\mu m$	$1\mu m$
V^*	$200mV$	$200mV$
Supply	$1.2V$	$1.8V$
Current consumption	$10\mu A$	$10\mu A$

- 3) The remaining variable in the design is to calculate W . Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation.

Create a testbench for PMOS transistor as shown below (we will use PMOS only in this lab). Use $W = 10\mu\text{m}$ (we will understand why shortly) and $L = 1\mu\text{m}$ (the same L selected before).



- 4) Sweep V_{GS} from 0 to $\approx V_{TH} + 0.4V$ with 10mV step. Set $V_{DS} = V_{DD}/2$.
- 5) We want to compare $V^* = 2I_D/g_m$ and $V_{ov} = V_{GS} - V_{TH}$ by plotting them overlaid. Use the calculator to create expressions for V^* and V_{ov} . You can save the expressions to reuse them later.
- 6) Plot V^* and V_{ov} overlaid vs V_{GS} . Make sure the y-axis of both curves has the same range. From the chart, you will notice that in the region of moderate inversion, V^* and V_{ov} are relatively close to each other (i.e., square-law is relatively valid). For strong inversion (large V_{ov}) or weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square-law.
- 7) An often used sweet-spot that provides good compromise between different trade-offs is $V^* = 200\text{mV}$. On the V^* and V_{ov} chart locate the point at which $V^* = 200\text{mV}$. Find the corresponding V_{ovQ} and V_{GSQ} .
- 8) Plot I_D , g_m , and g_{ds} vs V_{GS} . Find their values at V_{GSQ} . Let's name these values I_{DX} , g_{mX} , and g_{dsX} .
- 9) Now back to the assumption that we made that $W = 10\mu\text{m}$. This is not the actual value that we will use for our design. But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be $I_{DQ} = 10\mu\text{A}$ as given in the specs. Calculate W as shown below.

W	I_D
$10\mu\text{m}$	$I_{DX} @ V_Q^*$ (from the chart)
?	$I_{DQ} = 10\mu\text{A}$ (from the specs)

- 10) Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as V_{ov} is constant. On the other hand, $r_o = 1/g_{ds}$ is **inversely** proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross-multiplication).

PART 2: CD Amplifier

1. OP (Operating Point) Analysis

- 1) Create a new schematic for the CD amplifier (the schematic is not included in the lab document and is left for the student as an exercise). Use a PMOS and use a $10\mu\text{A}$ ideal current source for biasing (note that the current source will be connected to the source terminal). Connect the source to the bulk. Use $L = 1\mu\text{m}$ and W as determined in Part 1. Use $C_L = 2\text{pF}$, $R_{sig} = 2\text{M}\Omega$, and a DC input voltage = 0V.
- 2) Simulate the OP point. Report a snapshot clearly showing the following parameters (add a filter to your monitor).

ID
VGS
VDS
VTH
VDSAT
GM
GDS
GMB
CDB
CGD
CGS
CSB
Region

- 3) Check that the transistor operates in saturation.

2. AC Analysis

- 1) Perform AC analysis (1Hz:10GHz, logarithmic, 20points/decade) to investigate the frequency domain peaking.
- 2) Report the Bode plot magnitude.
- 3) Do you notice frequency domain peaking?
 ➔ Cadence Hint: Use the following expression to calculate the peaking in dB:
`ymin(dB20(VF("/vout")))`
- 4) Analytically calculate quality factor (use approximate expressions). Is the system underdamped or overdamped?
- 5) (Optional) Perform parametric sweep: CL = 2p, 4p, 8p.
 - Report Bode plot magnitude overlaid on same plot.
 - Report the peaking vs CL.
 - Comment.
- 6) (Optional) Perform parametric sweep: Rsig = 20k, 200k, 2M.
 - Report Bode plot magnitude overlaid on same plot.
 - Report the peaking vs Rsig.
 - Comment.

3. Transient Analysis

- 1) Use a pulse source (pulse_v_source) as your transient stimulus and set it as follows (delay = 2us, initial = 0V, period = 8us, pulse_value = 100mV, t_fall = 1ns, t_rise = 1ns, width = 4us). Run transient analysis (max step = 10n) for 10us to investigate the time domain ringing.
- 2) Report Vin and Vout overlaid vs time.
- 3) Calculate the DC voltage difference (DC shift) between Vin and Vout.
 - What is the relation between the DC shift and VGS?
 - How to shift the signal down instead of shifting it up?
- 4) Do you notice time domain ringing?
 ➔ Cadence Hint: Use the overshoot function to calculate the maximum overshoot as a percentage
- 5) (Optional) Perform parametric sweep: CL = 2p, 4p, 8p.
 - Report Vout vs time overlaid on same plot.
 - Report the overshoot vs CL.
 - Comment.
- 6) (Optional) Perform parametric sweep: Rsig = 20k, 200k, 2M.
 - Report Vout vs time overlaid on same plot.
 - Report the overshoot vs Rsig.
 - Comment.

4. Z_{out} (Inductive Rise) (optional)

- 1) We want to simulate the CD amplifier output impedance. Replace CL with an AC current source with magnitude = 1. Remove the AC input signal.
- 2) Perform AC analysis (1Hz:10GHz, logarithmic, 10points/decade). The voltage across the AC current source is itself the output impedance.
- 3) Plot the output impedance (magnitude and phase) vs frequency. Do you notice an inductive rise? Why?
- 4) Does Z_{out} fall at high frequency? Why?
Hint: C_{gd} appears in parallel with R_{sig} .
- 5) Analytically calculate the zeros, poles, and magnitude at low/high frequency for Z_{out} . Compare with simulation results in a table.

5. How to solve the peaking/ringing problem? (optional)

- 1) Place the input/output poles away from each other (as we did when we swept CL and Rsig).
- 2) (This part is optional) A compensation network can be used to compensate for the negative input impedance and prevent overshoots. Read [Johns and Martin, 2012] Section 4.4 and try to implement the compensation network.

Lab Summary

In Part 1 you learned:

- How to generate and use design charts for NMOS and PMOS transistors.
- How to design a PMOS common-drain amplifier.
- How the overdrive voltage of a MOS transistor deviates from the square law in different regions of operation.

In Part 2 you learned:

- How to do ac, DC and transient simulations of a CD amplifier.
- How the peaking in the frequency response of a CD amplifier changes with the load capacitor and source resistance.
- How the ringing in the transient response of a CD amplifier changes with the load capacitor and source resistance.
- How the output impedance of a CD amplifier shows inductive behavior.

Acknowledgements

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