وَمَا أُوتِيتُم مِّنَ الْعِلْمِ إِلَّا قَلِيلًا

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Analog IC Design
Lab 09 (Mini Project 01)
Two-Stage Miller OTA

Intended Learning Objectives

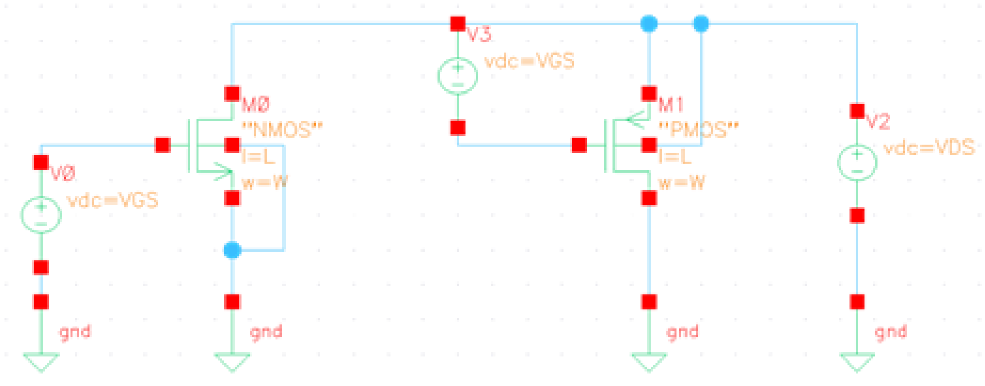
In this lab you will:

- Learn how to generate and use gm/ID design curves.
- Learn how to design a two-stage Miller OTA achieving given specifications.
- Learn how to simulate the open-loop characteristics of the two-stage Miller OTA.
- Learn how to simulate the closed-loop characteristics of the two-stage Miller OTA.

PART 1: gm/ID Design Charts

Use the following sweep ranges to characterize NMOS and PMOS transistors.

- W = 10um
- L = 0.2um:0.2um:5um → **parametric sweep**
- VGS ≈ (VTH-100m):5m:(VTH+VDD/3) → **DC sweep**
- VDS = VDD/3



Export simulation results to a csv file then import it in MATLAB.

→ Cadence Hint: In order to save OP point parameters vs DC sweep variable, create an empty text file and write the following statement (without quotes): "save *:oppoint sigtype=dev". Add this text file in adexl (Setup -> Model Libraries). If you are using SPICE models (e.g., Arizona PTM models) you need to add this statement at the beginning of the text file to switch back to Spectre (without quotes): "simulator lang = spectre".

Plot the following design charts vs gm/ID for both PMOS and NMOS[1]:

1) gm*ro
2) ID/W
3) gm/Cgg
4) VGS

PART 2: OTA Design

Use gm/Id methodology to design a differential input, single-ended output **two-stage Miller-compensated OTA**. The OTA is to be used as a buffer (unity gain feedback configuration) to probe sensitive internal signals in a complex mixed-signal design. The OTA should achieve the specs below.

Technology	0.13um	0.18um
Supply voltage	**1.2V**	**1.8V**
Static gain error	**<= 0.05%**	**<= 0.05%**
CMRR @ DC	**>= 74dB**	**>= 74dB**
Phase margin (avoid pole-zero doublets)	>= 70°	>= 70°
OTA current consumption	**<= 60uA**	**<= 60uA**
CMIR – high	**>= 0.6V**	**>= 1V**
CMIR – low	**<= 0.2V**	**<= 0.2V**
Output swing	**0.2 – 1V**	**0.2 – 1.6V**
Load	5pF	5pF
Buffer closed loop rise time (10% to 90%)	**<= 70ns**	**<= 70ns**
Slew rate (SR)	$5V/\mu s$	$5V/\mu s$

Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec), but design your own bias circuit (current mirrors). Create a schematic and an appropriate symbol for the OTA.

➔ Suggested Design Procedure (you may create your own!):

1) Use a single 10uA DC current source and a single DC voltage source in your test bench. Design your own current mirrors and bias circuitry.
2) A reasonable starting point for C_C is $0.5C_L$. You may refine this choice by doing sweeps in simulation.
3) Calculate the unity gain frequency (UGF) from the rise time requirement $(t_{rise} = 2.2\tau)$. Hence, calculate $g_{m1,2}$.

[1] While viewing MATLAB figure, use "View -> Plot Browser" to view the legend and enable or disable curves. While using the data cursor, right click on the cursor and select "Selection Style -> Mouse Position".

4) From the SR requirement, calculate the current required in the first stage (I_{B1}): $SR = \frac{I_{B1}}{C_C}$. Given the total current budget, calculate the current of the second stage.
5) Calculate gm/ID of the first stage.
6) Show that the closed-loop gain for a buffer is $A_{vCL} \approx 1 - \frac{1}{A_{vOL}}$, where A_{vOL} is the open-loop gain. Given A_{vCL} gain error spec $\left(\%error = \left|\frac{actual - ideal}{ideal}\right| \times 100\right)$, calculate the required DC gain in dB.
7) Assign larger gain for the first stage (why?). Do not split the gain equally between the two stages. You may assume the first stage gain is twice that of the second stage (6dB difference).
8) Given the 1st stage gain, calculate L (channel length) of the 1st stage input. You may assume input and load have the same gds.
9) Given gds/ID of the first stage current mirror load, select L. Note that gds/ID slightly increases with gm/ID, which is not known yet. To get an estimate for L, you may ignore this dependence and assume a relatively large gm/ID for the load at this point (e.g., gm/ID = 15).
10) Given the PM spec, calculate gm/ID of the second stage input transistor (Hint: assume $\omega_{p2} = 4\omega_u$).
11) Given the CMIR-high and Swing-high specs, calculate max vdsat for tail current source and output load. Take the lower value and assume V*= vdsat. Note that always V* > vdsat; thus, this assumption already adds some margin to make sure they are driven a little more into saturation. Now you have gm/ID of these two transistors. Note that these two transistors are identical (they form a current mirror; thus, they have same L and same gm/ID) except for the current (and width).
12) Use the CMRR spec to find gds of the tail current source (note that the second stage does not affect the CMRR). However, to complete this step you need gm of the current mirror load. This is not known yet, because we want VGS of 1st stage load = VGS of 2nd stage input. To break this deadlock, assume a relatively low gm/ID (e.g., gm/ID = 10) for first stage current mirror load[2]. Thus, get gds of tail current source.
13) Tail current source and 2nd stage load must have the same L (they form a current mirror). Thus, get gds of the 2nd stage load (note that both gm and gds are proportional to ID).
14) Given the 2nd stage gain, calculate gds and L of the 2nd stage input transistor. This transistor is now fully specified; thus, calculate its VGS.
15) Note that you need to avoid systematic offset. Use VGS charts to guarantee that 1st stage current mirror load and 2nd stage input transistor have the same VGS. Use this condition to determine the gm/ID of the current mirror load in the first stage. Check that the calculated gm/ID is larger than the one you assumed before (to guarantee that the CMRR is satisfied). Otherwise, re-iterate with the new gm/ID value (if the

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[2] For current mirror load, we first assumed gm/ID = 15 then we assumed gm/ID = 10. Is this contradicting? No. For the DC gain, we assumed a bit high gm/ID = 15 because if it is eventually a lower value (< 15) VA will be higher (gm/ID ↑ => V_A ↓) and the gain will be even better than the spec (positive error). Next, for the CMRR (Avcm) we assumed a bit low gm/ID = 10 because if it eventually higher (> 10) Avcm will be smaller and the CMRR will be even better than the spec (positive error). If eventually gm/ID < 10 or > 15 then we will have to reiterate.

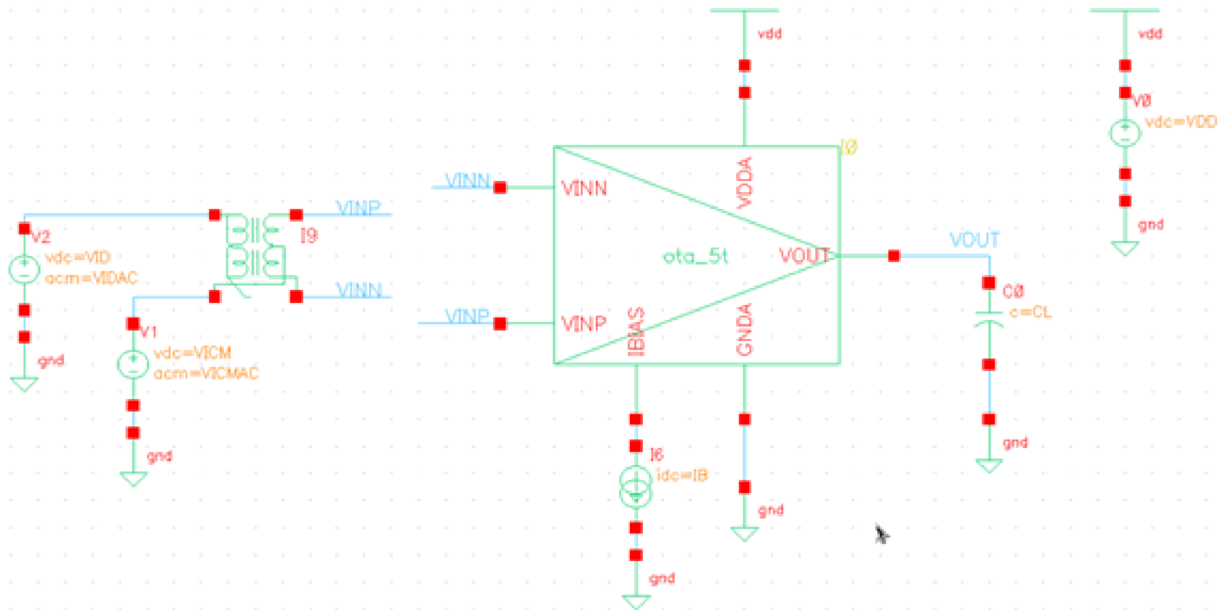
difference is large). If this step is not done properly, you will find that VOUT goes towards VDD or GND and one of the output transistors is out of saturation. In order to make sure that the systematic offset is canceled, you can sweep the width of the current mirror load with fine step till VOUT is around VDD/2.

16) Verify that your gm/ID choices do not violate the CMIR and the peak-to-peak output swing.
17) Choose R_Z to place the zero at infinity (some designers may move the LHP zero to the vicinity of the non-dominant pole to improve the PM). Do **NOT** place the LHP zero at a frequency less than ω_{p2}.

Report the following:

1) Detailed design procedure and hand analysis. Justify why you used NMOS or PMOS input pair for each stage.
2) A table showing W, L, g_m, I_D, g_m/I_D, $vdsat$, $V_{ov} = V_{GS} - V_{TH}$, and $V^* = 2I_D/g_m$ of all transistors (as calculated from gm/ID curves).

PART 3: Open-Loop OTA Simulation



Create a testbench similar to the one shown above (the shown schematic is from the 5T OTA lab). Note that IDC connection in the test bench (sinking or sourcing) may be different from the one shown above depending on the type of your input pair (PMOS/NMOS).

NOTE: The open-loop simulation will NOT work UNLESS there is ZERO offset voltage.

Report the following:

1) Schematic of the OTA and bias circuit with DC node voltages clearly annotated.
   - Use VICM at the middle of the CMIR.
   - Is the current (and gm) in the input pair exactly equal?
   - What is DC voltage at the output of the first stage? Why?
   - What is DC voltage at the output of the second stage? Why?

1) Diff small signal ccs:

- Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
- Set VIDAC = 1 and VICMAC = 0.
- Use VICM at the middle of the CMIR.

➔ Cadence Hint: Use Cadence calculator expressions to calculate circuit parameters (Ao, Ao in dB, BW, GBW, UGF). You may use Cadence calculator to create other useful expressions.

Name	Type	Expression/Signal/File
Ao	expr	ymax(mag(VF("/VOUT")))
Ao_dB	expr	dB20(ymax(mag(VF("/VOUT"))))
BW	expr	bandwidth(VF("/VOUT") 3 "low")
fu	expr	unityGainFreq(VF("/VOUT"))
GBW	expr	(Ao * BW)

- Plot diff gain (in dB) vs frequency.
- Compare simulation results with hand calculations in a table.

2) CM small signal ccs:

- Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
- Set VICMAC = 1 and VIDAC = 0.
- Use VICM at the middle of the CMIR.
- Plot CM gain in dB vs frequency.
- Compare simulation results with hand calculations in a table.

3) (Optional) CMRR:

➔ Cadence Hint: In Mentor Pyxis you have to get Avd and Avcm from two independent simulation runs (we cannot run both simultaneously because we have single ended output, thus we cannot differentiate between diff and CM signals at the output). But for Cadence Virtuoso you should use XF analysis (1Hz:10Gz, logarithmic, 10 points/decade) because you need to calculate the transfer function between multiple inputs and a single output.

➔ Cadence Hint: Access XF analysis results from the results browser or from adexl results tab (Right Click -> Direct Plot -> Main Form). You may use this expression in the calculator to plot the CMRR: dB20(mag(getData("/V2" ?result "xf"))) - dB20(mag(getData("/V1" ?result "xf"))) .

- Use VICM at the middle of the CMIR.
- Plot CMRR in dB vs frequency at VICM at the middle of the CMIR.
- Compare simulation results with hand calculations in a table.

2) (Optional) Diff large signal ccs:

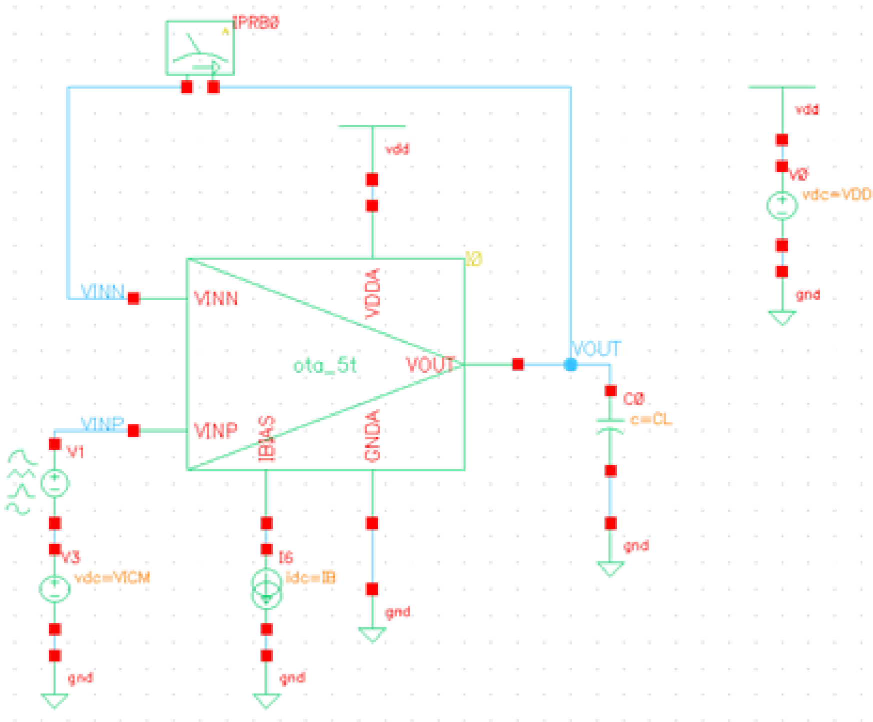
- Use VICM = VDD/2.
- Use DC sweep (**not parametric sweep**) VID = -0.1:0.1m:0.1. You must use a small step because the gain region is very small (steep slope).
- From the plot, what is the value of Vout at VID = 0. Compare it with the value you obtained in DC OP.
- Plot VOUT vs VID.

- Plot the derivative of VOUT vs VID. Compare the peak with Avd from ac analysis. Comment on the result.

4) CM large signal ccs (region vs VICM):
   - Use **DC sweep** (not parametric sweep) VICM = 0:10m:VDD.
   - Plot “region” OP parameter vs VICM for the input pair and the tail current source (0 cut-off, 1 triode, 2 sat, 3 subth, and 4 breakdown). Plot the results overlaid on the results of the previous method (10% reduction of GBW).
   - Plot “region” OP parameter vs VICM for the input pair and the tail current source.
   - Find the CM input range (CMIR). Compare with hand analysis in a table.
   - Note that the drawback of this method is that the “region” parameter cannot be experimentally measured in the lab.
5) (Optional) CM large signal ccs (GBW vs VICM):
   - Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
   - Set VIDAC = 1 and VICMAC = 0.
   - Use **parametric** sweep (**not DC sweep**) VICM = 0:10m:VDD.
   - Use Measures or EXTRACT to calculate the GBW.
   - Plot GBW vs VICM. Plot the results overlaid on the results of the previous method (region parameter).
   - Annotate the CM input range. Calculate the input range as the range over which the GBW is within 90% of the max GBW, i.e., 10% reduction in GBW[3].

[3] If you are using NMOS input pair, body effect may cause CMIR to extend till VDD (why?).

PART 4: Closed-Loop OTA Simulation



Create a new testbench with the OTA connected in a unity gain buffer feedback configuration (the shown schematic is from the 5T OTA lab). Place a current probe (iprobe) or a zero voltage source in the feedback loop.

Report the following:

1) Schematic of the OTA and the bias circuit with DC OP point clearly annotated in unity gain buffer configuration.
   - Use VICM at the middle of the CMIR.
   - Are the DC voltages at the input terminals of the op-amp exactly equal? Why?
   - Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?
   - Is the current (and gm) in the input pair exactly equal? Why?
2) Loop gain:
   - Use STB analysis (1Hz:10Gz, logarithmic, 10 points/decade) in unity gain buffer configuration.
   - Use VICM at the middle of the CMIR.
   - Plot loop gain in dB and phase vs frequency.

➔ Cadence Hint: Access STB analysis results from the results browser or from adexl results tab (Right Click in adexl Results tab-> Direct Plot -> Main Form).

   - Compare DC gain, fu, and GBW with those obtained from open-loop simulation. Comment
   - Report PM. Compare with hand calculations. Comment.
   - Compare simulation results with hand calculations in a table.

3) Slew rate:

- Apply a step input with the following parameters (delay = 1us, initial value = CMIR-low + 50mV, final value = CMIR-high – 50mV, rise time = 1ns, period = 1s, width = 1s). Note that we want a single step input, which is why we selected very large period and width for the pulse.
- Run transient analysis (stop = 5us and step = 0.1ns).
- Report Vin and Vout overlaid.
- Report the slew rate.
- Compare simulation results with hand calculations in a table.

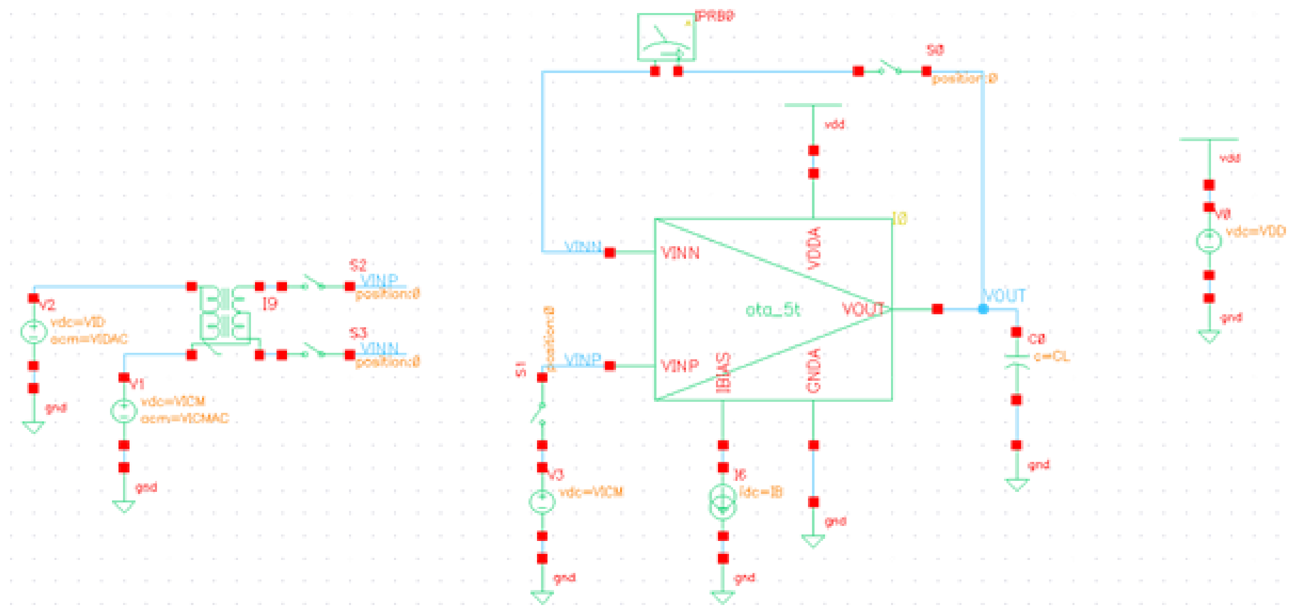
4) Settling time:

- Apply a small signal step input with the following parameters (delay = 1us, initial value = the middle of the CMIR, final value = the middle of the CMIR + 5mV, rise time = 1ns, period = 1s, width = 1s). Note that we want a single step input, which is why we selected very large period and width for the pulse. Note that we apply a small signal pulse (5mV step) to measure the small signal settling time.
- Calculate the output rise time from simulation.
- Compare simulation results with hand calculations in a table[4].
- Do you see any ringing? Why?

Part 5 (optional): DC Closed Loop AC Open-Loop OTA Simulation

Note that there will always be residual offset voltage between the first and second stages. This offset will drive the second stage output to one of the rails; thus, the biasing of the output stage will be disturbed. In order to avoid this problem, the DC OP point must be set by feedback, e.g., by putting the amplifier in unity gain buffer configuration in DC. Use a testbench similar to the one used in the 5T OTA lab as shown below. **Switches (sp1tswitch from analogLib library) are added in order to connect the feedback loop in DC and break it in AC (another option is to use resistors with different AC/DC values). Set S0 and S1 DC closed, and set S2 and S3 AC closed. The DC OP point is set by the unity gain feedback buffer connection, while the AC stimulus is set by the balun.**

[4] The simulation result will be better than expected. Why? (Hint: Using trise = 2.2τ is based on first-order model. Is second-order system faster?)



Lab Summary

- In Part 1 you learned:
  - How to generate and use gm/ID design curves.
- In Part 2 you learned:
  - How to design two-stage Miller OTA meeting desired specifications.
- In Part 3 you learned:
  - How to simulate the small-signal differential gain of two-stage Miller OTA in open-loop configuration.
  - How to simulate the small-signal common-mode gain of two-stage Miller OTA in open-loop configuration.
  - How to simulate the large-signal differential characteristics of two-stage Miller OTA in open-loop configuration.
  - How to simulate the large-signal common-mode characteristics of two-stage Miller OTA in open-loop configuration.
- In Part 4 you learned:
  - How to simulate the small-signal differential gain of two-stage Miller OTA in closed-loop configuration.
  - How to simulate the small-signal common-mode gain of two-stage Miller OTA in closed-loop configuration.
  - How to simulate the large-signal differential characteristics of two-stage Miller OTA in closed-loop configuration.
  - How to simulate the large-signal common-mode characteristics of two-stage Miller OTA in closed-loop configuration.
- In Part 5 you learned:
  - How to use dc closed-loop configuration to simulate an ac open-loop configuration.

Acknowledgements

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