وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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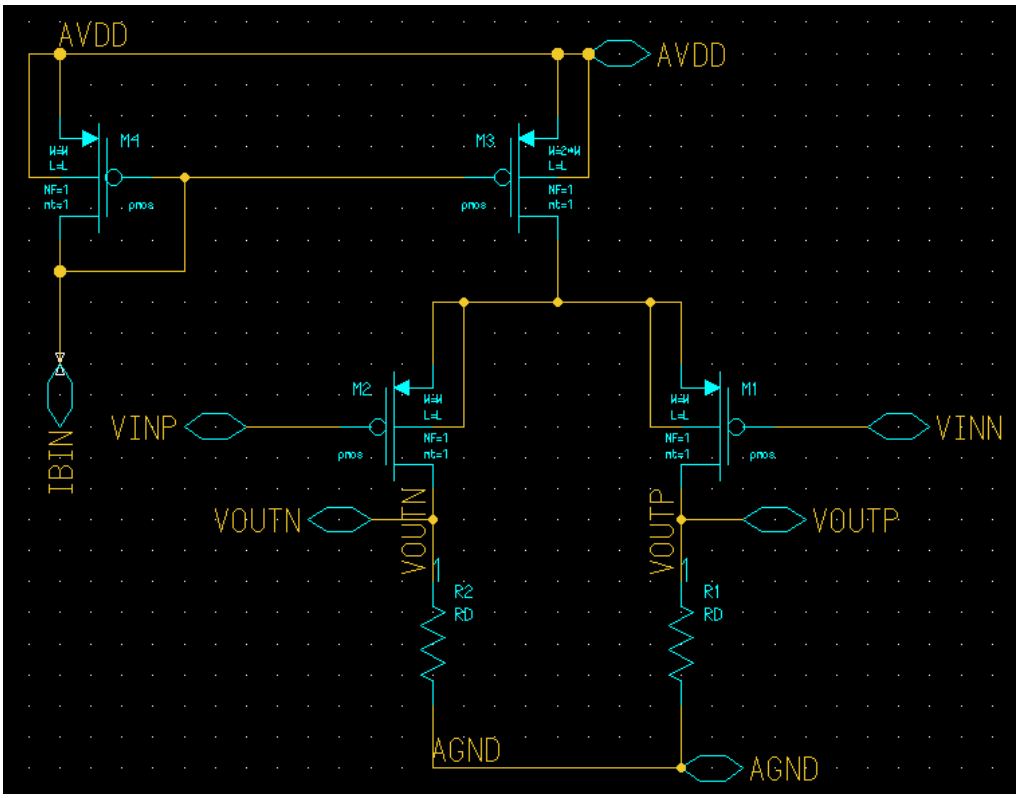
Analog IC Design
Lab 06
Differential Amplifier

Intended Learning Objectives

In this lab you will:

- Design and simulate a differential amplifier.
- Learn how to simulate the small-signal differential characteristics of a differential amplifier.
- Learn how to simulate the small-signal common-mode characteristics of a differential amplifier.
- Learn how to simulate the large-signal differential characteristics of a differential amplifier.
- Learn how to simulate the large-signal common-mode characteristics of a differential amplifier.



PART 1: Sizing Chart

1) We can show that the intrinsic gain of a MOSFET is given by

$$|A_v| \approx g_m r_o = \frac{2I_D}{V_{ov}} \times \frac{V_A}{I_D} = \frac{2V_A}{V_{ov}}$$

Interestingly, the gain only depends on λ and V_{ov}. However, to derive this expression we used $g_m = \frac{2I_D}{V_{ov}}$ which is based on the square-law. For a real MOSFET, if we compute V_{ov} and $\frac{2I_D}{g_m}$ they will not be equal. Let's define a new parameter called V-star (V^*) which is calculated from actual simulation data using the formula

$$V^* = \frac{2I_D}{g_m} \leftrightarrow g_m = \frac{2I_D}{V^*}$$

For a square-law device, $V^* = V_{ov}$, however, for a real MOSFET they are not equal. The actual gain is now given by

$$|A_v| \approx \frac{2V_A}{V^*}$$

The lower the V^* the higher the gain, but the larger the area and the lower the speed.

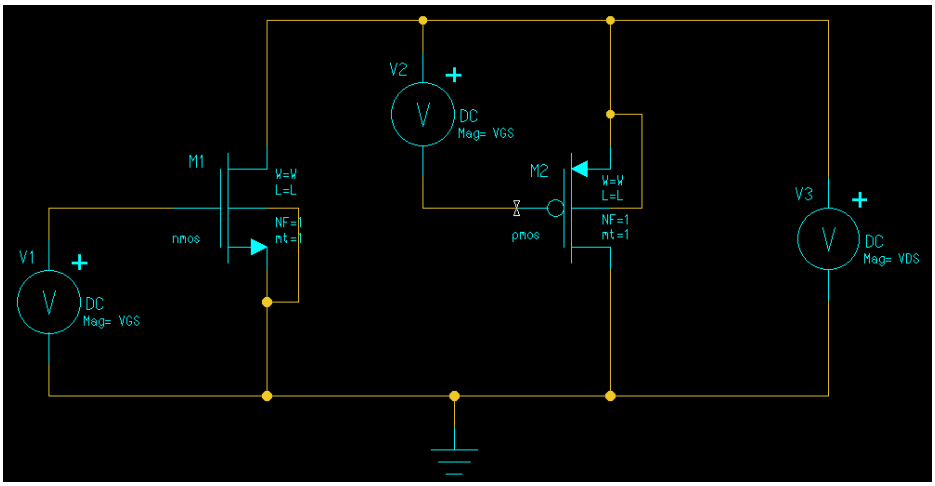
2) We want to design a differential amplifier with the specifications below. Note that the bias current is split between two transistors; each transistor gets $I_D = 20\mu A$.

Parameter	130 nm	180 nm
$\boldsymbol{L}$	$1\mu m$	$1\mu m$
CM output level[1]	0.5	0.7
Differential gain	5	8
Supply	$1.2V$	$1.8V$
Bias current $(\boldsymbol{I_{SS}})$	$40\mu A$	$40\mu A$

3) Choose R_D to meet the CM output level spec.
4) We can show that the differential amplifier gain is given by

$$|A_v| \approx g_m R_D = \frac{2I_D}{V^*} \times R_D = \frac{2V_{R_D}}{V^*}$$

5) Choose V^* to meet the differential gain spec.
6) The remaining variable in the design is to calculate W. Since the square-law is not accurate, we cannot use it to determine the sizing. Instead, we will use a sizing chart generated from simulation. Create a testbench for PMOS transistor as shown below (**we will use PMOS only in this lab**). Use $W = 10\mu m$ (we will understand why shortly).



7) Sweep VGS from 0 to $\approx V_{TH} + 0.4V$ with 10mV step. Set $V_{DS} = V_{DD}/2$.

[1] ISS*RD must be smaller than (VDD – V_{dsat3}) for proper large signal characteristics (why?).

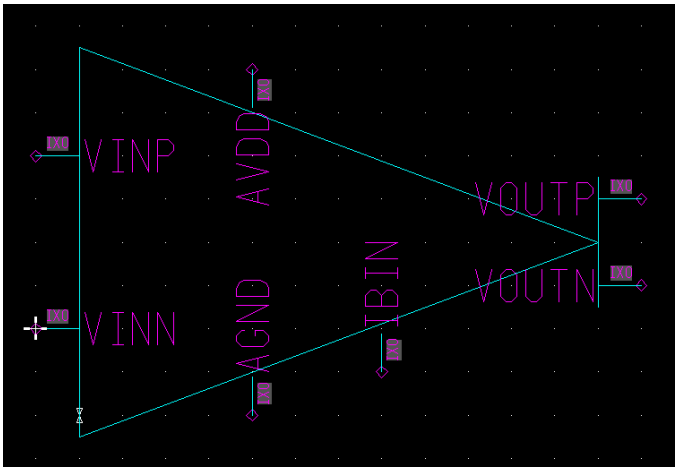
8) We want to compare $V^* = 2I_D/g_m$ and $V_{ov} = V_{GS} - V_{TH}$ by plotting them overlaid. Use the calculator to create expressions for V^* and V_{ov}. You can save the expressions to reuse them later.
9) Plot V^* and V_{ov} overlaid vs VGS. Make sure the y-axis of both curves has the same range. From the chart, you will notice that in the region of moderate inversion, V^* and V_{ov} are relatively close to each other (i.e., square-law is relatively valid). For strong inversion (large V_{ov}) or weak inversion (near-threshold and subthreshold operation) the behavior is quite far from the square-law.
10) On the V^* and V_{ov} chart locate the point at which V^* is equal to the value your previously calculated to meet the gain spec. Find the corresponding V_{ovQ} and V_{GSQ}.
11) Plot I_D, g_m, and g_{ds} vs V_{GS}. Find their values at V_{GSQ}. Let's name these values I_{DX}, g_{mX}, and g_{dsX}.
12) Now back to the assumption that we made that $W = 10\mu m$. This is not the actual value that we will use for our design. But the good news is that I_D is always proportional to W irrespective of the operating region and the model of the MOSFET (regardless square-law is valid or no). Thus, we can use ratio and proportion (cross-multiplication) to determine the correct width at which the current will be I_{DQ} as given in the specs. Calculate W as shown below.

W	I_D
$10\mu m$	I_{DX} @V_Q^* (from the chart)
?	$I_{DQ} = 20\mu A$ (from the specs)

13) Now we are almost done with the design of the amplifier. Note that g_m is also proportional to W as long as V_{ov} is constant. On the other hand, $r_o = 1/g_{ds}$ is **inversely** proportional to W (I_D) as long as L is constant. Before leaving this part, calculate g_{mQ} and g_{dsQ} using ratio and proportion (cross-multiplication).

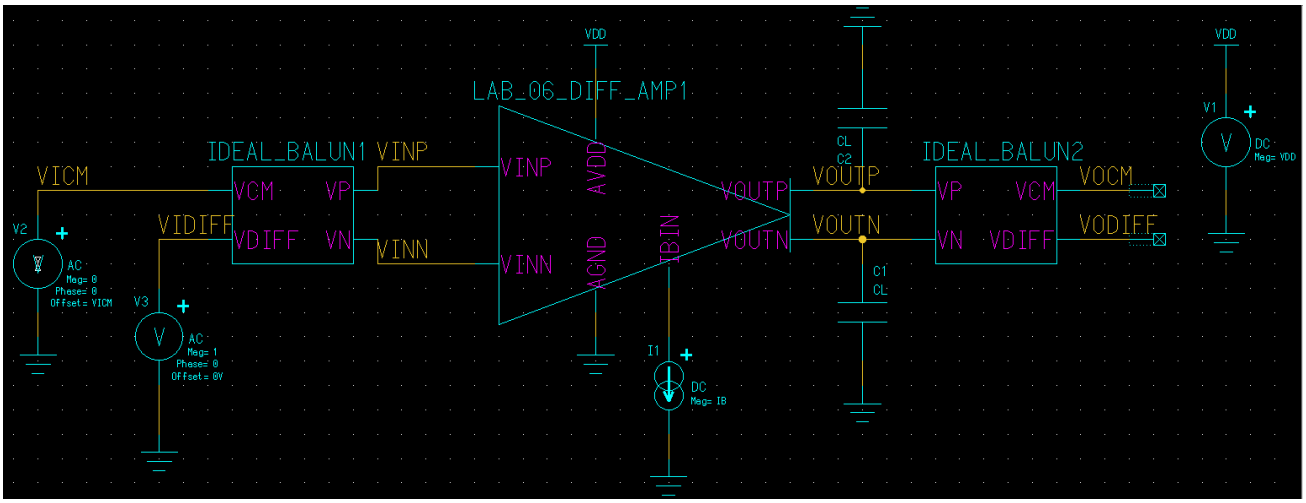
PART 2: Differential Amplifier

1) Create a new cell for the diff amp "lab_06_diff_amp". Create the schematic of a differential amplifier with PMOS input stage and resistive load. Use a simple current mirror for the bias current source as shown in the first figure in this document.
2) Create a symbol for the diff pair (use Create -> Cellview -> From Cellview).
3) Edit the diff amp symbol to be as shown below.



4) Create a new cell for the testbench "lab_06_diff_amp_tb". Create testbench schematic as shown below.

➔ Cadence Hint: Use ideal_balun from analogLib to separate common-mode and differential signals. In Mentor tools you have to create the balun yourself.



5) Size the transistors as designed in Part 1.
6) Use IB = 20uA (the CM multiplies this by 2, so each half in the diff pair gets IB).
7) Connect floating wires to noConn instance from basic library to avoid floating signal warnings.
8) Use CL = 1pF.
9) Analytically calculate the valid range for Vicm: the common mode input range (CMIR). Set Vicm at the center of this range.
   ➔ Cadence Hint: In adexl you can access the results of the last 10 simulation runs from the "History" tab. We want to access the last two simulation runs in order to compare Avd and Avcm. Open both simulations in the Results Browser.

Report the following:

1) OP simulation.
   - Report the schematic of the diff pair with DC OP point clearly annotated: id, vgs, vds, vth, vdsat, gm, gds, gmb, region.
   - Check that all transistors operate in saturation.
2) Diff small signal ccs:
   - Use AC magnitude = 1 for the diff source (and AC magnitude = 0 for the CM source).
   - Set Vicm at the center of the CMIR.
   - Run AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).
   - Report the Bode plot of small signal diff gain.
   - Compare the DC diff gain and BW with hand analysis in a table.
3) CM small signal ccs:
   - Use AC magnitude = 1 for the CM source (and AC magnitude = 0 for the diff source).
   - Run AC analysis (1Hz:10GHz, logarithmic, 10 points/decade).
   - Report the Bode plot of small signal CM gain.
   - Compare the DC CM gain with hand analysis in a table. Is it smaller than "1"? Why?
   - Justify the variation of Avcm vs frequency.
   - Plot Avd/Avcm in dB. Compare Avd/Avcm @ DC with hand analysis in a table.
   - Justify the variation of Avd/Avcm with frequency.

➔ Cadence Hint: Note that xf analysis cannot be used in this case because we have two outputs (Diff and CM). xf analysis is useful for the case of single-ended output op-amp where there is only one output terminal. It is also useful for fully diff op-amp to calculate CMRR(SE2diff), but not Avd/Avcm.

4) Diff large signal ccs:
   - Use dc sweep (not parametric sweep) for Vid = -VDD:10m:VDD. Set Vicm at the center of the CMIR.
   - Report diff large signal ccs (VODIFF vs VIDIFF). Compare the extreme values with hand analysis in a table.
5) CM large signal ccs (region vs VICM):
   - We will use the region parameter to know the operating region of each transistor vs sweep variable.

   ➔ Cadence Hint: The "region" meaning is as follows:

   0: cut-off

   1: triode

   2: sat

   3: subth

   4: breakdown

   - Use DC sweep (not parametric sweep) for Vicm = 0:10m:VDD (no need to run AC sim)

   ➔ Cadence Hint: To save the "region" parameter, add this this line to your save.scs file (in Model Libraries):

   save *:region sigtype=dev.

   - Disable ac analysis.
   - Plot "region" OP parameter vs VICM for the input pair and the tail current source.
   - Find the CM input range (CMIR). Compare with hand analysis in a table.
   - Note that the drawback of this method is that the "region" parameter cannot be experimentally measured in the lab and is not quantitively related to circuit specifications.
6) CM large signal ccs (GBW vs Vicm):
   - Use ac analysis (start = 1, stop = 1, pts(linear) = 1) to get Avd. Use parametric sweep (not dc sweep) for Vicm = 0:20m:VDD.

   ➔ Cadence Hint: Instead of using parametric sweep, a better alternative in Cadence is to use AC sweep but sweep a design variable (Vicm) instead of sweeping the frequency. The frequency is set at 1 Hz (or any other small value) to get the low frequency gain (DC gain).

   ➔ Cadence Hint: Use the following expression in adexl to calculate Avd: ymax(mag(VF("/VODIFF")))

   - Note that the bandwidth is determined by RD and CL, thus Avd variation is itself GBW variation.
   - Report CM large signal ccs (Avd vs Vicm). Assume the valid range for Vicm (CMIR) is defined by the condition that Avd is within 90% of the max gain, i.e., 10% drop in gain.
   - Plot the results overlaid on the results of the previous method (region parameter). Find the CM input range. Compare with the previous method in a table.

Lab Summary

- In Part 1 you learned:
  - How to generate and use design charts for NMOS and PMOS transistors.
  - How to design a resistive-loaded differential amplifier.
- In Part 2 you learned:

    - How to use an ideal balun.
- In Part 3 you learned:
    - How to simulate the small-signal differential gain of a differential amplifier.
    - How to simulate the small-signal common-mode gain of a differential amplifier.
    - How to simulate the large-signal differential characteristics of a differential amplifier.
    - How to simulate the large-signal common-mode characteristics of a differential amplifier.

Acknowledgements

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