Cairo University
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جامعة القاهرة

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Electronics ELC401A

CMOS Operational Amplifier Design

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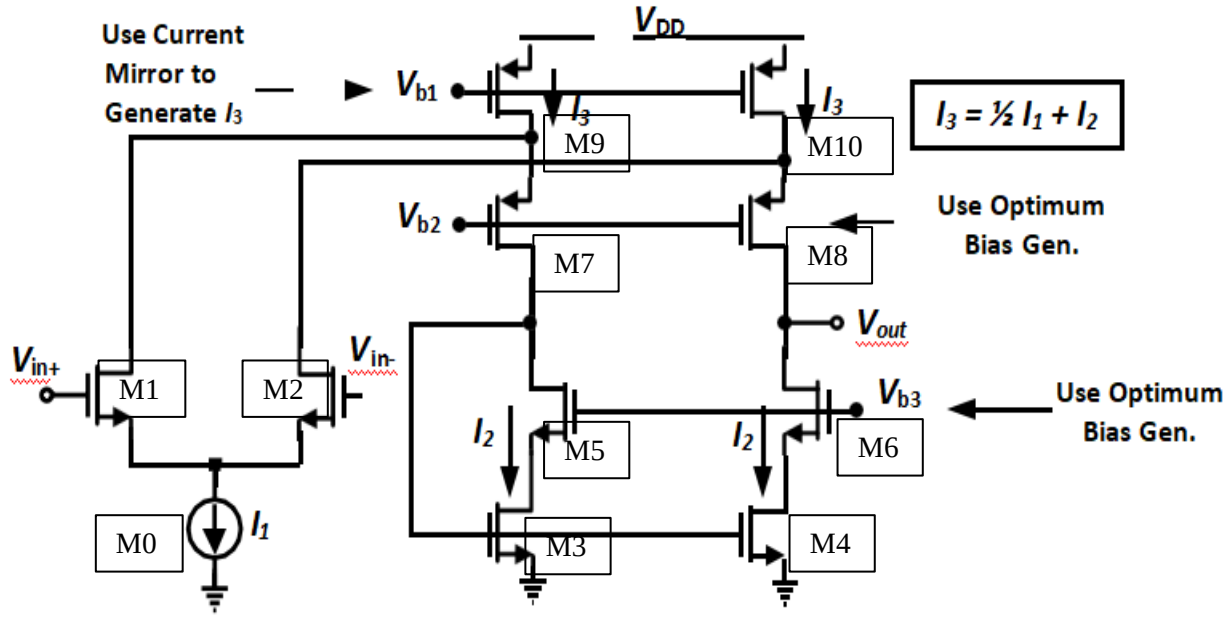
1. Problem Definition: Folded-Cascode Operational Amplifier for Buffer Use



1.1. Specifications Problem Analysis

You are required to design the single-ended single-stage op-amp shown such that:

- V_{DD} = 3.3V Tsmc130nm Nmos3v/Pmos3v of Vth=650mv
- V_{inCM} = V_{DD} / 2 = 1.65 V V_{DS1} , V_{DS2} is fixed at a certain value
- A_{DC} > 55 dB (DC differential gain) Vds=Veff+100mV
- GBW > 100 MHz for a load of 2pF Inv. Prob. Tunable Range for Bias of I_1
- Slew Rate > 100 V/μsec Small Signal Analysis
- Output Swing > 1.5V_{pp} Large Signal Analysis
- Input referred thermal noise density < $10nV/\sqrt{Hz}$
- PM > 60 degrees Inversely Proportional with GBW Tunable Range for Bias of I_1
- Minimize power consumption Vb Power Consumption

1.2. Large Signal Analysis

Specs & Givens:

- O/P Swing = $1.5V_{pp}$
- $V_{th\ n,p}$~= 650 mV
- $V_{DS}=V_{ov}+100mV$
- $V_{DD}=3.3$ V

Solution:

- Step1: Determine Overdrive Voltage:

$$V_{out,min} > V_{th} + V_{ov} \cap V_{out,min} > 2V_{ov} = V_{out,min} > V_{th} + V_{ov}$$
$$V_{out,max} < V_{DD} - 2V_{ov}$$
$$Output\ Swing = V_{out,max} - V_{out,min} = V_{DD} - 3V_{ov} - V_{th} > 1.5\ V_{pp}$$
$$choose\ V_{ov} = 0.3$$

- Step2: Determine Vb1 from overdrive voltage and V_{DS}=Vov+100mV

$$V_{DD} - V_{b1} = Veff + Vth + 0.1$$
$$V_{b1} = 2.25\ V$$

$$3.3 - V_{ov} - 0.1 - V_{b2} = (V_{ov} + V_{th}) + 0.1$$
$$V_{b2} = 1.85\ V$$

- Step3: Determine Vb2 from Vb1, overdrive voltage and V_{DS}=Vov+100mV

$$2Vth + Vov > V_{b3} > V_{th} + 2 * V_{ov}$$
$$for\ best\ swing\ choose\ V_{b3,min} = V_{th} + 2 * V_{ov} + 0.01 = 1.26\ V$$

- Step4: Determine bias voltage for M0

805mV< Vg of M0 < 850mV

if we choose max we will have max GBW and smallest phase margin and if we take the min opposite will occur so it is better to choose in between like 830mV

1.3. Small Signal Analysis

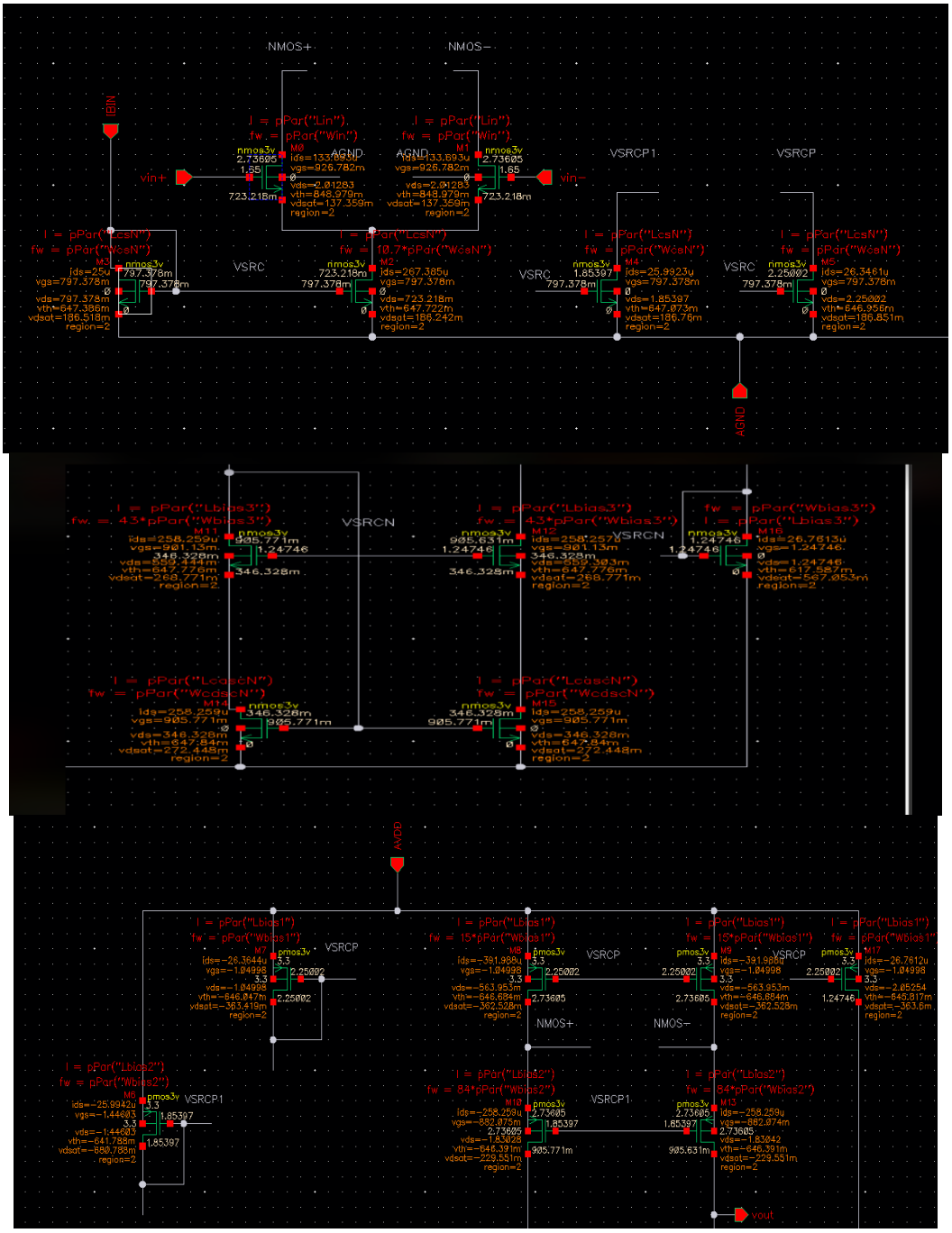
- Model Parameter Extraction neglecting short channel effects
  - Kn: 16 uA/V2
  - Vthn: 0.62
  - Kp: 6 uA/V2
  - Vthp: 0.63
  - L=1um
- Extracting Small Signal Parameters:
  - Slewrate > 100V/usec===>gm1,2=1.294mA/V
  - Bandwidth > 100MHz===> gm3,4=gm5,6=1.294mA/V

M#	Vg	W/L	Type	M#	Vg	W/L	Type
0	830mV	80.25	NMOS	5,6	1.26V	39.75	NMOS
1,2	1.65(given)	68.1	NMOS	7,8	1.85V	39.75*2	PMOS
3,4	Vout	39.75	NMOS	9,10	2.25V	39.75*2	PMOS

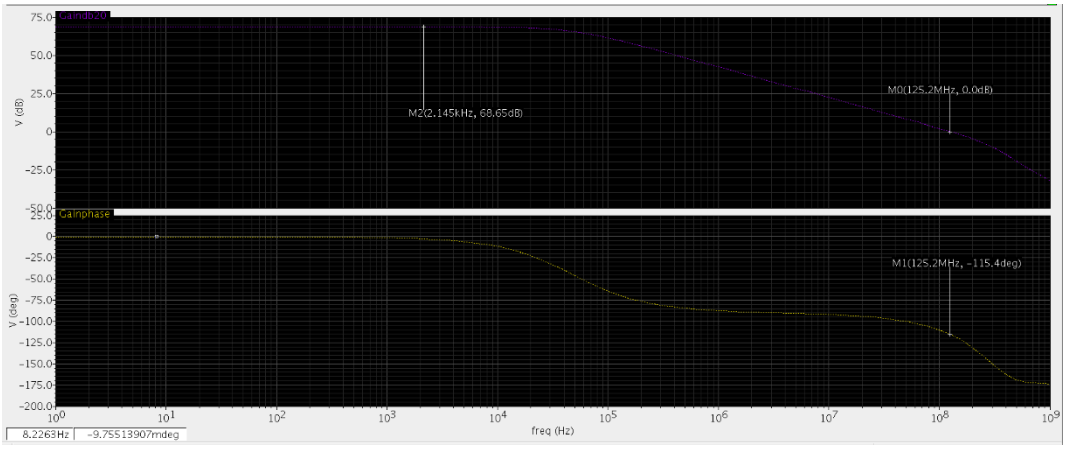
2. Simulations

2.1. Simulate the circuit (inside opamp)

2.1.1. Print all transistor operating point information (DC)



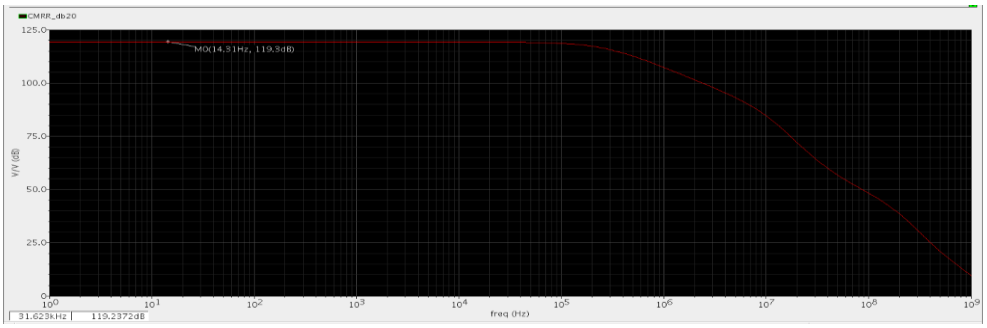
2.1.2. Plot the gain and phase versus frequency (AC). Show open-loop gain and PM



Comments:

Gain-Bandwidth product is about 125MHz>100MHz and Phase margin=180-115=65>60 degrees and DC-Gain=68.65dB>50dB

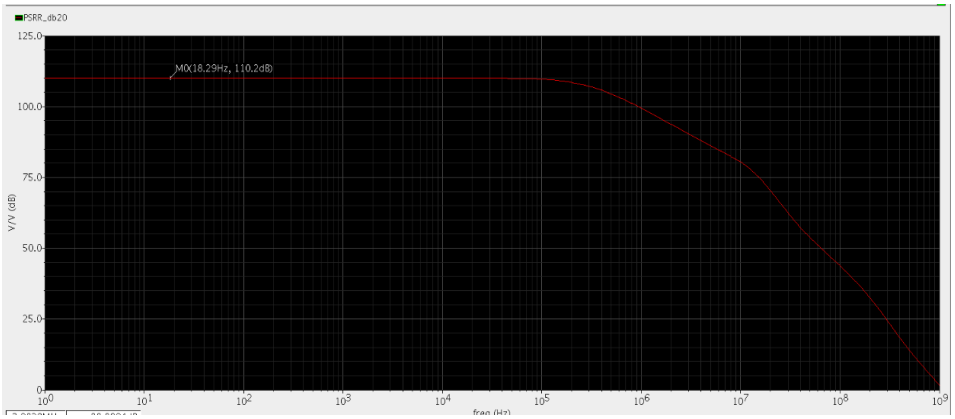
2.1.3. Plot the common-mode rejection ratio (CMRR)



Comments:

Common Mode Rejection Ratio is about 113 dB which is very high and make opamp act with very good efficiency in rejecting noise

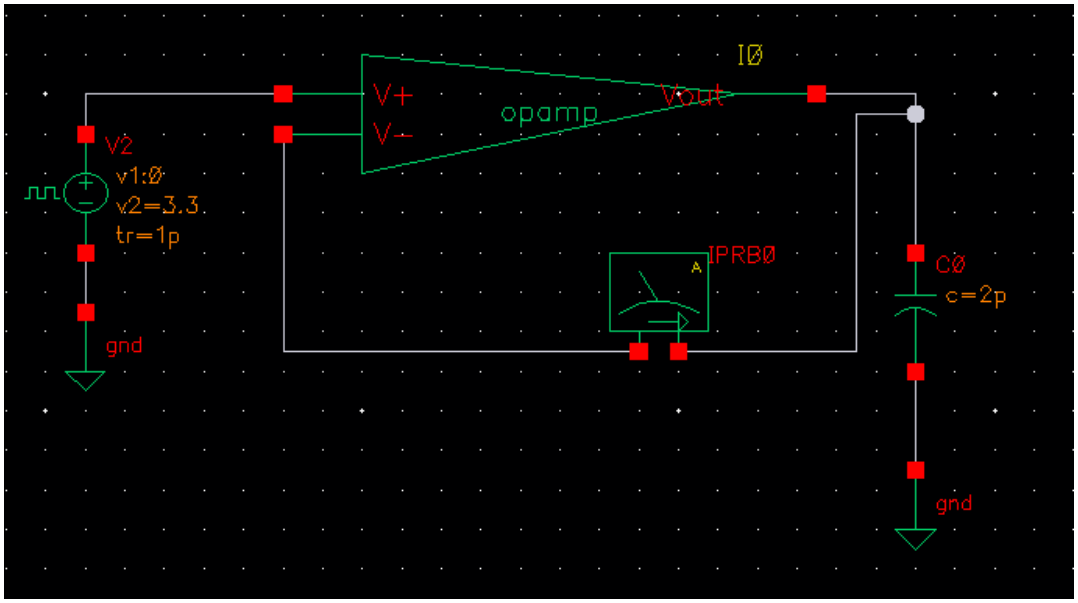
2.1.4. Plot the power supply rejection ratio (PSRR)



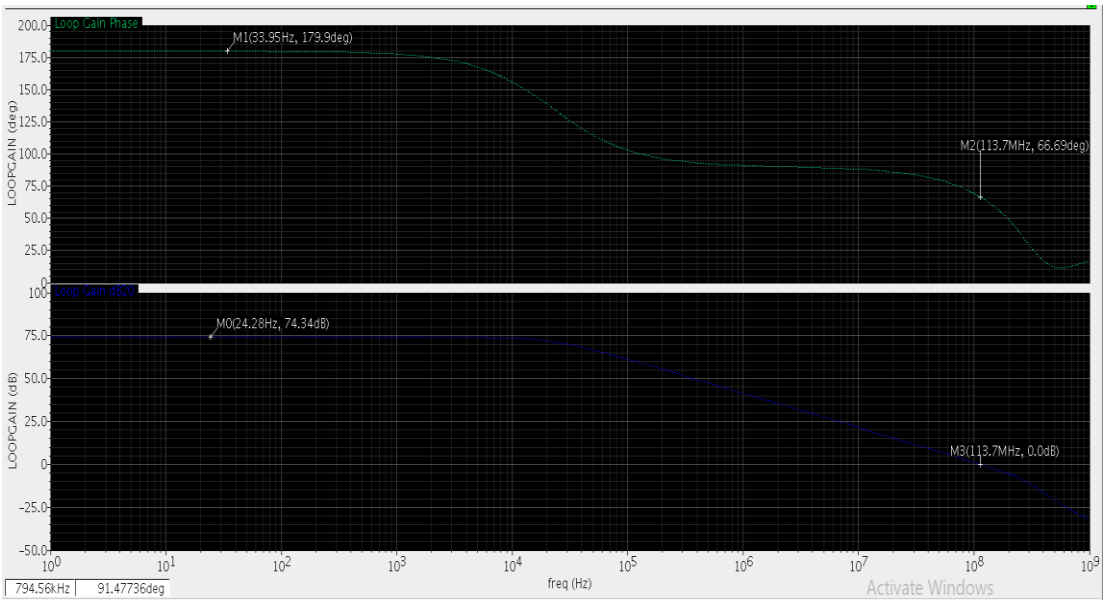
Comments:

Power supply rejection ratio is very high about 110 dB which means the high capability of this opamp to reject supply voltage variations

2.2. Place the op-amp in a unity feedback (Buffer) configuration:



2.2.1. Plot STB gain and phase versus frequency (AC) and calculate open-loop gain and PM



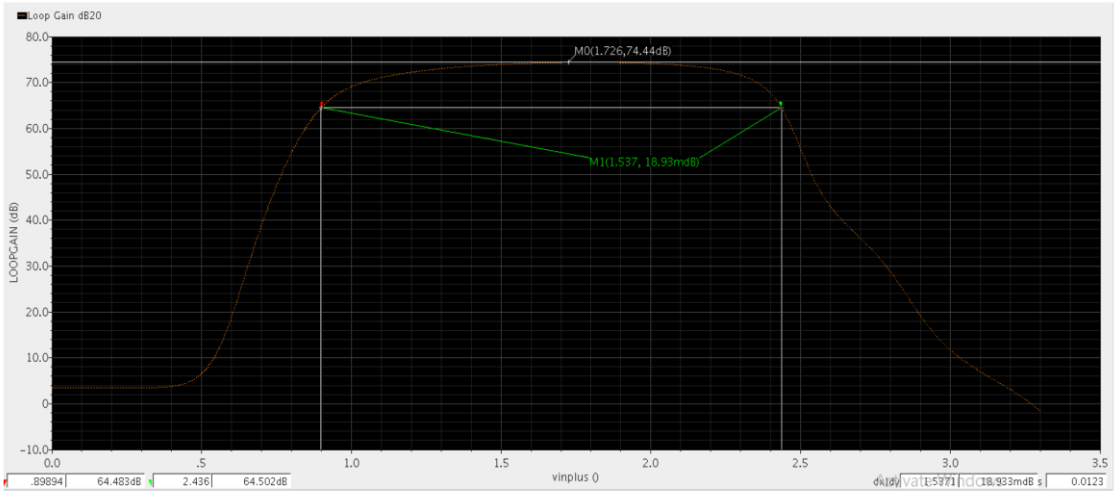
Comments:

Gain-Bandwidth product is 113.7 MHz and DC-gain=74.35dB

2.2.2. What is the difference between those results and previous open-loop AC results?

Using Probe sees another capacitance when measuring at input port of the opamp

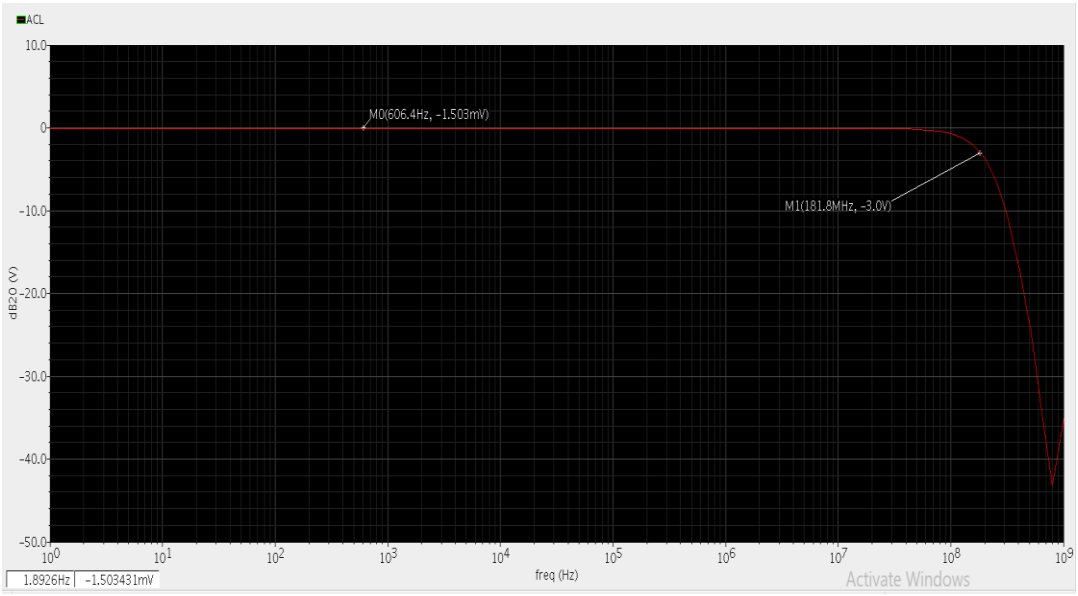
2.2.3. Plot the DC-gain versus V_{out} (report when DC-gain drops by 10dB to verify specifications)



Comments:

Output Swing is of value = 1.54Vpp > 1.5Vpp

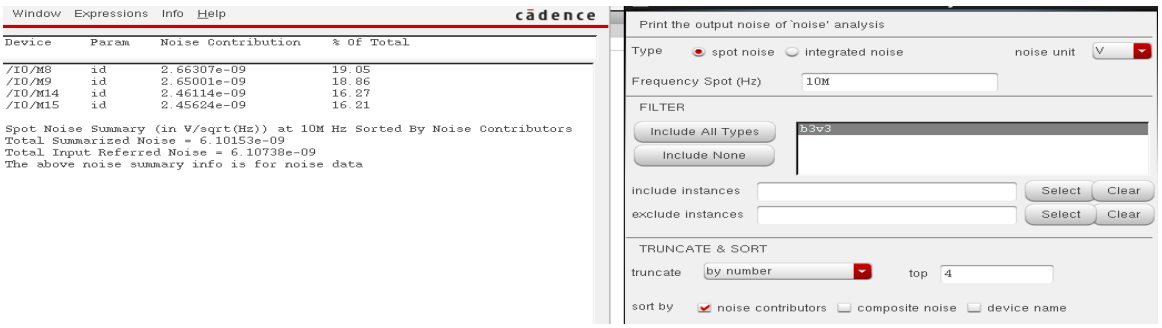
2.2.4. Plot the closed-loop (CL) frequency response. What is A_{CL} and BW_{CL} (comment)?



Comment:

Bandwidth is extended to 181.8 MHz and DC gain remains -1.503 mdb (Buffer since it ‘s very near to 0)

2.2.5. Simulate input-referred noise and tabulate top 4 contributors @10MHz (comment).



Window Expressions Info Help — cadence

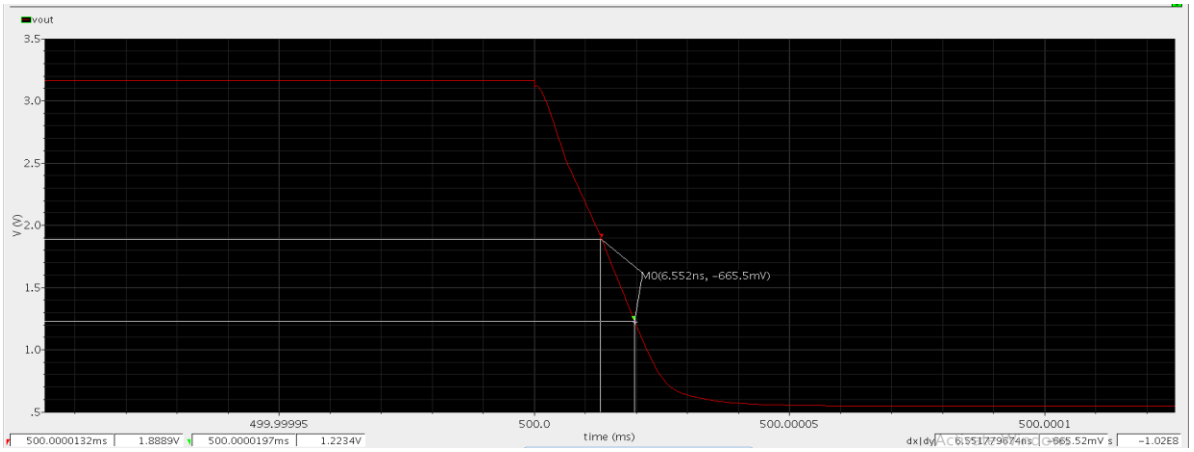
Device	Param	Noise Contribution	% Of Total
/IO/M8	id	2.66307e-09	19.05
/IO/M9	id	2.65001e-09	18.86
/IO/M14	id	2.46114e-09	16.27
/IO/M15	id	2.45624e-09	16.21

Spot Noise Summary (in V/sqrt(Hz)) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 6.10153e-09
Total Input Referred Noise = 6.10738e-09
The above noise summary info is for noise data

Comments:

Total input referred noise is of value 6.1 nV/ sqrt(Hz) < 10nV/sqrt(Hz)

2.2.6. Simulate the slew rate and verify the specifications.

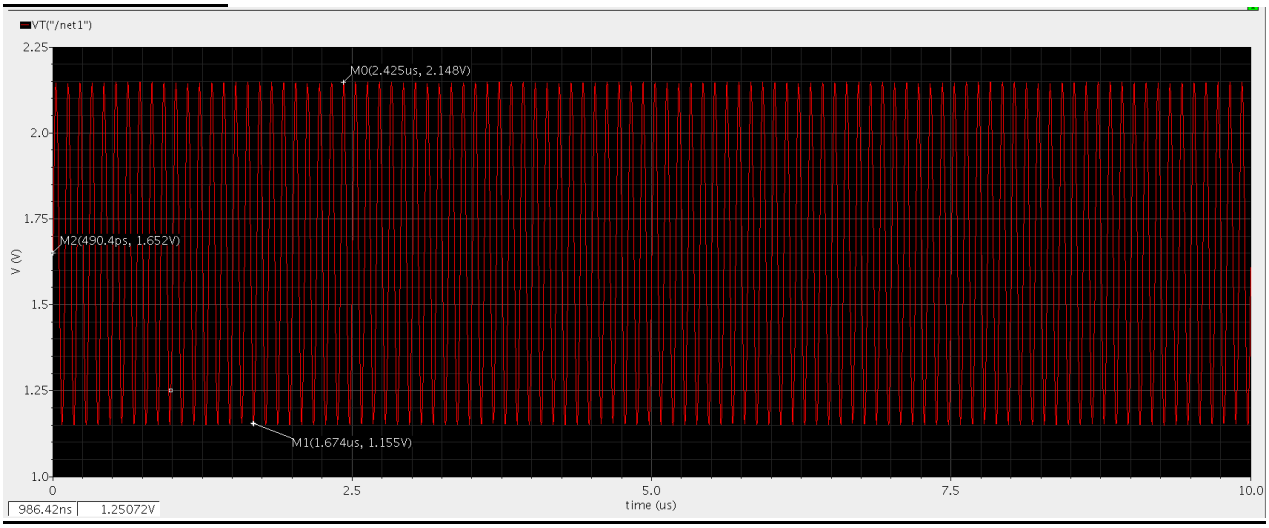


Comments:

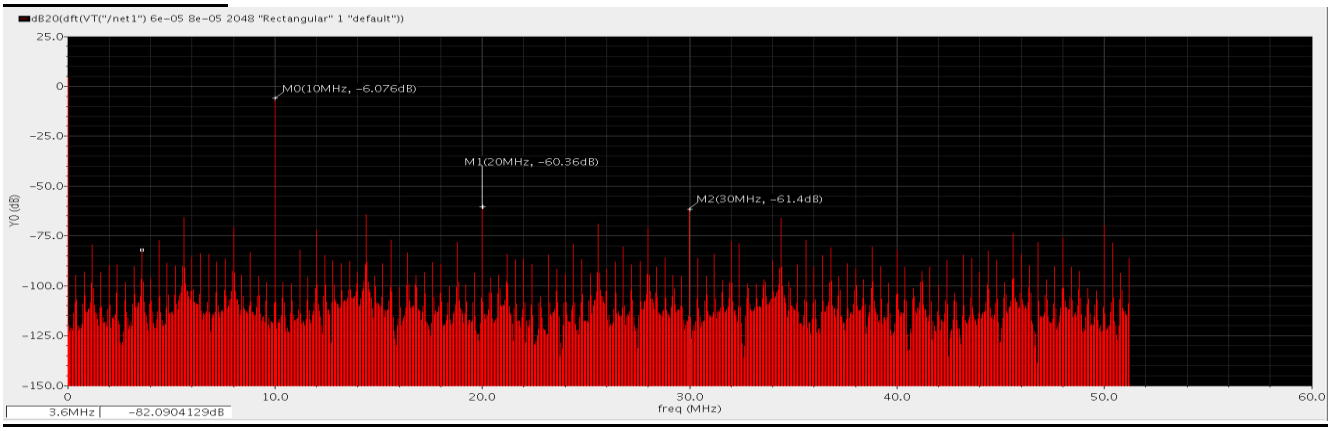
Slew rate is 102v/usec. > 100v/usec.

2.2.7. Apply a sine input signal of 1V_{pp} @10MHz and plot V_{out} (add proper input DC value). Plot DFT (in dB) and calculate harmonic distortion HD2, HD3, and THD (comment).

-plot V_{out} vs time:



-plot DFT of V_{out} (db20) vs frequency :



Comment:

AT 10 MHZ, The harmonic distortion=-6 db is clearly high since the source is excited at 10 MHz.

$HD2 = -60.36 + 6.07 = -54.29\ db, HD3 = -61.4 + 6.07 = -55.33\ db.$

--calculating THD :

We will use the calculator in cadence to calculator THD :

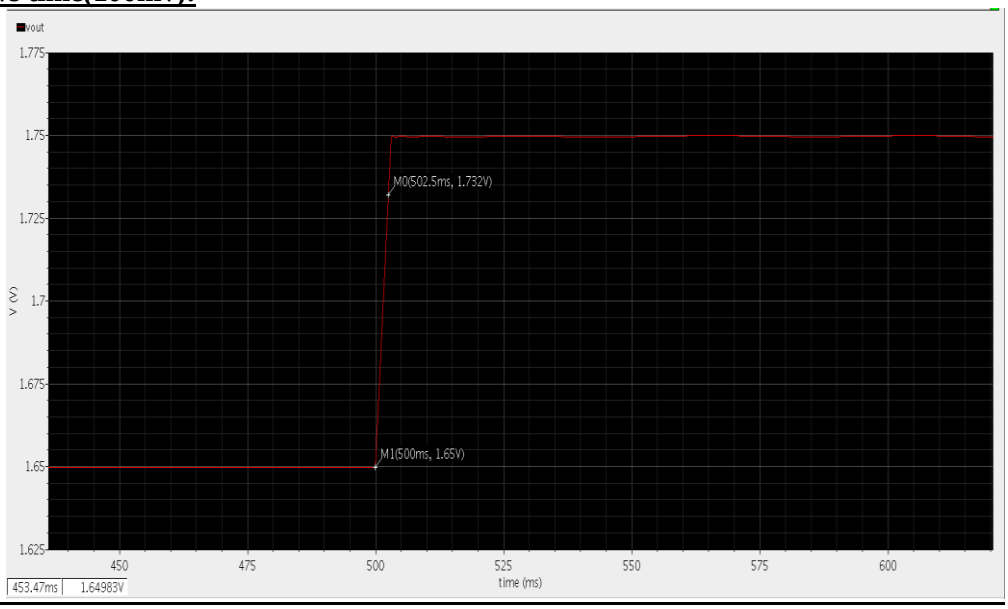
372.0E-3

Comment:

since THD is calculated as percentage,so THD =372E-3 % ,which means the harmonic distortion is very small nearly negligible.

2.2.8. Plot V_{out} for a small step input of 100mV (add proper input DC value). Calculate the fractional gain error (FGE) and 1% settling time (compare with hand analysis).

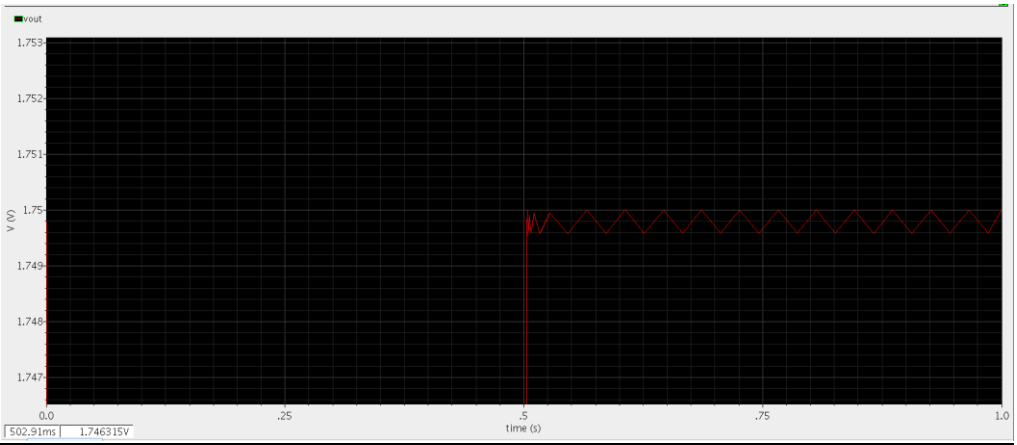
-plot V_{out} vs time(100mv):



Comment:

-from the previous :Ts=502.5-500=2.5msec.

-To calculate it analytically:$Ts = 4/(kGBW)$, since GBW=2*pi*181.8 MHz as it 's shown in ClosedLoop frequency response so Ts=3.5 ns.



Comment:

We can note that the analytical value is very different to the practical value and that's because PM is not very big nearly 66 deg. and that causes ringing as shown in the previous figure , so this suggests that the system is not underdamped and that's why this equation $Ts = 4/(kGBW)$ doesn't hold.

-Calculating FGE:

from the closed loop frequency response $Acl = 0.9998 = -1.503\ mdb$

so $FGE = |ideal\ gain\ -\ actual\ gain|/ideal\ gain = 1 - 0.9998/1 = 200E - 6.$

Analytically: $FGE = 1/kA_o$, since loop gain in buffer=74.34 db, so FGE=192E-6.

So as shown the two values practical and analytical are comparable.