

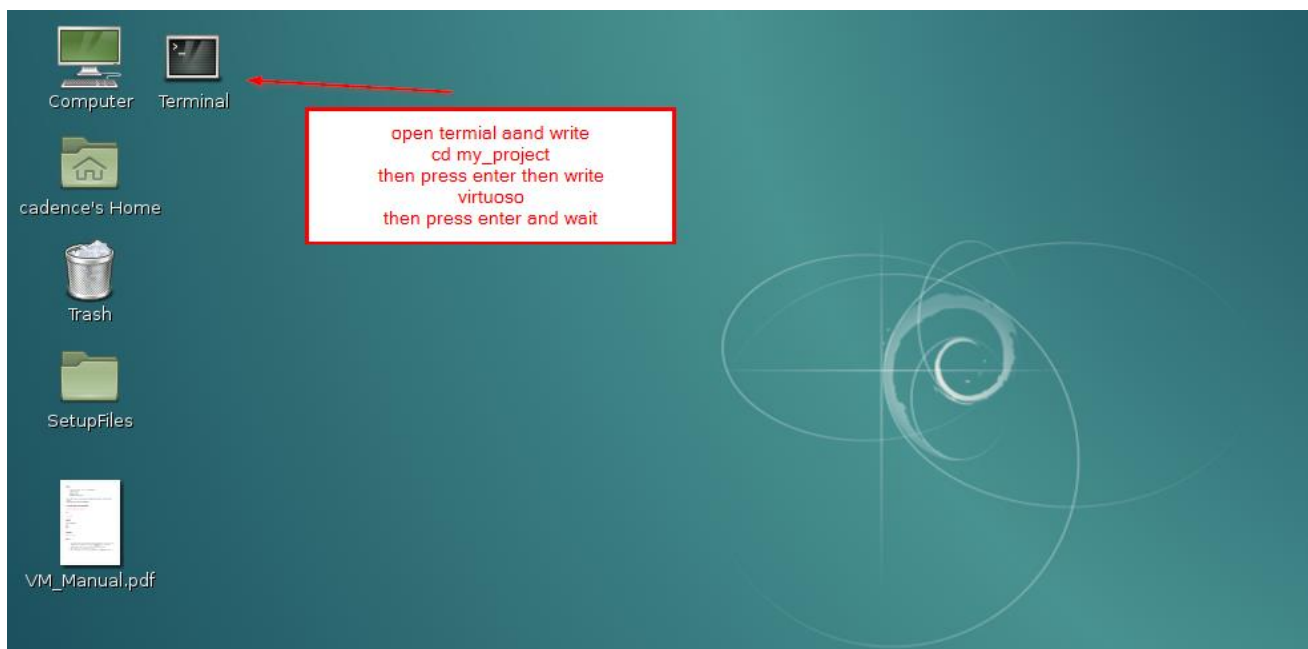
Analog IC Design

Lab 01 – Cadence Tutorial

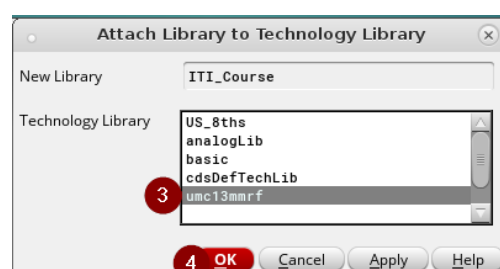
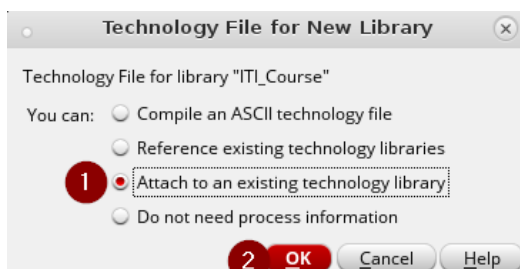
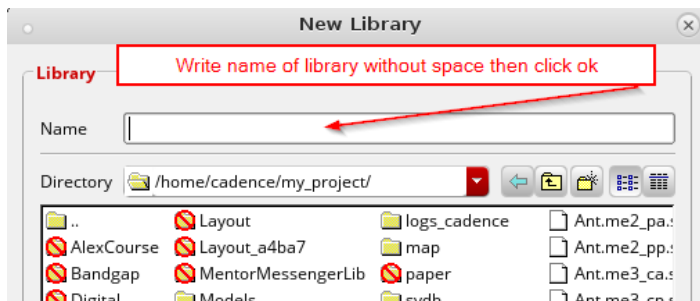
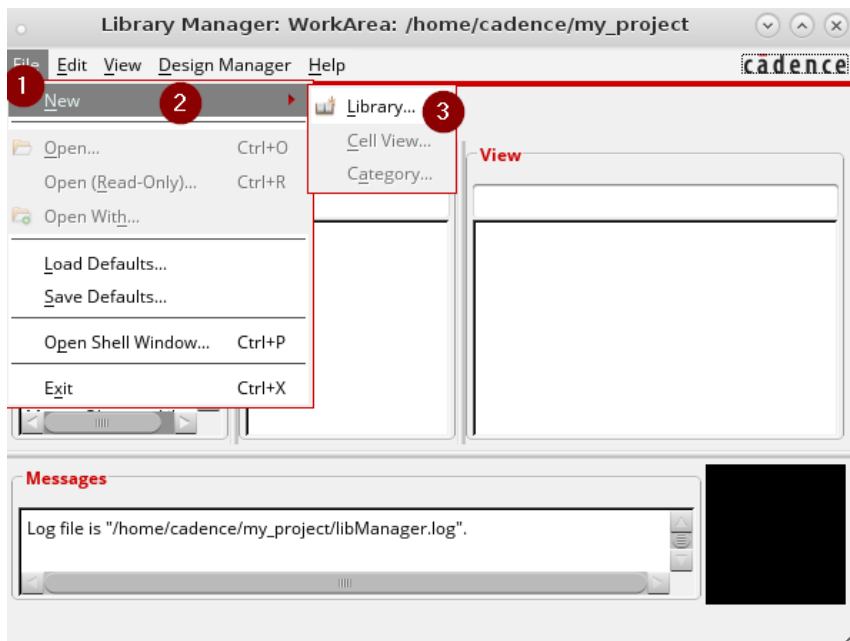
LPF Simulation and MOSFET Characteristics

Part 1: Low Pass Filter Simulation (LPF)

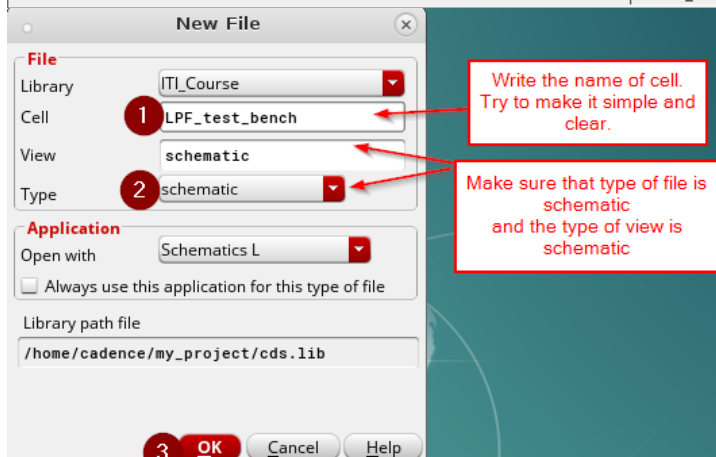
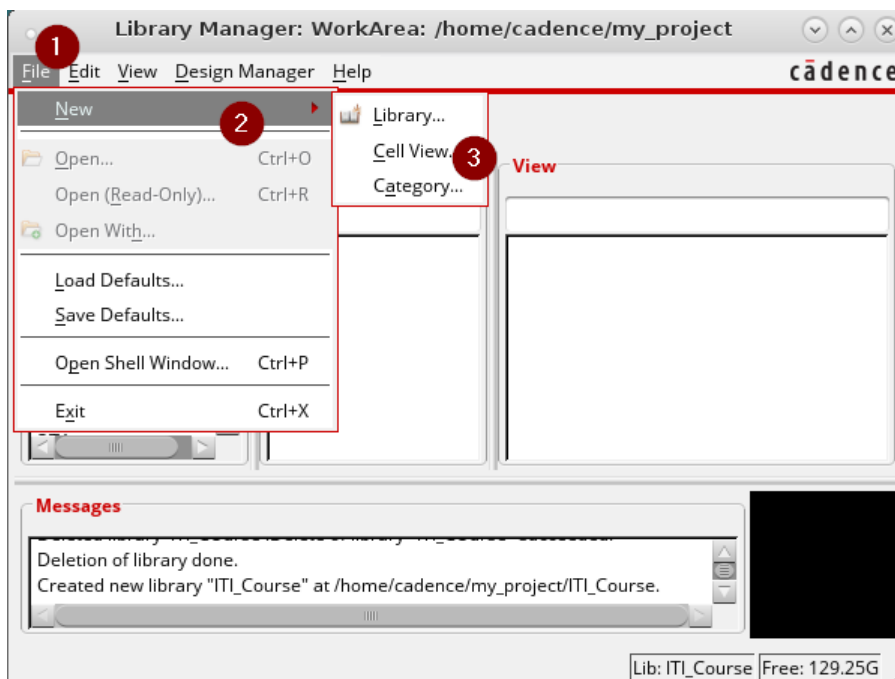
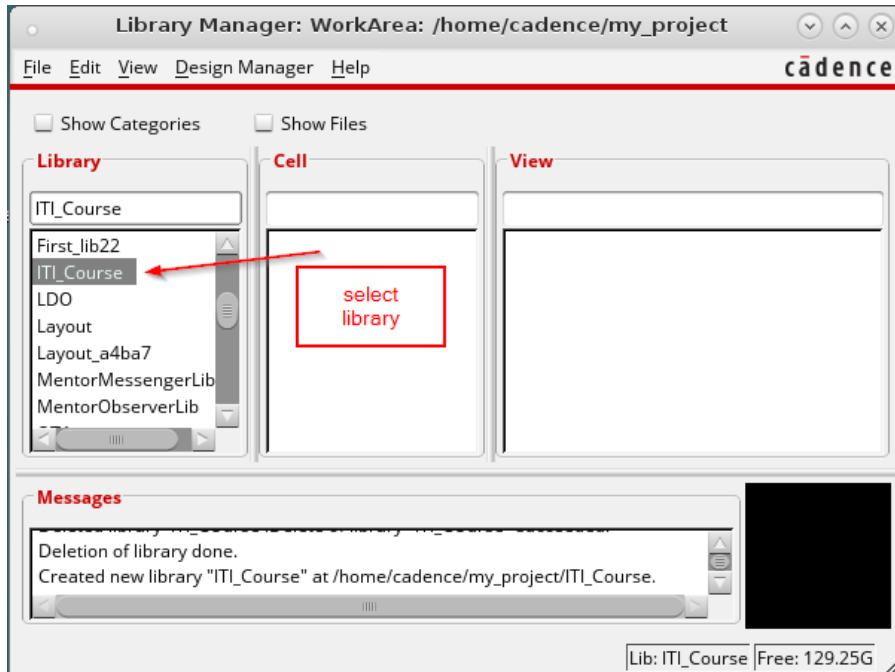
Run the tool from the terminal. Virtuoso and library manager windows will open. If you cannot see library manager window, you can open it from: Tools → Library Manager.



Now we will create a new library.



Now we want to create a new cell to draw the schematic in it.



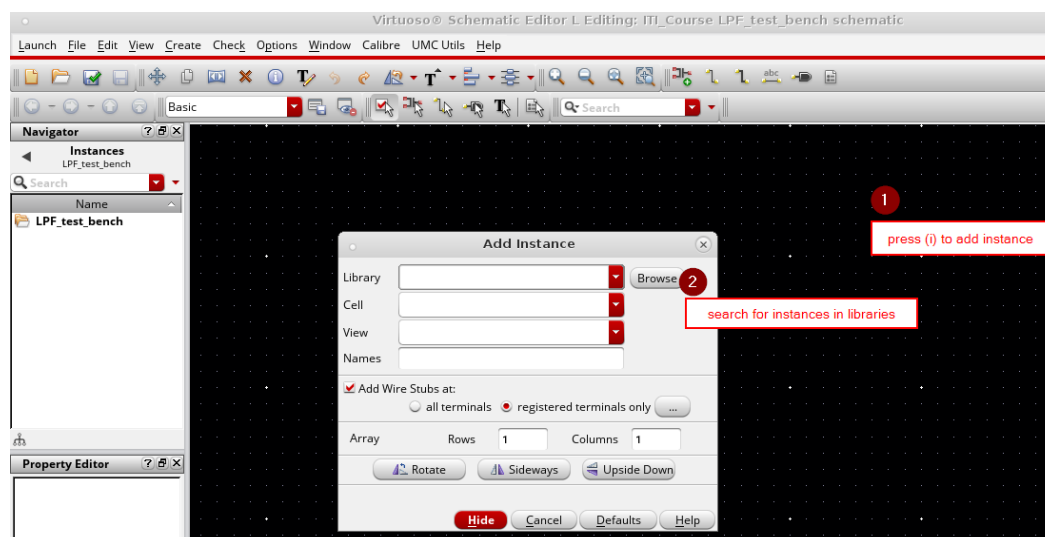
There are some useful shortcuts that will help us during schematic editing.

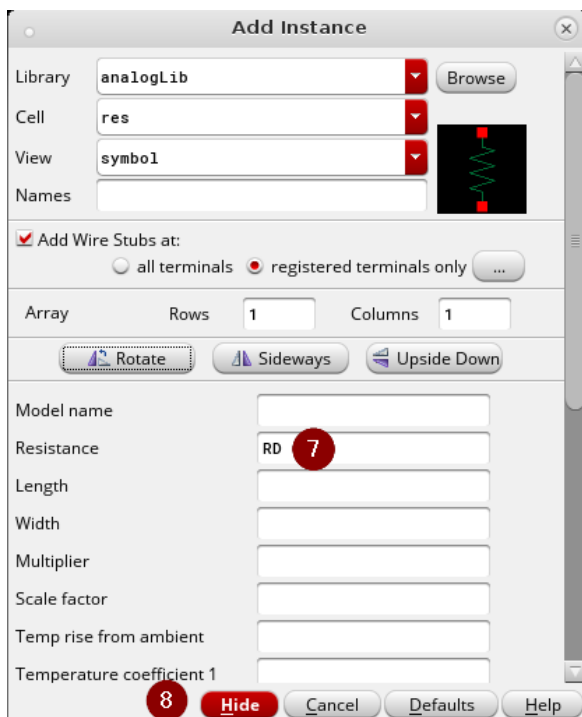
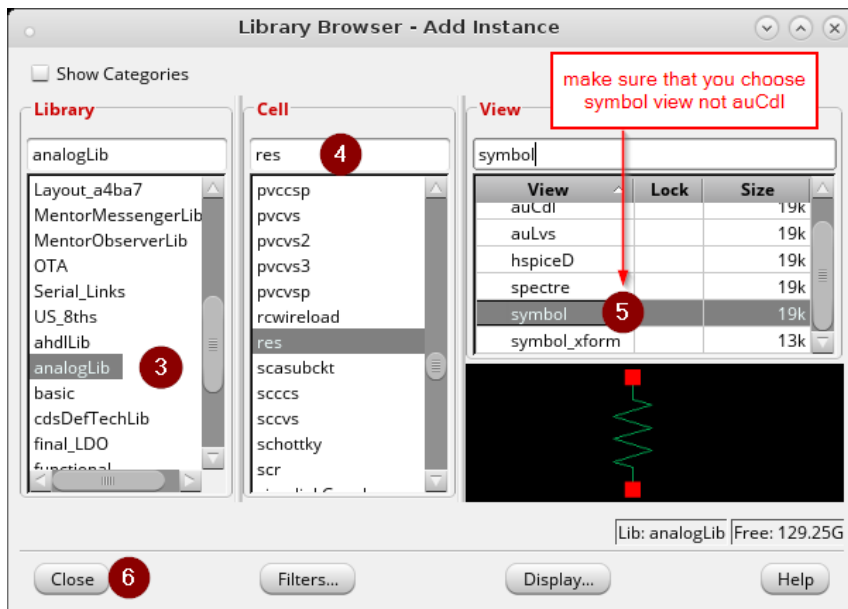
Hotkey	Function
i	Instance
q	Property
w	Wire
m	Move with connections
shift + m	Move without connections
c	Copy
r	Rotate
p	Pin
ctrl + a	Select all
d	Deselect
ctrl + d	Deselect all
u	Undo
shift + u	Redo
f	Fit
z	Zoom in
shift + z	Zoom out
shift + x	Check and Save
ctrl + e	Return (after descending into hierarchy)
l	Label

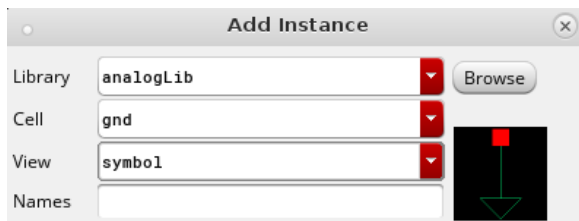
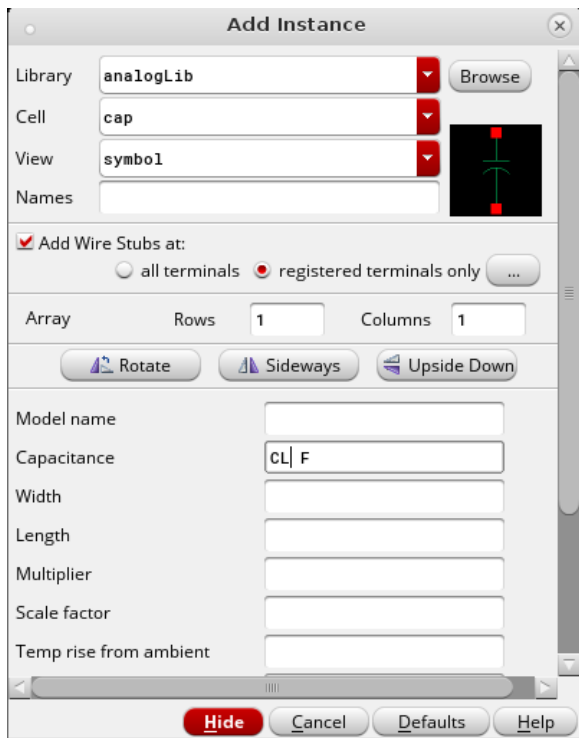
Some additional hotkeys inside the result viewer (VIVA):

m	Add marker
a + b	Add differential marker
c	Trace
s	Add subwindow

1. Transient Analysis







Add Instance

Cell:

View:

Names:

☒ Add Wire Stubs at:
☐ all terminals ☒ registered terminals only ...

Array: Rows Columns

Rotate Sideways Upside Down

DC voltage:

Source type:

Frequency name 1:

Delay time:

Zero value:

One value:

Period of waveform:

Rise time:

Fall time:

Type of rising & falling edge:

Pulse width:

Display small signal params: ☐

Display temperature params: ☐

Display noise parameters: ☐

Multiplier:

Hide Cancel Defaults Help

Create Wire Name

Names:

☐ Expand bus names

☐ Attach to multiple wires

☐ Create net alias labels

☐ Display bundles vertically

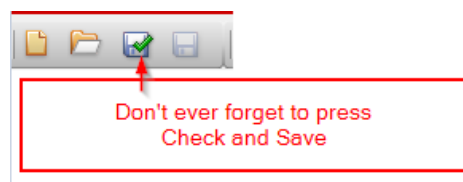
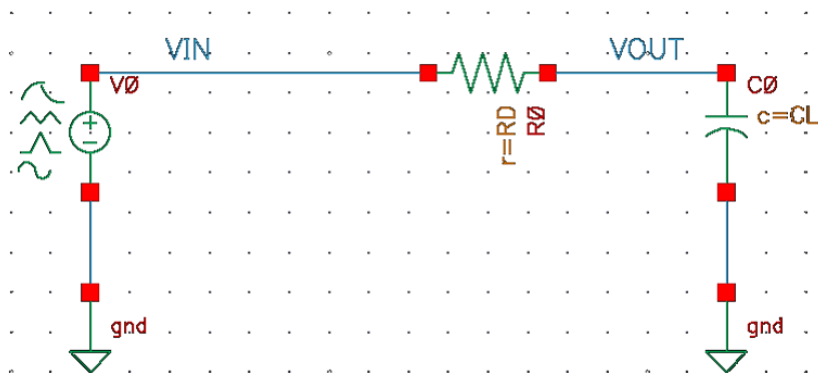
► Font

► Entry Style

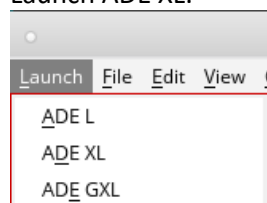
Rotation:

Hide Cancel Defaults Help

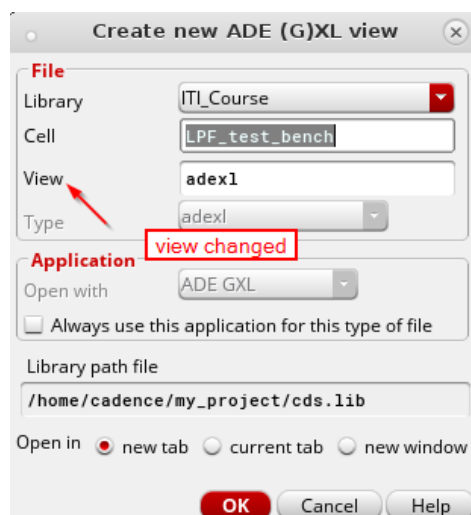
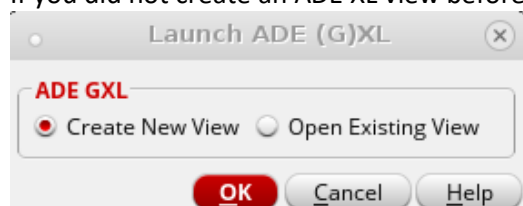
Schematic of LPF

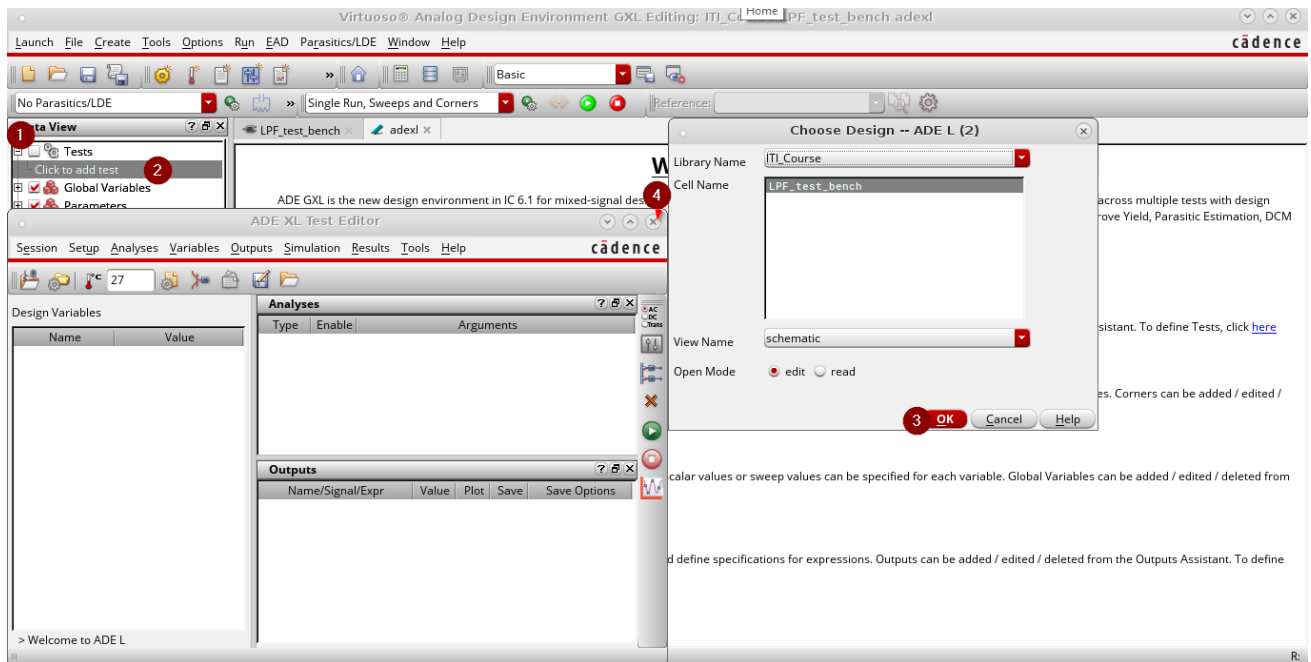


Launch ADE XL.

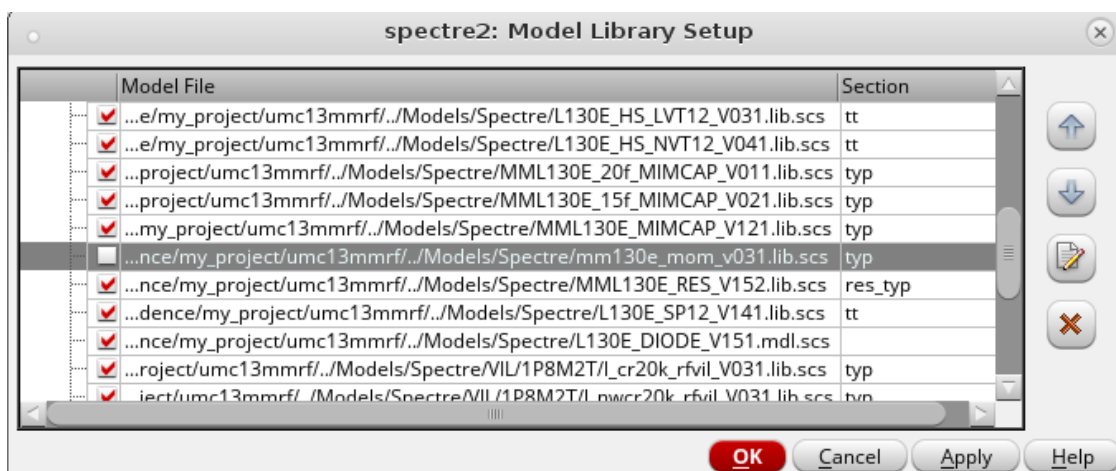
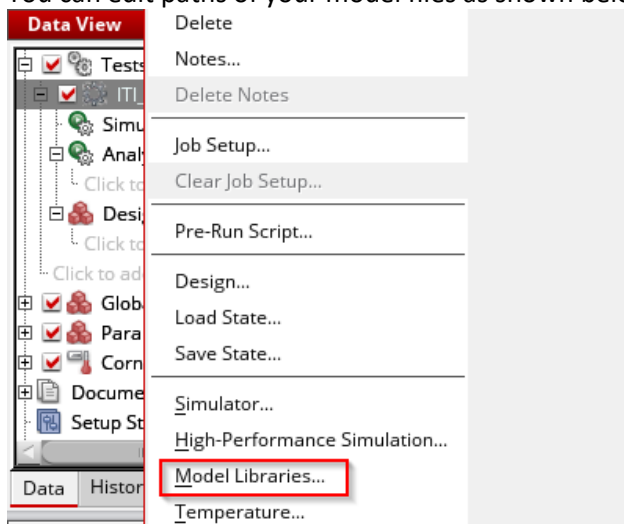


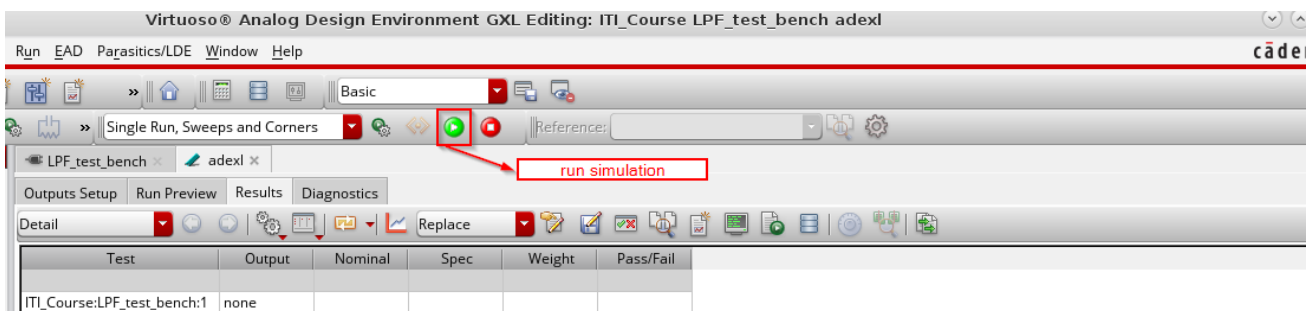
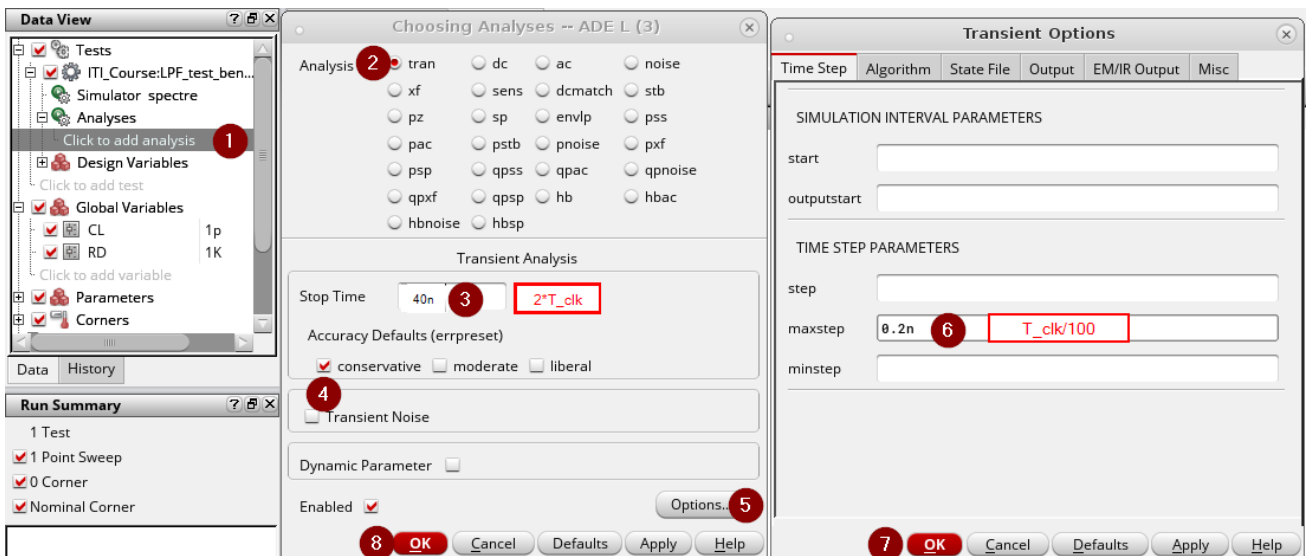
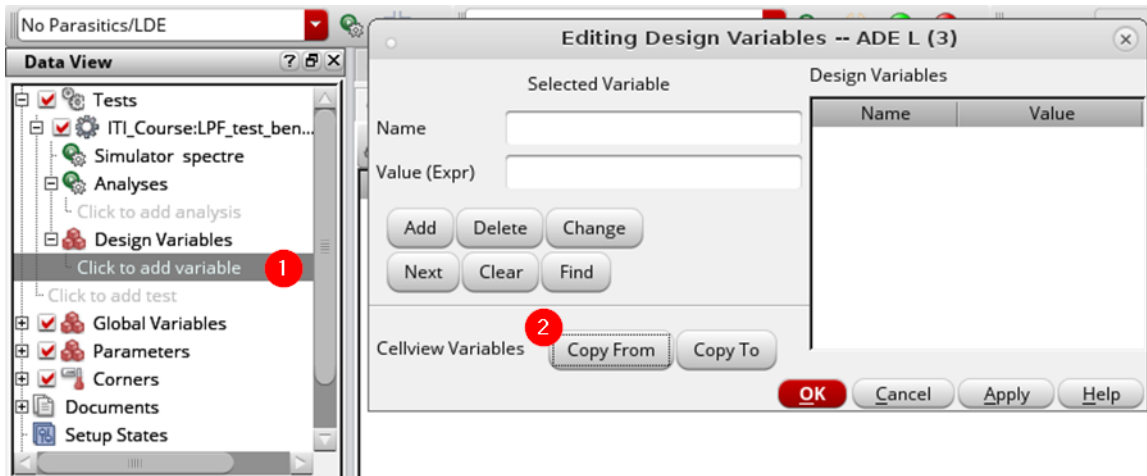
If you did not create an ADE XL view before for this schematic, select "Create New View".



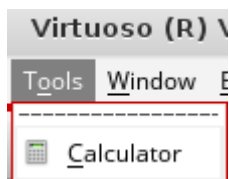
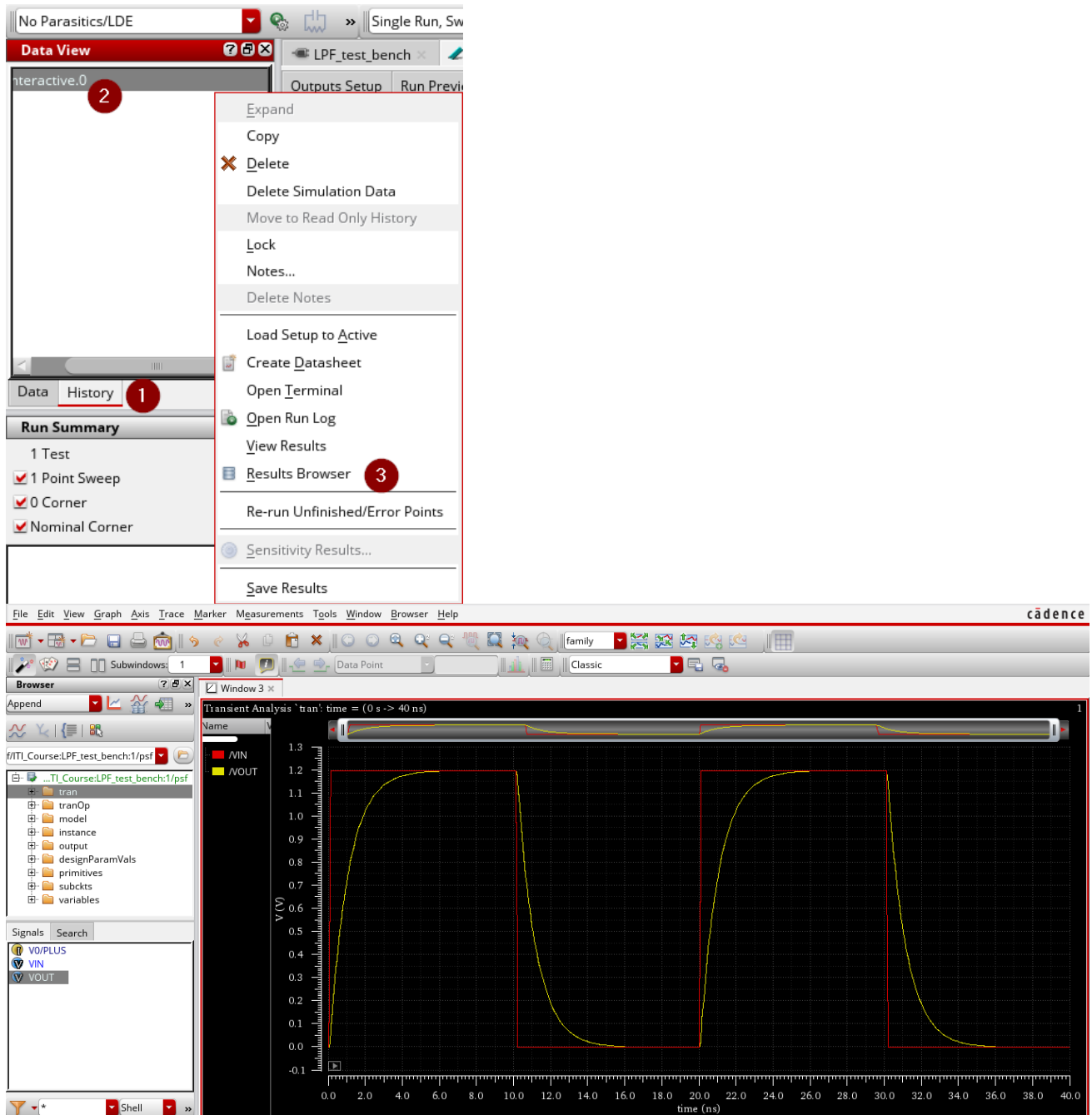


You can edit paths of your model files as shown below. If a specific file is giving you error, you can disable it.





View the results from “Results Browser”. There are several other methods to view the results.



Virtuoso® Analog Design Environment GXL Editing: ITI_Course LPF_test_bench adexl

Launch File Create Tools Options Run EAD Parasitics/LDE Window Help

Basic

No Parasitics/LDE

Single Run, Sweeps and Corners

Reference:

Data View

LPF_test_bench x adexl x

Outputs Setup Run Preview Results Diagnostics

Test	Name	Type	Details	EvalType	Plot	Save	Spec	Weight	Units	Digits	Notation	Suffix
ITI_C...	voutmax	expr	ymin(VT("/VOUT"))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>						
ITI_C...	voutmin	expr	ymin(VT("/VOUT"))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>						

8

9 give an easy name for your expressions

Function Panel

All

cross

Signal VT("/VOUT")

Threshold Value 0.1*voutmax

Edge Number 1

Edge Type rising

Number of occurrences single

Plot/print vs. time

OK Apply Defaults Close Help

Function Panel Stack

Successful evaluation

16 Trace: /VIN (RD=1.00e+03); Context: /home/cadence/simulation/ITI_Course/LPF_test_bench/adexl/results/data/Interactive.0/psf/ITI_Course:LPF_test_bench:1/psf; Dataset: tran-tr

Test	Name	Type	Details	EvalType	Plot	Save	Spec	Weight	Units	Digits	Notation	Suffix
ITI_Course:LPF_test_bench:1	voutmax	expr	ymin(VT("/VOUT"))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>						
ITI_Course:LPF_test_bench:1	voutmin	expr	ymin(VT("/VOUT"))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>						
ITI_Course:LPF_test_bench:1	time10rise	expr	cross(VT("/VOUT") (0.1 * voutmax) 1 "rising" nil nil)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>						
ITI_Course:LPF_test_bench:1	time90rise	expr	cross(VT("/VOUT") (0.9 * voutmax) 1 "rising" nil nil)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>						
ITI_Course:LPF_test_bench:1	rise_time	expr	(time90rise - time10rise)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>						
ITI_Course:LPF_test_bench:1	time90fall	expr	cross(VT("/VOUT") (0.9 * voutmax) 1 "falling" nil nil)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>						
ITI_Course:LPF_test_bench:1	time10fall	expr	cross(VT("/VOUT") (0.1 * voutmax) 1 "falling" nil nil)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>						
ITI_Course:LPF_test_bench:1	fall_time	expr	(time10fall - time90fall)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>						

Data View

Tests

ITI_Course:LPF_test_bench:1

Simulator spectre

Analyses

tran 0 40n conservative

Click to add analysis

Design Variables

Click to add test

Global Variables

CL 1p

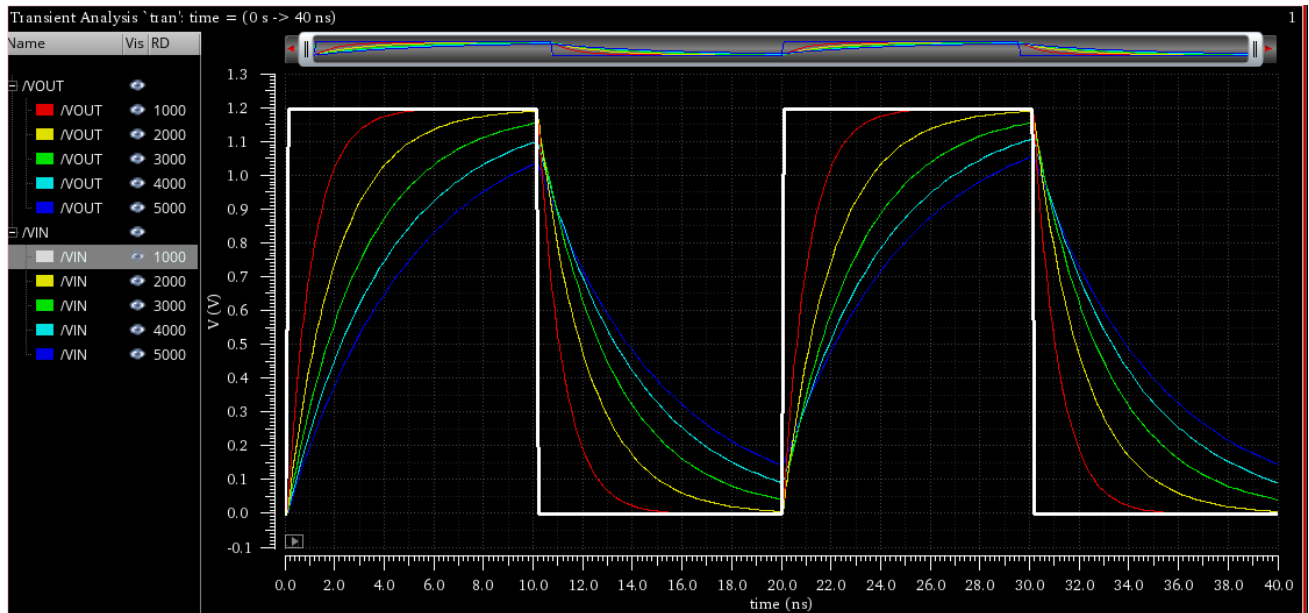
RD 1K:1K:5K

Click to add variable

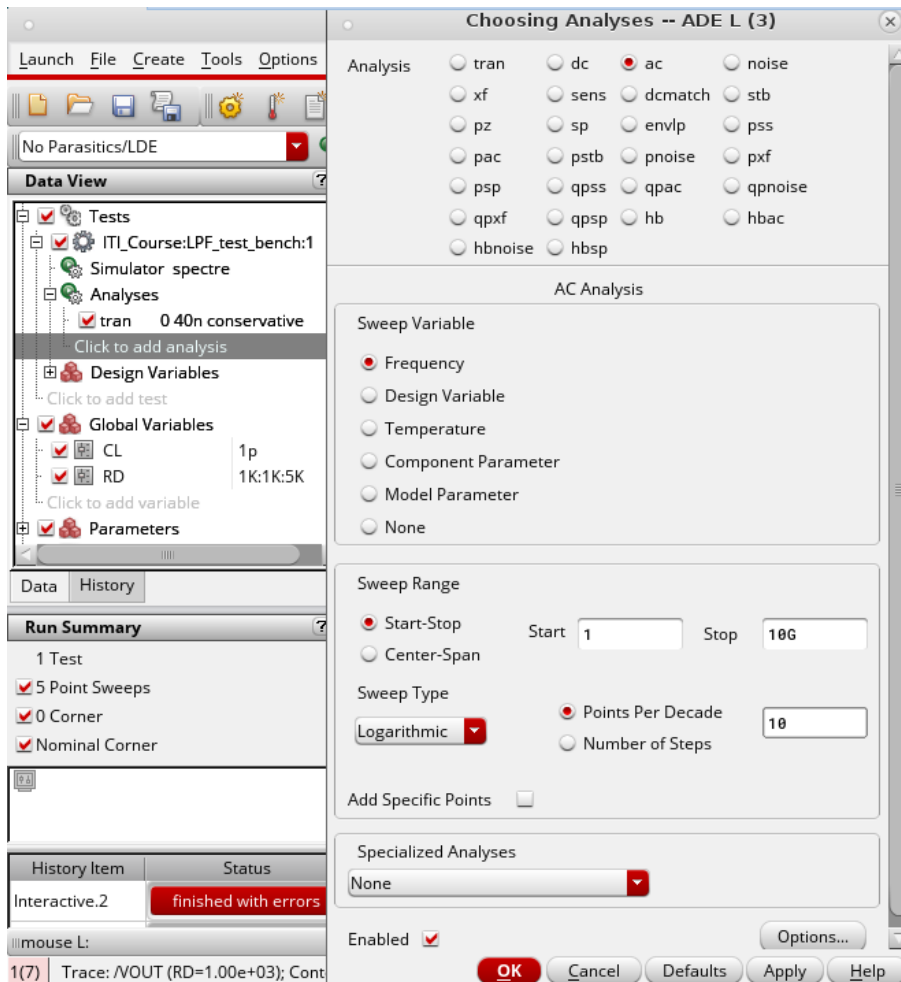
Parameters

parametric sweep

Data History



2. AC Analysis



Basic

No Parasitics/LDE

Single Run, Sweeps and Corners

Reference:

Data View

ITL_Course:LPF_test_bench:1

Simulator spectre

Analyses

tran 0.40n conservative

ac 110G 10 Logarithmic P...

Click to add analysis

Design Variables

Click to add test

Global Variables

CL 1p

RD 1K:1K:5K

Click to add variable

Outputs Setup

Run Preview

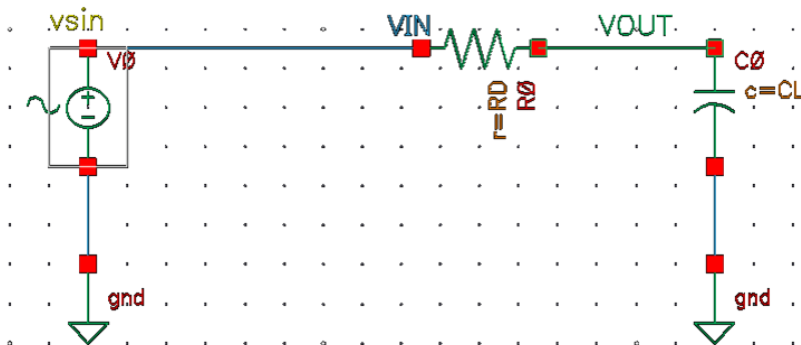
Results

Diagnostics

Test	Name	Type	Details	EvalType	Plot	Save	Spec
ITL_Course:LPF_test_bench:1	voutmax	expr	ymin(VT("/VOUT"))	point	<input type="checkbox"/>	<input type="checkbox"/>	
ITL_Course:LPF_test_bench:1	voutmin	expr	ymin(VT("/VOUT"))	point	<input type="checkbox"/>	<input type="checkbox"/>	
ITL_Course:LPF_test_bench:1	time10rise	expr	cross(VT("/VOUT") (0.1 * voutmax) 1 "rising" nil nil)	point	<input type="checkbox"/>	<input type="checkbox"/>	
ITL_Course:LPF_test_bench:1	time90rise	expr	cross(VT("/VOUT") (0.9 * voutmax) 1 "rising" nil nil)	point	<input type="checkbox"/>	<input type="checkbox"/>	
ITL_Course:LPF_test_bench:1	rise_time	expr	(time90rise - time10rise)	point	<input type="checkbox"/>	<input type="checkbox"/>	
ITL_Course:LPF_test_bench:1	time90fall	expr	cross(VT("/VOUT") (0.9 * voutmax) 1 "falling" nil nil)	point	<input type="checkbox"/>	<input type="checkbox"/>	
ITL_Course:LPF_test_bench:1	time10fall	expr	cross(VT("/VOUT") (0.1 * voutmax) 1 "falling" nil nil)	point	<input type="checkbox"/>	<input type="checkbox"/>	
ITL_Course:LPF_test_bench:1	fall_time	expr	(time10fall - time90fall)	point	<input type="checkbox"/>	<input type="checkbox"/>	

Uncheck tran analysis and outputs

Make sure to replace the vsource with vsin or vdc because vsource doesn't work with AC analysis



cross

Signal dB20(VF("/VOUT"))

Threshold Value DCgain-3

Edge Number 1

Edge Type either

Number of occurrences single

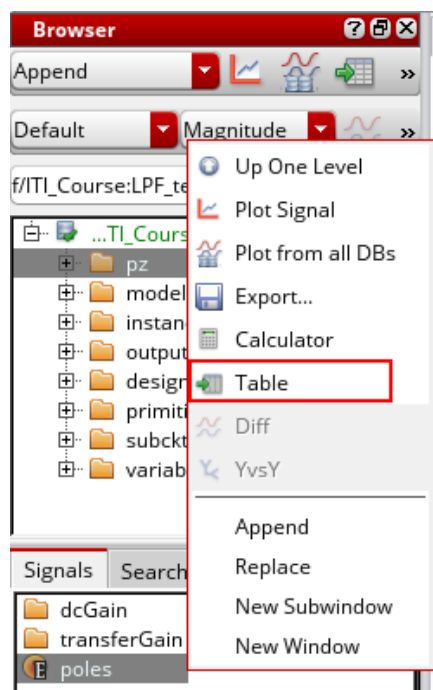
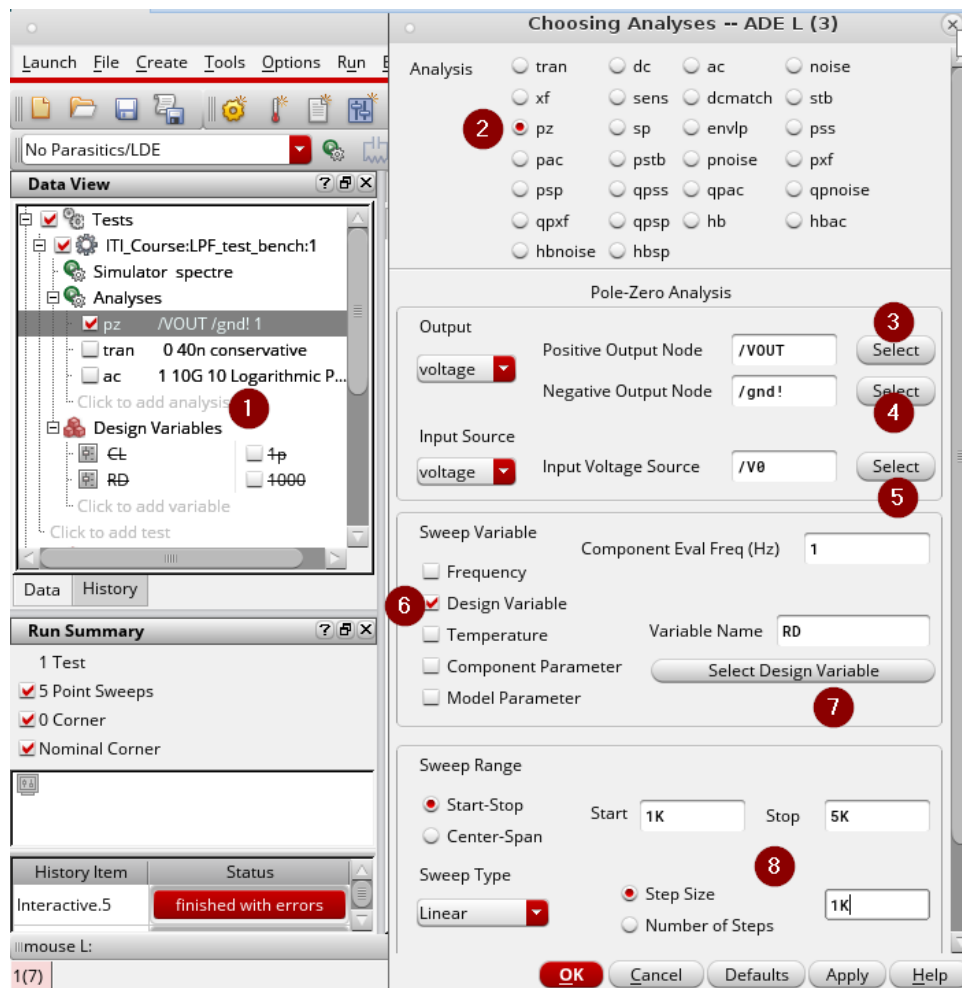
Plot/print vs. time

OK Apply Defaults Close Help

ITL_Course:LPF_test_bench:1		expr	VF("/VOUT")	point	<input type="checkbox"/>	<input type="checkbox"/>
ITL_Course:LPF_test_bench:1		expr	phase(VF("/VOUT"))	point	<input type="checkbox"/>	<input type="checkbox"/>
ITL_Course:LPF_test_bench:1	VoutdB	expr	dB20(mag(v("/VOUT" ?result "ac")))	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>
ITL_Course:LPF_test_bench:1	DCgain	expr	ymin(VoutdB)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>
ITL_Course:LPF_test_bench:1	BW3dB	expr	cross(VoutdB (DCgain - 3) 1 "either" nil nil)	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>

Test	Output	Nominal	Spec	Weight	Pass/Fail
ITL_Course:LPF_test_bench:1	VoutdB				
ITL_Course:LPF_test_bench:1	DCgain	0			
ITL_Course:LPF_test_bench:1	BW3dB	158.8M			

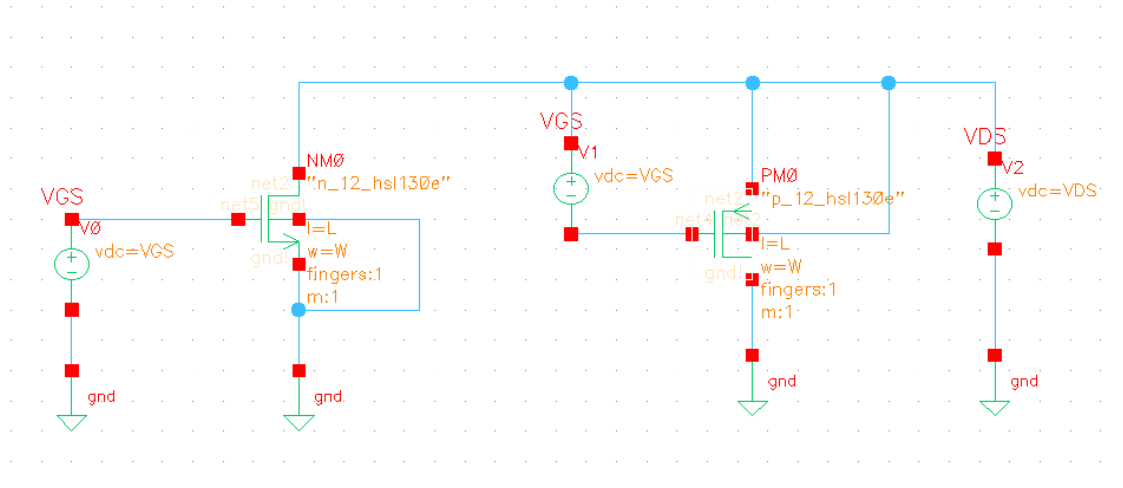
3. Pole Zero Analysis



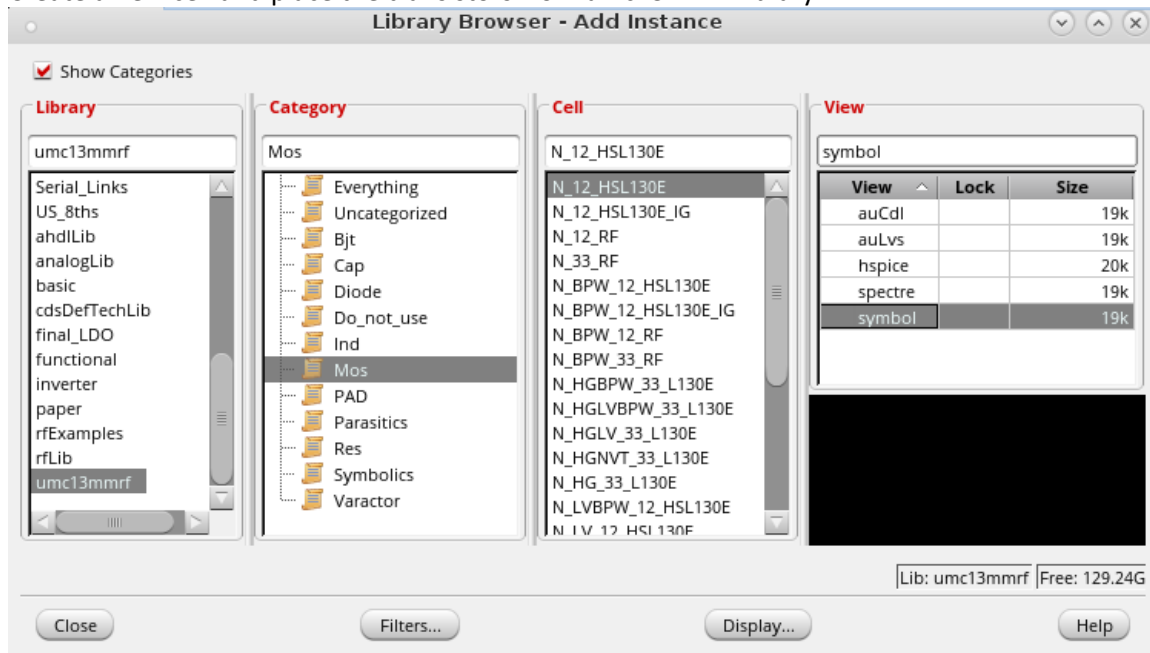
/poles x					
qfactor	/poles ...0 (Hz)	/poles ...0 (Hz)	/poles ...0 (Hz)	/poles ...0 (Hz)	/poles ...0 (Hz)
1 500.0E-3	159.2E6	79.58E6	53.05E6	39.79E6	31.83E6

Part 2: MOSFET Characteristics

Create a testbench for NMOS and PMOS characterization as below.



Create a new cell and place the transistors from umc13mmrf library

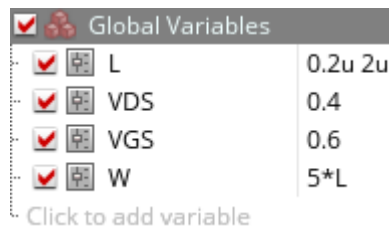


1. ID vs VGS

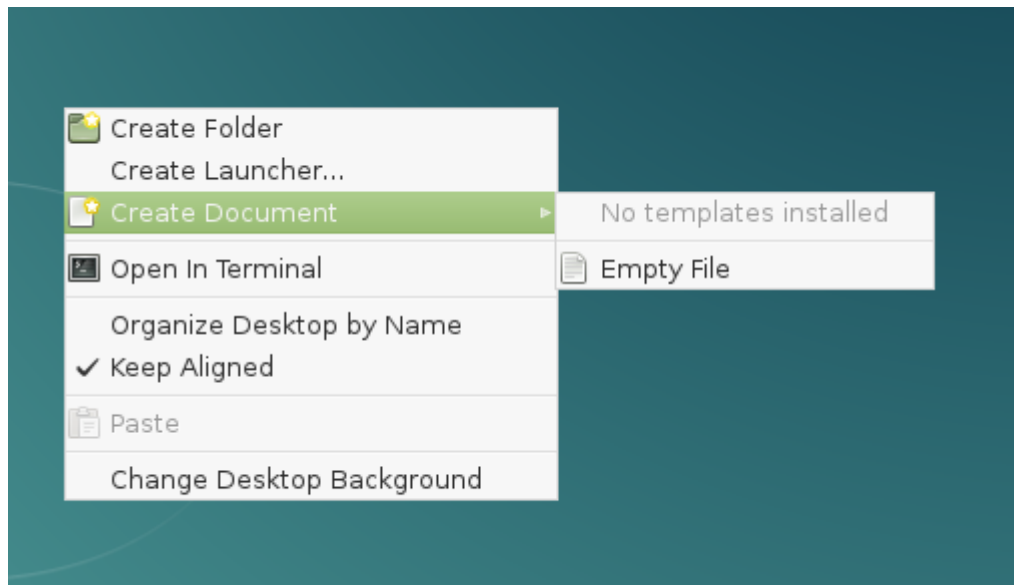
- ➔ Cadence Hint: Use DC sweep instead of parametric sweep whenever possible. DC sweep is extremely faster, and uses much less resources and disk space. In this question you should use DC sweep for VGS.

- ➔ Cadence Hint: To simulate both the short channel and the long channel devices in the same simulation run you can use parametric sweep. Define L as a parameter ($L = 200\text{n}$, 2μ) and define W as a function of L ($W = 5*L$).

First launch adexl and set values of parameters.



Create a new text file



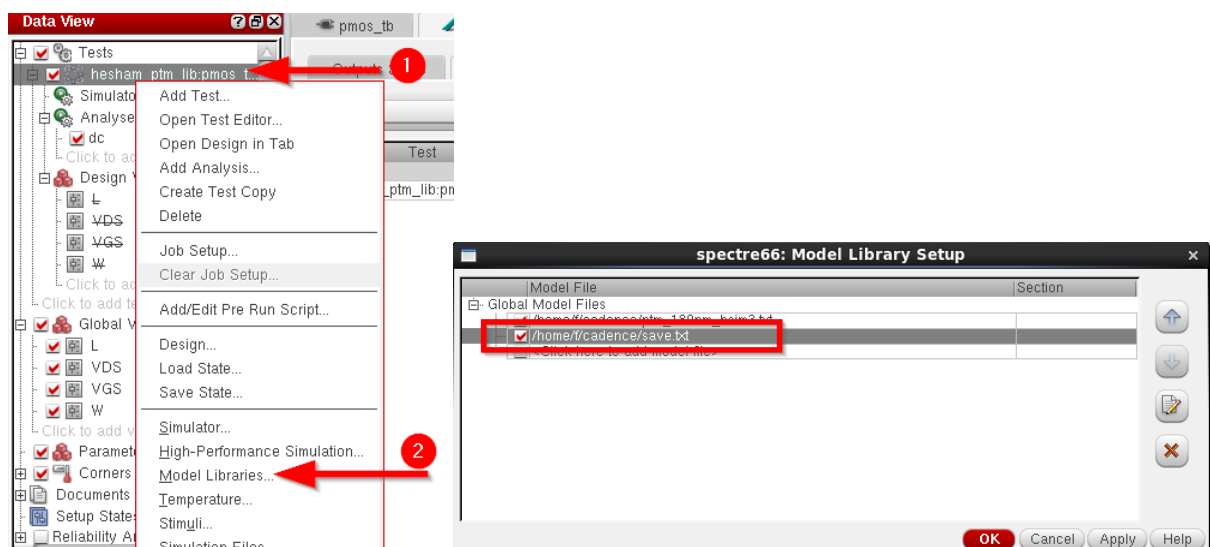
Write these commands in the file

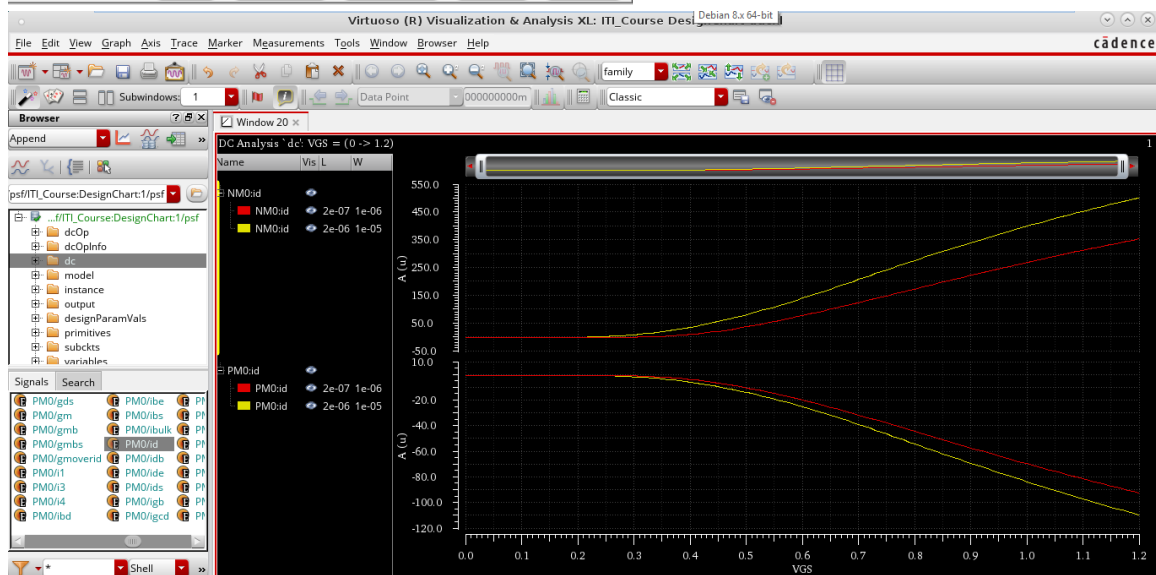
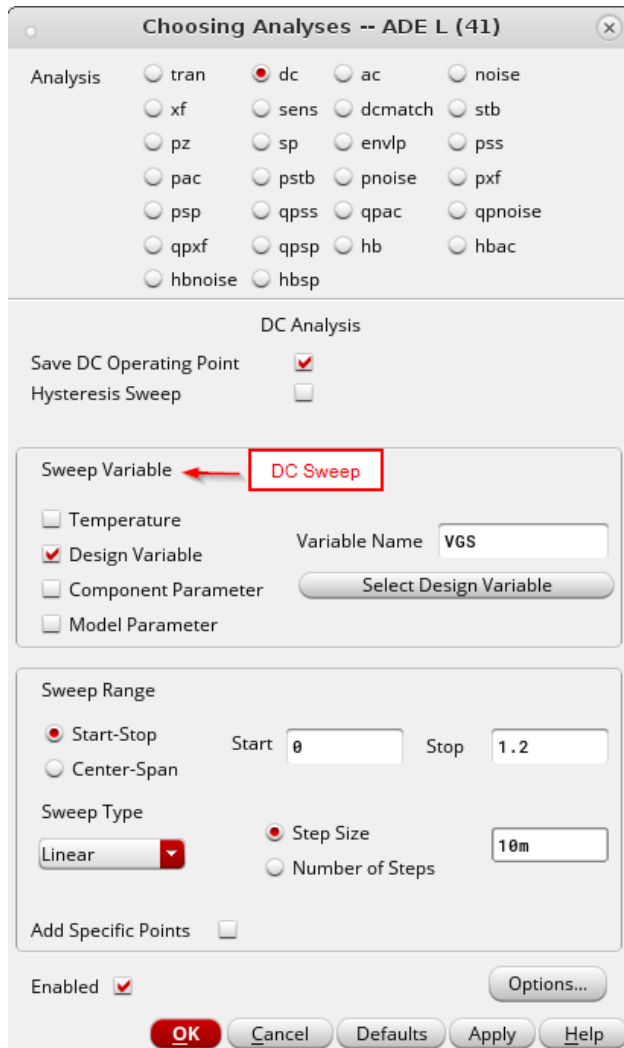
simulator lang = spectre

save *:oppoint sigtype=dev

Save the file and give it a name (e.g., save.txt)

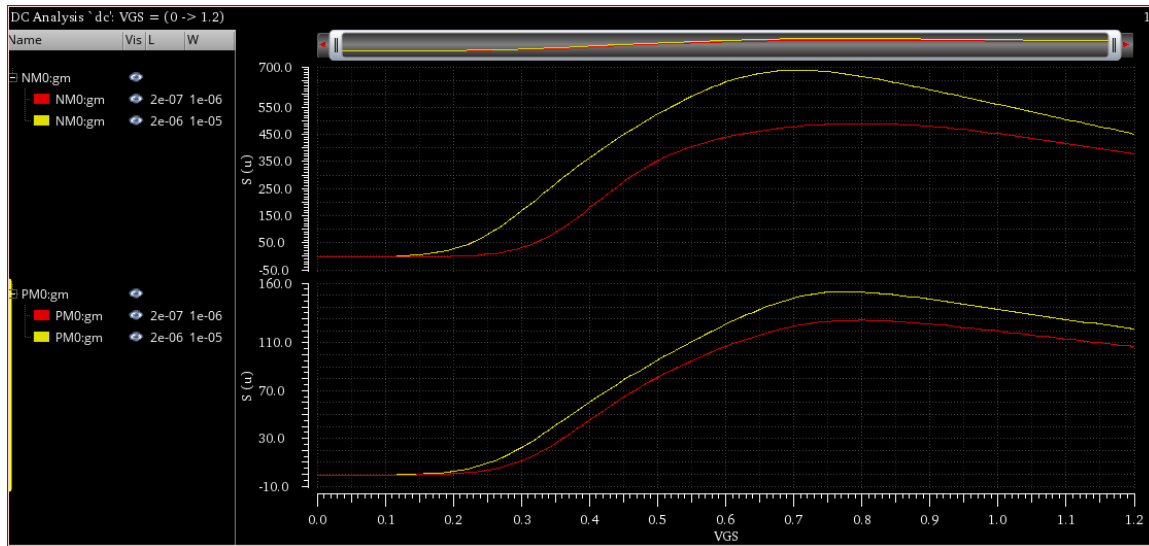
Open Model Libraries and add the file you just created to the libraries.





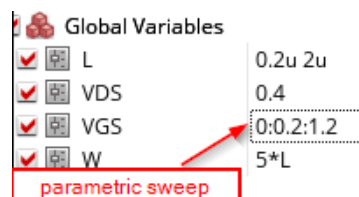
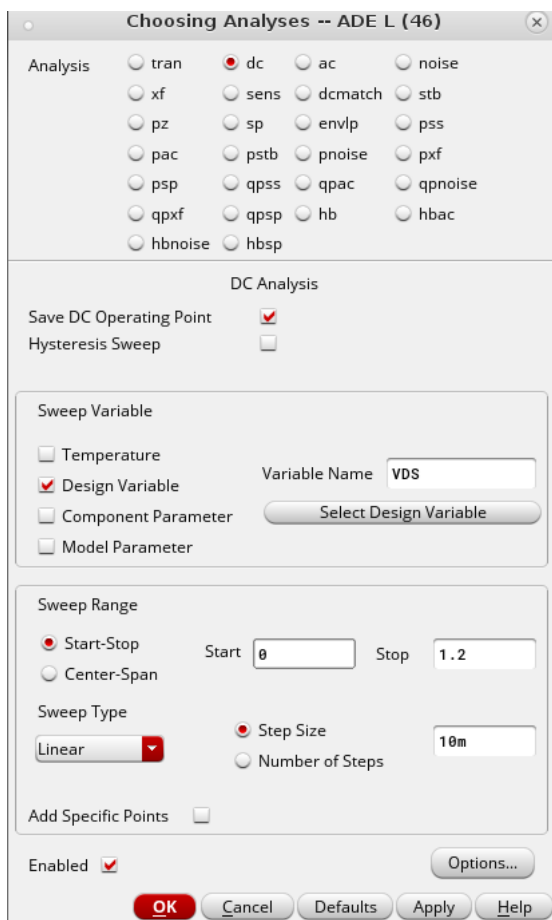
2. g_m vs VGS

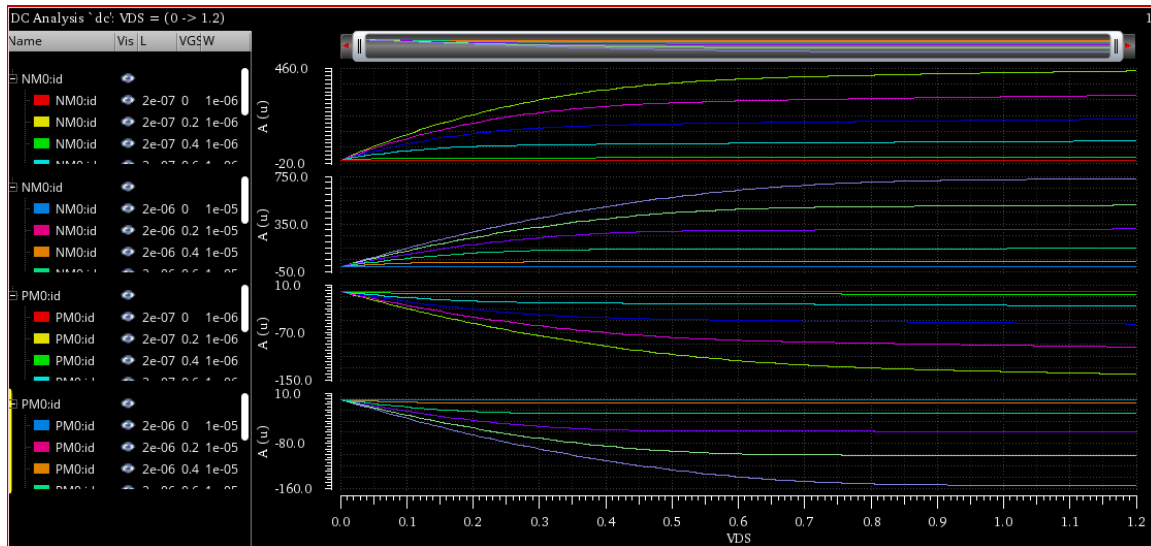
➔ Cadence Hint: In order to save g_m vs DC sweep variable, create an empty text file and write the following statement (without quotes): "save *:gm sigtype=dev". To save all OP point parameters for all transistors use (without quotes): "save *:oppoint sigtype=dev". Add this text file in adexl (Setup -> Model Libraries).



3. ID vs VDS

- ➔ Cadence Hint: In Mentor Eldo and Synopsys HSPICE you can do nested DC sweep (DC sweep with multiple variables) . But in Cadence Virtuoso you can use only one DC sweep variable. Thus, you should use DC sweep for the variable with fine step, i.e., the primary variable (VDS in this case), and parametric sweep for the variable with coarse step, i.e., secondary variable (VGS in this case).





4. g_m and r_o in Triode and Saturation

