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Electronics (Section (5))

٣ج ١٠.

To have analog circuit design
We should know

- Bandwidth (closed loop) → Gain bandwidth (open loop)
- Gain
- Slew rate
- O/p swing (Range of o/ps at which all transistors are still operating in sat.)
  ⇒ linearity
- Noise & offset

* How we calculate these parameters using cadence & what are parameters controlling them?

(a) DC gain / GBW / PSRR / Stability {AC analysis}

DC gain → $g_{m_{i/p}}$, o/p impedance (r_o)

GBW → $g_{m_{i/p}}$ / load capacitance

Stability → poles we see from path from i/p to o/p as well as zeros due to multipath

(b) Stability [open loop + CMFB] {Stb analysis}

We need to have PM > 45° (Min) to have stable system

To get such PM or even PM ≃ 60

⇒ For dominant pole system

$$A(s) = \frac{A_0}{\left(1+\frac{s}{\omega_d}\right)\left(1+\frac{s}{\omega_{p_2}}\right)}$$

dominant pole

We should have $\left[\omega_{p_2} = 2 * GBW\right]$

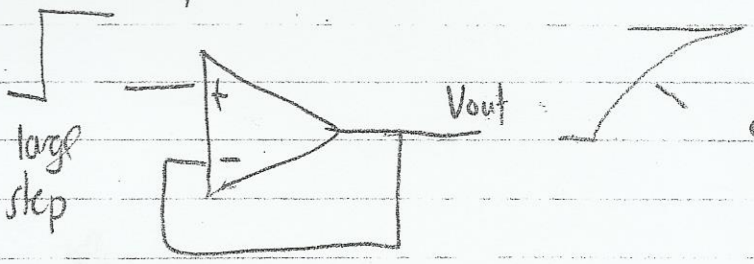
$\left[\omega_{p_2} = 2 * \frac{g_{m\,in}}{C_L}\right]$ to get $(PM = 60^\circ)$

which is my optimum value

(C) Noise {noise analysis}

(d) Slew rate, o/p swing {transient analysis}

↳ to see when clipping occurs to the o/p signal



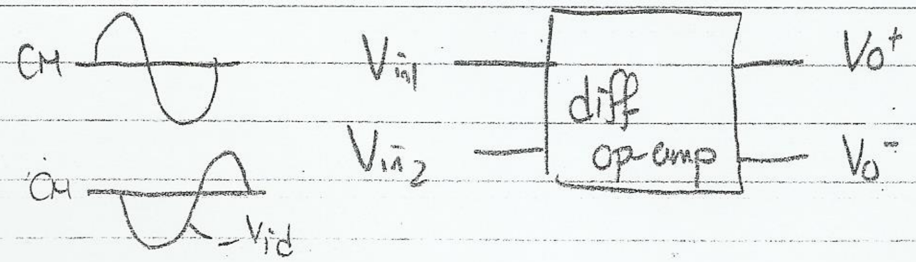
$$\left.\frac{dV_{out}}{dt}\right|_{max} = \text{Slew rate}$$

(e) Offset {Monte carlo simulation}

* If we consider the op-amp as 2 port network, have

$V_i|_{CM}$ ≡ to bias transistors to work properly

$V_i|_{DM}$ ≡ Signal to be amplified (Small signal)



∴ $V_{id} = V_{in1} - V_{in2}$

$V_{iCM} = \dfrac{V_{in1} + V_{in2}}{2}$

∴ $V_{i1} = V_{CM} + \dfrac{V_{id}}{2}$

$V_{i2} = V_{CM} - \dfrac{V_{id}}{2}$

So now, we've for the o/p as well (CM) & diff mode

$$\begin{bmatrix} V_{od} \\ V_{oCM} \end{bmatrix} = \begin{bmatrix} A_{dd} & A_{cd} \\ A_{dc} & A_{cc} \end{bmatrix} \begin{bmatrix} V_{id} \\ V_i|_{CM} \end{bmatrix}$$

∴ $V_{od} = \underbrace{A_{dd}}_{\text{DC gain}} V_{id} + \underbrace{A_{cd}}_{\text{we don't need to have (CM) sig contribution in the diff. o/p}} V_i|_{CM}$

So thats is why we need to see $(CMRR)\Big|_1 = \left|\frac{A_{dd}}{A_{cd}}\right|$ to be as large as possible

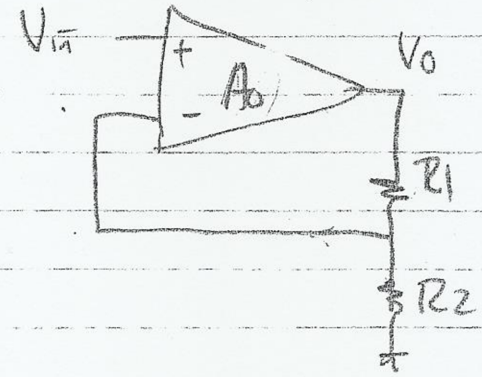
⇒ So first use (I_D) & (V_{CM}) to operate the transistors in saturation,
& after that use small signal i/p to be amplified using DC gain

⇒ What does gain $(A(s))$ & GBW & Slew rate represent ?

(a) Gain $A(s)$ ⟹ Accuracy of op-amp.

for finite gain (A_0)

$\therefore A(s) = A_0$



Ideal gain $= 1 + \frac{R_2}{R_1} = \frac{1}{\beta}$

$\left[\beta = \frac{R_2}{R_1 + R_2}\right] \Rightarrow$

Real - gain $= \frac{A_0}{1 + A_0\beta} = \frac{1}{\frac{1}{A_0} + \beta} = \frac{1}{\beta\left(1 + \frac{1}{A_0\beta}\right)}$

$$= \frac{1}{\beta(1+\frac{1}{A_0\beta})}$$ using binomial theorem

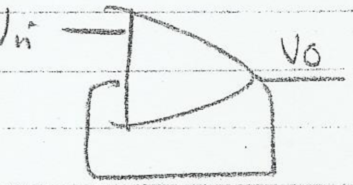
$$= \frac{1}{\beta}\left(1-\frac{1}{A_0\beta}\right)$$

$\therefore$ Gain error $= \frac{1}{A_0\beta}$

So if it's required to be 0.1 %

for best (β) case $=1$

buffer connected



$(\beta = 1)$

$\therefore$ $A_0 = 1000 = 60\,dB$

So it decides the gain error (Accuracy of syst

(b) Gain-bandwidth (GBW)

$= \text{Gain} * BW$

For single pole op-amp. $BW = \omega_0 = \frac{1}{R_{out} * C_L}$

dominant pole —— ω_0

$\therefore \; GBW = G_m * R_{out} * \frac{1}{R_{out} * C_L} = A_o \omega_d$

$$GBW = \frac{G_m}{C_L} = \frac{g_m|_{i/p}}{C_L}$$

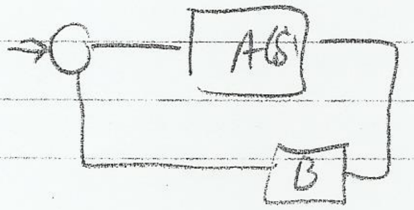
it represents speed of of the op-amp

Why ? for single pole op-amp

$$A(s) = \frac{A_o}{1 + \frac{s}{\omega_d}} \qquad \omega_d = \frac{1}{R_{out} * C_L}.$$

$$A(s) \cong \frac{A_o \omega_d}{s} = \frac{GBW}{s}$$

for the same config



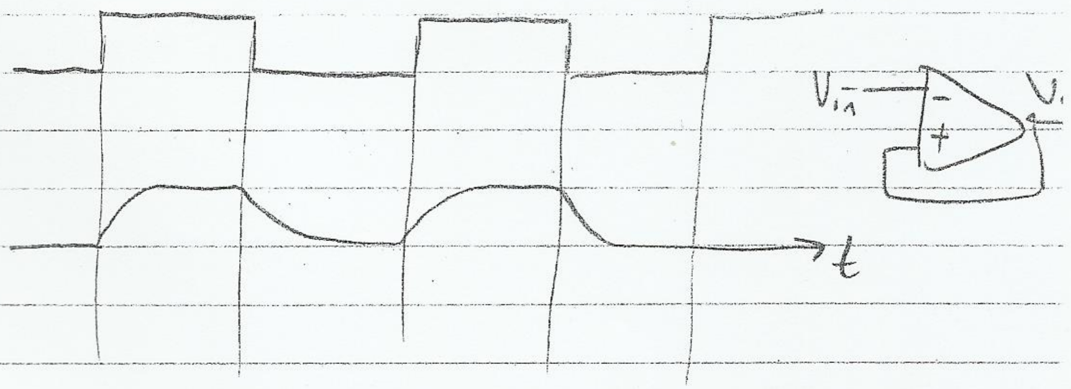
$$\frac{V_o}{V_{in}}(s) = \frac{A(s)}{1 + A(s)\beta}$$

$$\frac{V_o}{V_{in}}(s) = \frac{GBW}{s + GBW * \beta} \qquad \{\mathcal{L}^{-1}\}$$

$$\frac{V_o}{V_{in}}(t) = \left(1 - e^{-t/\tau}\right)$$

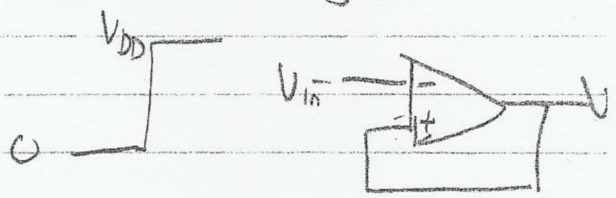
$$\boxed{\tau = \frac{1}{\beta * GBW}}$$

So that if small clk i/p.



So that's why (GBW) represent speed of my system
It decides the speed at which the o/p will respond to the input

(c) Slew rate
Instead of applying small clock i/p
apply Large unit step [0 - V_{DD}]



Slew rate represents

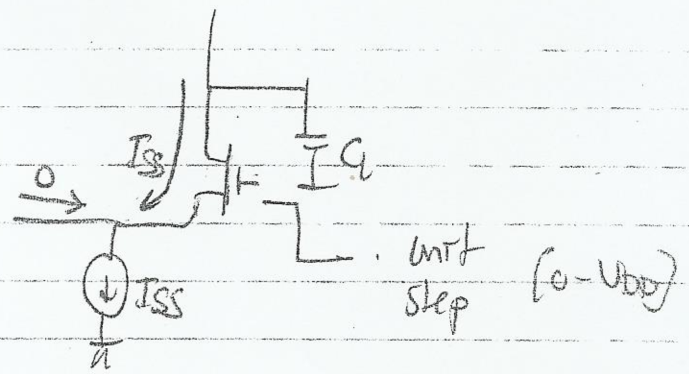
$$\left.\frac{dV_{out}}{dt}\right|_{max} = \text{Slew rate} = \frac{I_{SS}}{C_L}$$

as it will steer all the current in one branch

& that current would charge the capacitor of the load

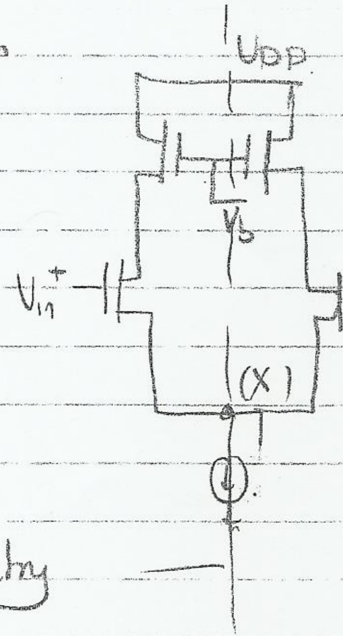
$\therefore I = C \frac{dV_{out}}{dt}$

$\therefore \left.\frac{dV_{out}}{dt}\right|_{max} = \frac{I_{SS}}{C_L}$



* Fully differential Vs. Single ended

$\Rightarrow$ for fully diff. configuration

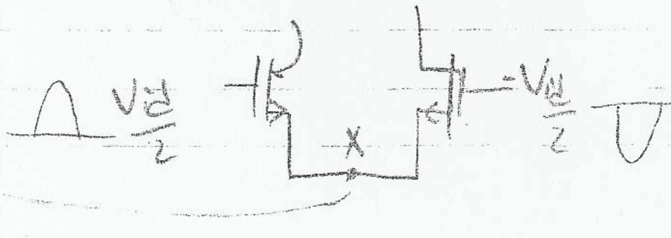


When we solve for

(a) Differential inputs ($\frac{V_{id}}{2}$, $\frac{-V_{id}}{2}$)

We've node (X) as virtual gnd

it's source follower node so it's virtual ground



So that all points on line of symmetry are virtual gnd {for AC analysis}

(b) Common mode input

Now line of symmetry, will divide resistances (seen at node X) into (2) parallel resistances

& the points on line of symmetry are open circuits

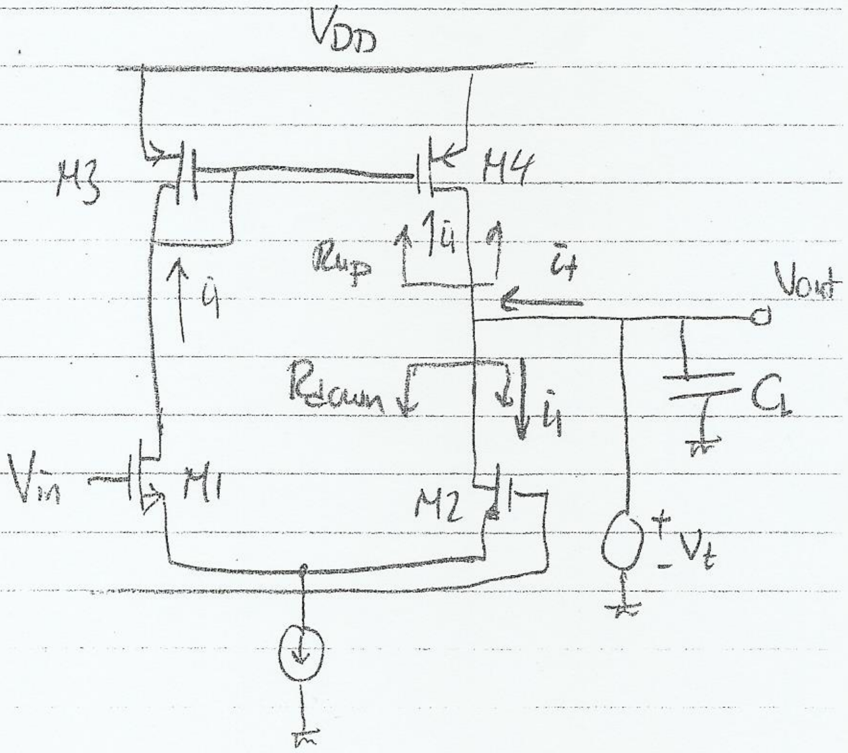
⇒ For single ended
No half model can be used

So we must solve for the whole circuit

To find

R_{out} =

from the basic principles



$$i_t = \frac{V_t}{r_{o4}} + i_1 + i_1$$ (KCL at o/p node)

$\therefore R_{out} = r_{op} \parallel \frac{R_{down}}{2}$

$R_{down} = r_{on} (1 + g_m R_{S_2})$

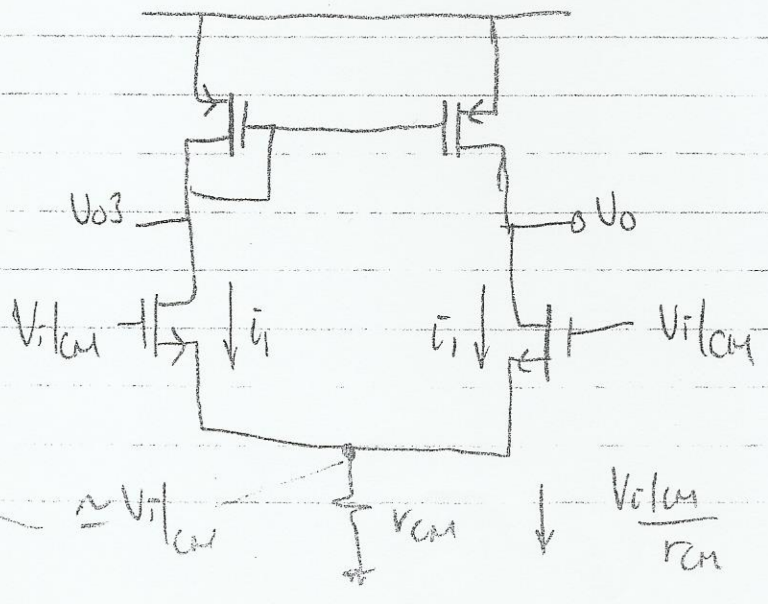
$R_{S_2} \simeq \frac{1}{g_{m_1}}$

$R_{down} = r_{on} \left(1 + g_{m_2}/g_{m_1}\right) \simeq 2 r_{on}$

$\therefore R_{out} = r_{op} \parallel \frac{2 r_{on}}{2} \approx r_{op} \parallel r_{on}$

$\therefore A_{diff} = g_m (r_{op} \parallel r_{on})$

$\Rightarrow$ What about calculating A_{dc} for the same circuit ?



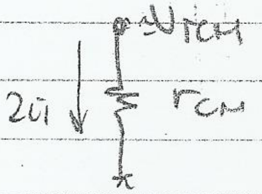
Source follower

From symmetry $V_{o3} \simeq V_o|_{CM}$

$V_{o3} = i_1 * R_{out}|_{V_{o3}}$ $\quad R_{out} = \frac{1}{g_{mp}}$

$= \frac{-i_1}{g_{mp}}$

$i_1 = \frac{V_{ICM}}{2 r_{CM}}$



$V_o|_3 = \frac{V_I|_{CM}}{2 r_{CM} g_{mp}} = V_o|_{CM}$

$\therefore CM|_{gain} = \frac{1}{2 r_{CM} g_{mp}}$

$* \; CMRR = \left| \frac{A_{diff}}{A_{CM}} \right| = g_{mn} (r_{on} // r_{op}) (2 r_{CM} g_m$

⇒ How to get conditions on biasing voltages in fully differential configuration?

* Put one condition on transistor to be in saturation

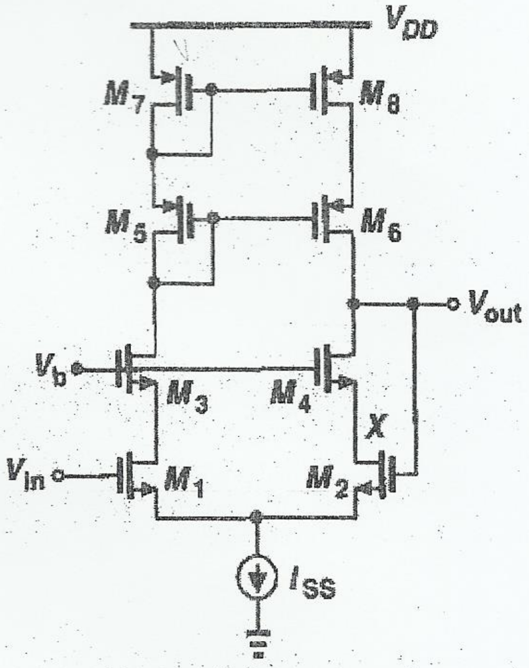
$V_{GD} < V_{th}$

(That will get upper bound in NMOS & lower bound in PMOS)

* To move from (V_b) to the gnd direction & get conditions to be on sat. $(V_{DS} = V_{eff})$ & $(V_{GS} = V_{eff} + V_{th})$

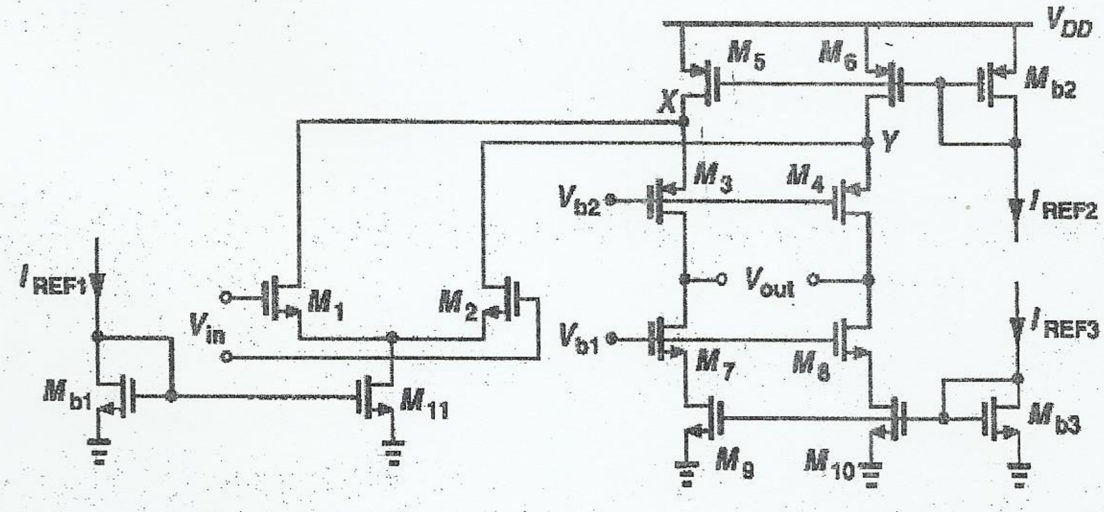
Problem Set II

Problem (1)



For the previous circuit, find the region of operation of each transistor while varying the input V_{in} from 0 to V_{DD}. Find the output range for proper operation (V_{out} tracks V_{in}).

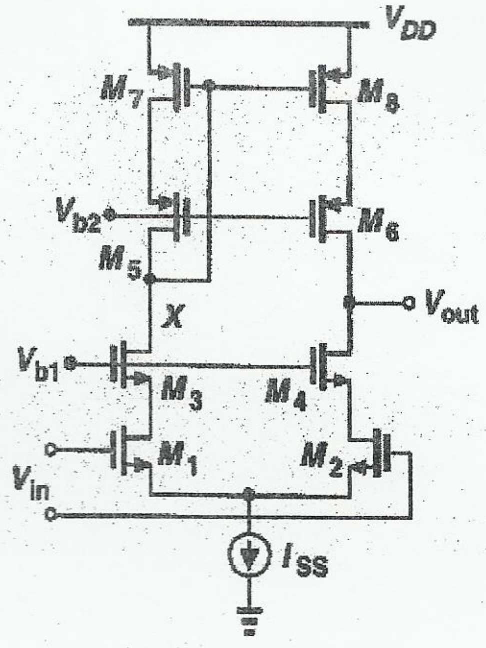
Problem (2)

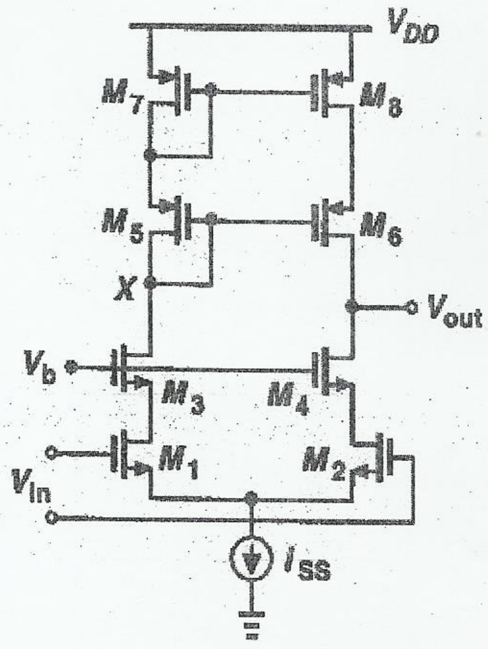


For the previous circuit:

1- Find the relation between I_{REF1}, I_{REF2} and I_{REF3}.
2- Assume output load capacitance C_L at V_{out}, find the exact expression of the Gain-Bandwidth product (GBW) in terms of the circuit parameters.
3- Find the maximum output range as a function of V_{b1} and V_{b2}.
4- Find the values of V_{b1} and V_{b2} for maximum output swing.

Problem (3)

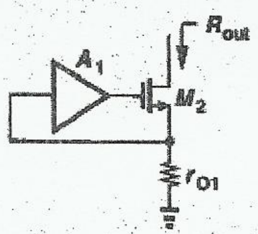


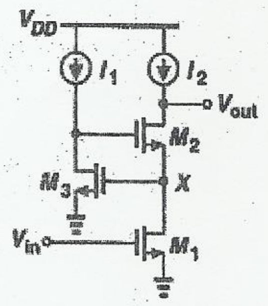


Compare between the two circuits in terms of:

1- DC-gain
2- GBW (assume a load capacitance C_L)
3- Maximum available output swing.

Problem (3)



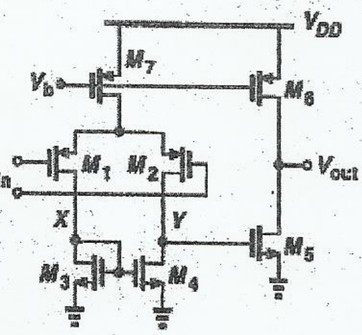


Find the Rout of the first circuit and hence find the G_m and A_v of the second circuit.

Problem (4)

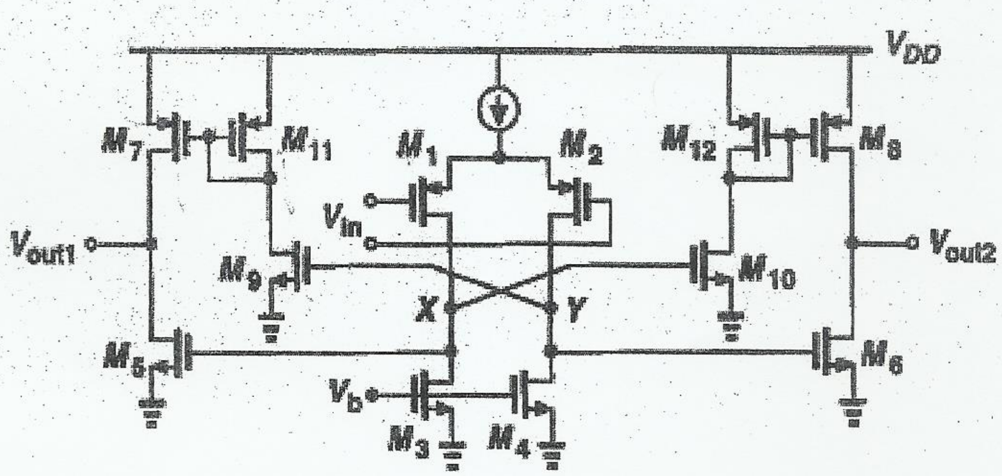
For the two-stage opamp below, V_{DD} = 2.5V, μ_nC_{ox}=100μA/V , , μ_pC_{ox}=50μA/V and for a total power consumption of 6mW, find the maximum GBW for a load capacitance of C_L = 1pF and such that the non-dominant pole is double the GBW product. For this value, find the DC-gain and the maximum output swing.

Assume: V_{OD5}=V_{OD6} and V_{OD1}=V_{OD3}



Problem (5)

Find the DC-gain of the following opamp circuit.



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Section

Electronics

Sheet [2]

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الكترونيك

م/ آحمد عيسى

٣/١٢٥

Problem (1)

For M_1

$$\boxed{V_{in} > V_{eff_1} + V_{th_1} + V_{eff_{ss}}}$$

$$V_{GD_1} < V_{th_1}$$

$$V_{in} - (V_b - V_{eff_3} - V_{th_3}) < V_{th_1}$$

$$\boxed{V_{in} < V_b - V_{eff_3} + V_{th_1} - V_{th_3}}$$

for M_3

$$V_{GD_3} < V_{th_3}$$

$$\boxed{V_b < V_{th_3} + V_{DD} - \left[V_{eff_7} + |V_{th_7}| + V_{eff_5} + |V_{th_5}|\right]}$$

for M_2

$$V_{GD_2} < V_{th_2}$$

$$\boxed{V_{out} < V_{th_2} + V_b - (V_{eff_4} + V_{th_4})}$$

for M_4

$$V_{GD_4} < V_{th_4}$$

$$V_b - V_{out} < V_{th_4}$$

$$-V_{out} < V_{th4} - V_b$$

$$\boxed{V_{out} > V_b - V_{th_4}} \Rightarrow \boxed{V_{out} > (V_{in} - V_{eff_3} + V_{th} - V_{th4}}$$

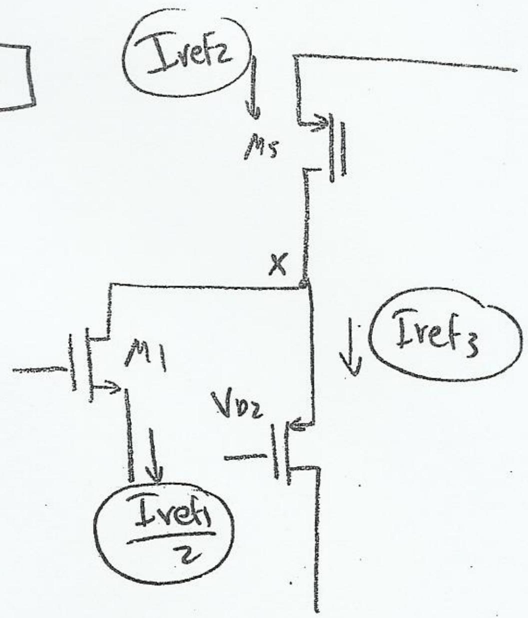
for M_6

$$V_{DG_6} < |V_{th_6}|$$

$$\boxed{V_{out} < V_{DD} - [V_{eff_7} + |V_{th_7}| + V_{eff_5} + |V_{th_5}|]}$$

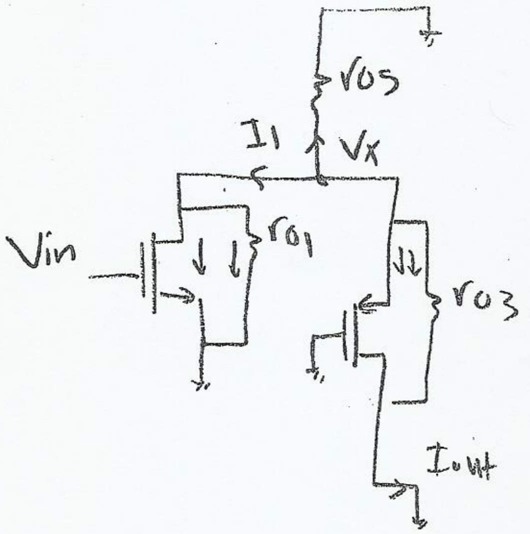
Problem 2

1]



$$\boxed{I_{ref_2} = I_{ref_3} + \frac{I_{ref_1}}{2}}$$

2] to get G_m



$$\boxed{I_1 = g_{m_1} V_{in} + \frac{V_X}{r_{o1}}}$$

KCL at V_X :

$$I_1 + \frac{V_X}{r_{o5}} + I_{out} = 0$$

$$\boxed{I_{out} = -g_{m_1} V_{in} - \frac{V_X}{r_{o1}} - \frac{V_X}{r_{o5}}} \rightarrow (1)$$

$$V_x = r_{o3}\left(I_{out} - g_{m3} V_x \right)$$

$$V_x \left(1 + g_{m3} r_{o3} \right) = r_{o3} I_{out}$$

$$\boxed{V_x = \frac{r_{o3}}{1+g_{m3} r_{o3}} I_{out}}$$

then in (1)

$$I_{out} = -g_{m1} V_{in} - \left(\frac{1}{r_{o1}} + \frac{1}{r_{o5}}\right)\left(\frac{r_{o3}}{1+g_{m3} r_{o3}}\right) I_{out}$$

$$I_{out}\left[1 + \left(\frac{1}{r_{o1}} + \frac{1}{r_{o5}}\right)\left(\frac{r_{o3}}{1+g_{m3} r_{o3}}\right)\right] = -g_{m1} V_i$$

then
$$\boxed{G_m = \frac{I_{out}}{V_{in}} = \frac{-g_{m1}}{1 + \left(\frac{1}{r_{o1}} + \frac{1}{r_{o5}}\right)\left(\frac{r_{o3}}{1+g_{m3} r_{o3}}\right)}}$$

then $A_v = G_m R_{out}$ (gain of half circuit)

A_d (diff. gain) $= -A_v = -G_m R_{out}$

Dominant pole $= w_d = \frac{1}{C_L R_{out}}$

then $GBW = A_d w_d = -G_m \cancel{R_{out}} \frac{1}{C_L \cancel{R_{out}}} = \frac{g_{m1}}{C_L\left[1 + \left(\frac{1}{r_{o1}} + \frac{1}{r_{o5}}\right)\left(\frac{r_{o3}}{1+g_{1}\ldots}\right.\right.}$

$$\boxed{GBW = \frac{g_{m1}}{C_L\left[1 + \left(\frac{1}{\ldots} + \frac{1}{\ldots}\right)\left(\frac{r_{o3}}{\ldots}\right)\right]}}$$

3 for M_3

$V_{DG_3} < |V_{th_3}|$

$$\boxed{V_{out} < |V_{th_3}| + V_{b2}}$$

$$\boxed{V_{out\,max} = |V_{th_3}| + V_{b2\,max}}$$

for M_7

$V_{GD_7} < V_{th_7}$

$V_{b_1} < V_{th_7} + V_{out}$

$$\boxed{V_{out} > V_{b_1} - V_{th_7}}$$

$$\boxed{V_{out\,min} = V_{b1\,min} - V_{th_7}}$$

Maximum output swing for half circuit

$$= \boxed{|V_{th_3}| + V_{b2\,max} - V_{b1\,min} + V_{th_7}}$$

Maximum output swing for differential circuit

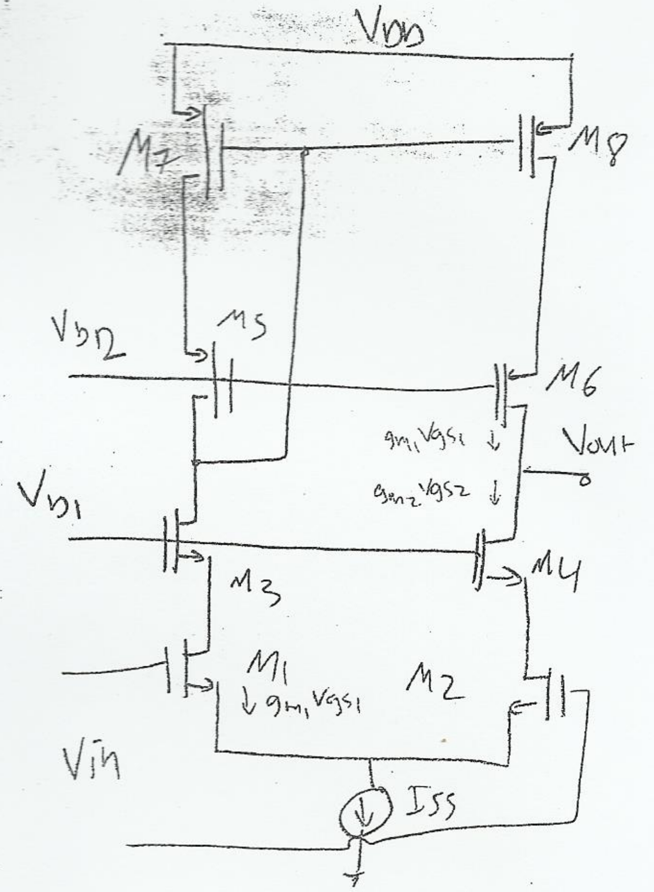
$$= 2 \times \left[|V_{th}|_3 + V_{b2\,max} - V_{b1\,min} + V_{th_7} \right]$$

4 For maximum output swing

V_{b_1} should be min. $= V_{eff_7} + V_{th_7} + V_{eff_9}$

V_{b_2} should be max. $= V_{DD} - V_{eff_5} - [V_{eff_3} + V_{th}$

Problem 3



① DC gain

$$\boxed{G_m = g_{m1}}$$

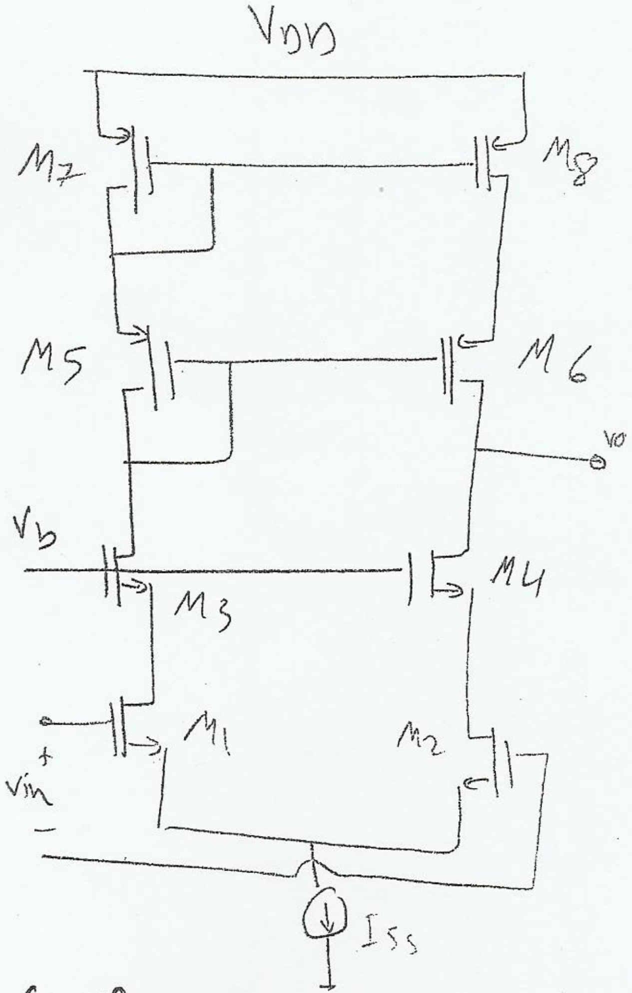
$$\boxed{R_{out} \cong g_{m4} r_{o4} r_{o2} \parallel g_{m6} r_{o6} r_{o8}}$$

$$A_v = G_m R_{out}$$

② GBW

$$\omega_d = \frac{1}{R_{out} C_L}$$

$$GBW = A_v \omega_d = \frac{G_m R_{out}}{R_{out} C_L} = \boxed{\frac{g_{m1}}{C_L}}$$



① DC gain

$$\boxed{G_m = g_{m1}}$$

$$\boxed{R_{out} \cong g_{m4} r_{o4} r_{o2} \parallel g_{m6} r_{o6} r_{o8}}$$

$$A_v = G_m R_{out}$$

② GBW

$$\omega_d = \frac{1}{R_{out} C_L}$$

$$GBW = A_v \omega_d = \frac{G_m R_{out}}{R_{out} C_L} = \boxed{\frac{g_{m1}}{C_L}}$$

③ Maximum output swing

$$\boxed{V_{out\,min} = V_{eff4} + V_{eff2} + V_{effss}}$$

for M6

$$-V_{b2} + V_{out} < |V_{th6}|$$

$$\boxed{V_{out} < |V_{th6}| + V_{b2}}$$

for M5

$$V_{DG} < |V_{th}|_5$$

$$\boxed{V_{DD} - V_{eff7} + |V_{tn7}| < V_{b2} + |V_{tn5}|}$$

for getting Minimum V_{b2}

but we need max V_{b2}

for M7

$$V_{DG7} < |V_{th7}|$$

$$V_{b2} - [V_{eff5} + |V_{tn5}|] - (V_{DD} - [V_{eff7} + |V_{tn7}|]) < V_{th7}$$

$$\boxed{V_{b2max} < V_{DD} - V_{eff7} + V_{eff5} + |V_{th5}|}$$

then $V_{out\,max} < |V_{th6}| + V_{b\,max}$

$$\boxed{V_{out\,max} = |V_{th6}| + V_{DD} - V_{eff7} + V_{eff5} + |V_{tn5}|}$$

swing = $V_{out\,max} - V_{out\,min}$

③ Max. output swing

$$\boxed{V_{out\,min} = V_{eff4} + V_{eff2} + V_{effss}}$$

for M6

$$V_{DG} < |V_{th6}|$$

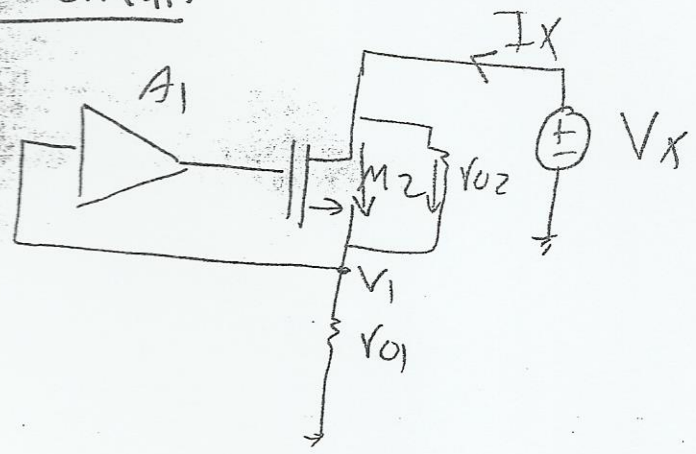
$$V_{out} < |V_{th6}| + V_{DD} - [V_{eff7} + |V_{th}| + V_{eff5} + |V_{th}|$$

$$\boxed{V_{out\,max} = |V_{th6}| + V_{DD} - [V_{eff7} + V_{eff5} + |V}$$

Max. swing = $V_{out\,max} - V_{out\,min}$

Problem (4)

1st Circuit



$$I_x = g_m V_{gs} + \frac{V_x - V_1}{r_{o2}}$$

$$V_{gs} = A_1 V_1 - V_1 = (A_1 - 1) V_1$$

as $\boxed{V_1 = I_x r_{o1}}$

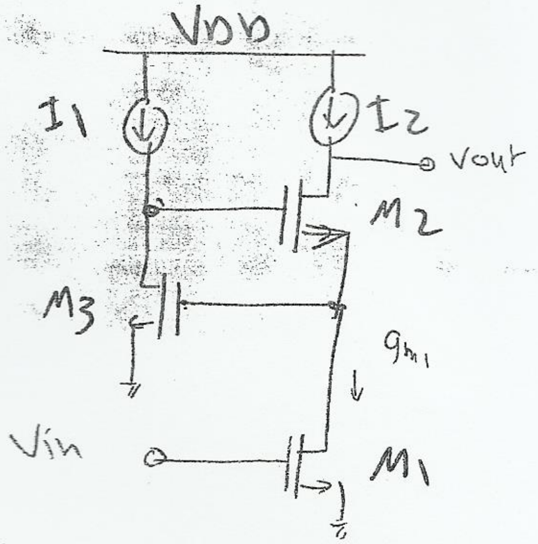
then $V_{gs} = (A_1 - 1)(I_x r_{o1})$

$$I_x = g_m (A_1 - 1)(I_x r_{o1}) + \left(\frac{V_x - I_x r_{o1}}{r_{o2}} \right)$$

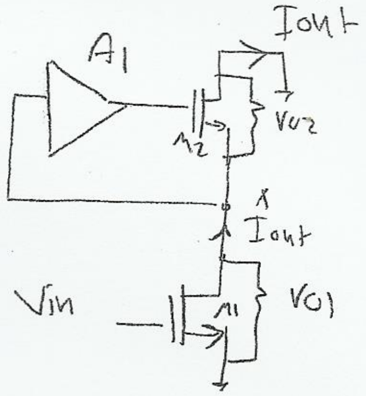
$$I_x \left[r_{o2} - g_m (A_1 - 1) r_{o1} r_{o2} + r_{o1} \right] = V_x$$

$$\boxed{R_{out} = \frac{V_x}{I_x} = (r_{o1} + r_{o2}) - g_m (A_1 - 1) r_{o1} r_{o2}}$$

for the 2nd Circuit



to get Gm



$$I_{out} = -\left[g_{m_2} V_{gs_2} + \frac{0 - V_x}{r_{o2}} \right]$$

$$\boxed{I_{out} = \frac{V_x}{r_{o2}} - g_{m_2}(A_1 - 1) V_x}$$

$$\boxed{V_x = (-I_{out} - g_{m_1} V_{in})\, r_{o1}}$$

then $I_{out} = \underbrace{\left[\frac{1}{r_{o2}} - g_{m_2}(A_1 - 1) \right]}_{\text{let it} \equiv B} r_{o1} \left[-I_{out} - g_{m_1} V_{i}\right.$

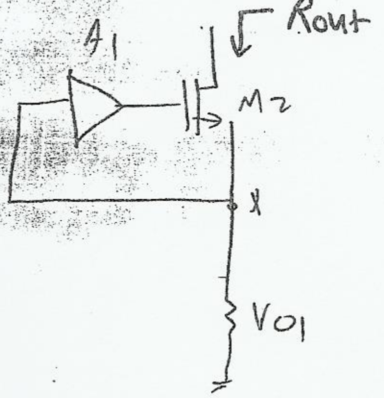
$$I_{out}\left[1 + B r_{o1} \right] = B r_{o1} (-g_{m_1} V_{in})$$

$$G_m = \frac{I_{out}}{V_{in}} = \boxed{\frac{-B r_{o1} g_{m_1}}{1 + B r_{o1}}} \simeq \boxed{-g_{m_1}}$$

where $B = \frac{1}{r_{o2}} - g_{m_2}(A_1 - 1)$

to get Rout

$V_{in} = 0$
$V_{GS_1} = 0$

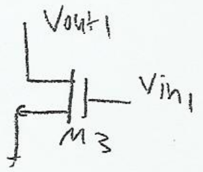


Rout (from the 1^{st} circuit)

$= (r_{o1} + r_{o2}) - g_m (A_1 - 1) r_{o1} r_{o2}$

then $\boxed{A_v = G_m R_{out}}$

where $\boxed{A_1 = -g_{m_3} r_{o3}}$ → Common source amplifier



Problem (5)

Given :-

$V_{DD} = 2.5V$

$\mu_n C_{ox} = 100 \ \mu A/V$

$\mu_p C_{ox} = 50 \ \mu A/V$

$P = 6mW$

$C_Y = 1fF$

$C_L = 1pF$

$W_{nd} = 2\,GBW$

$V_{OD_5} = V_{OD_6}$

$V_{OD_1} = V_{OD_3}$

$r_o = \frac{6000\,L}{I}$

r_o in Ω, L in μm, I in mA

$V_{thn} = 0.5$

$V_{thp} = -0.5$

---

soln

1st stage :-

$$G_{m_I} \approx -g_{m_1}$$

$$R_{out_I} \approx r_{o4} // r_{o2} \simeq \frac{r_{o4}}{2}$$

2nd stage

$$G_{m_{II}} = -g_{m_5}$$

$$R_{out_{II}} = r_{o5} // r_{o6} \simeq \frac{r_{o5}}{2}$$

$$Gain = A_{v_I} * A_{v_{II}}$$

$$\boxed{W_d = \frac{1}{C_L R_{out_{II}}}} \qquad \boxed{W_{nd} = \frac{1}{C_Y R_{out_I}}}$$

$$\text{Power} = 6\,mW$$

$$(I_7 + I_6) V_{DD} = 6\,mW$$

$$\boxed{(I_7 + I_6) = 2.4\,mA}$$

$$\boxed{2I_1 + I_6 = 2.4\,mA}$$

let $V_{OD5} = V_{OD6} = V_{OD7} = 0.2\,V$

$V_{OD1} = V_{OD3} = V_{OD2} = V_{OD4} = 0.15\,V$

let $\boxed{I_6 = 100\,\mu A = 0.1\,mA}$

then $\boxed{I_1 = I_2 = \frac{I_7}{2} = 1.15\,mA}$

then $g_{m1} = \dfrac{2I_1}{V_{OD1}} = \dfrac{46}{3}\,mA/V$

$g_{m5} = \dfrac{2I_5}{V_{OD5}} = 1\,mA/V$

$\boxed{R_{out\,I} = \dfrac{3000\,L_4}{1.15}}$

then $W_{nd} = \dfrac{23 \times 10^{11}}{6\,L_4}$

$\boxed{R_{out\,II} = \dfrac{3000\,L_5}{0.1}}$

$W_d = \dfrac{10^8}{3L_5}$

$$\text{Gain} = g_{m1}\, g_{m5}\, R_{out\,I}\, R_{out\,II}$$

$$= (1)\left(\frac{46}{3}\right)(10^{-6})\left(\frac{6000\, L_4}{2 \times 1.15}\right)\left(\frac{6000\, L_5}{2 \times 0.1}\right)$$

$$\boxed{\text{Gain} = 1200\, L_4 L_5}$$

for $\quad W_{nd} = 2\,GBW \quad = 2 * \text{Gain} * W_d$

$$\frac{23 \times 10^{11}}{6\,\text{[illegible]}\,L_4} = 2(1200)(L_4 L_5)\left(\frac{10^8}{3 L_5}\right)$$

then $\quad L_4 = \sqrt{\frac{115}{24}} \simeq 2.18898\ \mu m$

let $\quad L_2 = L_4$

let $\quad L_5 = L_6 = 5\ \mu m$

then $\quad \boxed{W_d = \frac{20}{3} \times 10^6\ \text{rad/sec}}$

$$\boxed{W_{nd} = 1.75119 \times 10^{11}\ \text{rad/sec}}$$

$$\boxed{\text{Gain} = 13133.925\ \text{V/V}}$$

<u>for M_5</u>

$$I_5 = \frac{K}{2} V_{OD_5}^2$$

$$100 = (0.5)(100) \left.\frac{W}{L}\right)_5 (0.2)^2$$

$$\boxed{W_5 = 50 L_5}$$

<u>for M_6</u>

$$I_6 = \frac{K}{2} V_{OD_6}^2$$

$$100 = (0.5)(50) \left.\frac{W}{L}\right)_6 (0.2)^2$$

$$\boxed{W_6 = 100 L_6}$$

<u>for M_2</u>

$$\boxed{W_2 = 2044.44 L_2}$$

<u>for M_4</u>

$$\boxed{W_4 = 1022.2 L_4}$$

<u>output swing</u> $= V_{out\,max} - V_{out\,min}$

$$= (V_{DD} - V_{eff_6}) - (V_{eff_5})$$

$$= V_{DD} - (2 \times 0.2)$$

$$= \boxed{2 \text{ Volts}}$$

for M_7, M_8

$$V_{DG} \leq |V_{thp}|$$

$$V_{DD} - V_b \leq |V_{thp}|$$

$$V_b \geq V_{DD} - |V_{thp}|$$

then $V_b = V_{DD} - |V_{thp}|$

for $\boxed{V_{SG} - |V_{th}|_p = V_{OD}}$ $= 2.4 - 0.5$

$$\boxed{V_b = 1.9\ V}$$

Problem (6)

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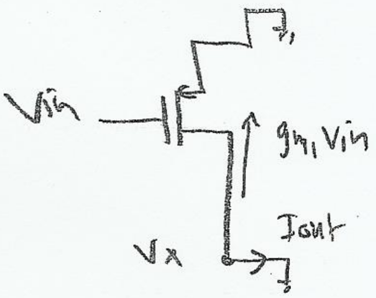
from the circuit sym. , we will work on one half only.

Gain of half circuit = Gain of first stage * Gain of 2nd.

1st stage



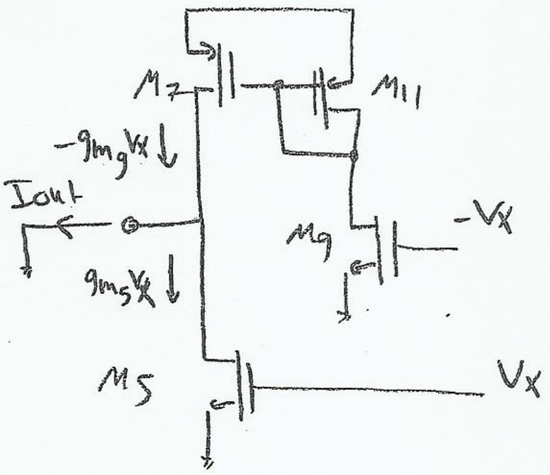
$I_{out} = -g_{m1} V_{in}$

$\boxed{Gm_I = -g_{m1}}$

$\boxed{Rout_I = r_{o1} \,//\, r_{o3}}$

$\boxed{Av_I = Gm_I \, Rout_I}$

2nd stage



$I_{out} = - g_{m9}V_x - g_{m5}V_x$

$= -(g_{m9} + g_{m5})V_x$ for symmetry, $g_{m9} =$

$I_{out} = -2g_{m9}V_x$

$\boxed{Gm_{II} = -2g_{m9}}$ $\boxed{Rout_{II} = r_{o7} \,//\, r_{o5}}$

then $\boxed{Av_{II} = Gm_{II} \, Rout_{II}}$

then $Av = Av_I \, Av_{II}$ (gain of half circuit)

$$\boxed{Av = 2 g_{m9} \, g_{m1} \, (r_{o1} \parallel r_{o3})(r_{o7} \parallel r_{o5})}$$

& $\boxed{Ad = -Av}$ → differential gain