

# CMOS Analog IC Design

**Course Duration:** 90 hours (45 hours lectures + 45 hours labs)

**CAD Tools:** Full-custom design tools from any major EDA vendor (Cadence, Synopsys, Mentor)

**Instructor:** [Dr. Hesham Omran](#) (Email: [hesham.omran@eng.asu.edu.eg](mailto:hesham.omran@eng.asu.edu.eg))

## Course Prerequisites:

- Basic undergraduate mathematics: complex numbers, basic differentiation and integration, etc.
- Basic undergraduate circuit analysis course: resistors, capacitors, inductors, Ohm's law, KVL, KCL, nodal analysis, mesh analysis, superposition, Norton and Thevenin equivalents, simple RC circuits.
- Basic undergraduate semiconductor physics course: doping, n-type and p-type semiconductors, holes, electrons, diffusion and drift currents, pn-junction operation and models.
- Basic undergraduate electronic circuits course: transistor models, dc biasing, small signal analysis, basic amplifiers (common-source, common-gate, common-drain), op-amp applications (inverting amplifier, non-inverting amplifier, integrator, differentiator, etc.).

## Course Description:

- This course covers core topics in analog IC design, and prepares the student for real-life design of complex analog/mixed-signal blocks. The course focuses on CMOS circuits because CMOS is the prevalent technology in the integrated circuits market. Both analysis and design are covered in this course.
- The course contains a strong hands-on component. Each training day is composed of lectures and labs. During the labs, the students will be trained to use industry-standard CAD tools to analyze and design analog CMOS circuits.
- The course applies modern teaching methods such as the flipped classroom model and interactive discussions. You will be challenged with interview questions and you will be given practical tips and hints. Your progress will be continuously assessed using daily quizzes and you will be given real feedback on your work.
- This course fills the following gaps in conventional undergraduate/graduate courses:
  1. Focusing on analysis by inspection skills and developing the "designer's intuition" which is necessary to be a real designer
  2. Verifying hand-analysis and theoretical concepts using extensive circuit simulations
  3. Using industry standard CAD tools to design and verify analog CMOS circuits
  4. Design of analog CMOS circuits to achieve required specifications using state-of-the-art design methodologies

## Course Resources:

- [Lecture videos \(part 1\)](#)
- [Lecture videos \(part 2\)](#)
- [Lecture slides](#)
- [Labs \(Cadence\)](#)
- [Labs \(Mentor\)](#)
- [MaharaTech MOOC \(part 1\)](#)
- [MaharaTech MOOC \(part 2\)](#)

## Course Plan:

Day	Lecture (3h/day)	Lab (3h/day)
1	<ul style="list-style-type: none"> <li>• Lecture 01: Introduction</li> <li>• Lecture 02: Circuits and systems review</li> <li>• Lecture 03: Semiconductors review</li> </ul>	<ul style="list-style-type: none"> <li>• <b>Lab 01 (Part 1): Basic simulations of RC circuit</b> Transient simulation, AC simulation, pole-zero simulation, parametric sweeps, calculator and expressions</li> </ul>
2	<ul style="list-style-type: none"> <li>• Lecture 04: MOSFET large signal model</li> <li>• Lecture 05: MOSFET small signal model</li> </ul>	<ul style="list-style-type: none"> <li>• <b>Lab 01 (Part 2): MOSFET long channel and short channel characteristics</b> DC sweeps, ID-VGS, gm-VGS, ID-VDS, gm and gds in triode and saturation</li> </ul>
3	<ul style="list-style-type: none"> <li>• Lecture 06: Single-stage CMOS amplifiers</li> <li>• Lecture 07: Cascode amplifiers</li> </ul>	<ul style="list-style-type: none"> <li>• <b>Lab 02: Common-source amplifier</b> Creating design charts, OP simulation, gain non-linearity, maximum attainable gain, gain linearization</li> </ul>
4	<ul style="list-style-type: none"> <li>• Lecture 08: Frequency response (1)</li> <li>• Lecture 09: Frequency response (2)</li> </ul>	<ul style="list-style-type: none"> <li>• <b>Lab 03: Cascode amplifier</b> Cascode with active load, cascode with resistive load, effect of cascode on gain, BW, and GBW</li> </ul>
5	<ul style="list-style-type: none"> <li>• Lecture 10: Current mirrors</li> </ul>	<ul style="list-style-type: none"> <li>• <b>Lab 04: Frequency response of CD buffer</b> Complex poles, frequency-domain peaking, time-domain ringing, inductive rise</li> </ul>
6	<ul style="list-style-type: none"> <li>• Lecture 11: Differential amplifier</li> </ul>	<ul style="list-style-type: none"> <li>• <b>Lab 05: Current mirrors</b> Simple current mirror, cascode current mirror, wide-swing (low-compliance) current mirror</li> </ul>
7	<ul style="list-style-type: none"> <li>• Lecture 12: Five-transistor OTA</li> <li>• Lecture 13: Gm/ID design methodology</li> </ul>	<ul style="list-style-type: none"> <li>• <b>Lab 06: Differential amplifier</b> Differential gain, common-mode gain, CMRR, common-mode input range, large signal operation</li> </ul>
8	<ul style="list-style-type: none"> <li>• Lecture 14: OTA design example</li> </ul>	<ul style="list-style-type: none"> <li>• <b>Lab 07: OTA design</b> Gm/ID design charts, design procedure of five-transistor OTA, open-loop simulation, closed-loop simulation</li> </ul>
9	<ul style="list-style-type: none"> <li>• Lecture 15: Negative feedback</li> </ul>	
10	<ul style="list-style-type: none"> <li>• Lecture 16: OTA stability and compensation</li> </ul>	<ul style="list-style-type: none"> <li>• <b>Lab 08: Negative feedback</b> Behavioral modeling, hierarchy editor, effect of feedback on gain/BW/GBW, open-loop gain, closed-loop gain, loop-gain, gain desensitization</li> </ul>
11	<ul style="list-style-type: none"> <li>• Lecture 17: Noise (1)</li> <li>• Lecture 18: Noise (2)</li> </ul>	<ul style="list-style-type: none"> <li>• <b>Lab 09 (Mini Project 01): Two-stage Miller OTA</b> Design procedure of two-stage Miller OTA, frequency compensation, RHP zero, verification</li> </ul>
12	<ul style="list-style-type: none"> <li>• Lecture 19: OTA topologies</li> </ul>	
13	<ul style="list-style-type: none"> <li>• Lecture 20: Common-mode feedback (CMFB)</li> </ul>	<ul style="list-style-type: none"> <li>• <b>Lab 10: Noise simulation</b> AC noise simulation, transient noise simulation, noise in five-transistor OTA</li> </ul>
14	<ul style="list-style-type: none"> <li>• Lecture 21: Slew rate and PSRR</li> <li>• Lecture 22: Variability and mismatch</li> </ul>	<ul style="list-style-type: none"> <li>• <b>Lab 11 (Mini Project 02): Fully differential folded cascode OTA</b> Design of folded cascode OTA with capacitive feedback, behavioral and actual CMFB network</li> </ul>
15	<ul style="list-style-type: none"> <li>• Lecture 23: Biasing and references</li> </ul>	