ECE 425 - VLSI Design & Test Automation
Spring 2021
Project - Combinational Circuit Logic Simulation Tool
Due Date: 04-30-2021

1 Objective

The objective of this part of the project is to implement a logic simulation tool in C language for combinational circuits. Logic simulation is defined as the process of applying values at the primary inputs (Input vector) and observe and report the values at the primary outputs (Output Response). You have to use the codes already provided.

2 Input Files

This project uses basic C data structures (Arrays, Structures and Pointers). The input to your program is an ISCAS'85 benchmark combinational circuit(.isc) and corresponding file that contains the input vectors(.vec).The nodes of the circuit have already been labeled topological

1. **.isc**: *This file contains information about the combinational circuit.*
2. **.vec**: *This file contains information about the input vectors (values at the primary inputs).* Each line in this file is a input vector. The total number of characters in each line is equal to the number of primary inputs in the corresponding circuit.The characters in the line represents '0': logic zero, '1': logic one, 'x': don't care value. During simulation, the 'x' is considered as ' 2' for this part of the project. The *.vec* file contains only few input vector of all possible input vectors of the circuit.

3 Exercises

We will provide code to read the **.isc** files and store the information in **NODE** structures. The NODE structure is an adjacency list and the PATTERN structure is an array.

1. **Step 1:** Understand how the data structures and graphs have been programed. Structure array is an adjacency list where for each node we have linked lists of all its predecessor and successor nodes that represent Fanin and Fanout of that node.
2. **Step 2:** How to traverse the graph G. The nodes are already labeled in topological order. The focus will be to learn how to traverse a linked list for each node V.
3. **Step 3:** To create arrays to store the truth tables for the three basic functions (OR,AND,NOT).
4. **Step 4:** To develop code that determines the logic values at the output of node V after we traverse the linked list of its predecessors.

5. **Step 5:**Apply the input pattern to the primary input of circuit and propagate these values to the primary output of the circuit. The output response obtained at the primary outputs of the given circuit by this step is called output response of the circuit.

4 Submission

Simulate every input vector and report the corresponding logic responses at the primary outputs for all given circuits. The input pattern and its output response should be saved in an output file. Submission requires:

1. All the program code files.
2. Generated result file for each combinational circuit (**one file with input pattern and its output response**). The output file contains all the information in the order exactly as the given **.vec** file.

Note: Codes and results should be verified by TA before submission. Unverified submission will not be considered and results in zero points.
Submission is online through D2L. Printout submission is not needed. The submission contains above mentioned files.