ECE 520 - VLSI Design & Test Automation
Spring 2020
Project Part 2 - Combinational Circuit Logic Fault Simulation Tool
Due Date: 04-24-2020

1 Objective

The objective of this part of the project is to implement a serial fault simulation tool in C language for combinational circuits. You have to use the codes already implemented for Project part 1.

2 Input Files

The input to your program is an ISCAS-85 benchmark combinational circuit (*.isc*), corresponding file that contains the input vectors (*.vec*) and faults information (*.faults*).

1. **.isc**: This file contains information about the combinational circuit.
2. **.vec**: This file contains information about the input vectors (values at the primary inputs). Each line in this file is a input vector. The total number of characters in each line is equal to the number of primary inputs in the corresponding circuit. The characters in the line represents '0': logic zero, '1': logic one, 'x': don't care value. During simulation, the 'x' is considered as '2'. The *.vec* file contains only few input vector of all possible input vectors of the circuit.
3. **.fau**: This file contains information about the fault nodes and its struck at value of a particular circuit. Each line in this file is about the single stuck-at fault. The line 3\1 represents gate with the id '3' has struck at the value '1'. The *.faults* file contains only few faults among all possible faults of the circuit.

3 Serial Fault Simulation Program Flow

Required: The information provided in the first two input files need to be stored in the respective data structures as described in the part 1 .

1. Write a function to read the *.faults* file and store the information in the FAULT structure.
2. Take a single input vector in the PATTERN structure.
3. Apply the input pattern to the primary input of circuit ('x' value is assigned as '2') and propagate these values to the primary output of the circuit. The output response obtained at the primary outputs of the given circuit by this step is called fault free response of the circuit.

4. Print the Input vector, Input vector after 'x' value assigned and output response for each pattern in the output file.
5. Take a single fault in the FAULT structure. Inject the fault in the particular node and propagate the faulty value to the primary output. The output response obtained after injecting the fault is called as faulty response of the circuit.
6. Compare the fault free and faulty response to identify whether the fault at particular node is identified by the given input pattern or not.
7. Print the fault is detected or not in the output file.
8. Repeat the steps 5-7 for each fault in the FAULT structure for the single input pattern.
9. Repeat the steps 2-8 for each input vector in the PATTERN structure of the given circuit.

Note: The steps excluding 5-7 are already done in Project part 1.

4 Submission

Submission is through D2L. Printout submission is not needed. The submission contains below mentioned files.

Note: Codes and results should be verified by TA before submission. Unverified submission will not be considered and results in zero points.

1. All the program code files.
2. Generated result files for each combinational circuit. The output file contains all the information in the order exactly as described in the above Program Flow.