1. Description

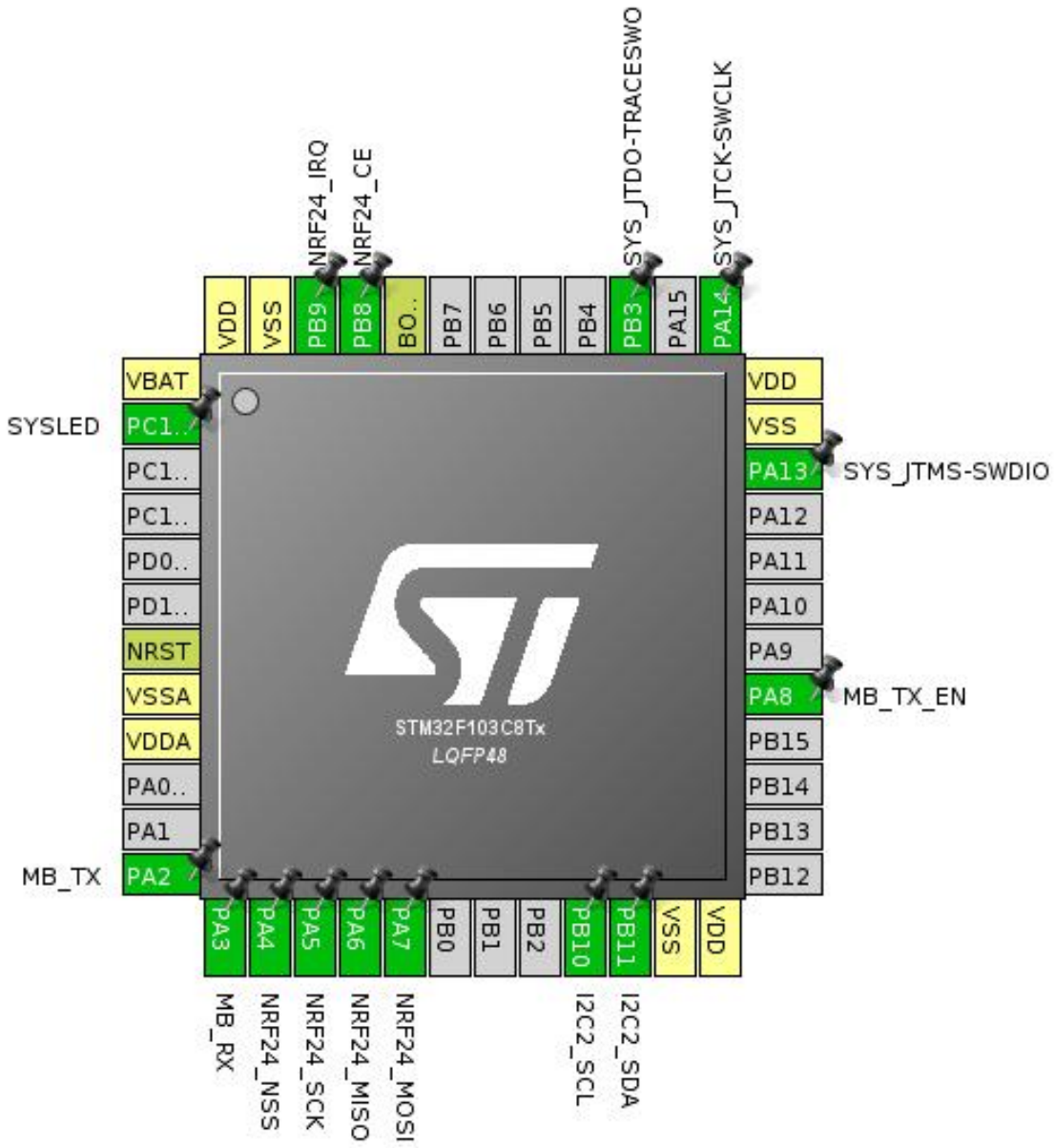
1.1. Project

Project Name	sensor-server-lqfp48
Board Name	No information
Generated with:	STM32CubeMX 4.9.0
Date	08/23/2016

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-TAMPER-RTC *	I/O	GPIO_Output	SYSLED
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
12	PA2	I/O	USART2_TX	MB_TX
13	PA3	I/O	USART2_RX	MB_RX
14	PA4	I/O	SPI1_NSS	NRF24_NSS
15	PA5	I/O	SPI1_SCK	NRF24_SCK
16	PA6	I/O	SPI1_MISO	NRF24_MISO
17	PA7	I/O	SPI1_MOSI	NRF24_MOSI
21	PB10	I/O	I2C2_SCL	
22	PB11	I/O	I2C2_SDA	
23	VSS	Power		
24	VDD	Power		
29	PA8 *	I/O	GPIO_Output	MB_TX_EN
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
39	PB3	I/O	SYS_JTDO-TRACESWO	
44	BOOT0	Boot		
45	PB8 *	I/O	GPIO_Output	NRF24_CE
46	PB9	I/O	GPIO_EXTI9	NRF24_IRQ
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. IPs and Middleware Configuration

4.1. I2C2

I2C: I2C

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

4.2. IWDG

mode: Activated

Clocking:

IWDG counter clock prescaler	4
IWDG down-counter reload value	4095

4.3. SPI1

Mode: Full-Duplex Master

mode: Hardware NSS Signal

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**16.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Output Hardware

4.4. SYS

Debug: Trace-Asynchronous_SW

4.5. TIM4

mode: Clock Source

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

4.6. USART2

Mode: Asynchronous

Basic Parameters:

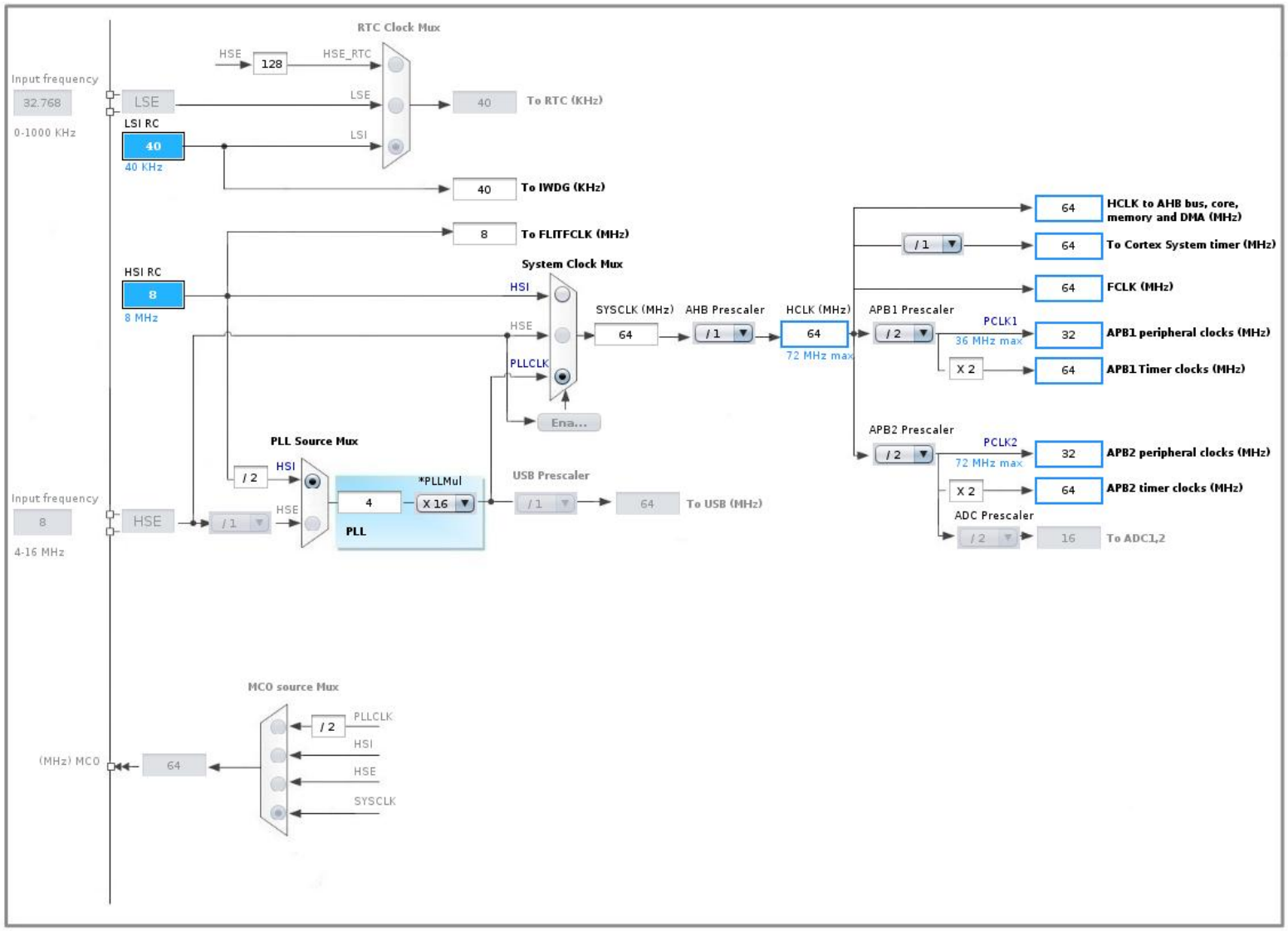
Baud Rate	115200
Word Length	**9 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

2. Clock Tree Configuration



3. Power Plugin report

3.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103C8Tx
Datasheet	13587_Rev16

3.2. Parameter Selection

Temperature	25
Vdd	3.3