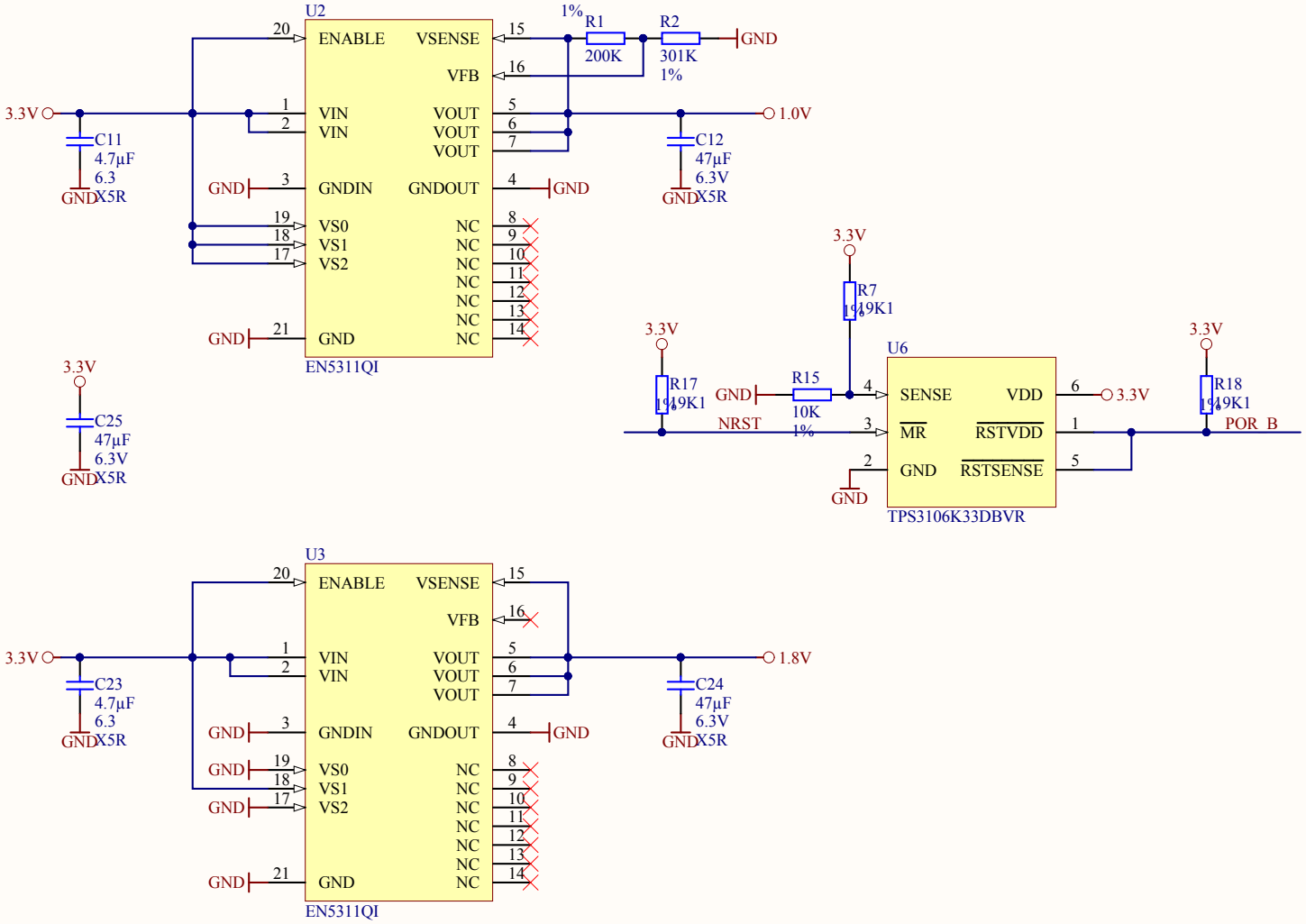

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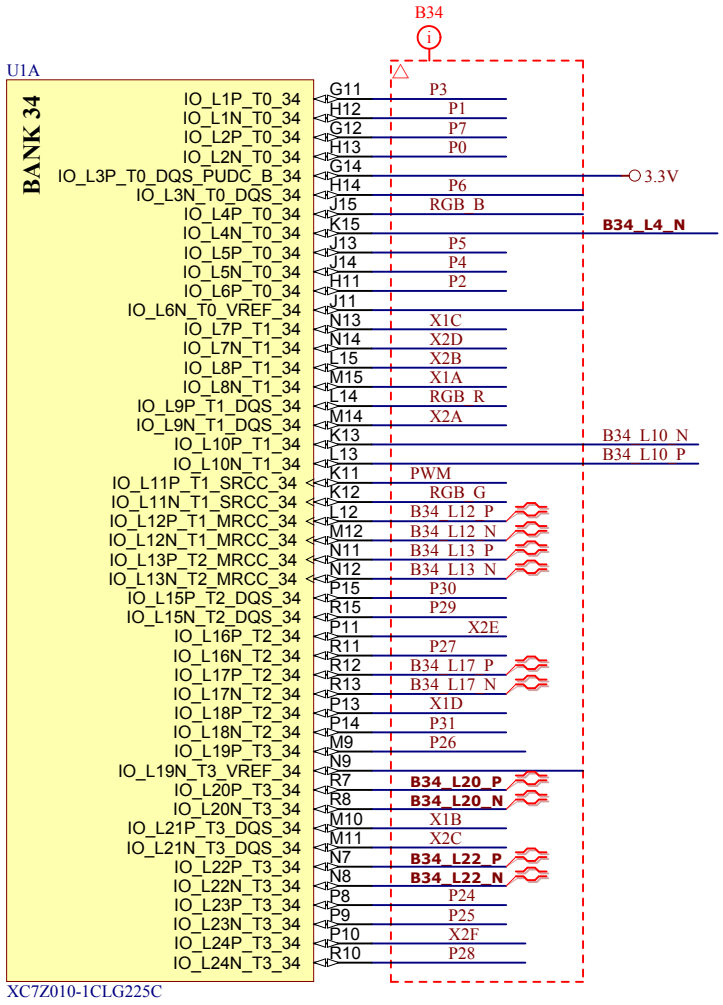

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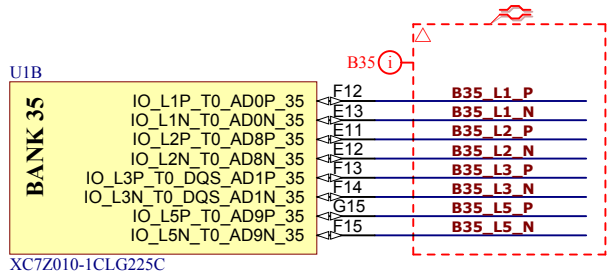

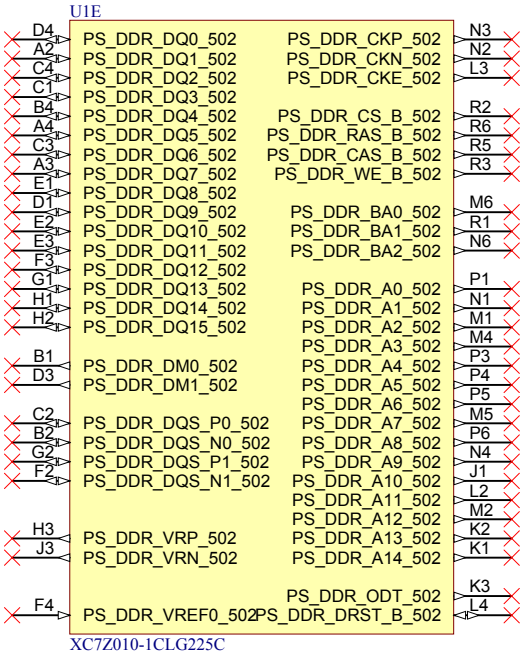

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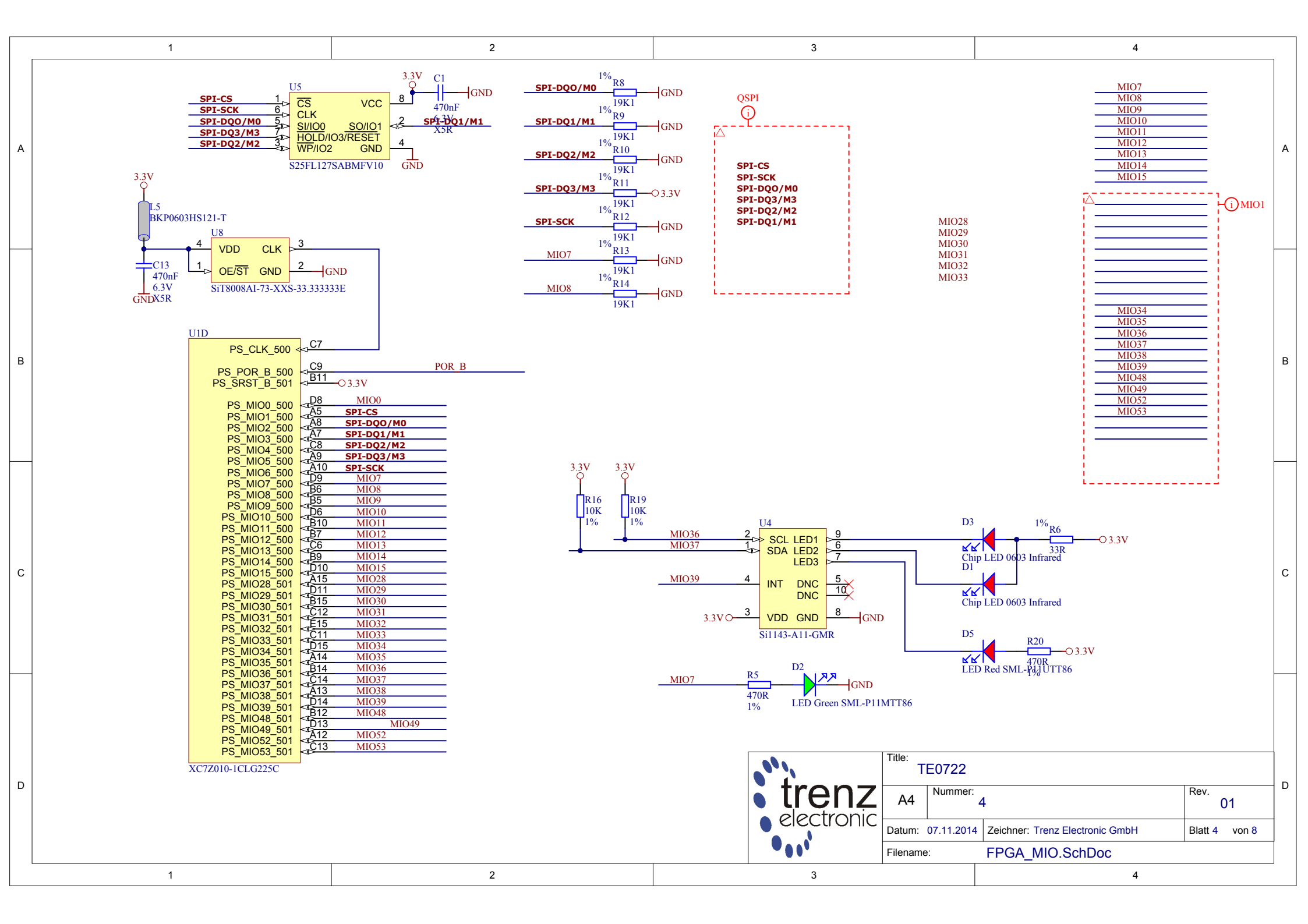
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SPI-DQ3/M3
SPI-DQ2/M2
CS
CLK
SI/IO0
HOLD/IO3/RESET
WP/IO2
VCC
SO/IO1
GND
S25FL127SABMFV10
3.3V
C1
470nF
6.3V
X5R
GND
SPI-DQ1/M1
R8
R9
R10
R11
R12
R13
R14
19K1
1%
MIO7
MIO8
QSPI
MIO28
MIO29
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MIO31
MIO32
MIO33
MIO34
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L5
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C13
U1D
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D1
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Zeichner:
Trenz Electronic GmbH
Blatt 4
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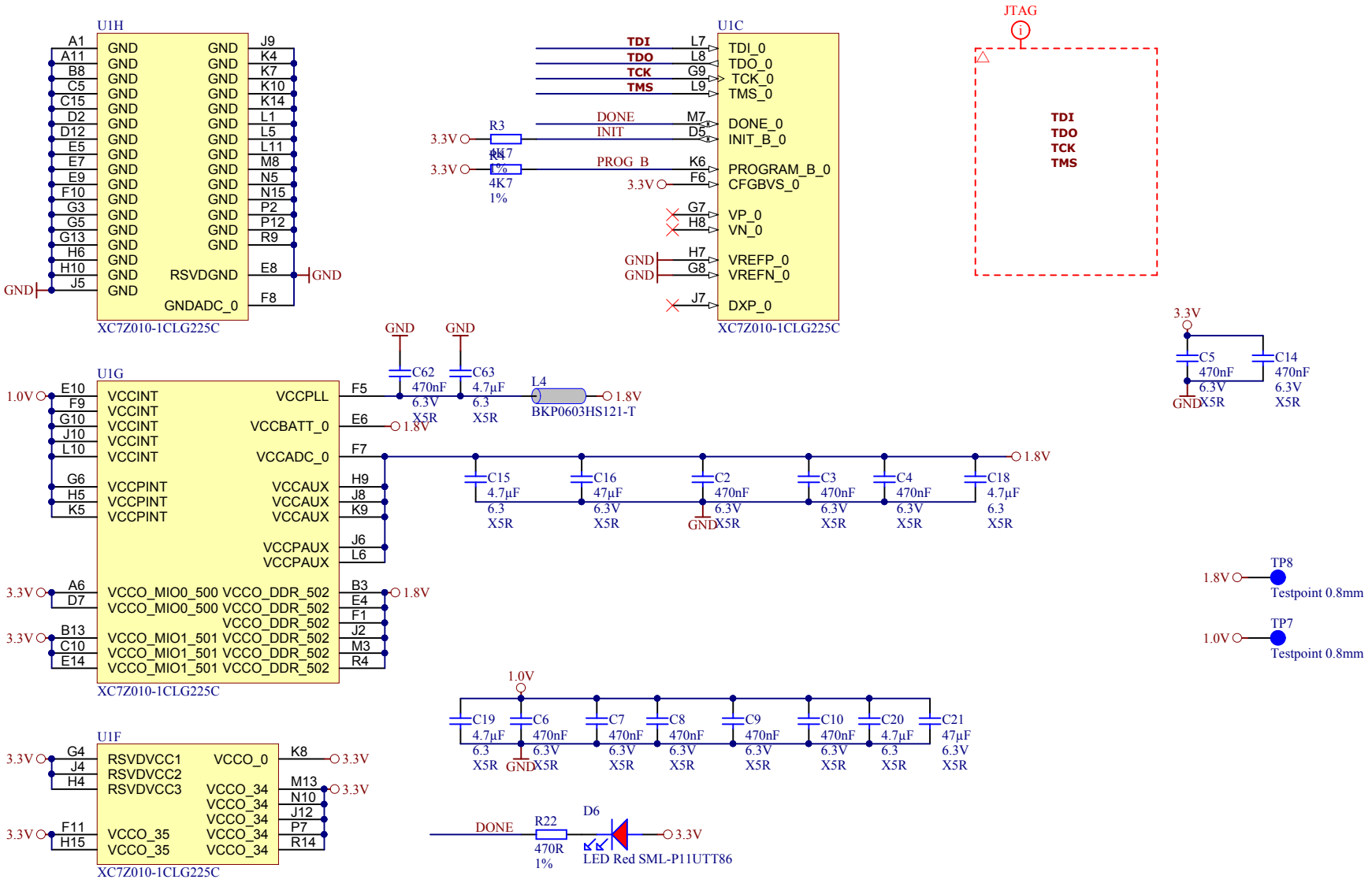

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Hardware released under CERN OHL version 1.2
http://www.ohwr.org/projects/cernohl/wiki

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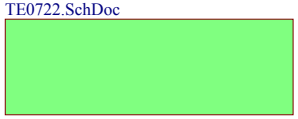

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U_POWER
POWER.SchDoc

U_FPGA_B34
FPGA_B34.SchDoc

U_FPGA_B35
FPGA_B35.SchDoc

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U_FPGA_PWR
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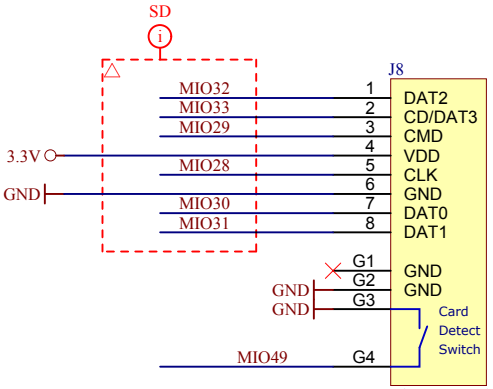

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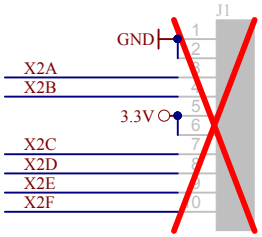

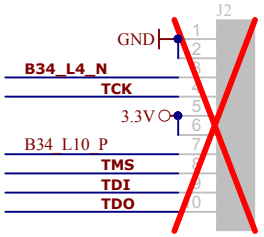

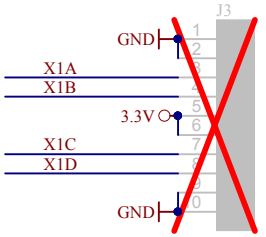

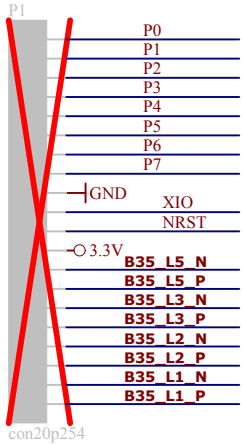

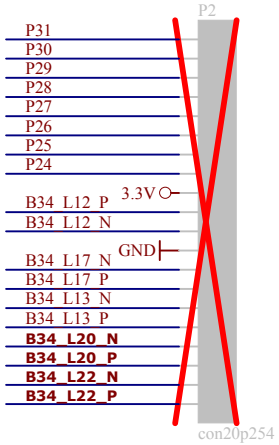

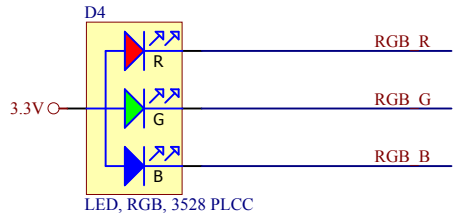

LED, RGB, 3528 PLCC

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