

# UMC



## UM92870 Series

### Integrated DTMF Receiver

#### Features

- Full DTMF receiver in single 18-pin package
- Single 5-volt power supply
- Internal gain setting amplifier
- Adjustable guard time
- Built-in dial-tone filter

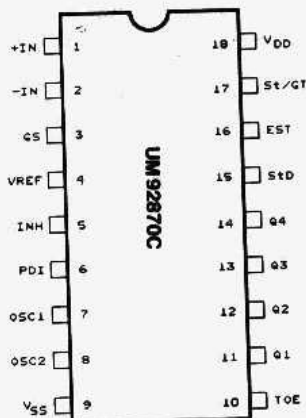
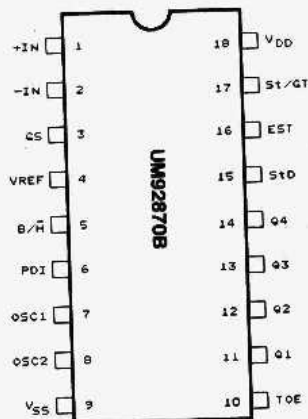
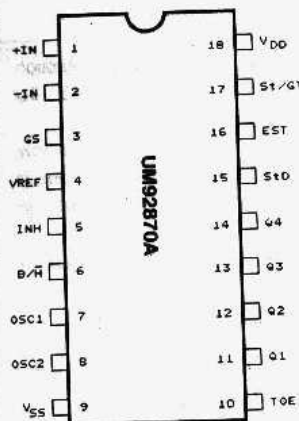
- Uses inexpensive 3.5795 MHz crystal
- CMOS for low power consumption
- Tristate outputs
- Early steering output

#### General Description

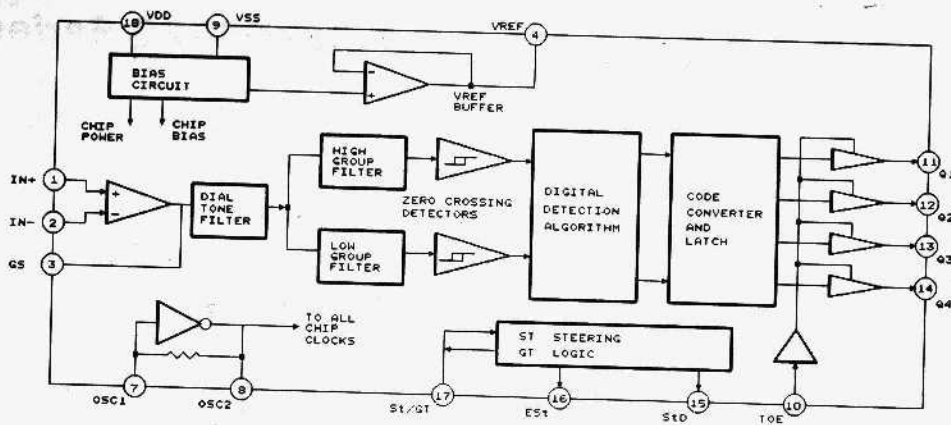
The UM92870 is a complete DTMF receiver designed to detect standard DTMF signals. It includes a differential input amplifier, filter section, decoder section, and steering logic circuits. The differential input amplifier allows adjustment of gain and choice of input configuration. The filter section provides a dial tone filter for dial-tone rejection and separates

the dual-tone signal into low-group and high-group tones. The decoder decodes all 16 DTMF tone pairs into a four bit code. The steering logic circuits allow the designer to tailor system parameters such as talk-off and noise immunity. The UM92870 is packaged in 3 standard 18-pin DIP configurations and requires only a few external passive components.

#### Pin Configurations



### Block Diagram



### Pin Description

Pin No.	Symbol	I/O	Description									
1	IN+	I	Non-inverting input of op-amp.									
2	IN-	I	Inverting input of op-amp.									
3	GS	I	Gain select. Gives access to output of front end differential amplifier for connection of feedback resistor.									
4	VREF	O	Reference Voltage output. May be used to bias the inputs at midrail, $V_{DD}/2$ .									
5,6	INH , B/ $\bar{H}$ , PDI	I,I,I	<p>INH: DTMF signal control,When this pin is pulled high, detection of tone pairs containing the 1633Hz component is inhibited. To detect all 16 standard digits this pin must be pulled low.</p> <p>B/ <math>\bar{H}</math> : Digital output format control. When this pin is pulled low, the UM92870 output is given in hexadecimal code. When input is high, output is in 2-of-8 binary code. Output codes are shown in Table 1.</p> <p>PDI: power down input. To enter power down mode, this pin must be pulled high.</p> <table><tr><td>UM92870A</td><td>Pin No. 5,6</td><td>INH , B/ <math>\bar{H}</math></td></tr><tr><td>UM92870B</td><td>Pin No. 5,6</td><td>B/ <math>\bar{H}</math> , PDI</td></tr><tr><td>UM92870C</td><td>Pin No. 5,6</td><td>INH, PDI</td></tr></table>	UM92870A	Pin No. 5,6	INH , B/ $\bar{H}$	UM92870B	Pin No. 5,6	B/ $\bar{H}$ , PDI	UM92870C	Pin No. 5,6	INH, PDI
UM92870A	Pin No. 5,6	INH , B/ $\bar{H}$										
UM92870B	Pin No. 5,6	B/ $\bar{H}$ , PDI										
UM92870C	Pin No. 5,6	INH, PDI										

**Pin Description (Continued)**

Pin No.	Symbol	I/O	Description
7	OSC1	I	Clock input.
8	OSC2	I	Clock output. A 3.5795 MHz crystal connected between OSC1 and OSC2 completes the oscillator circuit.
9	Vss	I	Negative power supply input.
10	TOE	I	Three-state output enable. Logic high enables the output from Q1 through Q4.
11 - 14	Q1 - Q4	O	Three-state output. When enabled by TOE, provides the code which corresponds to the last valid tone-pair received. See Table 1.
15	StD	O	Delayed steering output. Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/Gt falls below VTST.
16	ESst	O	Early steering output. Presents a logic high once the digital algorithm has detected a valid tone pair. Any subsequent loss of signal condition will cause ESst to return to a logic low.
17	St/GT	I/O	Steering input/guard time output (bi-directional). A voltage greater than VTST detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than VTST output acts to reset the external steering time constant; its state is a function of ESst and the voltage on St.
18	VDD	I	Positive power supply input.

Stock #

(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13) (14) (15) (16) (17) (18) (19) (20) (21) (22) (23) (24) (25) (26) (27) (28) (29) (30) (31) (32) (33) (34) (35) (36) (37) (38) (39) (40) (41) (42) (43) (44) (45) (46) (47) (48) (49) (50) (51) (52) (53) (54) (55) (56) (57) (58) (59) (60) (61) (62) (63) (64) (65) (66) (67) (68) (69) (70) (71) (72) (73) (74) (75) (76) (77) (78) (79) (80) (81) (82) (83) (84) (85) (86) (87) (88) (89) (90) (91) (92) (93) (94) (95) (96) (97) (98) (99) (100)

Digit	TOE	Hexadecimal				Binary Coded 2 of 8				Low Group Frequency (Hz)	High Group Frequency (Hz)
		Q4	Q3	Q2	Q1	Q4	Q3	Q2	Q1		
1	H	0	0	0	1	0	0	0	0	697	1209
2	H	0	0	1	0	0	0	0	1	697	1336
3	H	0	0	1	1	0	0	1	0	697	1477
4	H	0	1	0	0	0	1	0	0	770	1209
5	H	0	1	0	1	0	1	0	1	770	1336
6	H	0	1	1	0	0	1	1	0	770	1477
7	H	0	1	1	1	1	0	0	0	852	1209
8	H	1	0	0	0	1	0	0	1	852	1336
9	H	1	0	0	1	1	0	1	0	852	1477
0	H	1	0	1	0	1	1	0	1	941	1336
*	H	1	0	1	1	1	1	0	0	941	1209
#	H	1	1	0	0	1	1	1	0	941	1477
A	H	1	1	0	1	0	0	1	1	697	1633
B	H	1	1	1	0	0	1	1	1	770	1633
C	H	1	1	1	1	1	0	1	1	852	1633
D	H	0	0	0	0	1	1	1	1	941	1633
ANY	L	Z	Z	Z	Z	Z	Z	Z	Z	-	-

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMPEDANCE

Table 1. DTMF Signal Output Codes

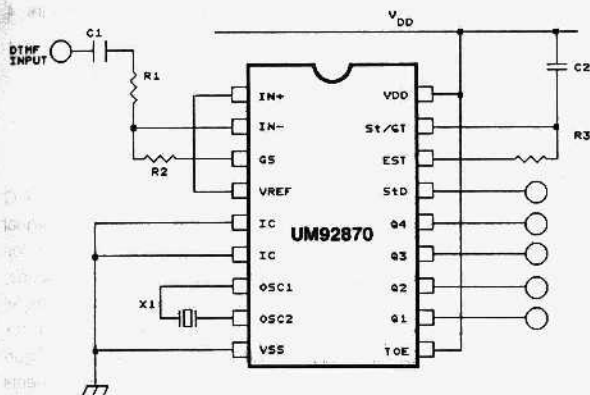
## Function Description

The UM92870 monolithic DTMF receiver offers small size, low power consumption and high performance. Its general operation is described as follows:

### Differential Input Amplifier

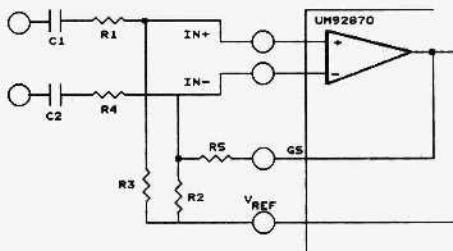
To aid design flexibility, the UM92870 provides a differential input operational amplifier as well as a

bias source (  $V_{REF}$  ) which is used to bias the input at midrail. Adjustment of gain is achieved by connecting a feedback resistor to the op-amp output (GS). Figure 1 shows the differential configuration with the op-amp connected for unity gain and  $V_{REF}$  biasing the input at  $V_{DD}/2$ . Figure 2 shows the differential configuration, which permits the adjustment of gain with the feedback resistor,  $R_5$ .



#### Notes:

- $R_1, R_2 = 100\text{k}\Omega \pm 1\%$
- $R_3 = 300\text{k}\Omega \pm 1\%$
- $C_1, C_2 = 100\text{ nF} \pm 5\%$
- $X_1 = 3.579545\text{ MHz}$



#### DIFFERENTIAL INPUT AMPLIFIER

$C_1 = C_2 = 10\text{ nF}$

$R_1 = R_4 = 100\text{k}\Omega$  All resistors are  $\pm 1\%$  tolerance  
 $R_2 = 60\text{k}\Omega$  All capacitors are  $\pm 5\%$  tolerance

$$R_3 = \frac{R_2 R_5}{R_2 + R_5}$$

$$\text{VOLTAGE GAIN (A}_{v\text{ diff}}) = \frac{R_5}{R_1} \cdot \left( \frac{\frac{1}{R_4} + \frac{1}{R_2} + \frac{1}{R_5}}{\frac{1}{R_1} + \frac{1}{R_3}} \right)$$

$$= \frac{R_5}{R_1}, \text{ if } R_1 = R_4 \text{ and } R_3 = \frac{R_2 R_5}{R_2 + R_5}$$

#### INPUT IMPEDANCE

$$Z_{\text{INDIFF}} = \sqrt{R_1^2 + \left( \frac{1}{\omega C} \right)^2}, \text{ where } C = C_1 = C_2$$

Figure 1. Single Ended Input Configuration

Figure 2. Differential Input Configuration

## Filter Section

The differential input stage is followed by a low pass continuous RC active filter which performs an anti-aliasing function. Dial tone at 350Hz and 440Hz is then rejected by a third order switched capacitor notch filter. (See figure 3) The signal, still in its composite form, is then split into its individual high and low

frequency components by two sixth order switched capacitor bandpass filters. Each component tone is then smoothed by an output filter and squared up by a hard limiting comparator. If the original DTMF input signals are valid tones, then the outputs of the comparators will be two rectangular waves.