

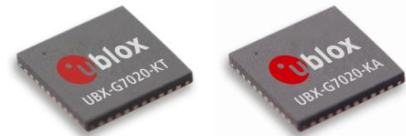
UBX-G7020-KT/KA

u-blox 7 GPS/GNSS chips

Data Sheet

Highlights:

- u-blox 7 position engine featuring excellent accuracy and time-to-first-fix performance
- Multi-GNSS engine for GPS, GLONASS, Galileo and QZSS
- AssistNow Online, Offline and Autonomous for faster TTFF
- Minimal board space
- Low power consumption
- Minimal e-BOM



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Document Information

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Document status information

Objective Specification	This document contains target values. Revised and supplementary data will be published later.
Advance Information	This document contains data based on early testing. Revised and supplementary data will be published later.
Preliminary	This document contains data from product verification. Revised and supplementary data may be published later.
Released	This document contains the final product specification.

This document applies to the following products:

Name	Type number	ROM/FLASH version	PCN reference
UBX-G7020-KT QFN40 package (Standard grade)	UBX-G7020-KT-A0100 A	1.00	N/A
UBX-G7020-KA QFN40 package (Automotive grade)	UBX-G7020-KA-A0100 A	1.00	N/A

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Contents

Contents.....	3
1 Functional description.....	6
1.1 Overview	6
1.2 Highlights and features.....	6
1.3 GNSS performance	7
1.4 Block diagram.....	8
1.5 GPS	8
1.6 Augmented GPS	8
1.6.1 Assisted GPS (A-GPS).....	8
1.6.2 AssistNow Autonomous	9
1.6.3 Differential GPS (D-GPS)	9
1.7 GNSS.....	9
1.7.1 GLONASS	9
1.7.2 Galileo.....	9
1.7.3 QZSS	9
1.8 Data logging.....	9
1.9 Protocols and interfaces.....	10
2 RF subsystem	11
2.1 Low noise amplifier.....	11
2.2 Gain block	11
2.3 Mixer and low-pass filter	11
2.4 Programmable gain amplifier	11
2.5 ADC	11
3 Baseband subsystem.....	13
3.1 GNSS processing engines.....	13
3.2 Interfaces.....	14
3.2.1 UART.....	14
3.2.2 USB.....	14
3.2.3 SPI.....	14
3.2.4 Display Data Channel (DDC)	14
3.2.5 Serial Quad Interface (SQI).....	14
3.2.6 JTAG	14
3.3 Peripheral Input Output (PIO).....	14
3.4 Watchdog (WD).....	15
3.5 Timer Counter (TC).....	15
3.6 Clock generation	15
3.6.1 Crystal and TCXO oscillator	15
3.6.2 PLL	15

3.6.3	Real-Time Clock (RTC)	15
3.7	Power Management Unit (PMU)	16
3.7.1	DC/DC converter	16
3.8	Memory	16
3.8.1	Backup RAM	16
3.8.2	System RAM	16
3.8.3	GNSS RAM	16
3.8.4	Acquisition engine RAM	16
3.8.5	eFuse memory	17
4	Operating modes and power management	18
4.1	Operating modes	18
4.1.1	Continuous Mode	18
4.1.2	Power Save Mode	18
4.2	Calculating power consumption	18
5	Configuration management	19
5.1	Configuration hierarchy	19
5.2	Configuration by PIOs	19
5.2.1	PIO5 (CONFIG-SEL)	19
5.2.2	PIO10 (D-SEL)	19
5.2.3	PIO12 (SBM-SEL)	20
5.3	Configuration by eFuse	20
6	Pin definition	21
6.1	Pin assignment	21
6.1.1	QFN40 (UBX-G7020-KT, UBX-G7020-KA)	21
6.2	Pin description	22
7	Electrical specification	24
7.1	Absolute maximum rating	24
7.2	Operating conditions	25
7.2.1	DC electrical characteristic	25
7.2.2	Baseband AC parameters	26
7.2.3	RF AC parameters	27
7.2.4	Power consumption	28
7.3	Indicative power requirements	28
7.4	SPI timing diagrams	29
7.4.1	Timing recommendations	29
7.5	DDC timing diagrams	29
8	Mechanical specification	30
8.1	QFN40 / UBX-G7020-KT, UBX-G7020-KA	30
9	Reliability tests and approvals	31

9.1	Reliability tests	31
9.2	Approvals	31
10	Product handling	32
10.1	Packaging	32
10.1.1	Reels	32
10.1.2	Tapes	33
10.2	Moisture Sensitivity Levels	33
10.3	ESD handling precautions	33
11	Default messages	34
12	Labeling and ordering information.....	35
12.1	Product labeling	35
12.1.1	QFN40.....	35
12.2	Explanation of product codes.....	36
12.3	Ordering codes	36
	Related documents.....	37
	Revision history.....	37
	Contact.....	38

1 Functional description

1.1 Overview

Featuring a single die solution, low power consumption and low costs, the UBX-G7020 GPS/GNSS chips are multi-GNSS (GPS, GLONASS, Galileo, QZSS and SBAS) positioning chips developed to meet the requirements of an extensive range of applications and end-products. Based on the high performance u-blox 7 position engine, these receivers provide exceptional sensitivity and acquisition times without requiring an external host. u-blox' advanced RF-design and interference suppression measures enable reliable positioning even in difficult signal conditions.

u-blox 7 technology delivers high performance with low power consumption and low costs. An integrated DC/DC converter and intelligent power management are breakthroughs for low-power applications. The minimal BOM requires as few as 8 external components and the small footprint further reduces costs by enabling 2-layer PCB integration. LDOs and an LNA are built-in and costly external memory is not needed. This makes UBX G7020 positioning chips the ideal solutions for cost sensitive applications that don't require firmware update capability. For applications needing firmware update capability the UBX-G7020 can be connected to an external SQI FLASH memory. Lower price GPS/GNSS crystals as well as high performance TCXOs are also supported.

1.2 Highlights and features

- u-blox 7 position engine featuring:
 - over 2 million effective correlators
 - down to 1 s acquisition time
 - -148 dBm coldstart acquisition sensitivity and -162 dBm tracking sensitivity
 - up to 10 Hz update rate
- Supports data logging
- Intelligent, user configurable power management and a built-in DC/DC converter for significantly lower power consumption
- Supports u-blox' AssistNow Online / AssistNow Offline A-GPS services and is OMA SUPL compliant
- Faster acquisition with AssistNow Autonomous (no connectivity required)
- Supports GLONASS and is ready for Galileo
- Supports Crystal and TCXO oscillators
- Minimal BOM costs and minimum board space ($< 30 \text{ mm}^2$) for a complete receiver implementation
- Standard and automotive grade $5.0 \times 5.0 \text{ mm}^2$ QFN40 package with 0.4 mm pitch. This package offers the most cost-effective form of u-blox 7 technology.

1.3 GNSS performance

Parameter	Specification		
Receiver type	56 Channels GPS L1C/A SBAS L1C/A QZSS L1C/A GLONASS L1OF Galileo E1B/C ¹		
Time-To-First-Fix ² (GPS only)	Cold Start Warm Start Hot Start Aided Starts ³	TCXO 26 s 26 s <1 s <1 s	Crystal 27 s 27 s <1 s <3 s
Sensitivity ⁴ (GPS only)	Tracking & Navigation Reacquisition Cold Start Hot Start	TCXO -162 dBm -160 dBm -148 dBm -157 dBm	Crystal -162 dBm -160 dBm -147 dBm -156 dBm
Horizontal position accuracy ⁵	GPS without SBAS GPS with SBAS GLONASS	< 2.5 m < 2.0 m TBD	
Accuracy of Timepulse signal	RMS 99% Time Pulse	30 ns < 60 ns Configurable f = 0.25 Hz ... 10 MHz	
Max navigation update rate		TBD	
Velocity accuracy ⁶		0.1 m/s	
Heading accuracy ⁶		0.5 degrees	
Dynamics		≤ 4 g	
Operational limits	Altitude Velocity	50000 m 500 m/s	

Table 1: u-blox 7 GNSS performance

¹ Ready to support Galileo E1B/C when available

² All satellites at -130 dBm, > 6 SVs

³ Dependent on aiding data connection speed and latency

⁴ Demonstrated with a good external LNA

⁵ CEP, 50%, 24 hours static, -130 dBm, > 6 SVs

⁶ 50% @ 30 m/s

1.4 Block diagram

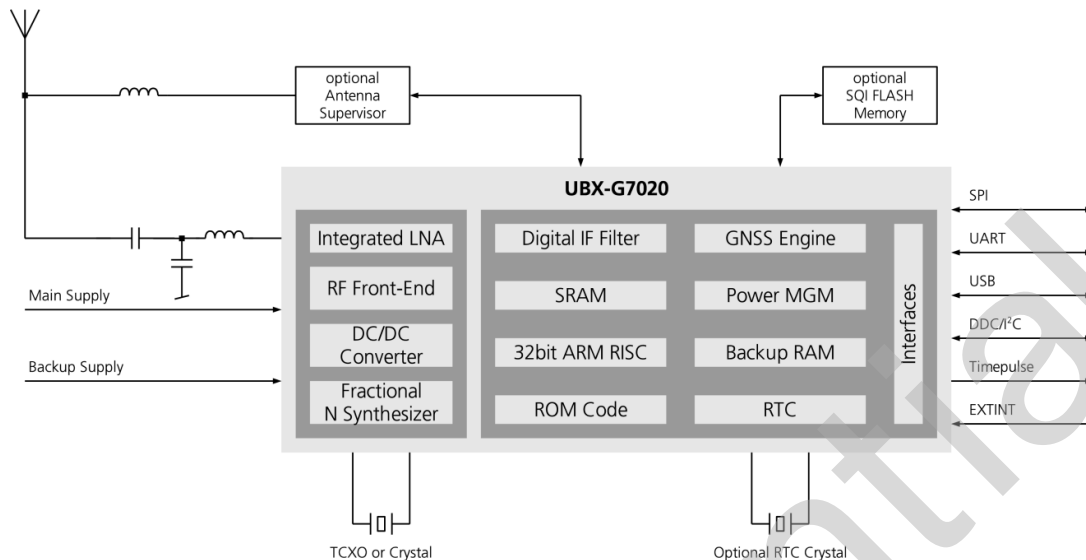


Figure 1: u-blox 7 block diagram

1.5 GPS

u-blox 7 receivers are designed to receive and track the L1C/A signals provided at 1575.42 MHz by the Global Positioning System (GPS).

1.6 Augmented GPS

1.6.1 Assisted GPS (A-GPS)

A-GPS improves GPS performance by delivering aiding data to the GPS receiver via wireless networks or the Internet. Supplying information such as ephemeris, almanac, approximate last position, time and satellite status and an optional time synchronization signal significantly reduces Time to First Fix (TTFF) and improves acquisition sensitivity.

AssistNow Online and AssistNow Offline are u-blox' end-to-end A-GPS services for devices with or without network connectivity. AssistNow Online and AssistNow Offline can either be used alone or in combination. They are very easy to implement, require no additional hardware, and generate virtually no CPU load. All UBX-G7020 chips support u-blox' AssistNow Online, AssistNow Offline and AssistNow Autonomous A-GPS services, and are OMA SUPL compliant.

1.6.1.1 AssistNow Online

With AssistNow Online, an internet-connected GPS device downloads assistance data from u-blox' AssistNow Online Service at system start-up. AssistNow Online is network operator independent and globally available. u-blox only sends ephemeris data for those satellites currently visible to the device requesting the data, thus minimizing the amount of data transferred.

1.6.1.2 AssistNow Offline

With AssistNow Offline, users download u-blox' Differential Almanac Correction Data from the Internet at their convenience. The correction data can either be stored in the GPS receiver's FLASH memory (if available) or in the memory of the application processor. Therefore, the service requires no connectivity at system start-up and enables a position fix within seconds, even when no network is available.

1.6.2 AssistNow Autonomous

AssistNow Autonomous provides functionality similar to Assisted-GPS without the need for a host or external network connection. It is an embedded feature available free-of-charge that accelerates GPS positioning by capitalizing on the periodic nature of GPS satellite orbits. GPS orbit predictions are directly calculated by the GPS receiver and no external aiding data or connectivity is required. AssistNow Autonomous can be used alone, or together with AssistNow Online or AssistNow Offline for increased positioning speed and accuracy.



For more details see the u-blox 7 Receiver Description Including Protocol Specification [2]

1.6.3 Differential GPS (D-GPS)

1.6.3.1 Satellite-Based Augmentation System (SBAS)

u-blox 7 receivers support SBAS. These systems supplement GPS data with additional regional or wide area GPS augmentation data. The system broadcasts the augmentation data via satellite and this information can be used by GPS receivers to improve the resulting GPS precision. SBAS satellites can be used as additional satellites for ranging (navigation), further enhancing precision. The following SBAS are supported with u-blox 7: WAAS, EGNOS and MSAS.



For more details see the u-blox 7 Receiver Description Including Protocol Specification [2]

1.7 GNSS

u-blox 7 GPS chips are multi-GNSS receivers and can receive and track GPS, GLONASS, Galileo and QZSS signals.

1.7.1 GLONASS

u-blox 7 GPS chips can receive and track GPS or GLONASS signals using the same hardware. In order to take advantage of GPS and GLONASS, dedicated hardware preparation must be taken during the design-in phase, see the UBX—G7020 Hardware Integration Manual [1] for u-blox design recommendations.

The ability to receive and track GLONASS L1OF satellite signals with the same hardware results in an optimized hardware BOM and allows design of GLONASS ready receivers where required by regulations.

Note, that because of the different center frequencies, GLONASS and GPS signals cannot be received and tracked simultaneously.

1.7.2 Galileo

u-blox 7 receivers are ready to receive and track GPS and Galileo signals simultaneously, enhancing accuracy and coverage. When Galileo E1B/C signals become available, u-blox 7 receivers equipped with FLASH memory will be able to receive and process them via a simple firmware update. The ability to receive and track Galileo satellite signals will result in higher coverage, improved reliability and better accuracy.

1.7.3 QZSS

The Quasi-Zenith Satellite System (QZSS) is a regional navigation satellite system which transmits in addition to GPS the L1C/A signals for the Pacific region covering Japan and Australia. u-blox 7 receivers are able to receive and to track these signals simultaneously to GPS resulting in better availability especially under bad signal conditions e.g. in urban canyons.

1.8 Data logging

New with u-blox 7 is the data logging feature, which enables continuous storage of position, velocity and time information to an external SPI FLASH memory. The information can be downloaded from the receiver later for further analysis or for conversion to a mapping tool. For more information see the u-blox 7 Receiver Description Including Protocol Specification [2].

1.9 Protocols and interfaces

Protocol	Type
NMEA	Input/output, ASCII, 0183, 2.3 (compatible to 3.0)
UBX	Input/output, binary, u-blox proprietary

Table 2: Available Protocols

All protocols are available on UART, USB, DDC (I2C compliant) and SPI. For specification of the various protocols see the u-blox 7 Receiver Description Including Protocol Specification [2].

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2 RF subsystem

The RF subsystem implements a low-IF architecture. The input signal is either a 6 MHz wide portion of the spectrum centered at the GPS/Galileo L1 band or a 10 MHz wide spectrum centered at the GLONASS L1OF band. The received signal is amplified by a single-ended low-noise amplifier, and then fed to a gain block, which offers further amplification, thus reducing the noise figure requirements for the I and Q mixers. The gain block also provides a single-ended to differential conversion. After down-conversion, I and Q signals are low-pass filtered and amplified by a Programmable Gain Amplifier (PGA). The differential I and Q signals are then sent to the baseband section, where A/D conversion, signal processing and final image rejection are performed.

2.1 Low noise amplifier

The low noise amplifier (LNA) makes use of a single stage cascode configuration and requires external matching for adequate function. For improved performance an external LNA should be added as shown in Figure 2. Depending on the application it might be useful to consider additional filtering.

2.2 Gain block

A single stage differential amplifier follows the LNA providing further amplification and conversion from single-ended to differential signaling.

2.3 Mixer and low-pass filter

u-blox 7 receivers make use of a passive IQ mixer topology to convert the GNSS signals to a low intermediate frequency (IF). The following low-pass filters are designed to remove high-frequency mixing products from the I and Q signals. Their cut-off frequencies are adjustable to compensate IC process variation.

2.4 Programmable gain amplifier

The programmable gain amplifiers (PGA) are used to provide the ADCs with appropriate input levels. They make use of a four stage approach consisting of three variable gain stages. The PGA gain is adjusted by firmware based on the ADC output signal levels, providing an automatic gain control (AGC) for the receiver.

2.5 ADC

Two 5-bit ADCs are used for A/D conversion. The output signaling of the ADCs are differential I and Q signals, which are processed in the following baseband subsystem.

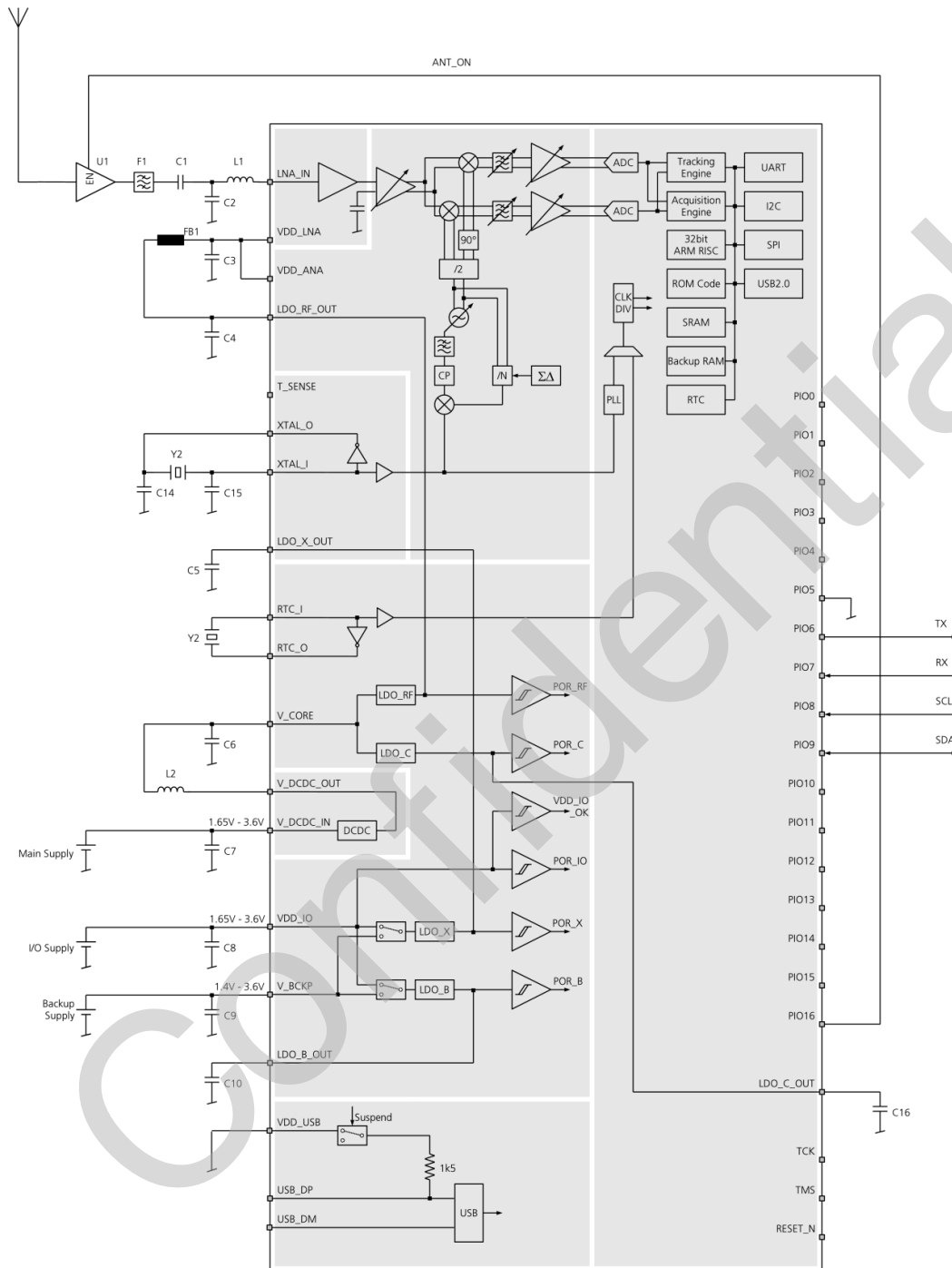


Figure 2: u-blox 7 RF and baseband subsystem

3 Baseband subsystem

The baseband subsystem integrates a Cortex-M3™ CPU and all the memory required for embedded firmware execution. Specific hardware required for signal acquisition and tracking and a wide selection of interfaces are provided. Analog functional blocks such as PLL, A/D converters and Power Management Unit (PMU) are fully integrated. u-blox 7's embedded firmware provides all the algorithms needed to calculate navigation data output.

Figure 3 shows the block diagram for the baseband section. Selected functional blocks are described in the following sections.

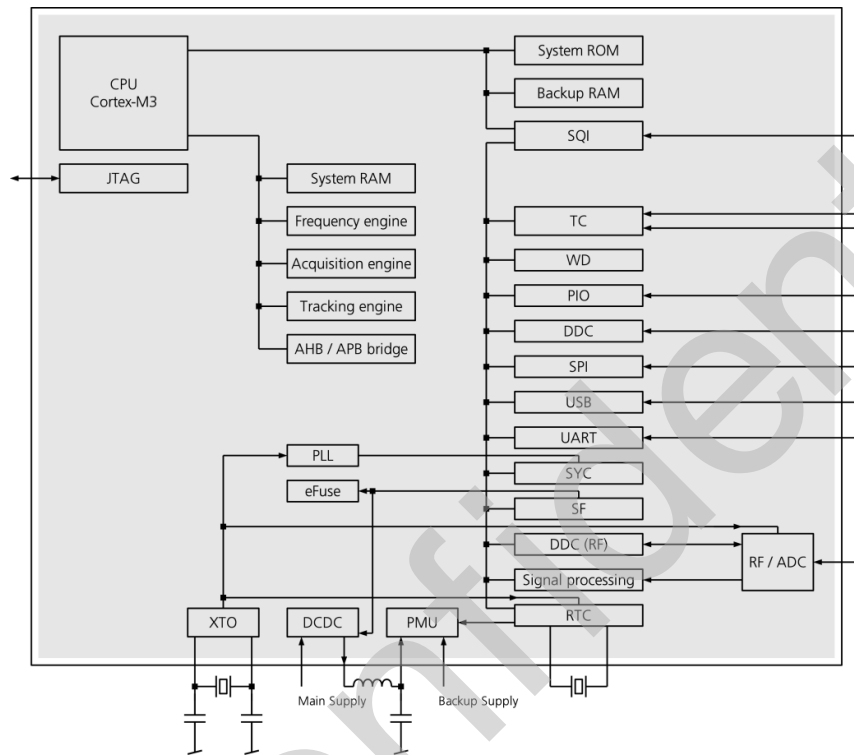


Figure 3: u-blox 7 baseband subsystem

3.1 GNSS processing engines

The acquisition and tracking engines are the main hardware components that perform the GNSS signal processing. Both engines are capable of removing residual carrier (Doppler) offset and perform correlation with GNSS codes.

Since acquisition and tracking functions are completely separate, the acquisition engine can be shut down completely when it's not needed. In turn, even if all channels of the tracking engine are fully loaded, the full power of the acquisition engine is at the disposal of the firmware.

Both engines feature dedicated memory blocks in order to keep silicon area and power consumption to a minimum. State-of-the-art clock management features allow adapting power consumption to the actual processing state of the firmware and its corresponding hardware needs.

Embedded firmware employs various strategies in order to make the best use of the two engines. The user may tune this strategy to a particular application by changing the configuration settings.

3.2 Interfaces

A number of interfaces are provided either for data communication or memory access. The embedded firmware uses these interfaces according to their respective protocol specifications. For specific applications, the firmware also supports the connection of peripheral devices, such as external memories or sensors, to some of the interfaces.



The digital I/Os of the baseband part are supplied with VDD_IO from the host system. The wide range of VDD_IO allows seamless interfacing to standard logic voltage levels independently of the baseband supply voltage level. However, in many applications VDD_IO will be simply connected to the main supply voltage. Without supplying VDD_IO, the system will be kept in reset state.

3.2.1 UART

The UBX-G7020 makes use of a UART interface, which can be used for communication to a host. It supports configurable baud rates. For supported baud rates see the u-blox 7 Receiver Description Including Protocol Specification [2].

3.2.2 USB

A USB version 2.0 FS (Full Speed, 12 Mb/s) interface can be used for communication as an alternative to the UART. The pull-up resistor on pin USB_DP is integrated to signal a full-speed device to the host. The VDD_USB pin supplies the USB interface.

3.2.3 SPI

The SPI interface is designed to allow communication to a host CPU. The interface can be operated in slave mode only. The maximum transfer rate using SPI is 6 Mb/s. Note that SPI is not available in the default configuration, because its pins are shared with the UART and DDC interfaces. The SPI interface can be enabled by connecting PIO10 to ground (see section 5.2.2). In this case the DDC interface for data communication is no longer available. The UART interface can be mapped to PIO15 and PIO16.

3.2.4 Display Data Channel (DDC)

An I²C compliant DDC interface is available for communication with an external host CPU. The interface can be operated in slave mode only. The DDC protocol and electrical interface are fully compatible with Fast-Mode of the I²C industry standard. Since the maximum SCL clock frequency is 400 kHz, thus the maximum transfer rate is 400 kb/s.

3.2.5 Serial Quad Interface (SQI)

The SQI is used to connect the UBX-G7020 with an external FLASH memory. The FLASH memory is required for firmware updates and for data logging. It can be used to store configurations and to save AssistNow Offline data.



For more information see the UBX—G7020 Hardware Integration Manual [1]

3.2.6 JTAG

The JTAG interface can be used for boundary scan testing. The UBX-G7020 provides two dedicated pins and two PIOs for this purpose. Both pins and PIOs are listed in Table 10.



For more information see the UBX—G7020 Hardware Integration Manual [1]

3.3 Peripheral Input Output (PIO)

The PIO block has two basic functions.

- It provides I/O pins for the interfaces. The configuration of the pins is determined by the dedicated interface.
- It allows the use of I/O pins as general-purpose I/O.



For more information see the UBX—G7020 Hardware Integration Manual [1]

3.4 Watchdog (WD)

u-blox 7 includes a Watchdog timer, that prevents system-lockups caused if the software gets trapped in a deadlock. During normal operation, the firmware resets the watchdog's internal counter at regular intervals before timer overflow occurs.

3.5 Timer Counter (TC)

Timer counter has two TIMEMARK inputs and two TIMEPULSE outputs.

TIMEMARK inputs (routed through EXTINT0 and EXTINT1) timestamp external events relative to GPS time.

TIMEPULSE outputs generate pulse trains synchronized with GPS or UTC time grid with intervals configurable over a wide frequency range. Thus one TIMEPULSE output may be used as a low frequency time synchronization pulse while the other is being used as a high frequency reference frequency.

All input and output signals are synchronized with the receiver internal clock frequency of 48 MHz, resulting in an inherent maximum quantization error of in- and output signals of +/- 10 ns.

3.6 Clock generation

3.6.1 Crystal and TCXO oscillator

The oscillator generates the proper reference for the RF and Baseband PLL respectively. The default clock frequency for UBX-G7020 is 26 MHz. One can choose an external crystal as frequency reference or an external TCXO for frequency generation. In the latter case the internal circuit is used as a buffer/driver amplifier for the TCXO. A TCXO allows accelerated weak signal acquisition; enabling faster start and reacquisition times. The crystal oscillator provides good performance in a cost effective solution and results in some power reduction compared to the TCXO. With UBX-G7020 an RTC replacement mode is introduced, where the 26 MHz crystal oscillator can also be used to provide a frequency reference to the RTC without using an additional crystal for the RTC. For this reason the clocking oscillator is supplied internally by a separate power domain called LDO_X, which can be powered via VDD_IO or V_BCKP.



The default clock frequency is 26 MHz, however, the firmware supports a wide selection range of reference frequencies as can be seen in the u-blox 7 Receiver Description Including Protocol Specification [2].

3.6.2 PLL

The fully integrated low-power fractional sigma-delta PLL generates the system frequency from a wide range of reference frequencies supplied by different crystal or TCXO oscillators. The PLL output frequency is programmable; maximum frequency is 96 MHz for both the system clock and the SQI clock. When power consumption is critical, the PLL can be disabled and the CPU runs directly from an external clock (RTC clock or direct clock input). When the USB device is connected, the PLL is enabled by the firmware in order to provide the USB interface with the required 48 MHz clock.

3.6.3 Real-Time Clock (RTC)

The RTC is driven by a 32 kHz oscillator, which makes use of an external RTC crystal. The signal for the RTC can also be internally derived from the 26 MHz crystal oscillator. If the main supply voltage fails and a battery is connected to V_BCKP, parts of the baseband section switch off, but the RTC still runs providing a timing reference for the receiver. This operating mode is called Hardware Backup Mode, which enables all relevant data to be saved in the backup RAM to later allow a hot or warm start.

The RTC crystal is optional, but it is required in Power Save Mode for optimized power consumption. In these cases, actual time is maintained in the RTC and Ephemeris and other last known data is kept in the backup RAM. In A-GPS based systems the RTC is not required, when coarse or fine time information is available from the network.



If neither backup RAM nor RTC are used, the backup battery backup battery is not needed and V_BCKP should be connected to VDD_IO.

3.7 Power Management Unit (PMU)

The PMU provides 4 power domains that are internally generated by LDOs and supervised by several voltage monitors:

1. Backup - the backup domain runs the RTC section and the backup memory. The backup domain provides three modes:
 - Run mode: when the voltage level at VDD_IO allows proper system operation.
 - SW backup mode: if the voltage at VDD_IO is still OK, but the LDOs for the other power domains are switched off by software command.
 - HW backup mode: when the voltage at VDD_IO fails, but an external battery is connected to V_BCKP. In this case the PMU will automatically switch off the remaining blocks but keeps RTC and backup memory alive.
2. Core - the core domain is the main power domain for the baseband subsystem. Its LDO_C can be connected directly to a main power supply via V_CORE or supplied by the built-in DC/DC converter.
3. RF - the RF domain supplies the RF subsystem. The LDO of the RF domain is called LDO_RF. Its input is internally connected to the input of LDO_C of the core domain (see Figure 2).
4. Clock - the clock domain supplies the oscillator. Its LDO_X may be supplied by either the main power supply connected to VDD_IO or an external backup battery connected to V_BCKP (see section 3.6.1).

3.7.1 DC/DC converter

u-blox 7 integrates a DC/DC converter, allowing reduced power consumption especially when using a main supply voltage above 2.5 V. To use the DC/DC converter the main power supply must be connected to V_DCDC_IN and a capacitor and an inductor must be added to connect V_DCDC_OUT to V_CORE as shown in Figure 2. If a converter is not used, connect V_DCDC_IN/V_DCDC_OUT to V_CORE.



For more information see the UBX—G7020 Hardware Integration Manual [1]

3.8 Memory

3.8.1 Backup RAM

u-blox 7 receivers include 32 kB internal backup RAM, which enables all relevant data to be saved in case of a power failure. Furthermore, it can be used to store configuration data. The backup RAM is also used as a cache for the SQI flash and as the main code RAM for the processor.

3.8.2 System RAM

u-blox 7 receivers use a 128 kB system RAM, which is shared by the processor for data access and by the UART and SPI DMA.

3.8.3 GNSS RAM

u-blox 7 receivers use a 128 kB GNSS RAM, which is used to share data between the acquisition and tracking engines. This memory can also be used by the processor, but with less efficiency.

3.8.4 Acquisition engine RAM

u-blox 7 receivers include a 56 kB dedicated RAM for the GNSS acquisition engine.

3.8.5 eFuse memory

With u-blox 7 a 1 kb eFuse memory is integrated to permanently save configuration settings. If no external FLASH memory is available the eFuse memory can also be used to store the low level configuration.

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4 Operating modes and power management

u-blox 7 technology offers a power optimized architecture with built-in autonomous power saving functions to minimize power consumption at any given time. Furthermore, the receiver can be operated in two operating modes for maximum performance or for optimized power consumption respectively. In addition a high efficiency DC/DC converter is integrated to allow low power consumption even for higher main supply voltages.

4.1 Operating modes

u-blox 7 chips have two operating modes:

- Continuous Mode for best GPS performance
- Power Save Mode to optimize power consumption

4.1.1 Continuous Mode

Continuous Mode uses the acquisition engine at full performance resulting in the shortest possible TTFF and the highest sensitivity. It searches for all possible satellites until the Almanac is completely downloaded. The receiver then switches to the tracking engine to lower power consumption.

Thus, a lower tracking current consumption level will be achieved when:

- A valid GPS position is obtained
- The entire Almanac has been downloaded
- The Ephemeris for each satellite in view is valid

4.1.2 Power Save Mode

For power sensitive applications u-blox 7 receivers provide a Power Save Mode for reduced power consumption.

Power Save Mode uses two dedicated operations called ON/OFF and Cyclic tracking, that reduce average current consumption in different ways to match the needs of the specific application. These operations can be set by using a specific ubx message.



For more information about power management strategies, see the u-blox 7 Receiver Description Including Protocol Specification [2].



Power Save Mode is not available in GLONASS mode.

4.2 Calculating power consumption

See the UBX—G7020 Hardware Integration Manual [1]

5 Configuration management

5.1 Configuration hierarchy

u-blox 7 receivers can be configured to meet the specific needs of the application. In a system reboot the stored configuration is loaded from different sources with the following hierarchy:

1. Present configuration in system RAM
2. Configuration in backup RAM
3. Configuration in SQI FLASH memory
4. Configuration by PIOs
5. Configuration in eFuse memory

5.2 Configuration by PIOs

To allow for smaller chip packages, UBX-G7020 chips have fewer boot time configuration pins than previous generations. Only two PIOs remain for applications using FLASH memory: PIO10 and PIO12. In this case the receiver must start in Safe Boot Mode and any change of the default hardware configuration must be set via eFuse before programming the FLASH memory (see Table 3). If no FLASH memory is used and PIO5 is set to low, then PIO0 to PIO4 become configuration pins for setting the hardware (HW) configuration at system startup.



All PIOs include an internal pull-up resistor.

5.2.1 PIO5 (CONFIG-SEL)

For applications without a FLASH memory, PIO5 must be set to low to change the default hardware configuration. In this case PIO0 to PIO4 become available as HW configuration pins.

PIO #	Default HW configuration	HW configuration if PIO is set to low	Remarks
0	Reserved	Reserved	
1	Reserved	Reserved	
2	DC/DC enabled	DC/DC disabled	
3	19 pF XTAL	Reserved	If PIO4 is left open
3	3.0 V TCXO	1.8 V TCXO	If PIO4 is connected to ground
4	XTAL	TCXO	

Table 3: HW configuration by PIOs including the default HW configuration




For more information about HW configuration see the UBX-G7020 Hardware Integration Manual [1].

5.2.2 PIO10 (D-SEL)

At startup the PIO10 pin determines which data interfaces are used for communication. If PIO10 is set high or is not connected, UART and DDC become available. If PIO10 is set low, i.e. connected to ground, the UBX-G7020 can communicate to a host via SPI.

PIO #	PIO10="high"	PIO10="low"
6	UART TX	SPI MISO
7	UART RX	SPI MOSI
8	DDC SCL	SPI CLK
9	DDC SDA	SPI CS_N

Table 4: Data interface selection by PIO10

 In case PIO10 is connected to ground the UART interface can still be available when remapped to PIO15 and PIO16 (see the u-blox 7 Receiver Description Including Protocol Specification [2]).

5.2.3 PIO12 (SBM-SEL)


If PIO12 is low at startup, the receiver enters Safe Boot Mode. In this mode the receiver does not calculate positioning data, but is set into a defined state that allows such actions as changing the low level configuration by eFuse, programming the FLASH memory in production, or recovering a corrupted FLASH memory.

5.3 Configuration by eFuse

New with u-blox 7 is the ability to use eFuse to change the default HW configuration, remap the PIOs, and store SW configuration settings. Table 5 lists the default function of the PIOs.

PIO #	Default Function	I/O	Remarks
0	SQI D0	I/O	Connect to external SQI FLASH memory, leave open if no FLASH is connected.
1	SQI D1	I/O	Connect to external SQI FLASH memory, leave open if no FLASH is connected.
2	SQI D2	I/O	Connect to external SQI FLASH memory, leave open if no FLASH is connected.
3	SQI D3	I/O	Connect to external SQI FLASH memory, leave open if no FLASH is connected.
4	SQI CLK	O	Connect to external SQI FLASH memory, leave open if no FLASH is connected.
5	SQI CS_N CONFIG_SEL	I/O	Connect to external SQI FLASH memory, leave open if no FLASH is connected. If connected low PIO0 to PIO4 become configuration pins
6	UART TX	O	UART transmit
7	UART RX	I	UART receive
8	DDC SCL	I	DDC serial clock
9	DDC SDA	I/O	DDC serial data line
10	D_SEL	I	Selects interfaces for communication
11	TIMEPULSE1	O	1PPS by default, but can be configured from 0.25 Hz to 10 MHz.
12	TIMEPULSE2 SAFEBOOT_N	I/O	1PPS by default, but can be configured from 0.25 Hz to 10 MHz. If connected low at startup, the receiver starts in SAFEBOOT Mode (see section 5.1.3)
13	EXTINT1	I	External Interrupt 1
14	EXTINT2	I	External Interrupt 2
15	ANT_OK	I	Antenna status from an external antenna supervisor circuit.
16	ANT_ON	O	Antenna on/off switch to an external antenna supervisor circuit or to power on and off an external LNA.

Table 5: Default function of the PIOs

 For more information about configuration using eFuse, see the u-blox 7 Receiver Description Including Protocol Specification [2].

6 Pin definition

6.1 Pin assignment

Section 6.1.1 shows the pin assignments. Most PIOs are configurable and have shared functions. Use special care when designing with these pins since the overall function of the device can be affected. The default configuration of the PIOs is listed in Table 5 .



For more information see the u-blox 7 Receiver Description Including Protocol Specification [2].

6.1.1 QFN40 (UBX-G7020-KT, UBX-G7020-KA)

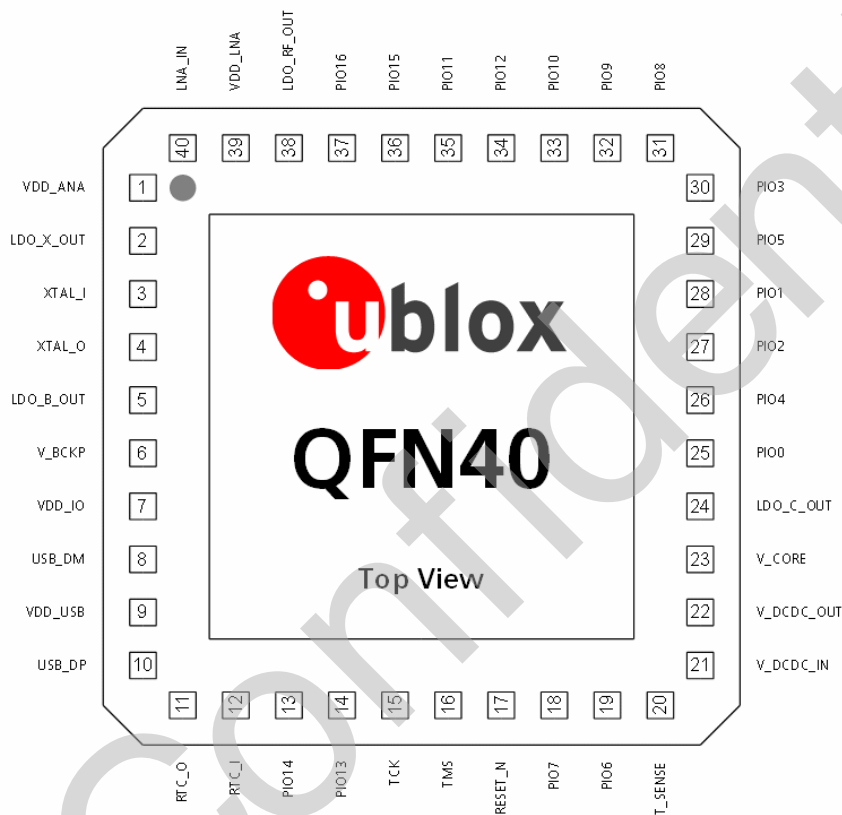


Figure 4: Pin assignment QFN40 (UBX-G7020-KT / UBX-G7020-KA)



For multiple function PIOs, select the specific signal by sending the specific configuration message or e-fusing.

6.2 Pin description

Name	Pin QFN40	Power Domain	I/O Reset	I/O Core off	Description
V_DCDC_IN	21	DC/DC	-	-	DC/DC Input
V_DCDC_OUT	22	DC/DC	-	-	DC/DC Output
V_CORE	23	Core	-	-	Main Core Supply
V_BCKP	6	Backup	-	-	Backup Cell Supply
VDD_IO	7	IO	-	-	I/O Ring Power Supply
VDD_USB	9	USB	-	-	USB Power Supply
VDD_ANA	1	RF	-	-	Analog Power Supply
VDD_LNA	39	RF/LNA	-	-	LNA Power Supply
LDO_RF_OUT	38	RF	-	-	RF Power Output (Capacitor to ground is required!)
LDO_C_OUT	24	Core	-	-	Core Power Output (Capacitor to ground is required!)
LDO_B_OUT	5	Backup	-	-	Backup Power Output (Capacitor to ground is required!)
LDO_X_OUT	2	Clock	-	-	Clock Power Output (Capacitor to ground is required!)

Table 6: Power Management

Name	Pin QFN40	Power Domain	I/O Reset	I/O Pwr off	Description
LNA_IN	40	RF/LNA	Input	Input	LNA Input (LNA requires an external input matching!)
XTAL_I	3	Clock	Input	Input	XTO Input
XTAL_O	4	Clock	Output	Output	XTO Output
RTC_I	12	Backup	Input	Input	RTC Input
RTC_O	11	Backup	Output	Output	RTC Output
T_SENSE	20	Clock	Input	Input	ADC Input (This pin is not supported with FW1.0!)

Table 7: System

Name	Pin QFN40	Power Domain	I/O Reset	I/O Pwr off	Description
VDD_USB	9	USB	-	-	USB Power Supply (see table 9)
USB_DP	10	USB	Input	Input	I/O Differential USB D+
USB_DM	8	USB	Input	Input	I/O Differential USB D-

Table 8: USB

Name	Pin QFN40	Power Domain	I/O Reset	I/O Pwr off	Description
TCK	15	IO	Input Pull-down	Input Pull-down	JTAG Test Clock Input
TMS	16	IO	Input Pull-up	Input Pull-up	JTAG Test Mode Select
PIO13 / TDI	14	IO	Input Pull-up	Input Pull-up	JTAG Test Data Input (TDI function is not provided by default. The PIO has to be remapped!)
PIO14 / TDO	13	IO	Input Pull-up	Input Pull-up	JTAG Test Data Output (TDO function is not provided by default. The PIO has to be remapped!)

Table 9: JTAG

Name	Pin QFN40	Power Domain	I/O Reset	I/O Pwr off	Description
PIO0	25	IO	Input Pull-up	Input Pull-up	I/O PIO0 or CFG-PIN
PIO1	28	IO	Input Pull-up	Input Pull-up	I/O PIO1 or CFG-PIN
PIO2	27	IO	Input Pull-up	Input Pull-up	I/O PIO2 or CFG-PIN
PIO3	30	IO	Input Pull-up	Input Pull-up	I/O PIO3 or CFG-PIN
PIO4	26	IO	Input Pull-up	Input Pull-up	I/O PIO4 or CFG-PIN
PIO5	29	IO	Input Pull-up	Input Pull-up	I/O PIO5 or CONFIG-SEL
PIO6	19	IO	Input Pull-up	Input Pull-up	I/O PIO6
PIO7	18	IO	Input Pull-up	Input Pull-up	I/O PIO7
PIO8	31	IO	Input Pull-up	Input Pull-up	I/O PIO8
PIO9	32	IO	Input Pull-up	Input Pull-up	I/O PIO9
PIO10	33	IO	Input Pull-up	Input Pull-up	D-SEL
PIO11	35	IO	Input Pull-up	Input Pull-up	I/O PIO11
PIO12	34	IO	Input Pull-up	Input Pull-up	I/O PIO12 and SBM-SEL
PIO13	14	IO	Input Pull-up	Input Pull-up	I/O PIO13
PIO14	13	IO	Input Pull-up	Input Pull-up	I/O PIO14
PIO15	36	IO	Input Pull-up	Input Pull-up	I/O PIO15
PIO16	36	IO	Input Pull-up	Input Pull-up	I/O PIO16

Table 10: PIOs

7 Electrical specification



The limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.



Where application information is given, it is advisory only and does not form part of the specification. For more information regarding power management see the UBX-G7020 Hardware Integration Manual [1].

7.1 Absolute maximum rating

Symbol	Parameter	Min.	Max.	Unit
V _{CORE} , V _{DCDC_IN} , V _{DCDC_OUT}	Supply voltage baseband main core and RF LDOs inputs Input voltage of the internal DC/DC converter Output voltage of the internal DC/DC converter	-0.5	3.6	V
VDD_IO	Supply voltage I/O ring	-0.5	3.6	V
VDD_USB	Supply voltage USB	-0.5	3.6	V
V _{BCKP}	Supply voltage baseband backup core and TCXO LDOs inputs	-0.5	3.6	V
VDD_ANA, VDD_LNA	Supply voltage RF front-end	-0.5	1.6	V
V _i	Input voltage on XTAL_I	-0.5	3.6	V
V _i _{ANA}	Input voltage on RTC_I	-0.5	1.6	V
V _i _{DIG}	Input voltage on PIO0-16, RESET_N, TCK and TMS	-0.5	3.6	V
Pr _{fin}	RF Input power on LNA_IN		+15	dBm
P _{tot}	Total power dissipation		500	mW
T _{jun}	Junction temperature	-40	+105	°C
T _s	Storage temperature	-40	+125	°C

Table 11: Absolute maximum ratings



Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection diodes.

7.2 Operating conditions



The test conditions specified in Table 13 apply to all characteristics defined in this section.

Symbol	Parameter	Min.	Typ.	Max.	Unit
Tamb	Ambient temperature	-40	+25	+85	°C
GND	Ground		0		V
LDO_RF_OUT, LDO_C_OUT, LDO_B_OUT, LDO_X_OUT	LDOs output voltage		1.2		V
V_CORE	Core supply voltage		3.3		V
V_BCKP	Backup battery supply voltage		3.3		V
VDD_IO	Supply voltage I/O ring		3.3		V
VDD_USB	Supply voltage USB		3.3		V
VDD_ANA, VDD_LNA	Supply voltages for RF front-end supplied by LDO_RF_OUT		1.2		V
Fref	Reference frequency		26		MHz

Table 12: Test conditions

7.2.1 DC electrical characteristic



For block diagrams of the Power Management Unit (PMU) see the UBX-G7020 Hardware Integration Manual [1].

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD_IO	Supply voltage I/O ring	1.65	3.3	3.6	V
VDD_USB	Supply voltage USB	3.0	3.3	3.6	V
V_CORE	Input voltage for LDO_C and LDO_RF	1.4	3.3	3.6	V
V_BCKP	Input voltage for LDO_B and LDO_X (backup mode)	1.4		3.6	V
VDD_IO	Input voltage for LDO_B and LDO_X (normal mode)	1.65		3.6	V
V_DCDC_IN	Input voltage for DC/DC converter	1.65		3.6	V

Table 13: Power supply pins

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
LDO_RF_OUT	LDO_RF output voltage		1.1	1.2	1.3	V
LDO_B_OUT	LDO_B output voltage		1.1	1.2	1.3	V
LDO_C_OUT	LDO_C output voltage		1.1	1.2	1.3	V
VDD_ANA	Power pin		1.1	1.2	1.3	V
VDD_LNA	Power pin		1.1	1.2	1.3	V
V_SWITCH_U	Min. voltage on VDD_IO to switch from V_BCKP to VDD_IO supply			1.42		V
V_SWITCH_I	Min. voltage on VDD_IO to switch from VDD_IO to V_BCKP supply			1.37		V
POR_B_U	Rising threshold value for LDO_B_OUT			1.18		V
POR_B_I	Falling threshold value for LDO_B_OUT			1.15		V
POR_C_U	Rising threshold value for LDO_C_OUT			1.18		V
POR_C_I	Falling threshold value for LDO_C_OUT			1.15		V
POR_IO_U	Rising threshold value for VDD_IO	0 – 1.65 V		1.54		V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
	configured by eFuse	1 – 2.7 V		2.44		
POR_IO_I	Falling threshold value for VDD_IO configured by eFuse	0 – 1.65 V 1 – 2.7 V		1.52 2.38		V
POR_RF_U	Rising threshold value for LDO_RF_OUT			1.12		V
POR_RF_I	Falling threshold value for LDO_RF_OUT			1.00		V
POR_X_U	Rising threshold value for LDO_X_OUT	3 V		2.94		V
POR_X_I	Falling threshold value for LDO_X_OUT	3 V		2.91		V

Table 14: Power management unit

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Ileak	Leakage current input pins			< 1		nA
Vil	Low level input voltage		0		0.2*VDD_IO	V
Vih	High level input voltage		0.7*VDD_IO		VDD_IO+0.5	V
Vol	Low level output voltage	Iol=4mA			0.4	V
Voh	High level output voltage	Ioh=4mA		VDD_IO -0.4		V
Rpu_iic	Pull-up resistor for PIO0-5,8,9, 11-14			11		kΩ
Rpu	Pull-up resistor			115		kΩ
Rpd	Pull-down resistor			98		kΩ

Table 15: Digital IO pins

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Ileak	Leakage current input pins				1	μA
Vil	Low level input voltage	VDD_USB >= 3.0 V	0		0.8	V
Vih	High level input voltage	VDD_USB >= 3.0 V	2.0		VDD_USB	V
Vol	Low level output voltage	R _L = 1.425 kΩ to VDD_USB, VDD_USB >= 3.0 V, 22 Ω external series resistor			0.3	V
Voh	High level output voltage	R _L = 14.25 kΩ to GND, VDD_USB >= 3.0, 22 Ω external series resistor	2.8			V
Rpui	Pull-up resistor, Idle State		870	900	950	Ω
Rpuo	Pull-up resistor, Operational State		1400	1490	1600	Ω

Table 16: USB pins

7.2.2 Baseband AC parameters

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
RTC_Fxtal	RTC crystal resonant frequency			32768		Hz
RTC_T_start	RTC startup time		0.2	0.35	0.9	sec
RTC_losc	32KHz OSC current source			1		μA
RTC_Drive	32KHz OSC drive level	ESR = 80 kΩ		TBD		nW
RTC_Amp	32KHz OSC oscillation amplitude	ESR = 80 kΩ	50		350	mVpp
RTC_ESR	32KHz Xtal equivalent series resistance				80	kΩ
RTC_CL	RTC integrated load capacitance	ESR = 80 kΩ	4	7	12	pF
TCXO_Freq	TCXO frequency			26		MHz
TCXO_IN_VPP	TCXO input peak-to-peak voltage		0.8			V _{pp}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Xtal_Freq	XTO frequency			26		MHz
XTAL_Drive	XTAL drive Level	@26 MHz, 12 Ohm < ESR < 60 Ohm	5	20	60	μW
DCDC_eff	DC/DC efficiency	@3.3 input V, 4-80mA, External components L=0.47 uH, C=4.7uF	85			%
DCDC_out	DC/DC output voltage	DCDC enabled, bypass inactive		1.4		V
T_SENSE_freq	Measurement ADC delta-sigma frequency			500		kHz
T_SENSE_IH	Measurement ADC high current for ΔVbe			320		μA
T_SENSE_IL	Measurement ADC low current for ΔVbe			10		μA
T_SENSE_Acc	Measurement ADC accuracy	JTM trimmed at 60°C	-2.5		2.5	°C

Table 17: Baseband AC parameters

7.2.3 RF AC parameters⁷

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fin	Receiver input frequency		1550	1575.42	1650	MHz
NFtot	Receiver chain noise figure			TBD		dB
LNA_S11	LNA input return loss	50 Ohm environment		-10		dB
Ext_Gain	External gain before LNA_IN	50 Ohm environment			30	dB
Input_P1dB	Input 1dB compression point of the down-conversion chain @880 MHz @1575.42 MHz @1710 MHz @1920 MHz	50 Ohm input, ADC output, 60dB voltage gain		TBD TBD TBD TBD		dBm
Input_IP3	Input 3 rd order intercept point of the down-conversion chain IIP3 @880 MHz @1575.42 MHz @1710 MHz @1920 MHz	50 Ohm input, ADC output, 60dB voltage gain		TBD TBD TBD TBD		dBm

Table 18: RF AC parameters
⁷ Measured with an external matching

7.2.4 Power consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{BCKP}	V_BCKP backup current using the RTC crystal	HW Backup mode LDO_B_OUT=1.2V, VDD_IO=V_CORE=0V		12		μA
I_{BCKP}	V_BCKP backup current using the 26MHz XTO in RTC replacement mode	HW Backup mode LDO_B_OUT=1.2V, VDD_IO=V_CORE=0V		85		μA
I_{VDD_IO}	VDD_IO backup current using the RTC crystal	SW Backup mode LDO_B_OUT=1.2V, VDD_IO=V_CORE = 3V, LDO_C_OUT=LDO_RF_OUT= LDO_X_OUT=0V		17		μA
I_{VDD_IO}	VDD_IO backup current using the 26MHz XTO in RTC replacement mode	SW Backup mode LDO_B_OUT=1.2V, VDD_IO=V_CORE = 3V, LDO_C_OUT=LDO_RF_OUT= LDO_X_OUT=0V		90		μA
I_{SLEEP}	V_CORE sleep core current	Sleep mode, LDO_C_OUT=LDO_RF_OUT = 1.2V		125		μA

Table 19: Power Consumption



All values in Table 19 are measured at 25°C ambient temperature.

7.3 Indicative power requirements

Table 21 lists examples of the total system supply current including RF and baseband section for a possible application.



Values in Table 21 are provided for customer information only as an example of typical power requirements. Values are characterized on samples, actual power requirements can vary depending on FW version used, external circuitry, number of SVs tracked, signal strength, type of start as well as time, duration and conditions of test.

Parameter	Min	Typ	Max	Unit
Peak supply current			TBD	mA
Sustained supply current ⁸	Acquisition	TBD		mA
	Tracking (Continuous Mode) ⁹	15		mA
	Tracking (Power Save Mode) ⁹	TBD		mA

Table 20: Indicative power requirements

For more information about power requirements, see the UBX-G7020 Hardware Integration Manual [1].

⁸ 3.3V DC/DC converter used to supply V_CORE. Use this figure to determine required battery capacity.

⁹ With strong signals, all orbits available. For cold starts typical 12 min after First Fix. For hot starts typical 15 sec after First Fix. Power Save Mode at 1 fix/s.

7.4 SPI timing diagrams

In order to avoid incorrect operation of the SPI, the user needs to comply with certain timing conditions. The following signals need to be considered for timing constraints:

Symbol	Description
SPI CS_N (SS_N)	Slave select signal
SPI CLK (SCK)	Slave clock signal

Table 21: Symbol description



Figure 5: SPI timing diagram

7.4.1 Timing recommendations

The recommendations below are based on a firmware running from Flash memory.

Parameter	Description	Recommendation
t_{INIT}	Initialization Time	500 μ s
t_{DES}	Deselect Time	1 ms.
Bit rate		1 Mb/s

Table 22: SPI timing recommendations



The values in the above table result from the requirement of an error-free transmission. By allowing just a few errors and disabling the glitch filter, the bit rate can be increased considerably.

7.5 DDC timing diagrams

The DDC interface is I²C Fast Mode compliant. For timing parameters consult the I²C standard.



The maximum bit rate is 400 kb/s. The interface stretches the clock when slowed down when serving interrupts, so real bit rates may be slightly lower.

8 Mechanical specification

8.1 QFN40 / UBX-G7020-KT, UBX-G7020-KA

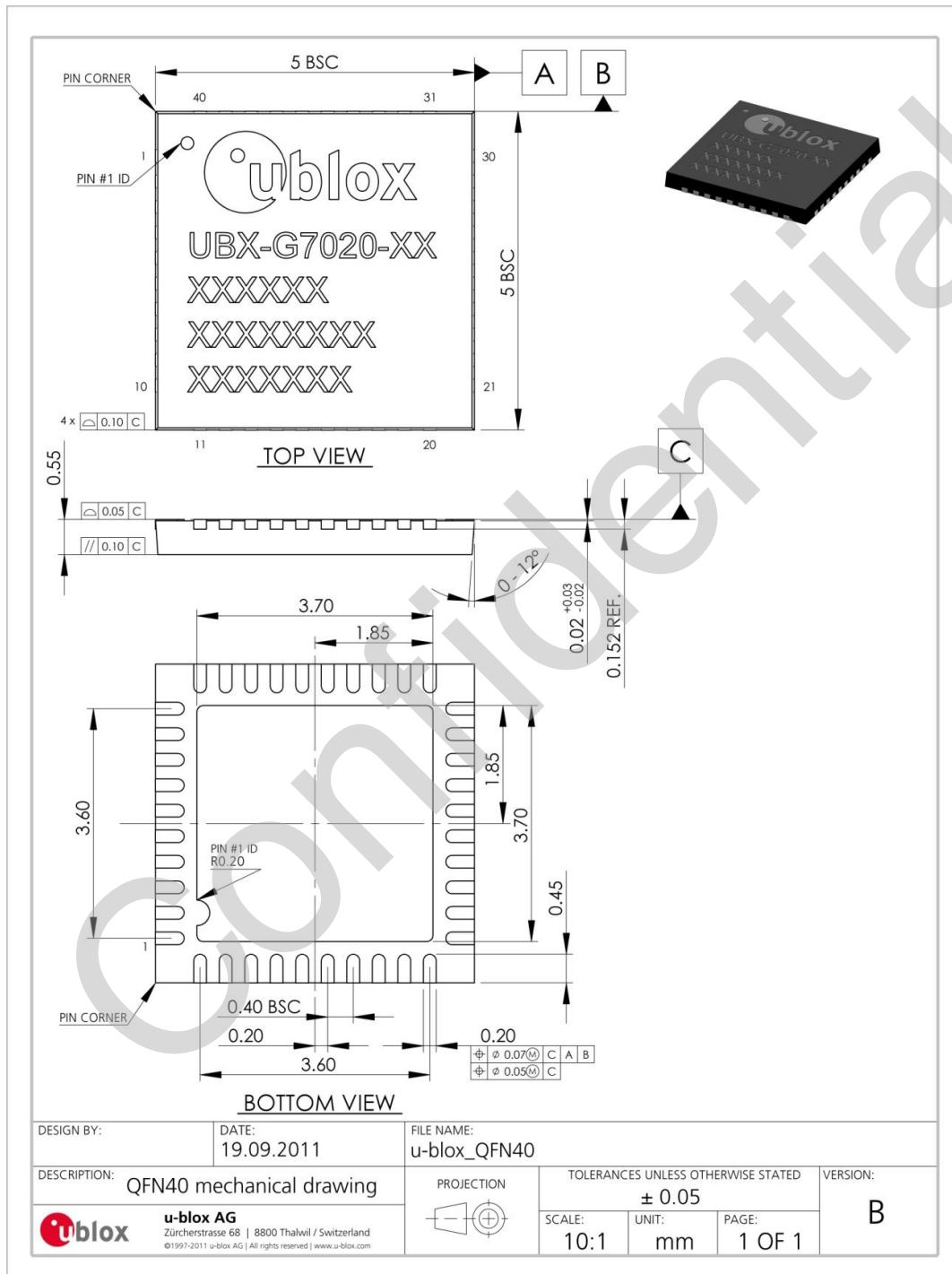


Figure 6: u-blox 7 mechanical drawing for QFN40

9 Reliability tests and approvals

9.1 Reliability tests

Qualifications requirements according to AEC-Q100 "Failure Mechanism Based Stress Test Qualification For Integrated Circuits" and appropriate JEDEC standards e.g. JESD47 "Stress-Test-Driven Qualification of Integrated Circuits"

9.2 Approvals



Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

UBX-G7020-CT, UBX-G7020-KT, and UBX-G7020-KA are RoHS compliant and green (no halogens).

10 Product handling

10.1 Packaging

UBX-G7020 chips are delivered as hermetically sealed, reeled tapes in order to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the u-blox Package Information Guide [4].



Figure 7: Reeled u-blox chips

10.1.1 Reels

UBX-G7020 chips are deliverable in quantities of 2000pcs on a reel, they are delivered using reel Type A as described in the u-blox Package Information Guide [4].

Parameter	Specification
Reel Type	A
Delivery Quantity	2000

Table 24: Reel information for UBX-G7020 chips

IC Package	Tape Width	Flange Combination
QFN40	16 mm	8 mm + 8 mm

Table 25: Reel composition of two halves

10.1.2 Tapes

Figure 10 shows the feed direction and illustrates the orientation of the UBX-G7020 chips on the reel: The chips are placed such that the pin 1 is at the upper left.

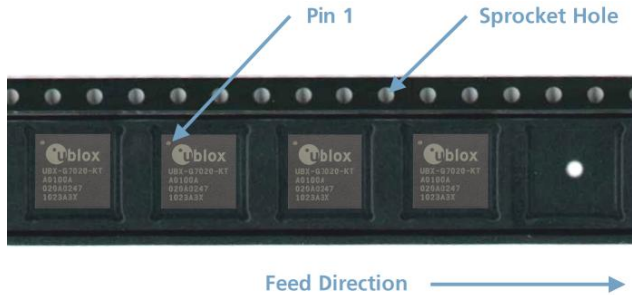


Figure 8: Orientation of UBX-G7020 chips on the tape

The dimensions of the tapes for UBX-G7020 chips are specified in Figure 11 (measurements in mm).

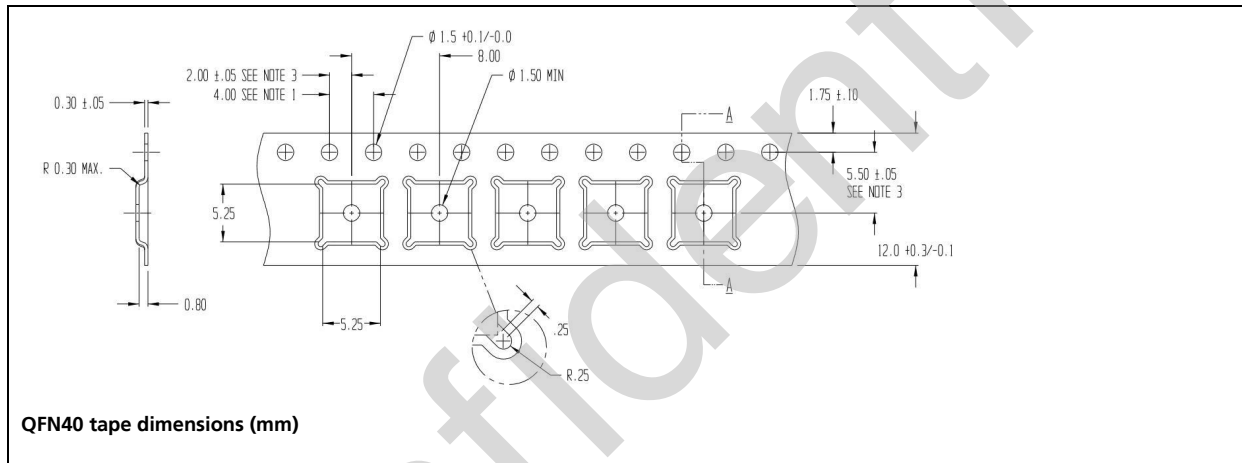


Figure 9: UBX-G7020 tape dimensions (mm)

10.2 Moisture Sensitivity Levels

The Moisture Sensitivity Levels (MSL) for UBX-G7020 chips are specified in Table 27. For more information regarding moisture sensitivity levels, labeling, storage and drying see the u-blox Package Information Guide [4].

Package	MSL Level
QFN40	1

Table 26: MSL levels



For MSL standard see IPC/JEDEC J-STD-020, which can be downloaded from www.jedec.org.

10.3 ESD handling precautions



UBX-G7020 chips contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Observe precautions for handling! Failure to observe these precautions can result in severe damage to the GPS receiver!

11 Default messages

Interface	Settings
UART Output	9600 Baud, 8 bits, no parity bit, 1 stop bit Configured to transmit both NMEA and UBX protocols, but only following NMEA and no UBX messages have been activated at start-up: TBD
USB Output	Configured to transmit both NMEA and UBX protocols, but only following NMEA and no UBX messages have been activated at start-up: TBD USB Power Mode: Bus Powered
UART Input	9600 Baud, 8 bits, no parity bit, 1 stop bit, Autobauding disabled Automatically accepts following protocols without need of explicit configuration: UBX, NMEA The GPS receiver supports interleaved UBX and NMEA messages.
USB Input	Automatically accepts following protocols without need of explicit configuration: UBX, NMEA The GPS receiver supports interleaved UBX and NMEA messages. USB Power Mode: Bus Powered

Table 27: Default messages



Please refer to the u-blox 7 Receiver Description Including Protocol Specification [2] for information about further settings.

12 Labeling and ordering information

12.1 Product labeling

12.1.1 QFN40

QFN40 semiconductor products provide 4 lines of text:

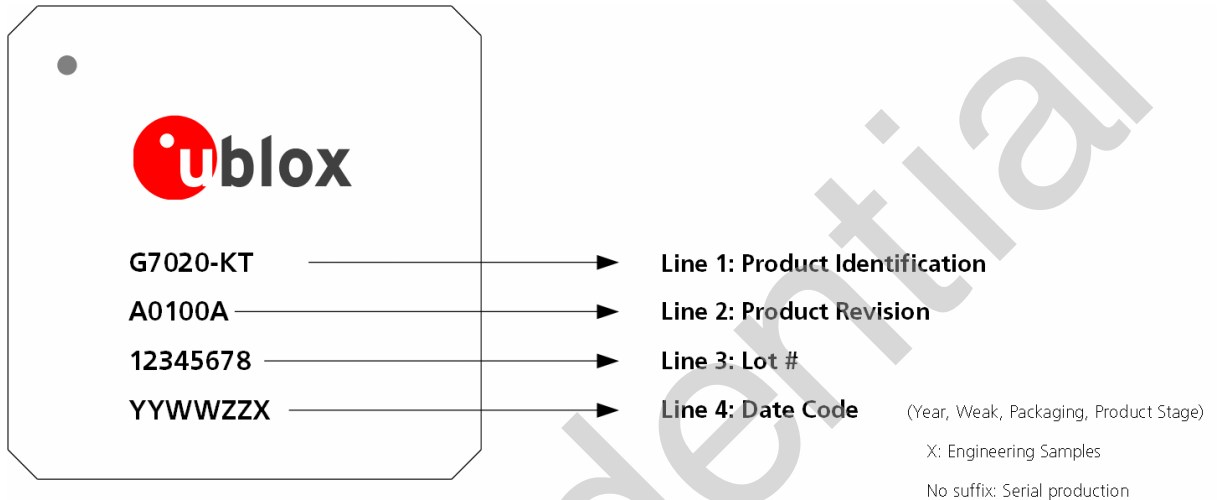


Figure 10: Description of QFN product label

12.2 Explanation of product codes

3 different product code formats are used. The **Product Name** is used in documentation such as this datasheet and identifies all u-blox 7 products, independent of packaging and quality grade. The **Ordering Code** includes packaging and quality, while the **Type Number** includes the hardware and firmware versions. Table 29 below details these 3 different formats:

Format	Structure
Product Name	Gmmnn
Ordering Code	UBX-Gmmnn-PT-VV
Type Number	UBX-Gmmnn-PT-RffooS

Table 28: Product code formats

The parts of the product code are explained in Table 30.

Code	Meaning	Example
UBX	u-blox	
G	GNSS Product	
mm	Baseband	70 = u-blox 7 BB section
nn	RF	20 = u-blox 7 RF section
P	Package Type	C = WL-CSP50 K = QFN40
T	Quality grade	T = Standard A = Automotive
VV	Optional chip variant	
R	Baseband Hardware Revision	Increasing Alphabetic Character
ff	Firmware Revision	Increasing Number
oo	eFuse revision	Increasing Number
S	RF Hardware Revision	Increasing Alphabetic Character

Table 29: part identification code

12.3 Ordering codes

Ordering No.	Product
UBX-G7020-KT	u-blox 7 GPS/GNSS Receiver, 40 Pin QFN

Table 30: Product ordering codes for standard grade chips

Ordering No.	Product
UBX-G7020-KA	u-blox 7 GPS/GNSS Receiver, 40 Pin QFN

Table 31: Product ordering codes for automotive grade chip



Product changes affecting form, fit or function are documented by u-blox. For a list of Product Change Notifications (PCNs) see our website at: <http://www.u-blox.com/en/notifications.html>.

Related documents

- [1] UBX-G7020 Hardware Integration Manual, Docu. No. GPS.G7-HW-10003
- [2] u-blox 7 Receiver Description Including Protocol Specification (confidential version), Docu. No. GPS.G7-SW-xxxx
- [3] u-blox 7 Receiver Description Including Protocol Specification (public version), Docu. No. GPS.G7-SW-xxxx
- [4] u-blox Package Information Guide, Docu. No. GPS-X-11004

For complete contact information visit us at www.u-blox.com

Revision history

Revision	Date	Name	Status / Comments
-	1/20/2012	ffel	Initial release
1	1/27/2012	ffel	Updated Table 3 and Figure 3.

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