Void Functions

Verilog makes a very clear differentiation between tasks and functions. The most important difference is that a task can consume time, whereas a function cannot. A function cannot have a delay.

a System Verilog task that does not consume time, you should make it a void function,which is a function that does not return a value.Now it can be called from any task or function.

Void function syntax:

```
function void print_method();
        $display("state = %s", cur state.name());
endfunction
```

Note:- void function means(function with no return value).

```
module void_function;
 int x;
 //void function to display current simulation time
 function void print_state();
  $display("\tCurrent simulation time is %0d\n",$time);
 endfunction

 initial begin
  #5;
  current_time();
  #15;
  current_time();
 end
endmodule
```

System Verilog function can be,

Static function: Static functions share the same storage space for all function calls.
Automatic function: Automatic functions allocate unique, stacked storage for each function call.