USB Power Delivery ENGINEERING CHANGE NOTICE

Title: PPS Current Requirements above Nominal Prog Voltage
Applied to: USB Power Delivery Specification Revision 3.0 Version 1.1

Brief description of the functional changes proposed:
Propose to allow PPS modes (5V Prog, 9V Prog, 15V Prog and 20V Prog) to reduce current in the range above the nominal Prog voltage proportionally to the PDP wattage associated with the charger rating. For example, if the charger is rated for 27W PDP and has negotiated a 9V Prog @ 3 A contract with the Sink, the current of the Source is allowed to reduce as voltage increases from 9 V to 11 V proportionally as defined by PDP/output voltage. The change is proposed as an acceptable current range, the high end defined by the nominal amperage defined by PDP/nominal Prog voltage, low end defined by PDP/output voltage at the time of measurement. For clarity, renames "Current Foldback" to "Current Limit". Replaces Figure 7-7 to clarify the behavior in Current Limit mode.

Benefits as a result of the proposed changes:
Allows power supply design to nominally align with the PDP rating as opposed to requiring the design to scale well beyond PDP, for example this would allow a PDP 27W implementation of 9V Prog to remain at 27 W at the high end of the voltage range (11 V) as opposed to requiring it to supply 3 A @ 11 V = 33 W.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
Existing designs will still comply, provides a wider acceptable range for future designs.

An analysis of the hardware implications:
Eases design performance requirements for Sources … presumes that at the higher end of the voltage range, that the charging profiles for mobile charging will not be degraded by maintaining a profile no greater than the PDP rating.

An analysis of the software implications:
None

An analysis of the compliance testing implications:
Compliance testing will remain fundamentally the same, simply with a wider acceptable range on current measurement in the voltage range from nominal Prog voltage up to the maximum voltage of the Prog mode range.

USB Power Delivery ENGINEERING CHANGE NOTICE

Actual Change Requested

(a). Apply to entire document

From/To Text:

This applies to the entire document including text, figures, tables and notes.

CF → CL

Current foldback → Current Limit.

'Cf' used within parameter name to 'CL'

(b). Section 1.6 Table 1-1

From Text:

Sink Directed Charge	A charging scheme whereby the Sink connects the Source to its battery through safety and other circuitry. Sink Directed Charge has two different modes of operation: • When the Current Foldback feature is not activated, the Sink controls the Source's output current by adjusting the Source's output voltage • When the Current Foldback feature is activated, the Source automatically controls its output current by adjusting its output voltage. The Sink is responsible for managing the current so as not to exceed the advertised capability of the Source and to protect itself from over-current events.

To Text:

Sink Directed Charge	A charging scheme whereby the Sink connects the Source to its battery through safety and other circuitry. When the Current Limit feature is activated, the Source automatically controls its output current by adjusting its output voltage.

(c). Section 6.4.1.2.5

From Text:

6.4.1.2.5 Programmable Power Supply Augmented Power Data Object

Table 6-13 below describes a Programmable Power Supply (1100b) APDO for a Source. See Section 7.1.3 for the electrical requirements of the power supply. This APDO is used primarily for Sink Directed Charge of a Battery in the Sink. When applying a current to the Battery greater than the cable supports, a high efficiency fixed scaler ***May*** be used in the Sink to reduce the cable current.

The voltage fields define the output voltage range over which the power supply ***Shall*** be adjustable in 20mV steps. The Maximum Current field contains the current the Programmable Power Supply ***Shall*** be capable of delivering over the advertised voltage range.

Table 6-13 Programmable Power Supply APDO - Source

Bit(s)	Description
B31…30	11b – Augmented Power Data Object (APDO)
B29…28	00b – Programmable Power Supply 01b…11b - ***Reserved***, ***Shall Not*** be used
B27…25	***Reserved*** – ***Shall*** be set to zero
B24…17	Maximum Voltage in 100mV increments
B16	***Reserved*** – ***Shall*** be set to zero
B15…8	Minimum Voltage in 100mV increments
B7	***Reserved*** – ***Shall*** be set to zero
B6…0	Maximum Current in 50mA increments

To Text:

6.4.1.2.5 Programmable Power Supply Augmented Power Data Object

Table 6-13 below describes a Programmable Power Supply (1100b) APDO for a Source. See Section 7.1.3 for the electrical requirements of the power supply. This APDO is used primarily for Sink Directed Charge of a Battery in the Sink. When applying a current to the Battery greater than the cable supports, a high efficiency fixed scaler ***May*** be used in the Sink to reduce the cable current.

The voltage fields define the output voltage range over which the power supply ***Shall*** be adjustable in 20mV steps. The Maximum Current field contains the current the Programmable Power Supply ***Shall*** be capable of delivering over the advertised voltage range.

Table 6-13 Programmable Power Supply APDO - Source

Bit(s)	Description
B31…30	11b – Augmented Power Data Object (APDO)
B29…28	00b – Programmable Power Supply 01b…11b - ***Reserved***, ***Shall Not*** be used
B27	PPS Power Limited
B26…25	***Reserved*** – ***Shall*** be set to zero
B24…17	Maximum Voltage in 100mV increments
B16	***Reserved*** – ***Shall*** be set to zero
B15…8	Minimum Voltage in 100mV increments
B7	***Reserved*** – ***Shall*** be set to zero
B6…0	Maximum Current in 50mA increments

6.4.1.2.5.1 PPS Power Limited

When the PPS Power Limited bit is set, the PPS Source ***Shall Not*** supply power that exceeds the Source's rated PDP. If the requested Output Voltage in the RDO exceeds the nominal Prog voltage (e.g. 5V for the 5VProg), the PPS ***Shall*** limit its output current so that the product the requested Output Voltage in the RDO times the actual current it delivers is less than or equal to the PDP. The PPS Source ***Shall Not*** reject an RDO that would exceed the PDP so long as the Output Voltage and Output Current do not exceed the Maximum Voltage and Maximum Current in the APDO. A PPS Source that sets the Power Output Limited bit is responsible to automatically limit the its output current so as not to exceed its PDP (See Figure 7-7).

When the PPS Power Limited bit is cleared, the PPS Source ***Shall*** deliver the Maximum Current up to the Maximum Voltage as advertised in its APDO.

(d). Sections 7.1.4.4

From Text:

7.1.4.4 Programmable Power Supply Current Foldback

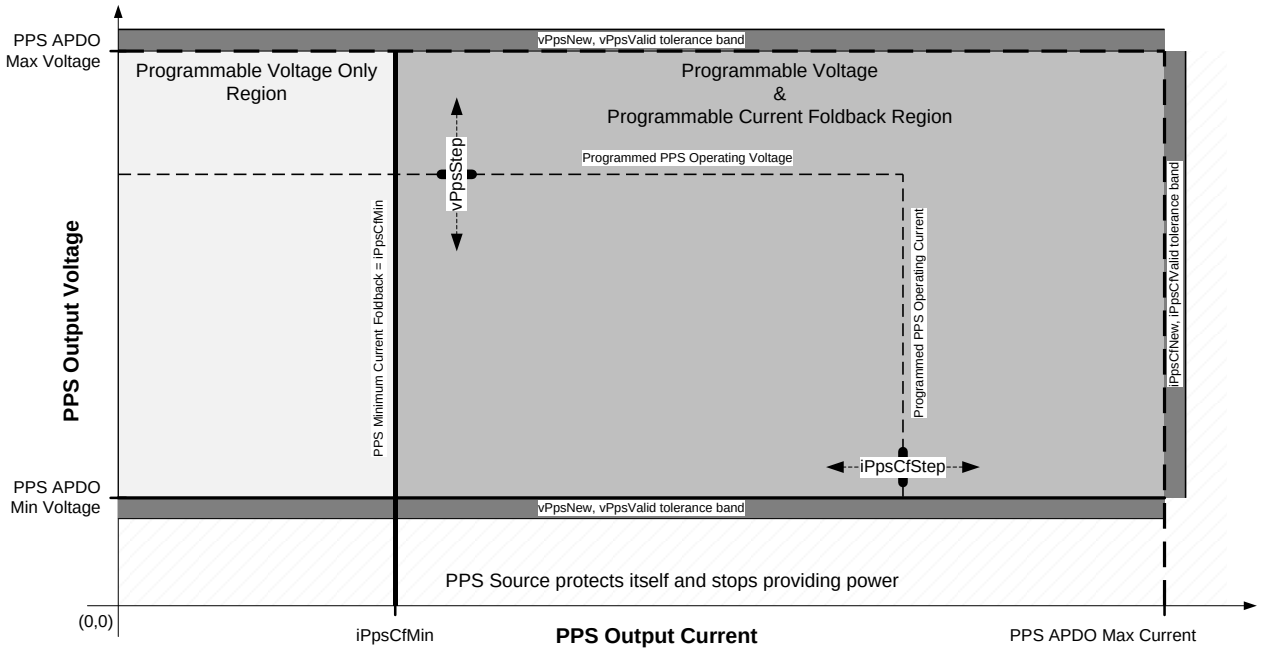
The Programmable Power Supply ***Shall*** foldback its output current to the Operating Current value in the Programmable RDO when the Sink attempts to draw more current than the Output Current level. The programming step size for the Output Current is ***iPpsCfStep***. All programming changes of the Operating Current ***Shall*** settle to the new Operating Current value within ***tPpsCfProgramSettle***. The PPS Operating Current regulation accuracy during current foldback is defined as ***iPpsCfNew***. The minimum programmable foldback level is ***iPpsCfMin***. A Source that supports PPS ***Shall*** support foldback programmability between ***iPpsCfMin*** and the Maximum Current value in the PPS APDO.

Any current overshoot or undershoot that occurs due to a load change during Current Foldback ***Shall Not*** exceed ***iPpsCfTransient*** and ***Shall*** settle to the Operating Current value within ***tPpsCfSettle***. Voltage overshoot or undershoot caused by a transition from Current Foldback mode to Constant Voltage mode ***Shall Not*** exceed ***vPpsCfCvTransient*** and ***Shall*** settle to the Operating Voltage value within ***tPpsCfCvTransient***. Likewise, current overshoot or undershoot caused by a transition from Constant Voltage mode to Current Foldback mode ***Shall Not*** exceed ***iPpsCvCfTransient*** and ***Shall*** settle to the Operating Current value within ***tPpsCvCfTransient***.

The PPS ***Shall*** maintain its output voltage within the Minimum Voltage and Maximum Voltage values advertised in the PPS APDO for all static and dynamic load conditions during Current Foldback operation. The PPS is not expected to deliver power if the load condition results in an output voltage that is lower than the Minimum Voltage value advertised in the PPS APDO. Rather, the Source ***Shall*** send ***Hard Reset*** Signaling and discharge V_{BUS} to ***vSafe0V*** then resume default operation at ***vSafe5V***.

The relationship between PPS programmable output voltage and PPS programmable Current Foldback ***Shall*** be as shown in Figure 7-7.

Figure 7-7 PPS Programmable Voltage and Foldback



To Text:

7.1.4.4 Programmable Power Supply Current Limit

The Programmable Power Supply ***Shall*** limit its output current to the Operating Current value in the Programmable RDO when the Sink attempts to draw more current than the Output Current level. The programming step size for the Output Current is ***iPpsCLStep***. All programming changes of the Operating Current ***Shall*** settle to the new Operating Current value within ***tPpsCLProgramSettle***. The PPS Operating Current regulation accuracy during Current Limit is defined as ***iPpsCLNew***. The minimum programmable Operating Current level in the RDO is ***iPpsCLMin***. A Source that supports PPS ***Shall*** support Current Limit programmability between ***iPpsCLMin*** and the Maximum Current value in the PPS APDO.

Any current overshoot or undershoot that occurs due to a load change during Current Limit ***Shall Not*** exceed ***iPpsCLTransient*** and ***Shall*** settle to the Operating Current value within ***tPpsCLSettle***. Voltage overshoot or undershoot caused by a transition from Current Limit mode to Constant Voltage mode ***Shall Not*** exceed ***vPpsCLCVTransient*** and ***Shall*** settle to the Operating Voltage value within ***tPpsCLCVTransient***. Likewise, current overshoot or undershoot caused by a transition from Constant Voltage mode to Current Limit mode ***Shall Not*** exceed ***iPpsCVCLTransient*** and ***Shall*** settle to the Operating Current value within ***tPpsCVCLTransient***.

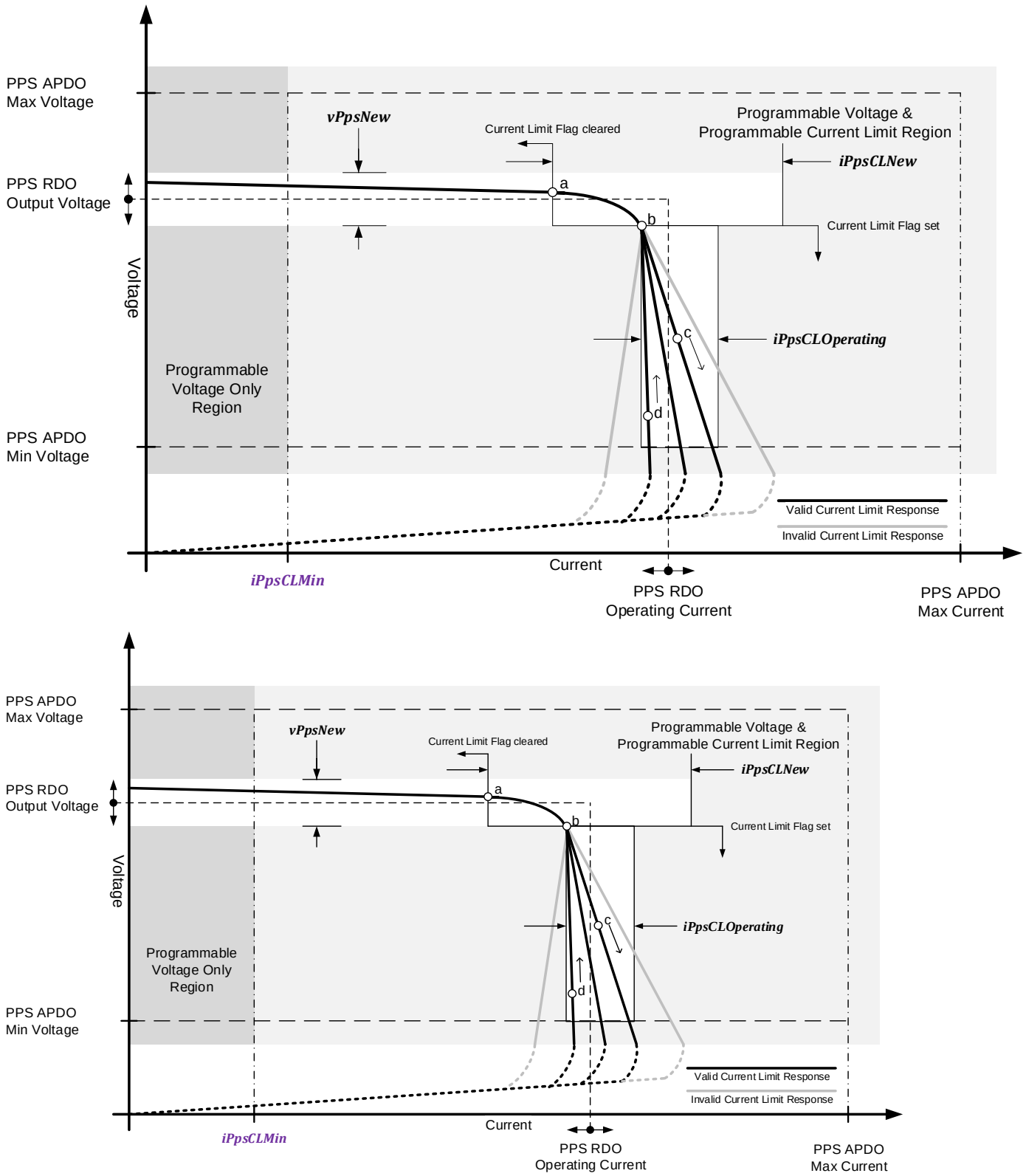
The PPS ***Shall*** maintain its output voltage within the Minimum Voltage and Maximum Voltage values advertised in the PPS APDO for all static and dynamic load conditions during Current Limit operation. The PPS is not expected to deliver power if the load condition results in an output voltage that is lower than the Minimum Voltage value advertised in the PPS APDO. Rather, the Source ***Shall*** send ***Hard Reset*** Signaling and discharge V_{BUS} to ***vSafe0V*** then resume default operation at ***vSafe5V***.

When the Sink attempts to draw more current than the Operating Current in the RDO, the Source ***Shall*** limit its output current. The current available from the Source during Current Limit mode ***Shall*** meet ***iPpsCLNew*** plus ***iPpsCLOperating***. The Sink ***May Not*** reduce its Operating Current request in the RDO when the Current Limit Flag is set.

Current limiting ***Shall*** be performed by the PPS Source. Sinks ***May Not*** limit their input current with respect to the RDO but ***Shall*** meet the requirements of Section 7.2.9. The Source ***Shall Not*** shutdown or otherwise disrupt the available output power while in Current Limit mode unless another protection mechanism as outlined in Section 7.1.7 is engaged to protect the Source from damage.

The relationship between PPS programmable output voltage and PPS programmable Current Limit ***Shall*** be as shown in Figure 7-7. The transition between the Constant Voltage mode and the Current Limit mode occurs between points *a* and *b*. The Current Limit Flag shall be set or cleared within this region. In Current Limit mode when the load resistance decreases the output current of the Source shall never decrease nor increase more than iPpsCLOperating. The proper behavior is represented by *c*. Likewise, as the load resistance increases, the output current of the Source ***Shall Not*** increase. The proper behavior is represented by *d*.

Figure 7-7 PPS Programmable Voltage and Current Limit[RP-M1]



Notes:

1. Point *a* represents entry into the transition region between Constant Voltage mode and Current Limit mode.

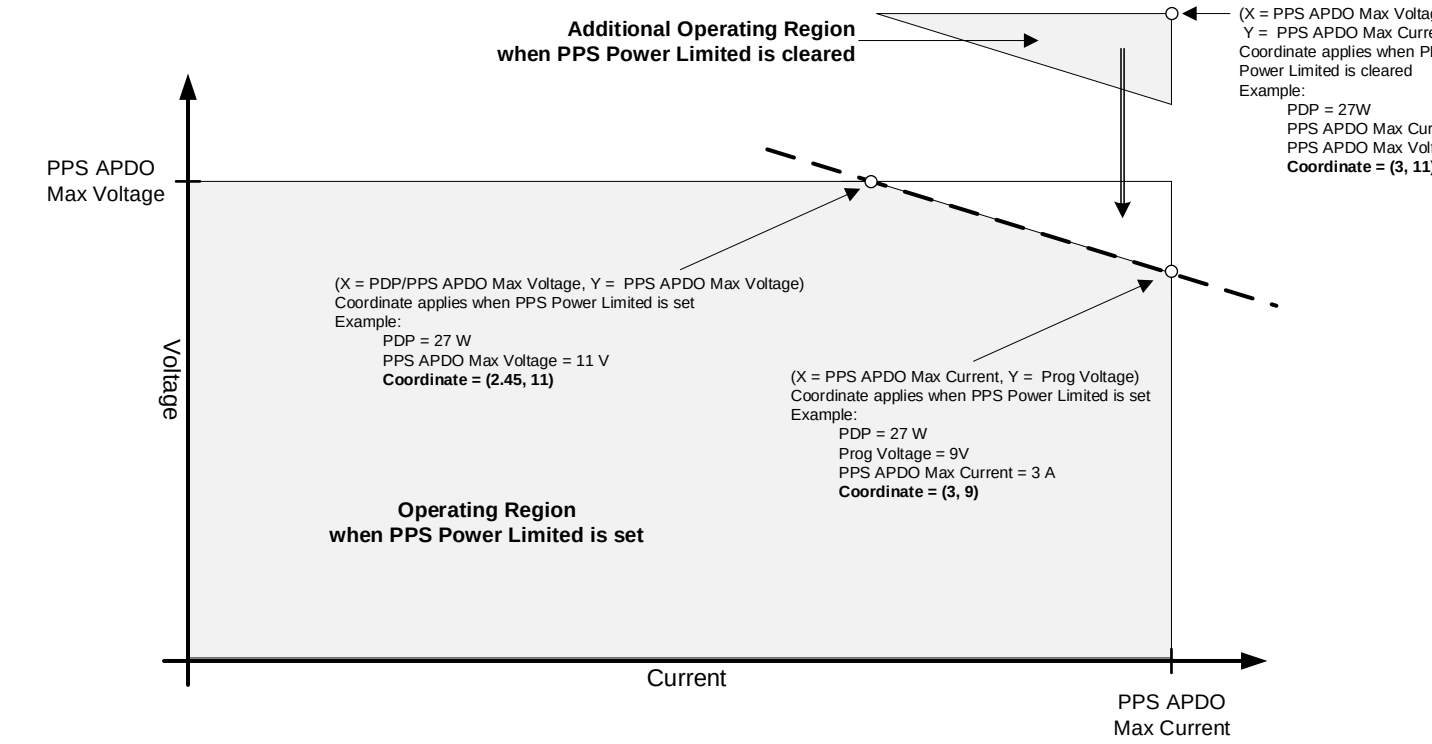
2. Point *b* represents exit from the transition region between Constant Voltage mode and Current Limit mode.
3. Point *b* is where the allowable increase in current up to iPpsCLOperating begins.
4. Point *c* represents the behavior as the load resistance decreases during Current Limit mode. See Table 7-19 for the allowed change in Operating Current (*iPpsCLOperating*) during this behavior.
5. Point *d* represents the behavior as the load resistance increases during Current Limit mode. See Table 7-19 for the allowed change in Operating Current (*iPpsCLOperating*) during this behavior.

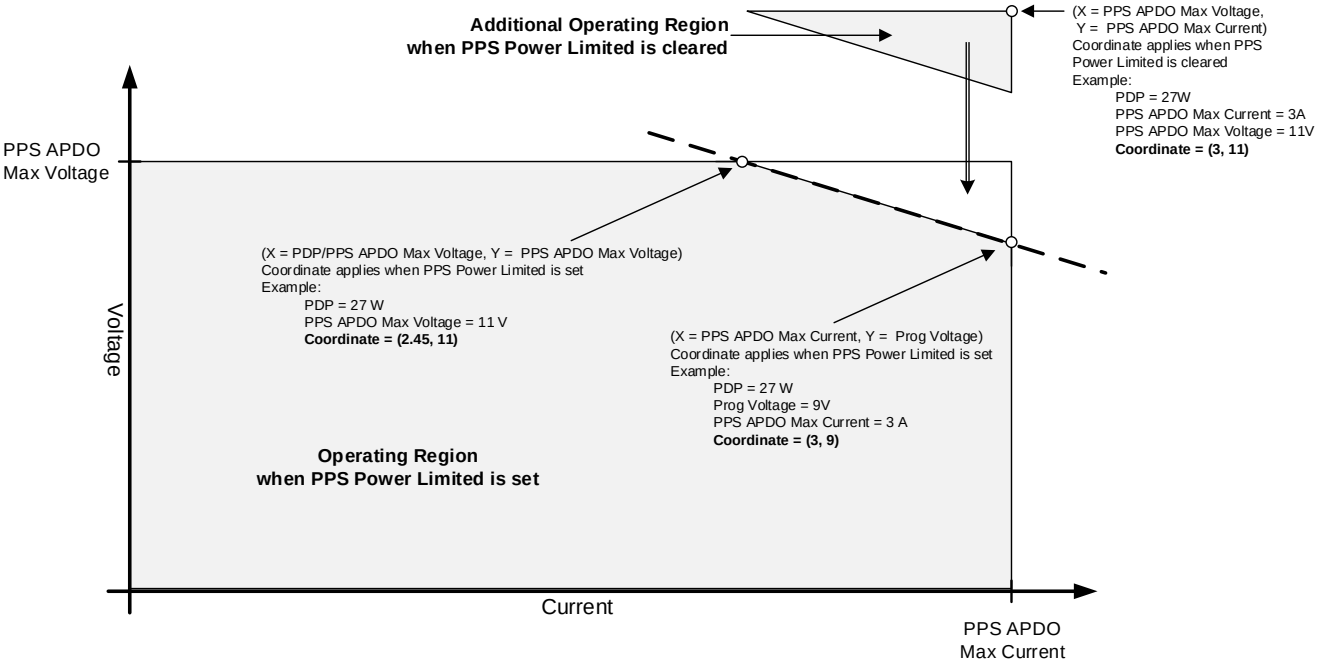
7.1.4.4.1 Constant Power Mode

In Constant Power mode (when the PPS Power Limited bit is set) the Source ***Shall*** limit its output current so that the product of the output current times the output voltage does not exceed the Source's PDP. Sinks ***May Not*** limit their Operating Current request in the RDO but ***Shall*** meet the requirements of Section 7.2.9.

The relationship between PPS programmable output voltage and PPS programmable Current Limit in the Constant Power mode ***Shall*** be as shown in Figure 7-8.

Figure 7-8 PPS Constant Power Mode





(e). Sections 7.4.1/7.4.2

From Text:

7.4.1 Source Electrical Parameters

The Source Electrical Parameters that ***Shall*** be followed are specified in Table 7-19.

Table 7-19 Source Electrical Parameters

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
cSrcBulk[1]	Source bulk capacitance when a Port is powered from a dedicated supply.	10			µF	Section 7.1.2
cSrcBulkShared[1]	Source bulk capacitance when a Port is powered from a shared supply.	120			µF	Section 7.1.2
iPpsCfMin	Minimum current foldback setting.	1			A	Section 7.1.4.4
iPpsCfNew	Current foldback accuracy					Section 7.1.4.4
	1A ≤ Operating Current ≤ 3A	-150		150	mA	
	Operating current > 3A	-5		5	%	
iPpsCfStep	PPS current foldback programming step size.		50		mA	Section 7.1.4.4
iPpsCfTransient	CF load transient current bounds.	-250		250	mA	Section 7.1.4.4
iPpsCvCfTransient	CV to CF transient current bounds assuming the Operating Voltage reduction of Section 7.2.3.1.	-100		500	mA	Section 7.1.4.4
tNewSnk	Time allowed for an initial Source in Swap Standby to transition new Sink operation.			15	ms	Figure 7-23, Figure 7-24
tPpsCfCvTransient	CF to CV transient voltage settling time.			25	ms	Section 7.1.4.4
tPpsCfProgramSettle	PPS current foldback programming settling time	125		250	ms	Section 7.1.4.4
tPpsCfSettle	CF load transient current settling time.	125		250	ms	Section 7.1.4.4
tPpsCvCfTransient	CV to CF transient settling time.	125		250	ms	Section 7.1.8.1
tPpsSrcTransition	The time the Programmable Power Supply ***Shall*** transition between requested voltages.	0		25	ms	Section 7.3
tPpsTransient	The maximum time for the Programmable power Supply to be between			5	ms	Section 7.1.8.1

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
	vPpsNew and vPpsValid in response to a load transient					
tSrcFRSwap	Time from the initial Sink detecting that V_{BUS} has dropped below ***vSafe5V*** until the initial Sink/new Source is able to supply USB Type-C Current (see ***[USB Type-C 1.2]***)			150	µs	Section 7.1.13
tSrcReady	Time from positive/negative transition start (t0) to when the Source is ready to provide the newly negotiated power level.			285	ms	Figure 7-2, Figure 7-3
tSrcRecover	Time allotted for the Source to recover.	0.66		1	s	Section 7.1.5
tSrcSettle	Time from positive/negative transition start (t0) to when the transitioning voltage is within the range ***vSrcNew.***			275	ms	Figure 7-2
tSrcSwapStdby	The maximum time for the Source to transition to Swap Standby.			650	ms	Table 7-9 Table 7-10
tSrcTransient	The maximum time for the Source output voltage to be between ***vSrcNew*** and ***vSrcValid*** in response to a load transient.			5	ms	Section 7.1.8
tSrcTransition	The time the Source ***Shall*** wait before transitioning the power supply to ensure that the Sink has sufficient time to prepare.	25		35	ms	Section 7.3
tSrcTurnOn	Transition time from ***vSafe0V*** to ***vSafe5V***.			275	ms	Table 7-12 Table 7-13
vPpsCfCvTransient	CF to CV load transient voltage bounds.	Operating Voltage * 0.95 – 0.1V		Operating Voltage * 1.05 + 0.1V	V	Section 7.1.4.4
vPpsCvCfTransient	CV to CF transient voltage bounds assuming the Operating Voltage reduction of Section 7.2.3.1.	Operating Voltage – 1.0V		Operating Voltage + 0.5V	V	Section 7.1.8.1
vPpsMaxVoltage	Maximum Voltage Field in the Programmable Power Supply APDO.	APDO Voltage *0.95		APDO Voltage * 1.05	V	Section 7.1.4.3
vPpsMinVoltage	Minimum Voltage Field in the Programmable Power Supply APDO.	APDO Voltage *0.95		APDO Voltage * 1.05	V	Section 7.1.4.3

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
vPpsNew	Programmable RDO Output Voltage measured at the Source receptacle.	RDO Output Voltage *0.95	RDO Output Voltage	RDO Output Voltage *1.05	V	Section 7.1.8.1
vPpsSlewNeg	Programmable Power Supply maximum slew rate for negative voltage changes			-30	mV/µs	Section 7.1.8.1
vPpsSlewPos	Programmable Power Supply maximum slew rate for positive voltage changes			30	mV/µs	Section 7.1.8.1
vPpsStep	PPS voltage programming step size.		20		mV	Section 7.1.8.1
vPpsValid	The range in addition to ***vPpsNew*** which the Programmable Power Supply output is considered ***Valid*** in response to a load step.	-0.1		0.1	V	Section 7.1.8.1
vSrcNeg	Most negative voltage allowed during transition.			-0.3	V	Figure 7-8
vSrcNew	Fixed Supply output measured at the Source receptacle.	PDO Voltage *0.95	PDO Voltage	PDO Voltage *1.05	V	Figure 7-2 Figure 7-3
	Variable Supply output measured at the Source receptacle.	PDO Minimum Voltage		PDO Maximum Voltage	V	
	Battery Supply output measured at the Source receptacle.	PDO Minimum Voltage		PDO Maximum Voltage	V	
vSrcPeak	The range that a Fixed Supply in Peak Current operation is allowed when overload conditions occur.	PDO Voltage *0.90		PDO Voltage *1.05	V	Table 6-10 Figure 7-10
vSrcSlewNeg	Maximum slew rate allowed for negative voltage transitions. Limits current based on a 3 A connector rating and maximum Sink bulk capacitance of 100 µF.			-30	mV/µs	Section 7.1.4.2 Figure 7-3
vSrcSlewPos	Maximum slew rate allowed for positive voltage transitions. Limits current based on a 3 A connector rating and maximum Sink bulk capacitance of 100 µF.			30	mV/µs	Section 7.1.4 Figure 7-2

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
vSrcValid	The range in addition to ***vSrcNew*** which a newly negotiated voltage is considered ***Valid*** during and after a transition. This range also applies to ***vSafe5V***.	-0.5		0.5	V	Figure 7-2 Figure 7-3
Note 1: The Source ***Shall*** charge and discharge the total bulk capacitance to meet the transition time requirements.						

7.4.2 Sink Electrical Parameters

The Sink Electrical Parameters that ***Shall*** be followed are specified in Table 7-20.

Table 7-20 Sink Electrical Parameters

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
cSnkBulk[1]	Sink bulk capacitance on V_{BUS} at Attach.	1		10	µF	Section 7.2.2
cSnkBulkPd	Bulk capacitance on V_{BUS} a Sink is allowed after a successful negotiation.	1		100	µF	Section 7.2.2
iLoadReleaseRate	Load release di/dt . Refer to ***[USB Type-C 1.2]*** Section 3.7.3.3.2 for cable details.	-150			mA/µs	Section 7.2.6
iLoadStepRate	Load step di/dt . Refer to ***[USB Type-C 1.2]*** Section 3.7.3.3.2 for cable details.			150	mA/µs	Section 7.2.6
iOvershoot	Positive or negative overshoot when a load change occurs less than or equal to ***iLoadStepRate***; relative to the settled value after the load change. Refer to USB ***[USB Type-C 1.2]*** Section 3.7.3.3.2 for cable details.	-230		230	mA	Section 7.2.6
iPpsCfLoadRelease	Maximum load release decrease during Current Foldback.	-500			mA	Section 7.2.3.1
iPpsCfLoadReleaseRate	Maximum load decrease slew rate during Current Foldback.	-150			mA/µs	Section 7.2.3.1
iPpsCfLoadStep	Maximum load step increase during Current Foldback.			500	mA	Section 7.2.3.1
iPpsCfLoadStepRate	Maximum load increase slew rate during Current Foldback.			150	mA/µs	Section 7.2.3.1
iSafe0mA	Maximum current a Sink is allowed to draw when V_{BUS} is driven to ***vSafe0V***.			1.0	mA	Figure 7-26 Figure 7-27
iSnkSwapStdby	Maximum current a Sink can draw during Swap Standby. Ideally this current is very near to 0 mA largely influenced by Port leakage current.			2.5	mA	Section 7.2.7
pHubSusp	Suspend power consumption for a hub. 25mW + 25mW per downstream Port for up to 4 ports.			125	mW	Section 7.2.3
pSnkStdby	Maximum power consumption while in Sink Standby.			2.5	W	Section 7.2.3
pSnkSusp	Suspend power consumption for a peripheral device.			25	mW	Section 7.2.3

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
tNewSrc	Maximum time allowed for an initial Sink in Swap Standby to transition to new Source operation.			275	ms	Section 7.2.7 Table 7-9 Table 7-10
tSnkHardResetPrepare	Time allotted for the Sink power electronics to prepare for a Hard Reset.			15	ms	Table 7-13
tSnkNewPower	Maximum transition time between power levels.			15	ms	Section 7.2.3
tSnkRecover	Time for the Sink to resume USB Default Operation.			150	ms	Table 7-12
tSnkStdby	Time to transition to Sink Standby from Sink.			15	ms	Section 7.2.3
tSnkSwapStdby	Maximum time for the Sink to transition to Swap Standby.			15	ms	Section 7.2.7
Note 1: If more bypass capacitance than *cSnkBulk* max or *cSnkBulkPd* max is required in the device, then the device ***Shall*** incorporate some form of V_{BUS} surge current limiting as described in *[USB 3.1]* Section 11.4.4.1.						

To Text:

7.4.1 Source Electrical Parameters

The Source Electrical Parameters that ***Shall*** be followed are specified in Table 7-19.

Table 7-19 Source Electrical Parameters

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
cSrcBulk[1]	Source bulk capacitance when a Port is powered from a dedicated supply.	10			µF	Section 7.1.2
cSrcBulkShared[1]	Source bulk capacitance when a Port is powered from a shared supply.	120			µF	Section 7.1.2
iPpsCLMin	Minimum Current ~~foldback~~ Limit setting.	1			A	Section 7.1.4.4
iPpsCLNew	Current Limit accuracy					Section 7.1.4.4
	1A ≤ Operating Current ≤ 3A	-150		150	mA	
	Operating current > 3A	-5		5	%	
iPpsCLOperating	Total allowed change in Operating Current from point *b* in Figure 7-7 as the load resistance decreases during Current Limit mode.	0		+100	mA	See Figure 7-7
iPpsCLStep	PPS Current Limit programming step size.		50		mA	Section 7.1.4.4
iPpsCLTransient	CL load transient current bounds.	-250		250	mA	Section 7.1.4.4
iPpsCVCLTransient	CV to CL transient current bounds assuming	-100		500	mA	Section 7.1.4.4

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
	the Operating Voltage reduction of Section 7.2.3.1.					
tNewSnk	Time allowed for an initial Source in Swap Standby to transition new Sink operation.			15	ms	Figure 7-23, Figure 7-24
tPpsCLCVTransient	CL to CV transient voltage settling time.			25	ms	Section 7.1.4.4
tPpsCLProgramSettle	PPS Current Limit programming settling time	125		250	ms	Section 7.1.4.4
tPpsCLSettle	CL load transient current settling time.	125		250	ms	Section 7.1.4.4
tPpsCVCLTransient	CV to CL transient settling time.	125		250	ms	Section 7.1.8.1
tPpsSrcTransition	The time the Programmable Power Supply ***Shall*** transition between requested voltages.	0		25	ms	Section 7.3
tPpsTransient	The maximum time for the Programmable power Supply to be between vPpsNew and vPpsValid in response to a load transient			5	ms	Section 7.1.8.1
tSrcFRSwap	Time from the initial Sink detecting that V_{BUS} has dropped below ***vSafe5V*** until the initial Sink/new Source is able to supply USB Type-C Current (see ***[USB Type-C 1.2]***)			150	µs	Section 7.1.13
tSrcReady	Time from positive/negative transition start (t0) to when the Source is ready to provide the newly negotiated power level.			285	ms	Figure 7-2, Figure 7-3
tSrcRecover	Time allotted for the Source to recover.	0.66		1	s	Section 7.1.5
tSrcSettle	Time from positive/negative transition start (t0) to when the transitioning voltage is within the range ***vSrcNew.***			275	ms	Figure 7-2
tSrcSwapStdby	The maximum time for the Source to transition to Swap Standby.			650	ms	Table 7-9 Table 7-10

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
tSrcTransient	The maximum time for the Source output voltage to be between *vSrcNew* and *vSrcValid* in response to a load transient.			5	ms	Section 7.1.8
tSrcTransition	The time the Source ***Shall*** wait before transitioning the power supply to ensure that the Sink has sufficient time to prepare.	25		35	ms	Section 7.3
tSrcTurnOn	Transition time from *vSafe0V* to *vSafe5V*.			275	ms	Table 7-12 Table 7-13
vPpsCLCVTransient	CL to CV load transient voltage bounds.	Operating Voltage * 0.95 – 0.1V		Operating Voltage * 1.05 + 0.1V	V	Section 7.1.4.4
vPpsCVCLTransient	CV to CL transient voltage bounds assuming the Operating Voltage reduction of Section 7.2.3.1.	Operating Voltage – 1.0V		Operating Voltage + 0.5V	V	Section 7.1.8.1
vPpsMaxVoltage	Maximum Voltage Field in the Programmable Power Supply APDO.	APDO Voltage *0.95		APDO Voltage * 1.05	V	Section 7.1.4.3
vPpsMinVoltage	Minimum Voltage Field in the Programmable Power Supply APDO.	APDO Voltage *0.95		APDO Voltage * 1.05	V	Section 7.1.4.3
vPpsNew	Programmable RDO Output Voltage measured at the Source receptacle.	RDO Output Voltage *0.95	RDO Output Voltage	RDO Output Voltage *1.05	V	Section 7.1.8.1
vPpsSlewNeg	Programmable Power Supply maximum slew rate for negative voltage changes			-30	mV/µs	Section 7.1.8.1
vPpsSlewPos	Programmable Power Supply maximum slew rate for positive voltage changes			30	mV/µs	Section 7.1.8.1
vPpsStep	PPS voltage programming step size.		20		mV	Section 7.1.8.1
vPpsValid	The range in addition to *vPpsNew* which the Programmable Power Supply output is considered ***Valid*** in response to a load step.	-0.1		0.1	V	Section 7.1.8.1
vSrcNeg	Most negative voltage allowed during transition.			-0.3	V	Figure 7-8
vSrcNew	Fixed Supply output measured at the Source receptacle.	PDO Voltage *0.95	PDO Voltage	PDO Voltage *1.05	V	Figure 7-2 Figure 7-3

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
	Variable Supply output measured at the Source receptacle.	PDO Minimum Voltage		PDO Maximum Voltage	V	
	Battery Supply output measured at the Source receptacle.	PDO Minimum Voltage		PDO Maximum Voltage	V	
vSrcPeak	The range that a Fixed Supply in Peak Current operation is allowed when overload conditions occur.	PDO Voltage *0.90		PDO Voltage *1.05	V	Table 6-10 Figure 7-10
vSrcSlewNeg	Maximum slew rate allowed for negative voltage transitions. Limits current based on a 3 A connector rating and maximum Sink bulk capacitance of 100 µF.			-30	mV/µs	Section 7.1.4.2 Figure 7-3
vSrcSlewPos	Maximum slew rate allowed for positive voltage transitions. Limits current based on a 3 A connector rating and maximum Sink bulk capacitance of 100 µF.			30	mV/µs	Section 7.1.4 Figure 7-2
vSrcValid	The range in addition to ***vSrcNew*** which a newly negotiated voltage is considered ***Valid*** during and after a transition. This range also applies to ***vSafe5V***.	-0.5		0.5	V	Figure 7-2 Figure 7-3
Note 1: The Source ***Shall*** charge and discharge the total bulk capacitance to meet the transition time requirements.						

7.4.2 Sink Electrical Parameters

The Sink Electrical Parameters that ***Shall*** be followed are specified in Table 7-20.

Table 7-20 Sink Electrical Parameters

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
cSnkBulk[1]	Sink bulk capacitance on V_{BUS} at Attach.	1		10	µF	Section 7.2.2
cSnkBulkPd	Bulk capacitance on V_{BUS} a Sink is allowed after a successful negotiation.	1		100	µF	Section 7.2.2
iLoadReleaseRate	Load release di/dt . Refer to ***[USB Type-C 1.2]*** Section 3.7.3.3.2 for cable details.	-150			mA/µs	Section 7.2.6
iLoadStepRate	Load step di/dt . Refer to ***[USB Type-C 1.2]*** Section 3.7.3.3.2 for cable details.			150	mA/µs	Section 7.2.6
iOvershoot	Positive or negative overshoot when a load change occurs less than or equal to ***iLoadStepRate***; relative to the settled value after the load change. Refer to USB ***[USB Type-C 1.2]*** Section 3.7.3.3.2 for cable details.	-230		230	mA	Section 7.2.6
iPpsCLLoadRelease	Maximum load release decrease during Current Limit.	-500			mA	Section 7.2.3.1
iPpsCLLoadReleaseRate	Maximum load decrease slew rate during Current Limit.	-150			mA/µs	Section 7.2.3.1
iPpsCLLoadStep	Maximum load step increase during Current Limit.			500	mA	Section 7.2.3.1
iPpsCLLoadStepRate	Maximum load increase slew rate during Current Limit.			150	mA/µs	Section 7.2.3.1
iSafe0mA	Maximum current a Sink is allowed to draw when V_{BUS} is driven to ***vSafe0V***.			1.0	mA	Figure 7-26 Figure 7-27
iSnkSwapStdby	Maximum current a Sink can draw during Swap Standby. Ideally this current is very near to 0 mA largely influenced by Port leakage current.			2.5	mA	Section 7.2.7
pHubSusp	Suspend power consumption for a hub. 25mW + 25mW per downstream Port for up to 4 ports.			125	mW	Section 7.2.3
pSnkStdby	Maximum power consumption while in Sink Standby.			2.5	W	Section 7.2.3

Parameter	Description	MIN	TYP	MAX	UNITS	Reference
pSnkSusp	Suspend power consumption for a peripheral device.			25	mW	Section 7.2.3
tNewSrc	Maximum time allowed for an initial Sink in Swap Standby to transition to new Source operation.			275	ms	Section 7.2.7 Table 7-9 Table 7-10
tSnkHardResetPrepare	Time allotted for the Sink power electronics to prepare for a Hard Reset.			15	ms	Table 7-13
tSnkNewPower	Maximum transition time between power levels.			15	ms	Section 7.2.3
tSnkRecover	Time for the Sink to resume USB Default Operation.			150	ms	Table 7-12
tSnkStdby	Time to transition to Sink Standby from Sink.			15	ms	Section 7.2.3
tSnkSwapStdby	Maximum time for the Sink to transition to Swap Standby.			15	ms	Section 7.2.7
Note 1: If more bypass capacitance than ***cSnkBulk*** max or ***cSnkBulkPd*** max is required in the device, then the device ***Shall*** incorporate some form of V_{BUS} surge current limiting as described in ***[USB 3.1]*** Section 11.4.4.1.						