Brief about USB 3.0 and Comparison with USB 2.0

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1 author:

Neel Tailor
Nirma University

USB 3.0 Protocol

Comparision of USB 2.0 and USB 3.0

Tailor Neel Kishorkumar
Institute of Technology, Nirma University,
Ahmedabad, India.
tailor.neel@gmail.com

***Abstract*—One of the most common digital interfaces found today is USB. This paper describes how super speed USB 3.0 works and in which area it is differing from its previous version high speed USB 2.0.**

***Keywords*—SuperSpeed,USB 2.0, USB 3.0**

I. Introduction

USB (Universal Serial Bus), as its name suggests it is external bus architecture to connect peripheral to host compute devices which are USB capable. The USB was formed by group of seven companies named Compaq, DEC(Digital Equipment Corporation), IBM(International Business Machine Corporations), Intel, Microsoft, NEC and Nortal in 1994.[1] The goal was to make it fundamentally easier to connect external devices to PCs by replacing the multitude of connectors at the back of PCs. USB was mainly designed to make a standard for connecting computer peripherals like digital cameras, disk drives, keyboards, portable media players, printers, network adapters to personal computers, both to communicate and to supply power.

Initially, the USB 1.0 specification was introduced with only a data transfer rate of 1.5 Mbit/s in January 1996. Then the USB 1.1 was launched with a maximum data transfer rate of 12 Mbit/s in September 1998. Moving on to USB 2.0 specification war released in April 2000 and was ratified by USB-IF(USB Implementers Forum) at the end of 2001. HP(Hewlett-Packard), Intel, Lucent Technologies(now Alcatel-Lucent), NEC and Philips jointly led the initiative to develop a higher data transfer rate, with the resulting specification achieving 480 Mbit/s, a 40 times faster than the original USB 1.1 specification. The USB 3.0 specification was released on 12 November 2008. Here, in USB 3.0, it is having an increased data transfer rate (up to 5Gbit/s), decreased power consumption, increased power output and most importantly, USB 3.0 is backwards-compatible with USB 2.0. Also, USB 3.0 consists of a new higher speed bus known as SuperSpeed that is in parallel with the USB 2.0 bus.

II. Comparision of USB 2.0 and USB 3.0

A. Speed

In USB 3.0 a new transfer type is introduced called SuperSpeed or SS which supports almost 5 Gbit/s where high speed USB 2.0 supports only 480 Mbit/s. So, USB 3.0 is 10 times faster than USB 2.0.

Fig. 1. USB 3.0 logo[4]

B. Bandwidth

USB 2.0 is having half-duplex two wire signaling which means unidirectional data flow with negotiated directional bus transitions. The template is used to format your paper and style the text. While USB 3.0 is having dual-simplex four wire signaling which means bi-directional data flows.

C. Bus Tranaction Protocol

USB 2.0 is host directed in which host polls continuously to all connected peripheral devices that any of them is having data to transfer and for this all devices must keep "on" at all times. In USB 3.0 polling is replaced by asynchronous notification. In SuperSpeed the host waits until a higher level application tells it that a peripheral is having data to share. Then the host contacts that specific peripheral to check if data is ready to share or not and when both ends of links that are peripheral and host are ready, the data is shared. With this USB 3.0 has also eliminated broadcast nature of USB 2.0.

D. Power Management

USB 3.0 is reducing power requirement by eliminating polling and broadcasting nature of USB 2.0 and with that it uses link-, device-, and function- level power management. Power management is done by using four different states in link power management which are U0, U1, U2 and U3. U0 is for activating link, U1 for link idle-fast exit, U2 for link idle-slower exit and U3 for link suspend.

III. USB 3.0 CABLE CONSTRUCTION AND WIRE ASSIGNMENTS

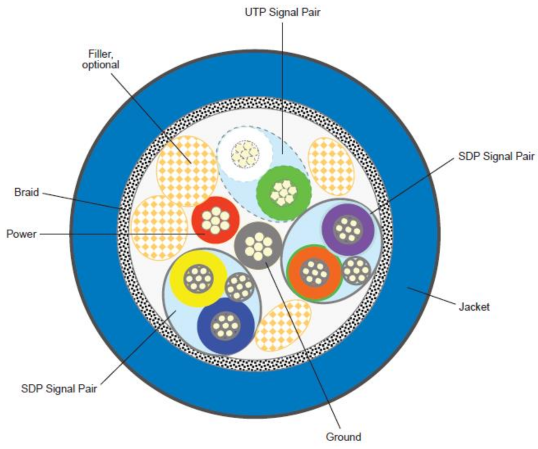

Fig. 2. Illustration of a USB 3.0 cable cross-section[2]

TABLE I. CABLE WIRE ASSIGNMENTS[3]

Wire No.	Wire Assignments		
	Signal Name	***Description***	***Color***
1	PWR	Power	Red
2	UTP_D-	Unshielded twist pair, Negative	White
3	UTP_D+	Unshielded twist pair, Positive	Green
4	GND_PWRrt	Ground for power return	Black
5	SDP1-	Shielded differential pair1,Negative	Blue
6	SDP1+	Shielded differential pair1,Positive	Yellow
7	SDP1_Drain	Drain wire for SDP1	-
8	SDP2-	Shielded differential pair2,Negative	Purple
9	SDP2+	Shielded differential pair1,Positive	Orange
10	SDP2_Drain	Drain wire for SDP2	-
Braid	Shield	Cable external braid to be 360° terminated on to plug metal shell	-

Fig. 1 illustrates the cross section of a USB 3.0 cable. There are basic three group of wires: UTP signal pair, SDP and power and ground wires. The purpose of intending UTP is to transmit USB 2.0 signaling while the SDPs are for SuperSpeed where shield is needed signal integrity and EMI performance for the SuperSpeed differential pair. Each SDP is attached with a drain wire, which is connected to system ground the GND_DRAIN pins in the connector.

IV. USB 3.0 BUS ARCHITECTURE

A. *SuperSpeed Capable Host with SuperSpeed Capable Software*

When the host is powered off, the hub will not provide power to its downstream ports unless the hub is supporting charging applications.

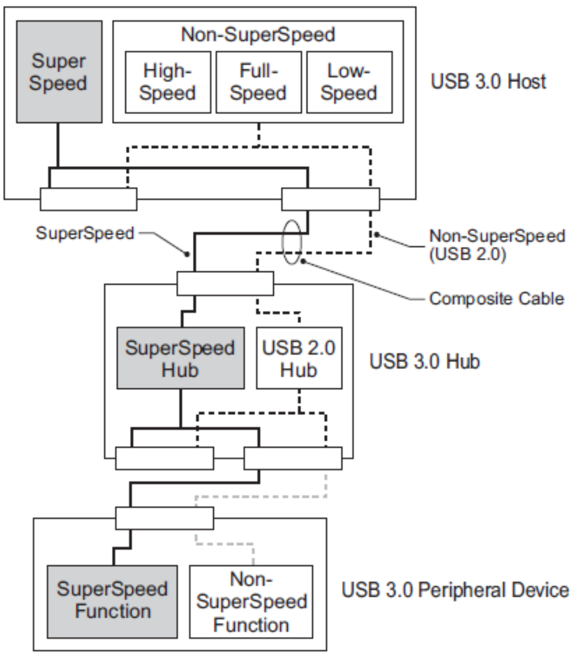

Fig. 3. USB 3.0 Dual Bus Topology[3]

When the host is powered on with a support of SuperSpeed, it enabled on its downstream ports by default the following events will take place

- Hub detects VBUS and SuperSpeed support and powers its downstream ports with SuperSpeed enabled.
- Hub connects both as a SuperSpeed and as a high-speed device
- Device detects VBUS and SuperSpeed support and connect as a SuperSpeed device
- Host system begins hub enumeration at both SuperSpeed and high-speed
- Host system begins device enumeration at SuperSpeed

B. *USB 2.0 host*

When the host is powered off, the hub will not provide power to its downstream ports unless the hub is supporting charging applications.

When the host is powered on and not having support of SuperSpeed hardware, the following events will take place

- Hub detects VBUS and connects at a high-speed device
- Host system begins hub enumeration at high-speed
- Hubs power downstream ports when directed by software with disabling SuperSpeed support
- Device connects at high-speed

- Host system begins device enumeration at high-speed

V. SuperSpeed Architecture

The SuperSpeed bus is having a layered communication architecture that is having main three elements which are SuperSpeed Interconnect which is path for devices through which they connected to and communicate with the host, Devices which is for implementing the required device-end and Host which is for implementing the required host-end. Devices and Host are the sources or sinks of information which communicate or exchange information using the SuperSpeed bus. Host is the owner of the SuperSpeed data activity schedule, management of the SuperSpeed bus and all devices which are connected to it.

A. Physical layer

The Physical layer defines the PHY portion of a port and the physical connection between the upstream facing port and the downstream facing port (on a hub or host). The SuperSpeed physical connection is a combination of two differential data pairs which are transmit path and receive path. A transmitter, channel and receiver are the electrical aspects of each path which combined represent a unidirectional differential link. At an electrical level, all differential links are initialized by enabling its receiver termination. The transmitter is responsible to detect the far end receiver termination as an indication of a bus connection and to inform the link layer so the connect status can be factored into link operation and management.

B. Link Layer

The SuperSpeed link is a connection of two ports which are logical and physical. The connected ports are called link partners. The link layer defines the communication between link partners and the logical portion of a port.

The logical portion of a port has:

- State machines to manage its end of the physical connections which includes initialization and event management of the physical layer i.e. connect, power management and removal.
- State machines and buffering to manage information exchanges with the link partner which implements protocol for control, power management and reliable delivery of packet headers from port to port.
- Ability to provide correct framing of sequences of bytes into packets during transmission
- Ability to detect received packets and error checks of received header packets for reliable delivery

C. Protocol Layer

The protocol layer defines the “end-to-end” communications rules between a host and device. The SuperSpeed protocol provides for application data information exchanges between a host and a device endpoint. This communication relationship is known as pipe. It is a host directed protocol, which indicates that the host always determines when application data is transferred between the device and host. In this, device is able to request asynchronously service from the host on behalf of a particular endpoint.

VI. USB 3.0 Enumeration

USB enumeration is the process in which host detects that a USB device is connected or not, identifies which devise is connected and then loads the relevant device drivers. The USB specifications have defined six different device states. During enumeration, a device goes through four of the states which are Powered, Default, Address and Configured.(Other two states are Attached and Suspend). This involves a combination of hardware techniques to detect something is connected and software techniques to identify what has been connected. After detection of a device the host will start an exchange with a device to determine what it is. The host does this by asking for device descriptors which will define the device class and what drivers will need to be loaded. During the enumeration the following sequence of steps will be followed.

A. Attaching device to USB port

The Port may be on the root hub at the host or a hub that connects downstream from the host. The hub provides power to the port, and the device will be in the Powered state. The device can maximum draw up to 150 mA from the bus before configuration and 900 mA after configuration.

B. The host detects a device

The USB hub continually monitors the voltage levels on D+ and D- signal lines of each of its ports because a USB port, having no device connected to it uses 15 kohm pull-down resistors to make connection between USB D+ and D- signal lines and GND line. When a device inserts into a port, the device’s brings its line high with its own pull-up resistors which will enable the host to detect that a device is connected.

C. Detecting a Device type

On detecting a downstream SuperSpeed termination at a port, a host initializes and trains the port’s link. Enumeration then proceeds at SuperSpeed with no need for further speed detecting.

Detecting whether connected device supports high speed, USB host uses two special signal states known as J and k Chirp. Host sends a series of alternating Chirp K and Chirp J. On detecting the pattern KJKJKJ, the device removes (switch OFF) its full-speed pull-up resistors and performs all further communications at high speed. If this initial communication fails then the USB host assumes that the device is a full speed device.

D. Establishing Signal Pair

Once the USB host identify that device is connected and at what data transfer rate it should communicate, the host will send a reset to the USB device. The device will start communication with host by using the default address of 00h. The device is in the Default state and device's USB registers are in their reset states. Now the device is ready to respond to control transfers at endpoint zero. This reset is visible to the new device only and the other devices on the bus don't see the reset. For USB 3.0, the host is not required to reset the port after learning of a new device connection.

E. Get Descriptor Request

The host sends the request to device address 00h, end-point zero. Because the host enumerates only one device at a time, only one device will respond to communications addressed to device address 00h even if several devices attach at once. There are different descriptors among them these two are specially for SuperSpeed.

- The BOS descriptor functions as a base descriptor for one or more related device capability descriptors. This provides a way to support
- The Device Capability Descriptor provides information that is specific to a technology or another aspect of a device or its function.

F. Assigning Address and Loading Drivers

When reset is complete, the host controller assigns a unique address to the device by sending a Set Address request. The address is valid until the device is detached a hub resets the port, or the system reboots. After learning about a device from its descriptor, the host looks for the best match in a driver to manage communications with the device. Windows hosts use INF files to identify the best match.

TABLE II. BOS Descriptor[1]

Offset (Decimal)	**Field**	**Size (Bytes)**	**Description**
0	bLength	1	Descriptor size in bytes(05h)
1	bDescriptorType	1	BOS(0Fh)
2	wTotalLength	2	The no. of bytes in this descriptor and all of its subordinate descriptors
4	bNumDeviceCaps	1	The no. of device capability descriptors subordinate to this BOS descriptor

TABLE III. Device Capability Descriptor[1]

Offset (Decimal)	**Field**	**Size (Bytes)**	**Description**
0	bLength	1	Descriptor size in bytes(varies)
1	bDescriptorType	1	Device Capability(10h)
2	bDevCapabilityType	1	01h = Wireless USB 02h = USB 2.0 Extension 03h = SuperSpeed_USB 04h = Container ID 00h,05h-FFh (reserved)
3	Capability-Dependent	Varies	Capability specific data and format

CONCLUSION

This paper overviewed the concept of SuperSpeed USB 3.0 and differences which make it faster and more preferable than USB 2.0. USB 3.0 is basic requirement of any system because it is the easiest way to make communication between a PC and external peripherals or any two end devices which supports USB like keyboard, printer, scanner, flash drives etc. Even this communication is fast and requires less power in comparisons of other communication techniques because of its power management technique.

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