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Design of Digital Systems

Project 2 Report

jda_lib

Design Constraints

1. Inverter Width	= 1xW
2. Orientation of transistor channel width	= Vertical
3. NMOS W/L ratio	= 8λ / 2λ
4. PMOS W/L ratio	= $1x(W/L)_N$
5. Special Gate design	= OAI
6. MUX design	= CMOS 2to1 MUX

The NMOS W/L ratio of 8/2 is used as the standard with to achieve a resistance of 1R. Therefore, while PMOS is $1x(W/L)_N$, both the NMOS and PMOS gate sizes in the designs are to be sized properly to achieve a pull-up or pull-down resistance of 1R.

Final Remarks and Conclusion

Much of the work so far is unverified, with no simulation run to check for operation errors. The Inverter and NAND gate are fine based on DMC and LVS checking. The only known error with the NOR gate is a possible issue with the PMOS gate sizing.

Schematics for all other Gates and non-hierarchical have been created, although the DFF implementation is incomplete.

Due to much working being incomplete, the current priority is the following to get done by next Lab session, Tuesday:

1. Simulate INV, NAND, and NOR, obtain all currently missing data and verify designs are functioning as expected.

2. Finish DFF and XOR in layout

3. Create presentation of work finished

Additional work to be completed within the next 10 days:

1. Complete FA cell, BSSUM cell along with the EDA tutorial 2

2. Complete the OAI and CMOS 2to1 MUX layouts

3. Verify all cells and update datasheets, double check for missing implementations.

Datasheets

Library Name:	jda_inv		
Cell Name:	jda_inv		
Function/Truthtable:			
	A	Y	
	0	1	
	1	0	
Propegation Delay:			
Symbol with Port Names:	symbol	in1	out1
Schematic:	schematic		
Layout:	layout		
Verilog Model:			
Comments/Notes:			

Library Name:	jda_nand2			
Cell Name:	jda_nand2			
Function/Truthtable:				
	A	B	Y	
	0	0	1	
	0	1	1	
	1	0	1	
	1	1	0	
Propegation Delay:				
Symbol with Port Names:	symbol	in1	in2	out1
Schematic:	schematic			
Layout:	layout			
Verilog Model:				
Comments/Notes:				

Library Name:	jda_nor2			
Cell Name:	jda_nor2			
Function/Truthtable:				
	A	B	Y	
	0	0	1	
	0	1	0	
	1	0	0	
	1	1	0	
Propegation Delay:				
Symbol with Port Names:	symbol	in1	in2	out1
Schematic:	schematic			
Layout:	layout			
Verilog Model:				
Comments/Notes:				

Library Name:	jda_OAI4				
Cell Name:	jda_OAI4				
Function/Truthtable:					
	A	B	C	D	Y
	0	0	0	0	1
	0	0	0	1	1
	0	0	1	0	1
	0	0	1	1	1
	0	1	0	0	1
	0	1	0	1	0
	0	1	1	0	0
	0	1	1	1	0
	1	0	0	0	1
	1	0	0	1	0
	1	0	1	0	0
	1	0	1	1	0
	1	1	0	0	1
	1	1	0	1	0
	1	1	1	0	0
	1	1	1	1	0
Propegation Delay:					
Symbol with Port Names:					
Schematic:	schematic				
Layout:					
Verilog Model:					
Comments/Notes:					

Library Name:	jda_MUX2to1			
Cell Name:	jda_MUX2to1			
Function/Truthtable:				
	s	A	B	Y
	0	0	0	0
	0	0	1	0
	0	1	0	1
	0	1	1	1
	1	0	0	0
	1	0	1	1
	1	1	0	0
	1	1	1	1
Propegation Delay:				
Symbol with Port Names:				
Schematic:	schematic			
Layout:				
Verilog Model:				
Comments/Notes:				

Library Name:	jda_dff			
Cell Name:	jda_dff			
Function/Truthtable:				
Propegation Delay:				
Symbol with Port Names:				
Schematic:	schematic			
Layout:	layout			
Verilog Model:				
Comments/Notes:				

Library Name:	jda_xor2			
Cell Name:	jda_xor2			
Function/Truthtable:				
	A	B	Y	
	0	0	0	
	0	1	1	
	1	0	1	
	1	1	0	
Propegation Delay:				
Symbol with Port Names:				
Schematic:	schematic			
Layout:	layout			
Verilog Model:				
Comments/Notes:				