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MCUXpresso SDK API Reference Manual

NXP Semiconductors



Contents

Chapter 1 Introduction

Chapter 2 Trademarks

Chapter 3 Architectural Overview

Chapter 4 Clock Driver

4.1 Overview	7
4.2 Data Structure Documentation	24
4.2.1 struct cgc_rtd_sys_clk_config_t	24
4.2.2 struct cgc_hifi_sys_clk_config_t	25
4.2.3 struct cgc_lpav_sys_clk_config_t	25
4.2.4 struct cgc_ddr_sys_clk_config_t	26
4.2.5 struct cgc_sosc_config_t	27
4.2.6 struct cgc_fro_config_t	27
4.2.7 struct cgc_lposc_config_t	28
4.2.8 struct cgc_pll0_config_t	28
4.2.9 struct cgc_rosc_config_t	29
4.2.10 struct cgc_pll1_config_t	29
4.2.11 struct cgc_pll4_config_t	30
4.3 Macro Definition Documentation	31
4.3.1 FSL_SDK_DISABLE_DRIVER_CLOCK_CONTROL	31
4.3.2 FSL_CLOCK_DRIVER_VERSION	31
4.3.3 PCC_PCS_VAL	32
4.3.4 GPIO_CLOCKS	32
4.3.5 SAI_CLOCKS	32
4.3.6 PCTL_CLOCKS	32
4.3.7 LPI2C_CLOCKS	32
4.3.8 I3C_CLOCKS	33
4.3.9 FLEXIO_CLOCKS	33
4.3.10 FLEXCAN_CLOCKS	33
4.3.11 PDM_CLOCKS	33
4.3.12 LCDIF_CLOCKS	33
4.3.13 MIPI_DSI_HOST_CLOCKS	34
4.3.14 EDMA_CLOCKS	34

Section No.	Title	Page No.
4.3.15	EDMA_CHAN_CLOCKS	34
4.3.16	LPUART_CLOCKS	34
4.3.17	DAC_CLOCKS	34
4.3.18	LPTMR_CLOCKS	35
4.3.19	LPADC_CLOCKS	35
4.3.20	LPSPI_CLOCKS	35
4.3.21	TPM_CLOCKS	35
4.3.22	LPIT_CLOCKS	35
4.3.23	CMP_CLOCKS	36
4.3.24	WDOG_CLOCKS	36
4.3.25	SEMA42_CLOCKS	36
4.3.26	TPIU_CLOCKS	36
4.3.27	FLEXSPI_CLOCKS	36
4.3.28	MRT_CLOCKS	37
4.3.29	BBNSM_CLOCKS	37
4.3.30	PXP_CLOCKS	37
4.3.31	EPDC_CLOCKS	37
4.4	Enumeration Type Documentation	37
4.4.1	clock_name_t	37
4.4.2	clock_ip_src_t	39
4.4.3	clock_lptmr_src_t	43
4.4.4	clock_ip_name_t	43
4.4.5	anonymous enum	44
4.4.6	cgc_sys_clk_t	44
4.4.7	cgc_rtd_sys_clk_src_t	44
4.4.8	cgc_nic_sys_clk_src_t	44
4.4.9	cgc_hifi_sys_clk_src_t	45
4.4.10	cgc_lpav_sys_clk_src_t	45
4.4.11	cgc_ddr_sys_clk_src_t	45
4.4.12	clock_rtd_clkout_src_t	45
4.4.13	clock_lpav_clkout_src_t	46
4.4.14	cgc_async_clk_t	46
4.4.15	cgc_sosc_monitor_mode_t	46
4.4.16	cgc_sosc_mode_t	47
4.4.17	_cgc_sosc_enable_mode	47
4.4.18	_cgc_fro_enable_mode	47
4.4.19	_cgc_lposc_enable_mode	47
4.4.20	cgc_pll_src_t	47
4.4.21	_cgc_pll_enable_mode	47
4.4.22	cgc_pll_pfd_clkout_t	48
4.4.23	cgc_pll0_mult_t	48
4.4.24	cgc_rosc_monitor_mode_t	48
4.4.25	cgc_pll1_mult_t	48
4.4.26	cgc_pll4_mult_t	49

Section No.	Title	Page No.
4.4.27	cgc_rtd_audclk_src_t	49
4.4.28	cgc_ad_audclk_src_t	49
4.4.29	cgc_lpav_audclk_src_t	49
4.5	Function Documentation	50
4.5.1	CLOCK_EnableClock	50
4.5.2	CLOCK_DisableClock	50
4.5.3	CLOCK_IsEnabledByOtherCore	50
4.5.4	CLOCK_SetIpSrc	50
4.5.5	CLOCK_SetIpSrcDiv	51
4.5.6	CLOCK_SetRtdAudClkSrc	51
4.5.7	CLOCK_SetAdAudClkSrc	51
4.5.8	CLOCK_SetLpavAudClkSrc	52
4.5.9	CLOCK_GetFreq	52
4.5.10	CLOCK_GetCm33CorePlatClkFreq	52
4.5.11	CLOCK_GetCm33BusClkFreq	52
4.5.12	CLOCK_GetCm33SlowClkFreq	53
4.5.13	CLOCK_GetFusionDspCorePlatClkFreq	53
4.5.14	CLOCK_GetFusionDspBusClkFreq	53
4.5.15	CLOCK_GetFusionDspSlowClkFreq	53
4.5.16	CLOCK_GetLvdsClkFreq	53
4.5.17	CLOCK_GetIpFreq	53
4.5.18	CLOCK_GetCm33SysClkFreq	54
4.5.19	CLOCK_SetCm33SysClkConfig	54
4.5.20	CLOCK_GetFusionDspSysClkFreq	54
4.5.21	CLOCK_SetFusionSysClkConfig	55
4.5.22	CLOCK_GetCm33SysClkConfig	55
4.5.23	CLOCK_GetFusionDspSysClkConfig	55
4.5.24	CLOCK_SetRtdClkOutConfig	55
4.5.25	CLOCK_SetRtcClkOutConfig	56
4.5.26	CLOCK_GetXbarBusClkFreq	56
4.5.27	CLOCK_GetHifiDspSysClkFreq	56
4.5.28	CLOCK_SetHifiDspSysClkConfig	56
4.5.29	CLOCK_GetHifiDspSysClkConfig	57
4.5.30	CLOCK_GetLpavSysClkFreq	57
4.5.31	CLOCK_SetLpavSysClkConfig	57
4.5.32	CLOCK_GetLpavSysClkConfig	57
4.5.33	CLOCK_GetDdrClkFreq	58
4.5.34	CLOCK_SetLpavClkOutConfig	58
4.5.35	CLOCK_InitSysOsc	58
4.5.36	CLOCK_DeinitSysOsc	59
4.5.37	CLOCK_SetRtdSysOscAsyncClkDiv	59
4.5.38	CLOCK_SetAdSysOscAsyncClkDiv	59
4.5.39	CLOCK_SetLpavSysOscAsyncClkDiv	60
4.5.40	CLOCK_GetSysOscFreq	60

Section No.	Title	Page No.
4.5.41	CLOCK_GetRtdSysOscAsyncFreq	60
4.5.42	CLOCK_GetAdSysOscAsyncFreq	61
4.5.43	CLOCK_GetLpavSysOscAsyncFreq	61
4.5.44	CLOCK_IsSysOscErr	61
4.5.45	CLOCK_SetSysOscMonitorMode	61
4.5.46	CLOCK_IsSysOscSelected	62
4.5.47	CLOCK_IsSysOscValid	62
4.5.48	CLOCK_InitFro	62
4.5.49	CLOCK_DeinitFro	62
4.5.50	CLOCK_SetRtdFroAsyncClkDiv	63
4.5.51	CLOCK_SetAdFroAsyncClkDiv	63
4.5.52	CLOCK_SetLpavFroAsyncClkDiv	63
4.5.53	CLOCK_EnableFroTuning	64
4.5.54	CLOCK_GetFroFreq	64
4.5.55	CLOCK_GetRtdFroAsyncFreq	64
4.5.56	CLOCK_GetAdFroAsyncFreq	64
4.5.57	CLOCK_GetLpavFroAsyncFreq	65
4.5.58	CLOCK_IsFroSelected	65
4.5.59	CLOCK_IsFroValid	65
4.5.60	CLOCK_InitLposc	65
4.5.61	CLOCK_DeinitLposc	66
4.5.62	CLOCK_IsLpOscValid	66
4.5.63	CLOCK_GetLpOscFreq	66
4.5.64	CLOCK_GetRtcOscFreq	66
4.5.65	CLOCK_IsRtcOscErr	67
4.5.66	CLOCK_SetRtcOscMonitorMode	67
4.5.67	CLOCK_IsRtcOscSelected	67
4.5.68	CLOCK_IsRtcOscValid	67
4.5.69	CLOCK_InitPll0	67
4.5.70	CLOCK_DeinitPll0	68
4.5.71	CLOCK_SetPll0AsyncClkDiv	68
4.5.72	CLOCK_GetPll0Freq	69
4.5.73	CLOCK_GetPll0AsyncFreq	69
4.5.74	CLOCK_GetPll0PfdFreq	69
4.5.75	CLOCK_EnablePll0PfdClkout	69
4.5.76	CLOCK_SetPll0LockTime	70
4.5.77	CLOCK_IsPll0Selected	70
4.5.78	CLOCK_IsPll0Valid	70
4.5.79	CLOCK_InitPll1	70
4.5.80	CLOCK_DeinitPll1	71
4.5.81	CLOCK_SetPll1AsyncClkDiv	71
4.5.82	CLOCK_GetPll1Freq	72
4.5.83	CLOCK_GetPll1AsyncFreq	72
4.5.84	CLOCK_GetPll1PfdFreq	72
4.5.85	CLOCK_EnablePll1PfdClkout	73

Section No.	Title	Page No.
4.5.86	CLOCK_EnablePll1SpectrumModulation	73
4.5.87	CLOCK_SetPll1LockTime	73
4.5.88	CLOCK_IsPll1Selected	74
4.5.89	CLOCK_IsPll1Valid	74
4.5.90	CLOCK_GetPll3Freq	74
4.5.91	CLOCK_GetPll3AsyncFreq	74
4.5.92	CLOCK_GetPll3PfdFreq	74
4.5.93	CLOCK_InitPll4	75
4.5.94	CLOCK_DeinitPll4	76
4.5.95	CLOCK_SetPll4AsyncClkDiv	77
4.5.96	CLOCK_GetPll4Freq	77
4.5.97	CLOCK_GetPll4AsyncFreq	77
4.5.98	CLOCK_GetPll4PfdFreq	77
4.5.99	CLOCK_EnablePll4PfdClkout	78
4.5.100	CLOCK_EnablePll4SpectrumModulation	78
4.5.101	CLOCK_SetPll4LockTime	79
4.5.102	CLOCK_IsPll4Selected	79
4.5.103	CLOCK_IsPll4Valid	79
4.5.104	CLOCK_SetXtal0Freq	79
4.5.105	CLOCK_SetXtal32Freq	79
4.5.106	CLOCK_SetLvdsFreq	80
4.5.107	CLOCK_SetMclkFreq	80
4.5.108	CLOCK_SetRxBclkFreq	80
4.5.109	CLOCK_SetTxBclkFreq	80
4.5.110	CLOCK_SetSpdifRxFreq	81
4.5.111	CLOCK_GetWdogClkFreq	82
4.5.112	CLOCK_GetFlexspiClkFreq	82
4.5.113	CLOCK_GetLpitClkFreq	82
4.5.114	CLOCK_GetFlexioClkFreq	82
4.5.115	CLOCK_GetI3cClkFreq	82
4.5.116	CLOCK_GetLpspiClkFreq	83
4.5.117	CLOCK_GetAdcClkFreq	83
4.5.118	CLOCK_GetDacClkFreq	83
4.5.119	CLOCK_GetTpiuClkFreq	84
4.5.120	CLOCK_GetSwoClkFreq	84
4.5.121	CLOCK_GetTpmClkFreq	84
4.5.122	CLOCK_GetLpi2cClkFreq	84
4.5.123	CLOCK_GetLpuartClkFreq	84
4.5.124	CLOCK_GetFlexcanClkFreq	85
4.5.125	CLOCK_GetCsiClkFreq	85
4.5.126	CLOCK_GetDsiClkFreq	85
4.5.127	CLOCK_GetEpdcClkFreq	85
4.5.128	CLOCK_GetGpu2dClkFreq	85
4.5.129	CLOCK_GetGpu3dClkFreq	86
4.5.130	CLOCK_GetDcnanoClkFreq	86

Section No.	Title	Page No.
4.5.131	CLOCK_GetCsiUiClkFreq	86
4.5.132	CLOCK_GetCsiEscClkFreq	86
4.5.133	CLOCK_GetRtdAudClkFreq	86
4.5.134	CLOCK_GetAdAudClkFreq	86
4.5.135	CLOCK_GetLpavAudClkFreq	87
4.5.136	CLOCK_GetSaiFreq	87
4.5.137	CLOCK_GetSpdifFreq	87
4.5.138	CLOCK_GetMqsFreq	87
4.5.139	CLOCK_GetMicfilFreq	87
4.5.140	CLOCK_GetMrtFreq	88
4.6	Variable Documentation	88
4.6.1	g_xtal0Freq	88
4.6.2	g_xtal32Freq	88
4.6.3	g_lvdsFreq	88
4.6.4	g_mclkFreq	88
4.6.5	g_rxBclkFreq	88
4.6.6	g_txBclkFreq	89
4.6.7	g_spdifRxFreq	89

Chapter 5 Fusion Driver

Chapter 6 IOMUXC: IOMUX Controller

Chapter 7 Reset Driver

Chapter 8 Sentinel Driver

Chapter 9 Upower Driver

9.1	System Clock Generator (SCG)	95
9.1.1	Function description	95
9.1.2	Typical use case	97

Chapter 10 ACMP: Analog Comparator Driver

10.1	Overview	99
10.2	Typical use case	99
10.2.1	Normal Configuration	99
10.2.2	Interrupt Configuration	99
10.2.3	Round robin Configuration	99
10.3	Data Structure Documentation	102

Section No.	Title	Page No.
10.3.1	<code>struct acmp_config_t</code>	102
10.3.2	<code>struct acmp_channel_config_t</code>	103
10.3.3	<code>struct acmp_filter_config_t</code>	103
10.3.4	<code>struct acmp_dac_config_t</code>	104
10.3.5	<code>struct acmp_round_robin_config_t</code>	104
10.3.6	<code>struct acmp_discrete_mode_config_t</code>	105
10.4	Macro Definition Documentation	105
10.4.1	<code>FSL_ACMP_DRIVER_VERSION</code>	105
10.4.2	<code>CMP_C0_CFx_MASK</code>	105
10.5	Enumeration Type Documentation	105
10.5.1	<code>_acmp_interrupt_enable</code>	106
10.5.2	<code>_acmp_status_flags</code>	106
10.5.3	<code>acmp_hysteresis_mode_t</code>	106
10.5.4	<code>acmp_reference_voltage_source_t</code>	106
10.5.5	<code>acmp_fixed_port_t</code>	106
10.5.6	<code>acmp_dac_work_mode_t</code>	107
10.5.7	<code>acmp_discrete_clock_source_t</code>	107
10.5.8	<code>acmp_discrete_sample_time_t</code>	107
10.5.9	<code>acmp_discrete_phase_time_t</code>	107
10.6	Function Documentation	108
10.6.1	<code>ACMP_Init</code>	108
10.6.2	<code>ACMP_Deinit</code>	108
10.6.3	<code>ACMP_GetDefaultConfig</code>	108
10.6.4	<code>ACMP_Enable</code>	108
10.6.5	<code>ACMP_EnableLinkToDAC</code>	109
10.6.6	<code>ACMP_SetChannelConfig</code>	109
10.6.7	<code>ACMP_EnableDMA</code>	109
10.6.8	<code>ACMP_EnableWindowMode</code>	110
10.6.9	<code>ACMP_SetFilterConfig</code>	110
10.6.10	<code>ACMP_SetDACConfig</code>	110
10.6.11	<code>ACMP_SetRoundRobinConfig</code>	111
10.6.12	<code>ACMP_SetRoundRobinPreState</code>	111
10.6.13	<code>ACMP_GetRoundRobinStatusFlags</code>	111
10.6.14	<code>ACMP_ClearRoundRobinStatusFlags</code>	112
10.6.15	<code>ACMP_GetRoundRobinResult</code>	112
10.6.16	<code>ACMP_EnableInterrupts</code>	112
10.6.17	<code>ACMP_DisableInterrupts</code>	113
10.6.18	<code>ACMP_GetStatusFlags</code>	113
10.6.19	<code>ACMP_ClearStatusFlags</code>	113
10.6.20	<code>ACMP_SetDiscreteModeConfig</code>	113
10.6.21	<code>ACMP_GetDefaultDiscreteModeConfig</code>	114

Section No.	Title	Page No.
Chapter 11 CACHE: LMEM CACHE Memory Controller		
11.1	Overview	115
11.2	Function groups	115
11.2.1	L1 CACHE Operation	115
11.3	Macro Definition Documentation	116
11.3.1	FSL_CACHE_DRIVER_VERSION	116
11.3.2	L1CODEBUSCACHE_LINESIZE_BYTE	116
11.3.3	L1SYSTEMBUSCACHE_LINESIZE_BYTE	116
11.4	Function Documentation	116
11.4.1	ICACHE_InvalidateByRange	116
11.4.2	DCACHE_InvalidateByRange	116
11.4.3	DCACHE_CleanByRange	117
11.4.4	DCACHE_CleanInvalidateByRange	117
Chapter 12 Common Driver		
12.1	Overview	118
12.2	Macro Definition Documentation	120
12.2.1	FSL_DRIVER_TRANSFER_DOUBLE_WEAK_IRQ	120
12.2.2	MAKE_STATUS	120
12.2.3	MAKE_VERSION	121
12.2.4	FSL_COMMON_DRIVER_VERSION	121
12.2.5	DEBUG_CONSOLE_DEVICE_TYPE_NONE	121
12.2.6	DEBUG_CONSOLE_DEVICE_TYPE_UART	121
12.2.7	DEBUG_CONSOLE_DEVICE_TYPE_LPUART	121
12.2.8	DEBUG_CONSOLE_DEVICE_TYPE_LPSCI	121
12.2.9	DEBUG_CONSOLE_DEVICE_TYPE_USBCDC	121
12.2.10	DEBUG_CONSOLE_DEVICE_TYPE_FLEXCOMM	121
12.2.11	DEBUG_CONSOLE_DEVICE_TYPE_IUART	121
12.2.12	DEBUG_CONSOLE_DEVICE_TYPE_VUSART	121
12.2.13	DEBUG_CONSOLE_DEVICE_TYPE_MINI_USART	121
12.2.14	DEBUG_CONSOLE_DEVICE_TYPE_SWO	121
12.2.15	DEBUG_CONSOLE_DEVICE_TYPE_QSCI	121
12.2.16	ARRAY_SIZE	121
12.3	Typedef Documentation	121
12.3.1	status_t	121
12.4	Enumeration Type Documentation	122
12.4.1	_status_groups	122
12.4.2	anonymous enum	124

Section No.	Title	Page No.
12.5 Function Documentation		124
12.5.1 SDK_Malloc		125
12.5.2 SDK_Free		126
12.5.3 SDK_DelayAtLeastUs		126

Chapter 13 CRC: Cyclic Redundancy Check Driver

13.1 Overview		127
13.2 CRC Driver Initialization and Configuration		127
13.3 CRC Write Data		127
13.4 CRC Get Checksum		127
13.5 Comments about API usage in RTOS		128
13.6 Data Structure Documentation		129
13.6.1 struct crc_config_t		129
13.7 Macro Definition Documentation		130
13.7.1 FSL_CRC_DRIVER_VERSION		130
13.7.2 CRC_DRIVER_USE_CRC16_CCIT_FALSE_AS_DEFAULT		130
13.8 Enumeration Type Documentation		130
13.8.1 crc_bits_t		130
13.8.2 crc_result_t		130
13.9 Function Documentation		130
13.9.1 CRC_Init		130
13.9.2 CRC_Deinit		131
13.9.3 CRC_GetDefaultConfig		131
13.9.4 CRC_WriteData		131
13.9.5 CRC_Get32bitResult		132
13.9.6 CRC_Get16bitResult		132

Chapter 14 DAC12: 12-bit Digital-to-Analog Converter Driver

14.1 Overview		133
14.2 Typical use case		133
14.2.1 A simple use case to output the user-defined DAC12 value.		133
14.2.2 Working with the trigger		133
14.3 Data Structure Documentation		136
14.3.1 struct dac12_hardware_info_t		136

Section No.	Title	Page No.
14.3.2	struct dac12_config_t	136
14.4	Macro Definition Documentation	137
14.4.1	FSL_DAC12_DRIVER_VERSION	137
14.4.2	DAC12_CR_W1C_FLAGS_MASK	137
14.4.3	DAC12_CR_ALL_FLAGS_MASK	137
14.5	Enumeration Type Documentation	137
14.5.1	_dac12_status_flags	137
14.5.2	_dac12_interrupt_enable	138
14.5.3	dac12_fifo_size_info_t	138
14.5.4	dac12_fifo_work_mode_t	138
14.5.5	dac12_reference_voltage_source_t	138
14.5.6	dac12_fifo_trigger_mode_t	139
14.5.7	dac12_reference_current_source_t	139
14.5.8	dac12_speed_mode_t	139
14.6	Function Documentation	139
14.6.1	DAC12_GetHardwareInfo	139
14.6.2	DAC12_Init	140
14.6.3	DAC12_GetDefaultConfig	140
14.6.4	DAC12_Deinit	140
14.6.5	DAC12_Enable	140
14.6.6	DAC12_ResetConfig	141
14.6.7	DAC12_ResetFIFO	141
14.6.8	DAC12_GetStatusFlags	141
14.6.9	DAC12_ClearStatusFlags	141
14.6.10	DAC12_EnableInterrupts	142
14.6.11	DAC12_DisableInterrupts	142
14.6.12	DAC12_EnableDMA	142
14.6.13	DAC12_SetData	142
14.6.14	DAC12_DoSoftwareTrigger	143
14.6.15	DAC12_GetFIFOReadPointer	143
14.6.16	DAC12_GetFIFOWritePointer	143

Chapter 15 DMAMUX: Direct Memory Access Multiplexer Driver

15.1	Overview	144
15.2	Typical use case	144
15.2.1	DMAMUX Operation	144
15.3	Macro Definition Documentation	144
15.3.1	FSL_DMAMUX_DRIVER_VERSION	144
15.4	Function Documentation	144

Section No.	Title	Page No.
15.4.1	DMAMUX_Init	144
15.4.2	DMAMUX_Deinit	145
15.4.3	DMAMUX_EnableChannel	145
15.4.4	DMAMUX_DisableChannel	145
15.4.5	DMAMUX_SetSource	146

Chapter 16 eDMA: Enhanced Direct Memory Access (eDMA) Controller Driver

16.1	Overview	147
16.2	Typical use case	147
16.2.1	eDMA Operation	147
16.3	Data Structure Documentation	152
16.3.1	struct edma_config_t	152
16.3.2	struct edma_transfer_config_t	153
16.3.3	struct edma_channel_Preemption_config_t	154
16.3.4	struct edma_minor_offset_config_t	154
16.3.5	struct edma_tcd_t	154
16.3.6	struct edma_handle_t	155
16.4	Macro Definition Documentation	156
16.4.1	FSL_EDMA_DRIVER_VERSION	156
16.5	Typedef Documentation	156
16.5.1	edma_callback	156
16.6	Enumeration Type Documentation	157
16.6.1	edma_transfer_size_t	157
16.6.2	edma_modulo_t	157
16.6.3	edma_bandwidth_t	158
16.6.4	edma_channel_link_type_t	158
16.6.5	anonymous enum	158
16.6.6	anonymous enum	159
16.6.7	edma_interrupt_enable_t	159
16.6.8	edma_transfer_type_t	159
16.6.9	anonymous enum	159
16.7	Function Documentation	160
16.7.1	EDMA_Init	160
16.7.2	EDMA_Deinit	161
16.7.3	EDMA_InstallTCD	161
16.7.4	EDMA_GetDefaultConfig	161
16.7.5	EDMA_EnableContinuousChannelLinkMode	162
16.7.6	EDMA_EnableMinorLoopMapping	162
16.7.7	EDMA_ResetChannel	162

Section No.	Title	Page No.
16.7.8	EDMA_SetTransferConfig	163
16.7.9	EDMA_SetMinorOffsetConfig	163
16.7.10	EDMA_SetChannelPreemptionConfig	164
16.7.11	EDMA_SetChannelLink	164
16.7.12	EDMA_SetBandWidth	165
16.7.13	EDMA_SetModulo	165
16.7.14	EDMA_EnableAsyncRequest	166
16.7.15	EDMA_EnableAutoStopRequest	166
16.7.16	EDMA_EnableChannelInterrupts	166
16.7.17	EDMA_DisableChannelInterrupts	166
16.7.18	EDMA_SetMajorOffsetConfig	167
16.7.19	EDMA_TcdReset	167
16.7.20	EDMA_TcdSetTransferConfig	167
16.7.21	EDMA_TcdSetMinorOffsetConfig	168
16.7.22	EDMA_TcdSetChannelLink	168
16.7.23	EDMA_TcdSetBandWidth	169
16.7.24	EDMA_TcdSetModulo	169
16.7.25	EDMA_TcdEnableAutoStopRequest	170
16.7.26	EDMA_TcdEnableInterrupts	171
16.7.27	EDMA_TcdDisableInterrupts	171
16.7.28	EDMA_TcdSetMajorOffsetConfig	171
16.7.29	EDMA_EnableChannelRequest	171
16.7.30	EDMA_DisableChannelRequest	172
16.7.31	EDMA_TriggerChannelStart	172
16.7.32	EDMA_GetRemainingMajorLoopCount	172
16.7.33	EDMA_GetErrorStatusFlags	173
16.7.34	EDMA_GetChannelStatusFlags	173
16.7.35	EDMA_ClearChannelStatusFlags	173
16.7.36	EDMA_CreateHandle	174
16.7.37	EDMA_InstallTCDMemory	174
16.7.38	EDMA_SetCallback	174
16.7.39	EDMA_PreparesTransferConfig	175
16.7.40	EDMA_PreparesTransfer	175
16.7.41	EDMA_SubmitTransfer	176
16.7.42	EDMA_StartTransfer	177
16.7.43	EDMA_StopTransfer	178
16.7.44	EDMA_AbortTransfer	178
16.7.45	EDMA_GetUnusedTCDNumber	178
16.7.46	EDMA_GetNextTCDAAddress	178
16.7.47	EDMA_HandleIRQ	179
Chapter 17 EWM: External Watchdog Monitor Driver		
17.1	Overview	180

Section No.	Title	Page No.
17.2	Typical use case	180
17.3	Data Structure Documentation	181
17.3.1	struct ewm_config_t	181
17.4	Macro Definition Documentation	181
17.4.1	FSL_EWM_DRIVER_VERSION	181
17.5	Enumeration Type Documentation	181
17.5.1	_ewm_interrupt_enable_t	181
17.5.2	_ewm_status_flags_t	181
17.6	Function Documentation	182
17.6.1	EWM_Init	182
17.6.2	EWM_Deinit	182
17.6.3	EWM_GetDefaultConfig	182
17.6.4	EWM_EnableInterrupts	183
17.6.5	EWM_DisableInterrupts	183
17.6.6	EWM_GetStatusFlags	183
17.6.7	EWM_Refresh	184

Chapter 18 FlexIO: FlexIO Driver

18.1	Overview	185
18.2	FlexIO Driver	186
18.2.1	Overview	186
18.2.2	Data Structure Documentation	190
18.2.3	Macro Definition Documentation	193
18.2.4	Typedef Documentation	193
18.2.5	Enumeration Type Documentation	193
18.2.6	Function Documentation	198
18.2.7	Variable Documentation	208
18.3	FlexIO I2C Master Driver	209
18.3.1	Overview	209
18.3.2	Typical use case	209
18.3.3	Data Structure Documentation	213
18.3.4	Macro Definition Documentation	215
18.3.5	Typedef Documentation	215
18.3.6	Enumeration Type Documentation	216
18.3.7	Function Documentation	216
18.4	FlexIO I2S Driver	226
18.4.1	Overview	226
18.4.2	Typical use case	226

Section No.	Title	Page No.
18.4.3	Data Structure Documentation	231
18.4.4	Macro Definition Documentation	233
18.4.5	Enumeration Type Documentation	234
18.4.6	Function Documentation	235
18.5	FlexIO SPI Driver	246
18.5.1	Overview	246
18.5.2	Typical use case	246
18.5.3	Data Structure Documentation	252
18.5.4	Macro Definition Documentation	256
18.5.5	Typedef Documentation	256
18.5.6	Enumeration Type Documentation	256
18.5.7	Function Documentation	258
18.6	FlexIO UART Driver	271
18.6.1	Overview	271
18.6.2	Typical use case	271
18.6.3	Data Structure Documentation	279
18.6.4	Macro Definition Documentation	282
18.6.5	Typedef Documentation	282
18.6.6	Enumeration Type Documentation	283
18.6.7	Function Documentation	283

Chapter 19 GPIO: General-Purpose Input/Output Driver

19.1	Overview	295
19.2	Data Structure Documentation	295
19.2.1	struct gpio_pin_config_t	295
19.3	Macro Definition Documentation	296
19.3.1	FSL_GPIO_DRIVER_VERSION	296
19.4	Enumeration Type Documentation	296
19.4.1	gpio_pin_direction_t	296
19.5	GPIO Driver	297
19.5.1	Overview	297
19.5.2	Typical use case	297
19.5.3	Function Documentation	298
19.6	FGPIO Driver	301
19.6.1	Typical use case	301

Section No.	Title	Page No.
Chapter 20 LLWU: Low-Leakage Wakeup Unit Driver		
20.1	Overview	302
20.2	External wakeup pins configurations	302
20.3	Internal wakeup modules configurations	302
20.4	Digital pin filter for external wakeup pin configurations	302
20.5	Macro Definition Documentation	303
20.5.1	FSL_LLWU_DRIVER_VERSION	303
20.6	Enumeration Type Documentation	303
20.6.1	llwu_external_pin_mode_t	303
20.6.2	llwu_pin_filter_mode_t	303
Chapter 21 LPADC: 12-bit SAR Analog-to-Digital Converter Driver		
21.1	Overview	304
21.2	Typical use case	304
21.2.1	Polling Configuration	304
21.2.2	Interrupt Configuration	304
21.3	Data Structure Documentation	307
21.3.1	struct lpadc_config_t	307
21.3.2	struct lpadc_conv_command_config_t	308
21.3.3	struct lpadc_conv_trigger_config_t	310
21.3.4	struct lpadc_conv_result_t	310
21.4	Macro Definition Documentation	311
21.4.1	FSL_LPADC_DRIVER_VERSION	311
21.4.2	LPADC_GET_ACTIVE_COMMAND_STATUS	311
21.4.3	LPADC_GET_ACTIVE_TRIGGER_STATUE	311
21.5	Enumeration Type Documentation	311
21.5.1	_lpadc_status_flags	311
21.5.2	_lpadc_interrupt_enable	312
21.5.3	lpadc_sample_scale_mode_t	312
21.5.4	lpadc_sample_channel_mode_t	312
21.5.5	lpadc_hardware_average_mode_t	312
21.5.6	lpadc_sample_time_mode_t	313
21.5.7	lpadc_hardware_compare_mode_t	313
21.5.8	lpadc_reference_voltage_source_t	313
21.5.9	lpadc_power_level_mode_t	314

Section No.	Title	Page No.
21.5.10	lpadc_trigger_priority_policy_t	314
21.6	Function Documentation	314
21.6.1	LPADC_Init	314
21.6.2	LPADC_GetDefaultConfig	315
21.6.3	LPADC_Deinit	315
21.6.4	LPADC_Enable	315
21.6.5	LPADC_DoResetFIFO	316
21.6.6	LPADC_DoResetConfig	316
21.6.7	LPADC_GetStatusFlags	316
21.6.8	LPADC_ClearStatusFlags	316
21.6.9	LPADC_EnableInterrupts	317
21.6.10	LPADC_DisableInterrupts	317
21.6.11	LPADC_EnableFIFOWatermarkDMA	317
21.6.12	LPADC_GetConvResultCount	317
21.6.13	LPADC_GetConvResult	318
21.6.14	LPADC_SetConvTriggerConfig	318
21.6.15	LPADC_GetDefaultConvTriggerConfig	318
21.6.16	LPADC_DoSoftwareTrigger	319
21.6.17	LPADC_SetConvCommandConfig	319
21.6.18	LPADC_GetDefaultConvCommandConfig	319

Chapter 22 LPI2C: Low Power Inter-Integrated Circuit Driver

22.1	Overview	321
22.2	Macro Definition Documentation	321
22.2.1	FSL_LPI2C_DRIVER_VERSION	321
22.2.2	I2C_RETRY_TIMES	322
22.3	Enumeration Type Documentation	322
22.3.1	anonymous enum	322
22.4	LPI2C Master Driver	323
22.4.1	Overview	323
22.4.2	Data Structure Documentation	326
22.4.3	Typedef Documentation	330
22.4.4	Enumeration Type Documentation	331
22.4.5	Function Documentation	333
22.5	LPI2C Slave Driver	347
22.5.1	Overview	347
22.5.2	Data Structure Documentation	349
22.5.3	Typedef Documentation	352
22.5.4	Enumeration Type Documentation	354

Section No.	Title	Page No.
22.5.5	Function Documentation	355
22.6	LPI2C Master DMA Driver	364
22.6.1	Overview	364
22.6.2	Data Structure Documentation	364
22.6.3	Typedef Documentation	365
22.6.4	Function Documentation	367
22.7	LPI2C FreeRTOS Driver	370
22.7.1	Overview	370
22.7.2	Macro Definition Documentation	370
22.7.3	Function Documentation	370
22.8	LPI2C CMSIS Driver	373
22.8.1	LPI2C CMSIS Driver	373
Chapter 23 LPIT: Low-Power Interrupt Timer		
23.1	Overview	375
23.2	Function groups	375
23.2.1	Initialization and deinitialization	375
23.2.2	Timer period Operations	375
23.2.3	Start and Stop timer operations	375
23.2.4	Status	376
23.2.5	Interrupt	376
23.3	Typical use case	376
23.3.1	LPIT tick example	376
23.4	Data Structure Documentation	378
23.4.1	struct lpit_chnl_params_t	378
23.4.2	struct lpit_config_t	379
23.5	Enumeration Type Documentation	379
23.5.1	lpit_chnl_t	379
23.5.2	lpit_timer_modes_t	379
23.5.3	lpit_trigger_select_t	380
23.5.4	lpit_trigger_source_t	380
23.5.5	lpit_interrupt_enable_t	380
23.5.6	lpit_status_flags_t	381
23.6	Function Documentation	381
23.6.1	LPIT_Init	381
23.6.2	LPIT_Deinit	381
23.6.3	LPIT_GetDefaultConfig	381

Section No.	Title	Page No.
23.6.4	LPIT_SetupChannel	382
23.6.5	LPIT_EnableInterrupts	382
23.6.6	LPIT_DisableInterrupts	382
23.6.7	LPIT_GetEnabledInterrupts	383
23.6.8	LPIT_GetStatusFlags	384
23.6.9	LPIT_ClearStatusFlags	384
23.6.10	LPIT_SetTimerPeriod	384
23.6.11	LPIT_GetCurrentTimerCount	385
23.6.12	LPIT_StartTimer	385
23.6.13	LPIT_StopTimer	385
23.6.14	LPIT_Reset	386

Chapter 24 LPSPI: Low Power Serial Peripheral Interface

24.1	Overview	387
24.2	LPSPI Peripheral driver	388
24.2.1	Overview	388
24.2.2	Function groups	388
24.2.3	Typical use case	388
24.2.4	Data Structure Documentation	395
24.2.5	Macro Definition Documentation	401
24.2.6	Typedef Documentation	401
24.2.7	Enumeration Type Documentation	402
24.2.8	Function Documentation	407
24.2.9	Variable Documentation	422

Chapter 25 LPTMR: Low-Power Timer

25.1	Overview	423
25.2	Function groups	423
25.2.1	Initialization and deinitialization	423
25.2.2	Timer period Operations	423
25.2.3	Start and Stop timer operations	423
25.2.4	Status	424
25.2.5	Interrupt	424
25.3	Typical use case	424
25.3.1	LPTMR tick example	424
25.4	Data Structure Documentation	426
25.4.1	struct lptmr_config_t	426
25.5	Enumeration Type Documentation	427

Section No.	Title	Page No.
25.5.1	<code>lptmr_pin_select_t</code>	427
25.5.2	<code>lptmr_pin_polarity_t</code>	427
25.5.3	<code>lptmr_timer_mode_t</code>	427
25.5.4	<code>lptmr_prescaler_glitch_value_t</code>	427
25.5.5	<code>lptmr_prescaler_clock_select_t</code>	428
25.5.6	<code>lptmr_interrupt_enable_t</code>	428
25.5.7	<code>lptmr_status_flags_t</code>	428
25.6	Function Documentation	428
25.6.1	<code>LPTMR_Init</code>	428
25.6.2	<code>LPTMR_Deinit</code>	429
25.6.3	<code>LPTMR_GetDefaultConfig</code>	429
25.6.4	<code>LPTMR_EnableInterrupts</code>	429
25.6.5	<code>LPTMR_DisableInterrupts</code>	430
25.6.6	<code>LPTMR_GetEnabledInterrupts</code>	430
25.6.7	<code>LPTMR_EnableTimerDMA</code>	430
25.6.8	<code>LPTMR_GetStatusFlags</code>	430
25.6.9	<code>LPTMR_ClearStatusFlags</code>	431
25.6.10	<code>LPTMR_SetTimerPeriod</code>	431
25.6.11	<code>LPTMR_GetCurrentTimerCount</code>	431
25.6.12	<code>LPTMR_StartTimer</code>	432
25.6.13	<code>LPTMR_StopTimer</code>	432

Chapter 26 LPUART: Low Power Universal Asynchronous Receiver/Transmitter Driver

26.1	Overview	433
26.2	LPUART Driver	434
26.2.1	<code>Overview</code>	434
26.2.2	<code>Typical use case</code>	434
26.2.3	<code>Data Structure Documentation</code>	439
26.2.4	<code>Macro Definition Documentation</code>	442
26.2.5	<code>Typedef Documentation</code>	442
26.2.6	<code>Enumeration Type Documentation</code>	442
26.2.7	<code>Function Documentation</code>	445

Chapter 27 LTC: LP Trusted Cryptography

27.1	Overview	462
27.2	LTC Driver Initialization and Configuration	462
27.3	Comments about API usage in RTOS	462
27.4	Comments about API usage in interrupt handler	462

Section No.	Title	Page No.
27.5 LTC Driver Examples		463
27.5.1 Simple examples		463
27.6 Macro Definition Documentation		463
27.6.1 FSL_LTC_DRIVER_VERSION		463
27.7 Function Documentation		464
27.7.1 LTC_Init		464
27.7.2 LTC_Deinit		464
27.8 LTC Blocking APIs		466
27.8.1 Overview		466
27.8.2 LTC DES driver		467
27.8.3 LTC AES driver		468
27.8.4 LTC HASH driver		475
27.8.5 LTC PKHA driver		479

Chapter 28 MSMC: Multicore System Mode Controller

28.1 Overview		481
28.2 Typical use case		481
28.2.1 Set Core 0 from RUN to VLPR mode		481
28.2.2 Set Core 0 from VLPR/HSRUN to RUN mode		481
28.3 Typical use case		481
28.3.1 Set Core 0 from RUN to HSRUN mode		481
28.3.2 Enter wait or stop modes		481
28.4 Data Structure Documentation		485
28.4.1 struct smc_reset_pin_filter_config_t		485
28.5 Macro Definition Documentation		485
28.5.1 FSL_MSMC_DRIVER_VERSION		485
28.6 Enumeration Type Documentation		485
28.6.1 smc_power_mode_protection_t		485
28.6.2 smc_power_state_t		485
28.6.3 smc_power_stop_entry_status_t		486
28.6.4 smc_run_mode_t		486
28.6.5 smc_stop_mode_t		486
28.6.6 smc_partial_stop_option_t		486
28.6.7 anonymous enum		487
28.6.8 smc_reset_source_t		487
28.6.9 smc_interrupt_enable_t		487

Section No.	Title	Page No.
28.7 Function Documentation		487
28.7.1 SMC_SetPowerModeProtection		488
28.7.2 SMC_GetPowerModeState		488
28.7.3 SMC_PreEnterStopModes		488
28.7.4 SMC_PostExitStopModes		488
28.7.5 SMC_PreEnterWaitModes		489
28.7.6 SMC_PostExitWaitModes		489
28.7.7 SMC_SetPowerModeRun		489
28.7.8 SMC_SetPowerModeHsrun		489
28.7.9 SMC_SetPowerModeWait		489
28.7.10 SMC_SetPowerModeStop		490
28.7.11 SMC_SetPowerModeVlpr		490
28.7.12 SMC_SetPowerModeVlpw		490
28.7.13 SMC_SetPowerModeVlps		491
28.7.14 SMC_SetPowerModeLls		491
28.7.15 SMC_SetPowerModeVlls		491
28.7.16 SMC_GetPreviousResetSources		492
28.7.17 SMC_GetStickyResetSources		492
28.7.18 SMC_ClearStickyResetSources		493
28.7.19 SMC_ConfigureResetPinFilter		493
28.7.20 SMC_SetSystemResetInterruptConfig		494
28.7.21 SMC_GetResetInterruptSourcesStatus		494
28.7.22 SMC_ClearResetInterruptSourcesStatus		495
28.7.23 SMC_GetBootOptionConfig		495

Chapter 29 MU: Messaging Unit

29.1 Overview		497
29.2 Function description		497
29.2.1 MU initialization		497
29.2.2 MU message		497
29.2.3 MU flags		498
29.2.4 Status and interrupt		498
29.2.5 MU misc functions		498
29.3 Macro Definition Documentation		502
29.3.1 FSL_MU_DRIVER_VERSION		502
29.4 Enumeration Type Documentation		502
29.4.1 _mu_status_flags		502
29.4.2 _mu_interrupt_enable		503
29.4.3 _mu_interrupt_trigger		503
29.4.4 _mu_core_status_flags		503

Section No.	Title	Page No.
29.5 Function Documentation		504
29.5.1 MU_Init		504
29.5.2 MU_Deinit		504
29.5.3 MU_SendMsgNonBlocking		504
29.5.4 MU_SendMsg		505
29.5.5 MU_ReceiveMsgNonBlocking		505
29.5.6 MU_ReceiveMsg		506
29.5.7 MU_SetFlagsNonBlocking		507
29.5.8 MU_SetFlags		507
29.5.9 MU_GetFlags		508
29.5.10 MU_GetCoreStatusFlags		508
29.5.11 MU_GetStatusFlags		508
29.5.12 MU_ClearStatusFlags		509
29.5.13 MU_EnableInterrupts		509
29.5.14 MU_DisableInterrupts		510
29.5.15 MU_TriggerInterrupts		510
29.5.16 MU_TriggerNmi		511
29.5.17 MU_ClearNmi		511
29.5.18 MU_BootOtherCore		511
29.5.19 MU_HoldOtherCoreReset		512
29.5.20 MU_ResetBothSides		512
29.5.21 MU_SetClockOnOtherCoreEnable		512
29.5.22 MU_HardwareResetOtherCore		513
29.5.23 MU_MaskHardwareReset		514

Chapter 30 PMC0: Power Management Controller

30.1 Overview		515
30.2 Typical use case		515
30.2.1 Turn on the PMC 1 using LDO Regulator		515
30.2.2 Turn on the PMC 1 using the PMIC		515
30.2.3 Turn off the LDO Regulator		516
30.2.4 Turn on the LDO Regulator		516
30.2.5 Change the Core Regulator voltage level in PMC 0 RUN or HSRUN mode		516
30.2.6 Change the SRAMs power mode during PMC 0 RUN mode		516
30.3 Data Structure Documentation		520
30.3.1 struct pmc0_hsrn_mode_config_t		520
30.3.2 struct pmc0_run_mode_config_t		521
30.3.3 struct pmc0_vlpr_mode_config_t		521
30.3.4 struct pmc0_stop_mode_config_t		522
30.3.5 struct pmc0_vlps_mode_config_t		523
30.3.6 struct pmc0_lls_mode_config_t		524
30.3.7 struct pmc0_vlls_mode_config_t		526

Section No.	Title	Page No.
30.3.8	<code>struct pmc0_bias_config_t</code>	526
30.4	Enumeration Type Documentation	527
30.4.1	<code>pmc0_high_volt_detect_monitor_select_t</code>	527
30.4.2	<code>pmc0_low_volt_detect_monitor_select_t</code>	528
30.4.3	<code>pmc0_core_regulator_select_t</code>	528
30.4.4	<code>pmc0_array_regulator_select_t</code>	528
30.4.5	<code>pmc0_vlls_array_regulator_select_t</code>	528
30.4.6	<code>pmc0_fbb_p_well_voltage_level_select_t</code>	528
30.4.7	<code>pmc0_fbb_n_well_voltage_level_select_t</code>	529
30.4.8	<code>pmc0_rbb_p_well_voltage_level_select_t</code>	529
30.4.9	<code>pmc0_rbb_n_well_voltage_level_select_t</code>	529
30.4.10	<code>_pmc0_status_flags</code>	530
30.4.11	<code>_pmc0_power_mode_status_flags</code>	530
30.5	Function Documentation	530
30.5.1	<code>PMC0_ConfigureHsrunMode</code>	530
30.5.2	<code>PMC0_ConfigureRunMode</code>	531
30.5.3	<code>PMC0_ConfigureVlprMode</code>	531
30.5.4	<code>PMC0_ConfigureStopMode</code>	531
30.5.5	<code>PMC0_ConfigureVlpsMode</code>	531
30.5.6	<code>PMC0_ConfigureLlsMode</code>	532
30.5.7	<code>PMC0_ConfigureVllsMode</code>	532
30.5.8	<code>PMC0_GetPMC0PowerModeStatusFlags</code>	532
30.5.9	<code>PMC0_GetPMC0PowerTransitionStatus</code>	533
30.5.10	<code>PMC0_GetPMC1PowerModeStatusFlags</code>	533
30.5.11	<code>PMC0_GetPMC1PowerTransitionStatus</code>	533
30.5.12	<code>PMC0_GetStatusFlags</code>	533
30.5.13	<code>PMC0_EnableLowVoltDetectInterrupt</code>	534
30.5.14	<code>PMC0_DisableLowVoltDetectInterrupt</code>	534
30.5.15	<code>PMC0_ClearLowVoltDetectFlag</code>	534
30.5.16	<code>PMC0_EnableHighVoltDetectInterrupt</code>	534
30.5.17	<code>PMC0_DisableHighVoltDetectInterrupt</code>	534
30.5.18	<code>PMC0_ClearHighVoltDetectFlag</code>	534
30.5.19	<code>PMC0_EnableLowVoltDetectReset</code>	535
30.5.20	<code>PMC0_EnableHighVoltDetectReset</code>	536
30.5.21	<code>PMC0_ClearPadsIsolation</code>	536
30.5.22	<code>PMC0_PowerOnPmc1</code>	536
30.5.23	<code>PMC0_EnableWaitLdoOkSignal</code>	536
30.5.24	<code>PMC0_EnablePmc1LdoRegulator</code>	537
30.5.25	<code>PMC0_EnablePmc1RBBMode</code>	537
30.5.26	<code>PMC0_SetBiasConfig</code>	537
30.5.27	<code>PMC0_ConfigureSramBankPowerDown</code>	537
30.5.28	<code>PMC0_ConfigureSramBankPowerDownStopMode</code>	538
30.5.29	<code>PMC0_ConfigureSramBankPowerDownStandbyMode</code>	538

Section No.	Title	Page No.
30.5.30	PMC0_EnableTemperatureSensor	539
30.5.31	PMC0_SetTemperatureSensorMode	539

Chapter 31 PORT: Port Control and Interrupts

31.1	Overview	540
31.2	Macro Definition Documentation	540
31.2.1	FSL_PORT_DRIVER_VERSION	540
31.3	Enumeration Type Documentation	540
31.3.1	port_interrupt_t	540

Chapter 32 QSPI: Quad Serial Peripheral Interface

32.1	Overview	542
32.2	Quad Serial Peripheral Interface Driver	543
32.2.1	Overview	543
32.2.2	Data Structure Documentation	548
32.2.3	Macro Definition Documentation	550
32.2.4	Enumeration Type Documentation	550
32.2.5	Function Documentation	553

Chapter 33 SAI: Serial Audio Interface

33.1	Overview	563
33.2	Typical configurations	563
33.3	Typical use case	564
33.3.1	SAI Send/receive using an interrupt method	564
33.3.2	SAI Send/receive using a DMA method	564
33.4	SAI Driver	565
33.4.1	Overview	565
33.4.2	Data Structure Documentation	573
33.4.3	Macro Definition Documentation	576
33.4.4	Enumeration Type Documentation	577
33.4.5	Function Documentation	581

Chapter 34 SEMA42: Hardware Semaphores Driver

34.1	Overview	611
34.2	Typical use case	611

Section No.	Title	Page No.
34.3 Macro Definition Documentation		612
34.3.1 SEMA42_GATE_NUM_RESET_ALL		612
34.3.2 SEMA42_GATEn		613
34.4 Enumeration Type Documentation		613
34.4.1 anonymous enum		613
34.4.2 sema42_gate_status_t		613
34.5 Function Documentation		613
34.5.1 SEMA42_Init		613
34.5.2 SEMA42_Deinit		614
34.5.3 SEMA42_TryLock		614
34.5.4 SEMA42_Lock		614
34.5.5 SEMA42_Unlock		615
34.5.6 SEMA42_GetGateStatus		615
34.5.7 SEMA42_ResetGate		615
34.5.8 SEMA42_ResetAllGates		616
Chapter 35 TPM: Timer PWM Module		
35.1 Overview		617
35.2 Introduction of TPM		617
35.2.1 Initialization and deinitialization		617
35.2.2 PWM Operations		617
35.2.3 Input capture operations		618
35.2.4 Output compare operations		618
35.2.5 Quad decode		618
35.2.6 Fault operation		618
35.2.7 Status		618
35.2.8 Interrupt		618
35.3 Typical use case		618
35.3.1 PWM output		619
35.4 Data Structure Documentation		623
35.4.1 struct tpm_chnl_pwm_signal_param_t		623
35.4.2 struct tpm_dual_edge_capture_param_t		624
35.4.3 struct tpm_phase_params_t		624
35.4.4 struct tpm_config_t		625
35.5 Macro Definition Documentation		625
35.5.1 FSL TPM DRIVER VERSION		626
35.6 Enumeration Type Documentation		626
35.6.1 tpm_chnl_t		626

Section No.	Title	Page No.
35.6.2	tpm_pwm_mode_t	626
35.6.3	tpm_pwm_level_select_t	626
35.6.4	tpm_pwm_pause_level_select_t	627
35.6.5	tpm_chnl_control_bit_mask_t	627
35.6.6	tpm_trigger_select_t	627
35.6.7	tpm_trigger_source_t	627
35.6.8	tpm_ext_trigger_polarity_t	627
35.6.9	tpm_output_compare_mode_t	628
35.6.10	tpm_input_capture_edge_t	628
35.6.11	tpm_quad_decode_mode_t	628
35.6.12	tpm_phase_polarity_t	629
35.6.13	tpm_clock_source_t	629
35.6.14	tpm_clock_prescale_t	629
35.6.15	tpm_interrupt_enable_t	629
35.6.16	tpm_status_flags_t	630
35.7	Function Documentation	630
35.7.1	TPM_Init	630
35.7.2	TPM_Deinit	630
35.7.3	TPM_GetDefaultConfig	630
35.7.4	TPM_CalculateCounterClkDiv	631
35.7.5	TPM_SetupPwm	631
35.7.6	TPM_UpdatePwmDutycycle	632
35.7.7	TPM_UpdateChnlEdgeLevelSelect	632
35.7.8	TPM_GetChannelContorlBits	633
35.7.9	TPM_DisableChannel	633
35.7.10	TPM_EnableChannel	633
35.7.11	TPM_SetupInputCapture	634
35.7.12	TPM_SetupOutputCompare	634
35.7.13	TPM_SetupDualEdgeCapture	635
35.7.14	TPM_SetupQuadDecode	636
35.7.15	TPM_SetChannelPolarity	636
35.7.16	TPM_EnableChannelExtTrigger	636
35.7.17	TPM_EnableInterrupts	637
35.7.18	TPM_DisableInterrupts	637
35.7.19	TPM_GetEnabledInterrupts	637
35.7.20	TPM_GetChannelValue	638
35.7.21	TPM_GetStatusFlags	638
35.7.22	TPM_ClearStatusFlags	638
35.7.23	TPM_SetTimerPeriod	639
35.7.24	TPM_GetCurrentTimerCount	639
35.7.25	TPM_StartTimer	640
35.7.26	TPM_StopTimer	641
35.7.27	TPM_Reset	641

Section No.	Title	Page No.
Chapter 36 TRGMUX: Trigger Mux Driver		
36.1	Overview	642
36.2	Typical use case	642
36.3	Macro Definition Documentation	642
36.3.1	FSL_TRGMUX_DRIVER_VERSION	642
36.4	Enumeration Type Documentation	642
36.4.1	anonymous enum	643
36.4.2	trgmux_trigger_input_t	643
36.5	Function Documentation	643
36.5.1	TRGMUX_LockRegister	643
36.5.2	TRGMUX_SetTriggerSource	643
Chapter 37 TRNG: True Random Number Generator		
37.1	TRNG Initialization	645
37.2	Get random data from TRNG	645
Chapter 38 TSTMR: Timestamp Timer Driver		
38.1	Overview	646
38.2	Function Documentation	646
38.2.1	TSTMR_ReadTimeStamp	646
38.2.2	TSTMR_DelayUs	646
Chapter 39 WDOG32: 32-bit Watchdog Timer		
39.1	Overview	648
39.2	Typical use case	648
39.3	Data Structure Documentation	650
39.3.1	struct wdog32_work_mode_t	650
39.3.2	struct wdog32_config_t	650
39.4	Macro Definition Documentation	650
39.4.1	FSL_WDOG32_DRIVER_VERSION	650
39.5	Enumeration Type Documentation	650
39.5.1	wdog32_clock_source_t	651

Section No.	Title	Page No.
39.5.2	wdog32_clock_prescaler_t	651
39.5.3	wdog32_test_mode_t	651
39.5.4	_wdog32_interrupt_enable_t	651
39.5.5	_wdog32_status_flags_t	651

39.6	Function Documentation	652
39.6.1	WDOG32_GetDefaultConfig	652
39.6.2	WDOG32_Init	652
39.6.3	WDOG32_Deinit	653
39.6.4	WDOG32_Unlock	653
39.6.5	WDOG32_Enable	653
39.6.6	WDOG32_Disable	653
39.6.7	WDOG32_EnableInterrupts	655
39.6.8	WDOG32_DisableInterrupts	655
39.6.9	WDOG32_GetStatusFlags	655
39.6.10	WDOG32_ClearStatusFlags	656
39.6.11	WDOG32_SetTimeoutValue	656
39.6.12	WDOG32_SetWindowSize	657
39.6.13	WDOG32_Refresh	657
39.6.14	WDOG32_GetCounterValue	657

Chapter 40 Debug Console

40.1	Overview	658
40.2	Function groups	658
40.2.1	Initialization	658
40.2.2	Advanced Feature	659
40.2.3	SDK_DEBUGCONSOLE and SDK_DEBUGCONSOLE_UART	663
40.3	Typical use case	664
40.4	Macro Definition Documentation	666
40.4.1	DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN	666
40.4.2	DEBUGCONSOLE_REDIRECT_TO_SDK	666
40.4.3	DEBUGCONSOLE_DISABLE	666
40.4.4	SDK_DEBUGCONSOLE	666
40.4.5	PRINTF	666
40.5	Function Documentation	666
40.5.1	DbgConsole_Init	666
40.5.2	DbgConsole_Deinit	667
40.5.3	DbgConsole_EnterLowpower	667
40.5.4	DbgConsole_ExitLowpower	668
40.5.5	DbgConsole_Printf	668

Section No.	Title	Page No.
40.5.6	DbgConsole_Vprintf	668
40.5.7	DbgConsole_Putchar	668
40.5.8	DbgConsole_Scanf	669
40.5.9	DbgConsole_Getchar	669
40.5.10	DbgConsole_BlockingPrintf	670
40.5.11	DbgConsole_BlockingVprintf	670
40.5.12	DbgConsole_Flush	670
40.5.13	StrFormatPrintf	671
40.5.14	StrFormatScanf	671

Chapter 41 Notification Framework

41.1	Overview	672
41.2	Notifier Overview	672
41.3	Data Structure Documentation	674
41.3.1	struct notifier_notification_block_t	674
41.3.2	struct notifier_callback_config_t	675
41.3.3	struct notifier_handle_t	675
41.4	Typedef Documentation	676
41.4.1	notifier_user_config_t	676
41.4.2	notifier_user_function_t	676
41.4.3	notifier_callback_t	677
41.5	Enumeration Type Documentation	677
41.5.1	_notifier_status	677
41.5.2	notifier_policy_t	678
41.5.3	notifier_notification_type_t	678
41.5.4	notifier_callback_type_t	678
41.6	Function Documentation	678
41.6.1	NOTIFIER_CreateHandle	679
41.6.2	NOTIFIER_SwitchConfig	680
41.6.3	NOTIFIER_GetErrorCallbackIndex	681

Chapter 42 Shell

42.1	Overview	682
42.2	Function groups	682
42.2.1	Initialization	682
42.2.2	Advanced Feature	682
42.2.3	Shell Operation	682

Section No.	Title	Page No.
42.3 Data Structure Documentation		684
42.3.1 struct shell_command_t		684
42.4 Macro Definition Documentation		685
42.4.1 SHELL_NON_BLOCKING_MODE		685
42.4.2 SHELL_AUTO_COMPLETE		685
42.4.3 SHELL_BUFFER_SIZE		685
42.4.4 SHELL_MAX_ARGS		685
42.4.5 SHELL_HISTORY_COUNT		685
42.4.6 SHELL_HANDLE_SIZE		685
42.4.7 SHELL_USE_COMMON_TASK		685
42.4.8 SHELL_TASK_PRIORITY		685
42.4.9 SHELL_TASK_STACK_SIZE		685
42.4.10 SHELL_HANDLE_DEFINE		686
42.4.11 SHELL_COMMAND_DEFINE		686
42.4.12 SHELL_COMMAND		687
42.5 Typedef Documentation		687
42.5.1 cmd_function_t		687
42.6 Enumeration Type Documentation		687
42.6.1 shell_status_t		687
42.7 Function Documentation		687
42.7.1 SHELL_Init		687
42.7.2 SHELL_RegisterCommand		688
42.7.3 SHELL_UnregisterCommand		689
42.7.4 SHELL_Write		689
42.7.5 SHELL_Printf		689
42.7.6 SHELL_WriteSynchronization		690
42.7.7 SHELL_PrintfSynchronization		690
42.7.8 SHELL_ChangePrompt		691
42.7.9 SHELL_PrintPrompt		691
42.7.10 SHELL_Task		691
42.7.11 SHELL_checkRunningInIsr		692

Chapter 43 CODEC Driver

43.1 Overview	693
43.2 CODEC Common Driver	694
43.2.1 Overview	694
43.2.2 Data Structure Documentation	699
43.2.3 Macro Definition Documentation	700
43.2.4 Enumeration Type Documentation	700

Section No.	Title	Page No.
43.2.5	Function Documentation	705
43.3	CODEC I2C Driver	709
43.3.1	Overview	709
43.3.2	Data Structure Documentation	710
43.3.3	Enumeration Type Documentation	710
43.3.4	Function Documentation	710
Chapter 44 Serial Manager		
44.1	Overview	713
44.2	Data Structure Documentation	716
44.2.1	struct serial_manager_config_t	716
44.2.2	struct serial_manager_callback_message_t	716
44.3	Macro Definition Documentation	716
44.3.1	SERIAL_MANAGER_WRITE_TIME_DELAY_DEFAULT_VALUE	717
44.3.2	SERIAL_MANAGER_READ_TIME_DELAY_DEFAULT_VALUE	717
44.3.3	SERIAL_MANAGER_USE_COMMON_TASK	717
44.3.4	SERIAL_MANAGER_HANDLE_SIZE	717
44.3.5	SERIAL_MANAGER_HANDLE_DEFINE	717
44.3.6	SERIAL_MANAGER_WRITE_HANDLE_DEFINE	717
44.3.7	SERIAL_MANAGER_READ_HANDLE_DEFINE	718
44.3.8	SERIAL_MANAGER_TASK_PRIORITY	718
44.3.9	SERIAL_MANAGER_TASK_STACK_SIZE	718
44.4	Enumeration Type Documentation	718
44.4.1	serial_port_type_t	718
44.4.2	serial_manager_type_t	719
44.4.3	serial_manager_status_t	719
44.5	Function Documentation	719
44.5.1	SerialManager_Init	719
44.5.2	SerialManager_Deinit	720
44.5.3	SerialManager_OpenWriteHandle	721
44.5.4	SerialManager_CloseWriteHandle	722
44.5.5	SerialManager_OpenReadHandle	722
44.5.6	SerialManager_CloseReadHandle	723
44.5.7	SerialManager_WriteBlocking	724
44.5.8	SerialManager_ReadBlocking	724
44.5.9	SerialManager_EnterLowpower	725
44.5.10	SerialManager_ExitLowpower	725
44.5.11	SerialManager_needPollingIsr	726

Section No.	Title	Page No.
Chapter 45 Lpspi_cmsis_driver		
45.1 Function groups	727
45.1.1 LPSPI CMSIS GetVersion Operation	727
45.1.2 LPSPI CMSIS GetCapabilities Operation	727
45.1.3 LPSPI CMSIS Initialize and Uninitialize Operation	727
45.1.4 LPSPI Transfer Operation	727
45.1.5 LPSPI Status Operation	727
45.1.6 LPSPI CMSIS Control Operation	728
45.2 Typical use case	728
45.2.1 Master Operation	728
45.2.2 Slave Operation	728
Chapter 46 Lpuart_cmsis_driver		
46.1 Function groups	729
46.1.1 LPUART CMSIS GetVersion Operation	729
46.1.2 LPUART CMSIS GetCapabilities Operation	729
46.1.3 LPUART CMSIS Initialize and Uninitialize Operation	729
46.1.4 LPUART CMSIS Transfer Operation	729
46.1.5 LPUART CMSIS Status Operation	730
46.1.6 LPUART CMSIS Control Operation	730
Chapter 47 Flexio_edma_i2s		
47.1 Overview	731
47.2 Data Structure Documentation	732
47.2.1 struct _flexio_i2s_edma_handle	732
47.3 Macro Definition Documentation	732
47.3.1 FSL_FLEXIO_I2S_EDMA_DRIVER_VERSION	733
47.4 Function Documentation	733
47.4.1 FLEXIO_I2S_TransferTxCreateHandleEDMA	733
47.4.2 FLEXIO_I2S_TransferRxCreateHandleEDMA	733
47.4.3 FLEXIO_I2S_TransferSetFormatEDMA	734
47.4.4 FLEXIO_I2S_TransferSendEDMA	734
47.4.5 FLEXIO_I2S_TransferReceiveEDMA	735
47.4.6 FLEXIO_I2S_TransferAbortSendEDMA	735
47.4.7 FLEXIO_I2S_TransferAbortReceiveEDMA	735
47.4.8 FLEXIO_I2S_TransferGetSendCountEDMA	736
47.4.9 FLEXIO_I2S_TransferGetReceiveCountEDMA	736

Section No.	Title	Page No.
Chapter 48 Flexio_edma_spi		
48.1 Overview	737
48.2 Data Structure Documentation	738
48.2.1 struct _flexio_spi_master_edma_handle	738
48.3 Macro Definition Documentation	738
48.3.1 FSL_FLEXIO_SPI_EDMA_DRIVER_VERSION	738
48.4 Typedef Documentation	738
48.4.1 flexio_spi_slave_edma_handle_t	739
48.5 Function Documentation	739
48.5.1 FLEXIO_SPI_MasterTransferCreateHandleEDMA	739
48.5.2 FLEXIO_SPI_MasterTransferEDMA	739
48.5.3 FLEXIO_SPI_MasterTransferAbortEDMA	740
48.5.4 FLEXIO_SPI_MasterTransferGetCountEDMA	740
48.5.5 FLEXIO_SPI_SlaveTransferCreateHandleEDMA	740
48.5.6 FLEXIO_SPI_SlaveTransferEDMA	741
48.5.7 FLEXIO_SPI_SlaveTransferAbortEDMA	741
48.5.8 FLEXIO_SPI_SlaveTransferGetCountEDMA	742
Chapter 49 Flexio_edma_uart		
49.1 Overview	743
49.2 Data Structure Documentation	744
49.2.1 struct _flexio_uart_edma_handle	744
49.3 Macro Definition Documentation	744
49.3.1 FSL_FLEXIO_UART_EDMA_DRIVER_VERSION	744
49.4 Typedef Documentation	744
49.4.1 flexio_uart_edma_transfer_callback_t	745
49.5 Function Documentation	745
49.5.1 FLEXIO_UART_TransferCreateHandleEDMA	745
49.5.2 FLEXIO_UART_TransferSendEDMA	745
49.5.3 FLEXIO_UART_TransferReceiveEDMA	746
49.5.4 FLEXIO_UART_TransferAbortSendEDMA	746
49.5.5 FLEXIO_UART_TransferAbortReceiveEDMA	746
49.5.6 FLEXIO_UART_TransferGetSendCountEDMA	747
49.5.7 FLEXIO_UART_TransferGetReceiveCountEDMA	747

Section No.	Title	Page No.
Chapter 50 Lpspi_edma_driver		
50.1 Overview	749
50.2 Data Structure Documentation	750
50.2.1 struct _lpspi_master_edma_handle	750
50.2.2 struct _lpspi_slave_edma_handle	752
50.3 Macro Definition Documentation	754
50.3.1 FSL_LPSPI_EDMA_DRIVER_VERSION	754
50.4 Typedef Documentation	754
50.4.1 lpspi_master_edma_transfer_callback_t	754
50.4.2 lpspi_slave_edma_transfer_callback_t	754
50.5 Function Documentation	754
50.5.1 LPSPI_MasterTransferCreateHandleEDMA	755
50.5.2 LPSPI_MasterTransferEDMA	755
50.5.3 LPSPI_MasterTransferAbortEDMA	756
50.5.4 LPSPI_MasterTransferGetCountEDMA	756
50.5.5 LPSPI_SlaveTransferCreateHandleEDMA	756
50.5.6 LPSPI_SlaveTransferEDMA	757
50.5.7 LPSPI_SlaveTransferAbortEDMA	758
50.5.8 LPSPI_SlaveTransferGetCountEDMA	759
Chapter 51 LPSPI FreeRTOS Driver		
51.1 Overview	760
51.2 Macro Definition Documentation	760
51.2.1 FSL_LPSPI_FREERTOS_DRIVER_VERSION	760
51.3 Function Documentation	760
51.3.1 LPSPI_RTOS_Init	760
51.3.2 LPSPI_RTOS_Deinit	761
51.3.3 LPSPI_RTOS_Transfer	761
Chapter 52 Lpuart_edma_driver		
52.1 Overview	762
52.2 Data Structure Documentation	763
52.2.1 struct _lpuart_edma_handle	763
52.3 Macro Definition Documentation	763
52.3.1 FSL_LPUART_EDMA_DRIVER_VERSION	763

Section No.	Title	Page No.
52.4	Typedef Documentation	763
52.4.1	lpuart_edma_transfer_callback_t	764
52.5	Function Documentation	764
52.5.1	LPUART_TransferCreateHandleEDMA	764
52.5.2	LPUART_SendEDMA	764
52.5.3	LPUART_ReceiveEDMA	765
52.5.4	LPUART_TransferAbortSendEDMA	765
52.5.5	LPUART_TransferAbortReceiveEDMA	765
52.5.6	LPUART_TransferGetSendCountEDMA	766
52.5.7	LPUART_TransferGetReceiveCountEDMA	766
52.5.8	LPUART_TransferEdmaHandleIRQ	767

Chapter 53 Lpuart_freertos_driver

53.1	Overview	768
53.2	Data Structure Documentation	768
53.2.1	struct lpuart_rtos_config_t	768
53.3	Macro Definition Documentation	769
53.3.1	FSL_LPUART_FREERTOS_DRIVER_VERSION	769
53.4	Function Documentation	769
53.4.1	LPUART_RTOS_Init	769
53.4.2	LPUART_RTOS_Deinit	770
53.4.3	LPUART_RTOS_Send	770
53.4.4	LPUART_RTOS_Receive	770
53.4.5	LPUART_RTOS_SetRxTimeout	771
53.4.6	LPUART_RTOS_SetTxTimeout	771

Chapter 54 Ltc_edma_driver

54.1	Overview	772
54.2	Data Structure Documentation	772
54.2.1	struct _ltc_edma_handle	772
54.3	Macro Definition Documentation	774
54.3.1	FSL_LTC_EDMA_DRIVER_VERSION	774
54.4	Typedef Documentation	774
54.4.1	ltc_edma_callback_t	774
54.4.2	ltc_edma_state_machine_t	774
54.5	Function Documentation	774

Section No.	Title	Page No.
54.5.1	LTC_CreateHandleEDMA	774
Chapter 55 Ltc_edma_driver_aes		
55.1	Overview	776
55.2	Function Documentation	776
55.2.1	LTC_AES_EncryptEcbEDMA	776
55.2.2	LTC_AES_DecryptEcbEDMA	777
55.2.3	LTC_AES_EncryptCbcEDMA	778
55.2.4	LTC_AES_DecryptCbcEDMA	779
55.2.5	LTC_AES_CryptCtrEDMA	780
Chapter 56 Qspi_edma_driver		
56.1	Overview	782
56.2	Data Structure Documentation	783
56.2.1	struct _qspi_edma_handle	783
56.3	Macro Definition Documentation	783
56.3.1	FSL_QSPI_EDMA_DRIVER_VERSION	783
56.4	Function Documentation	783
56.4.1	QSPI_TransferTxCreateHandleEDMA	783
56.4.2	QSPI_TransferRxCreateHandleEDMA	784
56.4.3	QSPI_TransferSendEDMA	784
56.4.4	QSPI_TransferReceiveEDMA	784
56.4.5	QSPI_TransferAbortSendEDMA	785
56.4.6	QSPI_TransferAbortReceiveEDMA	785
56.4.7	QSPI_TransferGetSendCountEDMA	785
56.4.8	QSPI_TransferGetReceiveCountEDMA	786
56.5	SAI EDMA Driver	787
56.5.1	Overview	787
56.5.2	Data Structure Documentation	788
56.5.3	Function Documentation	789
56.6	Da7212	800
56.6.1	Overview	800
56.6.2	Data Structure Documentation	802
56.6.3	Macro Definition Documentation	804
56.6.4	Enumeration Type Documentation	804
56.6.5	Function Documentation	806
56.6.6	Da7212_adapter	811
56.6.7	CODEC Adapter	819

Section No.	Title	Page No.
56.6.8	Sgtl5000_adapter	820
56.6.9	Wm8960_adapter	828
56.7	Sgtl5000	836
56.7.1	Overview	836
56.7.2	Data Structure Documentation	838
56.7.3	Macro Definition Documentation	839
56.7.4	Enumeration Type Documentation	839
56.7.5	Function Documentation	841
56.8	Wm8960	847
56.8.1	Overview	847
56.8.2	Data Structure Documentation	850
56.8.3	Macro Definition Documentation	851
56.8.4	Enumeration Type Documentation	852
56.8.5	Function Documentation	854
56.9	Serial_port_swo	860
56.9.1	Overview	860
56.9.2	Data Structure Documentation	860
56.9.3	Enumeration Type Documentation	860
56.10	Serial_port_uart	861
56.10.1	Overview	861
56.10.2	Enumeration Type Documentation	861

Chapter 1

Introduction

The MCUXpresso Software Development Kit (MCUXpresso SDK) is a collection of software enablement for NXP Microcontrollers that includes peripheral drivers, multicore support and integrated RTOS support for FreeRTOS™. In addition to the base enablement, the MCUXpresso SDK is augmented with demo applications, driver example projects, and API documentation to help users quickly leverage the support provided by MCUXpresso SDK. The [MCUXpresso SDK Web Builder](#) is available to provide access to all MCUXpresso SDK packages. See the *MCUXpresso Software Development Kit (SDK) Release Notes* (document MCUXSDKRNN) in the Supported Devices section at [MCUXpresso-SDK: Software Development Kit for MCUXpresso](#) for details.

The MCUXpresso SDK is built with the following runtime software components:

- Arm® and DSP standard libraries, and CMSIS-compliant device header files which provide direct access to the peripheral registers.
- Peripheral drivers that provide stateless, high-performance, ease-of-use APIs. Communication drivers provide higher-level transactional APIs for a higher-performance option.
- RTOS wrapper driver built on top of MCUXpresso SDK peripheral drivers and leverage native RTOS services to better comply to the RTOS cases.
- Real time operation systems (RTOS) for FreeRTOS OS.
- Stacks and middleware in source or object formats including:
 - CMSIS-DSP, a suite of common signal processing functions.
 - The MCUXpresso SDK comes complete with software examples demonstrating the usage of the peripheral drivers, RTOS wrapper drivers, middleware, and RTOSes.

All demo applications and driver examples are provided with projects for the following toolchains:

- IAR Embedded Workbench
- GNU Arm Embedded Toolchain

The peripheral drivers and RTOS driver wrappers can be used across multiple devices within the product family without modification. The configuration items for each driver are encapsulated into C language data structures. Device-specific configuration information is provided as part of the MCUXpresso SDK and need not be modified by the user. If necessary, the user is able to modify the peripheral driver and RTOS wrapper driver configuration during runtime. The driver examples demonstrate how to configure the drivers by passing the proper configuration data to the APIs. The folder structure is organized to reduce the total number of includes required to compile a project.

The rest of this document describes the API references in detail for the peripheral drivers and RTOS wrapper drivers. For the latest version of this and other MCUXpresso SDK documents, see the [mcuxpresso.nxp.com/apidoc/](#).



Deliverable	Location
Demo Applications	<install_dir>/boards/<board_name>/demo_apps
Driver Examples	<install_dir>/boards/<board_name>/driver_examples
Documentation	<install_dir>/docs
Middleware	<install_dir>/middleware
Drivers	<install_dir>/<device_name>/drivers/
CMSIS Standard Arm Cortex-M Headers, math and DSP Libraries	<install_dir>/CMSIS
Device Startup and Linker	<install_dir>/<device_name>/<toolchain>/
MCUXpresso SDK Utilities	<install_dir>/devices/<device_name>/utilities
RTOS Kernel Code	<install_dir>/rtos

MCUXpresso SDK Folder Structure

Chapter 2

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Chapter 3

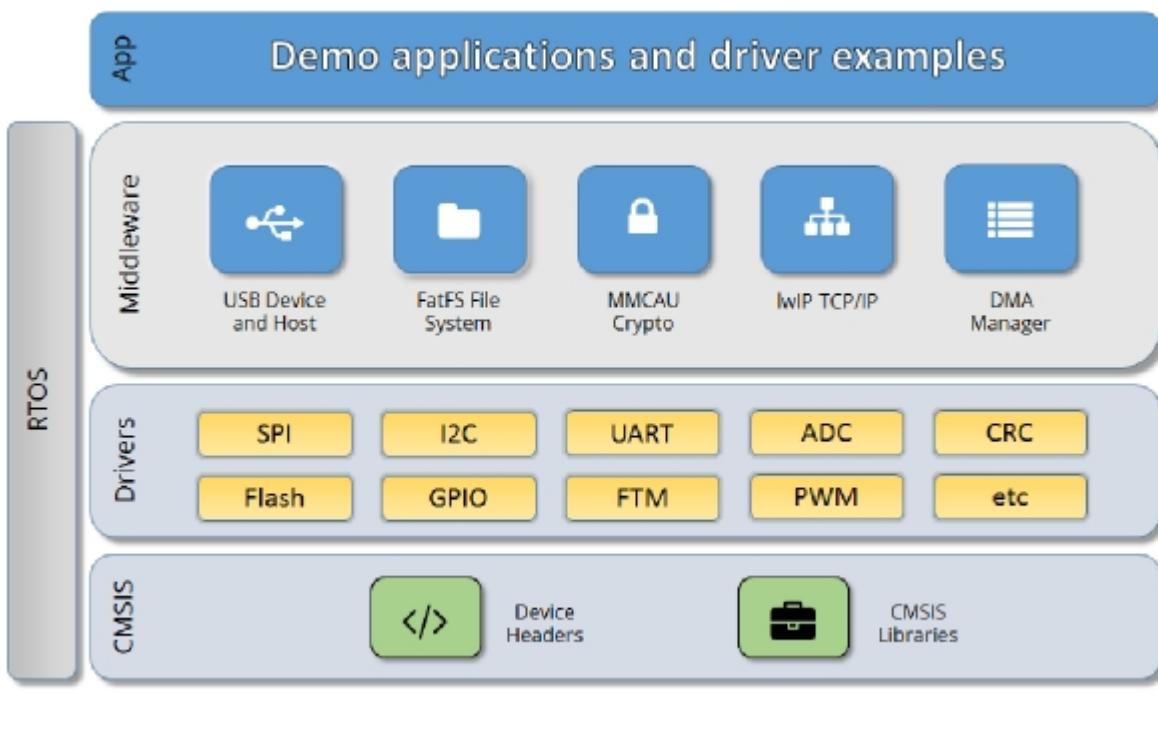
Architectural Overview

This chapter provides the architectural overview for the MCUXpresso Software Development Kit (MCUXpresso SDK). It describes each layer within the architecture and its associated components.

Overview

The MCUXpresso SDK architecture consists of five key components listed below.

1. The Arm Cortex Microcontroller Software Interface Standard (CMSIS) CORE compliance device-specific header files, SOC Header, and CMSIS math/DSP libraries.
2. Peripheral Drivers
3. Real-time Operating Systems (RTOS)
4. Stacks and Middleware that integrate with the MCUXpresso SDK
5. Demo Applications based on the MCUXpresso SDK



MCU header files

Each supported MCU device in the MCUXpresso SDK has an overall System-on Chip (SoC) memory-

mapped header file. This header file contains the memory map and register base address for each peripheral and the IRQ vector table with associated vector numbers. The overall SoC header file provides access to the peripheral registers through pointers and predefined bit masks. In addition to the overall SoC memory-mapped header file, the MCUXpresso SDK includes a feature header file for each device. The feature header file allows NXP to deliver a single software driver for a given peripheral. The feature file ensures that the driver is properly compiled for the target SOC.

CMSIS Support

Along with the SoC header files and peripheral extension header files, the MCUXpresso SDK also includes common CMSIS header files for the Arm Cortex-M core and the math and DSP libraries from the latest CMSIS release. The CMSIS DSP library source code is also included for reference.

MCUXpresso SDK Peripheral Drivers

The MCUXpresso SDK peripheral drivers mainly consist of low-level functional APIs for the MCU product family on-chip peripherals and also of high-level transactional APIs for some bus drivers/DM-A driver/eDMA driver to quickly enable the peripherals and perform transfers.

All MCUXpresso SDK peripheral drivers only depend on the CMSIS headers, device feature files, fsl_common.h, and fsl_clock.h files so that users can easily pull selected drivers and their dependencies into projects. With the exception of the clock/power-relevant peripherals, each peripheral has its own driver. Peripheral drivers handle the peripheral clock gating/ungating inside the drivers during initialization and deinitialization respectively.

Low-level functional APIs provide common peripheral functionality, abstracting the hardware peripheral register accesses into a set of stateless basic functional operations. These APIs primarily focus on the control, configuration, and function of basic peripheral operations. The APIs hide the register access details and various MCU peripheral instantiation differences so that the application can be abstracted from the low-level hardware details. The API prototypes are intentionally similar to help ensure easy portability across supported MCUXpresso SDK devices.

Transactional APIs provide a quick method for customers to utilize higher-level functionality of the peripherals. The transactional APIs utilize interrupts and perform asynchronous operations without user intervention. Transactional APIs operate on high-level logic that requires data storage for internal operation context handling. However, the Peripheral Drivers do not allocate this memory space. Rather, the user passes in the memory to the driver for internal driver operation. Transactional APIs ensure the NVIC is enabled properly inside the drivers. The transactional APIs do not meet all customer needs, but provide a baseline for development of custom user APIs.

Note that the transactional drivers never disable an NVIC after use. This is due to the shared nature of interrupt vectors on devices. It is up to the user to ensure that NVIC interrupts are properly disabled after usage is complete.

Interrupt handling for transactional APIs

A double weak mechanism is introduced for drivers with transactional API. The double weak indicates two levels of weak vector entries. See the examples below:

```
PUBWEAK SPI0_IRQHandler  
PUBWEAK SPI0_DriverIRQHandler  
SPI0_IRQHandler
```

```
LDR      R0, =SPI0_DriverIRQHandler  
BX      R0
```

The first level of the weak implementation are the functions defined in the vector table. In the devices/<DEVICE_NAME>/<TOOLCHAIN>/startup_<DEVICE_NAME>.s/.S file, the implementation of the first layer weak function calls the second layer of weak function. The implementation of the second layer weak function (ex. SPI0_DriverIRQHandler) jumps to itself (B). The MCUXpresso SDK drivers with transactional APIs provide the reimplementation of the second layer function inside of the peripheral driver. If the MCUXpresso SDK drivers with transactional APIs are linked into the image, the SPI0_DriverIRQHandler is replaced with the function implemented in the MCUXpresso SDK SPI driver.

The reason for implementing the double weak functions is to provide a better user experience when using the transactional APIs. For drivers with a transactional function, call the transactional APIs and the drivers complete the interrupt-driven flow. Users are not required to redefine the vector entries out of the box. At the same time, if users are not satisfied by the second layer weak function implemented in the MCUXpresso SDK drivers, users can redefine the first layer weak function and implement their own interrupt handler functions to suit their implementation.

The limitation of the double weak mechanism is that it cannot be used for peripherals that share the same vector entry. For this use case, redefine the first layer weak function to enable the desired peripheral interrupt functionality. For example, if the MCU's UART0 and UART1 share the same vector entry, redefine the UART0_UART1_IRQHandler according to the use case requirements.

Feature Header Files

The peripheral drivers are designed to be reusable regardless of the peripheral functional differences from one MCU device to another. An overall Peripheral Feature Header File is provided for the MCUXpresso SDK-supported MCU device to define the features or configuration differences for each sub-family device.

Application

See the *Getting Started with MCUXpresso SDK* document (MCUXSDKGSUG).

Chapter 4

Clock Driver

4.1 Overview

The MCUXpresso SDK provides APIs for MCUXpresso SDK devices' clock operation.

The clock driver supports:

- Clock generator (SOSC, FRO, PLL and so on) configuration
- Clock mux and divider configuration
- Getting clock frequency

Modules

- System Clock Generator (SCG)

Files

- file `fsl_clock.h`

Data Structures

- struct `cgc_rtd_sys_clk_config_t`
CGC system clock configuration for RTD. [More...](#)
- struct `cgc_hifi_sys_clk_config_t`
CGC system clock configuration for HIFI4 DSP. [More...](#)
- struct `cgc_lpav_sys_clk_config_t`
CGC system clock configuration for LPAV. [More...](#)
- struct `cgc_ddr_sys_clk_config_t`
CGC system clock configuration for DDR in LPAV. [More...](#)
- struct `cgc_sosc_config_t`
CGC system OSC configuration. [More...](#)
- struct `cgc_fro_config_t`
CGC FRO clock configuration. [More...](#)
- struct `cgc_lposec_config_t`
CGC LPOSC clock configuration. [More...](#)
- struct `cgc_pll0_config_t`
CGC PLL0 configuration. [More...](#)
- struct `cgc_rosc_config_t`
CGC RTC OSC configuration. [More...](#)
- struct `cgc_pll1_config_t`
CGC PLL1 configuration. [More...](#)
- struct `cgc_pll4_config_t`
CGC PLL4 configuration. [More...](#)

Macros

- `#define FSL_SDK_DISABLE_DRIVER_CLOCK_CONTROL 0`
Configure whether driver controls clock.
- `#define CGC_PLLPFD_PFD_VAL(pfdClkout, fracValue) ((uint32_t)((uint32_t)(fracValue) << (uint32_t)(pfdClkout)))
CGC (A/S)PLLPFD[PFDx] value.`
- `#define CGC_PLLPFD_PFD_MASK(pfdClkout) ((uint32_t)((uint32_t)(CGC_PLL0PFDCFG_PFD0_MASK) << (uint32_t)(pfdClkout)))
CGC (A/S)PLLPFD[PFD] mask.`
- `#define CGC_PLLPFD_PFD_VALID_MASK(pfdClkout) ((uint32_t)((uint32_t)CGC_PLL0PFD-CFG_PFD0_VALID_MASK << (uint32_t)(pfdClkout)))
CGC (A/S)PLLPFD[PFDx_VALID] mask.`
- `#define CGC_PLLPFD_PFD_CLKGATE_MASK(pfdClkout) ((uint32_t)((uint32_t)CGC_PLL0PFD-FCFG_PFD0_CLKGATE_MASK << (uint32_t)(pfdClkout)))
CGC (A/S)PLLPFD[PFDx_CLKGATE] mask.`
- `#define PCC_CLKCFG_PCD_MASK (0x7U)`
Re-define PCC register masks and bitfield operations to unify the different namings in the soc header file.
- `#define PCC_PCS_VAL(reg) (((reg)&PCC_CLKCFG_PCS_MASK) >> PCC_CLKCFG_PCS_SHIFT)`
Bitfield values for general PCC registers.
- `#define CLOCK_IP_SOURCE_PCC_INDEX(idx) ((idx) << 8U)`
Clock source index macros for clock_ip_src_t.
- `#define PCC_PCS_AVAIL_MASK (0x2U)`
Define PCC bit available mask for clock_ip_name_t.
- `#define IP_NAME_NON_PCC_FLAG_MASK ((uint32_t)1U << 30)`
Define Non-PCC register flag mask for clock_ip_name_t.
- `#define PCC_REG(name) (*(volatile uint32_t *)((uint32_t)(name) & ~(PCC_PCS_AVAIL_MASK | PCC_PCD_FRAC_AVAIL_MASK)))`
Define PCC register content for clock_ip_name_t.
- `#define GPIO_CLOCKS`
Clock ip name array for GPIO2P.
- `#define SAI_CLOCKS`
Clock ip name array for SAI.
- `#define PCTL_CLOCKS`
Clock ip name array for PCTL.
- `#define LPI2C_CLOCKS`
Clock ip name array for LPI2C.
- `#define I3C_CLOCKS`
Clock ip name array for I3C.
- `#define FLEXIO_CLOCKS`
Clock ip name array for FLEXIO.
- `#define FLEXCAN_CLOCKS`
Clock ip name array for FLEXCAN.
- `#define PDM_CLOCKS`
Clock ip name array for PDM.
- `#define LCDIF_CLOCKS`
Clock ip name array for LCDIF/DCNANO.
- `#define MIPI_DSI_HOST_CLOCKS`
Clock ip name array for MIPI DSI.
- `#define EDMA_CLOCKS`

- `#define EDMA_CHAN_CLOCKS`
Clock ip name array for EDMA.
- `#define LPUART_CLOCKS`
Clock ip name array for LPUART.
- `#define DAC_CLOCKS`
Clock ip name array for DAC.
- `#define LPTMR_CLOCKS`
Clock ip name array for LPTMR.
- `#define LPADC_CLOCKS`
Clock ip name array for LPADC.
- `#define LPSPI_CLOCKS`
Clock ip name array for LPSPI.
- `#define TPM_CLOCKS`
Clock ip name array for TPM.
- `#define LPIT_CLOCKS`
Clock ip name array for LPIT.
- `#define CMP_CLOCKS`
Clock ip name array for CMP.
- `#define WDOG_CLOCKS`
Clock ip name array for MU.
- `#define SEMA42_CLOCKS`
Clock ip name array for SEMA42.
- `#define TPIU_CLOCKS`
Clock ip name array for TPIU.
- `#define FLEXSPI_CLOCKS`
Clock ip name array for QSPI.
- `#define MRT_CLOCKS`
Clock ip name array for MRT.
- `#define BBNSM_CLOCKS`
Clock ip name array for BBNSM.
- `#define PXP_CLOCKS`
Clock ip name array for PXP.
- `#define EPDC_CLOCKS`
Clock ip name array for EPDC.

Enumerations

- enum `clock_name_t` {
 `kCLOCK_Cm33CorePlatClk`,
 `kCLOCK_Cm33BusClk`,
 `kCLOCK_Cm33SlowClk`,
 `kCLOCK_FusionDspCorePlatClk`,
 `kCLOCK_FusionDspBusClk`,
 `kCLOCK_FusionDspSlowClk`,
 `kCLOCK_XbarBusClk`,
 `kCLOCK_HifiDspClk`,
 `kCLOCK_HifiNicPlatClk`,
 `kCLOCK_NicLpavAxiClk`,
 `kCLOCK_NicLpavAhbClk`,
 `kCLOCK_NicLpavBusClk`,
 `kCLOCK_DdrClk`,
 `kCLOCK_SysOscClk`,
 `kCLOCK_FroClk`,
 `kCLOCK_LpOscClk`,
 `kCLOCK_RtcOscClk`,
 `kCLOCK_LvdsClk`,
 `kCLOCK_RtdFroDiv1Clk`,
 `kCLOCK_RtdFroDiv2Clk`,
 `kCLOCK_RtdFroDiv3Clk`,
 `kCLOCK_RtdSysOscDiv1Clk`,
 `kCLOCK_RtdSysOscDiv2Clk`,
 `kCLOCK_RtdSysOscDiv3Clk`,
 `kCLOCK_AdFroDiv1Clk`,
 `kCLOCK_AdFroDiv2Clk`,
 `kCLOCK_AdFroDiv3Clk`,
 `kCLOCK_AdSysOscDiv1Clk`,
 `kCLOCK_AdSysOscDiv2Clk`,
 `kCLOCK_AdSysOscDiv3Clk`,
 `kCLOCK_LpavFroDiv1Clk`,
 `kCLOCK_LpavFroDiv2Clk`,
 `kCLOCK_LpavFroDiv3Clk`,
 `kCLOCK_LpavSysOscDiv1Clk`,
 `kCLOCK_LpavSysOscDiv2Clk`,
 `kCLOCK_LpavSysOscDiv3Clk`,
 `kCLOCK_Pll0Clk`,
 `kCLOCK_Pll1Clk`,
 `kCLOCK_Pll3Clk`,
 `kCLOCK_Pll4Clk`,
 `kCLOCK_Pll0Pfd0Clk`,
 `kCLOCK_Pll0Pfd1Clk`,
 `kCLOCK_Pll0Pfd2Clk`,
 `kCLOCK_Pll0Pfd3Clk`,
 `kCLOCK_Pll1Pfd0Clk`,
 `kCLOCK_Pll1Pfd1Clk`,
 `kCLOCK_Pll1Pfd2Clk`,

kCLOCK_Pll4Pfd3Div2Clk }

Clock name used to get clock frequency.

- enum **clock_ip_src_t** {

kCLOCK_IpSrcNone = 0U,
 kCLOCK_Pcc0PlatIpSrcSysOscDiv1,
 kCLOCK_Pcc0PlatIpSrcFroDiv1,
 kCLOCK_Pcc0PlatIpSrcCm33Plat,
 kCLOCK_Pcc0PlatIpSrcFro,
 kCLOCK_Pcc0PlatIpSrcPll0Pfd3,
 kCLOCK_Pcc0BusIpSrcLpo = CLOCK_IP_SOURCE_PCC_INDEX(0U) | 1U,
 kCLOCK_Pcc0BusIpSrcSysOscDiv2,
 kCLOCK_Pcc0BusIpSrcFroDiv2,
 kCLOCK_Pcc0BusIpSrcCm33Bus,
 kCLOCK_Pcc0BusIpSrcPll1Pfd1Div,
 kCLOCK_Pcc0BusIpSrcPll0Pfd2Div,
 kCLOCK_Pcc0BusIpSrcPll0Pfd1Div,
 kCLOCK_Pcc1PlatIpSrcSysOscDiv1,
 kCLOCK_Pcc1PlatIpSrcFroDiv1,
 kCLOCK_Pcc1PlatIpSrcCm33Plat,
 kCLOCK_Pcc1PlatIpSrcFro,
 kCLOCK_Pcc1PlatIpSrcPll0Pfd3,
 kCLOCK_Pcc1BusIpSrcLpo = CLOCK_IP_SOURCE_PCC_INDEX(1U) | 1U,
 kCLOCK_Pcc1BusIpSrcSysOscDiv2,
 kCLOCK_Pcc1BusIpSrcFroDiv2,
 kCLOCK_Pcc1BusIpSrcCm33Bus,
 kCLOCK_Pcc1BusIpSrcPll1VcoDiv,
 kCLOCK_Pcc1BusIpSrcPll0Pfd2Div,
 kCLOCK_Pcc1BusIpSrcPll0Pfd1Div,
 kCLOCK_Pcc2BusIpSrcLpo = CLOCK_IP_SOURCE_PCC_INDEX(2U) | 1U,
 kCLOCK_Pcc2BusIpSrcSysOscDiv3,
 kCLOCK_Pcc2BusIpSrcFroDiv3,
 kCLOCK_Pcc2BusIpSrcFusionDspBus,
 kCLOCK_Pcc2BusIpSrcPll1VcoDiv,
 kCLOCK_Pcc2BusIpSrcPll0Pfd2Div,
 kCLOCK_Pcc2BusIpSrcPll0Pfd1Div,
 kCLOCK_Pcc3BusIpSrcLpo = CLOCK_IP_SOURCE_PCC_INDEX(3U) | 1U,
 kCLOCK_Pcc3BusIpSrcSysOscDiv2,
 kCLOCK_Pcc3BusIpSrcFroDiv2,
 kCLOCK_Pcc3BusIpSrcXbarBus = CLOCK_IP_SOURCE_PCC_INDEX(3U) | 4U,
 kCLOCK_Pcc3BusIpSrcPll3Pfd1Div1,
 kCLOCK_Pcc3BusIpSrcPll3Pfd0Div2,
 kCLOCK_Pcc3BusIpSrcPll3Pfd0Div1,
 kCLOCK_Pcc4PlatIpSrcSysOscDiv1,
 kCLOCK_Pcc4PlatIpSrcFroDiv1,
 kCLOCK_Pcc4PlatIpSrcPll3Pfd3Div2,
 kCLOCK_Pcc4PlatIpSrcPll3Pfd3Div1,
 kCLOCK_Pcc4PlatIpSrcPll3Pfd2Div2,
 kCLOCK_Pcc4PlatIpSrcPll3Pfd2Div1,
 kCLOCK_Pcc4PlatIpSrcPll3Pfd1Div2,
 kCLOCK_Pcc4BusIpSrcMux6SdrSourceIndex(4U) | 2U,
 kCLOCK_Pcc4BusIpSrcSysOscDiv2,
 kCLOCK_Pcc4BusIpSrcFroDiv2,

`kCLOCK_LpavTpm8ClkSrcPll4Pfd3Div1 }`

Clock source for peripherals that support various clock selections.

- enum `clock_lptmr_src_t` {

`kCLOCK_LptmrSrcLPO1M` = 0U,

`kCLOCK_LptmrSrcRtc1K` = 1U,

`kCLOCK_LptmrSrcRtc32K` = 2U,

`kCLOCK_LptmrSrcSysOsc` = 3U }

Clock source for LPTMR.

- enum `clock_ip_name_t`

Peripheral clock name definition used for clock gate, clock source and clock divider setting.

- enum {

`kStatus_CGC_Busy` = MAKE_STATUS(kStatusGroup_SCG, 1),

`kStatus_CGC_InvalidSrc` = MAKE_STATUS(kStatusGroup_SCG, 2) }

CGC status return codes.

- enum `cgc_sys_clk_t` {

`kCGC_SysClkSlow`,

`kCGC_SysClkBus`,

`kCGC_SysClkCorePlat`,

`kCGC_SysClkHifi4`,

`kCGC_SysClkNicHifi`,

`kCGC_SysClkLpavAxi`,

`kCGC_SysClkLpavAhb`,

`kCGC_SysClkLpavBus` }

CGC system clock type.

- enum `cgc_rtd_sys_clk_src_t` {

`kCGC_RtdSysClkSrcFro` = 0U,

`kCGC_RtdSysClkSrcPll0Pfd0` = 1U,

`kCGC_RtdSysClkSrcPll1Pfd0` = 2U,

`kCGC_RtdSysClkSrcSysOsc` = 3U,

`kCGC_RtdSysClkSrcRtcOsc` = 4U,

`kCGC_RtdSysClkSrcLvds` = 5U,

`kCGC_RtdSysClkSrcPll0` = 6U }

CGC system clock source for RTD.

- enum `cgc_nic_sys_clk_src_t` {

`kCGC_NicSysClkSrcFro` = 0U,

`kCGC_NicSysClkSrcPll3Pfd0` = 1U,

`kCGC_NicSysClkSrcSysOsc` = 2U,

`kCGC_NicSysClkSrcLvds` = 3U }

CGC system clock source for NIC in AD.

- enum `cgc_hifi_sys_clk_src_t` {

`kCGC_HifiSysClkSrcFro` = 0U,

`kCGC_HifiSysClkSrcPll4` = 1U,

`kCGC_HifiSysClkSrcPll4Pfd0` = 2U,

`kCGC_HifiSysClkSrcSysOsc` = 3U,

`kCGC_HifiSysClkSrcLvds` = 4U }

CGC system clock source for HIFI4 in LPAV.

- enum `cgc_lpav_sys_clk_src_t` {

```
kCGC_LpavSysClkSrcFro = 0U,
kCGC_LpavSysClkSrcPll4Pfd1 = 1U,
kCGC_LpavSysClkSrcSysOsc = 2U,
kCGC_LpavSysClkSrcLvdS = 3U }
```

CGC system clock source for LPAV.

- enum `cgc_ddr_sys_clk_src_t` {
 kCGC_DdrSysClkSrcFro = 0U,
 kCGC_DdrSysClkSrcPll4Pfd1 = 1U,
 kCGC_DdrSysClkSrcSysOsc = 2U,
 kCGC_DdrSysClkSrcLvdS = 3U }
- CGC system clock source for DDR.*
- enum `clock_rtd_clkout_src_t` {
 kClockRtdClkoutSelCm33Core = 0U,
 kClockRtdClkoutSelCm33Bus = 1U,
 kClockRtdClkoutSelCm33Slow = 2U,
 kClockRtdClkoutSelFusionDspCore = 3U,
 kClockRtdClkoutSelFusionDspBus = 4U,
 kClockRtdClkoutSelFusionDspSlow = 5U,
 kClockRtdClkoutSelFro48 = 6U,
 kClockRtdClkoutSelPll0VcoDiv = 7U,
 kClockRtdClkoutSelPll1VcoDiv = 8U,
 kClockRtdClkoutSelSysOsc = 9U,
 kClockRtdClkoutSelLpOsc = 10U }

CGC clock out configuration (CLKOUTCFG) in RTD.

- enum `clock_lpav_clkout_src_t` {
 kClockLpavClkoutSelHifi4 = 0U,
 kClockLpavClkoutSelNicHifi = 1U,
 kClockLpavClkoutSelLpavAxi = 2U,
 kClockLpavClkoutSelLpavAhb = 3U,
 kClockLpavClkoutSelLpavBus = 4U,
 kClockLpavClkoutSelDdr = 5U,
 kClockLpavClkoutSelFro48 = 6U,
 kClockLpavClkoutSelPll4VcoDiv = 7U,
 kClockLpavClkoutSelSysOsc = 9U,
 kClockLpavClkoutSelLpOsc = 10U }

CGC clock out configuration (CLKOUTCFG) in LPAV.

- enum `cgc_async_clk_t` {

```

kCGC_AsyncDiv1Clk = 1U,
kCGC_AsyncDiv2Clk = 2U,
kCGC_AsyncDiv3Clk = 3U,
kCGC_AsyncVcoClk = 4U,
kCGC_AsyncPfd0Div1Clk = 5U,
kCGC_AsyncPfd0Div2Clk = 6U,
kCGC_AsyncPfd1Div1Clk = 7U,
kCGC_AsyncPfd1Div2Clk = 8U,
kCGC_AsyncPfd2Div1Clk = 9U,
kCGC_AsyncPfd2Div2Clk = 10U,
kCGC_AsyncPfd3Div1Clk = 11U,
kCGC_AsyncPfd3Div2Clk = 12U }

```

CGC asynchronous clock type.

- enum `cgc_sosc_monitor_mode_t` {

kCGC_SysOscMonitorDisable = 0U,

kCGC_SysOscMonitorInt = CGC_SOSCCSR_SOSCCM_MASK,

kCGC_SysOscMonitorReset }
CGC system OSC monitor mode.
- enum `cgc_sosc_mode_t` {

kCGC_SysOscModeExt = 0U,

kCGC_SysOscModeOscLowPower = CGC_SOSCCFG_SYSOSC_BYPASS_EN_MASK,

kCGC_SysOscModeOscHighGain = CGC_SOSCCFG_SYSOSC_BYPASS_EN_MASK | CGC_SOSCCFG_HGO_MASK }
OSC work mode.
- enum `_cgc_sosc_enable_mode` {

kCGC_SysOscEnableInDeepSleep = CGC_SOSCCSR_SOSCDSEN_MASK,

kCGC_SysOscEnableInPowerDown = CGC_SOSCCSR_SOSCPDEN_MASK }
OSC enable mode.
- enum `_cgc_fro_enable_mode` { kCGC_FroEnableInDeepSleep = CGC_FROCSR_FRODSEN_MASK }
- enum `_cgc_lposc_enable_mode` {

kCGC_LposcEnableInDeepSleep = CGC_LPOSCCSR_LPOSCDSEN_MASK,

kCGC_LposcEnableInPowerDown = CGC_LPOSCCSR_LPOSCPDEN_MASK }
LPOSC enable mode.
- enum `cgc_pll_src_t` {

kCGC_PlISrcSysOsc,

kCGC_PlISrcFro24M }
CGC PLL clock source.
- enum `_cgc_pll_enable_mode` {

kCGC_PlIEnable = CGC_PLL0CSR_PLL0EN_MASK,

kCGC_PlIEnableInDeepSleep = CGC_PLL0CSR_PLL0DSEN_MASK }
PLL enable mode.
- enum `cgc_pll_pfd_clkout_t` {

kCGC_PlIPfd0Clk = 0U,

kCGC_PlIPfd1Clk = 8U,

kCGC_PlIPfd2Clk = 16U,

- ```
kCGC_PllPfd3Clk = 24U }
```

*CGC PLL PFD clouk out select.*
- enum `cgc_pll0_mult_t` {
 

```
kCGC_Pll0Mult15 = 1U,
```

```
kCGC_Pll0Mult16 = 2U,
```

```
kCGC_Pll0Mult20 = 3U,
```

```
kCGC_Pll0Mult22 = 4U,
```

```
kCGC_Pll0Mult25 = 5U,
```

```
kCGC_Pll0Mult30 = 6U }
```

*PLL0 Multiplication Factor.*
- enum `cgc_rtc_osc_monitor_mode_t` {
 

```
kCGC_RtcOscMonitorDisable = 0U,
```

```
kCGC_RtcOscMonitorInt = CGC_ROSCCTRL_ROSCCM_MASK,
```

```
kCGC_RtcOscMonitorReset }
```

*CGC RTC OSC monitor mode.*
- enum `cgc_pll1_mult_t` {
 

```
kCGC_Pll1Mult16 = 16U,
```

```
kCGC_Pll1Mult17 = 17U,
```

```
kCGC_Pll1Mult20 = 20U,
```

```
kCGC_Pll1Mult22 = 22U,
```

```
kCGC_Pll1Mult27 = 27U,
```

```
kCGC_Pll1Mult33 = 33U }
```

*PLL1 Multiplication Factor.*
- enum `cgc_pll4_mult_t` {
 

```
kCGC_Pll4Mult16 = 16U,
```

```
kCGC_Pll4Mult17 = 17U,
```

```
kCGC_Pll4Mult20 = 20U,
```

```
kCGC_Pll4Mult22 = 22U,
```

```
kCGC_Pll4Mult27 = 27U,
```

```
kCGC_Pll4Mult33 = 33U }
```

*PLL4 Multiplication Factor.*
- enum `cgc_rtd_audclk_src_t` {
 

```
kCGC_RtdAudClkSrcExtMclk0 = 0,
```

```
kCGC_RtdAudClkSrcExtMclk1 = 1,
```

```
kCGC_RtdAudClkSrcSai0RxBclk = 2,
```

```
kCGC_RtdAudClkSrcSai0TxBclk = 3,
```

```
kCGC_RtdAudClkSrcSai1RxBclk = 4,
```

```
kCGC_RtdAudClkSrcSai1TxBclk = 5,
```

```
kCGC_RtdAudClkSrcSai2RxBclk = 6,
```

```
kCGC_RtdAudClkSrcSai2TxBclk = 7,
```

```
kCGC_RtdAudClkSrcSai3RxBclk = 8,
```

```
kCGC_RtdAudClkSrcSai3TxBclk = 9 }
```

*AUD\_CLK0 source in RTD.*
- enum `cgc_ad_audclk_src_t` {

```
kCGC_AdAudClkSrcExtMclk2 = 0,
kCGC_AdAudClkSrcSai4RxBclk = 1,
kCGC_AdAudClkSrcSai4TxBclk = 2,
kCGC_AdAudClkSrcSai5RxBclk = 3,
kCGC_AdAudClkSrcSai5TxBclk = 4 }
```

*AUD\_CLK1 source in AD.*

- enum `cgc_lpav_audclk_src_t` {
 

```
kCGC_LpavAudClkSrcExtMclk3 = 0,
kCGC_LpavAudClkSrcSai6RxBclk = 1,
kCGC_LpavAudClkSrcSai6TxBclk = 2,
kCGC_LpavAudClkSrcSai7RxBclk = 3,
kCGC_LpavAudClkSrcSai7TxBclk = 4,
kCGC_LpavAudClkSrcSpdifRx = 5 }
```

*AUD\_CLK2 source in LPAV.*

## Functions

- static void `CLOCK_EnableClock (clock_ip_name_t name)`

*Enable the clock for specific IP.*
- static void `CLOCK_DisableClock (clock_ip_name_t name)`

*Disable the clock for specific IP.*
- static bool `CLOCK_IsEnabledByOtherCore (clock_ip_name_t name)`

*Check whether the clock is already enabled and configured by any other core.*
- void `CLOCK_SetIpSrc (clock_ip_name_t name, clock_ip_src_t src)`

*Set the clock source for specific IP module.*
- void `CLOCK_SetIpSrcDiv (clock_ip_name_t name, clock_ip_src_t src, uint8_t divValue, uint8_t fracValue)`

*Set the clock source and divider for specific IP module.*
- static void `CLOCK_SetRtdAudClkSrc (cgc_rtd_audclk_src_t src)`

*Set the AUD\_CLK0 source in RTD.*
- static void `CLOCK_SetAdAudClkSrc (cgc_ad_audclk_src_t src)`

*Set the AUD\_CLK1 source in AD.*
- static void `CLOCK_SetLpavAudClkSrc (cgc_lpav_audclk_src_t src)`

*Set the AUD\_CLK2 source in LPAV.*
- uint32\_t `CLOCK_GetFreq (clock_name_t clockName)`

*Gets the clock frequency for a specific clock name.*
- uint32\_t `CLOCK_GetCm33CorePlatClkFreq (void)`

*Get the CM33 core/platform clock frequency.*
- uint32\_t `CLOCK_GetCm33BusClkFreq (void)`

*Get the CM33 bus clock frequency.*
- uint32\_t `CLOCK_GetCm33SlowClkFreq (void)`

*Get the CM33 slow clock frequency.*
- uint32\_t `CLOCK_GetFusionDspCorePlatClkFreq (void)`

*Get the Fusion DSP core/platform clock frequency.*
- uint32\_t `CLOCK_GetFusionDspBusClkFreq (void)`

*Get the Fusion DSP bus clock frequency.*
- uint32\_t `CLOCK_GetFusionDspSlowClkFreq (void)`

*Get the Fusion DSP slow clock frequency.*
- uint32\_t `CLOCK_GetLvdsClkFreq (void)`

*Get the external LVDS pad clock frequency (LVDS).*

- `uint32_t CLOCK_GetIpFreq (clock_ip_name_t name)`  
*Gets the clock frequency for a specific IP module.*

## Variables

- `volatile uint32_t g_xtal0Freq`  
*External XTAL (SYSOSC) clock frequency.*
- `volatile uint32_t g_xtal32Freq`  
*External XTAL32/EXTAL32 clock frequency.*
- `volatile uint32_t g_lvdsFreq`  
*External LVDS pad clock frequency.*
- `volatile uint32_t g_mclkFreq [4]`  
*External MCLK pad clock frequency.*
- `volatile uint32_t g_rxBclkFreq [8]`  
*External RX\_BCLK pad clock frequency.*
- `volatile uint32_t g_txBclkFreq [8]`  
*External TX\_BCLK pad clock frequency.*
- `volatile uint32_t g_spdifRxFreq`  
*Recovered SPDIF\_RX clock frequency.*

## Driver version

- `#define FSL_CLOCK_DRIVER_VERSION (MAKE_VERSION(2, 0, 0))`  
*CLOCK driver version 2.0.0.*

## MCU System Clock.

- `uint32_t CLOCK_GetCm33SysClkFreq (cgc_sys_clk_t type)`  
*Gets the CGC CM33 system clock frequency.*
- `static void CLOCK_SetCm33SysClkConfig (const cgc_rtd_sys_clk_config_t *config)`  
*Sets the system clock configuration for CM33 domain.*
- `uint32_t CLOCK_GetFusionDspSysClkFreq (cgc_sys_clk_t type)`  
*Gets the CGC Fusion DSP system clock frequency.*
- `static void CLOCK_SetFusionSysClkConfig (const cgc_rtd_sys_clk_config_t *config)`  
*Sets the system clock configuration for FusionF1 DSP domain.*
- `static void CLOCK_GetCm33SysClkConfig (cgc_rtd_sys_clk_config_t *config)`  
*Gets the system clock configuration for CM33 domain.*
- `static void CLOCK_GetFusionDspSysClkConfig (cgc_rtd_sys_clk_config_t *config)`  
*Gets the system clock configuration for FusionF1 DSP domain.*
- `static void CLOCK_SetRtdClkOutConfig (clock_rtd_elkout_src_t setting, uint8_t div, bool enable)`  
*Sets the clock out configuration in RTD.*
- `static void CLOCK_SetRtcClkOutConfig (uint8_t div)`  
*Sets the RTC\_CLOCKOUT configuration.*
- `uint32_t CLOCK_GetXbarBusClkFreq (void)`  
*Gets the CGC XBAR bus clock frequency in AD.*
- `uint32_t CLOCK_GetHifiDspSysClkFreq (cgc_sys_clk_t type)`  
*Gets the CGC HIFI DSP system clock frequency in LPAV.*
- `static void CLOCK_SetHifiDspSysClkConfig (const cgc_hifi_sys_clk_config_t *config)`  
*Sets the system clock configuration for HIFI4 DSP domain.*
- `static void CLOCK_GetHifiDspSysClkConfig (cgc_hifi_sys_clk_config_t *config)`  
*Gets the system clock configuration for HIFI4 DSP domain.*

- `uint32_t CLOCK_GetLpavSysClkFreq (cgc_sys_clk_t type)`  
*Gets the CGC NIC LPAV system clock frequency in LPAV.*
- `static void CLOCK_SetLpavSysClkConfig (const cgc_lpav_sys_clk_config_t *config)`  
*Sets the system clock configuration for NIC LPAV domain.*
- `static void CLOCK_GetLpavSysClkConfig (cgc_lpav_sys_clk_config_t *config)`  
*Gets the system clock configuration for NIC LPAV domain.*
- `uint32_t CLOCK_GetDdrClkFreq (void)`  
*Gets the CGC DDR clock frequency in LPAV.*
- `static void CLOCK_SetLpavClkOutConfig (clock_lpav_clkout_src_t setting, uint8_t div, bool enable)`  
*Sets the clock out configuration in LPAV.*

## CGC System OSC Clock.

- `status_t CLOCK_InitSysOsc (const cgc_sosc_config_t *config)`  
*Initializes the CGC system OSC.*
- `status_t CLOCK_DeinitSysOsc (void)`  
*De-initializes the CGC system OSC.*
- `void CLOCK_SetRtdSysOscAsyncClkDiv (cgc_async_clk_t asyncClk, uint8_t divider)`  
*Set the asynchronous clock divider in RTD.*
- `void CLOCK_SetAdSysOscAsyncClkDiv (cgc_async_clk_t asyncClk, uint8_t divider)`  
*Set the asynchronous clock divider in AD.*
- `void CLOCK_SetLpavSysOscAsyncClkDiv (cgc_async_clk_t asyncClk, uint8_t divider)`  
*Set the asynchronous clock divider in LPAV.*
- `uint32_t CLOCK_GetSysOscFreq (void)`  
*Gets the CGC system OSC clock frequency (SYSOSC).*
- `uint32_t CLOCK_GetRtdSysOscAsyncFreq (cgc_async_clk_t type)`  
*Gets the CGC asynchronous clock frequency from the system OSC in RTD.*
- `uint32_t CLOCK_GetAdSysOscAsyncFreq (cgc_async_clk_t type)`  
*Gets the CGC asynchronous clock frequency from the system OSC in AD.*
- `uint32_t CLOCK_GetLpavSysOscAsyncFreq (cgc_async_clk_t type)`  
*Gets the CGC asynchronous clock frequency from the system OSC in LPAV.*
- `static bool CLOCK_IsSysOscErr (void)`  
*Checks whether the system OSC clock error occurs.*
- `static void CLOCK_ClearSysOscErr (void)`  
*Clears the system OSC clock error.*
- `static void CLOCK_SetSysOscMonitorMode (cgc_sosc_monitor_mode_t mode)`  
*Sets the system OSC monitor mode.*
- `static bool CLOCK_IsSysOscSelected (void)`  
*Checks whether the system OSC clock is used as clock source.*
- `static bool CLOCK_IsSysOscValid (void)`  
*Checks whether the system OSC clock is valid.*

## CGC FRO Clock.

- `status_t CLOCK_InitFro (const cgc_fro_config_t *config)`  
*Initializes the CGC FRO clock.*
- `status_t CLOCK_DeinitFro (void)`  
*De-initializes the CGC FRO.*
- `void CLOCK_SetRtdFroAsyncClkDiv (cgc_async_clk_t asyncClk, uint8_t divider)`  
*Set the asynchronous clock divider in RTD.*

- void **CLOCK\_SetAdFroAsyncClkDiv** (`cgc_async_clk_t` asyncClk, `uint8_t` divider)  
*Set the asynchronous clock divider in AD.*
- void **CLOCK\_SetLpavFroAsyncClkDiv** (`cgc_async_clk_t` asyncClk, `uint8_t` divider)  
*Set the asynchronous clock divider in LPAV.*
- void **CLOCK\_EnableFroTuning** (bool enable)  
*Enable/Disable FRO tuning.*
- `uint32_t` **CLOCK\_GetFroFreq** (void)  
*Gets the CGC FRO clock frequency.*
- `uint32_t` **CLOCK\_GetRtdFroAsyncFreq** (`cgc_async_clk_t` type)  
*Gets the CGC asynchronous clock frequency from the FRO in RTD.*
- `uint32_t` **CLOCK\_GetAdFroAsyncFreq** (`cgc_async_clk_t` type)  
*Gets the CGC asynchronous clock frequency from the FRO in AD.*
- `uint32_t` **CLOCK\_GetLpavFroAsyncFreq** (`cgc_async_clk_t` type)  
*Gets the CGC asynchronous clock frequency from the FRO in LPAV.*
- static bool **CLOCK\_IsFroSelected** (void)  
*Checks whether the FRO clock is used as clock source.*
- static bool **CLOCK\_IsFroValid** (void)  
*Checks whether the FRO clock is valid.*

## CGC LPOSC Clock.

- `status_t` **CLOCK\_InitLposc** (`const cgc_lposc_config_t *config`)  
*Initializes the CGC LPOSC clock.*
- `status_t` **CLOCK\_DeinitLposc** (void)  
*De-initializes the CGC LPOSC.*
- static bool **CLOCK\_IsLpOscValid** (void)  
*Checks whether the LPOSC clock is valid.*
- `uint32_t` **CLOCK\_GetLpOscFreq** (void)  
*Gets the CGC LPOSC clock frequency.*

## CGC RTCOSC Clock.

- `uint32_t` **CLOCK\_GetRtcOscFreq** (void)  
*Gets the CGC RTC OSC clock frequency.*
- static bool **CLOCK\_IsRtcOscErr** (void)  
*Checks whether the RTC OSC clock error occurs.*
- static void **CLOCK\_ClearRtcOscErr** (void)  
*Clears the RTC OSC clock error.*
- void **CLOCK\_SetRtcOscMonitorMode** (`cgc_rosc_monitor_mode_t` mode)  
*Sets the RTC OSC monitor mode.*
- static bool **CLOCK\_IsRtcOscSelected** (void)  
*Checks whether the RTCOSC clock is used as clock source.*
- static bool **CLOCK\_IsRtcOscValid** (void)  
*Checks whether the RTC OSC clock is valid.*

## CGC PLL0 Clock.

- `status_t` **CLOCK\_InitPll0** (`const cgc_pll0_config_t *config`)  
*Initializes the CGC PLL0.*
- `status_t` **CLOCK\_DeinitPll0** (void)  
*De-initializes the CGC PLL0.*

- void **CLOCK\_SetPll0AsyncClkDiv** (`cgc_async_clk_t` asyncClk, `uint8_t` divider)  
*Set the asynchronous clock divider.*
- `uint32_t CLOCK_GetPll0Freq` (`void`)  
*Gets the CGC PLL0 clock frequency.*
- `uint32_t CLOCK_GetPll0AsyncFreq` (`cgc_async_clk_t` type)  
*Gets the CGC asynchronous clock frequency from the PLL0.*
- `uint32_t CLOCK_GetPll0PfdFreq` (`cgc_pll_pfd_clkout_t` pfdClkout)  
*Gets the CGC PLL0 PFD clock frequency.*
- void **CLOCK\_EnablePll0PfdClkout** (`cgc_pll_pfd_clkout_t` pfdClkout, `uint8_t` fracValue)  
*Enables the CGC PLL0 Fractional Divide (PFD) clock out with configurations.*
- static void **CLOCK\_DisablePll0PfdClkout** (`cgc_pll_pfd_clkout_t` pfdClkout)  
*Disables the CGC PLL0 Fractional Divide (PFD) clock out.*
- static void **CLOCK\_SetPll0LockTime** (`uint16_t` lockTime)  
*Sets the CGC PLL0 lock time.*
- static bool **CLOCK\_IsPll0Selected** (`void`)  
*Checks whether the PLL0 clock is used as clock source.*
- static bool **CLOCK\_IsPll0Valid** (`void`)  
*Checks whether the PLL0 clock is valid.*

## CGC PLL1 Clock.

- `status_t CLOCK_InitPll1` (`const cgc_pll1_config_t *`config)  
*Initializes the CGC PLL1.*
- `status_t CLOCK_DeinitPll1` (`void`)  
*De-initializes the CGC PLL1.*
- void **CLOCK\_SetPll1AsyncClkDiv** (`cgc_async_clk_t` asyncClk, `uint8_t` divider)  
*Set the asynchronous clock divider.*
- `uint32_t CLOCK_GetPll1Freq` (`void`)  
*Gets the CGC PLL1 clock frequency.*
- `uint32_t CLOCK_GetPll1AsyncFreq` (`cgc_async_clk_t` type)  
*Gets the CGC asynchronous clock frequency from the PLL1.*
- `uint32_t CLOCK_GetPll1PfdFreq` (`cgc_pll_pfd_clkout_t` pfdClkout)  
*Gets the CGC PLL1 PFD clock frequency.*
- void **CLOCK\_EnablePll1PfdClkout** (`cgc_pll_pfd_clkout_t` pfdClkout, `uint8_t` fracValue)  
*Enables the CGC PLL1 Fractional Divide (PFD) clock out with configurations.*
- static void **CLOCK\_DisablePll1PfdClkout** (`cgc_pll_pfd_clkout_t` pfdClkout)  
*Disables the CGC PLL1 Fractional Divide (PFD) clock out.*
- static void **CLOCK\_EnablePll1SpectrumModulation** (`uint16_t` step, `uint16_t` stop)  
*Enables the CGC PLL1 spread spectrum modulation feature with configurations.*
- static void **CLOCK\_DisablePll1SpectrumModulation** (`void`)  
*Disables the CGC PLL1 spread spectrum modulation.*
- static void **CLOCK\_SetPll1LockTime** (`uint16_t` lockTime)  
*Sets the CGC PLL1 lock time.*
- static bool **CLOCK\_IsPll1Selected** (`void`)  
*Checks whether the PLL1 clock is used as clock source.*
- static bool **CLOCK\_IsPll1Valid** (`void`)  
*Checks whether the PLL1 clock is valid.*

## CGC PLL3 Clock.

- `uint32_t CLOCK_GetPll3Freq` (`void`)

- `uint32_t CLOCK_GetPll3AsyncFreq (cgc_async_clk_t type)`  
*Gets the CGC PLL3 clock frequency.*
- `uint32_t CLOCK_GetPll3PfdFreq (cgc_pll_pfd_clkout_t pfdClkout)`  
*Gets the CGC PLL3 PFD clock frequency.*

## CGC PLL4 Clock.

- `status_t CLOCK_InitPll4 (const cgc_pll4_config_t *config)`  
*Initializes the CGC PLL4.*
- `status_t CLOCK_DeinitPll4 (void)`  
*De-initializes the CGC PLL4.*
- `void CLOCK_SetPll4AsyncClkDiv (cgc_async_clk_t asyncClk, uint8_t divider)`  
*Set the asynchronous clock divider.*
- `uint32_t CLOCK_GetPll4Freq (void)`  
*Gets the CGC PLL4 clock frequency.*
- `uint32_t CLOCK_GetPll4AsyncFreq (cgc_async_clk_t type)`  
*Gets the CGC asynchronous clock frequency from the PLL4.*
- `uint32_t CLOCK_GetPll4PfdFreq (cgc_pll_pfd_clkout_t pfdClkout)`  
*Gets the CGC PLL4 PFD clock frequency.*
- `void CLOCK_EnablePll4PfdClkout (cgc_pll_pfd_clkout_t pfdClkout, uint8_t fracValue)`  
*Enables the CGC PLL4 Fractional Divide (PFD) clock out with configurations.*
- `static void CLOCK_DisablePll4PfdClkout (cgc_pll_pfd_clkout_t pfdClkout)`  
*Disables the CGC PLL4 Fractional Divide (PFD) clock out.*
- `static void CLOCK_EnablePll4SpectrumModulation (uint16_t step, uint16_t stop)`  
*Enables the CGC PLL4 spread spectrum modulation feature with configurations.*
- `static void CLOCK_SetPll4LockTime (uint16_t lockTime)`  
*Sets the CGC PLL4 lock time.*
- `static bool CLOCK_IsPll4Selected (void)`  
*Checks whether the PLL4 clock is used as clock source.*
- `static bool CLOCK_IsPll4Valid (void)`  
*Checks whether the PLL4 clock is valid.*

## External clock frequency

- `static void CLOCK_SetXtal0Freq (uint32_t freq)`  
*Sets the XTAL0 frequency based on board settings.*
- `static void CLOCK_SetXtal32Freq (uint32_t freq)`  
*Sets the XTAL32 frequency based on board settings.*
- `static void CLOCK_SetLvdsFreq (uint32_t freq)`  
*Sets the LVDS pad frequency based on board settings.*
- `static void CLOCK_SetMclkFreq (uint32_t index, uint32_t freq)`  
*Sets the MCLK pad frequency based on Audio settings.*
- `static void CLOCK_SetRxBclkFreq (uint32_t instance, uint32_t freq)`  
*Sets the RX\_BCLK pad frequency based on Audio settings.*
- `static void CLOCK_SetTxBclkFreq (uint32_t instance, uint32_t freq)`  
*Sets the TX\_BCLK pad frequency based on Audio settings.*
- `static void CLOCK_SetSpdifRxFreq (uint32_t freq)`  
*Sets the SPDIF\_RX frequency based on Audio settings.*

## Get peripheral frequency

- `uint32_t CLOCK_GetWdogClkFreq (uint32_t instance)`  
*Gets the WDOG clock frequency in RTD and LPAV.*
- `uint32_t CLOCK_GetFlexspiClkFreq (uint32_t instance)`  
*Gets the FlexSPI clock frequency in RTD.*
- `uint32_t CLOCK_GetLpitClkFreq (void)`  
*Gets the LPIT clock frequency in RTD.*
- `uint32_t CLOCK_GetFlexioClkFreq (void)`  
*Gets the FlexIO clock frequency in RTD.*
- `uint32_t CLOCK_GetI3cClkFreq (uint32_t instance)`  
*Gets the I3C clock frequency in RTD and LPAV.*
- `uint32_t CLOCK_GetLpspiClkFreq (uint32_t instance)`  
*Gets the LPSPI clock frequency in RTD.*
- `uint32_t CLOCK_GetAdcClkFreq (uint32_t instance)`  
*Gets the ADC clock frequency.*
- `uint32_t CLOCK_GetDacClkFreq (uint32_t instance)`  
*Gets the DAC clock frequency.*
- `uint32_t CLOCK_GetTpiuClkFreq (void)`  
*Gets the TPIU clock frequency.*
- `uint32_t CLOCK_GetSwoClkFreq (void)`  
*Gets the SWO clock frequency.*
- `uint32_t CLOCK_GetTpmClkFreq (uint32_t instance)`  
*Gets the TPM clock frequency.*
- `uint32_t CLOCK_GetLpi2cClkFreq (uint32_t instance)`  
*Gets the LPI2C clock frequency in RTD.*
- `uint32_t CLOCK_GetLpuartClkFreq (uint32_t instance)`  
*Gets the LPUART clock frequency in RTD.*
- `uint32_t CLOCK_GetFlexcanClkFreq (void)`  
*Gets the FlexCAN clock frequency.*
- `uint32_t CLOCK_GetCsiClkFreq (void)`  
*Gets the CSI clock frequency.*
- `uint32_t CLOCK_GetDsiClkFreq (void)`  
*Gets the DSI clock frequency.*
- `uint32_t CLOCK_GetEpdcClkFreq (void)`  
*Gets the EPDC clock frequency.*
- `uint32_t CLOCK_GetGpu2dClkFreq (void)`  
*Gets the GPU2D clock frequency.*
- `uint32_t CLOCK_GetGpu3dClkFreq (void)`  
*Gets the GPU3D clock frequency.*
- `uint32_t CLOCK_GetDcnanoClkFreq (void)`  
*Gets the DC Nano clock frequency.*
- `uint32_t CLOCK_GetCsiUiClkFreq (void)`  
*Gets the CSI clk\_ui clock frequency.*
- `uint32_t CLOCK_GetCsiEscClkFreq (void)`  
*Gets the CSI clk\_esc clock frequency.*
- `uint32_t CLOCK_GetRtdAudClkFreq (void)`  
*Gets the audio clock frequency in RTD.*
- `uint32_t CLOCK_GetAdAudClkFreq (void)`  
*Gets the audio clock frequency in AD.*
- `uint32_t CLOCK_GetLpavAudClkFreq (void)`  
*Gets the audio clock frequency in LPAV.*

- `uint32_t CLOCK_GetSaiFreq (uint32_t instance)`  
*Gets the SAI clock frequency.*
- `uint32_t CLOCK_GetSpdifFreq (void)`  
*Gets the SPDIF clock frequency.*
- `uint32_t CLOCK_GetMqsFreq (uint32_t instance)`  
*Gets the MQS clock frequency.*
- `uint32_t CLOCK_GetMicfilFreq (void)`  
*Gets the EMICFIL clock frequency.*
- `uint32_t CLOCK_GetMrtFreq (void)`  
*Gets the MRT clock frequency.*

## 4.2 Data Structure Documentation

### 4.2.1 struct cgc\_rtd\_sys\_clk\_config\_t

#### Data Fields

- `uint32_t divSlow: 6`  
*Slow clock divider, selected division is the value of the field + 1.*
- `uint32_t __pad0__: 1`  
*Reserved.*
- `uint32_t divBus: 6`  
*Bus clock divider, selected division is the value of the field + 1.*
- `uint32_t __pad1__: 8`  
*Reserved.*
- `uint32_t divCore: 6`  
*Core/Platform clock divider, selected division is the value of the field + 1.*
- `uint32_t switchFin: 1`  
*1: Clock is running.*
- `uint32_t src: 3`  
*System clock source, see `cgc_rtd_sys_clk_src_t`.*
- `uint32_t locked: 1`  
*Clock register locked.*

#### Field Documentation

- (1) `uint32_t cgc_rtd_sys_clk_config_t::__pad0__`
  - (2) `uint32_t cgc_rtd_sys_clk_config_t::divBus`
  - (3) `uint32_t cgc_rtd_sys_clk_config_t::__pad1__`
  - (4) `uint32_t cgc_rtd_sys_clk_config_t::divCore`
  - (5) `uint32_t cgc_rtd_sys_clk_config_t::switchFin`
- 0: Clock is not running.
- (6) `uint32_t cgc_rtd_sys_clk_config_t::src`

(7) `uint32_t cgc_rtd_sys_clk_config_t::locked`

#### 4.2.2 struct cgc\_hifi\_sys\_clk\_config\_t

##### Data Fields

- `uint32_t __pad0__`: 14  
*Reserved.*
- `uint32_t divPlat`: 6  
*Platform clock divider, selected division is the value of the field + 1.*
- `uint32_t __pad1__`: 1  
*Reserved.*
- `uint32_t divCore`: 6  
*Core clock divider, selected division is the value of the field + 1.*
- `uint32_t switchFin`: 1  
*1: Clock is running.*
- `uint32_t src`: 3  
*System clock source, see [cgc\\_hifi\\_sys\\_clk\\_src\\_t](#).*
- `uint32_t locked`: 1  
*Clock register locked.*

##### Field Documentation

(1) `uint32_t cgc_hifi_sys_clk_config_t::__pad0__`

(2) `uint32_t cgc_hifi_sys_clk_config_t::divPlat`

(3) `uint32_t cgc_hifi_sys_clk_config_t::__pad1__`

(4) `uint32_t cgc_hifi_sys_clk_config_t::divCore`

(5) `uint32_t cgc_hifi_sys_clk_config_t::switchFin`

0: Clock is not running.

(6) `uint32_t cgc_hifi_sys_clk_config_t::src`

(7) `uint32_t cgc_hifi_sys_clk_config_t::locked`

#### 4.2.3 struct cgc\_ipav\_sys\_clk\_config\_t

##### Data Fields

- `uint32_t __pad0__`: 7  
*Reserved.*
- `uint32_t divBus`: 6  
*Platform clock divider, selected division is the value of the field + 1.*
- `uint32_t __pad1__`: 1  
*Reserved.*

- `uint32_t divAhb`: 6  
*Platform clock divider, selected division is the value of the field + 1.*
- `uint32_t __pad2__`: 1  
*Reserved.*
- `uint32_t divAxi`: 6  
*Core clock divider, selected division is the value of the field + 1.*
- `uint32_t switchFin`: 1  
*1: Clock is running.*
- `uint32_t src`: 2  
*System clock source, see `cgc_lpav_sys_clk_src_t`.*
- `uint32_t __pad3__`: 1  
*Reserved.*
- `uint32_t locked`: 1  
*Clock register locked.*

## Field Documentation

- (1) `uint32_t cgc_lpav_sys_clk_config_t::__pad0__`
- (2) `uint32_t cgc_lpav_sys_clk_config_t::divBus`
- (3) `uint32_t cgc_lpav_sys_clk_config_t::__pad1__`
- (4) `uint32_t cgc_lpav_sys_clk_config_t::divAhb`
- (5) `uint32_t cgc_lpav_sys_clk_config_t::__pad2__`
- (6) `uint32_t cgc_lpav_sys_clk_config_t::divAxi`
- (7) `uint32_t cgc_lpav_sys_clk_config_t::switchFin`

0: Clock is not running.

- (8) `uint32_t cgc_lpav_sys_clk_config_t::src`
- (9) `uint32_t cgc_lpav_sys_clk_config_t::__pad3__`
- (10) `uint32_t cgc_lpav_sys_clk_config_t::locked`

### 4.2.4 struct cgc\_ddr\_sys\_clk\_config\_t

## Data Fields

- `uint32_t __pad0__`: 21  
*Reserved.*
- `uint32_t divDdr`: 6  
*DDR clock divider, selected division is the value of the field + 1.*
- `uint32_t switchFin`: 1  
*1: Clock is running.*
- `uint32_t src`: 3

- `uint32_t locked`: 1  
*Clock register locked.*

#### Field Documentation

- (1) `uint32_t cgc_ddr_sys_clk_config_t::__pad0__`
  - (2) `uint32_t cgc_ddr_sys_clk_config_t::divDdr`
  - (3) `uint32_t cgc_ddr_sys_clk_config_t::switchFin`
- 0: Clock is not running.
- (4) `uint32_t cgc_ddr_sys_clk_config_t::src`
  - (5) `uint32_t cgc_ddr_sys_clk_config_t::locked`

#### 4.2.5 struct `cgc_sosc_config_t`

##### Data Fields

- `uint32_t freq`  
*System OSC frequency.*
- `cgc_sosc_monitor_mode_t monitorMode`  
*Clock monitor mode selected.*
- `uint8_t enableMode`  
*Enable mode, OR'ed value of \_cgc\_sosc\_enable\_mode.*
- `cgc_sosc_mode_t workMode`  
*OSC work mode.*

#### Field Documentation

- (1) `uint32_t cgc_sosc_config_t::freq`
- (2) `cgc_sosc_monitor_mode_t cgc_sosc_config_t::monitorMode`
- (3) `uint8_t cgc_sosc_config_t::enableMode`
- (4) `cgc_sosc_mode_t cgc_sosc_config_t::workMode`

#### 4.2.6 struct `cgc_fro_config_t`

##### Data Fields

- `uint32_t enableMode`  
*Enable mode, OR'ed value of \_cgc\_fro\_enable\_mode.*

#### Field Documentation

(1) `uint32_t cgc_fro_config_t::enableMode`

#### 4.2.7 struct `cgc_lposc_config_t`

##### Data Fields

- `uint32_t enableMode`  
*Enable mode, OR'ed value of \_cgc\_lposc\_enable\_mode.*

##### Field Documentation

(1) `uint32_t cgc_lposc_config_t::enableMode`

#### 4.2.8 struct `cgc_pll0_config_t`

##### Data Fields

- `uint8_t enableMode`  
*Enable mode, OR'ed value of \_cgc\_pll\_enable\_mode.*
- `uint8_t div1`  
*PLLDIV\_VCO divider value.*
- `uint8_t pfd1Div`  
*PLLDIV\_PFD\_0 DIV1 divider value.*
- `uint8_t pfd2Div`  
*PLLDIV\_PFD\_0 DIV2 divider value.*
- `cgc_pll_src_t src`  
*Clock source.*
- `cgc_pll0_mult_t mult`  
*PLL multiplier.*

##### Field Documentation

(1) `uint8_t cgc_pll0_config_t::div1`

Disabled when div1 == 0.

(2) `uint8_t cgc_pll0_config_t::pfd1Div`

Disabled when pfd1Div == 0.

(3) `uint8_t cgc_pll0_config_t::pfd2Div`

Disabled when pfd2Div == 0.

(4) `cgc_pll_src_t cgc_pll0_config_t::src`

(5) `cgc_pll0_mult_t cgc_pll0_config_t::mult`

## 4.2.9 struct cgc\_rosr\_config\_t

### Data Fields

- `cgc_rosr_monitor_mode_t monitorMode`  
*Clock monitor mode selected.*

#### Field Documentation

(1) `cgc_rosr_monitor_mode_t cgc_rosr_config_t::monitorMode`

## 4.2.10 struct cgc\_pll1\_config\_t

### Data Fields

- `uint8_t enableMode`  
*Enable mode, OR'ed value of \_cgc\_pll\_enable\_mode.*
- `uint8_t div1`  
*PLLDIV\_VCO divider value.*
- `uint8_t pfd1Div`  
*PLLDIV\_PFD\_0 DIV1 divider value.*
- `uint8_t pfd2Div`  
*PLLDIV\_PFD\_0 DIV2 divider value.*
- `cgc_pll_src_t src`  
*Clock source.*
- `cgc_pll1_mult_t mult`  
*PLL1 multiplier.*
- `uint32_t num: 30`  
*30-bit numerator of the PLL1 Fractional-Loop divider.*
- `uint32_t denom: 30`  
*30-bit denominator of the PLL1 Fractional-Loop divider.*

#### Field Documentation

(1) `uint8_t cgc_pll1_config_t::div1`

Disabled when div1 == 0.

(2) `uint8_t cgc_pll1_config_t::pfd1Div`

Disabled when pfd1Div == 0.

(3) `uint8_t cgc_pll1_config_t::pfd2Div`

Disabled when pfd2Div == 0.

(4) `cgc_pll_src_t cgc_pll1_config_t::src`

(5) `cgc_pll1_mult_t cgc_pll1_config_t::mult`

- (6) `uint32_t cgc_pll1_config_t::num`
- (7) `uint32_t cgc_pll1_config_t::denom`

#### 4.2.11 `struct cgc_pll4_config_t`

##### Data Fields

- `uint8_t enableMode`  
*Enable mode, OR'ed value of \_cgc\_pll\_enable\_mode.*
- `uint8_t div1`  
*PLLDIV\_VCO divider value.*
- `uint8_t pfd0Div1`  
*PLLDIV\_PFD\_0 DIV1 divider value.*
- `uint8_t pfd0Div2`  
*PLLDIV\_PFD\_0 DIV2 divider value.*
- `uint8_t pfd1Div1`  
*PLLDIV\_PFD\_0 DIV3 divider value.*
- `uint8_t pfd1Div2`  
*PLLDIV\_PFD\_0 DIV4 divider value.*
- `uint8_t pfd2Div1`  
*PLLDIV\_PFD\_1 DIV1 divider value.*
- `uint8_t pfd2Div2`  
*PLLDIV\_PFD\_1 DIV2 divider value.*
- `uint8_t pfd3Div1`  
*PLLDIV\_PFD\_2 DIV3 divider value.*
- `uint8_t pfd3Div2`  
*PLLDIV\_PFD\_2 DIV4 divider value.*
- `cgc_pll_src_t src`  
*Clock source.*
- `cgc_pll4_mult_t mult`  
*PLL4 multiplier.*
- `uint32_t num: 30`  
*30-bit numerator of the PLL4 Fractional-Loop divider.*
- `uint32_t denom: 30`  
*30-bit denominator of the PLL4 Fractional-Loop divider.*

##### Field Documentation

- (1) `uint8_t cgc_pll4_config_t::div1`

Disabled when div1 == 0.

- (2) `uint8_t cgc_pll4_config_t::pfd0Div1`

Disabled when pfd0Div1 == 0.

- (3) `uint8_t cgc_pll4_config_t::pfd0Div2`

Disabled when pfd0Div2 == 0.

(4) `uint8_t cgc_pll4_config_t::pfld1Div1`

Disabled when pfld1Div1 == 0.

(5) `uint8_t cgc_pll4_config_t::pfld1Div2`

Disabled when pfld1Div2 == 0.

(6) `uint8_t cgc_pll4_config_t::pfld2Div1`

Disabled when pfld2Div1 == 0.

(7) `uint8_t cgc_pll4_config_t::pfld2Div2`

Disabled when pfld2Div2 == 0.

(8) `uint8_t cgc_pll4_config_t::pfld3Div1`

Disabled when pfld3Div1 == 0.

(9) `uint8_t cgc_pll4_config_t::pfld3Div2`

Disabled when pfld3Div2 == 0.

(10) `cgc_pll_src_t cgc_pll4_config_t::src`

(11) `cgc_pll4_mult_t cgc_pll4_config_t::mult`

(12) `uint32_t cgc_pll4_config_t::num`

(13) `uint32_t cgc_pll4_config_t::denom`

## 4.3 Macro Definition Documentation

### 4.3.1 #define FSL\_SDK\_DISABLE\_DRIVER\_CLOCK\_CONTROL 0

When set to 0, peripheral drivers will enable clock in initialize function and disable clock in de-initialize function. When set to 1, peripheral driver will not control the clock, application could control the clock out of the driver.

Note

All drivers share this feature switcher. If it is set to 1, application should handle clock enable and disable for all drivers.

### 4.3.2 #define FSL\_CLOCK\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 0))

**4.3.3 #define PCC\_PCS\_VAL( reg ) (((reg)&PCC\_CLKCFG\_PCS\_MASK) >> PCC\_CLKCFG\_PCS\_SHIFT)**

**4.3.4 #define GPIO\_CLOCKS**

**Value:**

```
{
 kCLOCK_RgpioA, kCLOCK_RgpioB, kCLOCK_RgpioC, kCLOCK_RgpioD, kCLOCK_RgpioE, kCLOCK_RgpioF \
}
```

**4.3.5 #define SAI\_CLOCKS**

**Value:**

```
{
 \
 kCLOCK_Sai0, kCLOCK_Sai1, kCLOCK_Sai2, kCLOCK_Sai3, kCLOCK_Sai4, kCLOCK_Sai5, kCLOCK_Sai6,
 kCLOCK_Sai7 \
}
```

**4.3.6 #define PCTL\_CLOCKS**

**Value:**

```
{
 kCLOCK_PctlA, kCLOCK_PctlB, kCLOCK_IpInvalid, kCLOCK_IpInvalid, kCLOCK_PctlE, kCLOCK_PctlF \
}
```

**4.3.7 #define LPI2C\_CLOCKS**

**Value:**

```
{
 \
 kCLOCK_Lpi2c0, kCLOCK_Lpi2c1, kCLOCK_Lpi2c2, kCLOCK_Lpi2c3, kCLOCK_Lpi2c4, kCLOCK_Lpi2c5,
 kCLOCK_Lpi2c6, \
 kCLOCK_Lpi2c7 \
}
```

#### 4.3.8 #define I3C\_CLOCKS

**Value:**

```
{
 kCLOCK_I3c0, kCLOCK_I3c1, kCLOCK_I3c2 \
}
```

#### 4.3.9 #define FLEXIO\_CLOCKS

**Value:**

```
{
 kCLOCK_Flexio0, kCLOCK_Flexio1 \
}
```

#### 4.3.10 #define FLEXCAN\_CLOCKS

**Value:**

```
{
 kCLOCK_Flexcan \
}
```

#### 4.3.11 #define PDM\_CLOCKS

**Value:**

```
{
 kCLOCK_Micfil \
}
```

#### 4.3.12 #define LCDIF\_CLOCKS

**Value:**

```
{
 kCLOCK_Dcnano \
}
```

#### 4.3.13 #define MIPI\_DSI\_HOST\_CLOCKS

**Value:**

```
{
 kCLOCK_Dsi \
}
```

#### 4.3.14 #define EDMA\_CLOCKS

**Value:**

```
{
 kCLOCK_Dma0, kCLOCK_Dma1, kCLOCK_Dma2 \
}
```

#### 4.3.15 #define EDMA\_CHAN\_CLOCKS

**Value:**

```
{
 kCLOCK_Dma0Ch0, kCLOCK_Dma1Ch0, kCLOCK_Dma2Ch0 \
}
```

#### 4.3.16 #define LPUART\_CLOCKS

**Value:**

```
{
 kCLOCK_Lpuart0, kCLOCK_Lpuart1, kCLOCK_Lpuart2, kCLOCK_Lpuart3, kCLOCK_Lpuart4, kCLOCK_Lpuart5, \
 kCLOCK_Lpuart6, kCLOCK_Lpuart7 \
}
```

#### 4.3.17 #define DAC\_CLOCKS

**Value:**

```
{
 kCLOCK_Dac0, kCLOCK_Dac1 \
}
```

### 4.3.18 #define LPTMR\_CLOCKS

**Value:**

```
{
 KCLOCK_Lptmr0, KCLOCK_Lptmr1 \
}
```

### 4.3.19 #define LPADC\_CLOCKS

**Value:**

```
{
 KCLOCK_Adco, KCLOCK_Adcl \
}
```

### 4.3.20 #define LPSPI\_CLOCKS

**Value:**

```
{
 KCLOCK_Lpspi0, KCLOCK_Lpspi1, KCLOCK_Lpspi2, KCLOCK_Lpspi3, KCLOCK_Lpspi4, KCLOCK_Lpspi5 \
}
```

### 4.3.21 #define TPM\_CLOCKS

**Value:**

```
{
 \
 KCLOCK_Tpm0, KCLOCK_Tpm1, KCLOCK_Tpm2, KCLOCK_Tpm3, KCLOCK_Tpm4, KCLOCK_Tpm5, KCLOCK_Tpm6,
 KCLOCK_Tpm7, \
 KCLOCK_Tpm8
}
```

### 4.3.22 #define LPIT\_CLOCKS

**Value:**

```
{
 KCLOCK_Lpit0, KCLOCK_Lpit1 \
}
```

#### 4.3.23 #define CMP\_CLOCKS

**Value:**

```
{
 kCLOCK_Cmp0, kCLOCK_Cmp1 \
}
```

#### 4.3.24 #define WDOG\_CLOCKS

**Value:**

```
{
 kCLOCK_Wdog0, kCLOCK_Wdog1, kCLOCK_Wdog2, kCLOCK_Wdog3, kCLOCK_Wdog4, kCLOCK_Wdog5 \
}
```

Clock ip name array for WDOG.

#### 4.3.25 #define SEMA42\_CLOCKS

**Value:**

```
{
 kCLOCK_Sema420, kCLOCK_Sema421, kCLOCK_Sema422 \
}
```

#### 4.3.26 #define TPIU\_CLOCKS

**Value:**

```
{
 kCLOCK_Tpiu \
}
```

#### 4.3.27 #define FLEXSPI\_CLOCKS

**Value:**

```
{
 kCLOCK_Flexspi0, kCLOCK_Flexspi1, kCLOCK_Flexspi2 \
}
```

#### 4.3.28 #define MRT\_CLOCKS

**Value:**

```
{
 kCLOCK_Mrt \
}
```

#### 4.3.29 #define BBNSM\_CLOCKS

**Value:**

```
{
 kCLOCK_Bbnsm \
}
```

#### 4.3.30 #define PXP\_CLOCKS

**Value:**

```
{
 kCLOCK_Pxp \
}
```

#### 4.3.31 #define EPDC\_CLOCKS

**Value:**

```
{
 kCLOCK_Epdc \
}
```

### 4.4 Enumeration Type Documentation

#### 4.4.1 enum clock\_name\_t

Enumerator

*kCLOCK\_Cm33CorePlatClk* RTD : CM33 Core/Platform clock.  
*kCLOCK\_Cm33BusClk* RTD : CM33 Bus clock.  
*kCLOCK\_Cm33SlowClk* RTD : CM33 Slow clock.  
*kCLOCK\_FusionDspCorePlatClk* RTD : FusionF1 DSP Core/Platform clock.  
*kCLOCK\_FusionDspBusClk* RTD : FusionF1 DSP Bus clock.

***kCLOCK\_FusionDspSlowClk*** RTD : FusionF1 DSP Slow clock.

***kCLOCK\_XbarBusClk*** AD : XBAR Bus clock.

***kCLOCK\_HifiDspClk*** LPAV: HIFI4 clock.

***kCLOCK\_HifiNicPlatClk*** LPAV: NIC HIFI clock.

***kCLOCK\_NicLpavAxiClk*** LPAV: NIC LPAV AXI clock.

***kCLOCK\_NicLpavAhbClk*** LPAV: NIC LPAV AHB clock.

***kCLOCK\_NicLpavBusClk*** LPAV: LPAV Bus clock.

***kCLOCK\_DdrClk*** LPAV: DDR clock.

***kCLOCK\_SysOscClk*** CGC system OSC clock. (SYSOSC)

***kCLOCK\_FroClk*** CGC FRO 192MHz clock.

***kCLOCK\_LpOscClk*** CGC LPOSC clock. (LPOSC)

***kCLOCK\_RtcOscClk*** CGC RTC OSC clock. (RTCOSC)

***kCLOCK\_LvdsClk*** LVDS pad input clock frequency.

***kCLOCK\_RtdFroDiv1Clk*** FRODIV1\_CLK in RTD.

***kCLOCK\_RtdFroDiv2Clk*** FRODIV2\_CLK in RTD.

***kCLOCK\_RtdFroDiv3Clk*** FRODIV3\_CLK in RTD.

***kCLOCK\_RtdSysOscDiv1Clk*** SOSCDIV1\_CLK in RTD.

***kCLOCK\_RtdSysOscDiv2Clk*** SOSCDIV2\_CLK in RTD.

***kCLOCK\_RtdSysOscDiv3Clk*** SOSCDIV3\_CLK in RTD.

***kCLOCK\_AdFroDiv1Clk*** FRODIV1\_CLK in AD.

***kCLOCK\_AdFroDiv2Clk*** FRODIV2\_CLK in AD.

***kCLOCK\_AdFroDiv3Clk*** FRODIV3\_CLK in AD.

***kCLOCK\_AdSysOscDiv1Clk*** SOSCDIV1\_CLK in AD.

***kCLOCK\_AdSysOscDiv2Clk*** SOSCDIV2\_CLK in AD.

***kCLOCK\_AdSysOscDiv3Clk*** SOSCDIV3\_CLK in AD.

***kCLOCK\_LpavFroDiv1Clk*** FRODIV1\_CLK in LPAV.

***kCLOCK\_LpavFroDiv2Clk*** FRODIV2\_CLK in LPAV.

***kCLOCK\_LpavFroDiv3Clk*** FRODIV3\_CLK in LPAV.

***kCLOCK\_LpavSysOscDiv1Clk*** SOSCDIV1\_CLK in LPAV.

***kCLOCK\_LpavSysOscDiv2Clk*** SOSCDIV2\_CLK in LPAV.

***kCLOCK\_LpavSysOscDiv3Clk*** SOSCDIV3\_CLK in LPAV.

***kCLOCK\_Pll0Clk*** CGC PLL0 clock. (PLL0CLK)

***kCLOCK\_Pll1Clk*** CGC PLL1 clock. (PLL1CLK)

***kCLOCK\_Pll3Clk*** CGC PLL3 clock. (PLL3CLK)

***kCLOCK\_Pll4Clk*** CGC PLL4 clock. (PLL4CLK)

***kCLOCK\_Pll0Pfd0Clk*** pll0 pfd0.

***kCLOCK\_Pll0Pfd1Clk*** pll0 pfd1.

***kCLOCK\_Pll0Pfd2Clk*** pll0 pfd2.

***kCLOCK\_Pll0Pfd3Clk*** pll0 pfd3.

***kCLOCK\_Pll1Pfd0Clk*** pll1 pfd0.

***kCLOCK\_Pll1Pfd1Clk*** pll1 pfd1.

***kCLOCK\_Pll1Pfd2Clk*** pll1 pfd2.

***kCLOCK\_Pll1Pfd3Clk*** pll1 pfd3.

***kCLOCK\_Pll3Pfd0Clk*** pll3 pfd0.

***kCLOCK\_Pll3Pfd1Clk*** pll3 pfd1.

*kCLOCK\_Pll3Pfd2Clk* pll3 pfd2.  
*kCLOCK\_Pll3Pfd3Clk* pll3 pfd3.  
*kCLOCK\_Pll4Pfd0Clk* pll4 pfd0.  
*kCLOCK\_Pll4Pfd1Clk* pll4 pfd1.  
*kCLOCK\_Pll4Pfd2Clk* pll4 pfd2.  
*kCLOCK\_Pll4Pfd3Clk* pll4 pfd3.  
*kCLOCK\_Pll0VcoDivClk* PLL0VCODIV.  
*kCLOCK\_Pll0Pfd1DivClk* PLL0PFD1DIV.  
*kCLOCK\_Pll0Pfd2DivClk* PLL0PFD2DIV.  
*kCLOCK\_Pll1VcoDivClk* PLL1VCODIV.  
*kCLOCK\_Pll1Pfd1DivClk* PLL1PFD1DIV.  
*kCLOCK\_Pll1Pfd2DivClk* PLL1PFD2DIV.  
*kCLOCK\_Pll3VcoDivClk* PLL3VCODIV.  
*kCLOCK\_Pll3Pfd0Div1Clk* PLL3PFD0DIV1.  
*kCLOCK\_Pll3Pfd0Div2Clk* PLL3PFD0DIV2.  
*kCLOCK\_Pll3Pfd1Div1Clk* PLL3PFD1DIV1.  
*kCLOCK\_Pll3Pfd1Div2Clk* PLL3PFD1DIV2.  
*kCLOCK\_Pll3Pfd2Div1Clk* PLL3PFD2DIV1.  
*kCLOCK\_Pll3Pfd2Div2Clk* PLL3PFD2DIV2.  
*kCLOCK\_Pll3Pfd3Div1Clk* PLL3PFD3DIV1.  
*kCLOCK\_Pll3Pfd3Div2Clk* PLL3PFD3DIV2.  
*kCLOCK\_Pll4VcoDivClk* PLL4VCODIV.  
*kCLOCK\_Pll4Pfd0Div1Clk* PLL4PFD0DIV1.  
*kCLOCK\_Pll4Pfd0Div2Clk* PLL4PFD0DIV2.  
*kCLOCK\_Pll4Pfd1Div1Clk* PLL4PFD1DIV1.  
*kCLOCK\_Pll4Pfd1Div2Clk* PLL4PFD1DIV2.  
*kCLOCK\_Pll4Pfd2Div1Clk* PLL4PFD2DIV1.  
*kCLOCK\_Pll4Pfd2Div2Clk* PLL4PFD2DIV2.  
*kCLOCK\_Pll4Pfd3Div1Clk* PLL4PFD3DIV1.  
*kCLOCK\_Pll4Pfd3Div2Clk* PLL4PFD3DIV2.

#### 4.4.2 enum clock\_ip\_src\_t

Enumerator

*kCLOCK\_IpSrcNone* Clock is off.  
*kCLOCK\_Pcc0PlatIpSrcSysOscDiv1* PCC0, PCC1 Platform clock selection: kCLOCK\_RtdSys-OscDiv1Clk.  
*kCLOCK\_Pcc0PlatIpSrcFroDiv1* PCC0, PCC1 Platform clock selection: kCLOCK\_RtdFroDiv1-Clk.  
*kCLOCK\_Pcc0PlatIpSrcCm33Plat* PCC0, PCC1 Platform clock selection: kCLOCK\_Cm33Core-PlatClk.  
*kCLOCK\_Pcc0PlatIpSrcFro* PCC0, PCC1 Platform clock selection: kCLOCK\_FroClk.  
*kCLOCK\_Pcc0PlatIpSrcPll0Pfd3* PCC0, PCC1 Platform clock selection: kCLOCK\_Pll0Pfd3Clk.

***kCLOCK\_Pcc0BusIpSrcLpo*** PCC0, PCC1 Bus clock selection: kCLOCK\_LpOscClk.

***kCLOCK\_Pcc0BusIpSrcSysOscDiv2*** PCC0, PCC1 Bus clock selection: kCLOCK\_RtdSysOscDiv2Clk.

***kCLOCK\_Pcc0BusIpSrcFroDiv2*** PCC0, PCC1 Bus clock selection: kCLOCK\_RtdFroDiv2Clk.

***kCLOCK\_Pcc0BusIpSrcCm33Bus*** PCC0, PCC1 Bus clock selection: kCLOCK\_Cm33BusClk.

***kCLOCK\_Pcc0BusIpSrcPll1Pfd1Div*** PCC0 Bus clock selection: kCLOCK\_Pll1Pfd1DivClk.

***kCLOCK\_Pcc0BusIpSrcPll0Pfd2Div*** PCC0, PCC1 Bus clock selection: kCLOCK\_Pll0Pfd2DivClk.

***kCLOCK\_Pcc0BusIpSrcPll0Pfd1Div*** PCC0, PCC1 Bus clock selection: kCLOCK\_Pll0Pfd1DivClk.

***kCLOCK\_Pcc1PlatIpSrcSysOscDiv1*** PCC0, PCC1 Platform clock selection: kCLOCK\_RtdSysOscDiv1Clk.

***kCLOCK\_Pcc1PlatIpSrcFroDiv1*** PCC0, PCC1 Platform clock selection: kCLOCK\_RtdFroDiv1Clk.

***kCLOCK\_Pcc1PlatIpSrcCm33Plat*** PCC0, PCC1 Platform clock selection: kCLOCK\_Cm33CorePlatClk.

***kCLOCK\_Pcc1PlatIpSrcFro*** PCC0, PCC1 Platform clock selection: kCLOCK\_FroClk.

***kCLOCK\_Pcc1PlatIpSrcPll0Pfd3*** PCC0, PCC1 Platform clock selection: kCLOCK\_Pll0Pfd3Clk.

***kCLOCK\_Pcc1BusIpSrcLpo*** PCC0, PCC1 Bus clock selection: kCLOCK\_LpOscClk.

***kCLOCK\_Pcc1BusIpSrcSysOscDiv2*** PCC0, PCC1 Bus clock selection: kCLOCK\_RtdSysOscDiv2Clk.

***kCLOCK\_Pcc1BusIpSrcFroDiv2*** PCC0, PCC1 Bus clock selection: kCLOCK\_RtdFroDiv2Clk.

***kCLOCK\_Pcc1BusIpSrcCm33Bus*** PCC0, PCC1 Bus clock selection: kCLOCK\_Cm33BusClk.

***kCLOCK\_Pcc1BusIpSrcPll1VcoDiv*** PCC1 Bus clock selection: kCLOCK\_Pll1VcoDivClk.

***kCLOCK\_Pcc1BusIpSrcPll0Pfd2Div*** PCC0, PCC1 Bus clock selection: kCLOCK\_Pll0Pfd2DivClk.

***kCLOCK\_Pcc1BusIpSrcPll0Pfd1Div*** PCC0, PCC1 Bus clock selection: kCLOCK\_Pll0Pfd1DivClk.

***kCLOCK\_Pcc2BusIpSrcLpo*** PCC2 Bus clock selection: kCLOCK\_LpOscClk.

***kCLOCK\_Pcc2BusIpSrcSysOscDiv3*** PCC2 Bus clock selection: kCLOCK\_RtdSysOscDiv3Clk.

***kCLOCK\_Pcc2BusIpSrcFroDiv3*** PCC2 Bus clock selection: kCLOCK\_RtdFroDiv3Clk.

***kCLOCK\_Pcc2BusIpSrcFusionDspBus*** PCC2 Bus clock selection: kCLOCK\_FusionDspBusClk.

***kCLOCK\_Pcc2BusIpSrcPll1VcoDiv*** PCC2 Bus clock selection: kCLOCK\_Pll1VcoDivClk.

***kCLOCK\_Pcc2BusIpSrcPll0Pfd2Div*** PCC2 Bus clock selection: kCLOCK\_Pll0Pfd2DivClk.

***kCLOCK\_Pcc2BusIpSrcPll0Pfd1Div*** PCC2 Bus clock selection: kCLOCK\_Pll0Pfd1DivClk.

***kCLOCK\_Pcc3BusIpSrcLpo*** PCC3 Bus clock selection: kCLOCK\_LpOscClk.

***kCLOCK\_Pcc3BusIpSrcSysOscDiv2*** PCC3 Bus clock selection: kCLOCK\_AdSysOscDiv2Clk.

***kCLOCK\_Pcc3BusIpSrcFroDiv2*** PCC3 Bus clock selection: kCLOCK\_AdFroDiv2Clk.

***kCLOCK\_Pcc3BusIpSrcXbarBus*** PCC3 Bus clock selection: kCLOCK\_XbarBusClk.

***kCLOCK\_Pcc3BusIpSrcPll3Pfd1Div1*** PCC3 Bus clock selection: kCLOCK\_Pll3Pfd1Div1Clk.

***kCLOCK\_Pcc3BusIpSrcPll3Pfd0Div2*** PCC3 Bus clock selection: kCLOCK\_Pll3Pfd0Div2Clk.

***kCLOCK\_Pcc3BusIpSrcPll3Pfd0Div1*** PCC3 Bus clock selection: kCLOCK\_Pll3Pfd0Div1Clk.

***kCLOCK\_Pcc4PlatIpSrcSysOscDiv1*** PCC4 Platform clock selection: kCLOCK\_AdSysOscDiv1Clk.

***kCLOCK\_Pcc4PlatIpSrcFroDiv1*** PCC4 Platform clock selection: kCLOCK\_AdFroDiv1Clk.

***kCLOCK\_Pcc4PlatIpSrcPll3Pfd3Div2*** PCC4 Platform clock selection: kCLOCK\_Pl3Pfd3Div2-Clk.

***kCLOCK\_Pcc4PlatIpSrcPll3Pfd3Div1*** PCC4 Platform clock selection: kCLOCK\_Pl3Pfd3Div1-Clk.

***kCLOCK\_Pcc4PlatIpSrcPll3Pfd2Div2*** PCC4 Platform clock selection: kCLOCK\_Pl3Pfd2Div2-Clk.

***kCLOCK\_Pcc4PlatIpSrcPll3Pfd2Div1*** PCC4 Platform clock selection: kCLOCK\_Pl3Pfd2Div1-Clk.

***kCLOCK\_Pcc4PlatIpSrcPll3Pfd1Div2*** PCC4 Platform clock selection: kCLOCK\_Pl3Pfd1Div2-Clk.

***kCLOCK\_Pcc4BusIpSrcLpo*** PCC4 Bus clock selection: kCLOCK\_LpOscClk.

***kCLOCK\_Pcc4BusIpSrcSysOscDiv2*** PCC4 Bus clock selection: kCLOCK\_AdSysOscDiv2Clk.

***kCLOCK\_Pcc4BusIpSrcFroDiv2*** PCC4 Bus clock selection: kCLOCK\_AdFroDiv2Clk.

***kCLOCK\_Pcc4BusIpSrcXbarBus*** PCC4 Bus clock selection: kCLOCK\_XbarBusClk.

***kCLOCK\_Pcc4BusIpSrcPll3VcoDiv*** PCC4 Bus clock selection: kCLOCK\_Pl3VcoDivClk.

***kCLOCK\_Pcc4BusIpSrcPll3Pfd0Div1*** PCC4 Bus clock selection: kCLOCK\_Pl3Pfd0Div1Clk.

***kCLOCK\_Pcc5PlatIpSrcPll4Pfd3Div2*** PCC5 Platform clock selection: kCLOCK\_Pl4Pfd3Div2-Clk.

***kCLOCK\_Pcc5PlatIpSrcPll4Pfd2Div2*** PCC5 Platform clock selection: kCLOCK\_Pl4Pfd2Div2-Clk.

***kCLOCK\_Pcc5PlatIpSrcPll4Pfd2Div1*** PCC5 Platform clock selection: kCLOCK\_Pl4Pfd2Div1-Clk.

***kCLOCK\_Pcc5PlatIpSrcPll4Pfd1Div2*** PCC5 Platform clock selection: kCLOCK\_Pl4Pfd1Div2-Clk.

***kCLOCK\_Pcc5PlatIpSrcPll4Pfd1Div1*** PCC5 Platform clock selection: kCLOCK\_Pl4Pfd1Div1-Clk.

***kCLOCK\_Pcc5PlatIpSrcPll4Pfd0Div2*** PCC5 Platform clock selection: kCLOCK\_Pl4Pfd0Div2-Clk.

***kCLOCK\_Pcc5PlatIpSrcPll4Pfd0Div1*** PCC5 Platform clock selection: kCLOCK\_Pl4Pfd0Div1-Clk.

***kCLOCK\_Pcc5BusIpSrcLpo*** PCC5 Bus clock selection: kCLOCK\_LpOscClk.

***kCLOCK\_Pcc5BusIpSrcSysOscDiv2*** PCC5 Bus clock selection: kCLOCK\_LpavSysOscDiv2Clk.

***kCLOCK\_Pcc5BusIpSrcFroDiv2*** PCC5 Bus clock selection: kCLOCK\_LpavFroDiv2Clk.

***kCLOCK\_Pcc5BusIpSrcLpavBus*** PCC5 Bus clock selection: kCLOCK\_NicLpavBusClk.

***kCLOCK\_Pcc5BusIpSrcPll4VcoDiv*** PCC5 Bus clock selection: kCLOCK\_Pl4VcoDivClk.

***kCLOCK\_Pcc5BusIpSrcPll4Pfd3Div1*** PCC5 Bus clock selection: kCLOCK\_Pl4Pfd3Div1Clk.

***kCLOCK\_Cm33SaiClkSrcPll1Pfd2Div*** PLL1 PFD2 DIV in RTD: kCLOCK\_Pl1Pfd2DivClk.

***kCLOCK\_Cm33SaiClkSrcRtdAudClk*** Common audio clock in RTD, see cgc\_rtd\_audclk\_src\_t.

***kCLOCK\_Cm33SaiClkSrcLpavAudClk*** Common audio clock in LPAV, see cgc\_lpav\_audclk\_src\_t.

***kCLOCK\_Cm33SaiClkSrcSysOsc*** SYSOSC main reference clock to the chip: kCLOCK\_SysOsc-Clk.

***kCLOCK\_FusionSaiClkSrcPll1Pfd2Div*** PLL1 PFD2 DIV in RTD: kCLOCK\_Pl1Pfd2DivClk.

***kCLOCK\_FusionSaiClkSrcExtMclk1*** External audio master clock input 1.

***kCLOCK\_FusionSaiClkSrcSai3Rx*** SAI3 receiver serial bit clock. Only for SAI2.

***kCLOCK\_FusionSaiClkSrcSai2Tx*** SAI2 transmitter serial bit clock. Only for SAI3.

***kCLOCK\_FusionSaiClkSrcSysOsc*** SYSOSC main reference clock to the chip: kCLOCK\_SysOscClk.

***kCLOCK\_FusionMicfilClkSrcPll1Pfd2Div*** PLL1 PFD2 DIV in RTD: kCLOCK\_Pll1Pfd2DivClk.

***kCLOCK\_FusionMicfilClkSrcFro24*** FRO24: kCLOCK\_FroClk/8.

***kCLOCK\_FusionMicfilClkSrcSysOsc*** SYSOSC main reference clock to the chip: kCLOCK\_SysOscClk.

***kCLOCK\_FusionMicfilClkSrcExtMclk1*** External audio master clock input 1.

***kCLOCK\_FusionMicfilClkSrcRtcOsc*** kCLOCK\_RtcOscClk.

***kCLOCK\_FusionMicfilClkSrcLpo*** kCLOCK\_LpOscClk.

***kCLOCK\_FusionTpm2ClkSrcPll1Pfd2Div*** PLL1 PFD2 DIV in RTD: kCLOCK\_Pll1Pfd2DivClk.

***kCLOCK\_FusionTpm2ClkSrcExtMclk1*** External audio master clock input 1.

***kCLOCK\_FusionTpm2ClkSrcLpo*** PCC2 Bus clock selection: kCLOCK\_LpOscClk.

***kCLOCK\_FusionTpm2ClkSrcSysOscDiv3*** PCC2 Bus clock selection: kCLOCK\_RtdSysOscDiv3Clk.

***kCLOCK\_FusionTpm2ClkSrcFroDiv3*** PCC2 Bus clock selection: kCLOCK\_RtdFroDiv3Clk.

***kCLOCK\_FusionTpm2ClkSrcFusionDspBus*** PCC2 Bus clock selection: kCLOCK\_FusionDspBusClk.

***kCLOCK\_FusionTpm2ClkSrcPll1VcoDiv*** PCC2 Bus clock selection: kCLOCK\_Pll1VcoDivClk.

***kCLOCK\_FusionTpm2ClkSrcPll0Pfd2Div*** PCC2 Bus clock selection: kCLOCK\_Pll0Pfd2DivClk.

***kCLOCK\_FusionTpm2ClkSrcPll0Pfd1Div*** PCC2 Bus clock selection: kCLOCK\_Pll0Pfd1DivClk.

***kCLOCK\_FusionTpm3ClkSrcPll1Pfd2Div*** PLL1 PFD2 DIV in RTD: kCLOCK\_Pll1Pfd2DivClk.

***kCLOCK\_FusionTpm3ClkSrcRtdAudClk*** Common audio clock in RTD, see cgc\_rtd\_audclk\_src\_t.

***kCLOCK\_FusionTpm3ClkSrcLpavAudClk*** Common audio clock in LPAV, see cgc\_lpav\_audclk\_src\_t.

***kCLOCK\_FusionTpm3ClkSrcLpo*** PCC2 Bus clock selection: kCLOCK\_LpOscClk.

***kCLOCK\_FusionTpm3ClkSrcSysOscDiv3*** PCC2 Bus clock selection: kCLOCK\_RtdSysOscDiv3Clk.

***kCLOCK\_FusionTpm3ClkSrcFroDiv3*** PCC2 Bus clock selection: kCLOCK\_RtdFroDiv3Clk.

***kCLOCK\_FusionTpm3ClkSrcFusionDspBus*** PCC2 Bus clock selection: kCLOCK\_FusionDspBusClk.

***kCLOCK\_FusionTpm3ClkSrcPll1VcoDiv*** PCC2 Bus clock selection: kCLOCK\_Pll1VcoDivClk.

***kCLOCK\_FusionTpm3ClkSrcPll0Pfd2Div*** PCC2 Bus clock selection: kCLOCK\_Pll0Pfd2DivClk.

***kCLOCK\_FusionTpm3ClkSrcPll0Pfd1Div*** PCC2 Bus clock selection: kCLOCK\_Pll0Pfd1DivClk.

***kCLOCK\_AdSaiClkSrcPll3Pfd1Div1*** PLL3 PFD1 DIV1 in AD: kCLOCK\_Pll3Pfd1Div2Clk.

***kCLOCK\_AdSaiClkSrcAdAudClk*** Common audio clock in AD, see cgc\_ad\_audclk\_src\_t.

***kCLOCK\_AdSaiClkSrcLpavAudClk*** Common audio clock in LPAV, see cgc\_lpav\_audclk\_src\_t.

***kCLOCK\_AdSaiClkSrcSysOsc*** SYSOSC main reference clock to the chip: kCLOCK\_SysOscClk.

***kCLOCK\_AdTpm67ClkSrcPll3Pfd1Div1*** PLL3 PFD1 DIV1 in AD: kCLOCK\_Pll3Pfd1Div2Clk.

***kCLOCK\_AdTpm67ClkSrcAdAudClk*** Common audio clock in AD, see cgc\_ad\_audclk\_src\_t.

***kCLOCK\_AdTpm67ClkSrcLpavAudClk*** Common audio clock in LPAV, see `cgc_lpav_audclk_src_t`.

***kCLOCK\_AdTpm67ClkSrcLpo*** PCC4 Bus clock selection: `kCLOCK_LpOscClk`.

***kCLOCK\_AdTpm67ClkSrcSysOscDiv2*** PCC4 Bus clock selection: `kCLOCK_AdSysOscDiv2Clk`.

***kCLOCK\_AdTpm67ClkSrcFroDiv2*** PCC4 Bus clock selection: `kCLOCK_AdFroDiv2Clk`.

***kCLOCK\_AdTpm67ClkSrcXbarBus*** PCC4 Bus clock selection: `kCLOCK_XbarBusClk`.

***kCLOCK\_AdTpm67ClkSrcPll3VcoDiv*** PCC4 Bus clock selection: `kCLOCK_Pll3VcoDivClk`.

***kCLOCK\_AdTpm67ClkSrcPll3Pfd0Div1*** PCC4 Bus clock selection: `kCLOCK_Pll3Pfd0Div1Clk`.

***kCLOCK\_LpavSaiClkSrcPll1Pfd2Div*** PLL1 PFD2 DIV in RTD: `kCLOCK_Pll1Pfd2DivClk`.

***kCLOCK\_LpavSaiClkSrcPll3Pfd1Div1*** PLL3 PFD1 DIV1 in AD: `kCLOCK_Pll3Pfd1Div1Clk`.

***kCLOCK\_LpavSaiClkSrcRtdAudClk*** Common audio clock in RTD, see `cgc_rtd_audclk_src_t`.

***kCLOCK\_LpavSaiClkSrcAdAudClk*** Common audio clock in AD, see `cgc_ad_audclk_src_t`.

***kCLOCK\_LpavSaiClkSrcLpavAudClk*** Common audio clock in LPAV, see `cgc_lpav_audclk_src_t`.

***kCLOCK\_LpavSaiClkSrcSysOsc*** SYSOSC main reference clock to the chip.

***kCLOCK\_LpavTpm8ClkSrcPll1Pfd2Div*** PLL1 PFD2 DIV in RTD: `kCLOCK_Pll1Pfd2DivClk`.

***kCLOCK\_LpavTpm8ClkSrcPll3Pfd1Div1*** PLL3 PFD1 DIV1 in AD: `kCLOCK_Pll3Pfd1Div1Clk`.

***kCLOCK\_LpavTpm8ClkSrcRtdAudClk*** Common audio clock in RTD, see `cgc_rtd_audclk_src_t`.

***kCLOCK\_LpavTpm8ClkSrcAdAudClk*** Common audio clock in AD, see `cgc_ad_audclk_src_t`.

***kCLOCK\_LpavTpm8ClkSrcLpavAudClk*** Common audio clock in LPAV, see `cgc_lpav_audclk_src_t`.

***kCLOCK\_LpavTpm8ClkSrcLpo*** PCC5 Bus clock selection: `kCLOCK_LpOscClk`.

***kCLOCK\_LpavTpm8ClkSrcSysOscDiv2*** PCC5 Bus clock selection: `kCLOCK_LpavSysOscDiv2Clk`.

***kCLOCK\_LpavTpm8ClkSrcFroDiv2*** PCC5 Bus clock selection: `kCLOCK_LpavFroDiv2Clk`.

***kCLOCK\_LpavTpm8ClkSrcLpavBus*** PCC5 Bus clock selection: `kCLOCK_NicLpavBusClk`.

***kCLOCK\_LpavTpm8ClkSrcPll4VcoDiv*** PCC5 Bus clock selection: `kCLOCK_Pll4VcoDivClk`.

***kCLOCK\_LpavTpm8ClkSrcPll4Pfd3Div1*** PCC5 Bus clock selection: `kCLOCK_Pll4Pfd3Div1Clk`.

#### 4.4.3 enum `clock_lptmr_src_t`

Enumerator

***kCLOCK\_LptmrSrcLPO1M*** LPO 1MHz clock.

***kCLOCK\_LptmrSrcRtc1K*** RTC 1KHz clock.

***kCLOCK\_LptmrSrcRtc32K*** RTC 32KHz clock.

***kCLOCK\_LptmrSrcSysOsc*** system OSC clock.

#### 4.4.4 enum `clock_ip_name_t`

[31:2] is defined as the corresponding register address. [ 1:1] is used as indicator of existing of PCS. [ 0:0] is used as indicator of existing of PCD/FRAC.

#### 4.4.5 anonymous enum

Enumerator

*kStatus\_CGC\_Busy* Clock is busy.  
*kStatus\_CGC\_InvalidSrc* Invalid source.

#### 4.4.6 enum cgc\_sys\_clk\_t

Enumerator

*kCGC\_SysClkSlow* System slow clock.  
*kCGC\_SysClkBus* Bus clock.  
*kCGC\_SysClkCorePlat* Core/Platform clock.  
*kCGC\_SysClkHifi4* Hifi4 core clock.  
*kCGC\_SysClkNicHifi* Hifi4 platform clock.  
*kCGC\_SysClkLpavAxi* LPAV AXI clock.  
*kCGC\_SysClkLpavAhb* LPAV AHB clock.  
*kCGC\_SysClkLpavBus* LPAV Bus clock.

#### 4.4.7 enum cgc\_rtd\_sys\_clk\_src\_t

Enumerator

*kCGC\_RtdSysClkSrcFro* FRO192.  
*kCGC\_RtdSysClkSrcPll0Pfd0* PLL0 PFD0.  
*kCGC\_RtdSysClkSrcPll1Pfd0* PLL1 PFD0.  
*kCGC\_RtdSysClkSrcSysOsc* System OSC.  
*kCGC\_RtdSysClkSrcRtcOsc* RTC OSC.  
*kCGC\_RtdSysClkSrcLvds* LVDS XCVR.  
*kCGC\_RtdSysClkSrcPll0* PLL0.

#### 4.4.8 enum cgc\_nic\_sys\_clk\_src\_t

Enumerator

*kCGC\_NicSysClkSrcFro* FRO192.  
*kCGC\_NicSysClkSrcPll3Pfd0* PLL0 PFD0.  
*kCGC\_NicSysClkSrcSysOsc* System OSC.  
*kCGC\_NicSysClkSrcLvds* LVDS XCVR.

**4.4.9 enum cgc\_hifi\_sys\_clk\_src\_t**

Enumerator

*kCGC\_HifiSysClkSrcFro* FRO192.  
*kCGC\_HifiSysClkSrcPll4* PLL4.  
*kCGC\_HifiSysClkSrcPll4Pfd0* PLL4 PFD0.  
*kCGC\_HifiSysClkSrcSysOsc* System OSC.  
*kCGC\_HifiSysClkSrcLvds* LVDS XCVR.

**4.4.10 enum cgc\_lpav\_sys\_clk\_src\_t**

Enumerator

*kCGC\_LpavSysClkSrcFro* FRO192.  
*kCGC\_LpavSysClkSrcPll4Pfd1* PLL4 PFD1.  
*kCGC\_LpavSysClkSrcSysOsc* System OSC.  
*kCGC\_LpavSysClkSrcLvds* LVDS XCVR.

**4.4.11 enum cgc\_ddr\_sys\_clk\_src\_t**

Enumerator

*kCGC\_DdrSysClkSrcFro* FRO192.  
*kCGC\_DdrSysClkSrcPll4Pfd1* PLL4 PFD1.  
*kCGC\_DdrSysClkSrcSysOsc* System OSC.  
*kCGC\_DdrSysClkSrcLvds* LVDS XCVR.

**4.4.12 enum clock\_rtd\_clkout\_src\_t**

Enumerator

*kClockRtdClkoutSelCm33Core* CGC CM33 Core/Platform clock.  
*kClockRtdClkoutSelCm33Bus* CGC CM33 Bus clock.  
*kClockRtdClkoutSelCm33Slow* CGC CM33 Slow clock.  
*kClockRtdClkoutSelFusionDspCore* CGC Fusion DSP Core/Platform clock.  
*kClockRtdClkoutSelFusionDspBus* CGC Fusion DSP Bus clock.  
*kClockRtdClkoutSelFusionDspSlow* CGC Fusion DSP Slow clock.  
*kClockRtdClkoutSelFro48* FRO48: kCLOCK\_FroClk/4.  
*kClockRtdClkoutSelPll0VcoDiv* PLL0 VCO DIV: kCLOCK\_Pll0VcoDivClk.  
*kClockRtdClkoutSelPll1VcoDiv* PLL1 VCO DIV: kCLOCK\_Pll1VcoDivClk.  
*kClockRtdClkoutSelSysOsc* System OSC.  
*kClockRtdClkoutSelLpOsc* CGC LPOSOC clock.

#### 4.4.13 enum clock\_lpav\_clkout\_src\_t

Enumerator

- kClockLpavClkoutSelHifi4* CGC HIFI4 core clock.
- kClockLpavClkoutSelNicHifi* CGC HIFI4 platform clock.
- kClockLpavClkoutSelLpavAxi* CGC NIC LPAV AXI clock.
- kClockLpavClkoutSelLpavAhb* CGC NIC LPAV AHB clock.
- kClockLpavClkoutSelLpavBus* CGC LPAV Bus clock.
- kClockLpavClkoutSelDdr* CGC DDR clock.
- kClockLpavClkoutSelFro48* FRO48: kCLOCK\_FroClk/4.
- kClockLpavClkoutSelPll4VcoDiv* PLL4 VCO DIV: kCLOCK\_Pll4VcoDivClk.
- kClockLpavClkoutSelSysOsc* System OSC.
- kClockLpavClkoutSelLpOsc* CGC LPOSC clock.

#### 4.4.14 enum cgc\_async\_clk\_t

Enumerator

- kCGC\_AsyncDiv1Clk* The async clock by DIV1, e.g. SOSCDIV1\_CLK, FRODIV1\_CLK.
- kCGC\_AsyncDiv2Clk* The async clock by DIV2, e.g. SOSCDIV2\_CLK, FRODIV2\_CLK.
- kCGC\_AsyncDiv3Clk* The async clock by DIV3, e.g. SOSCDIV3\_CLK, FRODIV3\_CLK.
- kCGC\_AsyncVcoClk* The async clock by PLL VCO DIV.
- kCGC\_AsyncPfd0Div1Clk* The async clock by PLL PFD0 DIV1.
- kCGC\_AsyncPfd0Div2Clk* The async clock by PLL PFD0 DIV2.
- kCGC\_AsyncPfd1Div1Clk* The async clock by PLL PFD1 DIV or DIV1.
- kCGC\_AsyncPfd1Div2Clk* The async clock by PLL PFD1 DIV2.
- kCGC\_AsyncPfd2Div1Clk* The async clock by PLL PFD2 DIV or DIV1.
- kCGC\_AsyncPfd2Div2Clk* The async clock by PLL PFD2 DIV2.
- kCGC\_AsyncPfd3Div1Clk* The async clock by PLL PFD3 DIV1.
- kCGC\_AsyncPfd3Div2Clk* The async clock by PLL PFD3 DIV2.

#### 4.4.15 enum cgc\_sosc\_monitor\_mode\_t

Enumerator

- kCGC\_SysOscMonitorDisable* Monitor disabled.
- kCGC\_SysOscMonitorInt* Interrupt when the system OSC error is detected.
- kCGC\_SysOscMonitorReset* Reset when the system OSC error is detected.

**4.4.16 enum cgc\_sosc\_mode\_t**

Enumerator

- kCGC\_SysOscModeExt* Use external clock.
- kCGC\_SysOscModeOscLowPower* Oscillator low power.
- kCGC\_SysOscModeOscHighGain* Oscillator high gain.

**4.4.17 enum \_cgc\_sosc\_enable\_mode**

Enumerator

- kCGC\_SysOscEnableInDeepSleep* Enable OSC in deep sleep mode.
- kCGC\_SysOscEnableInPowerDown* Enable OSC in low power mode.

**4.4.18 enum \_cgc\_fro\_enable\_mode**

Enumerator

- kCGC\_FroEnableInDeepSleep* Enable FRO in deep sleep mode.

**4.4.19 enum \_cgc\_lposc\_enable\_mode**

Enumerator

- kCGC\_LposcEnableInDeepSleep* Enable OSC in deep sleep mode.
- kCGC\_LposcEnableInPowerDown* Enable OSC in low power mode.

**4.4.20 enum cgc\_pll\_src\_t**

Enumerator

- kCGC\_PlISrcSysOsc* PLL clock source is system OSC.
- kCGC\_PlISrcFro24M* PLL clock source is FRO 24M.

**4.4.21 enum \_cgc\_pll\_enable\_mode**

Enumerator

- kCGC\_PlLEnable* Enable PLL clock.
- kCGC\_PlLEnableInDeepSleep* Enable PLL in deep sleep mode.

**4.4.22 enum cgc\_pll\_pfd\_clkout\_t**

Enumerator

- kCGC\_PllPfd0Clk* PFD0 output clock selected.
- kCGC\_PllPfd1Clk* PFD1 output clock selected.
- kCGC\_PllPfd2Clk* PFD2 output clock selected.
- kCGC\_PllPfd3Clk* PFD3 output clock selected.

**4.4.23 enum cgc\_pll0\_mult\_t**

Enumerator

- kCGC\_PlloMult15* Divide by 15.
- kCGC\_PlloMult16* Divide by 16.
- kCGC\_PlloMult20* Divide by 20.
- kCGC\_PlloMult22* Divide by 22.
- kCGC\_PlloMult25* Divide by 25.
- kCGC\_PlloMult30* Divide by 30.

**4.4.24 enum cgc\_rosc\_monitor\_mode\_t**

Enumerator

- kCGC\_RtcOscMonitorDisable* Monitor disabled.
- kCGC\_RtcOscMonitorInt* Interrupt when the RTC OSC error is detected.
- kCGC\_RtcOscMonitorReset* Reset when the RTC OSC error is detected.

**4.4.25 enum cgc\_pll1\_mult\_t**

Enumerator

- kCGC\_PlloMult16* Divide by 16.
- kCGC\_PlloMult17* Divide by 17.
- kCGC\_PlloMult20* Divide by 20.
- kCGC\_PlloMult22* Divide by 22.
- kCGC\_PlloMult27* Divide by 27.
- kCGC\_PlloMult33* Divide by 33.

**4.4.26 enum cgc\_pll4\_mult\_t**

Enumerator

- kCGC\_Pl4Mult16* Divide by 16.
- kCGC\_Pl4Mult17* Divide by 17.
- kCGC\_Pl4Mult20* Divide by 20.
- kCGC\_Pl4Mult22* Divide by 22.
- kCGC\_Pl4Mult27* Divide by 27.
- kCGC\_Pl4Mult33* Divide by 33.

**4.4.27 enum cgc\_rtd\_audclk\_src\_t**

Enumerator

- kCGC\_RtdAudClkSrcExtMclk0* External audio master clock input 0 from pin.
- kCGC\_RtdAudClkSrcExtMclk1* External audio master clock input 1 from pin.
- kCGC\_RtdAudClkSrcSai0RxBclk* SAI0 receiver serial bit clock.
- kCGC\_RtdAudClkSrcSai0TxBclk* SAI0 transmitter serial bit clock.
- kCGC\_RtdAudClkSrcSai1RxBclk* SAI1 receiver serial bit clock.
- kCGC\_RtdAudClkSrcSai1TxBclk* SAI1 transmitter serial bit clock.
- kCGC\_RtdAudClkSrcSai2RxBclk* SAI2 receiver serial bit clock.
- kCGC\_RtdAudClkSrcSai2TxBclk* SAI2 transmitter serial bit clock.
- kCGC\_RtdAudClkSrcSai3RxBclk* SAI3 receiver serial bit clock.
- kCGC\_RtdAudClkSrcSai3TxBclk* SAI3 transmitter serial bit clock.

**4.4.28 enum cgc\_ad\_audclk\_src\_t**

Enumerator

- kCGC\_AdAudClkSrcExtMclk2* External audio master clock input 2 from pin.
- kCGC\_AdAudClkSrcSai4RxBclk* SAI4 receiver serial bit clock.
- kCGC\_AdAudClkSrcSai4TxBclk* SAI4 transmitter serial bit clock.
- kCGC\_AdAudClkSrcSai5RxBclk* SAI5 receiver serial bit clock.
- kCGC\_AdAudClkSrcSai5TxBclk* SAI5 transmitter serial bit clock.

**4.4.29 enum cgc\_lpav\_audclk\_src\_t**

Enumerator

- kCGC\_LpavAudClkSrcExtMclk3* External audio master clock input 3 from pin.
- kCGC\_LpavAudClkSrcSai6RxBclk* SAI6 receiver serial bit clock.

*kCGC\_LpavAudClkSrcSai6TxBclk* SAI6 transmitter serial bit clock.

*kCGC\_LpavAudClkSrcSai7RxBclk* SAI7 receiver serial bit clock.

*kCGC\_LpavAudClkSrcSai7TxBclk* SAI7 transmitter serial bit clock.

*kCGC\_LpavAudClkSrcSpdifRx* SPDIF receiver clock.

## 4.5 Function Documentation

### 4.5.1 static void CLOCK\_EnableClock ( *clock\_ip\_name\_t name* ) [inline], [static]

Parameters

|             |                                                              |
|-------------|--------------------------------------------------------------|
| <i>name</i> | Which clock to enable, see <a href="#">clock_ip_name_t</a> . |
|-------------|--------------------------------------------------------------|

### 4.5.2 static void CLOCK\_DisableClock ( *clock\_ip\_name\_t name* ) [inline], [static]

Parameters

|             |                                                               |
|-------------|---------------------------------------------------------------|
| <i>name</i> | Which clock to disable, see <a href="#">clock_ip_name_t</a> . |
|-------------|---------------------------------------------------------------|

### 4.5.3 static bool CLOCK\_IsEnabledByOtherCore ( *clock\_ip\_name\_t name* ) [inline], [static]

Parameters

|             |                                                                  |
|-------------|------------------------------------------------------------------|
| <i>name</i> | Which peripheral to check, see <a href="#">clock_ip_name_t</a> . |
|-------------|------------------------------------------------------------------|

Returns

True if clock is already enabled, otherwise false.

### 4.5.4 void CLOCK\_SetIpSrc ( *clock\_ip\_name\_t name*, *clock\_ip\_src\_t src* )

Set the clock source for specific IP, not all modules need to set the clock source, should only use this function for the modules need source setting.

Parameters

|             |                                                                  |
|-------------|------------------------------------------------------------------|
| <i>name</i> | Which peripheral to check, see <a href="#">clock_ip_name_t</a> . |
| <i>src</i>  | Clock source to set.                                             |

#### 4.5.5 void CLOCK\_SetIpSrcDiv ( [clock\\_ip\\_name\\_t name](#), [clock\\_ip\\_src\\_t src](#), [uint8\\_t divValue](#), [uint8\\_t fracValue](#) )

Set the clock source and divider for specific IP, not all modules need to set the clock source and divider, should only use this function for the modules need source and divider setting.

Divider output clock = Divider input clock x [(fracValue+1)/(divValue+1)].

Parameters

|                  |                                                                  |
|------------------|------------------------------------------------------------------|
| <i>name</i>      | Which peripheral to check, see <a href="#">clock_ip_name_t</a> . |
| <i>src</i>       | Clock source to set.                                             |
| <i>divValue</i>  | The divider value.                                               |
| <i>fracValue</i> | The fraction multiply value.                                     |

#### 4.5.6 static void CLOCK\_SetRtdAudClkSrc ( [cgc\\_rtd\\_audclk\\_src\\_t src](#) ) [[inline](#)], [[static](#)]

NOTE: The audio clock pin frequency is decided by SAI, but clock driver cannot depend on SAI driver to get its pin frequencies, user need to explicitly set the MCLK/BCLK frequencies if other modules use the AUD\_CLK0 source and need to get correct frequency.

Parameters

|            |                      |
|------------|----------------------|
| <i>src</i> | Clock source to set. |
|------------|----------------------|

#### 4.5.7 static void CLOCK\_SetAdAudClkSrc ( [cgc\\_ad\\_audclk\\_src\\_t src](#) ) [[inline](#)], [[static](#)]

NOTE: The audio clock pin frequency is decided by SAI, but clock driver cannot depend on SAI driver to get its pin frequencies, user need to explicitly set the MCLK/BCLK frequencies if other modules use the AUD\_CLK1 source and need to get correct frequency.

Parameters

|            |                      |
|------------|----------------------|
| <i>src</i> | Clock source to set. |
|------------|----------------------|

#### 4.5.8 static void CLOCK\_SetLpavAudClkSrc ( `cgc_lpav_audclk_src_t src` ) [inline], [static]

NOTE: The audio clock pin frequency is decided by SAI, but clock driver cannot depend on SAI driver to get its pin frequencies, user need to explicitly set the MCLK/BCLK frequencies if other modules use the AUD\_CLK2 source and need to get correct frequency.

Parameters

|            |                      |
|------------|----------------------|
| <i>src</i> | Clock source to set. |
|------------|----------------------|

#### 4.5.9 uint32\_t CLOCK\_GetFreq ( `clock_name_t clockName` )

This function checks the current clock configurations and then calculates the clock frequency for a specific clock name defined in `clock_name_t`.

Parameters

|                  |                                                  |
|------------------|--------------------------------------------------|
| <i>clockName</i> | Clock names defined in <code>clock_name_t</code> |
|------------------|--------------------------------------------------|

Returns

Clock frequency value in hertz

#### 4.5.10 uint32\_t CLOCK\_GetCm33CorePlatClkFreq ( `void` )

Returns

Clock frequency in Hz.

#### 4.5.11 uint32\_t CLOCK\_GetCm33BusClkFreq ( `void` )

Returns

Clock frequency in Hz.

**4.5.12 uint32\_t CLOCK\_GetCm33SlowClkFreq( void )**

Returns

Clock frequency in Hz.

**4.5.13 uint32\_t CLOCK\_GetFusionDspCorePlatClkFreq( void )**

Returns

Clock frequency in Hz.

**4.5.14 uint32\_t CLOCK\_GetFusionDspBusClkFreq( void )**

Returns

Clock frequency in Hz.

**4.5.15 uint32\_t CLOCK\_GetFusionDspSlowClkFreq( void )**

Returns

Clock frequency in Hz.

**4.5.16 uint32\_t CLOCK\_GetLvdsClkFreq( void )**

Returns

Clock frequency in Hz.

**4.5.17 uint32\_t CLOCK\_GetIpFreq( clock\_ip\_name\_t name )**

This function gets the IP module clock frequency. It is only used for the IP modules which could select clock source by [CLOCK\\_SetIpSrc\(\)](#).

Parameters

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <i>name</i> | Which peripheral to get, see <a href="#">clock_ip_name_t</a> . |
|-------------|----------------------------------------------------------------|

Returns

Clock frequency value in hertz

#### 4.5.18 **uint32\_t CLOCK\_GetCm33SysClkFreq ( cgc\_sys\_clk\_t *type* )**

This function gets the CGC CM33 system clock frequency. These clocks are used for core, platform, bus and slow clock domains.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>type</i> | Which type of clock to get. |
|-------------|-----------------------------|

Returns

Clock frequency.

#### 4.5.19 **static void CLOCK\_SetCm33SysClkConfig ( const cgc\_rtd\_sys\_clk\_config\_t \* *config* ) [inline], [static]**

This function sets the system clock configuration for CM33 domain.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>config</i> | Pointer to the configuration. |
|---------------|-------------------------------|

#### 4.5.20 **uint32\_t CLOCK\_GetFusionDspSysClkFreq ( cgc\_sys\_clk\_t *type* )**

This function gets the CGC Fusion DSP system clock frequency. These clocks are used for core, platform, bus and slow clock domains.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>type</i> | Which type of clock to get. |
|-------------|-----------------------------|

Returns

Clock frequency.

#### 4.5.21 static void CLOCK\_SetFusionSysClkConfig ( const cgc\_rtd\_sys\_clk\_config\_t \* *config* ) [inline], [static]

This function sets the system clock configuration for FusionF1 DSP domain.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>config</i> | Pointer to the configuration. |
|---------------|-------------------------------|

#### 4.5.22 static void CLOCK\_GetCm33SysClkConfig ( cgc\_rtd\_sys\_clk\_config\_t \* *config* ) [inline], [static]

This function gets the system configuration for CM33 domain.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>config</i> | Pointer to the configuration. |
|---------------|-------------------------------|

#### 4.5.23 static void CLOCK\_GetFusionDspSysClkConfig ( cgc\_rtd\_sys\_clk\_config\_t \* *config* ) [inline], [static]

This function gets the system configuration for FusionF1 DSP domain.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>config</i> | Pointer to the configuration. |
|---------------|-------------------------------|

#### 4.5.24 static void CLOCK\_SetRtdClkOutConfig ( clock\_rtd\_clkout\_src\_t *setting*, uint8\_t *div*, bool *enable* ) [inline], [static]

This function sets the clock out configuration.

Parameters

|                |                                       |
|----------------|---------------------------------------|
| <i>setting</i> | The selection to set.                 |
| <i>div</i>     | The divider to set ( <i>div</i> > 0). |
| <i>enable</i>  | Enable clock out.                     |

#### 4.5.25 static void CLOCK\_SetRtcClkOutConfig ( uint8\_t *div* ) [inline], [static]

This function sets the RTC\_CLOCKOUT configuration.

Parameters

|            |                                       |
|------------|---------------------------------------|
| <i>div</i> | The divider to set ( <i>div</i> > 0). |
|------------|---------------------------------------|

#### 4.5.26 uint32\_t CLOCKGetXbarBusClkFreq ( void )

This function gets the CGC XBAR bus clock frequency.

Returns

Clock frequency.

#### 4.5.27 uint32\_t CLOCK\_GetHifiDspSysClkFreq ( cgc\_sys\_clk\_t *type* )

This function gets the CGC HIFI DSP system clock frequency. These clocks are used for core, platform domains.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>type</i> | Which type of clock to get. |
|-------------|-----------------------------|

Returns

Clock frequency.

#### 4.5.28 static void CLOCK\_SetHifiDspSysClkConfig ( const cgc\_hifi\_sys\_clk\_config\_t \* *config* ) [inline], [static]

This function sets the system clock configuration for HIFI4 DSP domain.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>config</i> | Pointer to the configuration. |
|---------------|-------------------------------|

#### 4.5.29 static void CLOCK\_GetHifiDspSysClkConfig ( `cgc_hifi_sys_clk_config_t * config` ) [inline], [static]

This function gets the system configuration for HIFI4 DSP domain.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>config</i> | Pointer to the configuration. |
|---------------|-------------------------------|

#### 4.5.30 uint32\_t CLOCK\_GetLpavSysClkFreq ( `cgc_sys_clk_t type` )

This function gets the CGC NIC LPAV system clock frequency. These clocks are used for AXI, AHB, Bus domains.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>type</i> | Which type of clock to get. |
|-------------|-----------------------------|

Returns

Clock frequency.

#### 4.5.31 static void CLOCK\_SetLpavSysClkConfig ( `const cgc_lpav_sys_clk_config_t * config` ) [inline], [static]

This function sets the system clock configuration for NIC LPAV domain.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>config</i> | Pointer to the configuration. |
|---------------|-------------------------------|

#### 4.5.32 static void CLOCK\_GetLpavSysClkConfig ( `cgc_lpav_sys_clk_config_t * config` ) [inline], [static]

This function gets the system configuration for NIC LPAV domain.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>config</i> | Pointer to the configuration. |
|---------------|-------------------------------|

#### 4.5.33 **uint32\_t CLOCK\_GetDdrClkFreq ( void )**

This function gets the CGC DDR clock frequency.

Returns

Clock frequency.

#### 4.5.34 **static void CLOCK\_SetLpavClkOutConfig ( clock\_lpav\_clkout\_src\_t *setting*, uint8\_t *div*, bool *enable* ) [inline], [static]**

This function sets the clock out configuration.

Parameters

|                |                                       |
|----------------|---------------------------------------|
| <i>setting</i> | The selection to set.                 |
| <i>div</i>     | The divider to set ( <i>div</i> > 0). |
| <i>enable</i>  | Enable clock out.                     |

#### 4.5.35 **status\_t CLOCK\_InitSysOsc ( const cgc\_sosc\_config\_t \* *config* )**

This function enables the CGC system OSC clock according to the configuration.

Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>config</i> | Pointer to the configuration structure. |
|---------------|-----------------------------------------|

Return values

|                        |                            |
|------------------------|----------------------------|
| <i>kStatus_Success</i> | System OSC is initialized. |
|------------------------|----------------------------|

|                         |                                                              |
|-------------------------|--------------------------------------------------------------|
| <i>kStatus_CGC_Busy</i> | System OSC has been enabled and is used by the system clock. |
| <i>kStatus_ReadOnly</i> | System OSC control register is locked.                       |

## Note

This function can't detect whether the system OSC has been enabled and used by an IP.

**4.5.36 status\_t CLOCK\_DeinitSysOsc ( void )**

This function disables the CGC system OSC clock.

## Return values

|                         |                                         |
|-------------------------|-----------------------------------------|
| <i>kStatus_Success</i>  | System OSC is deinitialized.            |
| <i>kStatus_CGC_Busy</i> | System OSC is used by the system clock. |
| <i>kStatus_ReadOnly</i> | System OSC control register is locked.  |

## Note

This function can't detect whether the system OSC is used by an IP.

**4.5.37 void CLOCK\_SetRtdSysOscAsyncClkDiv ( cgc\_async\_clk\_t *asyncClk*, uint8\_t *divider* )**

## Parameters

|                 |                                                       |
|-----------------|-------------------------------------------------------|
| <i>asyncClk</i> | Which asynchronous clock to configure.                |
| <i>divider</i>  | The divider value to set. Disabled when divider == 0. |

## Note

There might be glitch when changing the asynchronous divider, so make sure the asynchronous clock is not used while changing divider.

**4.5.38 void CLOCK\_SetAdSysOscAsyncClkDiv ( cgc\_async\_clk\_t *asyncClk*, uint8\_t *divider* )**

Parameters

|                 |                                                       |
|-----------------|-------------------------------------------------------|
| <i>asyncClk</i> | Which asynchronous clock to configure.                |
| <i>divider</i>  | The divider value to set. Disabled when divider == 0. |

Note

There might be glitch when changing the asynchronous divider, so make sure the asynchronous clock is not used while changing divider.

#### 4.5.39 void CLOCK\_SetLpavSysOscAsyncClkDiv ( `cgc_async_clk_t asyncClk,` `uint8_t divider` )

Parameters

|                 |                                                       |
|-----------------|-------------------------------------------------------|
| <i>asyncClk</i> | Which asynchronous clock to configure.                |
| <i>divider</i>  | The divider value to set. Disabled when divider == 0. |

Note

There might be glitch when changing the asynchronous divider, so make sure the asynchronous clock is not used while changing divider.

#### 4.5.40 uint32\_t CLOCK\_GetSysOscFreq ( `void` )

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.41 uint32\_t CLOCK\_GetRtdSysOscAsyncFreq ( `cgc_async_clk_t type` )

Parameters

---

|             |                              |
|-------------|------------------------------|
| <i>type</i> | The asynchronous clock type. |
|-------------|------------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.42 `uint32_t CLOCK_GetAdSysOscAsyncFreq ( cgc_async_clk_t type )`

Parameters

|             |                              |
|-------------|------------------------------|
| <i>type</i> | The asynchronous clock type. |
|-------------|------------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.43 `uint32_t CLOCK_GetLpavSysOscAsyncFreq ( cgc_async_clk_t type )`

Parameters

|             |                              |
|-------------|------------------------------|
| <i>type</i> | The asynchronous clock type. |
|-------------|------------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.44 `static bool CLOCK_IsSysOscErr ( void ) [inline], [static]`

Returns

True if the error occurs, false if not.

#### 4.5.45 `static void CLOCK_SetSysOscMonitorMode ( cgc_sosc_monitor_mode_t mode ) [inline], [static]`

This function sets the system OSC monitor mode. The mode can be disabled, it can generate an interrupt when the error is disabled, or reset when the error is detected.

Parameters

|             |                      |
|-------------|----------------------|
| <i>mode</i> | Monitor mode to set. |
|-------------|----------------------|

#### 4.5.46 static bool CLOCK\_IsSysOscSelected( void ) [inline], [static]

Returns

True if system OSC is used as clock source, false if not.

#### 4.5.47 static bool CLOCK\_IsSysOscValid( void ) [inline], [static]

Returns

True if clock is valid, false if not.

#### 4.5.48 status\_t CLOCK\_InitFro( const cgc\_fro\_config\_t \* config )

This function initializes the CGC FRO clock according to the configuration.

Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>config</i> | Pointer to the configuration structure. |
|---------------|-----------------------------------------|

Return values

|                         |                                                   |
|-------------------------|---------------------------------------------------|
| <i>kStatus_Success</i>  | FRO is initialized.                               |
| <i>kStatus_CGC_Busy</i> | FRO has been enabled and is used by system clock. |
| <i>kStatus_ReadOnly</i> | FRO control register is locked.                   |

Note

This function can't detect whether the FRO has been enabled and used by an IP.

#### 4.5.49 status\_t CLOCK\_DeinitFro( void )

This function deinitializes the CGC FRO.

Return values

|                         |                                 |
|-------------------------|---------------------------------|
| <i>kStatus_Success</i>  | FRO is deinitialized.           |
| <i>kStatus_CGC_Busy</i> | FRO is used by system clock.    |
| <i>kStatus_ReadOnly</i> | FRO control register is locked. |

Note

This function can't detect whether the FRO is used by an IP.

#### 4.5.50 void CLOCK\_SetRtdFroAsyncClkDiv ( *cgc\_async\_clk\_t asyncClk*, *uint8\_t divider* )

Parameters

|                 |                                                       |
|-----------------|-------------------------------------------------------|
| <i>asyncClk</i> | Which asynchronous clock to configure.                |
| <i>divider</i>  | The divider value to set. Disabled when divider == 0. |

Note

There might be glitch when changing the asynchronous divider, so make sure the asynchronous clock is not used while changing divider.

#### 4.5.51 void CLOCK\_SetAdFroAsyncClkDiv ( *cgc\_async\_clk\_t asyncClk*, *uint8\_t divider* )

Parameters

|                 |                                                       |
|-----------------|-------------------------------------------------------|
| <i>asyncClk</i> | Which asynchronous clock to configure.                |
| <i>divider</i>  | The divider value to set. Disabled when divider == 0. |

Note

There might be glitch when changing the asynchronous divider, so make sure the asynchronous clock is not used while changing divider.

#### 4.5.52 void CLOCK\_SetLpavFroAsyncClkDiv ( *cgc\_async\_clk\_t asyncClk*, *uint8\_t divider* )

Parameters

|                 |                                                       |
|-----------------|-------------------------------------------------------|
| <i>asyncClk</i> | Which asynchronous clock to configure.                |
| <i>divider</i>  | The divider value to set. Disabled when divider == 0. |

Note

There might be glitch when changing the asynchronous divider, so make sure the asynchronous clock is not used while changing divider.

#### 4.5.53 void CLOCK\_EnableFroTuning ( bool *enable* )

On enable, the function will wait until FRO is close to the target frequency.

#### 4.5.54 uint32\_t CLOCK\_GetFroFreq ( void )

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.55 uint32\_t CLOCK\_GetRtdFroAsyncFreq ( cgc\_async\_clk\_t *type* )

Parameters

|             |                              |
|-------------|------------------------------|
| <i>type</i> | The asynchronous clock type. |
|-------------|------------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.56 uint32\_t CLOCK\_GetAdFroAsyncFreq ( cgc\_async\_clk\_t *type* )

Parameters

|             |                              |
|-------------|------------------------------|
| <i>type</i> | The asynchronous clock type. |
|-------------|------------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.57 **uint32\_t CLOCK\_GetLpavFroAsyncFreq ( cgc\_async\_clk\_t *type* )**

Parameters

|             |                              |
|-------------|------------------------------|
| <i>type</i> | The asynchronous clock type. |
|-------------|------------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.58 **static bool CLOCK\_IsFroSelected ( void ) [inline], [static]**

Returns

True if FRO is used as clock source, false if not.

#### 4.5.59 **static bool CLOCK\_IsFroValid ( void ) [inline], [static]**

Returns

True if clock is valid, false if not.

#### 4.5.60 **status\_t CLOCK\_InitLposc ( const cgc\_lposc\_config\_t \* *config* )**

This function initializes the CGC LPOSOC clock according to the configuration.

Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>config</i> | Pointer to the configuration structure. |
|---------------|-----------------------------------------|

Return values

|                         |                                 |
|-------------------------|---------------------------------|
| <i>kStatus_Success</i>  | LPOSC is initialized.           |
| <i>kStatus_ReadOnly</i> | FRO control register is locked. |

Note

This function can't detect whether the LPOSC has been enabled and used by an IP.

#### 4.5.61 **status\_t CLOCK\_DeinitLposc( void )**

This function deinitializes the CGC LPOSC.

Return values

|                         |                                   |
|-------------------------|-----------------------------------|
| <i>kStatus_Success</i>  | LPOSC is deinitialized.           |
| <i>kStatus_ReadOnly</i> | LPOSC control register is locked. |

Note

This function can't detect whether the LPOSC is used by an IP.

#### 4.5.62 **static bool CLOCK\_IsLpOscValid( void ) [inline], [static]**

Returns

True if clock is valid, false if not.

#### 4.5.63 **uint32\_t CLOCK\_GetLpOscFreq( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.64 **uint32\_t CLOCK\_GetRtcOscFreq( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.65 static bool CLOCK\_IsRtcOscErr( void ) [inline], [static]**

Returns

True if error occurs, false if not.

**4.5.66 void CLOCK\_SetRtcOscMonitorMode( cgc\_rosc\_monitor\_mode\_t mode )**

This function sets the RTC OSC monitor mode. The mode can be disabled. It can generate an interrupt when the error is disabled, or reset when the error is detected.

Parameters

|             |                      |
|-------------|----------------------|
| <i>mode</i> | Monitor mode to set. |
|-------------|----------------------|

**4.5.67 static bool CLOCK\_IsRtcOscSelected( void ) [inline], [static]**

Returns

True if RTCOSC is used as clock source, false if not.

**4.5.68 static bool CLOCK\_IsRtcOscValid( void ) [inline], [static]**

Returns

True if the clock is valid, false if not.

**4.5.69 status\_t CLOCK\_InitPll0( const cgc\_pll0\_config\_t \* config )**

This function enables the CGC PLL0 clock according to the configuration. The PLL0 can use the OSC or FRO as the clock source. Ensure that the source clock is valid before calling this function.

Example code for initializing PLL0 clock output:

```
* const cgc_pll0_config_t g_cgcPll0Config = { .enableMode =
 kCGC_PllEnable,
*
*
*
*
*
* .div1 = 1U,
* .pfld1Div = 2U,
* .pfld2Div = 0U,
* .src = kCGC_PllSrcSysOsc,
* .mult = kCGC_Pll0Mult20 };
*
* CLOCK_InitPll0(&g_cgcPll0Config);
*
```

Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>config</i> | Pointer to the configuration structure. |
|---------------|-----------------------------------------|

Return values

|                         |                                                        |
|-------------------------|--------------------------------------------------------|
| <i>kStatus_Success</i>  | PLL0 is initialized.                                   |
| <i>kStatus_CGC_Busy</i> | PLL0 has been enabled and is used by the system clock. |
| <i>kStatus_ReadOnly</i> | PLL0 control register is locked.                       |

Note

This function can't detect whether the PLL0 has been enabled and used by an IP.

#### 4.5.70 status\_t CLOCK\_DeinitPll0 ( void )

This function disables the CGC PLL0.

Return values

|                         |                                   |
|-------------------------|-----------------------------------|
| <i>kStatus_Success</i>  | PLL0 is deinitialized.            |
| <i>kStatus_CGC_Busy</i> | PLL0 is used by the system clock. |
| <i>kStatus_ReadOnly</i> | PLL0 control register is locked.  |

Note

This function can't detect whether the PLL0 is used by an IP.

#### 4.5.71 void CLOCK\_SetPll0AsyncClkDiv ( cgc\_async\_clk\_t *asyncClk*, uint8\_t *divider* )

Parameters

|                 |                                        |
|-----------------|----------------------------------------|
| <i>asyncClk</i> | Which asynchronous clock to configure. |
|-----------------|----------------------------------------|

|                |                                                       |
|----------------|-------------------------------------------------------|
| <i>divider</i> | The divider value to set. Disabled when divider == 0. |
|----------------|-------------------------------------------------------|

## Note

There might be glitch when changing the asynchronous divider, so make sure the asynchronous clock is not used while changing divider.

**4.5.72 uint32\_t CLOCK\_GetPII0Freq ( void )**

## Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.73 uint32\_t CLOCK\_GetPII0AsyncFreq ( cgc\_async\_clk\_t *type* )**

## Parameters

|             |                              |
|-------------|------------------------------|
| <i>type</i> | The asynchronous clock type. |
|-------------|------------------------------|

## Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.74 uint32\_t CLOCK\_GetPII0PfdFreq ( cgc\_pll\_pfd\_clkout\_t *pfdClkout* )**

## Parameters

|                  |                                                         |
|------------------|---------------------------------------------------------|
| <i>pfdClkout</i> | The selected PFD clock out. See "cgc_pll_pfd_clkout_t". |
|------------------|---------------------------------------------------------|

## Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.75 void CLOCK\_EnablePII0PfdClkout ( cgc\_pll\_pfd\_clkout\_t *pfdClkout*, uint8\_t *fracValue* )**

PLL Frequency = Fref \* MULT  
 PFD Clock Frequency = PLL output frequency \* 18/frac value

```

* Example code for configuring PLL0 PFD0 clock output:
* const cgc_pll0_config_t g_cgcPll0Config = { .enableMode =
 kCGC_PllEnable,
*
* .div1 = 1U,
* .pfld1Div = 2U,
* .pfld2Div = 0U,
* .src = kCGC_PllSrcSysOsc,
* .mult = kCGC_Pll0Mult20 };
*
* CLOCK_InitPll0(&g_cgcPll0Config);
* CLOCK_EnablePll0PfdClkout(kCGC_PllPfd0Clk, 15U);
*

```

## Parameters

|                  |                                                                              |
|------------------|------------------------------------------------------------------------------|
| <i>pfdClkout</i> | PLL0 PFD clock out select.                                                   |
| <i>fracValue</i> | Fractional Divider value. Recommended to be kept between 12-35 for all PFDs. |

#### 4.5.76 static void CLOCK\_SetPll0LockTime ( uint16\_t *lockTime* ) [inline], [static]

## Parameters

|                 |                                                                       |
|-----------------|-----------------------------------------------------------------------|
| <i>lockTime</i> | Reference clocks to count before PLL0 is considered locked and valid. |
|-----------------|-----------------------------------------------------------------------|

#### 4.5.77 static bool CLOCK\_IsPll0Selected ( void ) [inline], [static]

## Returns

True if PLL0 is used as clock source, false if not.

#### 4.5.78 static bool CLOCK\_IsPll0Valid ( void ) [inline], [static]

## Returns

True if the clock is valid, false if not.

#### 4.5.79 status\_t CLOCK\_InitPll1 ( const cgc\_pll1\_config\_t \* *config* )

This function enables the CGC PLL1 clock according to the configuration. The PLL1 can use the system OSC or FRO as the clock source. Ensure that the source clock is valid before calling this function.

Example code for initializing PLL1 clock output:

```

* const cgc_pll1_config_t g_cgcPll1Config = { .enableMode =
 kCGC_PllEnable,
*
* .div1 = 0U,
* .pfld1Div = 0U,
* .pfld2Div = 0U,
* .src = kCGC_PllSrcFro24M,
* .mult = kCGC_Pll1Mult22,
* .num = 578,
* .denom = 1000 };
* CLOCK_InitPll1(&g_cgcPll1Config);
*

```

## Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>config</i> | Pointer to the configuration structure. |
|---------------|-----------------------------------------|

## Return values

|                         |                                                        |
|-------------------------|--------------------------------------------------------|
| <i>kStatus_Success</i>  | PLL1 is initialized.                                   |
| <i>kStatus_CGC_Busy</i> | PLL1 has been enabled and is used by the system clock. |
| <i>kStatus_ReadOnly</i> | PLL1 control register is locked.                       |

## Note

This function can't detect whether the PLL1 has been enabled and is used by an IP.

**4.5.80 status\_t CLOCK\_DeinitPll1 ( void )**

This function disables the CGC PLL1.

## Return values

|                         |                                   |
|-------------------------|-----------------------------------|
| <i>kStatus_Success</i>  | PLL1 is deinitialized.            |
| <i>kStatus_CGC_Busy</i> | PLL1 is used by the system clock. |
| <i>kStatus_ReadOnly</i> | PLL1 control register is locked.  |

## Note

This function can't detect whether the PLL1 is used by an IP.

**4.5.81 void CLOCK\_SetPll1AsyncClkDiv ( cgc\_async\_clk\_t *asyncClk*, uint8\_t *divider* )**

Parameters

|                 |                                                       |
|-----------------|-------------------------------------------------------|
| <i>asyncClk</i> | Which asynchronous clock to configure.                |
| <i>divider</i>  | The divider value to set. Disabled when divider == 0. |

Note

There might be glitch when changing the asynchronous divider, so make sure the asynchronous clock is not used while changing divider.

#### 4.5.82 `uint32_t CLOCK_GetPII1Freq( void )`

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.83 `uint32_t CLOCK_GetPII1AsyncFreq( cgc_async_clk_t type )`

Parameters

|             |                              |
|-------------|------------------------------|
| <i>type</i> | The asynchronous clock type. |
|-------------|------------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.84 `uint32_t CLOCK_GetPII1PfdFreq( cgc_pll_pfd_clkout_t pfdClkout )`

Parameters

|                  |                                                          |
|------------------|----------------------------------------------------------|
| <i>pfdClkout</i> | The selected PFD clocks out. See "cgc_pll_pfd_clkout_t". |
|------------------|----------------------------------------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.85 void CLOCK\_EnablePll1PfdClkout ( *cgc\_pll\_pfd\_clkout\_t pfdClkout*, *uint8\_t fracValue* )

PLL1 Frequency = Fref \* (MULT + NUM/DENOM) PFD Clock Frequency = PLL output frequency \* 18/frac value

Example code for configuring PLL1 as PLL1 PFD clock output:

```
* const cgc_pll1_config_t g_cgcPll1Config = { .enableMode =
 kCGC_PllEnable,
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*
*
* CLOCK_InitPll1(&g_cgcPll1Config);
* CLOCK_EnablePll1PfdClkout(kCGC_PllPfd0Clk, 15U);
*
```

Parameters

|                  |                                                                              |
|------------------|------------------------------------------------------------------------------|
| <i>pfdClkout</i> | PLL1 PFD clock out select.                                                   |
| <i>fracValue</i> | Fractional Divider value. Recommended to be kept between 12-35 for all PFDs. |

#### 4.5.86 static void CLOCK\_EnablePll1SpectrumModulation ( *uint16\_t step*, *uint16\_t stop* ) [inline], [static]

This function sets the CGC PLL1 spread spectrum modulation configurations. STOP and STEP together control the modulation depth (maximum frequency change) and modulation frequency.

Modulation Depth = (STOP/MFD)\*Fref where MFD is the DENOM field value in DENOM register.  
Modulation Frequency = (STEP/(2\*STOP))\*Fref.

Parameters

|             |                            |
|-------------|----------------------------|
| <i>step</i> | PLL1 Spread Spectrum STEP. |
| <i>stop</i> | PLL1 Spread Spectrum STOP. |

#### 4.5.87 static void CLOCK\_SetPll1LockTime ( *uint16\_t lockTime* ) [inline], [static]

Parameters

|                 |                                                                       |
|-----------------|-----------------------------------------------------------------------|
| <i>lockTime</i> | Reference clocks to count before PLL1 is considered locked and valid. |
|-----------------|-----------------------------------------------------------------------|

#### 4.5.88 static bool CLOCK\_IsPII1Selected ( void ) [inline], [static]

Returns

True if PLL1 is used as clock source, false if not.

#### 4.5.89 static bool CLOCK\_IsPII1Valid ( void ) [inline], [static]

Returns

True if the clock is valid, false if not.

#### 4.5.90 uint32\_t CLOCK\_GetPII3Freq ( void )

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.91 uint32\_t CLOCK\_GetPII3AsyncFreq ( cgc\_async\_clk\_t *type* )

Parameters

|             |                              |
|-------------|------------------------------|
| <i>type</i> | The asynchronous clock type. |
|-------------|------------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.92 uint32\_t CLOCK\_GetPII3PfdFreq ( cgc\_pll\_pfd\_clkout\_t *pfdClkout* )

## Parameters

|                  |                                                         |
|------------------|---------------------------------------------------------|
| <i>pfdClkout</i> | The selected PFD clock out. See "cgc_pll_pfd_clkout_t". |
|------------------|---------------------------------------------------------|

## Returns

Clock frequency; If the clock is invalid, returns 0.

4.5.93 status\_t CLOCK\_InitPLL4 ( const cgc\_pll4\_config\_t \* config )

This function enables the CGC PLL4 clock according to the configuration. The PLL4 can use the OSC or FRO as the clock source. Ensure that the source clock is valid before calling this function.

Example code for initializing PLL4 clock output:

```
* const cgc_pll4_config_t g_cgcPll4Config = { .enableMode =
 kCGC_PllEnable,
*
* .div1 = OU,
* .pfld0Div1 = OU,
* .pfld0Div2 = OU,
* .pfld1Div1 = OU,
* .pfld1Div2 = OU,
* .pfld2Div1 = OU,
* .pfld2Div2 = OU,
* .pfld3Div1 = OU,
* .pfld3Div2 = OU,
* .src = kCGC_PllSrcFro24M,
* .mult = kCGC_Pll4Mult22,
* .num = 578,
* .denom = 1000};
*
* CLOCK_InitPll4 (&g_cgcPll4Config);
*
```

## Parameters

*config* Pointer to the configuration structure.

## Return values

|                               |                                                        |
|-------------------------------|--------------------------------------------------------|
| <code>kStatus_Success</code>  | PLL4 is initialized.                                   |
| <code>kStatus_CGC_Busy</code> | PLL4 has been enabled and is used by the system clock. |
| <code>kStatus_ReadOnly</code> | PLL4 control register is locked.                       |

## Note

This function can't detect whether the PLL4 has been enabled and used by an IP.

#### 4.5.94 status\_t CLOCK\_DeinitPLL4( void )

This function disables the CGC PLL4.

Return values

|                         |                                   |
|-------------------------|-----------------------------------|
| <i>kStatus_Success</i>  | PLL4 is deinitialized.            |
| <i>kStatus_CGC_Busy</i> | PLL4 is used by the system clock. |
| <i>kStatus_ReadOnly</i> | PLL4 control register is locked.  |

Note

This function can't detect whether the PLL4 is used by an IP.

#### 4.5.95 void CLOCK\_SetPll4AsyncClkDiv ( *cgc\_async\_clk\_t asyncClk*, *uint8\_t divider* )

Parameters

|                 |                                                       |
|-----------------|-------------------------------------------------------|
| <i>asyncClk</i> | Which asynchronous clock to configure.                |
| <i>divider</i>  | The divider value to set. Disabled when divider == 0. |

Note

There might be glitch when changing the asynchronous divider, so make sure the asynchronous clock is not used while changing divider.

#### 4.5.96 uint32\_t CLOCK\_GetPll4Freq ( void )

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.97 uint32\_t CLOCK\_GetPll4AsyncFreq ( *cgc\_async\_clk\_t type* )

Parameters

---

|             |                              |
|-------------|------------------------------|
| <i>type</i> | The asynchronous clock type. |
|-------------|------------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.98 `uint32_t CLOCK_GetPll4PfdFreq ( cgc_pll_pfd_clkout_t pfdClkout )`

Parameters

|                  |                                                         |
|------------------|---------------------------------------------------------|
| <i>pfdClkout</i> | The selected PFD clock out. See "cgc_pll_pfd_clkout_t". |
|------------------|---------------------------------------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.99 `void CLOCK_EnablePll4PfdClkout ( cgc_pll_pfd_clkout_t pfdClkout, uint8_t fracValue )`

PLL Frequency = Fref \* MULT PFD Clock Frequency = PLL output frequency \* 18/frac value

```
* Example code for configuring PLL4 PFD0 clock output:
* const cgc_pll4_config_t g_cgcPll4Config = { .enableMode =
 kCGC_PllEnable,
*
* .div1 = 0U,
* .pfd0Div1 = 0U,
* .pfd0Div2 = 0U,
* .pfd1Div1 = 0U,
* .pfd1Div2 = 0U,
* .pfd2Div1 = 0U,
* .pfd2Div2 = 0U,
* .pfd3Div1 = 0U,
* .pfd3Div2 = 0U,
* .src = kCGC_PllSrcFro24M,
* .mult = kCGC_Pll4Mult22,
* .num = 578,
* .denom = 1000 };
*
* CLOCK_InitPll4(&g_cgcPll4Config);
* CLOCK_EnablePll4PfdClkout(kCGC_PllPfd0Clk, 15U);
*
```

Parameters

|                  |                                                                              |
|------------------|------------------------------------------------------------------------------|
| <i>pf4Clkout</i> | PLL4 PFD clock out select.                                                   |
| <i>fracValue</i> | Fractional Divider value. Recommended to be kept between 12-35 for all PFDs. |

#### 4.5.100 static void CLOCK\_EnablePII4SpectrumModulation ( *uint16\_t step*, *uint16\_t stop* ) [inline], [static]

This function sets the CGC PLL4 spread spectrum modulation configurations. STOP and STEP together control the modulation depth (maximum frequency change) and modulation frequency.

Modulation Depth = (STOP/MFD)\*Fref where MFD is the DENOM field value in DENOM register.  
 Modulation Frequency = (STEP/(2\*STOP))\*Fref.

Parameters

|             |                            |
|-------------|----------------------------|
| <i>step</i> | PLL4 Spread Spectrum STEP. |
| <i>stop</i> | PLL4 Spread Spectrum STOP. |

#### 4.5.101 static void CLOCK\_SetPII4LockTime ( *uint16\_t lockTime* ) [inline], [static]

Parameters

|                 |                                                                       |
|-----------------|-----------------------------------------------------------------------|
| <i>lockTime</i> | Reference clocks to count before PLL4 is considered locked and valid. |
|-----------------|-----------------------------------------------------------------------|

#### 4.5.102 static bool CLOCK\_IsPII4Selected ( void ) [inline], [static]

Returns

True if PLL4 is used as clock source, false if not.

#### 4.5.103 static bool CLOCK\_IsPII4Valid ( void ) [inline], [static]

Returns

True if the clock is valid, false if not.

4.5.104 **static void CLOCK\_SetXtal0Freq ( uint32\_t *freq* ) [inline], [static]**

Parameters

|             |                                               |
|-------------|-----------------------------------------------|
| <i>freq</i> | The XTAL0/EXTAL0 input clock frequency in Hz. |
|-------------|-----------------------------------------------|

#### 4.5.105 static void CLOCK\_SetXtal32Freq ( uint32\_t *freq* ) [inline], [static]

Parameters

|             |                                                 |
|-------------|-------------------------------------------------|
| <i>freq</i> | The XTAL32/EXTAL32 input clock frequency in Hz. |
|-------------|-------------------------------------------------|

#### 4.5.106 static void CLOCK\_SetLvdsFreq ( uint32\_t *freq* ) [inline], [static]

Parameters

|             |                                           |
|-------------|-------------------------------------------|
| <i>freq</i> | The LVDS pad input clock frequency in Hz. |
|-------------|-------------------------------------------|

#### 4.5.107 static void CLOCK\_SetMclkFreq ( uint32\_t *index*, uint32\_t *freq* ) [inline], [static]

Parameters

|              |                                           |
|--------------|-------------------------------------------|
| <i>index</i> | The MCLK index.                           |
| <i>freq</i>  | The MCLK pad input clock frequency in Hz. |

#### 4.5.108 static void CLOCK\_SetRxBclkFreq ( uint32\_t *instance*, uint32\_t *freq* ) [inline], [static]

Parameters

|                 |                                                     |
|-----------------|-----------------------------------------------------|
| <i>instance</i> | The SAI instance to contribute to this RX_BCLK pad. |
| <i>freq</i>     | The RX_BCLK pad input clock frequency in Hz.        |

#### 4.5.109 static void CLOCK\_SetTxBclkFreq ( uint32\_t *instance*, uint32\_t *freq* ) [inline], [static]

Parameters

|                 |                                                     |
|-----------------|-----------------------------------------------------|
| <i>instance</i> | The SAI instance to contribute to this TX_BCLK pad. |
| <i>freq</i>     | The TX_BCLK pad input clock frequency in Hz.        |

#### 4.5.110 static void CLOCK\_SetSpdifRxFreq ( uint32\_t *freq* ) [inline], [static]

Parameters

|             |                                           |
|-------------|-------------------------------------------|
| <i>freq</i> | The SPDIF_RX input clock frequency in Hz. |
|-------------|-------------------------------------------|

#### 4.5.111 uint32\_t CLOCK\_GetWdogClkFreq ( uint32\_t *instance* )

Parameters

|                 |                            |
|-----------------|----------------------------|
| <i>instance</i> | The WDOG instance (0-2,5). |
|-----------------|----------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.112 uint32\_t CLOCK\_GetFlexspiClkFreq ( uint32\_t *instance* )

Parameters

|                 |                             |
|-----------------|-----------------------------|
| <i>instance</i> | The FlexSPI instance (0-1). |
|-----------------|-----------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.113 uint32\_t CLOCK\_GetLpitClkFreq ( void )

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.114 uint32\_t CLOCK\_GetFlexioClkFreq ( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.115 uint32\_t CLOCK\_GetI3cClkFreq ( uint32\_t *instance* )**

Parameters

|                 |                         |
|-----------------|-------------------------|
| <i>instance</i> | The I3C instance (0-1). |
|-----------------|-------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.116 uint32\_t CLOCK\_GetLpspiClkFreq ( uint32\_t *instance* )**

Parameters

|                 |                           |
|-----------------|---------------------------|
| <i>instance</i> | The LPSPI instance (0-3). |
|-----------------|---------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.117 uint32\_t CLOCK\_GetAdcClkFreq ( uint32\_t *instance* )**

Parameters

|                 |                         |
|-----------------|-------------------------|
| <i>instance</i> | The ADC instance (0-1). |
|-----------------|-------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.118 uint32\_t CLOCK\_GetDacClkFreq ( uint32\_t *instance* )**

Parameters

|                 |                         |
|-----------------|-------------------------|
| <i>instance</i> | The DAC instance (0-1). |
|-----------------|-------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.119 `uint32_t CLOCK_GetTpiuClkFreq ( void )`

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.120 `uint32_t CLOCK_GetSwoClkFreq ( void )`

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.121 `uint32_t CLOCK_GetTpmClkFreq ( uint32_t instance )`

Parameters

|                 |                         |
|-----------------|-------------------------|
| <i>instance</i> | The TPM instance (0-8). |
|-----------------|-------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.122 `uint32_t CLOCK_GetLpi2cClkFreq ( uint32_t instance )`

Parameters

|                 |                           |
|-----------------|---------------------------|
| <i>instance</i> | The LPI2C instance (0-3). |
|-----------------|---------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

4.5.123 `uint32_t CLOCK_GetLpuartClkFreq ( uint32_t instance )`

Parameters

|                 |                            |
|-----------------|----------------------------|
| <i>instance</i> | The LPUART instance (0-3). |
|-----------------|----------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

#### **4.5.124 uint32\_t CLOCK\_GetFlexcanClkFreq ( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

#### **4.5.125 uint32\_t CLOCK\_GetCsiClkFreq ( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

#### **4.5.126 uint32\_t CLOCK\_GetDsiClkFreq ( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

#### **4.5.127 uint32\_t CLOCK\_GetEpdcClkFreq ( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

#### **4.5.128 uint32\_t CLOCK\_GetGpu2dClkFreq ( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.129 uint32\_t CLOCK\_GetGpu3dClkFreq ( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.130 uint32\_t CLOCK\_GetDcnanoClkFreq ( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.131 uint32\_t CLOCK\_GetCsiUiClkFreq ( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.132 uint32\_t CLOCK\_GetCsiEscClkFreq ( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.133 uint32\_t CLOCK\_GetRtdAudClkFreq ( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.134 uint32\_t CLOCK\_GetAdAudClkFreq ( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.135 uint32\_t CLOCK\_GetLpavAudClkFreq( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.136 uint32\_t CLOCK\_GetSaiFreq( uint32\_t *instance* )**

Parameters

|                 |                         |
|-----------------|-------------------------|
| <i>instance</i> | The SAI instance (0-7). |
|-----------------|-------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.137 uint32\_t CLOCK\_GetSpdifFreq( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.138 uint32\_t CLOCK\_GetMqsFreq( uint32\_t *instance* )**

Parameters

|                 |                         |
|-----------------|-------------------------|
| <i>instance</i> | The MQS instance (0-1). |
|-----------------|-------------------------|

Returns

Clock frequency; If the clock is invalid, returns 0.

**4.5.139 uint32\_t CLOCK\_GetMicfilFreq( void )**

Returns

Clock frequency; If the clock is invalid, returns 0.

#### 4.5.140 `uint32_t CLOCK_GetMrtFreq( void )`

Returns

Clock frequency; If the clock is invalid, returns 0.

### 4.6 Variable Documentation

#### 4.6.1 `volatile uint32_t g_xtal0Freq`

The XTAL (SYSOSC) clock frequency in Hz. When the clock is set up, use the function `CLOCK_SetXtalFreq` to set the value in the clock driver. For example, if XTAL is 24 MHz:

```
* CLOCK_InitSysOsc(...);
* CLOCK_SetXtalFreq(24000000);
*
```

This is important for the multicore platforms where only one core needs to set up the OSC/SYSOSC using `CLOCK_InitSysOsc`. All other cores need to call the `CLOCK_SetXtalFreq` to get a valid clock frequency.

#### 4.6.2 `volatile uint32_t g_xtal32Freq`

The XTAL32/EXTAL32 clock frequency in Hz. When the clock is set up, use the function `CLOCK_SetXtal32Freq` to set the value in the clock driver.

This is important for the multicore platforms where only one core needs to set up the clock. All other cores need to call the `CLOCK_SetXtal32Freq` to get a valid clock frequency.

#### 4.6.3 `volatile uint32_t g_lvdsFreq`

The LVDS pad clock frequency in Hz. When the clock is set up, use the function `CLOCK_SetLvdsFreq` to set the value in the clock driver.

#### 4.6.4 `volatile uint32_t g_mclkFreq[4]`

The MCLK pad clock frequency in Hz. When the clock is set up, use the function `CLOCK_SetMclkFreq` to set the value in the clock driver.

#### 4.6.5 `volatile uint32_t g_rxBclkFreq[8]`

The RX\_BCLK pad clock frequency in Hz. When the clock is set up, use the function `CLOCK_SetRx-BclkFreq` to set the value in the clock driver.

#### 4.6.6 volatile uint32\_t g\_txBclkFreq[8]

The TX\_BCLK pad clock frequency in Hz. When the clock is set up, use the function CLOCK\_SetTxBclkFreq to set the value in the clock driver.

#### 4.6.7 volatile uint32\_t g\_spdifRxFreq

The SPDIF\_RX clock frequency in Hz. When the clock is sampled, use the function CLOCK\_SetSpdifRxFreq to set the value in the clock driver.

# **Chapter 5**

## **Fusion Driver**

Fusion driver provides APIs for Fusion (DSP Domain) operation.

The fusion driver supports:

- Fusion (DSP Domain) init
- Fusion core start and stop

# **Chapter 6**

## **IOMUXC: IOMUX Controller**

IOMUXC driver provides APIs for pin configuration. It also supports the miscellaneous functions integrated in IOMUXC.

# **Chapter 7**

## **Reset Driver**

Reset driver supports peripheral reset.

# **Chapter 8**

## **Sentinel Driver**

Sentinel driver supports Sentinel(S400) system.

# **Chapter 9**

## **Upower Driver**

Upower driver supports uPower Controller.

## 9.1 System Clock Generator (SCG)

The MCUXpresso SDK provides a peripheral driver for the System Clock Generator (SCG) module of MCUXpresso SDK devices.

### 9.1.1 Function description

The SCG module contains the system PLL (SPLL), a slow internal reference clock (SIRC), a fast internal reference clock (FIRC), a low power FLL, and the system oscillator clock (SOSC). They can be configured separately as the source of MCU system clocks. Accordingly, the SCG driver provides these functions:

- MCU system clock configuration.
- SCG SOSC configuration.
- SCG SIRC configuration.
- SCG FIRC configuration.
- SCG SPLL configuration.
- SCG LPFLL configuration.

#### 9.1.1.1 MCU System Clock

MCU system clock configurations include the clock source selection and the clock dividers. The configurations for VLPR, RUN, and HSRUN modes are set separately using the `CLOCK_SetVlprModeSysClkConfig()`, `CLOCK_SetRunModeSysClkConfig()`, and the `CLOCK_SetHsrunModeSysClkConfig()` functions to configure the MCU system clock.

The current MCU system clock configuration can be obtained with the function `CLOCK_GetCurSysClkConfig()`. The current MCU system clock frequency can be obtained with the `CLOCK_GetSysClkFreq()` function.

#### 9.1.1.2 SCG System OSC Clock

The functions `CLOCK_InitSysOsc()`/`CLOCK_DeinitSysOsc()` are used for the SOSC clock initialization. The function `CLOCK_InitSysOsc` disables the SOSC internally and re-configures it. As a result, ensure that the SOSC is not used while calling these functions.

The SOSC clock can be used directly as the MCU system clock source. The SOSCDIV1\_CLK, SOSCDIV2\_CLK, and SOSCDIV3\_CLK can be used as the peripheral clock source. The clocks frequencies can be obtained by functions `CLOCK_GetSysOscFreq()` and `CLOCK_GetSysOscAsyncFreq()`.

To configure the SOSC monitor mode, use the function `CLOCK_SetSysOscMonitorMode()`. The clock error status can be received and cleared with the `CLOCK_IsSysOscErr()` and `CLOCK_ClearSysOscErr()` functions.

### 9.1.1.3 SCG Slow IRC Clock

The functions `CLOCK_InitSirc()`/`CLOCK_DeinitSirc()` are used for the SIRC clock initialization. The function `CLOCK_InitSirc` disables the SIRC internally and re-configures it. Ensure that the SIRC is not used while calling these functions.

The SIRC clock can be used directly as the MCU system clock source. The `SIRCDIV1_CLK`, `SIRCDIV2_CLK`, and `SIRCDIV3_CLK` can be used as the peripheral clock source. The clocks frequencies can be received with functions `CLOCK_GetSircFreq()` and `CLOCK_GetSircAsyncFreq()`.

### 9.1.1.4 SCG Fast IRC Clock

The functions `CLOCK_InitFirc()`/`CLOCK_DeinitFirc()` are used for the FIRC clock initialization. The function `CLOCK_InitFirc` disables the FIRC internally and re-configures it. Ensure that the FIRC is not used while calling these functions.

The FIRC clock can be used directly as the MCU system clock source. The `FIRCDIV1_CLK`, `FIRCDIV2_CLK`, and `FIRCDIV3_CLK` can be used as the peripheral clock source. The clocks frequencies could be obtained by functions `CLOCK_GetFircFreq()` and `CLOCK_GetFircAsyncFreq()`.

The FIRC can be trimmed by the external clock. See the Section "Typical use case" to enable the FIRC trim.

### 9.1.1.5 SCG Low Power FLL Clock

The functions `CLOCK_InitLpFll()`/`CLOCK_DeinitLpFll()` are used for the LPFLL clock initialization. The function `CLOCK_InitLpFll` disables the LPFLL internally and re-configures it. Ensure that the LPFLL is not used while calling these functions.

The LPFLL clock can be used directly as the MCU system clock source. The `LPFLLDIV1_CLK`, `LPFLLDIV2_CLK`, and `LPFLLDIV3_CLK` can be used as the peripheral clock source. The clocks frequencies could be obtained by functions `CLOCK_GetLpFllFreq()` and `CLOCK_GetLpFllAsyncFreq()`.

The LPFLL can be trimmed by the external clock, specific the `trimConfig` in `scg_lppll_config_t` to enable the clock trim.

### 9.1.1.6 SCG System PLL Clock

The functions `CLOCK_InitSysPll()`/`CLOCK_DeinitSysPll()` are used for the SPLL clock initialization. The function `CLOCK_InitSysPll` disables the SPLL internally and re-configures it. Ensure that the SPLL is not used while calling these functions.

To generate the desired SPLL frequency, PREDIV and MULT value must be set properly while initializing the SPLL. The function `CLOCK_GetSysPllMultDiv()` calculates the PREDIV and MULT. Passing in the reference clock frequency and the desired output frequency, the function returns the PREDIV and MULT which generate the frequency closest to the desired frequency.

Because the SPLL is based on the FIRC or SOSC, the FIRC or SOSC must be enabled first before the SPLL initialization. Also, when re-configuring the FIRC or SOSC, be careful with the SPLL.

The SPLL clock can be used directly as the MCU system clock source. The SPLLDIV1\_CLK, SPLLDIV2\_CLK, and SPLLDIV3\_CLK can be used as the peripheral clock source. The clocks frequencies can be obtained with functions `CLOCK_GetSysPllFreq()` and `CLOCK_GetSysPllAsyncFreq()`.

To configure the SPLL monitor mode, use the function `CLOCK_SetSysPllMonitorMode()`. The clock error status can be received and cleared by the `CLOCK_IsSysPllErr()` and `CLOCK_ClearSysPllErr()`.

### 9.1.1.7 SCG clock valid check

The functions such as the `CLOCK_IsFircValid()` are used to check whether a specific clock is valid or not. See "Typical use case" for details.

The clocks are valid after the initialization functions such as the `CLOCK_InitFirc()`. As a result, it is not necessary to call the `CLOCK_IsFircValid()` after the `CLOCK_InitFirc()`.

## 9.1.2 Typical use case

### 9.1.2.1 FIRC clock trim

During the FIRC initialization, applications can choose whether to enable trim or not.

1. Trim is not enabled. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/scg
2. Trim is enabled. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/scg

### 9.1.2.2 SPLL initialization

The following code shows how to set up the SCG SPLL. The SPLL uses the SOSC as a reference clock. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/scg

### 9.1.2.3 System clock configuration

While changing the system clock configuration, the actual system clock does not change until the target clock source is valid. Ensure that the clock source is valid before using it. The functions such as `CLOCK_IsSircValid()` are used for this purpose.

The SCG has a dedicated system clock configuration registers for VLPR, RUN, and HSRUN modes. During the power mode change, the system clock configuration may change too. In this case, check whether the clock source is valid during the power mode change.

In the following example, the SIRC is used as the system clock source in VLPR mode, the FIRC is used as a system clock source in RUN mode, and the SPLL is used as a system clock source in HSRUN mode.

The example work flow:

1. SIRC, FIRC, and SPLL are all enabled in RUN mode.
2. MCU enters VLPR mode. In VLPR mode, FIRC, and SPLL are disabled automatically.
3. MCU enters RUN mode. Wait for the FIRC to become valid.
4. MCU enters HSRUN mode. In step 3, the SPLL is already enabled, but may not be valid. Wait for it to become valid when entering HSRUN mode. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/scg

# Chapter 10

## ACMP: Analog Comparator Driver

### 10.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Comparator (ACMP) module of MCUXpresso SDK devices.

The ACMP driver is created to help the user operate the ACMP module better. This driver can be considered as a basic comparator with advanced features. The APIs for basic comparator can make the C-MP work as a general comparator, which compares the two input channel's voltage and creates the output of the comparator result immediately. The APIs for advanced feature can be used as the plug-in function based on the basic comparator, and can provide more ways to process the comparator's output.

### 10.2 Typical use case

#### 10.2.1 Normal Configuration

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/acmp

#### 10.2.2 Interrupt Configuration

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/acmp

#### 10.2.3 Round robin Configuration

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/acmp

### Data Structures

- struct `acmp_config_t`  
*Configuration for ACMP.* [More...](#)
- struct `acmp_channel_config_t`  
*Configuration for channel.* [More...](#)
- struct `acmp_filter_config_t`  
*Configuration for filter.* [More...](#)
- struct `acmp_dac_config_t`  
*Configuration for DAC.* [More...](#)
- struct `acmp_round_robin_config_t`  
*Configuration for round robin mode.* [More...](#)
- struct `acmp_discrete_mode_config_t`  
*Configuration for discrete mode.* [More...](#)

## Macros

- #define **CMP\_C0\_CFx\_MASK** (CMP\_C0\_CFR\_MASK | CMP\_C0\_CFF\_MASK)  
*The mask of status flags cleared by writing 1.*

## Enumerations

- enum **\_acmp\_interrupt\_enable** {
   
**kACMP\_OutputRisingInterruptEnable** = (1U << 0U),
   
**kACMP\_OutputFallingInterruptEnable** = (1U << 1U),
   
**kACMP\_RoundRobinInterruptEnable** = (1U << 2U) }
   
*Interrupt enable/disable mask.*
- enum **\_acmp\_status\_flags** {
   
**kACMP\_OutputRisingEventFlag** = CMP\_C0\_CFR\_MASK,
   
**kACMP\_OutputFallingEventFlag** = CMP\_C0\_CFF\_MASK,
   
**kACMP\_OutputAssertEventFlag** = CMP\_C0\_COUT\_MASK }
   
*Status flag mask.*
- enum **acmp\_hysteresis\_mode\_t** {
   
**kACMP\_HysteresisLevel0** = 0U,
   
**kACMP\_HysteresisLevel1** = 1U,
   
**kACMP\_HysteresisLevel2** = 2U,
   
**kACMP\_HysteresisLevel3** = 3U }
   
*Comparator hard block hysteresis control.*
- enum **acmp\_reference\_voltage\_source\_t** {
   
**kACMP\_VrefSourceVin1** = 0U,
   
**kACMP\_VrefSourceVin2** = 1U }
   
*CMP Voltage Reference source.*
- enum **acmp\_fixed\_port\_t** {
   
**kACMP\_FixedPlusPort** = 0U,
   
**kACMP\_FixedMinusPort** = 1U }
   
*Fixed mux port.*
- enum **acmp\_dac\_work\_mode\_t** {
   
**kACMP\_DACWorkLowSpeedMode** = 0U,
   
**kACMP\_DACWorkHighSpeedMode** = 1U }
   
*Internal DAC's work mode.*
- enum **acmp\_discrete\_clock\_source\_t** {
   
**kACMP\_DiscreteClockSlow** = 0U,
   
**kACMP\_DiscreteClockFast** = 1U }
   
*Discrete mode clock selection.*
- enum **acmp\_discrete\_sample\_time\_t** {
   
**kACMP\_DiscreteSampleTimeAs1T** = 0U,
   
**kACMP\_DiscreteSampleTimeAs2T** = 1U,
   
**kACMP\_DiscreteSampleTimeAs4T** = 2U,
   
**kACMP\_DiscreteSampleTimeAs8T** = 3U,
   
**kACMP\_DiscreteSampleTimeAs16T** = 4U,
   
**kACMP\_DiscreteSampleTimeAs32T** = 5U,
   
**kACMP\_DiscreteSampleTimeAs64T** = 6U,
   
**kACMP\_DiscreteSampleTimeAs256T** = 7U }

- *ACMP discrete sample selection.*
  - enum acmp\_discrete\_phase\_time\_t {
 kACMP\_DiscretePhaseTimeAlt0 = 0U,
 kACMP\_DiscretePhaseTimeAlt1 = 1U,
 kACMP\_DiscretePhaseTimeAlt2 = 2U,
 kACMP\_DiscretePhaseTimeAlt3 = 3U,
 kACMP\_DiscretePhaseTimeAlt4 = 4U,
 kACMP\_DiscretePhaseTimeAlt5 = 5U,
 kACMP\_DiscretePhaseTimeAlt6 = 6U,
 kACMP\_DiscretePhaseTimeAlt7 = 7U }
- ACMP discrete phase time selection.*

## Driver version

- #define FSL\_ACMP\_DRIVER\_VERSION (MAKE\_VERSION(2U, 0U, 6U))  
*ACMP driver version 2.0.6.*

## Initialization and deinitialization

- void ACMP\_Init (CMP\_Type \*base, const acmp\_config\_t \*config)  
*Initializes the ACMP.*
- void ACMP\_Deinit (CMP\_Type \*base)  
*Deinitializes the ACMP.*
- void ACMP\_GetDefaultConfig (acmp\_config\_t \*config)  
*Gets the default configuration for ACMP.*

## Basic Operations

- void ACMP\_Enable (CMP\_Type \*base, bool enable)  
*Enables or disables the ACMP.*
- void ACMP\_EnableLinkToDAC (CMP\_Type \*base, bool enable)  
*Enables the link from CMP to DAC enable.*
- void ACMP\_SetChannelConfig (CMP\_Type \*base, const acmp\_channel\_config\_t \*config)  
*Sets the channel configuration.*

## Advanced Operations

- void ACMP\_EnableDMA (CMP\_Type \*base, bool enable)  
*Enables or disables DMA.*
- void ACMP\_EnableWindowMode (CMP\_Type \*base, bool enable)  
*Enables or disables window mode.*
- void ACMP\_SetFilterConfig (CMP\_Type \*base, const acmp\_filter\_config\_t \*config)  
*Configures the filter.*
- void ACMP\_SetDACConfig (CMP\_Type \*base, const acmp\_dac\_config\_t \*config)  
*Configures the internal DAC.*
- void ACMP\_SetRoundRobinConfig (CMP\_Type \*base, const acmp\_round\_robin\_config\_t \*config)  
*Configures the round robin mode.*
- void ACMP\_SetRoundRobinPreState (CMP\_Type \*base, uint32\_t mask)  
*Defines the pre-set state of channels in round robin mode.*

- static uint32\_t [ACMP\\_GetRoundRobinStatusFlags](#) (CMP\_Type \*base)  
*Gets the channel input changed flags in round robin mode.*
- void [ACMP\\_ClearRoundRobinStatusFlags](#) (CMP\_Type \*base, uint32\_t mask)  
*Clears the channel input changed flags in round robin mode.*
- static uint32\_t [ACMP\\_GetRoundRobinResult](#) (CMP\_Type \*base)  
*Gets the round robin result.*

## Interrupts

- void [ACMP\\_EnableInterrupts](#) (CMP\_Type \*base, uint32\_t mask)  
*Enables interrupts.*
- void [ACMP\\_DisableInterrupts](#) (CMP\_Type \*base, uint32\_t mask)  
*Disables interrupts.*

## Status

- uint32\_t [ACMP\\_GetStatusFlags](#) (CMP\_Type \*base)  
*Gets status flags.*
- void [ACMP\\_ClearStatusFlags](#) (CMP\_Type \*base, uint32\_t mask)  
*Clears status flags.*

## Discrete mode

- void [ACMP\\_SetDiscreteModeConfig](#) (CMP\_Type \*base, const acmp\_discrete\_mode\_config\_t \*config)  
*Configure the discrete mode.*
- void [ACMP\\_GetDefaultDiscreteModeConfig](#) (acmp\_discrete\_mode\_config\_t \*config)  
*Get the default configuration for discrete mode setting.*

## 10.3 Data Structure Documentation

### 10.3.1 struct acmp\_config\_t

#### Data Fields

- acmp\_hysteresis\_mode\_t [hysteresisMode](#)  
*Hysteresis mode.*
- bool [enableHighSpeed](#)  
*Enable High Speed (HS) comparison mode.*
- bool [enableInvertOutput](#)  
*Enable inverted comparator output.*
- bool [useUnfilteredOutput](#)  
*Set compare output(COUT) to equal COUTA(true) or COUT(false).*
- bool [enablePinOut](#)  
*The comparator output is available on the associated pin.*

#### Field Documentation

##### (1) acmp\_hysteresis\_mode\_t acmp\_config\_t::hysteresisMode

- (2) `bool acmp_config_t::enableHighSpeed`
- (3) `bool acmp_config_t::enableInvertOutput`
- (4) `bool acmp_config_t::useUnfilteredOutput`
- (5) `bool acmp_config_t::enablePinOut`

### 10.3.2 struct acmp\_channel\_config\_t

The comparator's port can be input from channel mux or DAC. If port input is from channel mux, detailed channel number for the mux should be configured.

#### Data Fields

- `uint32_t plusMuxInput`  
*Plus mux input channel(0~7).*
- `uint32_t minusMuxInput`  
*Minus mux input channel(0~7).*

#### Field Documentation

- (1) `uint32_t acmp_channel_config_t::plusMuxInput`
- (2) `uint32_t acmp_channel_config_t::minusMuxInput`

### 10.3.3 struct acmp\_filter\_config\_t

#### Data Fields

- `bool enableSample`  
*Using external SAMPLE as sampling clock input, or using divided bus clock.*
- `uint32_t filterCount`  
*Filter Sample Count.*
- `uint32_t filterPeriod`  
*Filter Sample Period.*

#### Field Documentation

- (1) `bool acmp_filter_config_t::enableSample`
- (2) `uint32_t acmp_filter_config_t::filterCount`

Available range is 1-7, 0 would cause the filter disabled.

- (3) `uint32_t acmp_filter_config_t::filterPeriod`

The divider to bus clock. Available range is 0-255.

### 10.3.4 struct acmp\_dac\_config\_t

#### Data Fields

- acmp\_reference\_voltage\_source\_t referenceVoltageSource  
*Supply voltage reference source.*
- uint32\_t DACValue  
*Value for DAC Output Voltage.*

#### Field Documentation

- (1) acmp\_reference\_voltage\_source\_t acmp\_dac\_config\_t::referenceVoltageSource
- (2) uint32\_t acmp\_dac\_config\_t::DACValue

Available range is 0-255.

### 10.3.5 struct acmp\_round\_robin\_config\_t

#### Data Fields

- acmp\_fixed\_port\_t fixedPort  
*Fixed mux port.*
- uint32\_t fixedChannelNumber  
*Indicates which channel is fixed in the fixed mux port.*
- uint32\_t checkerChannelMask  
*Mask of checker channel index.*
- uint32\_t sampleClockCount  
*Specifies how many round-robin clock cycles(0~3) later the sample takes place.*
- uint32\_t delayModulus  
*Comparator and DAC initialization delay modulus.*

#### Field Documentation

- (1) acmp\_fixed\_port\_t acmp\_round\_robin\_config\_t::fixedPort
- (2) uint32\_t acmp\_round\_robin\_config\_t::fixedChannelNumber
- (3) uint32\_t acmp\_round\_robin\_config\_t::checkerChannelMask

Available range is channel0:0x01 to channel7:0x80 for round-robin checker.

- (4) uint32\_t acmp\_round\_robin\_config\_t::sampleClockCount
- (5) uint32\_t acmp\_round\_robin\_config\_t::delayModulus

### 10.3.6 struct acmp\_discrete\_mode\_config\_t

#### Data Fields

- bool `enablePositiveChannelDiscreteMode`  
*Positive Channel Continuous Mode Enable.*
- bool `enableNegativeChannelDiscreteMode`  
*Negative Channel Continuous Mode Enable.*
- bool `enableResistorDivider`  
*Resistor Divider Enable is used to enable the resistor divider for the inputs when they come from 3v domain and their values are above 1.8v.*
- `acmp_discrete_clock_source_t clockSource`  
*Select the clock source in order to generate the required timing for comparator to work in discrete mode.*
- `acmp_discrete_sample_time_t sampleTime`  
*Select the ACMP total sampling time period.*
- `acmp_discrete_phase_time_t phase1Time`  
*Select the ACMP phase 1 sampling time.*
- `acmp_discrete_phase_time_t phase2Time`  
*Select the ACMP phase 2 sampling time.*

#### Field Documentation

(1) **bool acmp\_discrete\_mode\_config\_t::enablePositiveChannelDiscreteMode**

By default, the continuous mode is used.

(2) **bool acmp\_discrete\_mode\_config\_t::enableNegativeChannelDiscreteMode**

By default, the continuous mode is used.

(3) **bool acmp\_discrete\_mode\_config\_t::enableResistorDivider**

(4) `acmp_discrete_clock_source_t acmp_discrete_mode_config_t::clockSource`

(5) `acmp_discrete_sample_time_t acmp_discrete_mode_config_t::sampleTime`

(6) `acmp_discrete_phase_time_t acmp_discrete_mode_config_t::phase1Time`

(7) `acmp_discrete_phase_time_t acmp_discrete_mode_config_t::phase2Time`

### 10.4 Macro Definition Documentation

10.4.1 `#define FSL_ACMP_DRIVER_VERSION (MAKE_VERSION(2U, 0U, 6U))`

10.4.2 `#define CMP_C0_CFx_MASK (CMP_C0_CFR_MASK | CMP_C0_CFF_MASK)`

### 10.5 Enumeration Type Documentation

### 10.5.1 enum \_acmp\_interrupt\_enable

Enumerator

- kACMP\_OutputRisingInterruptEnable*** Enable the interrupt when comparator outputs rising.
- kACMP\_OutputFallingInterruptEnable*** Enable the interrupt when comparator outputs falling.
- kACMP\_RoundRobinInterruptEnable*** Enable the Round-Robin interrupt.

### 10.5.2 enum \_acmp\_status\_flags

Enumerator

- kACMP\_OutputRisingEventFlag*** Rising-edge on compare output has occurred.
- kACMP\_OutputFallingEventFlag*** Falling-edge on compare output has occurred.
- kACMP\_OutputAssertEventFlag*** Return the current value of the analog comparator output.

### 10.5.3 enum acmp\_hysteresis\_mode\_t

See chip data sheet to get the actual hysteresis value with each level.

Enumerator

- kACMP\_HysteresisLevel0*** Offset is level 0 and Hysteresis is level 0.
- kACMP\_HysteresisLevel1*** Offset is level 0 and Hysteresis is level 1.
- kACMP\_HysteresisLevel2*** Offset is level 0 and Hysteresis is level 2.
- kACMP\_HysteresisLevel3*** Offset is level 0 and Hysteresis is level 3.

### 10.5.4 enum acmp\_reference\_voltage\_source\_t

Enumerator

- kACMP\_VrefSourceVin1*** Vin1 is selected as resistor ladder network supply reference Vin.
- kACMP\_VrefSourceVin2*** Vin2 is selected as resistor ladder network supply reference Vin.

### 10.5.5 enum acmp\_fixed\_port\_t

Enumerator

- kACMP\_FixedPlusPort*** Only the inputs to the Minus port are swept in each round.
- kACMP\_FixedMinusPort*** Only the inputs to the Plus port are swept in each round.

### 10.5.6 enum acmp\_dac\_work\_mode\_t

Enumerator

*kACMP\_DACWorkLowSpeedMode* DAC is selected to work in low speed and low power mode.

*kACMP\_DACWorkHighSpeedMode* DAC is selected to work in high speed high power mode.

### 10.5.7 enum acmp\_discrete\_clock\_source\_t

Enumerator

*kACMP\_DiscreteClockSlow* Slow clock (32kHz) is used as the discrete mode clock.

*kACMP\_DiscreteClockFast* Fast clock (16-20MHz) is used as the discrete mode clock.

### 10.5.8 enum acmp\_discrete\_sample\_time\_t

These values configures the analog comparator sampling timing (specified by the discrete mode clock period T which is selected by [acmp\\_discrete\\_clock\\_source\\_t](#)) in discrete mode.

Enumerator

*kACMP\_DiscreteSampleTimeAs1T* The sampling time equals to 1xT.

*kACMP\_DiscreteSampleTimeAs2T* The sampling time equals to 2xT.

*kACMP\_DiscreteSampleTimeAs4T* The sampling time equals to 4xT.

*kACMP\_DiscreteSampleTimeAs8T* The sampling time equals to 8xT.

*kACMP\_DiscreteSampleTimeAs16T* The sampling time equals to 16xT.

*kACMP\_DiscreteSampleTimeAs32T* The sampling time equals to 32xT.

*kACMP\_DiscreteSampleTimeAs64T* The sampling time equals to 64xT.

*kACMP\_DiscreteSampleTimeAs256T* The sampling time equals to 256xT.

### 10.5.9 enum acmp\_discrete\_phase\_time\_t

There are two phases for sampling input signals, phase 1 and phase 2.

Enumerator

*kACMP\_DiscretePhaseTimeAlt0* The phase x active in one sampling selection 0.

*kACMP\_DiscretePhaseTimeAlt1* The phase x active in one sampling selection 1.

*kACMP\_DiscretePhaseTimeAlt2* The phase x active in one sampling selection 2.

*kACMP\_DiscretePhaseTimeAlt3* The phase x active in one sampling selection 3.

*kACMP\_DiscretePhaseTimeAlt4* The phase x active in one sampling selection 4.

*kACMP\_DiscretePhaseTimeAlt5* The phase x active in one sampling selection 5.

*kACMP\_DiscretePhaseTimeAlt6* The phase x active in one sampling selection 6.

*kACMP\_DiscretePhaseTimeAlt7* The phase x active in one sampling selection 7.

## 10.6 Function Documentation

### 10.6.1 void ACMP\_Init ( CMP\_Type \* *base*, const acmp\_config\_t \* *config* )

The default configuration can be got by calling [ACMP\\_GetDefaultConfig\(\)](#).

Parameters

|               |                                          |
|---------------|------------------------------------------|
| <i>base</i>   | ACMP peripheral base address.            |
| <i>config</i> | Pointer to ACMP configuration structure. |

### 10.6.2 void ACMP\_Deinit ( CMP\_Type \* *base* )

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ACMP peripheral base address. |
|-------------|-------------------------------|

### 10.6.3 void ACMP\_GetDefaultConfig ( acmp\_config\_t \* *config* )

This function initializes the user configuration structure to default value. The default value are:

Example:

```
config->enableHighSpeed = false;
config->enableInvertOutput = false;
config->useUnfilteredOutput = false;
config->enablePinOut = false;
config->enableHysteresisBothDirections = false;
config->hysteresisMode = kACMP_hysteresisMode0;
```

Parameters

|               |                                          |
|---------------|------------------------------------------|
| <i>config</i> | Pointer to ACMP configuration structure. |
|---------------|------------------------------------------|

### 10.6.4 void ACMP\_Enable ( CMP\_Type \* *base*, bool *enable* )

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | ACMP peripheral base address. |
| <i>enable</i> | True to enable the ACMP.      |

### 10.6.5 void ACMP\_EnableLinkToDAC ( **CMP\_Type** \* *base*, **bool** *enable* )

When this bit is set, the DAC enable/disable is controlled by the bit CMP\_C0[EN] instead of CMP\_C1[D-ACEN].

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | ACMP peripheral base address. |
| <i>enable</i> | Enable the feature or not.    |

### 10.6.6 void ACMP\_SetChannelConfig ( **CMP\_Type** \* *base*, **const acmp\_channel\_config\_t** \* *config* )

Note that the plus/minus mux's setting is only valid when the positive/negative port's input isn't from DAC but from channel mux.

Example:

```
acmp_channel_config_t configStruct = {0};
configStruct.positivePortInput = kACMP_PortInputFromDAC;
configStruct.negativePortInput = kACMP_PortInputFromMux;
configStruct.minusMuxInput = 1U;
ACMP_SetChannelConfig(CMP0, &configStruct);
```

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>base</i>   | ACMP peripheral base address.               |
| <i>config</i> | Pointer to channel configuration structure. |

### 10.6.7 void ACMP\_EnableDMA ( **CMP\_Type** \* *base*, **bool** *enable* )

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | ACMP peripheral base address. |
| <i>enable</i> | True to enable DMA.           |

### 10.6.8 void ACMP\_EnableWindowMode ( CMP\_Type \* *base*, bool *enable* )

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | ACMP peripheral base address. |
| <i>enable</i> | True to enable window mode.   |

### 10.6.9 void ACMP\_SetFilterConfig ( CMP\_Type \* *base*, const acmp\_filter\_config\_t \* *config* )

The filter can be enabled when the filter count is bigger than 1, the filter period is greater than 0 and the sample clock is from divided bus clock or the filter is bigger than 1 and the sample clock is from external clock. Detailed usage can be got from the reference manual.

Example:

```
acmp_filter_config_t configStruct = {0};
configStruct.filterCount = 5U;
configStruct.filterPeriod = 200U;
configStruct.enableSample = false;
ACMP_SetFilterConfig(CMP0, &configStruct);
```

Parameters

|               |                                            |
|---------------|--------------------------------------------|
| <i>base</i>   | ACMP peripheral base address.              |
| <i>config</i> | Pointer to filter configuration structure. |

### 10.6.10 void ACMP\_SetDACConfig ( CMP\_Type \* *base*, const acmp\_dac\_config\_t \* *config* )

Example:

```
acmp_dac_config_t configStruct = {0};
configStruct.referenceVoltageSource = kACMP_VrefSourceVin1;
configStruct.DACValue = 20U;
configStruct.enableOutput = false;
configStruct.workMode = kACMP_DACWorkLowSpeedMode;
ACMP_SetDACConfig(CMP0, &configStruct);
```

Parameters

|               |                                                                              |
|---------------|------------------------------------------------------------------------------|
| <i>base</i>   | ACMP peripheral base address.                                                |
| <i>config</i> | Pointer to DAC configuration structure. "NULL" is for disabling the feature. |

#### 10.6.11 void ACMP\_SetRoundRobinConfig ( CMP\_Type \* *base*, const acmp\_round\_robin\_config\_t \* *config* )

Example:

```
acmp_round_robin_config_t configStruct = {0};
configStruct.fixedPort = kACMP_FixedPlusPort;
configStruct.fixedChannelNumber = 3U;
configStruct.checkerChannelMask = 0xF7U;
configStruct.sampleClockCount = 0U;
configStruct.delayModulus = 0U;
ACMP_SetRoundRobinConfig(CMP0, &configStruct);
```

Parameters

|               |                                                                                           |
|---------------|-------------------------------------------------------------------------------------------|
| <i>base</i>   | ACMP peripheral base address.                                                             |
| <i>config</i> | Pointer to round robin mode configuration structure. "NULL" is for disabling the feature. |

#### 10.6.12 void ACMP\_SetRoundRobinPreState ( CMP\_Type \* *base*, uint32\_t *mask* )

Note: The pre-state has different circuit with get-round-robin-result in the SOC even though they are same bits. So get-round-robin-result can't return the same value as the value are set by pre-state.

Parameters

|             |                                                                                        |
|-------------|----------------------------------------------------------------------------------------|
| <i>base</i> | ACMP peripheral base address.                                                          |
| <i>mask</i> | Mask of round robin channel index. Available range is channel0:0x01 to channel7-:0x80. |

#### 10.6.13 static uint32\_t ACMP\_GetRoundRobinStatusFlags ( CMP\_Type \* *base* ) [inline], [static]

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ACMP peripheral base address. |
|-------------|-------------------------------|

Returns

Mask of channel input changed asserted flags. Available range is channel0:0x01 to channel7:0x80.

#### **10.6.14 void ACMP\_ClearRoundRobinStatusFlags ( CMP\_Type \* *base*, uint32\_t *mask* )**

Parameters

|             |                                                                           |
|-------------|---------------------------------------------------------------------------|
| <i>base</i> | ACMP peripheral base address.                                             |
| <i>mask</i> | Mask of channel index. Available range is channel0:0x01 to channel7:0x80. |

#### **10.6.15 static uint32\_t ACMP\_GetRoundRobinResult ( CMP\_Type \* *base* ) [inline], [static]**

Note that the set-pre-state has different circuit with get-round-robin-result in the SOC even though they are same bits. So [ACMP\\_GetRoundRobinResult\(\)](#) can't return the same value as the value are set by ACMP\_SetRoundRobinPreState.

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ACMP peripheral base address. |
|-------------|-------------------------------|

Returns

Mask of round robin channel result. Available range is channel0:0x01 to channel7:0x80.

#### **10.6.16 void ACMP\_EnableInterrupts ( CMP\_Type \* *base*, uint32\_t *mask* )**

Parameters

|             |                                                |
|-------------|------------------------------------------------|
| <i>base</i> | ACMP peripheral base address.                  |
| <i>mask</i> | Interrupts mask. See "_acmp_interrupt_enable". |

**10.6.17 void ACMP\_DisableInterrupts ( CMP\_Type \* *base*, uint32\_t *mask* )**

Parameters

|             |                                                |
|-------------|------------------------------------------------|
| <i>base</i> | ACMP peripheral base address.                  |
| <i>mask</i> | Interrupts mask. See "_acmp_interrupt_enable". |

**10.6.18 uint32\_t ACMP\_GetStatusFlags ( CMP\_Type \* *base* )**

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | ACMP peripheral base address. |
|-------------|-------------------------------|

Returns

Status flags asserted mask. See "\_acmp\_status\_flags".

**10.6.19 void ACMP\_ClearStatusFlags ( CMP\_Type \* *base*, uint32\_t *mask* )**

Parameters

|             |                                              |
|-------------|----------------------------------------------|
| <i>base</i> | ACMP peripheral base address.                |
| <i>mask</i> | Status flags mask. See "_acmp_status_flags". |

**10.6.20 void ACMP\_SetDiscreteModeConfig ( CMP\_Type \* *base*, const acmp\_discrete\_mode\_config\_t \* *config* )**

Configure the discrete mode when supporting 3V domain with 1.8V core.

Parameters

|               |                                                                        |
|---------------|------------------------------------------------------------------------|
| <i>base</i>   | ACMP peripheral base address.                                          |
| <i>config</i> | Pointer to configuration structure. See "acmp_discrete_mode_config_t". |

#### 10.6.21 **void ACMP\_GetDefaultDiscreteModeConfig ( acmp\_discrete\_mode\_config\_t \* *config* )**

Parameters

|               |                                                                            |
|---------------|----------------------------------------------------------------------------|
| <i>config</i> | Pointer to configuration structure to be restored with the setting values. |
|---------------|----------------------------------------------------------------------------|

# Chapter 11

## CACHE: LMEM CACHE Memory Controller

### 11.1 Overview

The MCUXpresso SDK provides a peripheral driver for the CACHE Controller of MCUXpresso SDK devices.

The CACHE driver is created to help the user more easily operate the cache memory. The APIs for basic operations are including the following three levels: 1L. The L1 cache driver API. This level provides the level 1 caches controller drivers. The L1 caches in this arch is the previous the local memory controller (LMEM).

2L. The unified cache driver API. This level provides many APIs for unified cache driver APIs for combined L1 and L2 cache maintain operations. This is provided for SDK drivers (DMA, ENET, US-DHC, etc) which should do the cache maintenance in their transactional APIs. Because in this arch, there is no L2 cache so the unified cache driver API directly calls only L1 driver APIs.

### 11.2 Function groups

#### 11.2.1 L1 CACHE Operation

The L1 CACHE has both code cache and data cache. This function group provides two independent API groups for both code cache and data cache. There are Enable/Disable APIs for code cache and data cache control and cache maintenance operations as Invalidate/Clean/CleanInvalidate by all and by address range.

#### Macros

- #define `L1CODEBUSCACHE_LINESIZE_BYTE` FSL\_FEATURE\_L1ICACHE\_LINESIZE\_BY-  
TE  
*code bus cache line size is equal to system bus line size, so the unified I/D cache line size equals too.*
- #define `L1SYSTEMBUSCACHE_LINESIZE_BYTE` `L1CODEBUSCACHE_LINESIZE_BYTE`  
*The system bus CACHE line size is 16B = 128b.*

#### Driver version

- #define `FSL_CACHE_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 6)`)  
*cache driver version.*

#### Unified Cache Control for all caches

- static void `ICACHE_InvalidateByRange` (uint32\_t address, uint32\_t size\_byte)  
*Invalidate instruction cache by range.*
- static void `DCACHE_InvalidateByRange` (uint32\_t address, uint32\_t size\_byte)  
*Invalidate data cache by range.*

- static void **DCACHE\_CleanByRange** (uint32\_t address, uint32\_t size\_byte)  
*Clean data cache by range.*
- static void **DCACHE\_CleanInvalidateByRange** (uint32\_t address, uint32\_t size\_byte)  
*Cleans and Invalidates data cache by range.*

## 11.3 Macro Definition Documentation

**11.3.1 #define FSL\_CACHE\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 6))**

**11.3.2 #define L1CODEBUSCACHE\_LINESIZE\_BYTE FSL\_FEATURE\_L1ICACHE\_LINESIZE\_BYTE**

The code bus CACHE line size is 16B = 128b.

**11.3.3 #define L1SYSTEMBUSCACHE\_LINESIZE\_BYTE L1CODEBUSCACHE\_LINESIZE\_BYTE**

## 11.4 Function Documentation

**11.4.1 static void ICACHE\_InvalidateByRange ( uint32\_t address, uint32\_t size\_byte ) [inline], [static]**

Parameters

|                  |                                       |
|------------------|---------------------------------------|
| <i>address</i>   | The physical address.                 |
| <i>size_byte</i> | size of the memory to be invalidated. |

Note

Address and size should be aligned to 16-Byte due to the cache operation unit FSL\_FEATURE\_L1ICACHE\_LINESIZE\_BYTE. The startAddr here will be forced to align to the cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

**11.4.2 static void DCACHE\_InvalidateByRange ( uint32\_t address, uint32\_t size\_byte ) [inline], [static]**

Parameters

|                  |                                       |
|------------------|---------------------------------------|
| <i>address</i>   | The physical address.                 |
| <i>size_byte</i> | size of the memory to be invalidated. |

Note

Address and size should be aligned to 16-Byte due to the cache operation unit FSL\_FEATURE\_L1DCACHE\_LINESIZE\_BYTE. The startAddr here will be forced to align to the cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

#### 11.4.3 static void DCACHE\_CleanByRange ( uint32\_t *address*, uint32\_t *size\_byte* ) [inline], [static]

Parameters

|                  |                                   |
|------------------|-----------------------------------|
| <i>address</i>   | The physical address.             |
| <i>size_byte</i> | size of the memory to be cleaned. |

Note

Address and size should be aligned to 16-Byte due to the cache operation unit FSL\_FEATURE\_L1DCACHE\_LINESIZE\_BYTE. The startAddr here will be forced to align to the cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

#### 11.4.4 static void DCACHE\_CleanInvalidateByRange ( uint32\_t *address*, uint32\_t *size\_byte* ) [inline], [static]

Parameters

|                  |                                                   |
|------------------|---------------------------------------------------|
| <i>address</i>   | The physical address.                             |
| <i>size_byte</i> | size of the memory to be Cleaned and Invalidated. |

Note

Address and size should be aligned to 16-Byte due to the cache operation unit FSL\_FEATURE\_L1DCACHE\_LINESIZE\_BYTE. The startAddr here will be forced to align to the cache line size if startAddr is not aligned. For the size\_byte, application should make sure the alignment or make sure the right operation order if the size\_byte is not aligned.

# Chapter 12

## Common Driver

### 12.1 Overview

The MCUXpresso SDK provides a driver for the common module of MCUXpresso SDK devices.

#### Macros

- `#define FSL_DRIVER_TRANSFER_DOUBLE_WEAK_IRQ 1`  
*Macro to use the default weak IRQ handler in drivers.*
- `#define MAKE_STATUS(group, code) (((group)*100L) + (code)))`  
*Construct a status code value from a group and code number.*
- `#define MAKE_VERSION(major, minor, bugfix) (((major) * 65536L) + ((minor) * 256L) + (bugfix))`  
*Construct the version number for drivers.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_NONE 0U`  
*No debug console.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_UART 1U`  
*Debug console based on UART.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_LPUART 2U`  
*Debug console based on LPUART.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_LPSCI 3U`  
*Debug console based on LPSCI.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_USBCDC 4U`  
*Debug console based on USBCDC.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_FLEXCOMM 5U`  
*Debug console based on FLEXCOMM.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_IUART 6U`  
*Debug console based on i.MX UART.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_VUSART 7U`  
*Debug console based on LPC\_VUSART.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_MINI_USART 8U`  
*Debug console based on LPC\_USART.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_SWO 9U`  
*Debug console based on SWO.*
- `#define DEBUG_CONSOLE_DEVICE_TYPE_QSCI 10U`  
*Debug console based on QSCI.*
- `#define ARRAY_SIZE(x) (sizeof(x) / sizeof((x)[0]))`  
*Computes the number of elements in an array.*

#### Typedefs

- `typedef int32_t status_t`  
*Type used for all status and error return values.*

## Enumerations

- enum `_status_groups` {  
  `kStatusGroup_Generic` = 0,  
  `kStatusGroup_FLASH` = 1,  
  `kStatusGroup_LP SPI` = 4,  
  `kStatusGroup_FLEXIO_SPI` = 5,  
  `kStatusGroup_DSPI` = 6,  
  `kStatusGroup_FLEXIO_UART` = 7,  
  `kStatusGroup_FLEXIO_I2C` = 8,  
  `kStatusGroup_LPI2C` = 9,  
  `kStatusGroup_UART` = 10,  
  `kStatusGroup_I2C` = 11,  
  `kStatusGroup_LPSCI` = 12,  
  `kStatusGroup_LPUART` = 13,  
  `kStatusGroup_SPI` = 14,  
  `kStatusGroup_XRDC` = 15,  
  `kStatusGroup_SEMA42` = 16,  
  `kStatusGroup_SDHC` = 17,  
  `kStatusGroup_SDMMC` = 18,  
  `kStatusGroup_SAI` = 19,  
  `kStatusGroup_MCG` = 20,  
  `kStatusGroup_SCG` = 21,  
  `kStatusGroup_SD SPI` = 22,  
  `kStatusGroup_FLEXIO_I2S` = 23,  
  `kStatusGroup_FLEXIO_MCULCD` = 24,  
  `kStatusGroup_FLASHIAP` = 25,  
  `kStatusGroup_FLEXCOMM_I2C` = 26,  
  `kStatusGroup_I2S` = 27,  
  `kStatusGroup_IUART` = 28,  
  `kStatusGroup_CSI` = 29,  
  `kStatusGroup_MIPI_DSI` = 30,  
  `kStatusGroup_SDRAMC` = 35,  
  `kStatusGroup_POWER` = 39,  
  `kStatusGroup_ENET` = 40,  
  `kStatusGroup_PHY` = 41,  
  `kStatusGroup_TRGMUX` = 42,  
  `kStatusGroup_SMARTCARD` = 43,  
  `kStatusGroup_LMEM` = 44,  
  `kStatusGroup_QSPI` = 45,  
  `kStatusGroup_DMA` = 50,  
  `kStatusGroup_EDMA` = 51,  
  `kStatusGroup_DMAMGR` = 52,  
  `kStatusGroup_FLEXCAN` = 53,  
  `kStatusGroup_LTC` = 54,  
  `kStatusGroup_FLEXIO_CAMERA` = 55,  
  `kStatusGroup_LPC_SPI` = 56,  
  `kStatusGroup_LPC_USACARD` = 58,  
  `kStatusGroup_SDIF` = 59,

```

kStatusGroup_POWER_MANAGER = 159 }

Status group numbers.
• enum {
 kStatus_Success = MAKE_STATUS(kStatusGroup_Generic, 0),
 kStatus_Fail = MAKE_STATUS(kStatusGroup_Generic, 1),
 kStatus_ReadOnly = MAKE_STATUS(kStatusGroup_Generic, 2),
 kStatus_OutOfRange = MAKE_STATUS(kStatusGroup_Generic, 3),
 kStatus_InvalidArgument = MAKE_STATUS(kStatusGroup_Generic, 4),
 kStatus_Timeout = MAKE_STATUS(kStatusGroup_Generic, 5),
 kStatus_NoTransferInProgress,
 kStatus_Busy = MAKE_STATUS(kStatusGroup_Generic, 7),
 kStatus_NoData }

Generic status return codes.

```

## Functions

- void \* **SDK\_Malloc** (size\_t size, size\_t alignbytes)  
*Allocate memory with given alignment and aligned size.*
- void **SDK\_Free** (void \*ptr)  
*Free memory.*
- void **SDK\_DelayAtLeastUs** (uint32\_t delayTime\_us, uint32\_t coreClock\_Hz)  
*Delay at least for some time.*

## Driver version

- #define **FSL\_COMMON\_DRIVER\_VERSION** (MAKE\_VERSION(2, 3, 2))  
*common driver version.*

## Min/max macros

- #define **MIN**(a, b) (((a) < (b)) ? (a) : (b))
- #define **MAX**(a, b) (((a) > (b)) ? (a) : (b))

## UINT16\_MAX/UINT32\_MAX value

- #define **UINT16\_MAX** ((uint16\_t)-1)
- #define **UINT32\_MAX** ((uint32\_t)-1)

## Suppress fallthrough warning macro

- #define **SUPPRESS\_FALL\_THROUGH\_WARNING()**

## 12.2 Macro Definition Documentation

### 12.2.1 #define FSL\_DRIVER\_TRANSFER\_DOUBLE\_WEAK\_IRQ 1

### 12.2.2 #define MAKE\_STATUS( *group*, *code* ) (((*group*)\*100L) + (*code*))

### 12.2.3 #define MAKE\_VERSION( major, minor, bugfix ) (((major) \* 65536L) + ((minor) \* 256L) + (bugfix))

The driver version is a 32-bit number, for both 32-bit platforms(such as Cortex M) and 16-bit platforms(such as DSC).

|        |               |               |         |   |
|--------|---------------|---------------|---------|---|
| Unused | Major Version | Minor Version | Bug Fix |   |
| 31     | 25 24         | 17 16         | 9 8     | 0 |

### 12.2.4 #define FSL\_COMMON\_DRIVER\_VERSION (MAKE\_VERSION(2, 3, 2))

### 12.2.5 #define DEBUG\_CONSOLE\_DEVICE\_TYPE\_NONE 0U

### 12.2.6 #define DEBUG\_CONSOLE\_DEVICE\_TYPE\_UART 1U

### 12.2.7 #define DEBUG\_CONSOLE\_DEVICE\_TYPE\_LPUART 2U

### 12.2.8 #define DEBUG\_CONSOLE\_DEVICE\_TYPE\_LPSCI 3U

### 12.2.9 #define DEBUG\_CONSOLE\_DEVICE\_TYPE\_USBCDC 4U

### 12.2.10 #define DEBUG\_CONSOLE\_DEVICE\_TYPE\_FLEXCOMM 5U

### 12.2.11 #define DEBUG\_CONSOLE\_DEVICE\_TYPE\_IUART 6U

### 12.2.12 #define DEBUG\_CONSOLE\_DEVICE\_TYPE\_VUSART 7U

### 12.2.13 #define DEBUG\_CONSOLE\_DEVICE\_TYPE\_MINI\_USART 8U

### 12.2.14 #define DEBUG\_CONSOLE\_DEVICE\_TYPE\_SWO 9U

### 12.2.15 #define DEBUG\_CONSOLE\_DEVICE\_TYPE\_QSCI 10U

### 12.2.16 #define ARRAY\_SIZE( x ) (sizeof(x) / sizeof((x)[0]))

## 12.3 Typedef Documentation

### 12.3.1 typedef int32\_t status\_t

## 12.4 Enumeration Type Documentation

### 12.4.1 enum \_status\_groups

Enumerator

- kStatusGroup\_Generic*** Group number for generic status codes.
- kStatusGroup\_FLASH*** Group number for FLASH status codes.
- kStatusGroup\_LP SPI*** Group number for LP SPI status codes.
- kStatusGroup\_FLEXIO\_SPI*** Group number for FLEXIO SPI status codes.
- kStatusGroup\_DSPI*** Group number for DSPI status codes.
- kStatusGroup\_FLEXIO\_UART*** Group number for FLEXIO UART status codes.
- kStatusGroup\_FLEXIO\_I2C*** Group number for FLEXIO I2C status codes.
- kStatusGroup\_LPI2C*** Group number for LPI2C status codes.
- kStatusGroup\_UART*** Group number for UART status codes.
- kStatusGroup\_I2C*** Group number for I2C status codes.
- kStatusGroup\_LPSCI*** Group number for LPSCI status codes.
- kStatusGroup\_LPUART*** Group number for LPUART status codes.
- kStatusGroup\_SPI*** Group number for SPI status code.
- kStatusGroup\_XRDC*** Group number for XRDC status code.
- kStatusGroup\_SEMA42*** Group number for SEMA42 status code.
- kStatusGroup\_SDHC*** Group number for SDHC status code.
- kStatusGroup\_SDMMC*** Group number for SDMMC status code.
- kStatusGroup\_SAI*** Group number for SAI status code.
- kStatusGroup\_MCG*** Group number for MCG status codes.
- kStatusGroup\_SCG*** Group number for SCG status codes.
- kStatusGroup\_SD SPI*** Group number for SD SPI status codes.
- kStatusGroup\_FLEXIO\_I2S*** Group number for FLEXIO I2S status codes.
- kStatusGroup\_FLEXIO\_MCU LCD*** Group number for FLEXIO LCD status codes.
- kStatusGroup\_FLASHIAP*** Group number for FLASHIAP status codes.
- kStatusGroup\_FLEXCOMM\_I2C*** Group number for FLEXCOMM I2C status codes.
- kStatusGroup\_I2S*** Group number for I2S status codes.
- kStatusGroup\_IUART*** Group number for IUART status codes.
- kStatusGroup\_CSI*** Group number for CSI status codes.
- kStatusGroup\_MIPI\_DSI*** Group number for MIPI DSI status codes.
- kStatusGroup\_SDRAMC*** Group number for SDRAMC status codes.
- kStatusGroup\_POWER*** Group number for POWER status codes.
- kStatusGroup\_ENET*** Group number for ENET status codes.
- kStatusGroup\_PHY*** Group number for PHY status codes.
- kStatusGroup\_TRGMUX*** Group number for TRGMUX status codes.
- kStatusGroup\_SMARTCARD*** Group number for SMARTCARD status codes.
- kStatusGroup\_LMEM*** Group number for LMEM status codes.
- kStatusGroup\_QSPI*** Group number for QSPI status codes.
- kStatusGroup\_DMA*** Group number for DMA status codes.
- kStatusGroup\_EDMA*** Group number for EDMA status codes.
- kStatusGroup\_DMAMGR*** Group number for DMAMGR status codes.

*kStatusGroup\_FLEXCAN* Group number for FlexCAN status codes.  
*kStatusGroup\_LTC* Group number for LTC status codes.  
*kStatusGroup\_FLEXIO\_CAMERA* Group number for FLEXIO CAMERA status codes.  
*kStatusGroup\_LPC\_SPI* Group number for LPC\_SPI status codes.  
*kStatusGroup\_LPC\_USART* Group number for LPC\_USART status codes.  
*kStatusGroup\_DMIC* Group number for DMIC status codes.  
*kStatusGroup\_SDIF* Group number for SDIF status codes.  
*kStatusGroup\_SPIFI* Group number for SPIFI status codes.  
*kStatusGroup OTP* Group number for OTP status codes.  
*kStatusGroup\_MCAN* Group number for MCAN status codes.  
*kStatusGroup\_CAAM* Group number for CAAM status codes.  
*kStatusGroup\_ECSPI* Group number for ECSPI status codes.  
*kStatusGroup\_USDHC* Group number for USDHC status codes.  
*kStatusGroup\_LPC\_I2C* Group number for LPC\_I2C status codes.  
*kStatusGroup\_DCP* Group number for DCP status codes.  
*kStatusGroup\_MSCAN* Group number for MSCAN status codes.  
*kStatusGroup\_ESAI* Group number for ESAI status codes.  
*kStatusGroup\_FLEXSPI* Group number for FLEXSPI status codes.  
*kStatusGroup\_MMDC* Group number for MMDC status codes.  
*kStatusGroup\_PDM* Group number for MIC status codes.  
*kStatusGroup\_SDMA* Group number for SDMA status codes.  
*kStatusGroup\_ICS* Group number for ICS status codes.  
*kStatusGroup\_SPDIF* Group number for SPDIF status codes.  
*kStatusGroup\_LPC\_MINISPI* Group number for LPC\_MINISPI status codes.  
*kStatusGroup\_HASHCRYPT* Group number for Hashcrypt status codes.  
*kStatusGroup\_LPC\_SPI\_SSP* Group number for LPC\_SPI\_SSP status codes.  
*kStatusGroup\_I3C* Group number for I3C status codes.  
*kStatusGroup\_LPC\_I2C\_1* Group number for LPC\_I2C\_1 status codes.  
*kStatusGroup\_NOTIFIER* Group number for NOTIFIER status codes.  
*kStatusGroup\_DebugConsole* Group number for debug console status codes.  
*kStatusGroup\_SEMC* Group number for SEMC status codes.  
*kStatusGroup\_ApplicationRangeStart* Starting number for application groups.  
*kStatusGroup\_IAP* Group number for IAP status codes.  
*kStatusGroup\_SFA* Group number for SFA status codes.  
*kStatusGroup\_SPC* Group number for SPC status codes.  
*kStatusGroup\_PUF* Group number for PUF status codes.  
*kStatusGroup\_TOUCH\_PANEL* Group number for touch panel status codes.  
*kStatusGroup\_HAL\_GPIO* Group number for HAL GPIO status codes.  
*kStatusGroup\_HAL\_UART* Group number for HAL UART status codes.  
*kStatusGroup\_HAL\_TIMER* Group number for HAL TIMER status codes.  
*kStatusGroup\_HAL\_SPI* Group number for HAL SPI status codes.  
*kStatusGroup\_HAL\_I2C* Group number for HAL I2C status codes.  
*kStatusGroup\_HAL\_FLASH* Group number for HAL FLASH status codes.  
*kStatusGroup\_HAL\_PWM* Group number for HAL PWM status codes.  
*kStatusGroup\_HAL\_RNG* Group number for HAL RNG status codes.

*kStatusGroup\_HAL\_I2S* Group number for HAL I2S status codes.  
*kStatusGroup\_TIMERMANAGER* Group number for TiMER MANAGER status codes.  
*kStatusGroup\_SERIALMANAGER* Group number for SERIAL MANAGER status codes.  
*kStatusGroup\_LED* Group number for LED status codes.  
*kStatusGroup\_BUTTON* Group number for BUTTON status codes.  
*kStatusGroup\_EXTERN\_EEPROM* Group number for EXTERN EEPROM status codes.  
*kStatusGroup\_SHELL* Group number for SHELL status codes.  
*kStatusGroup\_MEM\_MANAGER* Group number for MEM MANAGER status codes.  
*kStatusGroup\_LIST* Group number for List status codes.  
*kStatusGroup\_OSA* Group number for OSA status codes.  
*kStatusGroup\_COMMON\_TASK* Group number for Common task status codes.  
*kStatusGroup\_MSG* Group number for messaging status codes.  
*kStatusGroup\_SDK\_OCOTP* Group number for OCOTP status codes.  
*kStatusGroup\_SDK\_FLEXSPINOR* Group number for FLEXSPINOR status codes.  
*kStatusGroup\_CODEC* Group number for codec status codes.  
*kStatusGroup\_ASRC* Group number for codec status ASRC.  
*kStatusGroup\_OTFAD* Group number for codec status codes.  
*kStatusGroup\_SDIOSLV* Group number for SDIOSLV status codes.  
*kStatusGroup\_MECC* Group number for MECC status codes.  
*kStatusGroup\_ENET\_QOS* Group number for ENET\_QOS status codes.  
*kStatusGroup\_LOG* Group number for LOG status codes.  
*kStatusGroup\_I3CBUS* Group number for I3CBUS status codes.  
*kStatusGroup\_QSCI* Group number for QSCI status codes.  
*kStatusGroup\_SNT* Group number for SNT status codes.  
*kStatusGroup\_QUEUEDSPI* Group number for QSPI status codes.  
*kStatusGroup\_POWER\_MANAGER* Group number for POWER\_MANAGER status codes.

#### 12.4.2 anonymous enum

Enumerator

*kStatus\_Success* Generic status for Success.  
*kStatus\_Fail* Generic status for Fail.  
*kStatus\_ReadOnly* Generic status for read only failure.  
*kStatus\_OutOfRange* Generic status for out of range access.  
*kStatus\_InvalidArgument* Generic status for invalid argument check.  
*kStatus\_Timeout* Generic status for timeout.  
*kStatus\_NoTransferInProgress* Generic status for no transfer in progress.  
*kStatus\_Busy* Generic status for module is busy.  
*kStatus\_NoData* Generic status for no data is found for the operation.

#### 12.5 Function Documentation

### 12.5.1 **void\* SDK\_Malloc ( size\_t *size*, size\_t *alignbytes* )**

This is provided to support the dynamically allocated memory used in cache-able region.

Parameters

|                   |                                |
|-------------------|--------------------------------|
| <i>size</i>       | The length required to malloc. |
| <i>alignbytes</i> | The alignment size.            |

Return values

|            |                   |
|------------|-------------------|
| <i>The</i> | allocated memory. |
|------------|-------------------|

### 12.5.2 void SDK\_Free ( void \* *ptr* )

Parameters

|            |                           |
|------------|---------------------------|
| <i>ptr</i> | The memory to be release. |
|------------|---------------------------|

### 12.5.3 void SDK\_DelayAtLeastUs ( uint32\_t *delayTime\_us*, uint32\_t *coreClock\_Hz* )

Please note that, this API uses while loop for delay, different run-time environments make the time not precise, if precise delay count was needed, please implement a new delay function with hardware timer.

Parameters

|                     |                                    |
|---------------------|------------------------------------|
| <i>delayTime_us</i> | Delay time in unit of microsecond. |
| <i>coreClock_Hz</i> | Core clock frequency with Hz.      |

# Chapter 13

## CRC: Cyclic Redundancy Check Driver

### 13.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Cyclic Redundancy Check (CRC) module of MCUXpresso SDK devices.

The cyclic redundancy check (CRC) module generates 16/32-bit CRC code for error detection. The CRC module also provides a programmable polynomial, seed, and other parameters required to implement a 16-bit or 32-bit CRC standard.

### 13.2 CRC Driver Initialization and Configuration

[CRC\\_Init\(\)](#) function enables the clock gate for the CRC module in the SIM module and fully (re-)configures the CRC module according to the configuration structure. The seed member of the configuration structure is the initial checksum for which new data can be added to. When starting a new checksum computation, the seed is set to the initial checksum per the CRC protocol specification. For continued checksum operation, the seed is set to the intermediate checksum value as obtained from previous calls to [CRC\\_Get16bitResult\(\)](#) or [CRC\\_Get32bitResult\(\)](#) function. After calling the [CRC\\_Init\(\)](#), one or multiple [CRC\\_WriteData\(\)](#) calls follow to update the checksum with data and [CRC\\_Get16bitResult\(\)](#) or [CRC\\_Get32bitResult\(\)](#) follow to read the result. The crcResult member of the configuration structure determines whether the [CRC\\_Get16bitResult\(\)](#) or [CRC\\_Get32bitResult\(\)](#) return value is a final checksum or an intermediate checksum. The [CRC\\_Init\(\)](#) function can be called as many times as required allowing for runtime changes of the CRC protocol.

[CRC\\_GetDefaultConfig\(\)](#) function can be used to set the module configuration structure with parameters for CRC-16/CCIT-FALSE protocol.

### 13.3 CRC Write Data

The [CRC\\_WriteData\(\)](#) function adds data to the CRC. Internally, it tries to use 32-bit reads and writes for all aligned data in the user buffer and 8-bit reads and writes for all unaligned data in the user buffer. This function can update the CRC with user-supplied data chunks of an arbitrary size, so one can update the CRC byte by byte or with all bytes at once. Prior to calling the CRC configuration function [CRC\\_Init\(\)](#) fully specifies the CRC module configuration for the [CRC\\_WriteData\(\)](#) call.

### 13.4 CRC Get Checksum

The [CRC\\_Get16bitResult\(\)](#) or [CRC\\_Get32bitResult\(\)](#) function reads the CRC module data register. Depending on the prior CRC module usage, the return value is either an intermediate checksum or the final checksum. For example, for 16-bit CRCs the following call sequences can be used.

[CRC\\_Init\(\)](#) / [CRC\\_WriteData\(\)](#) / [CRC\\_Get16bitResult\(\)](#) to get the final checksum.

[CRC\\_Init\(\)](#) / [CRC\\_WriteData\(\)](#) / ... / [CRC\\_WriteData\(\)](#) / [CRC\\_Get16bitResult\(\)](#) to get the final checksum.

`CRC_Init()` / `CRC_WriteData()` / `CRC_Get16bitResult()` to get an intermediate checksum.

`CRC_Init()` / `CRC_WriteData()` / ... / `CRC_WriteData()` / `CRC_Get16bitResult()` to get an intermediate checksum.

## 13.5 Comments about API usage in RTOS

If multiple RTOS tasks share the CRC module to compute checksums with different data and/or protocols, the following needs to be implemented by the user.

The triplets

`CRC_Init()` / `CRC_WriteData()` / `CRC_Get16bitResult()` or `CRC_Get32bitResult()`

The triplets are protected by the RTOS mutex to protect the CRC module against concurrent accesses from different tasks. This is an example. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/crcRefer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/crc

## Data Structures

- struct `crc_config_t`  
*CRC protocol configuration. [More...](#)*

## Macros

- #define `CRC_DRIVER_USE_CRC16_CCIT_FALSE_AS_DEFAULT` 1  
*Default configuration structure filled by `CRC_GetDefaultConfig()`.*

## Enumerations

- enum `crc_bits_t` {  
`kCrcBits16` = 0U,  
`kCrcBits32` = 1U }  
*CRC bit width.*
- enum `crc_result_t` {  
`kCrcFinalChecksum` = 0U,  
`kCrcIntermediateChecksum` = 1U }  
*CRC result type.*

## Functions

- void `CRC_Init` (CRC\_Type \*base, const `crc_config_t` \*config)  
*Enables and configures the CRC peripheral module.*
- static void `CRC_Deinit` (CRC\_Type \*base)  
*Disables the CRC peripheral module.*
- void `CRC_GetDefaultConfig` (`crc_config_t` \*config)

- **void [CRC\\_WriteData](#) (CRC\_Type \*base, const uint8\_t \*data, size\_t dataSize)**  
*Writes data to the CRC module.*
- **uint32\_t [CRC\\_Get32bitResult](#) (CRC\_Type \*base)**  
*Reads the 32-bit checksum from the CRC module.*
- **uint16\_t [CRC\\_Get16bitResult](#) (CRC\_Type \*base)**  
*Reads a 16-bit checksum from the CRC module.*

## Driver version

- #define **FSL\_CRC\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 3))**  
*CRC driver version.*

## 13.6 Data Structure Documentation

### 13.6.1 struct [crc\\_config\\_t](#)

This structure holds the configuration for the CRC protocol.

#### Data Fields

- **uint32\_t polynomial**  
*CRC Polynomial, MSBit first.*
- **uint32\_t seed**  
*Starting checksum value.*
- **bool reflectIn**  
*Reflect bits on input.*
- **bool reflectOut**  
*Reflect bits on output.*
- **bool complementChecksum**  
*True if the result shall be complement of the actual checksum.*
- **crc\_bits\_t crcBits**  
*Selects 16- or 32- bit CRC protocol.*
- **crc\_result\_t crcResult**  
*Selects final or intermediate checksum return from [CRC\\_Get16bitResult\(\)](#) or [CRC\\_Get32bitResult\(\)](#)*

#### Field Documentation

##### (1) **uint32\_t [crc\\_config\\_t::polynomial](#)**

Example polynomial: 0x1021 = 1\_0000\_0010\_0001 =  $x^{12}+x^5+1$

##### (2) **bool [crc\\_config\\_t::reflectIn](#)**

##### (3) **bool [crc\\_config\\_t::reflectOut](#)**

##### (4) **bool [crc\\_config\\_t::complementChecksum](#)**

##### (5) **crc\_bits\_t [crc\\_config\\_t::crcBits](#)**

## 13.7 Macro Definition Documentation

### 13.7.1 #define FSL\_CRC\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 3))

Version 2.0.3.

Current version: 2.0.3

Change log:

- Version 2.0.3
  - Fix MISRA issues
- Version 2.0.2
  - Fix MISRA issues
- Version 2.0.1
  - move DATA and DATALL macro definition from header file to source file

### 13.7.2 #define CRC\_DRIVER\_USE\_CRC16\_CCIT\_FALSE\_AS\_DEFAULT 1

Use CRC16-CCIT-FALSE as default.

## 13.8 Enumeration Type Documentation

### 13.8.1 enum crc\_bits\_t

Enumerator

*kCrcBits16* Generate 16-bit CRC code.

*kCrcBits32* Generate 32-bit CRC code.

### 13.8.2 enum crc\_result\_t

Enumerator

*kCrcFinalChecksum* CRC data register read value is the final checksum. Reflect out and final xor protocol features are applied.

*kCrcIntermediateChecksum* CRC data register read value is intermediate checksum (raw value).

Reflect out and final xor protocol feature are not applied. Intermediate checksum can be used as a seed for [CRC\\_Init\(\)](#) to continue adding data to this checksum.

## 13.9 Function Documentation

### 13.9.1 void CRC\_Init ( **CRC\_Type** \* *base*, **const crc\_config\_t** \* *config* )

This function enables the clock gate in the SIM module for the CRC peripheral. It also configures the CRC module and starts a checksum computation by writing the seed.

Parameters

|               |                                     |
|---------------|-------------------------------------|
| <i>base</i>   | CRC peripheral address.             |
| <i>config</i> | CRC module configuration structure. |

### 13.9.2 static void CRC\_Deinit ( **CRC\_Type** \* *base* ) [inline], [static]

This function disables the clock gate in the SIM module for the CRC peripheral.

Parameters

|             |                         |
|-------------|-------------------------|
| <i>base</i> | CRC peripheral address. |
|-------------|-------------------------|

### 13.9.3 void CRC\_GetDefaultConfig ( **crc\_config\_t** \* *config* )

Loads default values to the CRC protocol configuration structure. The default values are as follows.

```
* config->polynomial = 0x1021;
* config->seed = 0xFFFF;
* config->reflectIn = false;
* config->reflectOut = false;
* config->complementChecksum = false;
* config->crcBits = kCrcBits16;
* config->crcResult = kCrcFinalChecksum;
*
```

Parameters

|               |                                       |
|---------------|---------------------------------------|
| <i>config</i> | CRC protocol configuration structure. |
|---------------|---------------------------------------|

### 13.9.4 void CRC\_WriteData ( **CRC\_Type** \* *base*, **const uint8\_t** \* *data*, **size\_t** *dataSize* )

Writes input data buffer bytes to the CRC data register. The configured type of transpose is applied.

Parameters

|                 |                                         |
|-----------------|-----------------------------------------|
| <i>base</i>     | CRC peripheral address.                 |
| <i>data</i>     | Input data stream, MSByte in data[0].   |
| <i>dataSize</i> | Size in bytes of the input data buffer. |

### 13.9.5 `uint32_t CRC_Get32bitResult ( CRC_Type * base )`

Reads the CRC data register (either an intermediate or the final checksum). The configured type of transpose and complement is applied.

Parameters

|             |                         |
|-------------|-------------------------|
| <i>base</i> | CRC peripheral address. |
|-------------|-------------------------|

Returns

An intermediate or the final 32-bit checksum, after configured transpose and complement operations.

### 13.9.6 `uint16_t CRC_Get16bitResult ( CRC_Type * base )`

Reads the CRC data register (either an intermediate or the final checksum). The configured type of transpose and complement is applied.

Parameters

|             |                         |
|-------------|-------------------------|
| <i>base</i> | CRC peripheral address. |
|-------------|-------------------------|

Returns

An intermediate or the final 16-bit checksum, after configured transpose and complement operations.

# Chapter 14

## DAC12: 12-bit Digital-to-Analog Converter Driver

### 14.1 Overview

The MCUXpresso SDK provides a peripheral driver for the 12-bit Digital-to-Analog Converter (DAC12) module of MCUXpresso SDK devices.

This DAC is the 12-bit resolution digital-to-analog converters with programmable reference generator output. Its output data items are loaded into a FIFO, so that various FIFO mode can be used to output the value for user-defined sequence.

The DAC driver provides a user-friendly interface to operate the DAC peripheral. The user can initialize/deinitialize the DAC driver, set data into FIFO, or enable the interrupt DMA for special events so that the hardware can process the DAC output data automatically. Also, the configuration for software and hardware trigger are also included in the driver.

### 14.2 Typical use case

#### 14.2.1 A simple use case to output the user-defined DAC12 value.

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/dac12

#### 14.2.2 Working with the trigger

Once more than one data is filled into the FIFO, the output pointer moves into configured mode when a trigger comes. This trigger can be from software or hardware, and moves one item for each trigger. Also, the interrupt/DMA event can be activated when the output pointer hits to the configured position.

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/dac12

### Files

- file [fsl\\_dac12.h](#)

### Data Structures

- struct [dac12\\_hardware\\_info\\_t](#)  
*DAC12 hardware information.* [More...](#)
- struct [dac12\\_config\\_t](#)  
*DAC12 module configuration.* [More...](#)

## Macros

- #define `DAC12_CR_W1C_FLAGS_MASK` (`DAC_CR_OVFF_MASK` | `DAC_CR_UDFF_MASK`)  
*Define "write 1 to clear" flags.*
- #define `DAC12_CR_ALL_FLAGS_MASK` (`DAC12_CR_W1C_FLAGS_MASK` | `DAC_CR_WMF_MASK` | `DAC_CR_NEMPTF_MASK` | `DAC_CR_FULLF_MASK`)  
*Define all the flag bits in DACx\_CR register.*

## Enumerations

- enum `_dac12_status_flags` {
   
`kDAC12_OverflowFlag` = `DAC_CR_OVFF_MASK`,  
`kDAC12_UnderflowFlag` = `DAC_CR_UDFF_MASK`,  
`kDAC12_WatermarkFlag` = `DAC_CR_WMF_MASK`,  
`kDAC12_NearlyEmptyFlag` = `DAC_CR_NEMPTF_MASK`,  
`kDAC12_FullFlag` = `DAC_CR_FULLF_MASK` }  
*DAC12 flags.*
- enum `_dac12_interrupt_enable` {
   
`kDAC12_UnderOrOverflowInterruptEnable` = `DAC_CR_UVIE_MASK`,  
`kDAC12_WatermarkInterruptEnable` = `DAC_CR_WTMIE_MASK`,  
`kDAC12_NearlyEmptyInterruptEnable` = `DAC_CR_EMPTIE_MASK`,  
`kDAC12_FullInterruptEnable` = `DAC_CR_FULLIE_MASK` }  
*DAC12 interrupts.*
- enum `dac12_fifo_size_info_t` {
   
`kDAC12_FIFOSize2` = 0U,  
`kDAC12_FIFOSize4` = 1U,  
`kDAC12_FIFOSize8` = 2U,  
`kDAC12_FIFOSize16` = 3U,  
`kDAC12_FIFOSize32` = 4U,  
`kDAC12_FIFOSize64` = 5U,  
`kDAC12_FIFOSize128` = 6U,  
`kDAC12_FIFOSize256` = 7U }  
*DAC12 FIFO size information provided by hardware.*
- enum `dac12_fifo_work_mode_t` {
   
`kDAC12_FIFODisabled` = 0U,  
`kDAC12_FIFOWorkAsNormalMode` = 1U,  
`kDAC12_FIFOWorkAsSwingMode` = 2U }  
*DAC12 FIFO work mode.*
- enum `dac12_reference_voltage_source_t` {
   
`kDAC12_ReferenceVoltageSourceAlt1` = 0U,  
`kDAC12_ReferenceVoltageSourceAlt2` = 1U }  
*DAC12 reference voltage source.*
- enum `dac12_fifo_trigger_mode_t` {
   
`kDAC12_FIFOTriggerByHardwareMode` = 0U,  
`kDAC12_FIFOTriggerBySoftwareMode` = 1U }  
*DAC12 FIFO trigger mode.*

- enum `dac12_reference_current_source_t` {
   
    `kDAC12_ReferenceCurrentSourceDisabled` = 0U,  
`kDAC12_ReferenceCurrentSourceAlt0` = 1U,  
`kDAC12_ReferenceCurrentSourceAlt1` = 2U,  
`kDAC12_ReferenceCurrentSourceAlt2` = 3U }
   
*DAC internal reference current source.*
- enum `dac12_speed_mode_t` {
   
    `kDAC12_SpeedLowMode` = 0U,  
`kDAC12_SpeedMiddleMode` = 1U,  
`kDAC12_SpeedHighMode` = 2U }
   
*DAC analog buffer speed mode for conversion.*

## Driver version

- #define `FSL_DAC12_DRIVER_VERSION` (`MAKE_VERSION`(2, 1, 0))
   
*DAC12 driver version 2.1.0.*

## Initialization and de-initialization

- void `DAC12_GetHardwareInfo` (`DAC_Type` \*base, `dac12_hardware_info_t` \*info)
   
*Get hardware information about this module.*
- void `DAC12_Init` (`DAC_Type` \*base, const `dac12_config_t` \*config)
   
*Initialize the DAC12 module.*
- void `DAC12_GetDefaultConfig` (`dac12_config_t` \*config)
   
*Initializes the DAC12 user configuration structure.*
- void `DAC12_Deinit` (`DAC_Type` \*base)
   
*De-initialize the DAC12 module.*
- static void `DAC12_Enable` (`DAC_Type` \*base, bool enable)
   
*Enable the DAC12's converter or not.*
- static void `DAC12_ResetConfig` (`DAC_Type` \*base)
   
*Reset all internal logic and registers.*
- static void `DAC12_ResetFIFO` (`DAC_Type` \*base)
   
*Reset the FIFO pointers.*

## Status

- static `uint32_t` `DAC12_GetStatusFlags` (`DAC_Type` \*base)
   
*Get status flags.*
- static void `DAC12_ClearStatusFlags` (`DAC_Type` \*base, `uint32_t` flags)
   
*Clear status flags.*

## Interrupts

- static void `DAC12_EnableInterrupts` (`DAC_Type` \*base, `uint32_t` mask)
   
*Enable interrupts.*
- static void `DAC12_DisableInterrupts` (`DAC_Type` \*base, `uint32_t` mask)
   
*Disable interrupts.*

## DMA control

- static void **DAC12\_EnableDMA** (DAC\_Type \*base, bool enable)  
*Enable DMA or not.*

## Functional feature

- static void **DAC12\_SetData** (DAC\_Type \*base, uint32\_t value)  
*Set data into the entry of FIFO buffer.*
- static void **DAC12\_DoSoftwareTrigger** (DAC\_Type \*base)  
*Do trigger the FIFO by software.*
- static uint32\_t **DAC12\_GetFIFOReadPointer** (DAC\_Type \*base)  
*Get the current read pointer of FIFO.*
- static uint32\_t **DAC12\_GetFIFOWritePointer** (DAC\_Type \*base)  
*Get the current write pointer of FIFO.*

## 14.3 Data Structure Documentation

### 14.3.1 struct dac12.hardware\_info\_t

#### Data Fields

- **dac12\_fifo\_size\_info\_t fifoSizeInfo**  
*The number of words in this device's DAC buffer.*

#### Field Documentation

(1) **dac12\_fifo\_size\_info\_t dac12.hardware\_info\_t::fifoSizeInfo**

### 14.3.2 struct dac12\_config\_t

Actually, the most fields are for FIFO buffer.

#### Data Fields

- **uint32\_t fifoWatermarkLevel**  
*FIFO's watermark, the max value can be the hardware FIFO size.*
- **dac12\_fifo\_work\_mode\_t fifoWorkMode**  
*FIFO's work mode about pointers.*
- **dac12\_reference\_voltage\_source\_t referenceVoltageSource**  
*Select the reference voltage source.*
- **dac12\_reference\_current\_source\_t referenceCurrentSource**  
*Select the trigger mode for FIFO.*
- **dac12\_speed\_mode\_t speedMode**  
*Select the speed mode for conversion.*
- **bool enableAnalogBuffer**  
*Enable analog buffer for high drive.*

**Field Documentation**

- (1) `uint32_t dac12_config_t::fifoWatermarkLevel`
- (2) `dac12_fifo_work_mode_t dac12_config_t::fifoWorkMode`
- (3) `dac12_reference_voltage_source_t dac12_config_t::referenceVoltageSource`
- (4) `dac12_reference_current_source_t dac12_config_t::referenceCurrentSource`

Select the reference current source.

- (5) `dac12_speed_mode_t dac12_config_t::speedMode`
- (6) `bool dac12_config_t::enableAnalogBuffer`

**14.4 Macro Definition Documentation**

**14.4.1 #define FSL\_DAC12\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 0))**

**14.4.2 #define DAC12\_CR\_W1C\_FLAGS\_MASK (DAC\_CR\_OVFF\_MASK | DAC\_CR\_UDFF\_MASK)**

**14.4.3 #define DAC12\_CR\_ALL\_FLAGS\_MASK (DAC12\_CR\_W1C\_FLAGS\_MASK | DAC\_CR\_WMF\_MASK | DAC\_CR\_NEMPTF\_MASK | DAC\_CR\_FULLF\_MASK)**

**14.5 Enumeration Type Documentation****14.5.1 enum \_dac12\_status\_flags**

Enumerator

***kDAC12\_OverflowFlag*** FIFO overflow status flag, which indicates that more data has been written into FIFO than it can hold.

***kDAC12\_UnderflowFlag*** FIFO underflow status flag, which means that there is a new trigger after the FIFO is nearly empty.

***kDAC12\_WatermarkFlag*** FIFO watermark status flag, which indicates the remaining FIFO data is less than the watermark setting.

***kDAC12\_NearlyEmptyFlag*** FIFO nearly empty flag, which means there is only one data remaining in FIFO.

***kDAC12\_FullFlag*** FIFO full status flag, which means that the FIFO read pointer equals the write pointer, as the write pointer increase.

### 14.5.2 enum \_dac12\_interrupt\_enable

Enumerator

***kDAC12\_UnderOrOverflowInterruptEnable*** Underflow and overflow interrupt enable.

***kDAC12\_WatermarkInterruptEnable*** Watermark interrupt enable.

***kDAC12\_NearlyEmptyInterruptEnable*** Nearly empty interrupt enable.

***kDAC12\_FullInterruptEnable*** Full interrupt enable.

### 14.5.3 enum dac12\_fifo\_size\_info\_t

Enumerator

***kDAC12\_FIFOSize2*** FIFO depth is 2.

***kDAC12\_FIFOSize4*** FIFO depth is 4.

***kDAC12\_FIFOSize8*** FIFO depth is 8.

***kDAC12\_FIFOSize16*** FIFO depth is 16.

***kDAC12\_FIFOSize32*** FIFO depth is 32.

***kDAC12\_FIFOSize64*** FIFO depth is 64.

***kDAC12\_FIFOSize128*** FIFO depth is 128.

***kDAC12\_FIFOSize256*** FIFO depth is 256.

### 14.5.4 enum dac12\_fifo\_work\_mode\_t

Enumerator

***kDAC12\_FIFODisabled*** FIFO disabled and only one level buffer is enabled. Any data written from this buffer goes to conversion.

***kDAC12\_FIFOWorkAsNormalMode*** Data will first read from FIFO to buffer then go to conversion.

***kDAC12\_FIFOWorkAsSwingMode*** In Swing mode, the FIFO must be set up to be full. In Swing back mode, a trigger changes the read pointer to make it swing between the FIFO Full and Nearly Empty state. That is, the trigger increases the read pointer till FIFO is nearly empty and decreases the read pointer till the FIFO is full.

### 14.5.5 enum dac12\_reference\_voltage\_source\_t

Enumerator

***kDAC12\_ReferenceVoltageSourceAlt1*** The DAC selects DACREF\_1 as the reference voltage.

***kDAC12\_ReferenceVoltageSourceAlt2*** The DAC selects DACREF\_2 as the reference voltage.

#### 14.5.6 enum dac12\_fifo\_trigger\_mode\_t

Enumerator

*kDAC12\_FIFOTriggerByHardwareMode* Buffer would be triggered by hardware.

*kDAC12\_FIFOTriggerBySoftwareMode* Buffer would be triggered by software.

#### 14.5.7 enum dac12\_reference\_current\_source\_t

Analog module needs reference current to keep working . Such reference current can generated by IP itself, or by on-chip PMC's "reference part". If no current reference be selected, analog module can't working normally ,even when other register can still be assigned, DAC would waste current but no function. To make the DAC work, either kDAC12\_ReferenceCurrentSourceAlt $x$  should be selected.

Enumerator

*kDAC12\_ReferenceCurrentSourceDisabled* None of reference current source is enabled.

*kDAC12\_ReferenceCurrentSourceAlt0* Use the internal reference current generated by the module itself.

*kDAC12\_ReferenceCurrentSourceAlt1* Use the ZTC(Zero Temperature Coefficient) reference current generated by on-chip power management module.

*kDAC12\_ReferenceCurrentSourceAlt2* Use the PTAT(Proportional To Absolution Temperature) reference current generated by power management module.

#### 14.5.8 enum dac12\_speed\_mode\_t

Enumerator

*kDAC12\_SpeedLowMode* Low speed mode.

*kDAC12\_SpeedMiddleMode* Middle speed mode.

*kDAC12\_SpeedHighMode* High speed mode.

### 14.6 Function Documentation

#### 14.6.1 void DAC12\_GetHardwareInfo ( DAC\_Type \* *base*, dac12\_hardware\_info\_t \* *info* )

Parameters

|             |                                                                           |
|-------------|---------------------------------------------------------------------------|
| <i>base</i> | DAC12 peripheral base address.                                            |
| <i>info</i> | Pointer to info structure, see to <a href="#">dac12_hardware_info_t</a> . |

#### 14.6.2 void DAC12\_Init ( DAC\_Type \* *base*, const dac12\_config\_t \* *config* )

Parameters

|               |                                                                             |
|---------------|-----------------------------------------------------------------------------|
| <i>base</i>   | DAC12 peripheral base address.                                              |
| <i>config</i> | Pointer to configuration structure, see to <a href="#">dac12_config_t</a> . |

#### 14.6.3 void DAC12\_GetDefaultConfig ( dac12\_config\_t \* *config* )

This function initializes the user configuration structure to a default value. The default values are:

```
* config->fifoWatermarkLevel = 0U;
* config->fifoWorkMode = kDAC12_FIFODisabled;
* config->referenceVoltageSource = kDAC12_ReferenceVoltageSourceAlt1;
* config->fifoTriggerMode = kDAC12_FIFOTriggerByHardwareMode;
* config->referenceCurrentSource = kDAC12_ReferenceCurrentSourceAlt0;
* config->speedMode = kDAC12_SpeedLowMode;
* config->speedMode = false;
* config->currentReferenceInternalTrimValue = 0x4;
*
```

Parameters

|               |                                                               |
|---------------|---------------------------------------------------------------|
| <i>config</i> | Pointer to the configuration structure. See "dac12_config_t". |
|---------------|---------------------------------------------------------------|

#### 14.6.4 void DAC12\_Deinit ( DAC\_Type \* *base* )

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | DAC12 peripheral base address. |
|-------------|--------------------------------|

#### 14.6.5 static void DAC12\_Enable ( DAC\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                      |
|---------------|--------------------------------------|
| <i>base</i>   | DAC12 peripheral base address.       |
| <i>enable</i> | Enable the DAC12's converter or not. |

#### 14.6.6 static void DAC12\_ResetConfig ( DAC\_Type \* *base* ) [inline], [static]

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | DAC12 peripheral base address. |
|-------------|--------------------------------|

#### 14.6.7 static void DAC12\_ResetFIFO ( DAC\_Type \* *base* ) [inline], [static]

FIFO pointers should only be reset when the DAC12 is disabled. This function can be used to configure both pointers to the same address to reset the FIFO as empty.

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | DAC12 peripheral base address. |
|-------------|--------------------------------|

#### 14.6.8 static uint32\_t DAC12\_GetStatusFlags ( DAC\_Type \* *base* ) [inline], [static]

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | DAC12 peripheral base address. |
|-------------|--------------------------------|

Returns

Mask of current status flags. See to [\\_dac12\\_status\\_flags](#).

#### 14.6.9 static void DAC12\_ClearStatusFlags ( DAC\_Type \* *base*, uint32\_t *flags* ) [inline], [static]

Note: Not all the flags can be cleared by this API. Several flags need special condition to clear them according to target chip's reference manual document.

Parameters

|              |                                                                                  |
|--------------|----------------------------------------------------------------------------------|
| <i>base</i>  | DAC12 peripheral base address.                                                   |
| <i>flags</i> | Mask of status flags to be cleared. See to <a href="#">_dac12_status_flags</a> . |

#### 14.6.10 static void DAC12\_EnableInterrupts ( **DAC\_Type** \* *base*, **uint32\_t** *mask* ) [**inline**], [**static**]

Parameters

|             |                                                                                          |
|-------------|------------------------------------------------------------------------------------------|
| <i>base</i> | DAC12 peripheral base address.                                                           |
| <i>mask</i> | Mask value of interrupts to be enabled. See to <a href="#">_dac12_interrupt_enable</a> . |

#### 14.6.11 static void DAC12\_DisableInterrupts ( **DAC\_Type** \* *base*, **uint32\_t** *mask* ) [**inline**], [**static**]

Parameters

|             |                                                                                           |
|-------------|-------------------------------------------------------------------------------------------|
| <i>base</i> | DAC12 peripheral base address.                                                            |
| <i>mask</i> | Mask value of interrupts to be disabled. See to <a href="#">_dac12_interrupt_enable</a> . |

#### 14.6.12 static void DAC12\_EnableDMA ( **DAC\_Type** \* *base*, **bool** *enable* ) [**inline**], [**static**]

When DMA is enabled, the DMA request will be generated by original interrupts. The interrupts will not be presented on this module at the same time.

#### 14.6.13 static void DAC12\_SetData ( **DAC\_Type** \* *base*, **uint32\_t** *value* ) [**inline**], [**static**]

When the DAC FIFO is disabled, and the one entry buffer is enabled, the DAC converts the data in the buffer to analog output voltage. Any write to the DATA register will replace the data in the buffer and push data to analog conversion without trigger support. When the DAC FIFO is enabled. Writing data would increase the write pointer of FIFO. Also, the data would be restored into the FIFO buffer.

Parameters

|              |                                 |
|--------------|---------------------------------|
| <i>base</i>  | DAC12 peripheral base address.  |
| <i>value</i> | Setting value into FIFO buffer. |

#### 14.6.14 static void DAC12\_DoSoftwareTrigger ( **DAC\_Type** \* *base* ) [inline], [static]

When the DAC FIFO is enabled, and software trigger is used. Doing trigger would increase the read pointer, and the data in the entry pointed by read pointer would be converted as new output.

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | DAC12 peripheral base address. |
|-------------|--------------------------------|

#### 14.6.15 static uint32\_t DAC12\_GetFIFOReadPointer ( **DAC\_Type** \* *base* ) [inline], [static]

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | DAC12 peripheral base address. |
|-------------|--------------------------------|

Returns

Read pointer index of FIFO buffer.

#### 14.6.16 static uint32\_t DAC12\_GetFIFOWritePointer ( **DAC\_Type** \* *base* ) [inline], [static]

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | DAC12 peripheral base address. |
|-------------|--------------------------------|

Returns

Write pointer index of FIFO buffer

# Chapter 15

## DMAMUX: Direct Memory Access Multiplexer Driver

### 15.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Direct Memory Access Multiplexer (DMAMUX) of MCUXpresso SDK devices.

### 15.2 Typical use case

#### 15.2.1 DMAMUX Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/dmamux

### Driver version

- #define `FSL_DMAMUX_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 5)`)  
*DMAMUX driver version 2.0.5.*

### DMAMUX Initialization and de-initialization

- void `DMAMUX_Init` (DMAMUX\_Type \*base)  
*Initializes the DMAMUX peripheral.*
- void `DMAMUX_Deinit` (DMAMUX\_Type \*base)  
*Deinitializes the DMAMUX peripheral.*

### DMAMUX Channel Operation

- static void `DMAMUX_EnableChannel` (DMAMUX\_Type \*base, uint32\_t channel)  
*Enables the DMAMUX channel.*
- static void `DMAMUX_DisableChannel` (DMAMUX\_Type \*base, uint32\_t channel)  
*Disables the DMAMUX channel.*
- static void `DMAMUX_SetSource` (DMAMUX\_Type \*base, uint32\_t channel, uint32\_t source)  
*Configures the DMAMUX channel source.*

### 15.3 Macro Definition Documentation

#### 15.3.1 #define `FSL_DMAMUX_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 5)`)

### 15.4 Function Documentation

#### 15.4.1 void `DMAMUX_Init` ( `DMAMUX_Type * base` )

This function ungates the DMAMUX clock.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | DMAMUX peripheral base address. |
|-------------|---------------------------------|

### 15.4.2 void DMAMUX\_Deinit ( DMAMUX\_Type \* *base* )

This function gates the DMAMUX clock.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | DMAMUX peripheral base address. |
|-------------|---------------------------------|

### 15.4.3 static void DMAMUX\_EnableChannel ( DMAMUX\_Type \* *base*, uint32\_t *channel* ) [inline], [static]

This function enables the DMAMUX channel.

Parameters

|                |                                 |
|----------------|---------------------------------|
| <i>base</i>    | DMAMUX peripheral base address. |
| <i>channel</i> | DMAMUX channel number.          |

### 15.4.4 static void DMAMUX\_DisableChannel ( DMAMUX\_Type \* *base*, uint32\_t *channel* ) [inline], [static]

This function disables the DMAMUX channel.

Note

The user must disable the DMAMUX channel before configuring it.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | DMAMUX peripheral base address. |
|-------------|---------------------------------|

|                |                        |
|----------------|------------------------|
| <i>channel</i> | DMAMUX channel number. |
|----------------|------------------------|

#### 15.4.5 static void DMAMUX\_SetSource ( **DMAMUX\_Type** \* *base*, **uint32\_t** *channel*, **uint32\_t** *source* ) [inline], [static]

Parameters

|                |                                                            |
|----------------|------------------------------------------------------------|
| <i>base</i>    | DMAMUX peripheral base address.                            |
| <i>channel</i> | DMAMUX channel number.                                     |
| <i>source</i>  | Channel source, which is used to trigger the DMA transfer. |

# Chapter 16

## eDMA: Enhanced Direct Memory Access (eDMA) Controller Driver

### 16.1 Overview

The MCUXpresso SDK provides a peripheral driver for the enhanced Direct Memory Access (eDMA) of MCUXpresso SDK devices.

### 16.2 Typical use case

#### 16.2.1 eDMA Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/edma

## Data Structures

- struct [edma\\_config\\_t](#)  
*eDMA global configuration structure.* [More...](#)
- struct [edma\\_transfer\\_config\\_t](#)  
*eDMA transfer configuration* [More...](#)
- struct [edma\\_channel\\_Preemption\\_config\\_t](#)  
*eDMA channel priority configuration* [More...](#)
- struct [edma\\_minor\\_offset\\_config\\_t](#)  
*eDMA minor offset configuration* [More...](#)
- struct [edma\\_tcd\\_t](#)  
*eDMA TCD.* [More...](#)
- struct [edma\\_handle\\_t](#)  
*eDMA transfer handle structure* [More...](#)

## Macros

- #define [DMA\\_DCHPRI\\_INDEX](#)(channel) (((channel) & ~0x03U) | (3U - ((channel)&0x03U)))  
*Compute the offset unit from DCHPRI3.*

## Typedefs

- typedef void(\* [edma\\_callback](#) )(struct \_edma\_handle \*handle, void \*userData, bool transferDone, uint32\_t tcds)  
*Define callback function for eDMA.*

## Enumerations

- enum `edma_transfer_size_t` {
   
    `kEDMA_TransferSize1Bytes` = 0x0U,
   
    `kEDMA_TransferSize2Bytes` = 0x1U,
   
    `kEDMA_TransferSize4Bytes` = 0x2U,
   
    `kEDMA_TransferSize8Bytes` = 0x3U,
   
    `kEDMA_TransferSize16Bytes` = 0x4U,
   
    `kEDMA_TransferSize32Bytes` = 0x5U }
   
    *eDMA transfer configuration*
- enum `edma_modulo_t` {
   
    `kEDMA_ModuloDisable` = 0x0U,
   
    `kEDMA_Modulo2bytes`,
   
    `kEDMA_Modulo4bytes`,
   
    `kEDMA_Modulo8bytes`,
   
    `kEDMA_Modulo16bytes`,
   
    `kEDMA_Modulo32bytes`,
   
    `kEDMA_Modulo64bytes`,
   
    `kEDMA_Modulo128bytes`,
   
    `kEDMA_Modulo256bytes`,
   
    `kEDMA_Modulo512bytes`,
   
    `kEDMA_Modulo1Kbytes`,
   
    `kEDMA_Modulo2Kbytes`,
   
    `kEDMA_Modulo4Kbytes`,
   
    `kEDMA_Modulo8Kbytes`,
   
    `kEDMA_Modulo16Kbytes`,
   
    `kEDMA_Modulo32Kbytes`,
   
    `kEDMA_Modulo64Kbytes`,
   
    `kEDMA_Modulo128Kbytes`,
   
    `kEDMA_Modulo256Kbytes`,
   
    `kEDMA_Modulo512Kbytes`,
   
    `kEDMA_Modulo1Mbytes`,
   
    `kEDMA_Modulo2Mbytes`,
   
    `kEDMA_Modulo4Mbytes`,
   
    `kEDMA_Modulo8Mbytes`,
   
    `kEDMA_Modulo16Mbytes`,
   
    `kEDMA_Modulo32Mbytes`,
   
    `kEDMA_Modulo64Mbytes`,
   
    `kEDMA_Modulo128Mbytes`,
   
    `kEDMA_Modulo256Mbytes`,
   
    `kEDMA_Modulo512Mbytes`,
   
    `kEDMA_Modulo1Gbytes`,
   
    `kEDMA_Modulo2Gbytes` }
   
    *eDMA modulo configuration*
- enum `edma_bandwidth_t` {

```

kEDMA_BandwidthStallNone = 0x0U,
kEDMA_BandwidthStall4Cycle = 0x2U,
kEDMA_BandwidthStall8Cycle = 0x3U }

Bandwidth control.
• enum edma_channel_link_type_t {
 kEDMA_LinkNone = 0x0U,
 kEDMA_MinorLink,
 kEDMA_MajorLink }

Channel link type.
• enum {
 kEDMA_DoneFlag = 0x1U,
 kEDMA_ErrorFlag = 0x2U,
 kEDMA_InterruptFlag = 0x4U }

_edma_channel_status_flags eDMA channel status flags.
• enum {
 kEDMA_DestinationBusErrorFlag = DMA_ES_DBE_MASK,
 kEDMA_SourceBusErrorFlag = DMA_ES_SBE_MASK,
 kEDMA_ScatterGatherErrorFlag = DMA_ES_SGE_MASK,
 kEDMA_NbytesErrorFlag = DMA_ES_NCE_MASK,
 kEDMA_DestinationOffsetErrorFlag = DMA_ES_DOE_MASK,
 kEDMA_DestinationAddressErrorFlag = DMA_ES_DAE_MASK,
 kEDMA_SourceOffsetErrorFlag = DMA_ES_SOE_MASK,
 kEDMA_SourceAddressErrorFlag = DMA_ES_SAE_MASK,
 kEDMA_ErrorChannelFlag = DMA_ES_ERRCHN_MASK,
 kEDMA_ChannelPriorityErrorFlag = DMA_ES_CPE_MASK,
 kEDMA_TransferCanceledFlag = DMA_ES_ECX_MASK,
 kEDMA_ValidFlag = (int)DMA_ES_VLD_MASK }

_edma_error_status_flags eDMA channel error status flags.
• enum edma_interrupt_enable_t {
 kEDMA_ErrorInterruptEnable = 0x1U,
 kEDMA_MajorInterruptEnable = DMA_CSR_INTMAJOR_MASK,
 kEDMA_HalfInterruptEnable = DMA_CSR_INTHALF_MASK }

eDMA interrupt source
• enum edma_transfer_type_t {
 kEDMA_MemoryToMemory = 0x0U,
 kEDMA_PeripheralToMemory,
 kEDMA_MemoryToPeripheral,
 kEDMA_PeripheralToPeripheral }

eDMA transfer type
• enum {
 kStatus_EDMA_QueueFull = MAKE_STATUS(kStatusGroup_EDMA, 0),
 kStatus_EDMA_Busy = MAKE_STATUS(kStatusGroup_EDMA, 1) }

_edma_transfer_status eDMA transfer status

```

## Driver version

- #define `FSL_EDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 4, 3)`)

*eDMA driver version*

## eDMA initialization and de-initialization

- void [EDMA\\_Init](#) (DMA\_Type \*base, const [edma\\_config\\_t](#) \*config)  
*Initializes the eDMA peripheral.*
- void [EDMA\\_Deinit](#) (DMA\_Type \*base)  
*Deinitializes the eDMA peripheral.*
- void [EDMA\\_InstallTCD](#) (DMA\_Type \*base, uint32\_t channel, [edma\\_tcd\\_t](#) \*tcd)  
*Push content of TCD structure into hardware TCD register.*
- void [EDMA\\_GetDefaultConfig](#) ([edma\\_config\\_t](#) \*config)  
*Gets the eDMA default configuration structure.*
- static void [EDMA\\_EnableContinuousChannelLinkMode](#) (DMA\_Type \*base, bool enable)  
*Enable/Disable continuous channel link mode.*
- static void [EDMA\\_EnableMinorLoopMapping](#) (DMA\_Type \*base, bool enable)  
*Enable/Disable minor loop mapping.*

## eDMA Channel Operation

- void [EDMA\\_ResetChannel](#) (DMA\_Type \*base, uint32\_t channel)  
*Sets all TCD registers to default values.*
- void [EDMA\\_SetTransferConfig](#) (DMA\_Type \*base, uint32\_t channel, const [edma\\_transfer\\_config\\_t](#) \*config, [edma\\_tcd\\_t](#) \*nextTcd)  
*Configures the eDMA transfer attribute.*
- void [EDMA\\_SetMinorOffsetConfig](#) (DMA\_Type \*base, uint32\_t channel, const [edma\\_minor\\_offset\\_config\\_t](#) \*config)  
*Configures the eDMA minor offset feature.*
- void [EDMA\\_SetChannelPreemptionConfig](#) (DMA\_Type \*base, uint32\_t channel, const [edma\\_channel\\_Preemption\\_config\\_t](#) \*config)  
*Configures the eDMA channel preemption feature.*
- void [EDMA\\_SetChannelLink](#) (DMA\_Type \*base, uint32\_t channel, [edma\\_channel\\_link\\_type\\_t](#) type, uint32\_t linkedChannel)  
*Sets the channel link for the eDMA transfer.*
- void [EDMA\\_SetBandWidth](#) (DMA\_Type \*base, uint32\_t channel, [edma\\_bandwidth\\_t](#) bandWidth)  
*Sets the bandwidth for the eDMA transfer.*
- void [EDMA\\_SetModulo](#) (DMA\_Type \*base, uint32\_t channel, [edma\\_modulo\\_t](#) srcModulo, [edma\\_modulo\\_t](#) destModulo)  
*Sets the source modulo and the destination modulo for the eDMA transfer.*
- static void [EDMA\\_EnableAsyncRequest](#) (DMA\_Type \*base, uint32\_t channel, bool enable)  
*Enables an async request for the eDMA transfer.*
- static void [EDMA\\_EnableAutoStopRequest](#) (DMA\_Type \*base, uint32\_t channel, bool enable)  
*Enables an auto stop request for the eDMA transfer.*
- void [EDMA\\_EnableChannelInterrupts](#) (DMA\_Type \*base, uint32\_t channel, uint32\_t mask)  
*Enables the interrupt source for the eDMA transfer.*
- void [EDMA\\_DisableChannelInterrupts](#) (DMA\_Type \*base, uint32\_t channel, uint32\_t mask)  
*Disables the interrupt source for the eDMA transfer.*
- void [EDMA\\_SetMajorOffsetConfig](#) (DMA\_Type \*base, uint32\_t channel, int32\_t sourceOffset, int32\_t destOffset)  
*Configures the eDMA channel TCD major offset feature.*

## eDMA TCD Operation

- void [EDMA\\_TcdReset](#) (edma\_tcd\_t \*tcd)  
*Sets all fields to default values for the TCD structure.*
- void [EDMA\\_TcdSetTransferConfig](#) (edma\_tcd\_t \*tcd, const edma\_transfer\_config\_t \*config, edma\_tcd\_t \*nextTcd)  
*Configures the eDMA TCD transfer attribute.*
- void [EDMA\\_TcdSetMinorOffsetConfig](#) (edma\_tcd\_t \*tcd, const edma\_minor\_offset\_config\_t \*config)  
*Configures the eDMA TCD minor offset feature.*
- void [EDMA\\_TcdSetChannelLink](#) (edma\_tcd\_t \*tcd, edma\_channel\_link\_type\_t type, uint32\_t linkedChannel)  
*Sets the channel link for the eDMA TCD.*
- static void [EDMA\\_TcdSetBandWidth](#) (edma\_tcd\_t \*tcd, edma\_bandwidth\_t bandWidth)  
*Sets the bandwidth for the eDMA TCD.*
- void [EDMA\\_TcdSetModulo](#) (edma\_tcd\_t \*tcd, edma\_modulo\_t srcModulo, edma\_modulo\_t destModulo)  
*Sets the source modulo and the destination modulo for the eDMA TCD.*
- static void [EDMA\\_TcdEnableAutoStopRequest](#) (edma\_tcd\_t \*tcd, bool enable)  
*Sets the auto stop request for the eDMA TCD.*
- void [EDMA\\_TcdEnableInterrupts](#) (edma\_tcd\_t \*tcd, uint32\_t mask)  
*Enables the interrupt source for the eDMA TCD.*
- void [EDMA\\_TcdDisableInterrupts](#) (edma\_tcd\_t \*tcd, uint32\_t mask)  
*Disables the interrupt source for the eDMA TCD.*
- void [EDMA\\_TcdSetMajorOffsetConfig](#) (edma\_tcd\_t \*tcd, int32\_t sourceOffset, int32\_t destOffset)  
*Configures the eDMA TCD major offset feature.*

## eDMA Channel Transfer Operation

- static void [EDMA\\_EnableChannelRequest](#) (DMA\_Type \*base, uint32\_t channel)  
*Enables the eDMA hardware channel request.*
- static void [EDMA\\_DisableChannelRequest](#) (DMA\_Type \*base, uint32\_t channel)  
*Disables the eDMA hardware channel request.*
- static void [EDMA\\_TriggerChannelStart](#) (DMA\_Type \*base, uint32\_t channel)  
*Starts the eDMA transfer by using the software trigger.*

## eDMA Channel Status Operation

- uint32\_t [EDMA\\_GetRemainingMajorLoopCount](#) (DMA\_Type \*base, uint32\_t channel)  
*Gets the remaining major loop count from the eDMA current channel TCD.*
- static uint32\_t [EDMA\\_GetErrorStatusFlags](#) (DMA\_Type \*base)  
*Gets the eDMA channel error status flags.*
- uint32\_t [EDMA\\_GetChannelStatusFlags](#) (DMA\_Type \*base, uint32\_t channel)  
*Gets the eDMA channel status flags.*
- void [EDMA\\_ClearChannelStatusFlags](#) (DMA\_Type \*base, uint32\_t channel, uint32\_t mask)  
*Clears the eDMA channel status flags.*

## eDMA Transactional Operation

- void [EDMA\\_CreateHandle](#) (edma\_handle\_t \*handle, DMA\_Type \*base, uint32\_t channel)  
*Creates the eDMA handle.*

- void **EDMA\_InstallTCDMemory** (**edma\_handle\_t** \*handle, **edma\_tcd\_t** \*tcdPool, **uint32\_t** tcdSize)
 

*Installs the TCDs memory pool into the eDMA handle.*
- void **EDMA\_SetCallback** (**edma\_handle\_t** \*handle, **edma\_callback** callback, void \*userData)
 

*Installs a callback function for the eDMA transfer.*
- void **EDMA\_PrepTransferConfig** (**edma\_transfer\_config\_t** \*config, void \*srcAddr, **uint32\_t** srcWidth, **int16\_t** srcOffset, void \*destAddr, **uint32\_t** destWidth, **int16\_t** destOffset, **uint32\_t** bytesEachRequest, **uint32\_t** transferBytes)
 

*Prepares the eDMA transfer structure configurations.*
- void **EDMA\_PrepTransfer** (**edma\_transfer\_config\_t** \*config, void \*srcAddr, **uint32\_t** srcWidth, void \*destAddr, **uint32\_t** destWidth, **uint32\_t** bytesEachRequest, **uint32\_t** transferBytes, **edma\_transfer\_type\_t** type)
 

*Prepares the eDMA transfer structure.*
- **status\_t EDMA\_SubmitTransfer** (**edma\_handle\_t** \*handle, const **edma\_transfer\_config\_t** \*config)
 

*Submits the eDMA transfer request.*
- void **EDMA\_StartTransfer** (**edma\_handle\_t** \*handle)
 

*eDMA starts transfer.*
- void **EDMA\_StopTransfer** (**edma\_handle\_t** \*handle)
 

*eDMA stops transfer.*
- void **EDMA\_AbortTransfer** (**edma\_handle\_t** \*handle)
 

*eDMA aborts transfer.*
- static **uint32\_t EDMA\_GetUnusedTCDNumber** (**edma\_handle\_t** \*handle)
 

*Get unused TCD slot number.*
- static **uint32\_t EDMA\_GetNextTCDAddress** (**edma\_handle\_t** \*handle)
 

*Get the next tcd address.*
- void **EDMA\_HandleIRQ** (**edma\_handle\_t** \*handle)
 

*eDMA IRQ handler for the current major loop transfer completion.*

## 16.3 Data Structure Documentation

### 16.3.1 struct edma\_config\_t

#### Data Fields

- bool **enableContinuousLinkMode**

*Enable (true) continuous link mode.*
- bool **enableHaltOnError**

*Enable (true) transfer halt on error.*
- bool **enableRoundRobinArbitration**

*Enable (true) round robin channel arbitration method or fixed priority arbitration is used for channel selection.*
- bool **enableDebugMode**

*Enable(true) eDMA debug mode.*

#### Field Documentation

##### (1) bool **edma\_config\_t::enableContinuousLinkMode**

Upon minor loop completion, the channel activates again if that channel has a minor loop channel link enabled and the link channel is itself.

**(2) bool edma\_config\_t::enableHaltOnError**

Any error causes the HALT bit to set. Subsequently, all service requests are ignored until the HALT bit is cleared.

**(3) bool edma\_config\_t::enableDebugMode**

When in debug mode, the eDMA stalls the start of a new channel. Executing channels are allowed to complete.

**16.3.2 struct edma\_transfer\_config\_t**

This structure configures the source/destination transfer attribute.

**Data Fields**

- **uint32\_t srcAddr**  
*Source data address.*
- **uint32\_t destAddr**  
*Destination data address.*
- **edma\_transfer\_size\_t srcTransferSize**  
*Source data transfer size.*
- **edma\_transfer\_size\_t destTransferSize**  
*Destination data transfer size.*
- **int16\_t srcOffset**  
*Sign-extended offset applied to the current source address to form the next-state value as each source read is completed.*
- **int16\_t destOffset**  
*Sign-extended offset applied to the current destination address to form the next-state value as each destination write is completed.*
- **uint32\_t minorLoopBytes**  
*Bytes to transfer in a minor loop.*
- **uint32\_t majorLoopCounts**  
*Major loop iteration count.*

**Field Documentation****(1) uint32\_t edma\_transfer\_config\_t::srcAddr****(2) uint32\_t edma\_transfer\_config\_t::destAddr****(3) edma\_transfer\_size\_t edma\_transfer\_config\_t::srcTransferSize****(4) edma\_transfer\_size\_t edma\_transfer\_config\_t::destTransferSize****(5) int16\_t edma\_transfer\_config\_t::srcOffset**

- (6) int16\_t edma\_transfer\_config\_t::destOffset
- (7) uint32\_t edma\_transfer\_config\_t::majorLoopCounts

### 16.3.3 struct edma\_channel\_Preemption\_config\_t

#### Data Fields

- bool enableChannelPreemption  
*If true: a channel can be suspended by other channel with higher priority.*
- bool enablePreemptAbility  
*If true: a channel can suspend other channel with low priority.*
- uint8\_t channelPriority  
*Channel priority.*

### 16.3.4 struct edma\_minor\_offset\_config\_t

#### Data Fields

- bool enableSrcMinorOffset  
*Enable(true) or Disable(false) source minor loop offset.*
- bool enableDestMinorOffset  
*Enable(true) or Disable(false) destination minor loop offset.*
- uint32\_t minorOffset  
*Offset for a minor loop mapping.*

#### Field Documentation

- (1) bool edma\_minor\_offset\_config\_t::enableSrcMinorOffset
- (2) bool edma\_minor\_offset\_config\_t::enableDestMinorOffset
- (3) uint32\_t edma\_minor\_offset\_config\_t::minorOffset

### 16.3.5 struct edma\_tcd\_t

This structure is same as TCD register which is described in reference manual, and is used to configure the scatter/gather feature as a next hardware TCD.

#### Data Fields

- \_\_IO uint32\_t SADDR  
*SADDR register, used to save source address.*
- \_\_IO uint16\_t SOFF  
*SOFF register, save offset bytes every transfer.*
- \_\_IO uint16\_t ATTR

- **ATTR register; source/destination transfer size and modulo.**
- **\_IO uint32\_t NBYTES**  
*Nbytes register, minor loop length in bytes.*
- **\_IO uint32\_t SLAST**  
*SLAST register.*
- **\_IO uint32\_t DADDR**  
*DADDR register, used for destination address.*
- **\_IO uint16\_t DOFF**  
*DOFF register, used for destination offset.*
- **\_IO uint16\_t CITER**  
*CITER register, current minor loop numbers, for unfinished minor loop.*
- **\_IO uint32\_t DLAST\_SGA**  
*DLASTSGA register, next tcd address used in scatter-gather mode.*
- **\_IO uint16\_t CSR**  
*CSR register, for TCD control status.*
- **\_IO uint16\_t BITER**  
*BITER register, begin minor loop count.*

## Field Documentation

(1) **\_IO uint16\_t edma\_tcd\_t::CITER**

(2) **\_IO uint16\_t edma\_tcd\_t::BITER**

## 16.3.6 struct edma\_handle\_t

### Data Fields

- **edma\_callback callback**  
*Callback function for major count exhausted.*
- **void \* userData**  
*Callback function parameter.*
- **DMA\_Type \* base**  
*eDMA peripheral base address.*
- **edma\_tcd\_t \* tcdPool**  
*Pointer to memory stored TCDs.*
- **uint8\_t channel**  
*eDMA channel number.*
- **volatile int8\_t header**  
*The first TCD index.*
- **volatile int8\_t tail**  
*The last TCD index.*
- **volatile int8\_t tcdUsed**  
*The number of used TCD slots.*
- **volatile int8\_t tcdSize**  
*The total number of TCD slots in the queue.*
- **uint8\_t flags**  
*The status of the current channel.*

## Field Documentation

- (1) `edma_callback edma_handle_t::callback`
- (2) `void* edma_handle_t::userData`
- (3) `DMA_Type* edma_handle_t::base`
- (4) `edma_tcd_t* edma_handle_t::tcdPool`
- (5) `uint8_t edma_handle_t::channel`
- (6) `volatile int8_t edma_handle_t::header`

Should point to the next TCD to be loaded into the eDMA engine.

- (7) `volatile int8_t edma_handle_t::tail`

Should point to the next TCD to be stored into the memory pool.

- (8) `volatile int8_t edma_handle_t::tcdUsed`

Should reflect the number of TCDs can be used/loaded in the memory.

- (9) `volatile int8_t edma_handle_t::tcdSize`

- (10) `uint8_t edma_handle_t::flags`

## 16.4 Macro Definition Documentation

### 16.4.1 `#define FSL_EDMA_DRIVER_VERSION (MAKE_VERSION(2, 4, 3))`

Version 2.4.3.

## 16.5 Typedef Documentation

### 16.5.1 `typedef void(* edma_callback)(struct _edma_handle *handle, void *userData, bool transferDone, uint32_t tclds)`

This callback function is called in the EDMA interrupt handle. In normal mode, run into callback function means the transfer users need is done. In scatter gather mode, run into callback function means a transfer control block (tcd) is finished. Not all transfer finished, users can get the finished tcd numbers using interface EDMA\_GetUnusedTCDNumber.

Parameters

---

|                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>handle</i>       | EDMA handle pointer, users shall not touch the values inside.                                                                                                                                                                                                                                                                                                                                                                                    |
| <i>userData</i>     | The callback user parameter pointer. Users can use this parameter to involve things users need to change in EDMA callback function.                                                                                                                                                                                                                                                                                                              |
| <i>transferDone</i> | If the current loaded transfer done. In normal mode it means if all transfer done. In scatter gather mode, this parameter shows is the current transfer block in EDM-A register is done. As the load of core is different, it will be different if the new tcd loaded into EDMA registers while this callback called. If true, it always means new tcd still not loaded into registers, while false means new tcd already loaded into registers. |
| <i>tcds</i>         | How many tcds are done from the last callback. This parameter only used in scatter gather mode. It tells user how many tcds are finished between the last callback and this.                                                                                                                                                                                                                                                                     |

## 16.6 Enumeration Type Documentation

### 16.6.1 enum edma\_transfer\_size\_t

Enumerator

- kEDMA\_TransferSize1Bytes*** Source/Destination data transfer size is 1 byte every time.
- kEDMA\_TransferSize2Bytes*** Source/Destination data transfer size is 2 bytes every time.
- kEDMA\_TransferSize4Bytes*** Source/Destination data transfer size is 4 bytes every time.
- kEDMA\_TransferSize8Bytes*** Source/Destination data transfer size is 8 bytes every time.
- kEDMA\_TransferSize16Bytes*** Source/Destination data transfer size is 16 bytes every time.
- kEDMA\_TransferSize32Bytes*** Source/Destination data transfer size is 32 bytes every time.

### 16.6.2 enum edma\_modulo\_t

Enumerator

- kEDMA\_ModuloDisable*** Disable modulo.
- kEDMA\_Modulo2bytes*** Circular buffer size is 2 bytes.
- kEDMA\_Modulo4bytes*** Circular buffer size is 4 bytes.
- kEDMA\_Modulo8bytes*** Circular buffer size is 8 bytes.
- kEDMA\_Modulo16bytes*** Circular buffer size is 16 bytes.
- kEDMA\_Modulo32bytes*** Circular buffer size is 32 bytes.
- kEDMA\_Modulo64bytes*** Circular buffer size is 64 bytes.
- kEDMA\_Modulo128bytes*** Circular buffer size is 128 bytes.
- kEDMA\_Modulo256bytes*** Circular buffer size is 256 bytes.
- kEDMA\_Modulo512bytes*** Circular buffer size is 512 bytes.
- kEDMA\_Modulo1Kbytes*** Circular buffer size is 1 K bytes.
- kEDMA\_Modulo2Kbytes*** Circular buffer size is 2 K bytes.
- kEDMA\_Modulo4Kbytes*** Circular buffer size is 4 K bytes.

***kEDMA\_Modulo8Kbytes*** Circular buffer size is 8 K bytes.  
***kEDMA\_Modulo16Kbytes*** Circular buffer size is 16 K bytes.  
***kEDMA\_Modulo32Kbytes*** Circular buffer size is 32 K bytes.  
***kEDMA\_Modulo64Kbytes*** Circular buffer size is 64 K bytes.  
***kEDMA\_Modulo128Kbytes*** Circular buffer size is 128 K bytes.  
***kEDMA\_Modulo256Kbytes*** Circular buffer size is 256 K bytes.  
***kEDMA\_Modulo512Kbytes*** Circular buffer size is 512 K bytes.  
***kEDMA\_Modulo1Mbytes*** Circular buffer size is 1 M bytes.  
***kEDMA\_Modulo2Mbytes*** Circular buffer size is 2 M bytes.  
***kEDMA\_Modulo4Mbytes*** Circular buffer size is 4 M bytes.  
***kEDMA\_Modulo8Mbytes*** Circular buffer size is 8 M bytes.  
***kEDMA\_Modulo16Mbytes*** Circular buffer size is 16 M bytes.  
***kEDMA\_Modulo32Mbytes*** Circular buffer size is 32 M bytes.  
***kEDMA\_Modulo64Mbytes*** Circular buffer size is 64 M bytes.  
***kEDMA\_Modulo128Mbytes*** Circular buffer size is 128 M bytes.  
***kEDMA\_Modulo256Mbytes*** Circular buffer size is 256 M bytes.  
***kEDMA\_Modulo512Mbytes*** Circular buffer size is 512 M bytes.  
***kEDMA\_Modulo1Gbytes*** Circular buffer size is 1 G bytes.  
***kEDMA\_Modulo2Gbytes*** Circular buffer size is 2 G bytes.

### 16.6.3 enum edma\_bandwidth\_t

Enumerator

***kEDMA\_BandwidthStallNone*** No eDMA engine stalls.  
***kEDMA\_BandwidthStall4Cycle*** eDMA engine stalls for 4 cycles after each read/write.  
***kEDMA\_BandwidthStall8Cycle*** eDMA engine stalls for 8 cycles after each read/write.

### 16.6.4 enum edma\_channel\_link\_type\_t

Enumerator

***kEDMA\_LinkNone*** No channel link.  
***kEDMA\_MinorLink*** Channel link after each minor loop.  
***kEDMA\_MajorLink*** Channel link while major loop count exhausted.

### 16.6.5 anonymous enum

Enumerator

***kEDMA\_DoneFlag*** DONE flag, set while transfer finished, CITER value exhausted.  
***kEDMA\_ErrorFlag*** eDMA error flag, an error occurred in a transfer  
***kEDMA\_InterruptFlag*** eDMA interrupt flag, set while an interrupt occurred of this channel

### 16.6.6 anonymous enum

Enumerator

- kEDMA\_DestinationBusErrorFlag* Bus error on destination address.
- kEDMA\_SourceBusErrorFlag* Bus error on the source address.
- kEDMA\_ScatterGatherErrorFlag* Error on the Scatter/Gather address, not 32byte aligned.
- kEDMA\_NbytesErrorFlag* NBYTES/CITER configuration error.
- kEDMA\_DestinationOffsetErrorFlag* Destination offset not aligned with destination size.
- kEDMA\_DestinationAddressErrorFlag* Destination address not aligned with destination size.
- kEDMA\_SourceOffsetErrorFlag* Source offset not aligned with source size.
- kEDMA\_SourceAddressErrorFlag* Source address not aligned with source size.
- kEDMA\_ErrorChannelFlag* Error channel number of the cancelled channel number.
- kEDMA\_ChannelPriorityErrorFlag* Channel priority is not unique.
- kEDMA\_TransferCanceledFlag* Transfer cancelled.
- kEDMA\_ValidFlag* No error occurred, this bit is 0. Otherwise, it is 1.

### 16.6.7 enum edma\_interrupt\_enable\_t

Enumerator

- kEDMA\_ErrorInterruptEnable* Enable interrupt while channel error occurs.
- kEDMA\_MajorInterruptEnable* Enable interrupt while major count exhausted.
- kEDMA\_HalfInterruptEnable* Enable interrupt while major count to half value.

### 16.6.8 enum edma\_transfer\_type\_t

Enumerator

- kEDMA\_MemoryToMemory* Transfer from memory to memory.
- kEDMA\_PeripheralToMemory* Transfer from peripheral to memory.
- kEDMA\_MemoryToPeripheral* Transfer from memory to peripheral.
- kEDMA\_PeripheralToPeripheral* Transfer from Peripheral to peripheral.

### 16.6.9 anonymous enum

Enumerator

- kStatus\_EDMA\_QueueFull* TCD queue is full.
- kStatus\_EDMA\_Busy* Channel is busy and can't handle the transfer request.

## 16.7 Function Documentation

### 16.7.1 void EDMA\_Init ( DMA\_Type \* *base*, const edma\_config\_t \* *config* )

This function ungates the eDMA clock and configures the eDMA peripheral according to the configuration structure.

Parameters

|               |                                                                |
|---------------|----------------------------------------------------------------|
| <i>base</i>   | eDMA peripheral base address.                                  |
| <i>config</i> | A pointer to the configuration structure, see "edma_config_t". |

Note

This function enables the minor loop map feature.

### 16.7.2 void EDMA\_Deinit ( DMA\_Type \* *base* )

This function gates the eDMA clock.

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | eDMA peripheral base address. |
|-------------|-------------------------------|

### 16.7.3 void EDMA\_InstallTCD ( DMA\_Type \* *base*, uint32\_t *channel*, edma\_tcd\_t \* *tcd* )

Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | EDMA peripheral base address. |
| <i>channel</i> | EDMA channel number.          |
| <i>tcd</i>     | Point to TCD structure.       |

### 16.7.4 void EDMA\_GetDefaultConfig ( edma\_config\_t \* *config* )

This function sets the configuration structure to default values. The default configuration is set to the following values.

```
* config.enableContinuousLinkMode = false;
* config.enableHaltOnError = true;
* config.enableRoundRobinArbitration = false;
* config.enableDebugMode = false;
*
```

Parameters

|               |                                                |
|---------------|------------------------------------------------|
| <i>config</i> | A pointer to the eDMA configuration structure. |
|---------------|------------------------------------------------|

### 16.7.5 static void EDMA\_EnableContinuousChannelLinkMode ( DMA\_Type \* *base*, bool *enable* ) [inline], [static]

Note

Do not use continuous link mode with a channel linking to itself if there is only one minor loop iteration per service request, for example, if the channel's NBYTES value is the same as either the source or destination size. The same data transfer profile can be achieved by simply increasing the NBYTES value, which provides more efficient, faster processing.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | EDMA peripheral base address.     |
| <i>enable</i> | true is enable, false is disable. |

### 16.7.6 static void EDMA\_EnableMinorLoopMapping ( DMA\_Type \* *base*, bool *enable* ) [inline], [static]

The TCDn.word2 is redefined to include individual enable fields, an offset field, and the NBYTES field.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | EDMA peripheral base address.     |
| <i>enable</i> | true is enable, false is disable. |

### 16.7.7 void EDMA\_ResetChannel ( DMA\_Type \* *base*, uint32\_t *channel* )

This function sets TCD registers for this channel to default values.

Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | eDMA peripheral base address. |
| <i>channel</i> | eDMA channel number.          |

## Note

This function must not be called while the channel transfer is ongoing or it causes unpredictable results.

This function enables the auto stop request feature.

### 16.7.8 void EDMA\_SetTransferConfig ( DMA\_Type \* *base*, uint32\_t *channel*, const edma\_transfer\_config\_t \* *config*, edma\_tcd\_t \* *nextTcd* )

This function configures the transfer attribute, including source address, destination address, transfer size, address offset, and so on. It also configures the scatter gather feature if the user supplies the TCD address. Example:

```
* edma_transfer_t config;
* edma_tcd_t tcd;
* config.srcAddr = ...;
* config.destAddr = ...;
* ...
* EDMA_SetTransferConfig(DMA0, channel, &config, &tcd);
*
```

## Parameters

|                |                                                                                               |
|----------------|-----------------------------------------------------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                                                                 |
| <i>channel</i> | eDMA channel number.                                                                          |
| <i>config</i>  | Pointer to eDMA transfer configuration structure.                                             |
| <i>nextTcd</i> | Point to TCD structure. It can be NULL if users do not want to enable scatter/gather feature. |

## Note

If nextTcd is not NULL, it means scatter gather feature is enabled and DREQ bit is cleared in the previous transfer configuration, which is set in the eDMA\_ResetChannel.

### 16.7.9 void EDMA\_SetMinorOffsetConfig ( DMA\_Type \* *base*, uint32\_t *channel*, const edma\_minor\_offset\_config\_t \* *config* )

The minor offset means that the signed-extended value is added to the source address or destination address after each minor loop.

Parameters

|                |                                                        |
|----------------|--------------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                          |
| <i>channel</i> | eDMA channel number.                                   |
| <i>config</i>  | A pointer to the minor offset configuration structure. |

### **16.7.10 void EDMA\_SetChannelPreemptionConfig ( DMA\_Type \* *base*, uint32\_t *channel*, const edma\_channel\_Preemption\_config\_t \* *config* )**

This function configures the channel preemption attribute and the priority of the channel.

Parameters

|                |                                                              |
|----------------|--------------------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                                |
| <i>channel</i> | eDMA channel number                                          |
| <i>config</i>  | A pointer to the channel preemption configuration structure. |

### **16.7.11 void EDMA\_SetChannelLink ( DMA\_Type \* *base*, uint32\_t *channel*, edma\_channel\_link\_type\_t *type*, uint32\_t *linkedChannel* )**

This function configures either the minor link or the major link mode. The minor link means that the channel link is triggered every time CITER decreases by 1. The major link means that the channel link is triggered when the CITER is exhausted.

Parameters

|                |                                                                                                                                                                              |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                                                                                                                                                |
| <i>channel</i> | eDMA channel number.                                                                                                                                                         |
| <i>type</i>    | A channel link type, which can be one of the following: <ul style="list-style-type: none"><li>• kEDMA_LinkNone</li><li>• kEDMA_MinorLink</li><li>• kEDMA_MajorLink</li></ul> |

|                      |                            |
|----------------------|----------------------------|
| <i>linkedChannel</i> | The linked channel number. |
|----------------------|----------------------------|

## Note

Users should ensure that DONE flag is cleared before calling this interface, or the configuration is invalid.

### 16.7.12 void EDMA\_SetBandWidth ( DMA\_Type \* *base*, uint32\_t *channel*, edma\_bandwidth\_t *bandWidth* )

Because the eDMA processes the minor loop, it continuously generates read/write sequences until the minor count is exhausted. The bandwidth forces the eDMA to stall after the completion of each read/write access to control the bus request bandwidth seen by the crossbar switch.

## Parameters

|                  |                                                                                                                                                                                                               |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>      | eDMA peripheral base address.                                                                                                                                                                                 |
| <i>channel</i>   | eDMA channel number.                                                                                                                                                                                          |
| <i>bandWidth</i> | A bandwidth setting, which can be one of the following: <ul style="list-style-type: none"> <li>• kEDMABandwidthStallNone</li> <li>• kEDMABandwidthStall4Cycle</li> <li>• kEDMABandwidthStall8Cycle</li> </ul> |

### 16.7.13 void EDMA\_SetModulo ( DMA\_Type \* *base*, uint32\_t *channel*, edma\_modulo\_t *srcModulo*, edma\_modulo\_t *destModulo* )

This function defines a specific address range specified to be the value after (SADDR + SOFF)/(DADDR + DOFF) calculation is performed or the original register value. It provides the ability to implement a circular data queue easily.

## Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | eDMA peripheral base address. |
| <i>channel</i> | eDMA channel number.          |

|                   |                             |
|-------------------|-----------------------------|
| <i>srcModulo</i>  | A source modulo value.      |
| <i>destModulo</i> | A destination modulo value. |

**16.7.14 static void EDMA\_EnableAsyncRequest ( DMA\_Type \* *base*, uint32\_t *channel*, bool *enable* ) [inline], [static]**

Parameters

|                |                                                  |
|----------------|--------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                    |
| <i>channel</i> | eDMA channel number.                             |
| <i>enable</i>  | The command to enable (true) or disable (false). |

**16.7.15 static void EDMA\_EnableAutoStopRequest ( DMA\_Type \* *base*, uint32\_t *channel*, bool *enable* ) [inline], [static]**

If enabling the auto stop request, the eDMA hardware automatically disables the hardware channel request.

Parameters

|                |                                                  |
|----------------|--------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                    |
| <i>channel</i> | eDMA channel number.                             |
| <i>enable</i>  | The command to enable (true) or disable (false). |

**16.7.16 void EDMA\_EnableChannelInterrupts ( DMA\_Type \* *base*, uint32\_t *channel*, uint32\_t *mask* )**

Parameters

|                |                                                                                                     |
|----------------|-----------------------------------------------------------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                                                                       |
| <i>channel</i> | eDMA channel number.                                                                                |
| <i>mask</i>    | The mask of interrupt source to be set. Users need to use the defined edma_interrupt_enable_t type. |

**16.7.17 void EDMA\_DisableChannelInterrupts ( DMA\_Type \* *base*, uint32\_t *channel*, uint32\_t *mask* )**

Parameters

|                |                                                                                           |
|----------------|-------------------------------------------------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                                                             |
| <i>channel</i> | eDMA channel number.                                                                      |
| <i>mask</i>    | The mask of the interrupt source to be set. Use the defined edma_interrupt_enable_t type. |

### 16.7.18 void EDMA\_SetMajorOffsetConfig ( DMA\_Type \* *base*, uint32\_t *channel*, int32\_t *sourceOffset*, int32\_t *destOffset* )

Adjustment value added to the source address at the completion of the major iteration count

Parameters

|                     |                                                                                     |
|---------------------|-------------------------------------------------------------------------------------|
| <i>base</i>         | eDMA peripheral base address.                                                       |
| <i>channel</i>      | edma channel number.                                                                |
| <i>sourceOffset</i> | source address offset will be applied to source address after major loop done.      |
| <i>destOffset</i>   | destination address offset will be applied to source address after major loop done. |

### 16.7.19 void EDMA\_TcdReset ( edma\_tcd\_t \* *tcd* )

This function sets all fields for this TCD structure to default value.

Parameters

|            |                               |
|------------|-------------------------------|
| <i>tcd</i> | Pointer to the TCD structure. |
|------------|-------------------------------|

Note

This function enables the auto stop request feature.

### 16.7.20 void EDMA\_TcdSetTransferConfig ( edma\_tcd\_t \* *tcd*, const edma\_transfer\_config\_t \* *config*, edma\_tcd\_t \* *nextTcd* )

The TCD is a transfer control descriptor. The content of the TCD is the same as the hardware TCD registers. The STCD is used in the scatter-gather mode. This function configures the TCD transfer attribute, including source address, destination address, transfer size, address offset, and so on. It also configures the scatter gather feature if the user supplies the next TCD address. Example:

```

* edma_transfer_t config = {
* ...
* }
* edma_tcd_t tcd __aligned(32);
* edma_tcd_t nextTcd __aligned(32);
* EDMA_TcdSetTransferConfig(&tcd, &config, &nextTcd);
*

```

## Parameters

|                |                                                                                                          |
|----------------|----------------------------------------------------------------------------------------------------------|
| <i>tcd</i>     | Pointer to the TCD structure.                                                                            |
| <i>config</i>  | Pointer to eDMA transfer configuration structure.                                                        |
| <i>nextTcd</i> | Pointer to the next TCD structure. It can be NULL if users do not want to enable scatter/gather feature. |

## Note

TCD address should be 32 bytes aligned or it causes an eDMA error.

If the nextTcd is not NULL, the scatter gather feature is enabled and DREQ bit is cleared in the previous transfer configuration, which is set in the EDMA\_TcdReset.

### 16.7.21 void EDMA\_TcdSetMinorOffsetConfig ( *edma\_tcd\_t \* tcd, const edma\_minor\_offset\_config\_t \* config* )

A minor offset is a signed-extended value added to the source address or a destination address after each minor loop.

## Parameters

|               |                                                        |
|---------------|--------------------------------------------------------|
| <i>tcd</i>    | A point to the TCD structure.                          |
| <i>config</i> | A pointer to the minor offset configuration structure. |

### 16.7.22 void EDMA\_TcdSetChannelLink ( *edma\_tcd\_t \* tcd, edma\_channel\_link\_type\_t type, uint32\_t linkedChannel* )

This function configures either a minor link or a major link. The minor link means the channel link is triggered every time CITER decreases by 1. The major link means that the channel link is triggered when the CITER is exhausted.

## Note

Users should ensure that DONE flag is cleared before calling this interface, or the configuration is invalid.

Parameters

|                      |                                                                                                                                                           |
|----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>tcd</i>           | Point to the TCD structure.                                                                                                                               |
| <i>type</i>          | Channel link type, it can be one of: <ul style="list-style-type: none"><li>• kEDMA_LinkNone</li><li>• kEDMA_MinorLink</li><li>• kEDMA_MajorLink</li></ul> |
| <i>linkedChannel</i> | The linked channel number.                                                                                                                                |

### 16.7.23 static void EDMA\_TcdSetBandWidth ( *edma\_tcd\_t \* tcd*, *edma\_bandwidth\_t bandWidth* ) [inline], [static]

Because the eDMA processes the minor loop, it continuously generates read/write sequences until the minor count is exhausted. The bandwidth forces the eDMA to stall after the completion of each read/write access to control the bus request bandwidth seen by the crossbar switch.

Parameters

|                  |                                                                                                                                                                                                           |
|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>tcd</i>       | A pointer to the TCD structure.                                                                                                                                                                           |
| <i>bandWidth</i> | A bandwidth setting, which can be one of the following: <ul style="list-style-type: none"><li>• kEDMABandwidthStallNone</li><li>• kEDMABandwidthStall4Cycle</li><li>• kEDMABandwidthStall8Cycle</li></ul> |

### 16.7.24 void EDMA\_TcdSetModulo ( *edma\_tcd\_t \* tcd*, *edma\_modulo\_t srcModulo*, *edma\_modulo\_t destModulo* )

This function defines a specific address range specified to be the value after (SADDR + SOFF)/(DADDR + DOFF) calculation is performed or the original register value. It provides the ability to implement a circular data queue easily.

Parameters

|            |                                 |
|------------|---------------------------------|
| <i>tcd</i> | A pointer to the TCD structure. |
|------------|---------------------------------|

|                   |                             |
|-------------------|-----------------------------|
| <i>srcModulo</i>  | A source modulo value.      |
| <i>destModulo</i> | A destination modulo value. |

### 16.7.25 static void EDMA\_TcdEnableAutoStopRequest ( *edma\_tcd\_t \* tcd, bool enable* ) [inline], [static]

If enabling the auto stop request, the eDMA hardware automatically disables the hardware channel request.

Parameters

|               |                                                  |
|---------------|--------------------------------------------------|
| <i>tcd</i>    | A pointer to the TCD structure.                  |
| <i>enable</i> | The command to enable (true) or disable (false). |

### 16.7.26 void EDMA\_TcdEnableInterrupts ( *edma\_tcd\_t \* tcd, uint32\_t mask* )

Parameters

|             |                                                                                                     |
|-------------|-----------------------------------------------------------------------------------------------------|
| <i>tcd</i>  | Point to the TCD structure.                                                                         |
| <i>mask</i> | The mask of interrupt source to be set. Users need to use the defined edma_interrupt_enable_t type. |

### 16.7.27 void EDMA\_TcdDisableInterrupts ( *edma\_tcd\_t \* tcd, uint32\_t mask* )

Parameters

|             |                                                                                                     |
|-------------|-----------------------------------------------------------------------------------------------------|
| <i>tcd</i>  | Point to the TCD structure.                                                                         |
| <i>mask</i> | The mask of interrupt source to be set. Users need to use the defined edma_interrupt_enable_t type. |

### 16.7.28 void EDMA\_TcdSetMajorOffsetConfig ( *edma\_tcd\_t \* tcd, int32\_t sourceOffset, int32\_t destOffset* )

Adjustment value added to the source address at the completion of the major iteration count

Parameters

|                     |                                                                                     |
|---------------------|-------------------------------------------------------------------------------------|
| <i>tcd</i>          | A point to the TCD structure.                                                       |
| <i>sourceOffset</i> | source address offset will be applied to source address after major loop done.      |
| <i>destOffset</i>   | destination address offset will be applied to source address after major loop done. |

### **16.7.29 static void EDMA\_EnableChannelRequest ( DMA\_Type \* *base*, uint32\_t *channel* ) [inline], [static]**

This function enables the hardware channel request.

Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | eDMA peripheral base address. |
| <i>channel</i> | eDMA channel number.          |

### **16.7.30 static void EDMA\_DisableChannelRequest ( DMA\_Type \* *base*, uint32\_t *channel* ) [inline], [static]**

This function disables the hardware channel request.

Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | eDMA peripheral base address. |
| <i>channel</i> | eDMA channel number.          |

### **16.7.31 static void EDMA\_TriggerChannelStart ( DMA\_Type \* *base*, uint32\_t *channel* ) [inline], [static]**

This function starts a minor loop transfer.

Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | eDMA peripheral base address. |
| <i>channel</i> | eDMA channel number.          |

### 16.7.32 **uint32\_t EDMA\_GetRemainingMajorLoopCount ( DMA\_Type \* *base*,                   uint32\_t *channel* )**

This function checks the TCD (Task Control Descriptor) status for a specified eDMA channel and returns the number of major loop count that has not finished.

## Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | eDMA peripheral base address. |
| <i>channel</i> | eDMA channel number.          |

## Returns

Major loop count which has not been transferred yet for the current TCD.

## Note

1. This function can only be used to get unfinished major loop count of transfer without the next TCD, or it might be inaccuracy.
  1. The unfinished/remaining transfer bytes cannot be obtained directly from registers while the channel is running. Because to calculate the remaining bytes, the initial NBYTES configured in DMA\_TCDn\_NBYTES\_MLNO register is needed while the eDMA IP does not support getting it while a channel is active. In another word, the NBYTES value reading is always the actual (decrementing) NBYTES value the dma\_engine is working with while a channel is running. Consequently, to get the remaining transfer bytes, a software-saved initial value of NBYTES (for example copied before enabling the channel) is needed. The formula to calculate it is shown below: RemainingBytes = RemainingMajorLoopCount \* NBYTE-S(initially configured)

### 16.7.33 static uint32\_t EDMA\_GetErrorStatusFlags ( DMA\_Type \* *base* ) [inline], [static]

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | eDMA peripheral base address. |
|-------------|-------------------------------|

## Returns

The mask of error status flags. Users need to use the \_edma\_error\_status\_flags type to decode the return variables.

### 16.7.34 uint32\_t EDMA\_GetChannelStatusFlags ( DMA\_Type \* *base*, uint32\_t *channel* )

Parameters

|                |                               |
|----------------|-------------------------------|
| <i>base</i>    | eDMA peripheral base address. |
| <i>channel</i> | eDMA channel number.          |

Returns

The mask of channel status flags. Users need to use the `_edma_channel_status_flags` type to decode the return variables.

### 16.7.35 void EDMA\_ClearChannelStatusFlags ( DMA\_Type \* *base*, uint32\_t *channel*, uint32\_t *mask* )

Parameters

|                |                                                                                                                       |
|----------------|-----------------------------------------------------------------------------------------------------------------------|
| <i>base</i>    | eDMA peripheral base address.                                                                                         |
| <i>channel</i> | eDMA channel number.                                                                                                  |
| <i>mask</i>    | The mask of channel status to be cleared. Users need to use the defined <code>_edma_channel_status_flags</code> type. |

### 16.7.36 void EDMA\_CreateHandle ( edma\_handle\_t \* *handle*, DMA\_Type \* *base*, uint32\_t *channel* )

This function is called if using the transactional API for eDMA. This function initializes the internal state of the eDMA handle.

Parameters

|                |                                                                               |
|----------------|-------------------------------------------------------------------------------|
| <i>handle</i>  | eDMA handle pointer. The eDMA handle stores callback function and parameters. |
| <i>base</i>    | eDMA peripheral base address.                                                 |
| <i>channel</i> | eDMA channel number.                                                          |

### 16.7.37 void EDMA\_InstallTCDMemory ( edma\_handle\_t \* *handle*, edma\_tcd\_t \* *tcdPool*, uint32\_t *tcdSize* )

This function is called after the EDMA\_CreateHandle to use scatter/gather feature. This function shall only be used while users need to use scatter gather mode. Scatter gather mode enables EDMA to load a new transfer control block (tcd) in hardware, and automatically reconfigure that DMA channel for a

new transfer. Users need to prepare tcd memory and also configure tcds using interface EDMA\_SubmitTransfer.

Parameters

|                |                                                           |
|----------------|-----------------------------------------------------------|
| <i>handle</i>  | eDMA handle pointer.                                      |
| <i>tcdPool</i> | A memory pool to store TCDs. It must be 32 bytes aligned. |
| <i>tcdSize</i> | The number of TCD slots.                                  |

### 16.7.38 void EDMA\_SetCallback ( *edma\_handle\_t \* handle, edma\_callback callback, void \* userData* )

This callback is called in the eDMA IRQ handler. Use the callback to do something after the current major loop transfer completes. This function will be called every time one tcd finished transfer.

Parameters

|                 |                                        |
|-----------------|----------------------------------------|
| <i>handle</i>   | eDMA handle pointer.                   |
| <i>callback</i> | eDMA callback function pointer.        |
| <i>userData</i> | A parameter for the callback function. |

### 16.7.39 void EDMA\_PrepTransferConfig ( *edma\_transfer\_config\_t \* config, void \* srcAddr, uint32\_t srcWidth, int16\_t srcOffset, void \* destAddr, uint32\_t destWidth, int16\_t destOffset, uint32\_t bytesEachRequest, uint32\_t transferBytes* )

This function prepares the transfer configuration structure according to the user input.

Parameters

|                         |                                                                   |
|-------------------------|-------------------------------------------------------------------|
| <i>config</i>           | The user configuration structure of type <i>edma_transfer_t</i> . |
| <i>srcAddr</i>          | eDMA transfer source address.                                     |
| <i>srcWidth</i>         | eDMA transfer source address width(bytes).                        |
| <i>srcOffset</i>        | source address offset.                                            |
| <i>destAddr</i>         | eDMA transfer destination address.                                |
| <i>destWidth</i>        | eDMA transfer destination address width(bytes).                   |
| <i>destOffset</i>       | destination address offset.                                       |
| <i>bytesEachRequest</i> | eDMA transfer bytes per channel request.                          |
| <i>transferBytes</i>    | eDMA transfer bytes to be transferred.                            |

## Note

The data address and the data width must be consistent. For example, if the SRC is 4 bytes, the source address must be 4 bytes aligned, or it results in source address error (SAE).

#### **16.7.40 void EDMA\_PrepTransfer ( *edma\_transfer\_config\_t \* config, void \* srcAddr, uint32\_t srcWidth, void \* destAddr, uint32\_t destWidth, uint32\_t bytesEachRequest, uint32\_t transferBytes, edma\_transfer\_type\_t type* )**

This function prepares the transfer configuration structure according to the user input.

## Parameters

|                         |                                                                         |
|-------------------------|-------------------------------------------------------------------------|
| <i>config</i>           | The user configuration structure of type <code>edma_transfer_t</code> . |
| <i>srcAddr</i>          | eDMA transfer source address.                                           |
| <i>srcWidth</i>         | eDMA transfer source address width(bytes).                              |
| <i>destAddr</i>         | eDMA transfer destination address.                                      |
| <i>destWidth</i>        | eDMA transfer destination address width(bytes).                         |
| <i>bytesEachRequest</i> | eDMA transfer bytes per channel request.                                |
| <i>transferBytes</i>    | eDMA transfer bytes to be transferred.                                  |
| <i>type</i>             | eDMA transfer type.                                                     |

## Note

The data address and the data width must be consistent. For example, if the SRC is 4 bytes, the source address must be 4 bytes aligned, or it results in source address error (SAE).

#### **16.7.41 status\_t EDMA\_SubmitTransfer ( *edma\_handle\_t \* handle, const edma\_transfer\_config\_t \* config* )**

This function submits the eDMA transfer request according to the transfer configuration structure. In scatter gather mode, call this function will add a configured tcd to the circular list of tcd pool. The tcd pools is setup by call function `EDMA_InstallTCDMemory` before.

Parameters

|               |                                                   |
|---------------|---------------------------------------------------|
| <i>handle</i> | eDMA handle pointer.                              |
| <i>config</i> | Pointer to eDMA transfer configuration structure. |

Return values

|                                |                                                                     |
|--------------------------------|---------------------------------------------------------------------|
| <i>kStatus_EDMA_Success</i>    | It means submit transfer request succeed.                           |
| <i>kStatus_EDMA_Queue-Full</i> | It means TCD queue is full. Submit transfer request is not allowed. |
| <i>kStatus_EDMA_Busy</i>       | It means the given channel is busy, need to submit request later.   |

#### 16.7.42 void EDMA\_StartTransfer ( *edma\_handle\_t \* handle* )

This function enables the channel request. Users can call this function after submitting the transfer request or before submitting the transfer request.

Parameters

|               |                      |
|---------------|----------------------|
| <i>handle</i> | eDMA handle pointer. |
|---------------|----------------------|

#### 16.7.43 void EDMA\_StopTransfer ( *edma\_handle\_t \* handle* )

This function disables the channel request to pause the transfer. Users can call [EDMA\\_StartTransfer\(\)](#) again to resume the transfer.

Parameters

|               |                      |
|---------------|----------------------|
| <i>handle</i> | eDMA handle pointer. |
|---------------|----------------------|

#### 16.7.44 void EDMA\_AbortTransfer ( *edma\_handle\_t \* handle* )

This function disables the channel request and clear transfer status bits. Users can submit another transfer after calling this API.

Parameters

|               |                     |
|---------------|---------------------|
| <i>handle</i> | DMA handle pointer. |
|---------------|---------------------|

#### 16.7.45 static uint32\_t EDMA\_GetUnusedTCDNumber ( *edma\_handle\_t \* handle* ) [**inline**], [**static**]

This function gets current tcd index which is run. If the TCD pool pointer is NULL, it will return 0.

Parameters

|               |                     |
|---------------|---------------------|
| <i>handle</i> | DMA handle pointer. |
|---------------|---------------------|

Returns

The unused tcd slot number.

#### 16.7.46 static uint32\_t EDMA\_GetNextTCDAccount ( *edma\_handle\_t \* handle* ) [**inline**], [**static**]

This function gets the next tcd address. If this is last TCD, return 0.

Parameters

|               |                     |
|---------------|---------------------|
| <i>handle</i> | DMA handle pointer. |
|---------------|---------------------|

Returns

The next TCD address.

#### 16.7.47 void EDMA\_HandleIRQ ( *edma\_handle\_t \* handle* )

This function clears the channel major interrupt flag and calls the callback function if it is not NULL.

Note: For the case using TCD queue, when the major iteration count is exhausted, additional operations are performed. These include the final address adjustments and reloading of the BITER field into the CITER. Assertion of an optional interrupt request also occurs at this time, as does a possible fetch of a new TCD from memory using the scatter/gather address pointer included in the descriptor (if scatter/gather is enabled).

For instance, when the time interrupt of TCD[0] happens, the TCD[1] has already been loaded into the eDMA engine. As sga and sga\_index are calculated based on the DLAST\_SGA bitfield lies in the TCD\_CSR register, the sga\_index in this case should be 2 (DLAST\_SGA of TCD[1] stores the address of TCD[2]). Thus, the "tcdUsed" updated should be (tcdUsed - 2U) which indicates the number of TCDs can be loaded in the memory pool (because TCD[0] and TCD[1] have been loaded into the eDMA engine at this point already.).

For the last two continuous ISRs in a scatter/gather process, they both load the last TCD (The last ISR does not load a new TCD) from the memory pool to the eDMA engine when major loop completes. Therefore, ensure that the header and tcdUsed updated are identical for them. tcdUsed are both 0 in this case as no TCD to be loaded.

See the "eDMA basic data flow" in the eDMA Functional description section of the Reference Manual for further details.

### Parameters

|               |                      |
|---------------|----------------------|
| <i>handle</i> | eDMA handle pointer. |
|---------------|----------------------|

# Chapter 17

## EWM: External Watchdog Monitor Driver

### 17.1 Overview

The MCUXpresso SDK provides a peripheral driver for the External Watchdog (EWM) Driver module of MCUXpresso SDK devices.

### 17.2 Typical use case

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/ewm

### Data Structures

- struct `ewm_config_t`  
*Describes EWM clock source. [More...](#)*

### Enumerations

- enum `_ewm_interrupt_enable_t` { `kEWM_InterruptEnable` = EWM\_CTRL\_INTEN\_MASK }  
*EWM interrupt configuration structure with default settings all disabled.*
- enum `_ewm_status_flags_t` { `kEWM_RunningFlag` = EWM\_CTRL\_EWMEN\_MASK }  
*EWM status flags.*

### Driver version

- #define `FSL_EWM_DRIVER_VERSION` (MAKE\_VERSION(2, 0, 3))  
*EWM driver version 2.0.3.*

### EWM initialization and de-initialization

- void `EWM_Init` (EWM\_Type \*base, const `ewm_config_t` \*config)  
*Initializes the EWM peripheral.*
- void `EWM_Deinit` (EWM\_Type \*base)  
*Deinitializes the EWM peripheral.*
- void `EWM_GetDefaultConfig` (`ewm_config_t` \*config)  
*Initializes the EWM configuration structure.*

### EWM functional Operation

- static void `EWM_EnableInterrupts` (EWM\_Type \*base, uint32\_t mask)  
*Enables the EWM interrupt.*
- static void `EWM_DisableInterrupts` (EWM\_Type \*base, uint32\_t mask)  
*Disables the EWM interrupt.*
- static uint32\_t `EWM_GetStatusFlags` (EWM\_Type \*base)  
*Gets all status flags.*

- void **EWM\_Refresh** (EWM\_Type \*base)  
*Services the EWM.*

## 17.3 Data Structure Documentation

### 17.3.1 struct ewm\_config\_t

Data structure for EWM configuration.

This structure is used to configure the EWM.

#### Data Fields

- bool **enableEwm**  
*Enable EWM module.*
- bool **enableEwmInput**  
*Enable EWM\_in input.*
- bool **setInputAssertLogic**  
*EWM\_in signal assertion state.*
- bool **enableInterrupt**  
*Enable EWM interrupt.*
- uint8\_t **prescaler**  
*Clock prescaler value.*
- uint8\_t **compareLowValue**  
*Compare low-register value.*
- uint8\_t **compareHighValue**  
*Compare high-register value.*

## 17.4 Macro Definition Documentation

### 17.4.1 #define FSL\_EWM\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 3))

## 17.5 Enumeration Type Documentation

### 17.5.1 enum \_ewm\_interrupt\_enable\_t

This structure contains the settings for all of EWM interrupt configurations.

Enumerator

**kEWM InterruptEnable** Enable the EWM to generate an interrupt.

### 17.5.2 enum \_ewm\_status\_flags\_t

This structure contains the constants for the EWM status flags for use in the EWM functions.

Enumerator

***kEWM\_RunningFlag*** Running flag, set when EWM is enabled.

## 17.6 Function Documentation

### 17.6.1 void EWM\_Init ( EWM\_Type \* *base*, const ewm\_config\_t \* *config* )

This function is used to initialize the EWM. After calling, the EWM runs immediately according to the configuration. Note that, except for the interrupt enable control bit, other control bits and registers are write once after a CPU reset. Modifying them more than once generates a bus transfer error.

This is an example.

```
* ewm_config_t config;
* EWM_GetDefaultConfig(&config);
* config.compareHighValue = 0xAAU;
* EWM_Init(ewm_base, &config);
*
```

Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | EWM peripheral base address  |
| <i>config</i> | The configuration of the EWM |

### 17.6.2 void EWM\_Deinit ( EWM\_Type \* *base* )

This function is used to shut down the EWM.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | EWM peripheral base address |
|-------------|-----------------------------|

### 17.6.3 void EWM\_GetDefaultConfig ( ewm\_config\_t \* *config* )

This function initializes the EWM configuration structure to default values. The default values are as follows.

```
* ewmConfig->enableEwm = true;
* ewmConfig->enableEwmInput = false;
* ewmConfig->setInputAssertLogic = false;
* ewmConfig->enableInterrupt = false;
* ewmConfig->ewm_lpo_clock_source_t = kEWM_LpoClockSource0;
* ewmConfig->prescaler = 0;
* ewmConfig->compareLowValue = 0;
* ewmConfig->compareHighValue = 0xFEU;
*
```

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>config</i> | Pointer to the EWM configuration structure. |
|---------------|---------------------------------------------|

See Also

[ewm\\_config\\_t](#)

#### 17.6.4 static void EWM\_EnableInterrupts ( **EWM\_Type** \* *base*, **uint32\_t** *mask* ) [**inline**], [**static**]

This function enables the EWM interrupt.

Parameters

|             |                                                                                                                                                                     |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | EWM peripheral base address                                                                                                                                         |
| <i>mask</i> | The interrupts to enable The parameter can be combination of the following source if defined <ul style="list-style-type: none"><li>• kEWM_InterruptEnable</li></ul> |

#### 17.6.5 static void EWM\_DisableInterrupts ( **EWM\_Type** \* *base*, **uint32\_t** *mask* ) [**inline**], [**static**]

This function enables the EWM interrupt.

Parameters

|             |                                                                                                                                                                      |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | EWM peripheral base address                                                                                                                                          |
| <i>mask</i> | The interrupts to disable The parameter can be combination of the following source if defined <ul style="list-style-type: none"><li>• kEWM_InterruptEnable</li></ul> |

#### 17.6.6 static **uint32\_t** EWM\_GetStatusFlags ( **EWM\_Type** \* *base* ) [**inline**], [**static**]

This function gets all status flags.

This is an example for getting the running flag.

```
* uint32_t status;
* status = EWM_GetStatusFlags(ewm_base) & kEWM_RunningFlag;
*
```

## Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | EWM peripheral base address |
|-------------|-----------------------------|

## Returns

State of the status flag: asserted (true) or not-asserted (false).

## See Also

[\\_ewm\\_status\\_flags\\_t](#)

- True: a related status flag has been set.
- False: a related status flag is not set.

### 17.6.7 void EWM\_Refresh ( EWM\_Type \* *base* )

This function resets the EWM counter to zero.

## Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | EWM peripheral base address |
|-------------|-----------------------------|

# Chapter 18

## FlexIO: FlexIO Driver

### 18.1 Overview

The MCUXpresso SDK provides a generic driver and multiple protocol-specific FlexIO drivers for the FlexIO module of MCUXpresso SDK devices.

### Modules

- [FlexIO Driver](#)
- [FlexIO I2C Master Driver](#)
- [FlexIO I2S Driver](#)
- [FlexIO SPI Driver](#)
- [FlexIO UART Driver](#)

## 18.2 FlexIO Driver

### 18.2.1 Overview

#### Data Structures

- struct `flexio_config_t`  
*Define FlexIO user configuration structure. [More...](#)*
- struct `flexio_timer_config_t`  
*Define FlexIO timer configuration structure. [More...](#)*
- struct `flexio_shifter_config_t`  
*Define FlexIO shifter configuration structure. [More...](#)*

#### Macros

- #define `FLEXIO_TIMER_TRIGGER_SEL_PININPUT`(x) ((uint32\_t)(x) << 1U)  
*Calculate FlexIO timer trigger.*

#### Typedefs

- typedef void(\* `flexio_isr_t` )(void \*base, void \*handle)  
*typedef for FlexIO simulated driver interrupt handler.*

#### Enumerations

- enum `flexio_timer_trigger_polarity_t` {
   
*kFLEXIO\_TimerTriggerPolarityActiveHigh = 0x0U,*
  
*kFLEXIO\_TimerTriggerPolarityActiveLow = 0x1U }*
  
*Define time of timer trigger polarity.*
- enum `flexio_timer_trigger_source_t` {
   
*kFLEXIO\_TimerTriggerSourceExternal = 0x0U,*
  
*kFLEXIO\_TimerTriggerSourceInternal = 0x1U }*
  
*Define type of timer trigger source.*
- enum `flexio_pin_config_t` {
   
*kFLEXIO\_PinConfigOutputDisabled = 0x0U,*
  
*kFLEXIO\_PinConfigOpenDrainOrBidirection = 0x1U,*
  
*kFLEXIO\_PinConfigBidirectionOutputData = 0x2U,*
  
*kFLEXIO\_PinConfigOutput = 0x3U }*
  
*Define type of timer/shifter pin configuration.*
- enum `flexio_pin_polarity_t` {
   
*kFLEXIO\_PinActiveHigh = 0x0U,*
  
*kFLEXIO\_PinActiveLow = 0x1U }*
  
*Definition of pin polarity.*

- enum `flexio_timer_mode_t` {
   
  `kFLEXIO_TimerModeDisabled` = 0x0U,
   
  `kFLEXIO_TimerModeDual8BitBaudBit` = 0x1U,
   
  `kFLEXIO_TimerModeDual8BitPWM` = 0x2U,
   
  `kFLEXIO_TimerModeSingle16Bit` = 0x3U }
   
    *Define type of timer work mode.*
- enum `flexio_timer_output_t` {
   
  `kFLEXIO_TimerOutputOneNotAffectedByReset` = 0x0U,
   
  `kFLEXIO_TimerOutputZeroNotAffectedByReset` = 0x1U,
   
  `kFLEXIO_TimerOutputOneAffectedByReset` = 0x2U,
   
  `kFLEXIO_TimerOutputZeroAffectedByReset` = 0x3U }
   
    *Define type of timer initial output or timer reset condition.*
- enum `flexio_timer_decrement_source_t` {
   
  `kFLEXIO_TimerDecSrcOnFlexIOClockShiftTimerOutput` = 0x0U,
   
  `kFLEXIO_TimerDecSrcOnTriggerInputShiftTimerOutput` = 0x1U,
   
  `kFLEXIO_TimerDecSrcOnPinInputShiftPinInput` = 0x2U,
   
  `kFLEXIO_TimerDecSrcOnTriggerInputShiftTriggerInput` = 0x3U }
   
    *Define type of timer decrement.*
- enum `flexio_timer_reset_condition_t` {
   
  `kFLEXIO_TimerResetNever` = 0x0U,
   
  `kFLEXIO_TimerResetOnTimerPinEqualToTimerOutput` = 0x2U,
   
  `kFLEXIO_TimerResetOnTimerTriggerEqualToTimerOutput` = 0x3U,
   
  `kFLEXIO_TimerResetOnTimerPinRisingEdge` = 0x4U,
   
  `kFLEXIO_TimerResetOnTimerTriggerRisingEdge` = 0x6U,
   
  `kFLEXIO_TimerResetOnTimerTriggerBothEdge` = 0x7U }
   
    *Define type of timer reset condition.*
- enum `flexio_timer_disable_condition_t` {
   
  `kFLEXIO_TimerDisableNever` = 0x0U,
   
  `kFLEXIO_TimerDisableOnPreTimerDisable` = 0x1U,
   
  `kFLEXIO_TimerDisableOnTimerCompare` = 0x2U,
   
  `kFLEXIO_TimerDisableOnTimerCompareTriggerLow` = 0x3U,
   
  `kFLEXIO_TimerDisableOnPinBothEdge` = 0x4U,
   
  `kFLEXIO_TimerDisableOnPinBothEdgeTriggerHigh` = 0x5U,
   
  `kFLEXIO_TimerDisableOnTriggerFallingEdge` = 0x6U }
   
    *Define type of timer disable condition.*
- enum `flexio_timer_enable_condition_t` {
   
  `kFLEXIO_TimerEnabledAlways` = 0x0U,
   
  `kFLEXIO_TimerEnableOnPrevTimerEnable` = 0x1U,
   
  `kFLEXIO_TimerEnableOnTriggerHigh` = 0x2U,
   
  `kFLEXIO_TimerEnableOnTriggerHighPinHigh` = 0x3U,
   
  `kFLEXIO_TimerEnableOnPinRisingEdge` = 0x4U,
   
  `kFLEXIO_TimerEnableOnPinRisingEdgeTriggerHigh` = 0x5U,
   
  `kFLEXIO_TimerEnableOnTriggerRisingEdge` = 0x6U,
   
  `kFLEXIO_TimerEnableOnTriggerBothEdge` = 0x7U }
   
    *Define type of timer enable condition.*
- enum `flexio_timer_stop_bit_condition_t` {

```
kFLEXIO_TimerStopBitDisabled = 0x0U,
kFLEXIO_TimerStopBitEnableOnTimerCompare = 0x1U,
kFLEXIO_TimerStopBitEnableOnTimerDisable = 0x2U,
kFLEXIO_TimerStopBitEnableOnTimerCompareDisable = 0x3U }
```

*Define type of timer stop bit generate condition.*

- enum `flexio_timer_start_bit_condition_t` {
   
kFLEXIO\_TimerStartBitDisabled = 0x0U,
   
kFLEXIO\_TimerStartBitEnabled = 0x1U }

*Define type of timer start bit generate condition.*

- enum `flexio_shifter_timer_polarity_t` {
   
kFLEXIO\_ShifterTimerPolarityOnPositive = 0x0U,
   
kFLEXIO\_ShifterTimerPolarityOnNegative = 0x1U }

*Define type of timer polarity for shifter control.*

- enum `flexio_shifter_mode_t` {
   
kFLEXIO\_ShifterDisabled = 0x0U,
   
kFLEXIO\_ShifterModeReceive = 0x1U,
   
kFLEXIO\_ShifterModeTransmit = 0x2U,
   
kFLEXIO\_ShifterModeMatchStore = 0x4U,
   
kFLEXIO\_ShifterModeMatchContinuous = 0x5U,
   
kFLEXIO\_ShifterModeState = 0x6U,
   
kFLEXIO\_ShifterModeLogic = 0x7U }

*Define type of shifter working mode.*

- enum `flexio_shifter_input_source_t` {
   
kFLEXIO\_ShifterInputFromPin = 0x0U,
   
kFLEXIO\_ShifterInputFromNextShifterOutput = 0x1U }

*Define type of shifter input source.*

- enum `flexio_shifter_stop_bit_t` {
   
kFLEXIO\_ShifterStopBitDisable = 0x0U,
   
kFLEXIO\_ShifterStopBitLow = 0x2U,
   
kFLEXIO\_ShifterStopBitHigh = 0x3U }

*Define of STOP bit configuration.*

- enum `flexio_shifter_start_bit_t` {
   
kFLEXIO\_ShifterStartBitDisabledLoadDataOnEnable = 0x0U,
   
kFLEXIO\_ShifterStartBitDisabledLoadDataOnShift = 0x1U,
   
kFLEXIO\_ShifterStartBitLow = 0x2U,
   
kFLEXIO\_ShifterStartBitHigh = 0x3U }

*Define type of START bit configuration.*

- enum `flexio_shifter_buffer_type_t` {
   
kFLEXIO\_ShifterBuffer = 0x0U,
   
kFLEXIO\_ShifterBufferBitSwapped = 0x1U,
   
kFLEXIO\_ShifterBufferByteSwapped = 0x2U,
   
kFLEXIO\_ShifterBufferBitByteSwapped = 0x3U,
   
kFLEXIO\_ShifterBufferNibbleByteSwapped = 0x4U,
   
kFLEXIO\_ShifterBufferHalfWordSwapped = 0x5U,
   
kFLEXIO\_ShifterBufferNibbleSwapped = 0x6U }

*Define FlexIO shifter buffer type.*

## Variables

- `FLEXIO_Type *const s_flexioBases []`  
*Pointers to flexio bases for each instance.*
- `const clock_ip_name_t s_flexioClocks []`  
*Pointers to flexio clocks for each instance.*

## Driver version

- `#define FSL_FLEXIO_DRIVER_VERSION (MAKE_VERSION(2, 0, 4))`  
*FlexIO driver version.*

## FlexIO Initialization and De-initialization

- `void FLEXIO_GetDefaultConfig (flexio_config_t *userConfig)`  
*Gets the default configuration to configure the FlexIO module.*
- `void FLEXIO_Init (FLEXIO_Type *base, const flexio_config_t *userConfig)`  
*Configures the FlexIO with a FlexIO configuration.*
- `void FLEXIO_Deinit (FLEXIO_Type *base)`  
*Gates the FlexIO clock.*
- `uint32_t FLEXIOGetInstance (FLEXIO_Type *base)`  
*Get instance number for FLEXIO module.*

## FlexIO Basic Operation

- `void FLEXIO_Reset (FLEXIO_Type *base)`  
*Resets the FlexIO module.*
- `static void FLEXIO_Enable (FLEXIO_Type *base, bool enable)`  
*Enables the FlexIO module operation.*
- `static uint32_t FLEXIO_ReadPinInput (FLEXIO_Type *base)`  
*Reads the input data on each of the FlexIO pins.*
- `static uint8_t FLEXIO_GetShifterState (FLEXIO_Type *base)`  
*Gets the current state pointer for state mode use.*
- `void FLEXIO_SetShifterConfig (FLEXIO_Type *base, uint8_t index, const flexio_shifter_config_t *shifterConfig)`  
*Configures the shifter with the shifter configuration.*
- `void FLEXIO_SetTimerConfig (FLEXIO_Type *base, uint8_t index, const flexio_timer_config_t *timerConfig)`  
*Configures the timer with the timer configuration.*

## FlexIO Interrupt Operation

- `static void FLEXIO_EnableShifterStatusInterrupts (FLEXIO_Type *base, uint32_t mask)`  
*Enables the shifter status interrupt.*
- `static void FLEXIO_DisableShifterStatusInterrupts (FLEXIO_Type *base, uint32_t mask)`

- static void [FLEXIO\\_EnableShifterErrorInterrupts](#) (FLEXIO\_Type \*base, uint32\_t mask)
 

*Disables the shifter status interrupt.*
- static void [FLEXIO\\_DisableShifterErrorInterrupts](#) (FLEXIO\_Type \*base, uint32\_t mask)
 

*Enables the shifter error interrupt.*
- static void [FLEXIO\\_DisableShifterErrorInterrupts](#) (FLEXIO\_Type \*base, uint32\_t mask)
 

*Disables the shifter error interrupt.*
- static void [FLEXIO\\_EnableTimerStatusInterrupts](#) (FLEXIO\_Type \*base, uint32\_t mask)
 

*Enables the timer status interrupt.*
- static void [FLEXIO\\_DisableTimerStatusInterrupts](#) (FLEXIO\_Type \*base, uint32\_t mask)
 

*Disables the timer status interrupt.*

## FlexIO Status Operation

- static uint32\_t [FLEXIO\\_GetShifterStatusFlags](#) (FLEXIO\_Type \*base)
 

*Gets the shifter status flags.*
- static void [FLEXIO\\_ClearShifterStatusFlags](#) (FLEXIO\_Type \*base, uint32\_t mask)
 

*Clears the shifter status flags.*
- static uint32\_t [FLEXIO\\_GetShifterErrorFlags](#) (FLEXIO\_Type \*base)
 

*Gets the shifter error flags.*
- static void [FLEXIO\\_ClearShifterErrorFlags](#) (FLEXIO\_Type \*base, uint32\_t mask)
 

*Clears the shifter error flags.*
- static uint32\_t [FLEXIO\\_GetTimerStatusFlags](#) (FLEXIO\_Type \*base)
 

*Gets the timer status flags.*
- static void [FLEXIO\\_ClearTimerStatusFlags](#) (FLEXIO\_Type \*base, uint32\_t mask)
 

*Clears the timer status flags.*

## FlexIO DMA Operation

- static void [FLEXIO\\_EnableShifterStatusDMA](#) (FLEXIO\_Type \*base, uint32\_t mask, bool enable)
 

*Enables/disables the shifter status DMA.*
- uint32\_t [FLEXIO\\_GetShifterBufferAddress](#) (FLEXIO\_Type \*base, flexio\_shifter\_buffer\_type\_t type, uint8\_t index)
 

*Gets the shifter buffer address for the DMA transfer usage.*
- status\_t [FLEXIO\\_RegisterHandleIRQ](#) (void \*base, void \*handle, flexio\_isr\_t isr)
 

*Registers the handle and the interrupt handler for the FlexIO-simulated peripheral.*
- status\_t [FLEXIO\\_UnregisterHandleIRQ](#) (void \*base)
 

*Unregisters the handle and the interrupt handler for the FlexIO-simulated peripheral.*

### 18.2.2 Data Structure Documentation

#### 18.2.2.1 struct flexio\_config\_t

##### Data Fields

- bool [enableFlexio](#)

*Enable/disable FlexIO module.*
- bool [enableInDoze](#)

- **bool enableInDebug**  
Enable/disable FlexIO operation in doze mode.
- **bool enableFastAccess**  
Enable/disable FlexIO operation in debug mode.  
Enable/disable fast access to FlexIO registers, fast access requires the FlexIO clock to be at least twice the frequency of the bus clock.

## Field Documentation

### (1) **bool flexio\_config\_t::enableFastAccess**

#### 18.2.2.2 struct flexio\_timer\_config\_t

##### Data Fields

- **uint32\_t triggerSelect**  
*The internal trigger selection number using MACROS.*
- **flexio\_timer\_trigger\_polarity\_t triggerPolarity**  
*Trigger Polarity.*
- **flexio\_timer\_trigger\_source\_t triggerSource**  
*Trigger Source, internal (see 'trgsel') or external.*
- **flexio\_pin\_config\_t pinConfig**  
*Timer Pin Configuration.*
- **uint32\_t pinSelect**  
*Timer Pin number Select.*
- **flexio\_pin\_polarity\_t pinPolarity**  
*Timer Pin Polarity.*
- **flexio\_timer\_mode\_t timerMode**  
*Timer work Mode.*
- **flexio\_timer\_output\_t timerOutput**  
*Configures the initial state of the Timer Output and whether it is affected by the Timer reset.*
- **flexio\_timer\_decrement\_source\_t timerDecrement**  
*Configures the source of the Timer decrement and the source of the Shift clock.*
- **flexio\_timer\_reset\_condition\_t timerReset**  
*Configures the condition that causes the timer counter (and optionally the timer output) to be reset.*
- **flexio\_timer\_disable\_condition\_t timerDisable**  
*Configures the condition that causes the Timer to be disabled and stop decrementing.*
- **flexio\_timer\_enable\_condition\_t timerEnable**  
*Configures the condition that causes the Timer to be enabled and start decrementing.*
- **flexio\_timer\_stop\_bit\_condition\_t timerStop**  
*Timer STOP Bit generation.*
- **flexio\_timer\_start\_bit\_condition\_t timerStart**  
*Timer STRAT Bit generation.*
- **uint32\_t timerCompare**  
*Value for Timer Compare N Register.*

## Field Documentation

- (1) `uint32_t flexio_timer_config_t::triggerSelect`
- (2) `flexio_timer_trigger_polarity_t flexio_timer_config_t::triggerPolarity`
- (3) `flexio_timer_trigger_source_t flexio_timer_config_t::triggerSource`
- (4) `flexio_pin_config_t flexio_timer_config_t::pinConfig`
- (5) `uint32_t flexio_timer_config_t::pinSelect`
- (6) `flexio_pin_polarity_t flexio_timer_config_t::pinPolarity`
- (7) `flexio_timer_mode_t flexio_timer_config_t::timerMode`
- (8) `flexio_timer_output_t flexio_timer_config_t::timerOutput`
- (9) `flexio_timer_decrement_source_t flexio_timer_config_t::timerDecrement`
- (10) `flexio_timer_reset_condition_t flexio_timer_config_t::timerReset`
- (11) `flexio_timer_disable_condition_t flexio_timer_config_t::timerDisable`
- (12) `flexio_timer_enable_condition_t flexio_timer_config_t::timerEnable`
- (13) `flexio_timer_stop_bit_condition_t flexio_timer_config_t::timerStop`
- (14) `flexio_timer_start_bit_condition_t flexio_timer_config_t::timerStart`
- (15) `uint32_t flexio_timer_config_t::timerCompare`

### 18.2.2.3 struct flexio\_shifter\_config\_t

#### Data Fields

- `uint32_t timerSelect`  
*Selects which Timer is used for controlling the logic/shift register and generating the Shift clock.*
- `flexio_shifter_timer_polarity_t timerPolarity`  
*Timer Polarity.*
- `flexio_pin_config_t pinConfig`  
*Shifter Pin Configuration.*
- `uint32_t pinSelect`  
*Shifter Pin number Select.*
- `flexio_pin_polarity_t pinPolarity`  
*Shifter Pin Polarity.*
- `flexio_shifter_mode_t shifterMode`  
*Configures the mode of the Shifter.*
- `uint32_t parallelWidth`  
*Configures the parallel width when using parallel mode.*

- **flexio\_shifter\_input\_source\_t inputSource**  
*Selects the input source for the shifter.*
- **flexio\_shifter\_stop\_bit\_t shifterStop**  
*Shifter STOP bit.*
- **flexio\_shifter\_start\_bit\_t shifterStart**  
*Shifter START bit.*

## Field Documentation

- (1) **uint32\_t flexio\_shifter\_config\_t::timerSelect**
- (2) **flexio\_shifter\_timer\_polarity\_t flexio\_shifter\_config\_t::timerPolarity**
- (3) **flexio\_pin\_config\_t flexio\_shifter\_config\_t::pinConfig**
- (4) **uint32\_t flexio\_shifter\_config\_t::pinSelect**
- (5) **flexio\_pin\_polarity\_t flexio\_shifter\_config\_t::pinPolarity**
- (6) **flexio\_shifter\_mode\_t flexio\_shifter\_config\_t::shifterMode**
- (7) **uint32\_t flexio\_shifter\_config\_t::parallelWidth**
- (8) **flexio\_shifter\_input\_source\_t flexio\_shifter\_config\_t::inputSource**
- (9) **flexio\_shifter\_stop\_bit\_t flexio\_shifter\_config\_t::shifterStop**
- (10) **flexio\_shifter\_start\_bit\_t flexio\_shifter\_config\_t::shifterStart**

## 18.2.3 Macro Definition Documentation

**18.2.3.1 #define FSL\_FLEXIO\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 4))**

**18.2.3.2 #define FLEXIO\_TIMER\_TRIGGER\_SEL\_PININPUT( x ) ((uint32\_t)(x) << 1U)**

## 18.2.4 Typedef Documentation

**18.2.4.1 typedef void(\* flexio\_isr\_t)(void \*base, void \*handle)**

## 18.2.5 Enumeration Type Documentation

### 18.2.5.1 enum flexio\_timer\_trigger\_polarity\_t

Enumerator

**kFLEXIO\_TimerTriggerPolarityActiveHigh** Active high.

**kFLEXIO\_TimerTriggerPolarityActiveLow** Active low.

### 18.2.5.2 enum flexio\_timer\_trigger\_source\_t

Enumerator

*kFLEXIO\_TimerTriggerSourceExternal* External trigger selected.

*kFLEXIO\_TimerTriggerSourceInternal* Internal trigger selected.

### 18.2.5.3 enum flexio\_pin\_config\_t

Enumerator

*kFLEXIO\_PinConfigOutputDisabled* Pin output disabled.

*kFLEXIO\_PinConfigOpenDrainOrBidirection* Pin open drain or bidirectional output enable.

*kFLEXIO\_PinConfigBidirectionOutputData* Pin bidirectional output data.

*kFLEXIO\_PinConfigOutput* Pin output.

### 18.2.5.4 enum flexio\_pin\_polarity\_t

Enumerator

*kFLEXIO\_PinActiveHigh* Active high.

*kFLEXIO\_PinActiveLow* Active low.

### 18.2.5.5 enum flexio\_timer\_mode\_t

Enumerator

*kFLEXIO\_TimerModeDisabled* Timer Disabled.

*kFLEXIO\_TimerModeDual8BitBaudBit* Dual 8-bit counters baud/bit mode.

*kFLEXIO\_TimerModeDual8BitPWM* Dual 8-bit counters PWM mode.

*kFLEXIO\_TimerModeSingle16Bit* Single 16-bit counter mode.

### 18.2.5.6 enum flexio\_timer\_output\_t

Enumerator

*kFLEXIO\_TimerOutputOneNotAffectedByReset* Logic one when enabled and is not affected by timer reset.

*kFLEXIO\_TimerOutputZeroNotAffectedByReset* Logic zero when enabled and is not affected by timer reset.

*kFLEXIO\_TimerOutputOneAffectedByReset* Logic one when enabled and on timer reset.

*kFLEXIO\_TimerOutputZeroAffectedByReset* Logic zero when enabled and on timer reset.

### 18.2.5.7 enum flexio\_timer\_decrement\_source\_t

Enumerator

- kFLEXIO\_TimerDecSrcOnFlexIOClockShiftTimerOutput*** Decrement counter on FlexIO clock, Shift clock equals Timer output.
- kFLEXIO\_TimerDecSrcOnTriggerInputShiftTimerOutput*** Decrement counter on Trigger input (both edges), Shift clock equals Timer output.
- kFLEXIO\_TimerDecSrcOnPinInputShiftPinInput*** Decrement counter on Pin input (both edges), Shift clock equals Pin input.
- kFLEXIO\_TimerDecSrcOnTriggerInputShiftTriggerInput*** Decrement counter on Trigger input (both edges), Shift clock equals Trigger input.

### 18.2.5.8 enum flexio\_timer\_reset\_condition\_t

Enumerator

- kFLEXIO\_TimerResetNever*** Timer never reset.
- kFLEXIO\_TimerResetOnTimerPinEqualToTimerOutput*** Timer reset on Timer Pin equal to Timer Output.
- kFLEXIO\_TimerResetOnTimerTriggerEqualToTimerOutput*** Timer reset on Timer Trigger equal to Timer Output.
- kFLEXIO\_TimerResetOnTimerPinRisingEdge*** Timer reset on Timer Pin rising edge.
- kFLEXIO\_TimerResetOnTimerTriggerRisingEdge*** Timer reset on Trigger rising edge.
- kFLEXIO\_TimerResetOnTimerTriggerBothEdge*** Timer reset on Trigger rising or falling edge.

### 18.2.5.9 enum flexio\_timer\_disable\_condition\_t

Enumerator

- kFLEXIO\_TimerDisableNever*** Timer never disabled.
- kFLEXIO\_TimerDisableOnPreTimerDisable*** Timer disabled on Timer N-1 disable.
- kFLEXIO\_TimerDisableOnTimerCompare*** Timer disabled on Timer compare.
- kFLEXIO\_TimerDisableOnTimerCompareTriggerLow*** Timer disabled on Timer compare and Trigger Low.
- kFLEXIO\_TimerDisableOnPinBothEdge*** Timer disabled on Pin rising or falling edge.
- kFLEXIO\_TimerDisableOnPinBothEdgeTriggerHigh*** Timer disabled on Pin rising or falling edge provided Trigger is high.
- kFLEXIO\_TimerDisableOnTriggerFallingEdge*** Timer disabled on Trigger falling edge.

### 18.2.5.10 enum flexio\_timer\_enable\_condition\_t

Enumerator

- kFLEXIO\_TimerEnabledAlways*** Timer always enabled.

***kFLEXIO\_TimerEnableOnPrevTimerEnable*** Timer enabled on Timer N-1 enable.

***kFLEXIO\_TimerEnableOnTriggerHigh*** Timer enabled on Trigger high.

***kFLEXIO\_TimerEnableOnTriggerHighPinHigh*** Timer enabled on Trigger high and Pin high.

***kFLEXIO\_TimerEnableOnPinRisingEdge*** Timer enabled on Pin rising edge.

***kFLEXIO\_TimerEnableOnPinRisingEdgeTriggerHigh*** Timer enabled on Pin rising edge and Trigger high.

***kFLEXIO\_TimerEnableOnTriggerRisingEdge*** Timer enabled on Trigger rising edge.

***kFLEXIO\_TimerEnableOnTriggerBothEdge*** Timer enabled on Trigger rising or falling edge.

### 18.2.5.11 enum flexio\_timer\_stop\_bit\_condition\_t

Enumerator

***kFLEXIO\_TimerStopBitDisabled*** Stop bit disabled.

***kFLEXIO\_TimerStopBitEnableOnTimerCompare*** Stop bit is enabled on timer compare.

***kFLEXIO\_TimerStopBitEnableOnTimerDisable*** Stop bit is enabled on timer disable.

***kFLEXIO\_TimerStopBitEnableOnTimerCompareDisable*** Stop bit is enabled on timer compare and timer disable.

### 18.2.5.12 enum flexio\_timer\_start\_bit\_condition\_t

Enumerator

***kFLEXIO\_TimerStartBitDisabled*** Start bit disabled.

***kFLEXIO\_TimerStartBitEnabled*** Start bit enabled.

### 18.2.5.13 enum flexio\_shifter\_timer\_polarity\_t

Enumerator

***kFLEXIO\_ShifterTimerPolarityOnPositive*** Shift on positive edge of shift clock.

***kFLEXIO\_ShifterTimerPolarityOnNegative*** Shift on negative edge of shift clock.

### 18.2.5.14 enum flexio\_shifter\_mode\_t

Enumerator

***kFLEXIO\_ShifterDisabled*** Shifter is disabled.

***kFLEXIO\_ShifterModeReceive*** Receive mode.

***kFLEXIO\_ShifterModeTransmit*** Transmit mode.

***kFLEXIO\_ShifterModeMatchStore*** Match store mode.

***kFLEXIO\_ShifterModeMatchContinuous*** Match continuous mode.

***kFLEXIO\_ShifterModeState*** SHIFTBUF contents are used for storing programmable state attributes.

***kFLEXIO\_ShifterModeLogic*** SHIFTBUF contents are used for implementing programmable logic look up table.

#### 18.2.5.15 enum flexio\_shifter\_input\_source\_t

Enumerator

***kFLEXIO\_ShifterInputFromPin*** Shifter input from pin.

***kFLEXIO\_ShifterInputFromNextShifterOutput*** Shifter input from Shifter N+1.

#### 18.2.5.16 enum flexio\_shifter\_stop\_bit\_t

Enumerator

***kFLEXIO\_ShifterStopBitDisable*** Disable shifter stop bit.

***kFLEXIO\_ShifterStopBitLow*** Set shifter stop bit to logic low level.

***kFLEXIO\_ShifterStopBitHigh*** Set shifter stop bit to logic high level.

#### 18.2.5.17 enum flexio\_shifter\_start\_bit\_t

Enumerator

***kFLEXIO\_ShifterStartBitDisabledLoadDataOnEnable*** Disable shifter start bit, transmitter loads data on enable.

***kFLEXIO\_ShifterStartBitDisabledLoadDataOnShift*** Disable shifter start bit, transmitter loads data on first shift.

***kFLEXIO\_ShifterStartBitLow*** Set shifter start bit to logic low level.

***kFLEXIO\_ShifterStartBitHigh*** Set shifter start bit to logic high level.

#### 18.2.5.18 enum flexio\_shifter\_buffer\_type\_t

Enumerator

***kFLEXIO\_ShifterBuffer*** Shifter Buffer N Register.

***kFLEXIO\_ShifterBufferBitSwapped*** Shifter Buffer N Bit Byte Swapped Register.

***kFLEXIO\_ShifterBufferByteSwapped*** Shifter Buffer N Byte Swapped Register.

***kFLEXIO\_ShifterBufferBitByteSwapped*** Shifter Buffer N Bit Swapped Register.

***kFLEXIO\_ShifterBufferNibbleByteSwapped*** Shifter Buffer N Nibble Byte Swapped Register.

***kFLEXIO\_ShifterBufferHalfWordSwapped*** Shifter Buffer N Half Word Swapped Register.

***kFLEXIO\_ShifterBufferNibbleSwapped*** Shifter Buffer N Nibble Swapped Register.

## 18.2.6 Function Documentation

### 18.2.6.1 void FLEXIO\_GetDefaultConfig ( flexio\_config\_t \* *userConfig* )

The configuration can used directly to call the FLEXIO\_Configure().

Example:

```
flexio_config_t config;
FLEXIO_GetDefaultConfig(&config);
```

Parameters

|                   |                                                   |
|-------------------|---------------------------------------------------|
| <i>userConfig</i> | pointer to <code>flexio_config_t</code> structure |
|-------------------|---------------------------------------------------|

### 18.2.6.2 void FLEXIO\_Init ( FLEXIO\_Type \* *base*, const flexio\_config\_t \* *userConfig* )

The configuration structure can be filled by the user or be set with default values by [FLEXIO\\_GetDefaultConfig\(\)](#).

Example

```
flexio_config_t config = {
.enableFlexio = true,
.enableInDoze = false,
.enableInDebug = true,
.enableFastAccess = false
};
FLEXIO_Configure(base, &config);
```

Parameters

|                   |                                                   |
|-------------------|---------------------------------------------------|
| <i>base</i>       | FlexIO peripheral base address                    |
| <i>userConfig</i> | pointer to <code>flexio_config_t</code> structure |

### 18.2.6.3 void FLEXIO\_Deinit ( FLEXIO\_Type \* *base* )

Call this API to stop the FlexIO clock.

Note

After calling this API, call the FLEXO\_Init to use the FlexIO module.

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | FlexIO peripheral base address |
|-------------|--------------------------------|

#### 18.2.6.4 `uint32_t FLEXIO_GetInstance ( FLEXIO_Type * base )`

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | FLEXIO peripheral base address. |
|-------------|---------------------------------|

#### 18.2.6.5 `void FLEXIO_Reset ( FLEXIO_Type * base )`

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | FlexIO peripheral base address |
|-------------|--------------------------------|

#### 18.2.6.6 `static void FLEXIO_Enable ( FLEXIO_Type * base, bool enable ) [inline], [static]`

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | FlexIO peripheral base address    |
| <i>enable</i> | true to enable, false to disable. |

#### 18.2.6.7 `static uint32_t FLEXIO_ReadPinInput ( FLEXIO_Type * base ) [inline], [static]`

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | FlexIO peripheral base address |
|-------------|--------------------------------|

Returns

FlexIO pin input data

#### 18.2.6.8 `static uint8_t FLEXIO_GetShifterState ( FLEXIO_Type * base ) [inline], [static]`

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | FlexIO peripheral base address |
|-------------|--------------------------------|

Returns

current State pointer

#### 18.2.6.9 void FLEXIO\_SetShifterConfig ( FLEXIO\_Type \* *base*, uint8\_t *index*, const flexio\_shifter\_config\_t \* *shifterConfig* )

The configuration structure covers both the SHIFTCTL and SHIFTCFG registers. To configure the shifter to the proper mode, select which timer controls the shifter to shift, whether to generate start bit/stop bit, and the polarity of start bit and stop bit.

Example

```
flexio_shifter_config_t config = {
 .timerSelect = 0,
 .timerPolarity = kFLEXIO_ShifterTimerPolarityOnPositive,
 .pinConfig = kFLEXIO_PinConfigOpenDrainOrBidirection,
 .pinPolarity = kFLEXIO_PinActiveLow,
 .shifterMode = kFLEXIO_ShifterModeTransmit,
 .inputSource = kFLEXIO_ShifterInputFromPin,
 .shifterStop = kFLEXIO_ShifterStopBitHigh,
 .shifterStart = kFLEXIO_ShifterStartBitLow
};
FLEXIO_SetShifterConfig(base, &config);
```

Parameters

|                      |                                                              |
|----------------------|--------------------------------------------------------------|
| <i>base</i>          | FlexIO peripheral base address                               |
| <i>index</i>         | Shifter index                                                |
| <i>shifterConfig</i> | Pointer to <a href="#">flexio_shifter_config_t</a> structure |

#### 18.2.6.10 void FLEXIO\_SetTimerConfig ( FLEXIO\_Type \* *base*, uint8\_t *index*, const flexio\_timer\_config\_t \* *timerConfig* )

The configuration structure covers both the TIMCTL and TIMCFG registers. To configure the timer to the proper mode, select trigger source for timer and the timer pin output and the timing for timer.

Example

```
flexio_timer_config_t config = {
 .triggerSelect = FLEXIO_TIMER_TRIGGER_SEL_SHIFTnSTAT(0),
 .triggerPolarity = kFLEXIO_TimerTriggerPolarityActiveLow,
 .triggerSource = kFLEXIO_TimerTriggerSourceInternal,
```

```

.pinConfig = kFLEXIO_PinConfigOpenDrainOrBidirection,
.pinSelect = 0,
.pinPolarity = kFLEXIO_PinActiveHigh,
.timerMode = kFLEXIO_TimerModeDual8BitBaudBit,
.timerOutput = kFLEXIO_TimerOutputZeroNotAffectedByReset,
.timerDecrement = kFLEXIO_TimerDecSrcOnFlexIOClockShiftTimerOutput

,
.timerReset = kFLEXIO_TimerResetOnTimerPinEqualToTimerOutput,
.timerDisable = kFLEXIO_TimerDisableOnTimerCompare,
.timerEnable = kFLEXIO_TimerEnableOnTriggerHigh,
.timerStop = kFLEXIO_TimerStopBitEnableOnTimerDisable,
.timerStart = kFLEXIO_TimerStartBitEnabled
};

FLEXIO_SetTimerConfig(base, &config);

```

#### Parameters

|                    |                                                             |
|--------------------|-------------------------------------------------------------|
| <i>base</i>        | FlexIO peripheral base address                              |
| <i>index</i>       | Timer index                                                 |
| <i>timerConfig</i> | Pointer to the <code>flexio_timer_config_t</code> structure |

#### 18.2.6.11 static void FLEXIO\_EnableShifterStatusInterrupts ( **FLEXIO\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

The interrupt generates when the corresponding SSF is set.

#### Parameters

|             |                                                                                   |
|-------------|-----------------------------------------------------------------------------------|
| <i>base</i> | FlexIO peripheral base address                                                    |
| <i>mask</i> | The shifter status mask which can be calculated by $(1 \ll \text{shifter index})$ |

#### Note

For multiple shifter status interrupt enable, for example, two shifter status enable, can calculate the mask by using  $((1 \ll \text{shifter index}0) | (1 \ll \text{shifter index}1))$

#### 18.2.6.12 static void FLEXIO\_DisableShifterStatusInterrupts ( **FLEXIO\_Type** \* *base*, **uint32\_t** *mask* ) [inline], [static]

The interrupt won't generate when the corresponding SSF is set.

Parameters

|             |                                                                                    |
|-------------|------------------------------------------------------------------------------------|
| <i>base</i> | FlexIO peripheral base address                                                     |
| <i>mask</i> | The shifter status mask which can be calculated by ( $1 << \text{shifter index}$ ) |

Note

For multiple shifter status interrupt enable, for example, two shifter status enable, can calculate the mask by using  $((1 << \text{shifter index}0) | (1 << \text{shifter index}1))$

#### 18.2.6.13 static void FLEXIO\_EnableShifterErrorInterrupts ( FLEXIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

The interrupt generates when the corresponding SEF is set.

Parameters

|             |                                                                                   |
|-------------|-----------------------------------------------------------------------------------|
| <i>base</i> | FlexIO peripheral base address                                                    |
| <i>mask</i> | The shifter error mask which can be calculated by ( $1 << \text{shifter index}$ ) |

Note

For multiple shifter error interrupt enable, for example, two shifter error enable, can calculate the mask by using  $((1 << \text{shifter index}0) | (1 << \text{shifter index}1))$

#### 18.2.6.14 static void FLEXIO\_DisableShifterErrorInterrupts ( FLEXIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

The interrupt won't generate when the corresponding SEF is set.

Parameters

|             |                                                                                   |
|-------------|-----------------------------------------------------------------------------------|
| <i>base</i> | FlexIO peripheral base address                                                    |
| <i>mask</i> | The shifter error mask which can be calculated by ( $1 << \text{shifter index}$ ) |

Note

For multiple shifter error interrupt enable, for example, two shifter error enable, can calculate the mask by using  $((1 << \text{shifter index}0) | (1 << \text{shifter index}1))$

**18.2.6.15 static void FLEXIO\_EnableTimerStatusInterrupts ( FLEXIO\_Type \* *base*,  
                  uint32\_t *mask* ) [inline], [static]**

The interrupt generates when the corresponding SSF is set.

Parameters

|             |                                                                                |
|-------------|--------------------------------------------------------------------------------|
| <i>base</i> | FlexIO peripheral base address                                                 |
| <i>mask</i> | The timer status mask which can be calculated by ( $1 << \text{timer index}$ ) |

Note

For multiple timer status interrupt enable, for example, two timer status enable, can calculate the mask by using  $((1 << \text{timer index}0) | (1 << \text{timer index}1))$

#### 18.2.6.16 static void FLEXIO\_DisableTimerStatusInterrupts ( FLEXIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

The interrupt won't generate when the corresponding SSF is set.

Parameters

|             |                                                                                |
|-------------|--------------------------------------------------------------------------------|
| <i>base</i> | FlexIO peripheral base address                                                 |
| <i>mask</i> | The timer status mask which can be calculated by ( $1 << \text{timer index}$ ) |

Note

For multiple timer status interrupt enable, for example, two timer status enable, can calculate the mask by using  $((1 << \text{timer index}0) | (1 << \text{timer index}1))$

#### 18.2.6.17 static uint32\_t FLEXIO\_GetShifterStatusFlags ( FLEXIO\_Type \* *base* ) [inline], [static]

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | FlexIO peripheral base address |
|-------------|--------------------------------|

Returns

Shifter status flags

#### 18.2.6.18 static void FLEXIO\_ClearShifterStatusFlags ( FLEXIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

|             |                                                                                    |
|-------------|------------------------------------------------------------------------------------|
| <i>base</i> | FlexIO peripheral base address                                                     |
| <i>mask</i> | The shifter status mask which can be calculated by ( $1 << \text{shifter index}$ ) |

Note

For clearing multiple shifter status flags, for example, two shifter status flags, can calculate the mask by using  $((1 << \text{shifter index}0) | (1 << \text{shifter index}1))$

#### 18.2.6.19 static uint32\_t FLEXIO\_GetShifterErrorFlags ( FLEXIO\_Type \* *base* ) [inline], [static]

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | FlexIO peripheral base address |
|-------------|--------------------------------|

Returns

Shifter error flags

#### 18.2.6.20 static void FLEXIO\_ClearShifterErrorFlags ( FLEXIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

|             |                                                                                   |
|-------------|-----------------------------------------------------------------------------------|
| <i>base</i> | FlexIO peripheral base address                                                    |
| <i>mask</i> | The shifter error mask which can be calculated by ( $1 << \text{shifter index}$ ) |

Note

For clearing multiple shifter error flags, for example, two shifter error flags, can calculate the mask by using  $((1 << \text{shifter index}0) | (1 << \text{shifter index}1))$

#### 18.2.6.21 static uint32\_t FLEXIO\_GetTimerStatusFlags ( FLEXIO\_Type \* *base* ) [inline], [static]

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | FlexIO peripheral base address |
|-------------|--------------------------------|

Returns

Timer status flags

#### **18.2.6.22 static void FLEXIO\_ClearTimerStatusFlags ( FLEXIO\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

Parameters

|             |                                                                              |
|-------------|------------------------------------------------------------------------------|
| <i>base</i> | FlexIO peripheral base address                                               |
| <i>mask</i> | The timer status mask which can be calculated by $(1 << \text{timer index})$ |

Note

For clearing multiple timer status flags, for example, two timer status flags, can calculate the mask by using  $((1 << \text{timer index}0) | (1 << \text{timer index}1))$

#### **18.2.6.23 static void FLEXIO\_EnableShifterStatusDMA ( FLEXIO\_Type \* *base*, uint32\_t *mask*, bool *enable* ) [inline], [static]**

The DMA request generates when the corresponding SSF is set.

Note

For multiple shifter status DMA enables, for example, calculate the mask by using  $((1 << \text{shifter index}0) | (1 << \text{shifter index}1))$

Parameters

|             |                                                                                  |
|-------------|----------------------------------------------------------------------------------|
| <i>base</i> | FlexIO peripheral base address                                                   |
| <i>mask</i> | The shifter status mask which can be calculated by $(1 << \text{shifter index})$ |

|               |                                   |
|---------------|-----------------------------------|
| <i>enable</i> | True to enable, false to disable. |
|---------------|-----------------------------------|

### 18.2.6.24 **uint32\_t FLEXIO\_GetShifterBufferAddress ( FLEXIO\_Type \* *base*, flexio\_shifter\_buffer\_type\_t *type*, uint8\_t *index* )**

Parameters

|              |                                              |
|--------------|----------------------------------------------|
| <i>base</i>  | FlexIO peripheral base address               |
| <i>type</i>  | Shifter type of flexio_shifter_buffer_type_t |
| <i>index</i> | Shifter index                                |

Returns

Corresponding shifter buffer index

### 18.2.6.25 **status\_t FLEXIO\_RegisterHandleIRQ ( void \* *base*, void \* *handle*, flexio\_isr\_t *isr* )**

Parameters

|               |                                                         |
|---------------|---------------------------------------------------------|
| <i>base</i>   | Pointer to the FlexIO simulated peripheral type.        |
| <i>handle</i> | Pointer to the handler for FlexIO simulated peripheral. |
| <i>isr</i>    | FlexIO simulated peripheral interrupt handler.          |

Return values

|                           |                                                |
|---------------------------|------------------------------------------------|
| <i>kStatus_Success</i>    | Successfully create the handle.                |
| <i>kStatus_OutOfRange</i> | The FlexIO type/handle/ISR table out of range. |

### 18.2.6.26 **status\_t FLEXIO\_UnregisterHandleIRQ ( void \* *base* )**

Parameters

|             |                                                  |
|-------------|--------------------------------------------------|
| <i>base</i> | Pointer to the FlexIO simulated peripheral type. |
|-------------|--------------------------------------------------|

Return values

|                           |                                                |
|---------------------------|------------------------------------------------|
| <i>kStatus_Success</i>    | Successfully create the handle.                |
| <i>kStatus_OutOfRange</i> | The FlexIO type/handle/ISR table out of range. |

## 18.2.7 Variable Documentation

### 18.2.7.1 **FLEXIO\_Type\* const s\_flexioBases[]**

### 18.2.7.2 **const clock\_ip\_name\_t s\_flexioClocks[]**

## 18.3 FlexIO I2C Master Driver

### 18.3.1 Overview

The MCUXpresso SDK provides a peripheral driver for I2C master function using Flexible I/O module of MCUXpresso SDK devices.

The FlexIO I2C master driver includes functional APIs and transactional APIs.

Functional APIs target low level APIs. Functional APIs can be used for the FlexIO I2C master initialization/configuration/operation for the optimization/customization purpose. Using the functional APIs requires the knowledge of the FlexIO I2C master peripheral and how to organize functional APIs to meet the application requirements. The FlexIO I2C master functional operation groups provide the functional APIs set.

Transactional APIs target high-level APIs. The transactional APIs can be used to enable the peripheral quickly and also in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code using the functional APIs or accessing the hardware registers.

Transactional APIs support an asynchronous transfer. This means that the functions [FLEXIO\\_I2C\\_MasterTransferNonBlocking\(\)](#) set up the interrupt non-blocking transfer. When the transfer completes, the upper layer is notified through a callback function with the kStatus\_Success status.

### 18.3.2 Typical use case

#### 18.3.2.1 FlexIO I2C master transfer using an interrupt method

```
flexio_i2c_master_handle_t g_m_handle;
flexio_i2c_master_config_t masterConfig;
flexio_i2c_master_transfer_t masterXfer;
volatile bool completionFlag = false;
const uint8_t sendData[] = [.....];
FLEXIO_I2C_Type i2cDev;

void FLEXIO_I2C_MasterCallback(FLEXIO_I2C_Type *base, status_t status, void *
 userData)
{
 userData = userData;

 if (kStatus_Success == status)
 {
 completionFlag = true;
 }
}

void main(void)
{
 //...

 FLEXIO_I2C_MasterGetDefaultConfig(&masterConfig);

 FLEXIO_I2C_MasterInit(&i2cDev, &user_config);
 FLEXIO_I2C_MasterTransferCreateHandle(&i2cDev, &g_m_handle,
 FLEXIO_I2C_MasterCallback, NULL);
}
```

```

// Prepares to send.
masterXfer.slaveAddress = g_accel_address[0];
masterXfer.direction = kI2C_Read;
masterXfer.subaddress = &who_am_i_reg;
masterXfer.subaddressSize = 1;
masterXfer.data = &who_am_i_value;
masterXfer.dataSize = 1;
masterXfer.flags = kI2C_TransferDefaultFlag;

// Sends out.
FLEXIO_I2C_MasterTransferNonBlocking(&i2cDev, &g_m_handle, &
 masterXfer);

// Wait for sending is complete.
while (!completionFlag)
{
}

// ...
}

```

## Data Structures

- struct **FLEXIO\_I2C\_Type**  
*Define FlexIO I2C master access structure typedef.* [More...](#)
- struct **flexio\_i2c\_master\_config\_t**  
*Define FlexIO I2C master user configuration structure.* [More...](#)
- struct **flexio\_i2c\_master\_transfer\_t**  
*Define FlexIO I2C master transfer structure.* [More...](#)
- struct **flexio\_i2c\_master\_handle\_t**  
*Define FlexIO I2C master handle structure.* [More...](#)

## Macros

- #define **I2C\_RETRY\_TIMES** 0U /\* Define to zero means keep waiting until the flag is assert/deassert. \*/  
*Retry times for waiting flag.*

## TypeDefs

- typedef void(\* **flexio\_i2c\_master\_transfer\_callback\_t** )(FLEXIO\_I2C\_Type \*base, flexio\_i2c\_master\_handle\_t \*handle, **status\_t** status, void \*userData)  
*FlexIO I2C master transfer callback typedef.*

## Enumerations

- enum {
 **kStatus\_FLEXIO\_I2C\_Busy** = MAKE\_STATUS(kStatusGroup\_FLEXIO\_I2C, 0),
 **kStatus\_FLEXIO\_I2C\_Idle** = MAKE\_STATUS(kStatusGroup\_FLEXIO\_I2C, 1),
 **kStatus\_FLEXIO\_I2C\_Nak** = MAKE\_STATUS(kStatusGroup\_FLEXIO\_I2C, 2),
 }

- ```

kStatus_FLEXIO_I2C_Timeout = MAKE_STATUS(kStatusGroup_FLEXIO_I2C, 3) }

FlexIO I2C transfer status.
• enum _flexio_i2c_master_interrupt {
    kFLEXIO_I2C_TxEmptyInterruptEnable = 0x1U,
    kFLEXIO_I2C_RxFullInterruptEnable = 0x2U }

Define FlexIO I2C master interrupt mask.
• enum _flexio_i2c_master_status_flags {
    kFLEXIO_I2C_TxEmptyFlag = 0x1U,
    kFLEXIO_I2C_RxFullFlag = 0x2U,
    kFLEXIO_I2C_ReceiveNakFlag = 0x4U }

Define FlexIO I2C master status mask.
• enum flexio_i2c_direction_t {
    kFLEXIO_I2C_Write = 0x0U,
    kFLEXIO_I2C_Read = 0x1U }

Direction of master transfer.

```

Driver version

- #define FSL_FLEXIO_I2C_MASTER_DRIVER_VERSION (MAKE_VERSION(2, 4, 0))

Initialization and deinitialization

- status_t FLEXIO_I2C_CheckForBusyBus (FLEXIO_I2C_Type *base)

Make sure the bus isn't already pulled down.
- status_t FLEXIO_I2C_MasterInit (FLEXIO_I2C_Type *base, flexio_i2c_master_config_t *masterConfig, uint32_t srcClock_Hz)

Ungates the FlexIO clock, resets the FlexIO module, and configures the FlexIO I2C hardware configuration.
- void FLEXIO_I2C_MasterDeinit (FLEXIO_I2C_Type *base)

De-initializes the FlexIO I2C master peripheral.
- void FLEXIO_I2C_MasterGetDefaultConfig (flexio_i2c_master_config_t *masterConfig)

Gets the default configuration to configure the FlexIO module.
- static void FLEXIO_I2C_MasterEnable (FLEXIO_I2C_Type *base, bool enable)

Enables/disables the FlexIO module operation.

Status

- uint32_t FLEXIO_I2C_MasterGetStatusFlags (FLEXIO_I2C_Type *base)

Gets the FlexIO I2C master status flags.
- void FLEXIO_I2C_MasterClearStatusFlags (FLEXIO_I2C_Type *base, uint32_t mask)

Clears the FlexIO I2C master status flags.

Interrupts

- void FLEXIO_I2C_MasterEnableInterrupts (FLEXIO_I2C_Type *base, uint32_t mask)

- Enables the FlexIO i2c master interrupt requests.
- void **FLEXIO_I2C_MasterDisableInterrupts** (**FLEXIO_I2C_Type** *base, **uint32_t** mask)
Disables the FlexIO I2C master interrupt requests.

Bus Operations

- void **FLEXIO_I2C_MasterSetBaudRate** (**FLEXIO_I2C_Type** *base, **uint32_t** baudRate_Bps, **uint32_t** srcClock_Hz)
Sets the FlexIO I2C master transfer baudrate.
- void **FLEXIO_I2C_MasterStart** (**FLEXIO_I2C_Type** *base, **uint8_t** address, **flexio_i2c_direction_t** direction)
Sends START + 7-bit address to the bus.
- void **FLEXIO_I2C_MasterStop** (**FLEXIO_I2C_Type** *base)
Sends the stop signal on the bus.
- void **FLEXIO_I2C_MasterRepeatedStart** (**FLEXIO_I2C_Type** *base)
Sends the repeated start signal on the bus.
- void **FLEXIO_I2C_MasterAbortStop** (**FLEXIO_I2C_Type** *base)
Sends the stop signal when transfer is still on-going.
- void **FLEXIO_I2C_MasterEnableAck** (**FLEXIO_I2C_Type** *base, **bool** enable)
Configures the sent ACK/NAK for the following byte.
- **status_t FLEXIO_I2C_MasterSetTransferCount** (**FLEXIO_I2C_Type** *base, **uint16_t** count)
Sets the number of bytes to be transferred from a start signal to a stop signal.
- static void **FLEXIO_I2C_MasterWriteByte** (**FLEXIO_I2C_Type** *base, **uint32_t** data)
Writes one byte of data to the I2C bus.
- static **uint8_t FLEXIO_I2C_MasterReadByte** (**FLEXIO_I2C_Type** *base)
Reads one byte of data from the I2C bus.
- **status_t FLEXIO_I2C_MasterWriteBlocking** (**FLEXIO_I2C_Type** *base, **const uint8_t** *txBuff, **uint8_t** txSize)
Sends a buffer of data in bytes.
- **status_t FLEXIO_I2C_MasterReadBlocking** (**FLEXIO_I2C_Type** *base, **uint8_t** *rxBuff, **uint8_t** rxSize)
Receives a buffer of bytes.
- **status_t FLEXIO_I2C_MasterTransferBlocking** (**FLEXIO_I2C_Type** *base, **flexio_i2c_master_transfer_t** *xfer)
Performs a master polling transfer on the I2C bus.

Transactional

- **status_t FLEXIO_I2C_MasterTransferCreateHandle** (**FLEXIO_I2C_Type** *base, **flexio_i2c_master_handle_t** *handle, **flexio_i2c_master_transfer_callback_t** callback, **void** *userData)
Initializes the I2C handle which is used in transactional functions.
- **status_t FLEXIO_I2C_MasterTransferNonBlocking** (**FLEXIO_I2C_Type** *base, **flexio_i2c_master_handle_t** *handle, **flexio_i2c_master_transfer_t** *xfer)
Performs a master interrupt non-blocking transfer on the I2C bus.
- **status_t FLEXIO_I2C_MasterTransferGetCount** (**FLEXIO_I2C_Type** *base, **flexio_i2c_master_handle_t** *handle, **size_t** *count)
Gets the master transfer status during a interrupt non-blocking transfer.

- void **FLEXIO_I2C_MasterTransferAbort** (**FLEXIO_I2C_Type** *base, **flexio_i2c_master_handle_t** *handle)
Aborts an interrupt non-blocking transfer early.
- void **FLEXIO_I2C_MasterTransferHandleIRQ** (void *i2cType, void *i2cHandle)
Master interrupt handler.

18.3.3 Data Structure Documentation

18.3.3.1 struct FLEXIO_I2C_Type

Data Fields

- **FLEXIO_Type** * **flexioBase**
FlexIO base pointer.
- **uint8_t** **SDAPinIndex**
Pin select for I2C SDA.
- **uint8_t** **SCLPinIndex**
Pin select for I2C SCL.
- **uint8_t** **shifterIndex** [2]
Shifter index used in FlexIO I2C.
- **uint8_t** **timerIndex** [3]
Timer index used in FlexIO I2C.
- **uint32_t** **baudrate**
Master transfer baudrate, used to calculate delay time.

Field Documentation

- (1) **FLEXIO_Type*** **FLEXIO_I2C_Type::flexioBase**
- (2) **uint8_t** **FLEXIO_I2C_Type::SDAPinIndex**
- (3) **uint8_t** **FLEXIO_I2C_Type::SCLPinIndex**
- (4) **uint8_t** **FLEXIO_I2C_Type::shifterIndex[2]**
- (5) **uint8_t** **FLEXIO_I2C_Type::timerIndex[3]**
- (6) **uint32_t** **FLEXIO_I2C_Type::baudrate**

18.3.3.2 struct flexio_i2c_master_config_t

Data Fields

- **bool** **enableMaster**
Enables the FlexIO I2C peripheral at initialization time.
- **bool** **enableInDoze**
Enable/disable FlexIO operation in doze mode.
- **bool** **enableInDebug**
Enable/disable FlexIO operation in debug mode.

- bool `enableFastAccess`
Enable/disable fast access to FlexIO registers, fast access requires
the FlexIO clock to be at least twice the frequency of the bus clock.
- uint32_t `baudRate_Bps`
Baud rate in Bps.

Field Documentation

- (1) `bool flexio_i2c_master_config_t::enableMaster`
- (2) `bool flexio_i2c_master_config_t::enableInDoze`
- (3) `bool flexio_i2c_master_config_t::enableInDebug`
- (4) `bool flexio_i2c_master_config_t::enableFastAccess`
- (5) `uint32_t flexio_i2c_master_config_t::baudRate_Bps`

18.3.3.3 struct flexio_i2c_master_transfer_t

Data Fields

- uint32_t `flags`
Transfer flag which controls the transfer, reserved for FlexIO I2C.
- uint8_t `slaveAddress`
7-bit slave address.
- `flexio_i2c_direction_t direction`
Transfer direction, read or write.
- uint32_t `subaddress`
Sub address.
- uint8_t `subaddressSize`
Size of command buffer.
- uint8_t volatile * `data`
Transfer buffer.
- volatile size_t `dataSize`
Transfer size.

Field Documentation

- (1) `uint32_t flexio_i2c_master_transfer_t::flags`
- (2) `uint8_t flexio_i2c_master_transfer_t::slaveAddress`
- (3) `flexio_i2c_direction_t flexio_i2c_master_transfer_t::direction`
- (4) `uint32_t flexio_i2c_master_transfer_t::subaddress`
Transferred MSB first.
- (5) `uint8_t flexio_i2c_master_transfer_t::subaddressSize`

- (6) `uint8_t volatile* flexio_i2c_master_transfer_t::data`
- (7) `volatile size_t flexio_i2c_master_transfer_t::dataSize`

18.3.3.4 struct _flexio_i2c_master_handle

FlexIO I2C master handle typedef.

Data Fields

- `flexio_i2c_master_transfer_t transfer`
FlexIO I2C master transfer copy.
- `size_t transferSize`
Total bytes to be transferred.
- `uint8_t state`
Transfer state maintained during transfer.
- `flexio_i2c_master_transfer_callback_t completionCallback`
Callback function called at transfer event.
- `void *userData`
Callback parameter passed to callback function.
- `bool needRestart`
Whether master needs to send re-start signal.

Field Documentation

- (1) `flexio_i2c_master_transfer_t flexio_i2c_master_handle_t::transfer`
- (2) `size_t flexio_i2c_master_handle_t::transferSize`
- (3) `uint8_t flexio_i2c_master_handle_t::state`
- (4) `flexio_i2c_master_transfer_callback_t flexio_i2c_master_handle_t::completionCallback`

Callback function called at transfer event.

- (5) `void* flexio_i2c_master_handle_t::userData`
- (6) `bool flexio_i2c_master_handle_t::needRestart`

18.3.4 Macro Definition Documentation

- 18.3.4.1 `#define I2C_RETRY_TIMES 0U /* Define to zero means keep waiting until the flag is assert/deassert. */`

18.3.5 Typedef Documentation

18.3.5.1 `typedef void(* flexio_i2c_master_transfer_callback_t)(FLEXIO_I2C_Type *base, flexio_i2c_master_handle_t *handle, status_t status, void *userData)`

18.3.6 Enumeration Type Documentation

18.3.6.1 anonymous enum

Enumerator

kStatus_FLEXIO_I2C_Busy I2C is busy doing transfer.

kStatus_FLEXIO_I2C_Idle I2C is busy doing transfer.

kStatus_FLEXIO_I2C_Nak NAK received during transfer.

kStatus_FLEXIO_I2C_Timeout Timeout polling status flags.

18.3.6.2 `enum _flexio_i2c_master_interrupt`

Enumerator

kFLEXIO_I2C_TxEmptyInterruptEnable Tx buffer empty interrupt enable.

kFLEXIO_I2C_RxFullInterruptEnable Rx buffer full interrupt enable.

18.3.6.3 `enum _flexio_i2c_master_status_flags`

Enumerator

kFLEXIO_I2C_TxEmptyFlag Tx shifter empty flag.

kFLEXIO_I2C_RxFullFlag Rx shifter full/Transfer complete flag.

kFLEXIO_I2C_ReceiveNakFlag Receive NAK flag.

18.3.6.4 `enum flexio_i2c_direction_t`

Enumerator

kFLEXIO_I2C_Write Master send to slave.

kFLEXIO_I2C_Read Master receive from slave.

18.3.7 Function Documentation

18.3.7.1 `status_t FLEXIO_I2C_CheckForBusyBus (FLEXIO_I2C_Type * base)`

Check the FLEXIO pin status to see whether either of SDA and SCL pin is pulled down.

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure..
-------------	--

Return values

<i>kStatus_Success</i>	
<i>kStatus_FLEXIO_I2C_Busy</i>	

18.3.7.2 status_t [FLEXIO_I2C_MasterInit](#) ([FLEXIO_I2C_Type](#) * *base*, [flexio_i2c_master_config_t](#) * *masterConfig*, [uint32_t](#) *srcClock_Hz*)

Example

```
FLEXIO_I2C_Type base = {
    .flexioBase = FLEXIO,
    .SDAPinIndex = 0,
    .SCLPinIndex = 1,
    .shifterIndex = {0,1},
    .timerIndex = {0,1}
};
flexio_i2c_master_config_t config = {
    .enableInDoze = false,
    .enableInDebug = true,
    .enableFastAccess = false,
    .baudRate_Bps = 100000
};
FLEXIO_I2C_MasterInit(base, &config, srcClock_Hz);
```

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
<i>masterConfig</i>	Pointer to flexio_i2c_master_config_t structure.
<i>srcClock_Hz</i>	FlexIO source clock in Hz.

Return values

<i>kStatus_Success</i>	Initialization successful
<i>kStatus_InvalidArgument</i>	The source clock exceed upper range limitation

18.3.7.3 void [FLEXIO_I2C_MasterDeinit](#) ([FLEXIO_I2C_Type](#) * *base*)

Calling this API Resets the FlexIO I2C master shifer and timer config, module can't work unless the [FLEXIO_I2C_MasterInit](#) is called.

Parameters

<i>base</i>	pointer to FLEXIO_I2C_Type structure.
-------------	---

18.3.7.4 void [FLEXIO_I2C_MasterGetDefaultConfig](#) ([flexio_i2c_master_config_t](#) * *masterConfig*)

The configuration can be used directly for calling the [FLEXIO_I2C_MasterInit\(\)](#).

Example:

```
flexio_i2c_master_config_t config;
FLEXIO\_I2C\_MasterGetDefaultConfig(&config);
```

Parameters

<i>masterConfig</i>	Pointer to flexio_i2c_master_config_t structure.
---------------------	--

18.3.7.5 static void [FLEXIO_I2C_MasterEnable](#) ([FLEXIO_I2C_Type](#) * *base*, [bool](#) *enable*) [inline], [static]

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
<i>enable</i>	Pass true to enable module, false does not have any effect.

18.3.7.6 [uint32_t FLEXIO_I2C_MasterGetStatusFlags](#) ([FLEXIO_I2C_Type](#) * *base*)

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure
-------------	--

Returns

Status flag, use status flag to AND [_flexio_i2c_master_status_flags](#) can get the related status.

18.3.7.7 void [FLEXIO_I2C_MasterClearStatusFlags](#) ([FLEXIO_I2C_Type](#) * *base*, [uint32_t](#) *mask*)

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
<i>mask</i>	Status flag. The parameter can be any combination of the following values: <ul style="list-style-type: none"> • kFLEXIO_I2C_RxFullFlag • kFLEXIO_I2C_ReceiveNakFlag

18.3.7.8 void FLEXIO_I2C_MasterEnableInterrupts ([FLEXIO_I2C_Type](#) * *base*, [uint32_t](#) *mask*)

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
<i>mask</i>	Interrupt source. Currently only one interrupt request source: <ul style="list-style-type: none"> • kFLEXIO_I2C_TransferCompleteInterruptEnable

18.3.7.9 void FLEXIO_I2C_MasterDisableInterrupts ([FLEXIO_I2C_Type](#) * *base*, [uint32_t](#) *mask*)

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
<i>mask</i>	Interrupt source.

18.3.7.10 void FLEXIO_I2C_MasterSetBaudRate ([FLEXIO_I2C_Type](#) * *base*, [uint32_t](#) *baudRate_Bps*, [uint32_t](#) *srcClock_Hz*)

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure
<i>baudRate_Bps</i>	the baud rate value in HZ

<i>srcClock_Hz</i>	source clock in HZ
--------------------	--------------------

18.3.7.11 void FLEXIO_I2C_MasterStart (FLEXIO_I2C_Type * *base*, uint8_t *address*, flexio_i2c_direction_t *direction*)

Note

This API should be called when the transfer configuration is ready to send a START signal and 7-bit address to the bus. This is a non-blocking API, which returns directly after the address is put into the data register but the address transfer is not finished on the bus. Ensure that the kFLEXIO_I2C_RxFullFlag status is asserted before calling this API.

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
<i>address</i>	7-bit address.
<i>direction</i>	transfer direction. This parameter is one of the values in flexio_i2c_direction_t : <ul style="list-style-type: none"> • kFLEXIO_I2C_Write: Transmit • kFLEXIO_I2C_Read: Receive

18.3.7.12 void FLEXIO_I2C_MasterStop (FLEXIO_I2C_Type * *base*)

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
-------------	---

18.3.7.13 void FLEXIO_I2C_MasterRepeatedStart (FLEXIO_I2C_Type * *base*)

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
-------------	---

18.3.7.14 void FLEXIO_I2C_MasterAbortStop (FLEXIO_I2C_Type * *base*)

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
-------------	---

18.3.7.15 void FLEXIO_I2C_MasterEnableAck ([FLEXIO_I2C_Type](#) * *base*, *bool enable*)

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
<i>enable</i>	True to configure send ACK, false configure to send NAK.

18.3.7.16 status_t FLEXIO_I2C_MasterSetTransferCount ([FLEXIO_I2C_Type](#) * *base*, [uint16_t](#) *count*)

Note

Call this API before a transfer begins because the timer generates a number of clocks according to the number of bytes that need to be transferred.

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
<i>count</i>	Number of bytes need to be transferred from a start signal to a re-start/stop signal

Return values

<i>kStatus_Success</i>	Successfully configured the count.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.

18.3.7.17 static void FLEXIO_I2C_MasterWriteByte ([FLEXIO_I2C_Type](#) * *base*, [uint32_t](#) *data*) [inline], [static]

Note

This is a non-blocking API, which returns directly after the data is put into the data register but the data transfer is not finished on the bus. Ensure that the TxEmptyFlag is asserted before calling this API.

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
<i>data</i>	a byte of data.

18.3.7.18 static uint8_t FLEXIO_I2C_MasterReadByte ([FLEXIO_I2C_Type](#) * *base*) [[inline](#)], [[static](#)]

Note

This is a non-blocking API, which returns directly after the data is read from the data register. Ensure that the data is ready in the register.

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
-------------	---

Returns

data byte read.

18.3.7.19 status_t FLEXIO_I2C_MasterWriteBlocking ([FLEXIO_I2C_Type](#) * *base*, const uint8_t * *txBuff*, uint8_t *txSize*)

Note

This function blocks via polling until all bytes have been sent.

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
<i>txBuff</i>	The data bytes to send.
<i>txSize</i>	The number of data bytes to send.

Return values

<i>kStatus_Success</i>	Successfully write data.
<i>kStatus_FLEXIO_I2C_-Nak</i>	Receive NAK during writing data.
<i>kStatus_FLEXIO_I2C_-Timeout</i>	Timeout polling status flags.

18.3.7.20 status_t FLEXIO_I2C_MasterReadBlocking (**FLEXIO_I2C_Type * base,** **uint8_t * rxBuff, uint8_t rxSize**)

Note

This function blocks via polling until all bytes have been received.

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
<i>rxBuff</i>	The buffer to store the received bytes.
<i>rxSize</i>	The number of data bytes to be received.

Return values

<i>kStatus_Success</i>	Successfully read data.
<i>kStatus_FLEXIO_I2C_- Timeout</i>	Timeout polling status flags.

18.3.7.21 status_t FLEXIO_I2C_MasterTransferBlocking (**FLEXIO_I2C_Type * base,** **flexio_i2c_master_transfer_t * xfer**)

Note

The API does not return until the transfer succeeds or fails due to receiving NAK.

Parameters

<i>base</i>	pointer to FLEXIO_I2C_Type structure.
<i>xfer</i>	pointer to flexio_i2c_master_transfer_t structure.

Returns

status of `status_t`.

18.3.7.22 status_t FLEXIO_I2C_MasterTransferCreateHandle (**FLEXIO_I2C_Type * base,** **flexio_i2c_master_handle_t * handle, flexio_i2c_master_transfer_callback_t callback, void * userData**)

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
<i>handle</i>	Pointer to flexio_i2c_master_handle_t structure to store the transfer state.
<i>callback</i>	Pointer to user callback function.
<i>userData</i>	User param passed to the callback function.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO type/handle/isr table out of range.

18.3.7.23 status_t FLEXIO_I2C_MasterTransferNonBlocking ([FLEXIO_I2C_Type](#) * *base*, [flexio_i2c_master_handle_t](#) * *handle*, [flexio_i2c_master_transfer_t](#) * *xfer*)

Note

The API returns immediately after the transfer initiates. Call [FLEXIO_I2C_MasterTransferGetCount](#) to poll the transfer status to check whether the transfer is finished. If the return status is not [kStatus_FLEXIO_I2C_Busy](#), the transfer is finished.

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure
<i>handle</i>	Pointer to flexio_i2c_master_handle_t structure which stores the transfer state
<i>xfer</i>	pointer to flexio_i2c_master_transfer_t structure

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_FLEXIO_I2C_Busy</i>	FlexIO I2C is not idle, is running another transfer.

18.3.7.24 status_t FLEXIO_I2C_MasterTransferGetCount ([FLEXIO_I2C_Type](#) * *base*, [flexio_i2c_master_handle_t](#) * *handle*, [size_t](#) * *count*)

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure.
<i>handle</i>	Pointer to flexio_i2c_master_handle_t structure which stores the transfer state.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Return values

<i>kStatus_InvalidArgument</i>	count is Invalid.
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.
<i>kStatus_Success</i>	Successfully return the count.

18.3.7.25 void FLEXIO_I2C_MasterTransferAbort ([FLEXIO_I2C_Type](#) * *base*, [flexio_i2c_master_handle_t](#) * *handle*)

Note

This API can be called at any time when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	Pointer to FLEXIO_I2C_Type structure
<i>handle</i>	Pointer to flexio_i2c_master_handle_t structure which stores the transfer state

18.3.7.26 void FLEXIO_I2C_MasterTransferHandleIRQ ([void](#) * *i2cType*, [void](#) * *i2cHandle*)

Parameters

<i>i2cType</i>	Pointer to FLEXIO_I2C_Type structure
<i>i2cHandle</i>	Pointer to flexio_i2c_master_transfer_t structure

18.4 FlexIO I2S Driver

18.4.1 Overview

The MCUXpresso SDK provides a peripheral driver for I2S function using Flexible I/O module of MCUXpresso SDK devices.

The FlexIO I2S driver includes functional APIs and transactional APIs.

Functional APIs are feature/property target low level APIs.

Functional APIs can be used for FlexIO I2S initialization/configuration/operation for optimization/customization purpose. Using the functional API requires the knowledge of the FlexIO I2S peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. FlexIO I2S functional operation groups provide the functional APIs set.

Transactional APIs are transaction target high level APIs. The transactional APIs can be used to enable the peripheral and also in the application if the code size and performance of transactional APIs can satisfy requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code. All transactional APIs use the sai_handle_t as the first parameter. Initialize the handle by calling the FlexIO_I2S_TransferTxCreateHandle() or FlexIO_I2S_TransferRxCreateHandle() API.

Transactional APIs support asynchronous transfer. This means that the functions [FLEXIO_I2S_TransferSendNonBlocking\(\)](#) and [FLEXIO_I2S_TransferReceiveNonBlocking\(\)](#) set up an interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the kStatus_FLEXIO_I2S_TxIdle and kStatus_FLEXIO_I2S_RxIdle status.

18.4.2 Typical use case

18.4.2.1 FlexIO I2S send/receive using an interrupt method

```
sai_handle_t g_saiTxHandle;
sai_config_t user_config;
sai_transfer_t sendXfer;
volatile bool txFinished;
volatile bool rxFinished;
const uint8_t sendData[] = [.....];

void FLEXIO_I2S_UserCallback(sai_handle_t *handle, status_t status, void *userData)
{
    userData = userData;

    if (kStatus_FLEXIO_I2S_TxIdle == status)
    {
        txFinished = true;
    }
}

void main(void)
{
    //...

    FLEXIO_I2S_TxGetDefaultConfig(&user_config);
```

```

FLEXIO_I2S_TxInit(FLEXIO_I2S0, &user_config);
FLEXIO_I2S_TransferTxCreateHandle(FLEXIO_I2S0, &g_saiHandle,
    FLEXIO_I2S_UserCallback, NULL);

//Configures the SAI format.
FLEXIO_I2S_TransferTxSetTransferFormat(FLEXIO_I2S0, &g_saiHandle, mclkSource, mclk);

// Prepares to send.
sendXfer.data = sendData
sendXfer.dataSize = sizeof(sendData)/sizeof(sendData[0]);
txFinished = false;

// Sends out.
FLEXIO_I2S_TransferSendNonBlocking(FLEXIO_I2S0, &g_saiHandle, &
    sendXfer);

// Waiting to send is finished.
while (!txFinished)
{
}

// ...
}

```

18.4.2.2 FLEXIO_I2S send/receive using a DMA method

```

sai_handle_t g_saiHandle;
dma_handle_t g_saiTxDmaHandle;
dma_handle_t g_saiRxDmaHandle;
sai_config_t user_config;
sai_transfer_t sendXfer;
volatile bool txFinished;
uint8_t sendData[] = ...;

void FLEXIO_I2S_UserCallback(sai_handle_t *handle, status_t status, void *userData)
{
    userData = userData;

    if (kStatus_FLEXIO_I2S_TxIdle == status)
    {
        txFinished = true;
    }
}

void main(void)
{
    //...

    FLEXIO_I2S_TxGetDefaultConfig(&user_config);
    FLEXIO_I2S_TxInit(FLEXIO_I2S0, &user_config);

    // Sets up the DMA.
    DMAMUX_Init(DMAMUX0);
    DMAMUX_SetSource(DMAMUX0, FLEXIO_I2S_TX_DMA_CHANNEL, FLEXIO_I2S_TX_DMA_REQUEST);
    DMAMUX_EnableChannel(DMAMUX0, FLEXIO_I2S_TX_DMA_CHANNEL);

    DMA_Init(DMA0);

    /* Creates the DMA handle. */
    DMA_TransferTxCreateHandle(&g_saiTxDmaHandle, DMA0, FLEXIO_I2S_TX_DMA_CHANNEL);

    FLEXIO_I2S_TransferTxCreateHandleDMA(FLEXIO_I2S0, &g_saiTxDmaHandle, FLEXIO_I2S_UserCallback, NULL);

    // Prepares to send.
    sendXfer.data = sendData
}

```

```

sendXfer.dataSize = sizeof(sendData)/sizeof(sendData[0]);
txFinished = false;

// Sends out.
FLEXIO_I2S_TransferSendDMA(&g_saiHandle, &sendXfer);

// Waiting to send is finished.
while (!txFinished)
{
}

// ...
}

```

Data Structures

- struct [FLEXIO_I2S_Type](#)
Define FlexIO I2S access structure typedef. [More...](#)
- struct [flexio_i2s_config_t](#)
FlexIO I2S configure structure. [More...](#)
- struct [flexio_i2s_format_t](#)
FlexIO I2S audio format, FlexIO I2S only support the same format in Tx and Rx. [More...](#)
- struct [flexio_i2s_transfer_t](#)
Define FlexIO I2S transfer structure. [More...](#)
- struct [flexio_i2s_handle_t](#)
Define FlexIO I2S handle structure. [More...](#)

Macros

- #define [I2S_RETRY_TIMES](#) 0U /* Define to zero means keep waiting until the flag is assert/deassert. */
Retry times for waiting flag.
- #define [FLEXIO_I2S_XFER_QUEUE_SIZE](#) (4U)
FlexIO I2S transfer queue size, user can refine it according to use case.

Typedefs

- typedef void(* [flexio_i2s_callback_t](#))(FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, [status_t](#) status, void *userData)
FlexIO I2S xfer callback prototype.

Enumerations

- enum {

kStatus_FLEXIO_I2S_Idle = MAKE_STATUS(kStatusGroup_FLEXIO_I2S, 0),

kStatus_FLEXIO_I2S_TxBusy = MAKE_STATUS(kStatusGroup_FLEXIO_I2S, 1),

kStatus_FLEXIO_I2S_RxBusy = MAKE_STATUS(kStatusGroup_FLEXIO_I2S, 2),

kStatus_FLEXIO_I2S_Error = MAKE_STATUS(kStatusGroup_FLEXIO_I2S, 3),

kStatus_FLEXIO_I2S_QueueFull = MAKE_STATUS(kStatusGroup_FLEXIO_I2S, 4),

kStatus_FLEXIO_I2S_Timeout }

FlexIO I2S transfer status.
- enum **flexio_i2s_master_slave_t** {

kFLEXIO_I2S_Master = 0x0U,

kFLEXIO_I2S_Slave = 0x1U }

Master or slave mode.
- enum {

kFLEXIO_I2S_TxDataRegEmptyInterruptEnable = 0x1U,

kFLEXIO_I2S_RxDataRegFullInterruptEnable = 0x2U }

_flexio_i2s_interrupt_enable Define FlexIO I2S interrupt mask.
- enum {

kFLEXIO_I2S_TxDataRegEmptyFlag = 0x1U,

kFLEXIO_I2S_RxDataRegFullFlag = 0x2U }

_flexio_i2s_status_flags Define FlexIO I2S status mask.
- enum **flexio_i2s_sample_rate_t** {

kFLEXIO_I2S_SampleRate8KHz = 8000U,

kFLEXIO_I2S_SampleRate11025Hz = 11025U,

kFLEXIO_I2S_SampleRate12KHz = 12000U,

kFLEXIO_I2S_SampleRate16KHz = 16000U,

kFLEXIO_I2S_SampleRate22050Hz = 22050U,

kFLEXIO_I2S_SampleRate24KHz = 24000U,

kFLEXIO_I2S_SampleRate32KHz = 32000U,

kFLEXIO_I2S_SampleRate44100Hz = 44100U,

kFLEXIO_I2S_SampleRate48KHz = 48000U,

kFLEXIO_I2S_SampleRate96KHz = 96000U }

Audio sample rate.
- enum **flexio_i2s_word_width_t** {

kFLEXIO_I2S_WordWidth8bits = 8U,

kFLEXIO_I2S_WordWidth16bits = 16U,

kFLEXIO_I2S_WordWidth24bits = 24U,

kFLEXIO_I2S_WordWidth32bits = 32U }

Audio word width.

Driver version

- #define **FSL_FLEXIO_I2S_DRIVER_VERSION** (MAKE_VERSION(2, 2, 0))

FlexIO I2S driver version 2.2.0.

Initialization and deinitialization

- void **FLEXIO_I2S_Init** (**FLEXIO_I2S_Type** *base, const **flexio_i2s_config_t** *config)
Initializes the FlexIO I2S.
- void **FLEXIO_I2S_GetDefaultConfig** (**flexio_i2s_config_t** *config)
Sets the FlexIO I2S configuration structure to default values.
- void **FLEXIO_I2S_Deinit** (**FLEXIO_I2S_Type** *base)
De-initializes the FlexIO I2S.
- static void **FLEXIO_I2S_Enable** (**FLEXIO_I2S_Type** *base, bool enable)
Enables/disables the FlexIO I2S module operation.

Status

- uint32_t **FLEXIO_I2S_GetStatusFlags** (**FLEXIO_I2S_Type** *base)
Gets the FlexIO I2S status flags.

Interrupts

- void **FLEXIO_I2S_EnableInterrupts** (**FLEXIO_I2S_Type** *base, uint32_t mask)
Enables the FlexIO I2S interrupt.
- void **FLEXIO_I2S_DisableInterrupts** (**FLEXIO_I2S_Type** *base, uint32_t mask)
Disables the FlexIO I2S interrupt.

DMA Control

- static void **FLEXIO_I2S_TxEnableDMA** (**FLEXIO_I2S_Type** *base, bool enable)
Enables/disables the FlexIO I2S Tx DMA requests.
- static void **FLEXIO_I2S_RxEnableDMA** (**FLEXIO_I2S_Type** *base, bool enable)
Enables/disables the FlexIO I2S Rx DMA requests.
- static uint32_t **FLEXIO_I2S_TxGetDataRegisterAddress** (**FLEXIO_I2S_Type** *base)
Gets the FlexIO I2S send data register address.
- static uint32_t **FLEXIO_I2S_RxGetDataRegisterAddress** (**FLEXIO_I2S_Type** *base)
Gets the FlexIO I2S receive data register address.

Bus Operations

- void **FLEXIO_I2S_MasterSetFormat** (**FLEXIO_I2S_Type** *base, **flexio_i2s_format_t** *format, uint32_t srcClock_Hz)
Configures the FlexIO I2S audio format in master mode.
- void **FLEXIO_I2S_SlaveSetFormat** (**FLEXIO_I2S_Type** *base, **flexio_i2s_format_t** *format)
Configures the FlexIO I2S audio format in slave mode.
- status_t **FLEXIO_I2S_WriteBlocking** (**FLEXIO_I2S_Type** *base, uint8_t bitWidth, uint8_t *txData, size_t size)
Sends data using a blocking method.
- static void **FLEXIO_I2S_WriteData** (**FLEXIO_I2S_Type** *base, uint8_t bitWidth, uint32_t data)

- Writes data into a data register.
 • `status_t FLEXIO_I2S_ReadBlocking (FLEXIO_I2S_Type *base, uint8_t bitWidth, uint8_t *rxData, size_t size)`
Receives a piece of data using a blocking method.
- static `uint32_t FLEXIO_I2S_ReadData (FLEXIO_I2S_Type *base)`
Reads a data from the data register.

Transactional

- void `FLEXIO_I2S_TransferTxCreateHandle (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, flexio_i2s_callback_t callback, void *userData)`
Initializes the FlexIO I2S handle.
- void `FLEXIO_I2S_TransferSetFormat (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, flexio_i2s_format_t *format, uint32_t srcClock_Hz)`
Configures the FlexIO I2S audio format.
- void `FLEXIO_I2S_TransferRxCreateHandle (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, flexio_i2s_callback_t callback, void *userData)`
Initializes the FlexIO I2S receive handle.
- `status_t FLEXIO_I2S_TransferSendNonBlocking (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, flexio_i2s_transfer_t *xfer)`
Performs an interrupt non-blocking send transfer on FlexIO I2S.
- `status_t FLEXIO_I2S_TransferReceiveNonBlocking (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, flexio_i2s_transfer_t *xfer)`
Performs an interrupt non-blocking receive transfer on FlexIO I2S.
- void `FLEXIO_I2S_TransferAbortSend (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle)`
Aborts the current send.
- void `FLEXIO_I2S_TransferAbortReceive (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle)`
Aborts the current receive.
- `status_t FLEXIO_I2S_TransferGetSendCount (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, size_t *count)`
Gets the remaining bytes to be sent.
- `status_t FLEXIO_I2S_TransferGetReceiveCount (FLEXIO_I2S_Type *base, flexio_i2s_handle_t *handle, size_t *count)`
Gets the remaining bytes to be received.
- void `FLEXIO_I2S_TransferTxHandleIRQ (void *i2sBase, void *i2sHandle)`
Tx interrupt handler.
- void `FLEXIO_I2S_TransferRxHandleIRQ (void *i2sBase, void *i2sHandle)`
Rx interrupt handler.

18.4.3 Data Structure Documentation

18.4.3.1 struct FLEXIO_I2S_Type

Data Fields

- `FLEXIO_Type * flexioBase`
FlexIO base pointer.

- `uint8_t txPinIndex`
Tx data pin index in FlexIO pins.
- `uint8_t rxPinIndex`
Rx data pin index.
- `uint8_t bclkPinIndex`
Bit clock pin index.
- `uint8_t fsPinIndex`
Frame sync pin index.
- `uint8_t txShifterIndex`
Tx data shifter index.
- `uint8_t rxShifterIndex`
Rx data shifter index.
- `uint8_t bclkTimerIndex`
Bit clock timer index.
- `uint8_t fsTimerIndex`
Frame sync timer index.

18.4.3.2 struct flexio_i2s_config_t

Data Fields

- `bool enableI2S`
Enable FlexIO I2S.
- `flexio_i2s_master_slave_t masterSlave`
Master or slave.
- `flexio_pin_polarity_t txPinPolarity`
Tx data pin polarity, active high or low.
- `flexio_pin_polarity_t rxPinPolarity`
Rx data pin polarity.
- `flexio_pin_polarity_t bclkPinPolarity`
Bit clock pin polarity.
- `flexio_pin_polarity_t fsPinPolarity`
Frame sync pin polarity.
- `flexio_shifter_timer_polarity_t txTimerPolarity`
Tx data valid on bclk rising or falling edge.
- `flexio_shifter_timer_polarity_t rxTimerPolarity`
Rx data valid on bclk rising or falling edge.

18.4.3.3 struct flexio_i2s_format_t

Data Fields

- `uint8_t bitWidth`
Bit width of audio data, always 8/16/24/32 bits.
- `uint32_t sampleRate_Hz`
Sample rate of the audio data.

18.4.3.4 struct flexio_i2s_transfer_t

Data Fields

- `uint8_t * data`
Data buffer start pointer.
- `size_t dataSize`
Bytes to be transferred.

Field Documentation

(1) `size_t flexio_i2s_transfer_t::dataSize`

18.4.3.5 struct _flexio_i2s_handle

Data Fields

- `uint32_t state`
Internal state.
- `flexio_i2s_callback_t callback`
Callback function called at transfer event.
- `void * userData`
Callback parameter passed to callback function.
- `uint8_t bitWidth`
Bit width for transfer, 8/16/24/32bits.
- `flexio_i2s_transfer_t queue [FLEXIO_I2S_XFER_QUEUE_SIZE]`
Transfer queue storing queued transfer.
- `size_t transferSize [FLEXIO_I2S_XFER_QUEUE_SIZE]`
Data bytes need to transfer.
- `volatile uint8_t queueUser`
Index for user to queue transfer.
- `volatile uint8_t queueDriver`
Index for driver to get the transfer data and size.

18.4.4 Macro Definition Documentation

18.4.4.1 `#define FSL_FLEXIO_I2S_DRIVER_VERSION (MAKE_VERSION(2, 2, 0))`

18.4.4.2 `#define I2S_RETRY_TIMES 0U /* Define to zero means keep waiting until the flag is assert/deassert. */`

18.4.4.3 `#define FLEXIO_I2S_XFER_QUEUE_SIZE (4U)`

18.4.5 Enumeration Type Documentation

18.4.5.1 anonymous enum

Enumerator

kStatus_FLEXIO_I2S_Idle FlexIO I2S is in idle state.
kStatus_FLEXIO_I2S_TxBusy FlexIO I2S Tx is busy.
kStatus_FLEXIO_I2S_RxBusy FlexIO I2S Rx is busy.
kStatus_FLEXIO_I2S_Error FlexIO I2S error occurred.
kStatus_FLEXIO_I2S_QueueFull FlexIO I2S transfer queue is full.
kStatus_FLEXIO_I2S_Timeout FlexIO I2S timeout polling status flags.

18.4.5.2 enum flexio_i2s_master_slave_t

Enumerator

kFLEXIO_I2S_Master Master mode.
kFLEXIO_I2S_Slave Slave mode.

18.4.5.3 anonymous enum

Enumerator

kFLEXIO_I2S_TxDataRegEmptyInterruptEnable Transmit buffer empty interrupt enable.
kFLEXIO_I2S_RxDataRegFullInterruptEnable Receive buffer full interrupt enable.

18.4.5.4 anonymous enum

Enumerator

kFLEXIO_I2S_TxDataRegEmptyFlag Transmit buffer empty flag.
kFLEXIO_I2S_RxDataRegFullFlag Receive buffer full flag.

18.4.5.5 enum flexio_i2s_sample_rate_t

Enumerator

kFLEXIO_I2S_SampleRate8KHz Sample rate 8000Hz.
kFLEXIO_I2S_SampleRate11025Hz Sample rate 11025Hz.
kFLEXIO_I2S_SampleRate12KHz Sample rate 12000Hz.
kFLEXIO_I2S_SampleRate16KHz Sample rate 16000Hz.
kFLEXIO_I2S_SampleRate22050Hz Sample rate 22050Hz.
kFLEXIO_I2S_SampleRate24KHz Sample rate 24000Hz.

kFLEXIO_I2S_SampleRate32KHz Sample rate 32000Hz.
kFLEXIO_I2S_SampleRate44100Hz Sample rate 44100Hz.
kFLEXIO_I2S_SampleRate48KHz Sample rate 48000Hz.
kFLEXIO_I2S_SampleRate96KHz Sample rate 96000Hz.

18.4.5.6 enum flexio_i2s_word_width_t

Enumerator

kFLEXIO_I2S_WordWidth8bits Audio data width 8 bits.
kFLEXIO_I2S_WordWidth16bits Audio data width 16 bits.
kFLEXIO_I2S_WordWidth24bits Audio data width 24 bits.
kFLEXIO_I2S_WordWidth32bits Audio data width 32 bits.

18.4.6 Function Documentation

18.4.6.1 void FLEXIO_I2S_Init (***FLEXIO_I2S_Type*** * *base*, ***const flexio_i2s_config_t*** * *config*)

This API configures FlexIO pins and shifter to I2S and configures the FlexIO I2S with a configuration structure. The configuration structure can be filled by the user, or be set with default values by [FLEXIO_I2S_GetDefaultConfig\(\)](#).

Note

This API should be called at the beginning of the application to use the FlexIO I2S driver. Otherwise, any access to the FlexIO I2S module can cause hard fault because the clock is not enabled.

Parameters

<i>base</i>	FlexIO I2S base pointer
<i>config</i>	FlexIO I2S configure structure.

18.4.6.2 void FLEXIO_I2S_GetDefaultConfig (***flexio_i2s_config_t*** * *config*)

The purpose of this API is to get the configuration structure initialized for use in [FLEXIO_I2S_Init\(\)](#). Users may use the initialized structure unchanged in [FLEXIO_I2S_Init\(\)](#) or modify some fields of the structure before calling [FLEXIO_I2S_Init\(\)](#).

Parameters

<i>config</i>	pointer to master configuration structure
---------------	---

18.4.6.3 void FLEXIO_I2S_Deinit (FLEXIO_I2S_Type * *base*)

Calling this API resets the FlexIO I2S shifter and timer config. After calling this API, call the FLEXO_I2S_Init to use the FlexIO I2S module.

Parameters

<i>base</i>	FlexIO I2S base pointer
-------------	-------------------------

18.4.6.4 static void FLEXIO_I2S_Enable (FLEXIO_I2S_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type
<i>enable</i>	True to enable, false dose not have any effect.

18.4.6.5 uint32_t FLEXIO_I2S_GetStatusFlags (FLEXIO_I2S_Type * *base*)

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure
-------------	--

Returns

Status flag, which are ORed by the enumerators in the _flexio_i2s_status_flags.

18.4.6.6 void FLEXIO_I2S_EnableInterrupts (FLEXIO_I2S_Type * *base*, uint32_t *mask*)

This function enables the FlexIO UART interrupt.

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure
<i>mask</i>	interrupt source

18.4.6.7 void FLEXIO_I2S_DisableInterrupts ([FLEXIO_I2S_Type](#) * *base*, [uint32_t](#) *mask*)

This function enables the FlexIO UART interrupt.

Parameters

<i>base</i>	pointer to FLEXIO_I2S_Type structure
<i>mask</i>	interrupt source

18.4.6.8 static void FLEXIO_I2S_TxEnableDMA ([FLEXIO_I2S_Type](#) * *base*, [bool](#) *enable*) [inline], [static]

Parameters

<i>base</i>	FlexIO I2S base pointer
<i>enable</i>	True means enable DMA, false means disable DMA.

18.4.6.9 static void FLEXIO_I2S_RxEnableDMA ([FLEXIO_I2S_Type](#) * *base*, [bool](#) *enable*) [inline], [static]

Parameters

<i>base</i>	FlexIO I2S base pointer
<i>enable</i>	True means enable DMA, false means disable DMA.

18.4.6.10 static [uint32_t](#) FLEXIO_I2S_TxGetDataRegisterAddress ([FLEXIO_I2S_Type](#) * *base*) [inline], [static]

This function returns the I2S data register address, mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure
-------------	--

Returns

FlexIO i2s send data register address.

18.4.6.11 static uint32_t FLEXIO_I2S_RxGetDataRegisterAddress ([FLEXIO_I2S_Type](#) * *base*) [inline], [static]

This function returns the I2S data register address, mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure
-------------	--

Returns

FlexIO i2s receive data register address.

18.4.6.12 void FLEXIO_I2S_MasterSetFormat ([FLEXIO_I2S_Type](#) * *base*, [flexio_i2s_format_t](#) * *format*, uint32_t *srcClock_Hz*)

Audio format can be changed in run-time of FlexIO I2S. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure
<i>format</i>	Pointer to FlexIO I2S audio data format structure.
<i>srcClock_Hz</i>	I2S master clock source frequency in Hz.

18.4.6.13 void FLEXIO_I2S_SlaveSetFormat ([FLEXIO_I2S_Type](#) * *base*, [flexio_i2s_format_t](#) * *format*)

Audio format can be changed in run-time of FlexIO I2S. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure
<i>format</i>	Pointer to FlexIO I2S audio data format structure.

18.4.6.14 status_t [FLEXIO_I2S_WriteBlocking](#) ([FLEXIO_I2S_Type](#) * *base*, [uint8_t](#) *bitWidth*, [uint8_t](#) * *txData*, [size_t](#) *size*)

Note

This function blocks via polling until data is ready to be sent.

Parameters

<i>base</i>	FlexIO I2S base pointer.
<i>bitWidth</i>	How many bits in a audio word, usually 8/16/24/32 bits.
<i>txData</i>	Pointer to the data to be written.
<i>size</i>	Bytes to be written.

Return values

<i>kStatus_Success</i>	Successfully write data.
<i>kStatus_FLEXIO_I2C_Timeout</i>	Timeout polling status flags.

18.4.6.15 static void [FLEXIO_I2S_WriteData](#) ([FLEXIO_I2S_Type](#) * *base*, [uint8_t](#) *bitWidth*, [uint32_t](#) *data*) [inline], [static]

Parameters

<i>base</i>	FlexIO I2S base pointer.
<i>bitWidth</i>	How many bits in a audio word, usually 8/16/24/32 bits.
<i>data</i>	Data to be written.

18.4.6.16 status_t [FLEXIO_I2S_ReadBlocking](#) ([FLEXIO_I2S_Type](#) * *base*, [uint8_t](#) *bitWidth*, [uint8_t](#) * *rxData*, [size_t](#) *size*)

Note

This function blocks via polling until data is ready to be sent.

Parameters

<i>base</i>	FlexIO I2S base pointer
<i>bitWidth</i>	How many bits in a audio word, usually 8/16/24/32 bits.
<i>rxData</i>	Pointer to the data to be read.
<i>size</i>	Bytes to be read.

Return values

<i>kStatus_Success</i>	Successfully read data.
<i>kStatus_FLEXIO_I2C_Timeout</i>	Timeout polling status flags.

**18.4.6.17 static uint32_t FLEXIO_I2S_ReadData (FLEXIO_I2S_Type * *base*)
[inline], [static]**

Parameters

<i>base</i>	FlexIO I2S base pointer
-------------	-------------------------

Returns

Data read from data register.

**18.4.6.18 void FLEXIO_I2S_TransferTxCreateHandle (FLEXIO_I2S_Type * *base*,
flexio_i2s_handle_t * *handle*, flexio_i2s_callback_t *callback*, void * *userData*)**

This function initializes the FlexIO I2S handle which can be used for other FlexIO I2S transactional APIs. Call this API once to get the initialized handle.

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure
<i>handle</i>	Pointer to flexio_i2s_handle_t structure to store the transfer state.
<i>callback</i>	FlexIO I2S callback function, which is called while finished a block.
<i>userData</i>	User parameter for the FlexIO I2S callback.

18.4.6.19 void FLEXIO_I2S_TransferSetFormat (**FLEXIO_I2S_Type * *base*, **flexio_i2s_handle_t** * *handle*, **flexio_i2s_format_t** * *format*, **uint32_t** *srcClock_Hz*)**

Audio format can be changed at run-time of FlexIO I2S. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure.
<i>handle</i>	FlexIO I2S handle pointer.
<i>format</i>	Pointer to audio data format structure.
<i>srcClock_Hz</i>	FlexIO I2S bit clock source frequency in Hz. This parameter should be 0 while in slave mode.

18.4.6.20 void FLEXIO_I2S_TransferRxCreateHandle (**FLEXIO_I2S_Type * *base*, **flexio_i2s_handle_t** * *handle*, **flexio_i2s_callback_t** *callback*, **void** * *userData*)**

This function initializes the FlexIO I2S handle which can be used for other FlexIO I2S transactional APIs. Call this API once to get the initialized handle.

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure.
<i>handle</i>	Pointer to flexio_i2s_handle_t structure to store the transfer state.
<i>callback</i>	FlexIO I2S callback function, which is called while finished a block.
<i>userData</i>	User parameter for the FlexIO I2S callback.

18.4.6.21 status_t FLEXIO_I2S_TransferSendNonBlocking (**FLEXIO_I2S_Type * *base*, **flexio_i2s_handle_t** * *handle*, **flexio_i2s_transfer_t** * *xfer*)**

Note

The API returns immediately after transfer initiates. Call FLEXIO_I2S_GetRemainingBytes to poll the transfer status and check whether the transfer is finished. If the return status is 0, the transfer is finished.

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure.
<i>handle</i>	Pointer to flexio_i2s_handle_t structure which stores the transfer state
<i>xfer</i>	Pointer to flexio_i2s_transfer_t structure

Return values

<i>kStatus_Success</i>	Successfully start the data transmission.
<i>kStatus_FLEXIO_I2S_Tx-Busy</i>	Previous transmission still not finished, data not all written to TX register yet.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

18.4.6.22 **status_t FLEXIO_I2S_TransferReceiveNonBlocking ([FLEXIO_I2S_Type](#) * *base*, [flexio_i2s_handle_t](#) * *handle*, [flexio_i2s_transfer_t](#) * *xfer*)**

Note

The API returns immediately after transfer initiates. Call FLEXIO_I2S_GetRemainingBytes to poll the transfer status to check whether the transfer is finished. If the return status is 0, the transfer is finished.

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure.
<i>handle</i>	Pointer to flexio_i2s_handle_t structure which stores the transfer state
<i>xfer</i>	Pointer to flexio_i2s_transfer_t structure

Return values

<i>kStatus_Success</i>	Successfully start the data receive.
------------------------	--------------------------------------

<i>kStatus_FLEXIO_I2S_-RxBusy</i>	Previous receive still not finished.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

18.4.6.23 void FLEXIO_I2S_TransferAbortSend (**FLEXIO_I2S_Type** * *base*, **flexio_i2s_handle_t** * *handle*)

Note

This API can be called at any time when interrupt non-blocking transfer initiates to abort the transfer in a early time.

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure.
<i>handle</i>	Pointer to flexio_i2s_handle_t structure which stores the transfer state

18.4.6.24 void FLEXIO_I2S_TransferAbortReceive (**FLEXIO_I2S_Type** * *base*, **flexio_i2s_handle_t** * *handle*)

Note

This API can be called at any time when interrupt non-blocking transfer initiates to abort the transfer in a early time.

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure.
<i>handle</i>	Pointer to flexio_i2s_handle_t structure which stores the transfer state

18.4.6.25 **status_t** FLEXIO_I2S_TransferGetSendCount (**FLEXIO_I2S_Type** * *base*, **flexio_i2s_handle_t** * *handle*, **size_t** * *count*)

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure.
<i>handle</i>	Pointer to flexio_i2s_handle_t structure which stores the transfer state
<i>count</i>	Bytes sent.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferInProgress</i>	There is not a non-blocking transaction currently in progress.

18.4.6.26 **status_t FLEXIO_I2S_TransferGetReceiveCount (**FLEXIO_I2S_Type * base,** **flexio_i2s_handle_t * handle,** **size_t * count**)**

Parameters

<i>base</i>	Pointer to FLEXIO_I2S_Type structure.
<i>handle</i>	Pointer to flexio_i2s_handle_t structure which stores the transfer state
<i>count</i>	Bytes received.

Returns

count Bytes received.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferInProgress</i>	There is not a non-blocking transaction currently in progress.

18.4.6.27 **void FLEXIO_I2S_TransferTxHandleIRQ (**void * i2sBase,** **void * i2sHandle**)**

Parameters

<i>i2sBase</i>	Pointer to FLEXIO_I2S_Type structure.
----------------	--

<i>i2sHandle</i>	Pointer to flexio_i2s_handle_t structure
------------------	--

18.4.6.28 void FLEXIO_I2S_TransferRxHandleIRQ (void * *i2sBase*, void * *i2sHandle*)

Parameters

<i>i2sBase</i>	Pointer to FLEXIO_I2S_Type structure.
<i>i2sHandle</i>	Pointer to flexio_i2s_handle_t structure.

18.5 FlexIO SPI Driver

18.5.1 Overview

The MCUXpresso SDK provides a peripheral driver for an SPI function using the Flexible I/O module of MCUXpresso SDK devices.

FlexIO SPI driver includes functional APIs and transactional APIs.

Functional APIs target low-level APIs. Functional APIs can be used for FlexIO SPI initialization/configuration/operation for optimization/customization purpose. Using the functional API requires the knowledge of the FlexIO SPI peripheral and how to organize functional APIs to meet the application requirements. All functional API use the [FLEXIO_SPI_Type](#) *base as the first parameter. FlexIO SPI functional operation groups provide the functional API set.

Transactional APIs target high-level APIs. Transactional APIs can be used to enable the peripheral and also in the application if the code size and performance of transactional APIs can satisfy requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code. All transactional APIs use the flexio_spi_master_handle_t/flexio_spi_slave_handle_t as the second parameter. Initialize the handle by calling the [FLEXIO_SPI_MasterTransferCreateHandle\(\)](#) or [FLEXIO_SPI_SlaveTransferCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer. This means that the functions [FLEXIO_SPI_MasterTransferNonBlocking\(\)](#)/[FLEXIO_SPI_SlaveTransferNonBlocking\(\)](#) set up an interrupt for data transfer. When the transfer is complete, the upper layer is notified through a callback function with the kStatus_FLEXIO_SPI_Idle status.

Note that the FlexIO SPI slave driver only supports discontinuous PCS access, which is a limitation. The FlexIO SPI slave driver can support continuous PCS, but the slave cannot adapt discontinuous and continuous PCS automatically. Users can change the timer disable mode in [FLEXIO_SPI_SlaveInit](#) manually, from kFLEXIO_TimerDisableOnTimerCompare to kFLEXIO_TimerDisableNever to enable a discontinuous PCS access. Only CPHA = 0 is supported.

18.5.2 Typical use case

18.5.2.1 FlexIO SPI send/receive using an interrupt method

```
flexio_spi_master_handle_t g_spiHandle;
FLEXIO_SPI_Type spiDev;
volatile bool txFinished;
static uint8_t srcBuff[BUFFER_SIZE];
static uint8_t destBuff[BUFFER_SIZE];

void FLEXIO_SPI_MasterUserCallback(FLEXIO_SPI_Type *base, flexio_spi_master_handle_t *handle
    , status_t status, void *userData)
{
    userData = userData;

    if (kStatus_FLEXIO_SPI_Idle == status)
    {
        txFinished = true;
    }
}
```

```

}

void main(void)
{
    //...
    flexio_spi_transfer_t xfer = {0};
    flexio_spi_master_config_t userConfig;

    FLEXIO_SPI_MasterGetDefaultConfig(&userConfig);
    userConfig.baudRate_Bps = 5000000U;

    spiDev.flexioBase = BOARD_FLEXIO_BASE;
    spiDev.SDOPinIndex = FLEXIO_SPI_MOSI_PIN;
    spiDev.SDIPinIndex = FLEXIO_SPI_MISO_PIN;
    spiDev.SCKPinIndex = FLEXIO_SPI_SCK_PIN;
    spiDev.CSnPinIndex = FLEXIO_SPI_CSn_PIN;
    spiDev.shifterIndex[0] = 0U;
    spiDev.shifterIndex[1] = 1U;
    spiDev.timerIndex[0] = 0U;
    spiDev.timerIndex[1] = 1U;

    FLEXIO_SPI_MasterInit(&spiDev, &userConfig, FLEXIO_CLOCK_FREQUENCY);

    xfer.txData = srcBuff;
    xfer.rxData = destBuff;
    xfer.dataSize = BUFFER_SIZE;
    xfer.flags = kFLEXIO_SPI_8bitMsb;
    FLEXIO_SPI_MasterTransferCreateHandle(&spiDev, &g_spiHandle,
                                         FLEXIO_SPI_MasterUserCallback, NULL);
    FLEXIO_SPI_MasterTransferNonBlocking(&spiDev, &g_spiHandle, &xfer);

    // Send finished.
    while (!txFinished)
    {
        // ...
    }
}

```

18.5.2.2 FlexIO_SPI Send/Receive in DMA way

```

dma_handle_t g_spiTxDmaHandle;
dma_handle_t g_spiRxDmaHandle;
flexio_spi_master_handle_t g_spiHandle;
FLEXIO_SPI_Type spiDev;
volatile bool txFinished;
static uint8_t srcBuff[BUFFER_SIZE];
static uint8_t destBuff[BUFFER_SIZE];
void FLEXIO_SPI_MasterUserCallback(FLEXIO_SPI_Type *base, flexio_spi_master_dma_handle_t
                                   *handle, status_t status, void *userData)
{
    userData = userData;

    if (kStatus_FLEXIO_SPI_Idle == status)
    {
        txFinished = true;
    }
}

void main(void)
{
    flexio_spi_transfer_t xfer = {0};
    flexio_spi_master_config_t userConfig;

    FLEXIO_SPI_MasterGetDefaultConfig(&userConfig);

```

```

userConfig.baudRate_Bps = 500000U;

spiDev.flexioBase = BOARD_FLEXIO_BASE;
spiDev.SDOPinIndex = FLEXIO_SPI_MOSI_PIN;
spiDev.SDIPinIndex = FLEXIO_SPI_MISO_PIN;
spiDev.SCKPinIndex = FLEXIO_SPI_SCK_PIN;
spiDev.CSnPinIndex = FLEXIO_SPI_CSn_PIN;
spiDev.shifterIndex[0] = 0U;
spiDev.shifterIndex[1] = 1U;
spiDev.timerIndex[0] = 0U;
spiDev.timerIndex[1] = 1U;

/* Init DMAMUX. */
DMAMUX_Init(EXAMPLE_FLEXIO_SPI_DMAMUX_BASEADDR)

/* Init the DMA/EDMA module */
#if defined(FSL_FEATURE_SOC_DMA_COUNT) && FSL_FEATURE_SOC_DMA_COUNT > 0U
DMA_Init(EXAMPLE_FLEXIO_SPI_DMA_BASEADDR);
DMA_CreateHandle(&txHandle, EXAMPLE_FLEXIO_SPI_DMA_BASEADDR, FLEXIO_SPI_TX_DMA_CHANNEL);
DMA_CreateHandle(&rxHandle, EXAMPLE_FLEXIO_SPI_DMA_BASEADDR, FLEXIO_SPI_RX_DMA_CHANNEL);
#endif /* FSL_FEATURE_SOC_DMA_COUNT */

#if defined(FSL_FEATURE_SOC_EDMA_COUNT) && FSL_FEATURE_SOC_EDMA_COUNT > 0U
edma_config_t edmaConfig;

EDMA_GetDefaultConfig(&edmaConfig);
EDMA_Init(EXAMPLE_FLEXIO_SPI_DMA_BASEADDR, &edmaConfig);
EDMA_CreateHandle(&txHandle, EXAMPLE_FLEXIO_SPI_DMA_BASEADDR,
FLEXIO_SPI_TX_DMA_CHANNEL);
EDMA_CreateHandle(&rxHandle, EXAMPLE_FLEXIO_SPI_DMA_BASEADDR,
FLEXIO_SPI_RX_DMA_CHANNEL);
#endif /* FSL_FEATURE_SOC_EDMA_COUNT */

dma_request_source_tx = (dma_request_source_t)(FLEXIO_DMA_REQUEST_BASE + spiDev.
shifterIndex[0]);
dma_request_source_rx = (dma_request_source_t)(FLEXIO_DMA_REQUEST_BASE + spiDev.
shifterIndex[1]);

/* Requests DMA channels for transmit and receive. */
DMAMUX_SetSource(EXAMPLE_FLEXIO_SPI_DMAMUX_BASEADDR, FLEXIO_SPI_TX_DMA_CHANNEL, (
dma_request_source_t)dma_request_source_tx);
DMAMUX_SetSource(EXAMPLE_FLEXIO_SPI_DMAMUX_BASEADDR, FLEXIO_SPI_RX_DMA_CHANNEL, (
dma_request_source_t)dma_request_source_rx);
DMAMUX_EnableChannel(EXAMPLE_FLEXIO_SPI_DMAMUX_BASEADDR,
FLEXIO_SPI_TX_DMA_CHANNEL);
DMAMUX_EnableChannel(EXAMPLE_FLEXIO_SPI_DMAMUX_BASEADDR,
FLEXIO_SPI_RX_DMA_CHANNEL);

FLEXIO_SPI_MasterInit(&spiDev, &userConfig, FLEXIO_CLOCK_FREQUENCY);

/* Initializes the buffer. */
for (i = 0; i < BUFFER_SIZE; i++)
{
    srcBuff[i] = i;
}

/* Sends to the slave. */
xfer.txData = srcBuff;
xfer.rxData = destBuff;
xfer.dataSize = BUFFER_SIZE;
xfer.flags = kFLEXIO_SPI_8bitMsb;
FLEXIO_SPI_MasterTransferCreateHandleDMA(&spiDev, &g_spiHandle, FLEXIO_SPI_MasterUserCallback, NULL
, &g_spitxDmaHandle, &g_spirxDmaHandle);
FLEXIO_SPI_MasterTransferDMA(&spiDev, &g_spiHandle, &xfer);

// Send finished.
while (!txFinished)
{

```

```

    }
    // ...
}

```

Data Structures

- struct **FLEXIO_SPI_Type**
Define FlexIO SPI access structure typedef. [More...](#)
- struct **flexio_spi_master_config_t**
Define FlexIO SPI master configuration structure. [More...](#)
- struct **flexio_spi_slave_config_t**
Define FlexIO SPI slave configuration structure. [More...](#)
- struct **flexio_spi_transfer_t**
Define FlexIO SPI transfer structure. [More...](#)
- struct **flexio_spi_master_handle_t**
Define FlexIO SPI handle structure. [More...](#)

Macros

- #define **FLEXIO_SPI_DUMMYDATA** (0xFFFFU)
FlexIO SPI dummy transfer data, the data is sent while txData is NULL.
- #define **SPI_RETRY_TIMES** 0U /* Define to zero means keep waiting until the flag is assert/deassert. */
Retry times for waiting flag.

Typedefs

- typedef flexio_spi_master_handle_t **flexio_spi_slave_handle_t**
Slave handle is the same with master handle.
- typedef void(* **flexio_spi_master_transfer_callback_t**)(FLEXIO_SPI_Type *base, flexio_spi_master_handle_t *handle, status_t status, void *userData)
FlexIO SPI master callback for finished transmit.
- typedef void(* **flexio_spi_slave_transfer_callback_t**)(FLEXIO_SPI_Type *base, flexio_spi_slave_handle_t *handle, status_t status, void *userData)
FlexIO SPI slave callback for finished transmit.

Enumerations

- enum {
 kStatus_FLEXIO_SPI_Busy = MAKE_STATUS(kStatusGroup_FLEXIO_SPI, 1),
 kStatus_FLEXIO_SPI_Idle = MAKE_STATUS(kStatusGroup_FLEXIO_SPI, 2),
 kStatus_FLEXIO_SPI_Error = MAKE_STATUS(kStatusGroup_FLEXIO_SPI, 3),
 kStatus_FLEXIO_SPI_Timeout }

Error codes for the FlexIO SPI driver.

- enum `flexio_spi_clock_phase_t` {

 `kFLEXIO_SPI_ClockPhaseFirstEdge` = 0x0U,

 `kFLEXIO_SPI_ClockPhaseSecondEdge` = 0x1U }

 FlexIO SPI clock phase configuration.
- enum `flexio_spi_shift_direction_t` {

 `kFLEXIO_SPI_MsbFirst` = 0,

 `kFLEXIO_SPI_LsbFirst` = 1 }

 FlexIO SPI data shifter direction options.
- enum `flexio_spi_data_bitcount_mode_t` {

 `kFLEXIO_SPI_8BitMode` = 0x08U,

 `kFLEXIO_SPI_16BitMode` = 0x10U }

 FlexIO SPI data length mode options.
- enum `_flexio_spi_interrupt_enable` {

 `kFLEXIO_SPI_TxEmptyInterruptEnable` = 0x1U,

 `kFLEXIO_SPI_RxFullInterruptEnable` = 0x2U }

 Define FlexIO SPI interrupt mask.
- enum `_flexio_spi_status_flags` {

 `kFLEXIO_SPI_TxBufferEmptyFlag` = 0x1U,

 `kFLEXIO_SPI_RxBufferFullFlag` = 0x2U }

 Define FlexIO SPI status mask.
- enum `_flexio_spi_dma_enable` {

 `kFLEXIO_SPI_TxDmaEnable` = 0x1U,

 `kFLEXIO_SPI_RxDmaEnable` = 0x2U,

 `kFLEXIO_SPI_DmaAllEnable` = 0x3U }

 Define FlexIO SPI DMA mask.
- enum `_flexio_spi_transfer_flags` {

 `kFLEXIO_SPI_8bitMsb` = 0x1U,

 `kFLEXIO_SPI_8bitLsb` = 0x2U,

 `kFLEXIO_SPI_16bitMsb` = 0x9U,

 `kFLEXIO_SPI_16bitLsb` = 0xaU }

 Define FlexIO SPI transfer flags.

Driver version

- #define `FSL_FLEXIO_SPI_DRIVER_VERSION` (MAKE_VERSION(2, 2, 1))

 FlexIO SPI driver version 2.2.1.

FlexIO SPI Configuration

- void `FLEXIO_SPI_MasterInit` (`FLEXIO_SPI_Type` *base, `flexio_spi_master_config_t` *masterConfig, `uint32_t` srcClock_Hz)

 Ungates the FlexIO clock, resets the FlexIO module, configures the FlexIO SPI master hardware, and configures the FlexIO SPI with FlexIO SPI master configuration.
- void `FLEXIO_SPI_MasterDeinit` (`FLEXIO_SPI_Type` *base)

 Resets the FlexIO SPI timer and shifter config.
- void `FLEXIO_SPI_MasterGetDefaultConfig` (`flexio_spi_master_config_t` *masterConfig)

- Gets the default configuration to configure the FlexIO SPI master.
- void **FLEXIO_SPI_SlaveInit** (**FLEXIO_SPI_Type** *base, **flexio_spi_slave_config_t** *slaveConfig)
Ungates the FlexIO clock, resets the FlexIO module, configures the FlexIO SPI slave hardware configuration, and configures the FlexIO SPI with FlexIO SPI slave configuration.
- void **FLEXIO_SPI_SlaveDeinit** (**FLEXIO_SPI_Type** *base)
Gates the FlexIO clock.
- void **FLEXIO_SPI_SlaveGetDefaultConfig** (**flexio_spi_slave_config_t** *slaveConfig)
Gets the default configuration to configure the FlexIO SPI slave.

Status

- uint32_t **FLEXIO_SPI_GetStatusFlags** (**FLEXIO_SPI_Type** *base)
Gets FlexIO SPI status flags.
- void **FLEXIO_SPI_ClearStatusFlags** (**FLEXIO_SPI_Type** *base, uint32_t mask)
Clears FlexIO SPI status flags.

Interrupts

- void **FLEXIO_SPI_EnableInterrupts** (**FLEXIO_SPI_Type** *base, uint32_t mask)
Enables the FlexIO SPI interrupt.
- void **FLEXIO_SPI_DisableInterrupts** (**FLEXIO_SPI_Type** *base, uint32_t mask)
Disables the FlexIO SPI interrupt.

DMA Control

- void **FLEXIO_SPI_EnableDMA** (**FLEXIO_SPI_Type** *base, uint32_t mask, bool enable)
Enables/disables the FlexIO SPI transmit DMA.
- static uint32_t **FLEXIO_SPI_GetTxDataRegisterAddress** (**FLEXIO_SPI_Type** *base, **flexio_spi_shift_direction_t** direction)
Gets the FlexIO SPI transmit data register address for MSB first transfer.
- static uint32_t **FLEXIO_SPI_GetRxDataRegisterAddress** (**FLEXIO_SPI_Type** *base, **flexio_spi_shift_direction_t** direction)
Gets the FlexIO SPI receive data register address for the MSB first transfer.

Bus Operations

- static void **FLEXIO_SPI_Enable** (**FLEXIO_SPI_Type** *base, bool enable)
Enables/disables the FlexIO SPI module operation.
- void **FLEXIO_SPI_MasterSetBaudRate** (**FLEXIO_SPI_Type** *base, uint32_t baudRate_Bps, uint32_t srcClockHz)
Sets baud rate for the FlexIO SPI transfer, which is only used for the master.
- static void **FLEXIO_SPI_WriteData** (**FLEXIO_SPI_Type** *base, **flexio_spi_shift_direction_t** direction, uint16_t data)
Writes one byte of data, which is sent using the MSB method.

- static uint16_t **FLEXIO_SPI_ReadData** (FLEXIO_SPI_Type *base, flexio_spi_shift_direction_t direction)

Reads 8 bit/16 bit data.
- status_t **FLEXIO_SPI_WriteBlocking** (FLEXIO_SPI_Type *base, flexio_spi_shift_direction_t direction, const uint8_t *buffer, size_t size)

Sends a buffer of data bytes.
- status_t **FLEXIO_SPI_ReadBlocking** (FLEXIO_SPI_Type *base, flexio_spi_shift_direction_t direction, uint8_t *buffer, size_t size)

Receives a buffer of bytes.
- status_t **FLEXIO_SPI_MasterTransferBlocking** (FLEXIO_SPI_Type *base, flexio_spi_transfer_t *xfer)

Receives a buffer of bytes.

Transactional

- status_t **FLEXIO_SPI_MasterTransferCreateHandle** (FLEXIO_SPI_Type *base, flexio_spi_master_handle_t *handle, flexio_spi_master_transfer_callback_t callback, void *userData)

Initializes the FlexIO SPI Master handle, which is used in transactional functions.
- status_t **FLEXIO_SPI_MasterTransferNonBlocking** (FLEXIO_SPI_Type *base, flexio_spi_master_handle_t *handle, flexio_spi_transfer_t *xfer)

Master transfer data using IRQ.
- void **FLEXIO_SPI_MasterTransferAbort** (FLEXIO_SPI_Type *base, flexio_spi_master_handle_t *handle)

Aborts the master data transfer, which used IRQ.
- status_t **FLEXIO_SPI_MasterTransferGetCount** (FLEXIO_SPI_Type *base, flexio_spi_master_handle_t *handle, size_t *count)

Gets the data transfer status which used IRQ.
- void **FLEXIO_SPI_MasterTransferHandleIRQ** (void *spiType, void *spiHandle)

FlexIO SPI master IRQ handler function.
- status_t **FLEXIO_SPI_SlaveTransferCreateHandle** (FLEXIO_SPI_Type *base, flexio_spi_slave_handle_t *handle, flexio_spi_slave_transfer_callback_t callback, void *userData)

Initializes the FlexIO SPI Slave handle, which is used in transactional functions.
- status_t **FLEXIO_SPI_SlaveTransferNonBlocking** (FLEXIO_SPI_Type *base, flexio_spi_slave_handle_t *handle, flexio_spi_transfer_t *xfer)

Slave transfer data using IRQ.
- static void **FLEXIO_SPI_SlaveTransferAbort** (FLEXIO_SPI_Type *base, flexio_spi_slave_handle_t *handle)

Aborts the slave data transfer which used IRQ, share same API with master.
- static status_t **FLEXIO_SPI_SlaveTransferGetCount** (FLEXIO_SPI_Type *base, flexio_spi_slave_handle_t *handle, size_t *count)

Gets the data transfer status which used IRQ, share same API with master.
- void **FLEXIO_SPI_SlaveTransferHandleIRQ** (void *spiType, void *spiHandle)

FlexIO SPI slave IRQ handler function.

18.5.3 Data Structure Documentation

18.5.3.1 struct FLEXIO_SPI_Type

Data Fields

- `FLEXIO_Type * flexioBase`
FlexIO base pointer.
- `uint8_t SDOPinIndex`
Pin select for data output.
- `uint8_t SDIPinIndex`
Pin select for data input.
- `uint8_t SCKPinIndex`
Pin select for clock.
- `uint8_t CSnPinIndex`
Pin select for enable.
- `uint8_t shifterIndex [2]`
Shifter index used in FlexIO SPI.
- `uint8_t timerIndex [2]`
Timer index used in FlexIO SPI.

Field Documentation

- (1) `FLEXIO_Type* FLEXIO_SPI_Type::flexioBase`
- (2) `uint8_t FLEXIO_SPI_Type::SDOPinIndex`
- (3) `uint8_t FLEXIO_SPI_Type::SDIPinIndex`
- (4) `uint8_t FLEXIO_SPI_Type::SCKPinIndex`
- (5) `uint8_t FLEXIO_SPI_Type::CSnPinIndex`
- (6) `uint8_t FLEXIO_SPI_Type::shifterIndex[2]`
- (7) `uint8_t FLEXIO_SPI_Type::timerIndex[2]`

18.5.3.2 struct flexio_spi_master_config_t

Data Fields

- `bool enableMaster`
Enable/disable FlexIO SPI master after configuration.
- `bool enableInDoze`
Enable/disable FlexIO operation in doze mode.
- `bool enableInDebug`
Enable/disable FlexIO operation in debug mode.
- `bool enableFastAccess`
*Enable/disable fast access to FlexIO registers,
fast access requires the FlexIO clock to be at least twice the frequency of the bus clock.*
- `uint32_t baudRate_Bps`
Baud rate in Bps.
- `flexio_spi_clock_phase_t phase`

- **Clock phase.**
- **flexio_spi_data_bitcount_mode_t dataMode**
8bit or 16bit mode.

Field Documentation

- (1) **bool flexio_spi_master_config_t::enableMaster**
- (2) **bool flexio_spi_master_config_t::enableInDoze**
- (3) **bool flexio_spi_master_config_t::enableInDebug**
- (4) **bool flexio_spi_master_config_t::enableFastAccess**
- (5) **uint32_t flexio_spi_master_config_t::baudRate_Bps**
- (6) **flexio_spi_clock_phase_t flexio_spi_master_config_t::phase**
- (7) **flexio_spi_data_bitcount_mode_t flexio_spi_master_config_t::dataMode**

18.5.3.3 struct flexio_spi_slave_config_t

Data Fields

- **bool enableSlave**
Enable/disable FlexIO SPI slave after configuration.
- **bool enableInDoze**
Enable/disable FlexIO operation in doze mode.
- **bool enableInDebug**
Enable/disable FlexIO operation in debug mode.
- **bool enableFastAccess**
*Enable/disable fast access to FlexIO registers,
fast access requires the FlexIO clock to be at least twice the frequency of the bus clock.*
- **flexio_spi_clock_phase_t phase**
Clock phase.
- **flexio_spi_data_bitcount_mode_t dataMode**
8bit or 16bit mode.

Field Documentation

- (1) **bool flexio_spi_slave_config_t::enableSlave**
- (2) **bool flexio_spi_slave_config_t::enableInDoze**
- (3) **bool flexio_spi_slave_config_t::enableInDebug**
- (4) **bool flexio_spi_slave_config_t::enableFastAccess**
- (5) **flexio_spi_clock_phase_t flexio_spi_slave_config_t::phase**
- (6) **flexio_spi_data_bitcount_mode_t flexio_spi_slave_config_t::dataMode**

18.5.3.4 struct flexio_spi_transfer_t

Data Fields

- `uint8_t * txData`
Send buffer.
- `uint8_t * rxData`
Receive buffer.
- `size_t dataSize`
Transfer bytes.
- `uint8_t flags`
FlexIO SPI control flag, MSB first or LSB first.

Field Documentation

- (1) `uint8_t* flexio_spi_transfer_t::txData`
- (2) `uint8_t* flexio_spi_transfer_t::rxData`
- (3) `size_t flexio_spi_transfer_t::dataSize`
- (4) `uint8_t flexio_spi_transfer_t::flags`

18.5.3.5 struct _flexio_spi_master_handle

typedef for `flexio_spi_master_handle_t` in advance.

Data Fields

- `uint8_t * txData`
Transfer buffer.
- `uint8_t * rxData`
Receive buffer.
- `size_t transferSize`
Total bytes to be transferred.
- `volatile size_t txRemainingBytes`
Send data remaining in bytes.
- `volatile size_t rxRemainingBytes`
Receive data remaining in bytes.
- `volatile uint32_t state`
FlexIO SPI internal state.
- `uint8_t bytePerFrame`
SPI mode, 2bytes or 1byte in a frame.
- `flexio_spi_shift_direction_t direction`
Shift direction.
- `flexio_spi_master_transfer_callback_t callback`
FlexIO SPI callback.
- `void * userData`
Callback parameter.

Field Documentation

- (1) `uint8_t* flexio_spi_master_handle_t::txData`
- (2) `uint8_t* flexio_spi_master_handle_t::rxData`
- (3) `size_t flexio_spi_master_handle_t::transferSize`
- (4) `volatile size_t flexio_spi_master_handle_t::txRemainingBytes`
- (5) `volatile size_t flexio_spi_master_handle_t::rxRemainingBytes`
- (6) `volatile uint32_t flexio_spi_master_handle_t::state`
- (7) `flexio_spi_shift_direction_t flexio_spi_master_handle_t::direction`
- (8) `flexio_spi_master_transfer_callback_t flexio_spi_master_handle_t::callback`
- (9) `void* flexio_spi_master_handle_t::userData`

18.5.4 Macro Definition Documentation

18.5.4.1 #define FSL_FLEXIO_SPI_DRIVER_VERSION (MAKE_VERSION(2, 2, 1))

18.5.4.2 #define FLEXIO_SPI_DUMMYDATA (0xFFFFU)

18.5.4.3 #define SPI_RETRY_TIMES 0U /* Define to zero means keep waiting until the flag is assert/deassert. */

18.5.5 Typedef Documentation

18.5.5.1 typedef flexio_spi_master_handle_t flexio_spi_slave_handle_t

18.5.6 Enumeration Type Documentation

18.5.6.1 anonymous enum

Enumerator

kStatus_FLEXIO_SPI_Busy FlexIO SPI is busy.

kStatus_FLEXIO_SPI_Idle SPI is idle.

kStatus_FLEXIO_SPI_Error FlexIO SPI error.

kStatus_FLEXIO_SPI_Timeout FlexIO SPI timeout polling status flags.

18.5.6.2 enum flexio_spi_clock_phase_t

Enumerator

kFLEXIO_SPI_ClockPhaseFirstEdge First edge on SPSCK occurs at the middle of the first cycle of a data transfer.

kFLEXIO_SPI_ClockPhaseSecondEdge First edge on SPSCK occurs at the start of the first cycle of a data transfer.

18.5.6.3 enum flexio_spi_shift_direction_t

Enumerator

kFLEXIO_SPI_MsbFirst Data transfers start with most significant bit.

kFLEXIO_SPI_LsbFirst Data transfers start with least significant bit.

18.5.6.4 enum flexio_spi_data_bitcount_mode_t

Enumerator

kFLEXIO_SPI_8BitMode 8-bit data transmission mode.

kFLEXIO_SPI_16BitMode 16-bit data transmission mode.

18.5.6.5 enum _flexio_spi_interrupt_enable

Enumerator

kFLEXIO_SPI_TxEmptyInterruptEnable Transmit buffer empty interrupt enable.

kFLEXIO_SPI_RxFullInterruptEnable Receive buffer full interrupt enable.

18.5.6.6 enum _flexio_spi_status_flags

Enumerator

kFLEXIO_SPI_TxBufferEmptyFlag Transmit buffer empty flag.

kFLEXIO_SPI_RxBufferFullFlag Receive buffer full flag.

18.5.6.7 enum _flexio_spi_dma_enable

Enumerator

kFLEXIO_SPI_TxDmaEnable Tx DMA request source.

kFLEXIO_SPI_RxDmaEnable Rx DMA request source.

kFLEXIO_SPI_DmaAllEnable All DMA request source.

18.5.6.8 enum _flexio_spi_transfer_flags

Enumerator

kFLEXIO_SPI_8bitMsb FlexIO SPI 8-bit MSB first.
kFLEXIO_SPI_8bitLsb FlexIO SPI 8-bit LSB first.
kFLEXIO_SPI_16bitMsb FlexIO SPI 16-bit MSB first.
kFLEXIO_SPI_16bitLsb FlexIO SPI 16-bit LSB first.

18.5.7 Function Documentation

18.5.7.1 void FLEXIO_SPI_MasterInit (**FLEXIO_SPI_Type** * *base*, **flexio_spi_master_config_t** * *masterConfig*, **uint32_t** *srcClock_Hz*)

The configuration structure can be filled by the user, or be set with default values by the [FLEXIO_SPI_MasterGetDefaultConfig\(\)](#).

Note

1.FlexIO SPI master only support CPOL = 0, which means clock inactive low. 2.For FlexIO SPI master, the input valid time is 1.5 clock cycles, for slave the output valid time is 2.5 clock cycles. So if FlexIO SPI master communicates with other spi IPs, the maximum baud rate is FlexIO clock frequency divided by 2*2=4. If FlexIO SPI master communicates with FlexIO SPI slave, the maximum baud rate is FlexIO clock frequency divided by (1.5+2.5)*2=8.

Example

```
FLEXIO_SPI_Type spiDev = {
    .flexioBase = FLEXIO,
    .SDOPinIndex = 0,
    .SDIPinIndex = 1,
    .SCKPinIndex = 2,
    .CSnPinIndex = 3,
    .shifterIndex = {0,1},
    .timerIndex = {0,1}
};
flexio_spi_master_config_t config = {
    .enableMaster = true,
    .enableInDoze = false,
    .enableInDebug = true,
    .enableFastAccess = false,
    .baudRate_Bps = 500000,
    .phase = kFLEXIO_SPI_ClockPhaseFirstEdge,
    .direction = kFLEXIO_SPI_MsbFirst,
    .dataMode = kFLEXIO_SPI_8BitMode
};
FLEXIO_SPI_MasterInit(&spiDev, &config, srcClock_Hz);
```

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>masterConfig</i>	Pointer to the flexio_spi_master_config_t structure.
<i>srcClock_Hz</i>	FlexIO source clock in Hz.

18.5.7.2 void FLEXIO_SPI_MasterDeinit ([FLEXIO_SPI_Type](#) * *base*)

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type .
-------------	--

18.5.7.3 void FLEXIO_SPI_MasterGetDefaultConfig ([flexio_spi_master_config_t](#) * *masterConfig*)

The configuration can be used directly by calling the [FLEXIO_SPI_MasterConfigure\(\)](#). Example:

```
flexio_spi_master_config_t masterConfig;
FLEXIO\_SPI\_MasterGetDefaultConfig(&masterConfig);
```

Parameters

<i>masterConfig</i>	Pointer to the flexio_spi_master_config_t structure.
---------------------	--

18.5.7.4 void FLEXIO_SPI_SlaveInit ([FLEXIO_SPI_Type](#) * *base*, [flexio_spi_slave_config_t](#) * *slaveConfig*)

The configuration structure can be filled by the user, or be set with default values by the [FLEXIO_SPI_SlaveGetDefaultConfig\(\)](#).

Note

1.Only one timer is needed in the FlexIO SPI slave. As a result, the second timer index is ignored. 2.- FlexIO SPI slave only support CPOL = 0, which means clock inactive low. 3.For FlexIO SPI master, the input valid time is 1.5 clock cycles, for slave the output valid time is 2.5 clock cycles. So if FlexIO SPI slave communicates with other spi IPs, the maximum baud rate is FlexIO clock frequency divided by 3*2=6. If FlexIO SPI slave communicates with FlexIO SPI master, the maximum baud rate is FlexIO clock frequency divided by (1.5+2.5)*2=8. Example

```
FLEXIO\_SPI\_Type spiDev = {
    .flexioBase = FLEXIO,
    .SDOPinIndex = 0,
```

```

.SDIPinIndex = 1,
.SCKPinIndex = 2,
.CSnPinIndex = 3,
.shifterIndex = {0,1},
.timerIndex = {0}
};

flexio_spi_slave_config_t config =
.enableSlave = true,
.enableInDoze = false,
.enableInDebug = true,
.enableFastAccess = false,
.phase = kFLEXIO_SPI_ClockPhaseFirstEdge,
.direction = kFLEXIO_SPI_MsbFirst,
.dataMode = kFLEXIO_SPI_8BitMode
};

FLEXIO_SPI_SlaveInit(&spiDev, &config);

```

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>slaveConfig</i>	Pointer to the flexio_spi_slave_config_t structure.

18.5.7.5 void FLEXIO_SPI_SlaveDeinit ([FLEXIO_SPI_Type](#) * *base*)

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type .
-------------	--

18.5.7.6 void FLEXIO_SPI_SlaveGetDefaultConfig ([flexio_spi_slave_config_t](#) * *slaveConfig*)

The configuration can be used directly for calling the [FLEXIO_SPI_SlaveConfigure\(\)](#). Example:

```

flexio_spi_slave_config_t slaveConfig;
FLEXIO_SPI_SlaveGetDefaultConfig(&slaveConfig);

```

Parameters

<i>slaveConfig</i>	Pointer to the flexio_spi_slave_config_t structure.
--------------------	---

18.5.7.7 uint32_t FLEXIO_SPI_GetStatusFlags ([FLEXIO_SPI_Type](#) * *base*)

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
-------------	---

Returns

status flag; Use the status flag to AND the following flag mask and get the status.

- kFLEXIO_SPI_TxEmptyFlag
- kFLEXIO_SPI_RxEmptyFlag

18.5.7.8 void FLEXIO_SPI_ClearStatusFlags (FLEXIO_SPI_Type * *base*, uint32_t *mask*)

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>mask</i>	status flag The parameter can be any combination of the following values: <ul style="list-style-type: none"> • kFLEXIO_SPI_TxEmptyFlag • kFLEXIO_SPI_RxEmptyFlag

18.5.7.9 void FLEXIO_SPI_EnableInterrupts (FLEXIO_SPI_Type * *base*, uint32_t *mask*)

This function enables the FlexIO SPI interrupt.

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>mask</i>	interrupt source. The parameter can be any combination of the following values: <ul style="list-style-type: none"> • kFLEXIO_SPI_RxFullInterruptEnable • kFLEXIO_SPI_TxEmptyInterruptEnable

18.5.7.10 void FLEXIO_SPI_DisableInterrupts (FLEXIO_SPI_Type * *base*, uint32_t *mask*)

This function disables the FlexIO SPI interrupt.

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>mask</i>	interrupt source The parameter can be any combination of the following values: <ul style="list-style-type: none"> • kFLEXIO_SPI_RxFullInterruptEnable • kFLEXIO_SPI_TxEmptyInterruptEnable

18.5.7.11 void FLEXIO_SPI_EnableDMA ([FLEXIO_SPI_Type](#) * *base*, [uint32_t](#) *mask*, [bool](#) *enable*)

This function enables/disables the FlexIO SPI Tx DMA, which means that asserting the kFLEXIO_SPI-TxEmptyFlag does/doesn't trigger the DMA request.

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>mask</i>	SPI DMA source.
<i>enable</i>	True means enable DMA, false means disable DMA.

18.5.7.12 static [uint32_t](#) FLEXIO_SPI_GetTxDataRegisterAddress ([FLEXIO_SPI_Type](#) * *base*, [flexio_spi_shift_direction_t](#) *direction*) [inline], [[static](#)]

This function returns the SPI data register address, which is mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>direction</i>	Shift direction of MSB first or LSB first.

Returns

FlexIO SPI transmit data register address.

18.5.7.13 static [uint32_t](#) FLEXIO_SPI_GetRxDataRegisterAddress ([FLEXIO_SPI_Type](#) * *base*, [flexio_spi_shift_direction_t](#) *direction*) [inline], [[static](#)]

This function returns the SPI data register address, which is mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>direction</i>	Shift direction of MSB first or LSB first.

Returns

FlexIO SPI receive data register address.

18.5.7.14 static void FLEXIO_SPI_Enable ([FLEXIO_SPI_Type](#) * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type .
<i>enable</i>	True to enable, false does not have any effect.

18.5.7.15 void FLEXIO_SPI_MasterSetBaudRate ([FLEXIO_SPI_Type](#) * *base*, uint32_t *baudRate_Bps*, uint32_t *srcClockHz*)

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>baudRate_Bps</i>	Baud Rate needed in Hz.
<i>srcClockHz</i>	SPI source clock frequency in Hz.

18.5.7.16 static void FLEXIO_SPI_WriteData ([FLEXIO_SPI_Type](#) * *base*, flexio_spi_shift_direction_t *direction*, uint16_t *data*) [inline], [static]

Note

This is a non-blocking API, which returns directly after the data is put into the data register but the data transfer is not finished on the bus. Ensure that the TxEmptyFlag is asserted before calling this API.

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>direction</i>	Shift direction of MSB first or LSB first.
<i>data</i>	8 bit/16 bit data.

18.5.7.17 static uint16_t FLEXIO_SPI_ReadData (FLEXIO_SPI_Type * *base*, flexio_spi_shift_direction_t *direction*) [inline], [static]

Note

This is a non-blocking API, which returns directly after the data is read from the data register. Ensure that the RxFullFlag is asserted before calling this API.

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>direction</i>	Shift direction of MSB first or LSB first.

Returns

8 bit/16 bit data received.

18.5.7.18 status_t FLEXIO_SPI_WriteBlocking (FLEXIO_SPI_Type * *base*, flexio_spi_shift_direction_t *direction*, const uint8_t * *buffer*, size_t *size*)

Note

This function blocks using the polling method until all bytes have been sent.

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>direction</i>	Shift direction of MSB first or LSB first.
<i>buffer</i>	The data bytes to send.

<i>size</i>	The number of data bytes to send.
-------------	-----------------------------------

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_FLEXIO_SPI_Timeout</i>	The transfer timed out and was aborted.

18.5.7.19 status_t FLEXIO_SPI_ReadBlocking (**FLEXIO_SPI_Type** * *base*, **flexio_spi_shift_direction_t** *direction*, **uint8_t** * *buffer*, **size_t** *size*)

Note

This function blocks using the polling method until all bytes have been received.

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>direction</i>	Shift direction of MSB first or LSB first.
<i>buffer</i>	The buffer to store the received bytes.
<i>size</i>	The number of data bytes to be received.
<i>direction</i>	Shift direction of MSB first or LSB first.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_FLEXIO_SPI_Timeout</i>	The transfer timed out and was aborted.

18.5.7.20 status_t FLEXIO_SPI_MasterTransferBlocking (**FLEXIO_SPI_Type** * *base*, **flexio_spi_transfer_t** * *xfer*)

Note

This function blocks via polling until all bytes have been received.

Parameters

<i>base</i>	pointer to FLEXIO_SPI_Type structure
<i>xfer</i>	FlexIO SPI transfer structure, see flexio_spi_transfer_t .

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_FLEXIO_SPI_Timeout</i>	The transfer timed out and was aborted.

18.5.7.21 status_t FLEXIO_SPI_MasterTransferCreateHandle ([FLEXIO_SPI_Type](#) * *base*, [flexio_spi_master_handle_t](#) * *handle*, [flexio_spi_master_transfer_callback_t](#) *callback*, [void](#) * *userData*)

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>handle</i>	Pointer to the flexio_spi_master_handle_t structure to store the transfer state.
<i>callback</i>	The callback function.
<i>userData</i>	The parameter of the callback function.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO type/handle/ISR table out of range.

18.5.7.22 status_t FLEXIO_SPI_MasterTransferNonBlocking ([FLEXIO_SPI_Type](#) * *base*, [flexio_spi_master_handle_t](#) * *handle*, [flexio_spi_transfer_t](#) * *xfer*)

This function sends data using IRQ. This is a non-blocking function, which returns right away. When all data is sent out/received, the callback function is called.

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>handle</i>	Pointer to the flexio_spi_master_handle_t structure to store the transfer state.
<i>xfer</i>	FlexIO SPI transfer structure. See flexio_spi_transfer_t .

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_FLEXIO_SPI_Busy</i>	SPI is not idle, is running another transfer.

18.5.7.23 void FLEXIO_SPI_MasterTransferAbort (**FLEXIO_SPI_Type** * *base*, **flexio_spi_master_handle_t** * *handle*)

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>handle</i>	Pointer to the flexio_spi_master_handle_t structure to store the transfer state.

18.5.7.24 status_t FLEXIO_SPI_MasterTransferGetCount (**FLEXIO_SPI_Type** * *base*, **flexio_spi_master_handle_t** * *handle*, **size_t** * *count*)

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>handle</i>	Pointer to the flexio_spi_master_handle_t structure to store the transfer state.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Return values

<i>kStatus_InvalidArgument</i>	<i>count</i> is Invalid.
<i>kStatus_Success</i>	Successfully return the count.

18.5.7.25 void FLEXIO_SPI_MasterTransferHandleIRQ (**void** * *spiType*, **void** * *spiHandle*)

Parameters

<i>spiType</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>spiHandle</i>	Pointer to the flexio_spi_master_handle_t structure to store the transfer state.

18.5.7.26 status_t **FLEXIO_SPI_SlaveTransferCreateHandle** (FLEXIO_SPI_Type * *base*,
flexio_spi_slave_handle_t * *handle*, flexio_spi_slave_transfer_callback_t
callback, void * *userData*)

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>handle</i>	Pointer to the <code>flexio_spi_slave_handle_t</code> structure to store the transfer state.
<i>callback</i>	The callback function.
<i>userData</i>	The parameter of the callback function.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO type/handle/ISR table out of range.

18.5.7.27 `status_t FLEXIO_SPI_SlaveTransferNonBlocking (FLEXIO_SPI_Type * base, flexio_spi_slave_handle_t * handle, flexio_spi_transfer_t * xfer)`

This function sends data using IRQ. This is a non-blocking function, which returns right away. When all data is sent out/received, the callback function is called.

Parameters

<i>handle</i>	Pointer to the <code>flexio_spi_slave_handle_t</code> structure to store the transfer state.
<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>xfer</i>	FlexIO SPI transfer structure. See flexio_spi_transfer_t .

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_FLEXIO_SPI_Busy</i>	SPI is not idle; it is running another transfer.

18.5.7.28 `static void FLEXIO_SPI_SlaveTransferAbort (FLEXIO_SPI_Type * base, flexio_spi_slave_handle_t * handle) [inline], [static]`

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>handle</i>	Pointer to the flexio_spi_slave_handle_t structure to store the transfer state.

18.5.7.29 static status_t FLEXIO_SPI_SlaveTransferGetCount (FLEXIO_SPI_Type * *base*, flexio_spi_slave_handle_t * *handle*, size_t * *count*) [inline], [static]

Parameters

<i>base</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>handle</i>	Pointer to the flexio_spi_slave_handle_t structure to store the transfer state.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Return values

<i>kStatus_InvalidArgument</i>	count is Invalid.
<i>kStatus_Success</i>	Successfully return the count.

18.5.7.30 void FLEXIO_SPI_SlaveTransferHandleIRQ (void * *spiType*, void * *spiHandle*)

Parameters

<i>spiType</i>	Pointer to the FLEXIO_SPI_Type structure.
<i>spiHandle</i>	Pointer to the flexio_spi_slave_handle_t structure to store the transfer state.

18.6 FlexIO UART Driver

18.6.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Universal Asynchronous Receiver/Transmitter (UART) function using the Flexible I/O.

FlexIO UART driver includes functional APIs and transactional APIs. Functional APIs target low-level APIs. Functional APIs can be used for the FlexIO UART initialization/configuration/operation for optimization/customization purpose. Using the functional APIs requires the knowledge of the FlexIO UART peripheral and how to organize functional APIs to meet the application requirements. All functional API use the [FLEXIO_UART_Type](#) * as the first parameter. FlexIO UART functional operation groups provide the functional APIs set.

Transactional APIs target high-level APIs. Transactional APIs can be used to enable the peripheral and also in the application if the code size and performance of transactional APIs satisfy requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code. All transactional APIs use the `flexio_uart_handle_t` as the second parameter. Initialize the handle by calling the [FLEXIO_UART_TransferCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer. This means that the functions `FLEXIO_UART_SendNonBlocking()` and `FLEXIO_UART_ReceiveNonBlocking()` set up an interrupt for data transfer. When the transfer is complete, the upper layer is notified through a callback function with the `kStatus_FLEXIO_UART_TxIdle` and `kStatus_FLEXIO_UART_RxIdle` status.

Transactional receive APIs support the ring buffer. Prepare the memory for the ring buffer and pass in the start address and size through calling the `FLEXIO_UART_InstallRingBuffer()`. When the ring buffer is enabled, the received data is saved to the ring buffer in the background. The function `FLEXIO_UART_ReceiveNonBlocking()` first gets data from the ring buffer. If ring buffer does not have enough data, the function returns the data to the ring buffer and saves the received data to user memory. When all data is received, the upper layer is informed through a callback with the `kStatus_FLEXIO_UART_RxIdle` status.

If the receive ring buffer is full, the upper layer is informed through a callback with status `kStatus_FLEXIO_UART_RxRingBufferOverrun`. In the callback function, the upper layer reads data from the ring buffer. If not, the oldest data is overwritten by the new data.

The ring buffer size is specified when calling the `FLEXIO_UART_InstallRingBuffer`. Note that one byte is reserved for the ring buffer maintenance. Create a handle as follows.

```
FLEXIO_UART_InstallRingBuffer(&uartDev, &handle, &ringBuffer, 32);
```

In this example, the buffer size is 32. However, only 31 bytes are used for saving data.

18.6.2 Typical use case

18.6.2.1 FlexIO UART send/receive using a polling method

```
uint8_t ch;
```

```

FLEXIO_UART_Type uartDev;
status_t result = kStatus_Success;
flexio_uart_user_config user_config;
FLEXIO_UART_GetDefaultConfig(&user_config);
user_config.baudRate_Bps = 115200U;
user_config.enableUart = true;

uartDev.flexioBase = BOARD_FLEXIO_BASE;
uartDev.TxPinIndex = FLEXIO_UART_TX_PIN;
uartDev.RxPinIndex = FLEXIO_UART_RX_PIN;
uartDev.shifterIndex[0] = 0U;
uartDev.shifterIndex[1] = 1U;
uartDev.timerIndex[0] = 0U;
uartDev.timerIndex[1] = 1U;

result = FLEXIO_UART_Init(&uartDev, &user_config, 48000000U);
//Check if configuration is correct.
if(result != kStatus_Success)
{
    return;
}
FLEXIO_UART_WriteBlocking(&uartDev, txbuff, sizeof(txbuff));

while(1)
{
    FLEXIO_UART_ReadBlocking(&uartDev, &ch, 1);
    FLEXIO_UART_WriteBlocking(&uartDev, &ch, 1);
}

```

18.6.2.2 FlexIO UART send/receive using an interrupt method

```

FLEXIO_UART_Type uartDev;
flexio_uart_handle_t g_uartHandle;
flexio_uart_config_t user_config;
flexio_uart_transfer_t sendXfer;
flexio_uart_transfer_t receiveXfer;
volatile bool txFinished;
volatile bool rxFinished;
uint8_t sendData[] = {'H', 'e', 'l', 'l', 'o'};
uint8_t receiveData[32];

void FLEXIO_UART_UserCallback(FLEXIO_UART_Type *base, flexio_uart_handle_t *handle,
    status_t status, void *userData)
{
    userData = userData;

    if (kStatus_FLEXIO_UART_TxIdle == status)
    {
        txFinished = true;
    }

    if (kStatus_FLEXIO_UART_RxIdle == status)
    {
        rxFinished = true;
    }
}

void main(void)
{
    //...

    FLEXIO_UART_GetDefaultConfig(&user_config);
    user_config.baudRate_Bps = 115200U;
    user_config.enableUart = true;
}

```

```

uartDev.flexioBase = BOARD_FLEXIO_BASE;
uartDev.TxPinIndex = FLEXIO_UART_TX_PIN;
uartDev.RxPinIndex = FLEXIO_UART_RX_PIN;
uartDev.shifterIndex[0] = 0U;
uartDev.shifterIndex[1] = 1U;
uartDev.timerIndex[0] = 0U;
uartDev.timerIndex[1] = 1U;

result = FLEXIO_UART_Init(&uartDev, &user_config, 1200000000U);
//Check if configuration is correct.
if(result != kStatus_Success)
{
    return;
}

FLEXIO_UART_TransferCreateHandle(&uartDev, &g_uartHandle,
    FLEXIO_UART_UserCallback, NULL);

// Prepares to send.
sendXfer.data = sendData;
sendXfer.dataSize = sizeof(sendData)/sizeof(sendData[0]);
txFinished = false;

// Sends out.
FLEXIO_UART_SendNonBlocking(&uartDev, &g_uartHandle, &sendXfer);

// Send finished.
while (!txFinished)
{
}

// Prepares to receive.
receiveXfer.data = receiveData;
receiveXfer.dataSize = sizeof(receiveData)/sizeof(receiveData[0]);
rxFinished = false;

// Receives.
FLEXIO_UART_ReceiveNonBlocking(&uartDev, &g_uartHandle, &receiveXfer, NULL);

// Receive finished.
while (!rxFinished)
{
}

// ...
}

```

18.6.2.3 FlexIO UART receive using the ringbuffer feature

```

#define RING_BUFFER_SIZE 64
#define RX_DATA_SIZE      32

FLEXIO_UART_Type uartDev;
flexio_uart_handle_t g_uartHandle;
flexio_uart_config_t user_config;
flexio_uart_transfer_t sendXfer;
flexio_uart_transfer_t receiveXfer;
volatile bool txFinished;
volatile bool rxFinished;
uint8_t receiveData[RX_DATA_SIZE];
uint8_t ringBuffer[RING_BUFFER_SIZE];

void FLEXIO_UART_UserCallback(FLEXIO_UART_Type *base, flexio_uart_handle_t *handle,
    status_t status, void *userData)
{

```

```

userData = userData;

if (kStatus_FLEXIO_UART_RxIdle == status)
{
    rxFinished = true;
}
}

void main(void)
{
    size_t bytesRead;
    //...

    FLEXIO_UART_GetDefaultConfig(&user_config);
    user_config.baudRate_Bps = 115200U;
    user_config.enableUart = true;

    uartDev.flexioBase = BOARD_FLEXIO_BASE;
    uartDev.TxPinIndex = FLEXIO_UART_TX_PIN;
    uartDev.RxPinIndex = FLEXIO_UART_RX_PIN;
    uartDev.shifterIndex[0] = 0U;
    uartDev.shifterIndex[1] = 1U;
    uartDev.timerIndex[0] = 0U;
    uartDev.timerIndex[1] = 1U;

    result = FLEXIO_UART_Init(&uartDev, &user_config, 48000000U);
    //Check if configuration is correct.
    if(result != kStatus_Success)
    {
        return;
    }

    FLEXIO_UART_TransferCreateHandle(&uartDev, &g_uartHandle,
        FLEXIO_UART_UserCallback, NULL);
    FLEXIO_UART_InstallRingBuffer(&uartDev, &g_uartHandle, ringBuffer, RING_BUFFER_SIZE);

    // Receive is working in the background to the ring buffer.

    // Prepares to receive.
    receiveXfer.data = receiveData;
    receiveXfer.dataSize = RX_DATA_SIZE;
    rxFinished = false;

    // Receives.
    FLEXIO_UART_ReceiveNonBlocking(&uartDev, &g_uartHandle, &receiveXfer, &bytesRead);

    if (bytesRead == RX_DATA_SIZE) /* Have read enough data. */
    {
        ;
    }
    else
    {
        if (bytesRead) /* Received some data, process first. */
        {
            ;
        }

        // Receive finished.
        while (!rxFinished)
        {
        }
    }
}

// ...
}

```

18.6.2.4 FlexIO UART send/receive using a DMA method

```

FLEXIO_UART_Type uartDev;
flexio_uart_handle_t g_uartHandle;
dma_handle_t g_uartTxDmaHandle;
dma_handle_t g_uartRxDmaHandle;
flexio_uart_config_t user_config;
flexio_uart_transfer_t sendXfer;
flexio_uart_transfer_t receiveXfer;
volatile bool txFinished;
volatile bool rxFinished;
uint8_t sendData[] = {'H', 'e', 'l', 'l', 'o'};
uint8_t receiveData[32];

void FLEXIO_UART_UserCallback(FLEXIO_UART_Type *base, flexio_uart_handle_t *handle,
    status_t status, void *userData)
{
    userData = userData;

    if (kStatus_FLEXIO_UART_TxIdle == status)
    {
        txFinished = true;
    }

    if (kStatus_FLEXIO_UART_RxIdle == status)
    {
        rxFinished = true;
    }
}

void main(void)
{
    //...

    FLEXIO_UART_GetDefaultConfig(&user_config);
    user_config.baudRate_Bps = 115200U;
    user_config.enableUart = true;

    uartDev.flexioBase = BOARD_FLEXIO_BASE;
    uartDev.TxPinIndex = FLEXIO_UART_TX_PIN;
    uartDev.RxPinIndex = FLEXIO_UART_RX_PIN;
    uartDev.shifterIndex[0] = 0U;
    uartDev.shifterIndex[1] = 1U;
    uartDev.timerIndex[0] = 0U;
    uartDev.timerIndex[1] = 1U;
    result = FLEXIO_UART_Init(&uartDev, &user_config, 48000000U);
    //Check if configuration is correct.
    if(result != kStatus_Success)
    {
        return;
    }

    /* Init DMAMUX. */
    DMAMUX_Init(EXAMPLE_FLEXIO_UART_DMAMUX_BASEADDR)

    /* Init the DMA/EDMA module */
#if defined(FSL_FEATURE_SOC_DMA_COUNT) && FSL_FEATURE_SOC_DMA_COUNT > 0U
    DMA_Init(EXAMPLE_FLEXIO_UART_DMA_BASEADDR);
    DMA_CreateHandle(&g_uartTxDmaHandle, EXAMPLE_FLEXIO_UART_DMA_BASEADDR, FLEXIO_UART_TX_DMA_CHANNEL);
    DMA_CreateHandle(&g_uartRxDmaHandle, EXAMPLE_FLEXIO_UART_DMA_BASEADDR, FLEXIO_UART_RX_DMA_CHANNEL);
#endif /* FSL_FEATURE_SOC_DMA_COUNT */

#if defined(FSL_FEATURE_SOC_EDMA_COUNT) && FSL_FEATURE_SOC_EDMA_COUNT > 0U
    edma_config_t edmaConfig;

    EDMA_GetDefaultConfig(&edmaConfig);
    EDMA_Init(EXAMPLE_FLEXIO_UART_DMA_BASEADDR, &edmaConfig);

```

```

    EDMA_CreateHandle(&g_uartTxDmaHandle, EXAMPLE_FLEXIO_UART_DMA_BASEADDR,
FLEXIO_UART_TX_DMA_CHANNEL);
    EDMA_CreateHandle(&g_uartRxDmaHandle, EXAMPLE_FLEXIO_UART_DMA_BASEADDR,
FLEXIO_UART_RX_DMA_CHANNEL);
#endif /* FSL_FEATURE_SOC_EDMA_COUNT */

dma_request_source_tx = (dma_request_source_t)(FLEXIO_DMA_REQUEST_BASE + uartDev.
shifterIndex[0]);
dma_request_source_rx = (dma_request_source_t)(FLEXIO_DMA_REQUEST_BASE + uartDev.
shifterIndex[1]);

/* Requests DMA channels for transmit and receive. */
DMAMUX_SetSource(EXAMPLE_FLEXIO_UART_DMAMUX_BASEADDR, FLEXIO_UART_TX_DMA_CHANNEL, (
dma_request_source_t)dma_request_source_tx);
DMAMUX_SetSource(EXAMPLE_FLEXIO_UART_DMAMUX_BASEADDR, FLEXIO_UART_RX_DMA_CHANNEL, (
dma_request_source_t)dma_request_source_rx);
DMAMUX_EnableChannel(EXAMPLE_FLEXIO_UART_DMAMUX_BASEADDR,
FLEXIO_UART_TX_DMA_CHANNEL);
DMAMUX_EnableChannel(EXAMPLE_FLEXIO_UART_DMAMUX_BASEADDR,
FLEXIO_UART_RX_DMA_CHANNEL);

FLEXIO_UART_TransferCreateHandleDMA(&uartDev, &g_uartHandle, FLEXIO_UART_UserCallback, NULL, &
g_uartTxDmaHandle, &g_uartRxDmaHandle);

// Prepares to send.
sendXfer.data = sendData;
sendXfer.dataSize = sizeof(sendData)/sizeof(sendData[0]);
txFinished = false;

// Sends out.
FLEXIO_UART_SendDMA(&uartDev, &g_uartHandle, &sendXfer);

// Send finished.
while (!txFinished)
{
}

// Prepares to receive.
receiveXfer.data = receiveData;
receiveXfer.dataSize = sizeof(receiveData)/sizeof(receiveData[0]);
rxFinished = false;

// Receives.
FLEXIO_UART_ReceiveDMA(&uartDev, &g_uartHandle, &receiveXfer, NULL);

// Receive finished.
while (!rxFinished)
{
}

// ...
}

```

Data Structures

- struct [FLEXIO_UART_Type](#)
Define FlexIO UART access structure typedef. [More...](#)
- struct [flexio_uart_config_t](#)
Define FlexIO UART user configuration structure. [More...](#)
- struct [flexio_uart_transfer_t](#)
Define FlexIO UART transfer structure. [More...](#)
- struct [flexio_uart_handle_t](#)

Define FLEXIO UART handle structure. [More...](#)

Macros

- `#define UART_RETRY_TIMES 0U /* Defining to zero means to keep waiting for the flag until it is assert/deassert. */`
Retry times for waiting flag.

Typedefs

- `typedef void(* flexio_uart_transfer_callback_t)(FLEXIO_UART_Type *base, flexio_uart_handle_t *handle, status_t status, void *userData)`
FlexIO UART transfer callback function.

Enumerations

- `enum {`
`kStatus_FLEXIO_UART_TxBusy = MAKE_STATUS(kStatusGroup_FLEXIO_UART, 0),`
`kStatus_FLEXIO_UART_RxBusy = MAKE_STATUS(kStatusGroup_FLEXIO_UART, 1),`
`kStatus_FLEXIO_UART_TxIdle = MAKE_STATUS(kStatusGroup_FLEXIO_UART, 2),`
`kStatus_FLEXIO_UART_RxIdle = MAKE_STATUS(kStatusGroup_FLEXIO_UART, 3),`
`kStatus_FLEXIO_UART_ERROR = MAKE_STATUS(kStatusGroup_FLEXIO_UART, 4),`
`kStatus_FLEXIO_UART_RxRingBufferOverrun,`
`kStatus_FLEXIO_UART_RxHardwareOverrun = MAKE_STATUS(kStatusGroup_FLEXIO_UART, 6),`
`kStatus_FLEXIO_UART_Timeout = MAKE_STATUS(kStatusGroup_FLEXIO_UART, 7),`
`kStatus_FLEXIO_UART_BaudrateNotSupport }`
Error codes for the UART driver.
- `enum flexio_uart_bit_count_per_char_t {`
`kFLEXIO_UART_7BitsPerChar = 7U,`
`kFLEXIO_UART_8BitsPerChar = 8U,`
`kFLEXIO_UART_9BitsPerChar = 9U }`
FlexIO UART bit count per char.
- `enum _flexio_uart_interrupt_enable {`
`kFLEXIO_UART_TxDataRegEmptyInterruptEnable = 0x1U,`
`kFLEXIO_UART_RxDataRegFullInterruptEnable = 0x2U }`
Define FlexIO UART interrupt mask.
- `enum _flexio_uart_status_flags {`
`kFLEXIO_UART_TxDataRegEmptyFlag = 0x1U,`
`kFLEXIO_UART_RxDataRegFullFlag = 0x2U,`
`kFLEXIO_UART_RxOverRunFlag = 0x4U }`
Define FlexIO UART status mask.

Driver version

- #define **FSL_FLEXIO_UART_DRIVER_VERSION** (MAKE_VERSION(2, 4, 0))
FlexIO UART driver version.

Initialization and deinitialization

- **status_t FLEXIO_UART_Init** (**FLEXIO_UART_Type** *base, const **flexio_uart_config_t** *userConfig, **uint32_t** srcClock_Hz)
Ungates the FlexIO clock, resets the FlexIO module, configures FlexIO UART hardware, and configures the FlexIO UART with FlexIO UART configuration.
- **void FLEXIO_UART_Deinit** (**FLEXIO_UART_Type** *base)
Resets the FlexIO UART shifter and timer config.
- **void FLEXIO_UART_GetDefaultConfig** (**flexio_uart_config_t** *userConfig)
Gets the default configuration to configure the FlexIO UART.

Status

- **uint32_t FLEXIO_UART_GetStatusFlags** (**FLEXIO_UART_Type** *base)
Gets the FlexIO UART status flags.
- **void FLEXIO_UART_ClearStatusFlags** (**FLEXIO_UART_Type** *base, **uint32_t** mask)
Gets the FlexIO UART status flags.

Interrupts

- **void FLEXIO_UART_EnableInterrupts** (**FLEXIO_UART_Type** *base, **uint32_t** mask)
Enables the FlexIO UART interrupt.
- **void FLEXIO_UART_DisableInterrupts** (**FLEXIO_UART_Type** *base, **uint32_t** mask)
Disables the FlexIO UART interrupt.

DMA Control

- **static uint32_t FLEXIO_UART_GetTxDataRegisterAddress** (**FLEXIO_UART_Type** *base)
Gets the FlexIO UARt transmit data register address.
- **static uint32_t FLEXIO_UART_GetRxDataRegisterAddress** (**FLEXIO_UART_Type** *base)
Gets the FlexIO UART receive data register address.
- **static void FLEXIO_UART_EnableTxDMA** (**FLEXIO_UART_Type** *base, **bool** enable)
Enables/disables the FlexIO UART transmit DMA.
- **static void FLEXIO_UART_EnableRxDMA** (**FLEXIO_UART_Type** *base, **bool** enable)
Enables/disables the FlexIO UART receive DMA.

Bus Operations

- **static void FLEXIO_UART_Enable** (**FLEXIO_UART_Type** *base, **bool** enable)

Enables/disables the FlexIO UART module operation.

- static void **FLEXIO_UART_WriteByte** (**FLEXIO_UART_Type** *base, const uint8_t *buffer)
Writes one byte of data.
- static void **FLEXIO_UART_ReadByte** (**FLEXIO_UART_Type** *base, uint8_t *buffer)
Reads one byte of data.
- **status_t FLEXIO_UART_WriteBlocking** (**FLEXIO_UART_Type** *base, const uint8_t *txData, size_t txSize)
Sends a buffer of data bytes.
- **status_t FLEXIO_UART_ReadBlocking** (**FLEXIO_UART_Type** *base, uint8_t *rxData, size_t rxSize)
Receives a buffer of bytes.

Transactional

- **status_t FLEXIO_UART_TransferCreateHandle** (**FLEXIO_UART_Type** *base, flexio_uart_handle_t *handle, flexio_uart_transfer_callback_t callback, void *userData)
Initializes the UART handle.
- void **FLEXIO_UART_TransferStartRingBuffer** (**FLEXIO_UART_Type** *base, flexio_uart_handle_t *handle, uint8_t *ringBuffer, size_t ringBufferSize)
Sets up the RX ring buffer.
- void **FLEXIO_UART_TransferStopRingBuffer** (**FLEXIO_UART_Type** *base, flexio_uart_handle_t *handle)
Aborts the background transfer and uninstalls the ring buffer.
- **status_t FLEXIO_UART_TransferSendNonBlocking** (**FLEXIO_UART_Type** *base, flexio_uart_handle_t *handle, flexio_uart_transfer_t *xfer)
Transmits a buffer of data using the interrupt method.
- void **FLEXIO_UART_TransferAbortSend** (**FLEXIO_UART_Type** *base, flexio_uart_handle_t *handle)
Aborts the interrupt-driven data transmit.
- **status_t FLEXIO_UART_TransferGetSendCount** (**FLEXIO_UART_Type** *base, flexio_uart_handle_t *handle, size_t *count)
Gets the number of bytes sent.
- **status_t FLEXIO_UART_TransferReceiveNonBlocking** (**FLEXIO_UART_Type** *base, flexio_uart_handle_t *handle, flexio_uart_transfer_t *xfer, size_t *receivedBytes)
Receives a buffer of data using the interrupt method.
- void **FLEXIO_UART_TransferAbortReceive** (**FLEXIO_UART_Type** *base, flexio_uart_handle_t *handle)
Aborts the receive data which was using IRQ.
- **status_t FLEXIO_UART_TransferGetReceiveCount** (**FLEXIO_UART_Type** *base, flexio_uart_handle_t *handle, size_t *count)
Gets the number of bytes received.
- void **FLEXIO_UART_TransferHandleIRQ** (void *uartType, void *uartHandle)
FlexIO UART IRQ handler function.

18.6.3 Data Structure Documentation

18.6.3.1 struct FLEXIO_UART_Type

Data Fields

- `FLEXIO_Type * flexioBase`
FlexIO base pointer.
- `uint8_t TxPinIndex`
Pin select for UART_Tx.
- `uint8_t RxPinIndex`
Pin select for UART_Rx.
- `uint8_t shifterIndex [2]`
Shifter index used in FlexIO UART.
- `uint8_t timerIndex [2]`
Timer index used in FlexIO UART.

Field Documentation

- (1) `FLEXIO_Type* FLEXIO_UART_Type::flexioBase`
- (2) `uint8_t FLEXIO_UART_Type::TxPinIndex`
- (3) `uint8_t FLEXIO_UART_Type::RxPinIndex`
- (4) `uint8_t FLEXIO_UART_Type::shifterIndex[2]`
- (5) `uint8_t FLEXIO_UART_Type::timerIndex[2]`

18.6.3.2 struct flexio_uart_config_t

Data Fields

- `bool enableUart`
Enable/disable FlexIO UART TX & RX.
- `bool enableInDoze`
Enable/disable FlexIO operation in doze mode.
- `bool enableInDebug`
Enable/disable FlexIO operation in debug mode.
- `bool enableFastAccess`
*Enable/disable fast access to FlexIO registers,
fast access requires the FlexIO clock to be at least twice the frequency of the bus clock.*
- `uint32_t baudRate_Bps`
Baud rate in Bps.
- `flexio_uart_bit_count_per_char_t bitCountPerChar`
number of bits, 7/8/9 -bit

Field Documentation

- (1) `bool flexio_uart_config_t::enableUart`
- (2) `bool flexio_uart_config_t::enableFastAccess`

(3) `uint32_t flexio_uart_config_t::baudRate_Bps`

18.6.3.3 struct flexio_uart_transfer_t

Data Fields

- `size_t dataSize`
Transfer size.
- `uint8_t * data`
The buffer of data to be transfer.
- `uint8_t * rxData`
The buffer to receive data.
- `const uint8_t * txData`
The buffer of data to be sent.

Field Documentation

- (1) `uint8_t* flexio_uart_transfer_t::data`
- (2) `uint8_t* flexio_uart_transfer_t::rxData`
- (3) `const uint8_t* flexio_uart_transfer_t::txData`

18.6.3.4 struct _flexio_uart_handle

Data Fields

- `const uint8_t *volatile txData`
Address of remaining data to send.
- `volatile size_t txDataSize`
Size of the remaining data to send.
- `uint8_t *volatile rxData`
Address of remaining data to receive.
- `volatile size_t rxDataSize`
Size of the remaining data to receive.
- `size_t txDataSizeAll`
Total bytes to be sent.
- `size_t rxDataSizeAll`
Total bytes to be received.
- `uint8_t * rxRingBuffer`
Start address of the receiver ring buffer.
- `size_t rxRingBufferSize`
Size of the ring buffer.
- `volatile uint16_t rxRingBufferHead`
Index for the driver to store received data into ring buffer.
- `volatile uint16_t rxRingBufferTail`
Index for the user to get data from the ring buffer.
- `flexio_uart_transfer_callback_t callback`
Callback function.
- `void * userData`
UART callback function parameter.

- volatile uint8_t **txState**
TX transfer state.
- volatile uint8_t **rxState**
RX transfer state.

Field Documentation

- (1) const uint8_t* volatile flexio_uart_handle_t::txData
- (2) volatile size_t flexio_uart_handle_t::txDataSize
- (3) uint8_t* volatile flexio_uart_handle_t::rxData
- (4) volatile size_t flexio_uart_handle_t::rxDataSize
- (5) size_t flexio_uart_handle_t::txDataSizeAll
- (6) size_t flexio_uart_handle_t::rxDataSizeAll
- (7) uint8_t* flexio_uart_handle_t::rxRingBuffer
- (8) size_t flexio_uart_handle_t::rxRingBufferSize
- (9) volatile uint16_t flexio_uart_handle_t::rxRingBufferHead
- (10) volatile uint16_t flexio_uart_handle_t::rxRingBufferTail
- (11) flexio_uart_transfer_callback_t flexio_uart_handle_t::callback
- (12) void* flexio_uart_handle_t::userData
- (13) volatile uint8_t flexio_uart_handle_t::txState

18.6.4 Macro Definition Documentation

18.6.4.1 #define FSL_FLEXIO_UART_DRIVER_VERSION (MAKE_VERSION(2, 4, 0))

18.6.4.2 #define UART_RETRY_TIMES 0U /* Defining to zero means to keep waiting for the flag until it is assert/deassert. */

18.6.5 Typedef Documentation

18.6.5.1 typedef void(* flexio_uart_transfer_callback_t)(FLEXIO_UART_Type *base, flexio_uart_handle_t *handle, status_t status, void *userData)

18.6.6 Enumeration Type Documentation

18.6.6.1 anonymous enum

Enumerator

kStatus_FLEXIO_UART_TxBusy Transmitter is busy.
kStatus_FLEXIO_UART_RxBusy Receiver is busy.
kStatus_FLEXIO_UART_TxIdle UART transmitter is idle.
kStatus_FLEXIO_UART_RxIdle UART receiver is idle.
kStatus_FLEXIO_UART_Error ERROR happens on UART.
kStatus_FLEXIO_UART_RxRingBufferOverrun UART RX software ring buffer overrun.
kStatus_FLEXIO_UART_RxHardwareOverrun UART RX receiver overrun.
kStatus_FLEXIO_UART_Timeout UART times out.
kStatus_FLEXIO_UART_BaudrateNotSupport Baudrate is not supported in current clock source.

18.6.6.2 enum flexio_uart_bit_count_per_char_t

Enumerator

kFLEXIO_UART_7BitsPerChar 7-bit data characters
kFLEXIO_UART_8BitsPerChar 8-bit data characters
kFLEXIO_UART_9BitsPerChar 9-bit data characters

18.6.6.3 enum _flexio_uart_interrupt_enable

Enumerator

kFLEXIO_UART_TxDataRegEmptyInterruptEnable Transmit buffer empty interrupt enable.
kFLEXIO_UART_RxDataRegFullInterruptEnable Receive buffer full interrupt enable.

18.6.6.4 enum _flexio_uart_status_flags

Enumerator

kFLEXIO_UART_TxDataRegEmptyFlag Transmit buffer empty flag.
kFLEXIO_UART_RxDataRegFullFlag Receive buffer full flag.
kFLEXIO_UART_RxOverRunFlag Receive buffer over run flag.

18.6.7 Function Documentation

18.6.7.1 status_t FLEXIO_UART_Init (FLEXIO_UART_Type * *base*, const flexio_uart_config_t * *userConfig*, uint32_t *srcClock_Hz*)

The configuration structure can be filled by the user or be set with default values by [FLEXIO_UART_GetDefaultConfig\(\)](#).

Example

```
FLEXIO_UART_Type base = {
    .flexioBase = FLEXIO,
    .TxPinIndex = 0,
    .RxPinIndex = 1,
    .shifterIndex = {0,1},
    .timerIndex = {0,1}
};
flexio_uart_config_t config = {
    .enableInDoze = false,
    .enableInDebug = true,
    .enableFastAccess = false,
    .baudRate_Bps = 115200U,
    .bitCountPerChar = 8
};
FLEXIO_UART_Init(base, &config, srcClock_Hz);
```

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>userConfig</i>	Pointer to the flexio_uart_config_t structure.
<i>srcClock_Hz</i>	FlexIO source clock in Hz.

Return values

<i>kStatus_Success</i>	Configuration success.
<i>kStatus_FLEXIO_UART_BaudrateNotSupport</i>	Baudrate is not supported for current clock source frequency.

18.6.7.2 void FLEXIO_UART_Deinit (FLEXIO_UART_Type * *base*)

Note

After calling this API, call the [FLEXIO_UART_Init](#) to use the FlexIO UART module.

Parameters

<i>base</i>	Pointer to FLEXIO_UART_Type structure
-------------	---

18.6.7.3 void FLEXIO_UART_GetDefaultConfig ([flexio_uart_config_t](#) * *userConfig*)

The configuration can be used directly for calling the [FLEXIO_UART_Init\(\)](#). Example:

```
flexio_uart_config_t config;
FLEXIO\_UART\_GetDefaultConfig(&userConfig);
```

Parameters

<i>userConfig</i>	Pointer to the flexio_uart_config_t structure.
-------------------	--

18.6.7.4 uint32_t FLEXIO_UART_GetStatusFlags ([FLEXIO_UART_Type](#) * *base*)

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
-------------	--

Returns

FlexIO UART status flags.

18.6.7.5 void FLEXIO_UART_ClearStatusFlags ([FLEXIO_UART_Type](#) * *base*, [uint32_t](#) *mask*)

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>mask</i>	Status flag. The parameter can be any combination of the following values: <ul style="list-style-type: none"> • kFLEXIO_UART_TxDataRegEmptyFlag • kFLEXIO_UART_RxEmptyFlag • kFLEXIO_UART_RxOverRunFlag

18.6.7.6 void FLEXIO_UART_EnableInterrupts ([FLEXIO_UART_Type](#) * *base*, [uint32_t](#) *mask*)

This function enables the FlexIO UART interrupt.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>mask</i>	Interrupt source.

18.6.7.7 void FLEXIO_UART_DisableInterrupts ([FLEXIO_UART_Type](#) * *base*, [uint32_t](#) *mask*)

This function disables the FlexIO UART interrupt.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>mask</i>	Interrupt source.

18.6.7.8 static [uint32_t](#) FLEXIO_UART_GetTxDataRegisterAddress ([FLEXIO_UART_Type](#) * *base*) [inline], [static]

This function returns the UART data register address, which is mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
-------------	--

Returns

FlexIO UART transmit data register address.

18.6.7.9 static [uint32_t](#) FLEXIO_UART_GetRxDataRegisterAddress ([FLEXIO_UART_Type](#) * *base*) [inline], [static]

This function returns the UART data register address, which is mainly used by DMA/eDMA.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
-------------	--

Returns

FlexIO UART receive data register address.

18.6.7.10 static void FLEXIO_UART_EnableTxDMA (FLEXIO_UART_Type * *base*, bool *enable*) [inline], [static]

This function enables/disables the FlexIO UART Tx DMA, which means asserting the kFLEXIO_UART_TxDataRegEmptyFlag does/doesn't trigger the DMA request.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>enable</i>	True to enable, false to disable.

18.6.7.11 static void FLEXIO_UART_EnableRxDMA ([FLEXIO_UART_Type](#) * *base*, *bool enable*) [inline], [static]

This function enables/disables the FlexIO UART Rx DMA, which means asserting kFLEXIO_UART_RxDataRegFullFlag does/doesn't trigger the DMA request.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>enable</i>	True to enable, false to disable.

18.6.7.12 static void FLEXIO_UART_Enable ([FLEXIO_UART_Type](#) * *base*, *bool enable*) [inline], [static]

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type .
<i>enable</i>	True to enable, false does not have any effect.

18.6.7.13 static void FLEXIO_UART_WriteByte ([FLEXIO_UART_Type](#) * *base*, *const uint8_t* * *buffer*) [inline], [static]

Note

This is a non-blocking API, which returns directly after the data is put into the data register. Ensure that the TxEmptyFlag is asserted before calling this API.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
-------------	--

<i>buffer</i>	The data bytes to send.
---------------	-------------------------

18.6.7.14 static void FLEXIO_UART_ReadByte (FLEXIO_UART_Type * *base*, uint8_t * *buffer*) [inline], [static]

Note

This is a non-blocking API, which returns directly after the data is read from the data register. Ensure that the RxFullFlag is asserted before calling this API.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>buffer</i>	The buffer to store the received bytes.

18.6.7.15 status_t FLEXIO_UART_WriteBlocking (FLEXIO_UART_Type * *base*, const uint8_t * *txData*, size_t *txSize*)

Note

This function blocks using the polling method until all bytes have been sent.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>txData</i>	The data bytes to send.
<i>txSize</i>	The number of data bytes to send.

Return values

<i>kStatus_FLEXIO_UART_Timeout</i>	Transmission timed out and was aborted.
<i>kStatus_Success</i>	Successfully wrote all data.

18.6.7.16 status_t FLEXIO_UART_ReadBlocking (FLEXIO_UART_Type * *base*, uint8_t * *rxData*, size_t *rxSize*)

Note

This function blocks using the polling method until all bytes have been received.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>rxData</i>	The buffer to store the received bytes.
<i>rxSize</i>	The number of data bytes to be received.

Return values

<i>kStatus_FLEXIO_UART_Timeout</i>	Transmission timed out and was aborted.
<i>kStatus_Success</i>	Successfully received all data.

18.6.7.17 status_t FLEXIO_UART_TransferCreateHandle ([FLEXIO_UART_Type](#) * *base*, [flexio_uart_handle_t](#) * *handle*, [flexio_uart_transfer_callback_t](#) *callback*, [void](#) * *userData*)

This function initializes the FlexIO UART handle, which can be used for other FlexIO UART transactional APIs. Call this API once to get the initialized handle.

The UART driver supports the "background" receiving, which means that users can set up a RX ring buffer optionally. Data received is stored into the ring buffer even when the user doesn't call the [FLEXIO_UART_TransferReceiveNonBlocking\(\)](#) API. If there is already data received in the ring buffer, users can get the received data from the ring buffer directly. The ring buffer is disabled if passing NULL as *ringBuffer*.

Parameters

<i>base</i>	to FLEXIO_UART_Type structure.
<i>handle</i>	Pointer to the flexio_uart_handle_t structure to store the transfer state.
<i>callback</i>	The callback function.
<i>userData</i>	The parameter of the callback function.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO type/handle/ISR table out of range.

18.6.7.18 void FLEXIO_UART_TransferStartRingBuffer ([FLEXIO_UART_Type](#) * *base*, [flexio_uart_handle_t](#) * *handle*, [uint8_t](#) * *ringBuffer*, [size_t](#) *ringBufferSize*)

This function sets up the RX ring buffer to a specific UART handle.

When the RX ring buffer is used, data received is stored into the ring buffer even when the user doesn't

call the `UART_ReceiveNonBlocking()` API. If there is already data received in the ring buffer, users can get the received data from the ring buffer directly.

Note

When using the RX ring buffer, one byte is reserved for internal use. In other words, if `ringBufferSize` is 32, only 31 bytes are used for saving data.

Parameters

<i>base</i>	Pointer to the <code>FLEXIO_UART_Type</code> structure.
<i>handle</i>	Pointer to the <code>flexio_uart_handle_t</code> structure to store the transfer state.
<i>ringBuffer</i>	Start address of ring buffer for background receiving. Pass NULL to disable the ring buffer.
<i>ringBufferSize</i>	Size of the ring buffer.

18.6.7.19 void FLEXIO_UART_TransferStopRingBuffer (`FLEXIO_UART_Type * base,` `flexio_uart_handle_t * handle`)

This function aborts the background transfer and uninstalls the ring buffer.

Parameters

<i>base</i>	Pointer to the <code>FLEXIO_UART_Type</code> structure.
<i>handle</i>	Pointer to the <code>flexio_uart_handle_t</code> structure to store the transfer state.

18.6.7.20 status_t FLEXIO_UART_TransferSendNonBlocking (`FLEXIO_UART_Type * base,` `flexio_uart_handle_t * handle,` `flexio_uart_transfer_t * xfer`)

This function sends data using an interrupt method. This is a non-blocking function, which returns directly without waiting for all data to be written to the TX register. When all data is written to the TX register in ISR, the FlexIO UART driver calls the callback function and passes the `kStatus_FLEXIO_UART_TxIdle` as status parameter.

Note

The `kStatus_FLEXIO_UART_TxIdle` is passed to the upper layer when all data is written to the TX register. However, it does not ensure that all data is sent out.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>handle</i>	Pointer to the <code>flexio_uart_handle_t</code> structure to store the transfer state.
<i>xfer</i>	FlexIO UART transfer structure. See flexio_uart_transfer_t .

Return values

<i>kStatus_Success</i>	Successfully starts the data transmission.
<i>kStatus_UART_TxBusy</i>	Previous transmission still not finished, data not written to the TX register.

18.6.7.21 void [FLEXIO_UART_TransferAbortSend](#) (`FLEXIO_UART_Type * base`, `flexio_uart_handle_t * handle`)

This function aborts the interrupt-driven data sending. Get the `remainBytes` to find out how many bytes are still not sent out.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>handle</i>	Pointer to the <code>flexio_uart_handle_t</code> structure to store the transfer state.

18.6.7.22 `status_t FLEXIO_UART_TransferGetSendCount (FLEXIO_UART_Type * base, flexio_uart_handle_t * handle, size_t * count)`

This function gets the number of bytes sent driven by interrupt.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>handle</i>	Pointer to the <code>flexio_uart_handle_t</code> structure to store the transfer state.
<i>count</i>	Number of bytes sent so far by the non-blocking transaction.

Return values

<i>kStatus_NoTransferIn-Progress</i>	transfer has finished or no transfer in progress.
<i>kStatus_Success</i>	Successfully return the count.

18.6.7.23 status_t FLEXIO_UART_TransferReceiveNonBlocking (FLEXIO_UART_Type * *base*, flexio_uart_handle_t * *handle*, flexio_uart_transfer_t * *xfer*, size_t * *receivedBytes*)

This function receives data using the interrupt method. This is a non-blocking function, which returns without waiting for all data to be received. If the RX ring buffer is used and not empty, the data in ring buffer is copied and the parameter *receivedBytes* shows how many bytes are copied from the ring buffer. After copying, if the data in ring buffer is not enough to read, the receive request is saved by the UART driver. When new data arrives, the receive request is serviced first. When all data is received, the UART driver notifies the upper layer through a callback function and passes the status parameter kStatus_UART_RxIdle. For example, if the upper layer needs 10 bytes but there are only 5 bytes in the ring buffer, the 5 bytes are copied to *xfer*->*data*. This function returns with the parameter *receivedBytes* set to 5. For the last 5 bytes, newly arrived data is saved from the *xfer*->*data*[5]. When 5 bytes are received, the UART driver notifies upper layer. If the RX ring buffer is not enabled, this function enables the RX and RX interrupt to receive data to *xfer*->*data*. When all data is received, the upper layer is notified.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>handle</i>	Pointer to the flexio_uart_handle_t structure to store the transfer state.
<i>xfer</i>	UART transfer structure. See flexio_uart_transfer_t .
<i>receivedBytes</i>	Bytes received from the ring buffer directly.

Return values

<i>kStatus_Success</i>	Successfully queue the transfer into the transmit queue.
<i>kStatus_FLEXIO_UART_RxBusy</i>	Previous receive request is not finished.

18.6.7.24 void FLEXIO_UART_TransferAbortReceive (FLEXIO_UART_Type * *base*, flexio_uart_handle_t * *handle*)

This function aborts the receive data which was using IRQ.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>handle</i>	Pointer to the flexio_uart_handle_t structure to store the transfer state.

**18.6.7.25 status_t FLEXIO_UART_TransferGetReceiveCount (FLEXIO_UART_Type *
base, flexio_uart_handle_t * handle, size_t * count)**

This function gets the number of bytes received driven by interrupt.

Parameters

<i>base</i>	Pointer to the FLEXIO_UART_Type structure.
<i>handle</i>	Pointer to the flexio_uart_handle_t structure to store the transfer state.
<i>count</i>	Number of bytes received so far by the non-blocking transaction.

Return values

<i>kStatus_NoTransferIn-Progress</i>	transfer has finished or no transfer in progress.
<i>kStatus_Success</i>	Successfully return the count.

18.6.7.26 void FLEXIO_UART_TransferHandleIRQ (*void *uartType, void *uartHandle*)

This function processes the FlexIO UART transmit and receives the IRQ request.

Parameters

<i>uartType</i>	Pointer to the FLEXIO_UART_Type structure.
<i>uartHandle</i>	Pointer to the flexio_uart_handle_t structure to store the transfer state.

Chapter 19

GPIO: General-Purpose Input/Output Driver

19.1 Overview

Modules

- FGPIO Driver
- GPIO Driver

Data Structures

- struct `gpio_pin_config_t`
The GPIO pin configuration structure. [More...](#)

Enumerations

- enum `gpio_pin_direction_t` {
 `kGPIO_DigitalInput` = 0U,
 `kGPIO_DigitalOutput` = 1U }
GPIO direction definition.

Driver version

- #define `FSL_GPIO_DRIVER_VERSION` (`MAKE_VERSION(2, 6, 0)`)
GPIO driver version.

19.2 Data Structure Documentation

19.2.1 struct `gpio_pin_config_t`

Each pin can only be configured as either an output pin or an input pin at a time. If configured as an input pin, leave the `outputConfig` unused. Note that in some use cases, the corresponding port property should be configured in advance with the `PORT_SetPinConfig()`.

Data Fields

- `gpio_pin_direction_t pinDirection`
GPIO direction, input or output.
- `uint8_t outputLogic`
Set a default output logic, which has no use in input.

19.3 Macro Definition Documentation

19.3.1 #define FSL_GPIO_DRIVER_VERSION (MAKE_VERSION(2, 6, 0))

19.4 Enumeration Type Documentation

19.4.1 enum gpio_pin_direction_t

Enumerator

kGPIO_DigitalInput Set current pin as digital input.

kGPIO_DigitalOutput Set current pin as digital output.

19.5 GPIO Driver

19.5.1 Overview

The MCUXpresso SDK provides a peripheral driver for the General-Purpose Input/Output (GPIO) module of MCUXpresso SDK devices.

19.5.2 Typical use case

19.5.2.1 Output Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/gpio

19.5.2.2 Input Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/gpio

GPIO Configuration

- void [GPIO_PinInit](#) (GPIO_Type *base, uint32_t pin, const [gpio_pin_config_t](#) *config)
Initializes a GPIO pin used by the board.

GPIO Output Operations

- static void [GPIO_PinWrite](#) (GPIO_Type *base, uint32_t pin, uint8_t output)
Sets the output level of the multiple GPIO pins to the logic 1 or 0.
- static void [GPIO_PortSet](#) (GPIO_Type *base, uint32_t mask)
Sets the output level of the multiple GPIO pins to the logic 1.
- static void [GPIO_PortClear](#) (GPIO_Type *base, uint32_t mask)
Sets the output level of the multiple GPIO pins to the logic 0.
- static void [GPIO_PortToggle](#) (GPIO_Type *base, uint32_t mask)
Reverses the current output logic of the multiple GPIO pins.

GPIO Input Operations

- static uint32_t [GPIO_PinRead](#) (GPIO_Type *base, uint32_t pin)
Reads the current input value of the GPIO port.

GPIO Interrupt

- uint32_t [GPIO_PortGetInterruptFlags](#) (GPIO_Type *base)
Reads the GPIO port interrupt status flag.

- void [GPIO_PortClearInterruptFlags](#) (GPIO_Type *base, uint32_t mask)
Clears multiple GPIO pin interrupt status flags.

19.5.3 Function Documentation

19.5.3.1 void [GPIO_PinInit](#) (GPIO_Type * *base*, uint32_t *pin*, const gpio_pin_config_t * *config*)

To initialize the GPIO, define a pin configuration, as either input or output, in the user file. Then, call the [GPIO_PinInit\(\)](#) function.

This is an example to define an input pin or an output pin configuration.

```
* Define a digital input pin configuration,
* gpio_pin_config_t config =
* {
*   kGPIO_DigitalInput,
*   0,
* }
* Define a digital output pin configuration,
* gpio_pin_config_t config =
* {
*   kGPIO_DigitalOutput,
*   0,
* }
```

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.)
<i>pin</i>	GPIO port pin number
<i>config</i>	GPIO pin configuration pointer

19.5.3.2 static void [GPIO_PinWrite](#) (GPIO_Type * *base*, uint32_t *pin*, uint8_t *output*) [inline], [static]

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.)
<i>pin</i>	GPIO pin number

<i>output</i>	GPIO pin output logic level. <ul style="list-style-type: none">• 0: corresponding pin output low-logic level.• 1: corresponding pin output high-logic level.
---------------	---

19.5.3.3 static void GPIO_PortSet (**GPIO_Type** * *base*, **uint32_t** *mask*) [inline], [static]

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.)
<i>mask</i>	GPIO pin number macro

19.5.3.4 static void GPIO_PortClear (**GPIO_Type** * *base*, **uint32_t** *mask*) [inline], [static]

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.)
<i>mask</i>	GPIO pin number macro

19.5.3.5 static void GPIO_PortToggle (**GPIO_Type** * *base*, **uint32_t** *mask*) [inline], [static]

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.)
<i>mask</i>	GPIO pin number macro

19.5.3.6 static **uint32_t** GPIO_PinRead (**GPIO_Type** * *base*, **uint32_t** *pin*) [inline], [static]

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.)
<i>pin</i>	GPIO pin number

Return values

<i>GPIO</i>	port input value <ul style="list-style-type: none"> • 0: corresponding pin input low-logic level. • 1: corresponding pin input high-logic level.
-------------	--

19.5.3.7 `uint32_t GPIO_PortGetInterruptFlags (GPIO_Type * base)`

If a pin is configured to generate the DMA request, the corresponding flag is cleared automatically at the completion of the requested DMA transfer. Otherwise, the flag remains set until a logic one is written to that flag. If configured for a level sensitive interrupt that remains asserted, the flag is set again immediately.

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.)
-------------	--

Return values

<i>The</i>	current GPIO port interrupt status flag, for example, 0x00010001 means the pin 0 and 17 have the interrupt.
------------	---

19.5.3.8 `void GPIO_PortClearInterruptFlags (GPIO_Type * base, uint32_t mask)`

Parameters

<i>base</i>	GPIO peripheral base pointer (GPIOA, GPIOB, GPIOC, and so on.)
<i>mask</i>	GPIO pin number macro

19.6 FGPIO Driver

This section describes the programming interface of the FGPIO driver. The FGPIO driver configures the FGPIO module and provides a functional interface to build the GPIO application.

Note

FGPIO (Fast GPIO) is only available in a few MCUs. FGPIO and GPIO share the same peripheral but use different registers. FGPIO is closer to the core than the regular GPIO and it's faster to read and write.

19.6.1 Typical use case

19.6.1.1 Output Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/gpio

19.6.1.2 Input Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/gpio

Chapter 20

LLWU: Low-Leakage Wakeup Unit Driver

20.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Low-Leakage Wakeup Unit (LLWU) module of MCUXpresso SDK devices. The LLWU module allows the user to select external pin sources and internal modules as a wake-up source from low-leakage power modes.

20.2 External wakeup pins configurations

Configures the external wakeup pins' working modes, gets, and clears the wake pin flags. External wakeup pins are accessed by the `pinIndex`, which is started from 1. Numbers of the external pins depend on the SoC configuration.

20.3 Internal wakeup modules configurations

Enables/disables the internal wakeup modules and gets the module flags. Internal modules are accessed by `moduleIndex`, which is started from 1. Numbers of external pins depend the on SoC configuration.

20.4 Digital pin filter for external wakeup pin configurations

Configures the digital pin filter of the external wakeup pins' working modes, gets, and clears the pin filter flags. Digital pin filters are accessed by the `filterIndex`, which is started from 1. Numbers of external pins depend on the SoC configuration.

Enumerations

- enum `llwu_external_pin_mode_t` {
 `kLLWU_ExternalPinDisable` = 0U,
 `kLLWU_ExternalPinRisingEdge` = 1U,
 `kLLWU_ExternalPinFallingEdge` = 2U,
 `kLLWU_ExternalPinAnyEdge` = 3U }
 External input pin control modes.
- enum `llwu_pin_filter_mode_t` {
 `kLLWU_PinFilterDisable` = 0U,
 `kLLWU_PinFilterRisingEdge` = 1U,
 `kLLWU_PinFilterFallingEdge` = 2U,
 `kLLWU_PinFilterAnyEdge` = 3U }
 Digital filter control modes.

Driver version

- #define `FSL_LLWU_DRIVER_VERSION` (`MAKE_VERSION(2, 0, 5)`)
LLWU driver version.

20.5 Macro Definition Documentation

20.5.1 `#define FSL_LLWU_DRIVER_VERSION (MAKE_VERSION(2, 0, 5))`

20.6 Enumeration Type Documentation

20.6.1 `enum llwu_external_pin_mode_t`

Enumerator

kLLWU_ExternalPinDisable Pin disabled as a wakeup input.

kLLWU_ExternalPinRisingEdge Pin enabled with the rising edge detection.

kLLWU_ExternalPinFallingEdge Pin enabled with the falling edge detection.

kLLWU_ExternalPinAnyEdge Pin enabled with any change detection.

20.6.2 `enum llwu_pin_filter_mode_t`

Enumerator

kLLWU_PinFilterDisable Filter disabled.

kLLWU_PinFilterRisingEdge Filter positive edge detection.

kLLWU_PinFilterFallingEdge Filter negative edge detection.

kLLWU_PinFilterAnyEdge Filter any edge detection.

Chapter 21

LPADC: 12-bit SAR Analog-to-Digital Converter Driver

21.1 Overview

The MCUXpresso SDK provides a peripheral driver for the 12-bit SAR Analog-to-Digital Converter (LP-ADC) module of MCUXpresso SDK devices.

21.2 Typical use case

21.2.1 Polling Configuration

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/lpadc

21.2.2 Interrupt Configuration

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/lpadc

Files

- file [fsl_lpadc.h](#)

Data Structures

- struct [lpadc_config_t](#)
LPADC global configuration. [More...](#)
- struct [lpadc_conv_command_config_t](#)
Define structure to keep the configuration for conversion command. [More...](#)
- struct [lpadc_conv_trigger_config_t](#)
Define structure to keep the configuration for conversion trigger. [More...](#)
- struct [lpadc_conv_result_t](#)
Define the structure to keep the conversion result. [More...](#)

Macros

- #define [LPADC_GET_ACTIVE_COMMAND_STATUS](#)(statusVal) ((statusVal & ADC_STAT_CMDACT_MASK) >> ADC_STAT_CMDACT_SHIFT)
Define the MACRO function to get command status from status value.
- #define [LPADC_GET_ACTIVE_TRIGGER_STATUS](#)(statusVal) ((statusVal & ADC_STAT_TRGACT_MASK) >> ADC_STAT_TRGACT_SHIFT)
Define the MACRO function to get trigger status from status value.

Enumerations

- enum `_lpadc_status_flags` {

 `kLPADC_ResultFIFOOverflowFlag` = ADC_STAT_FOF_MASK,

 `kLPADC_ResultFIFOReadyFlag` = ADC_STAT_RDY_MASK }

 Define hardware flags of the module.
- enum `_lpadc_interrupt_enable` {

 `kLPADC_ResultFIFOOverflowInterruptEnable` = ADC_IE_FOFIE_MASK,

 `kLPADC_FIFOWatermarkInterruptEnable` = ADC_IE_FWMIE_MASK }

 Define interrupt switchers of the module.
- enum `lpadc_sample_scale_mode_t` {

 `kLPADC_SamplePartScale` = 0U,

 `kLPADC_SampleFullScale` = 1U }

 Define enumeration of sample scale mode.
- enum `lpadc_sample_channel_mode_t` {

 `kLPADC_SampleChannelSingleEndSideA` = 0U,

 `kLPADC_SampleChannelSingleEndSideB` = 1U,

 `kLPADC_SampleChannelDiffBothSideAB` = 2U,

 `kLPADC_SampleChannelDiffBothSideBA` = 3U }

 Define enumeration of channel sample mode.
- enum `lpadc.hardware_average_mode_t` {

 `kLPADC_HardwareAverageCount1` = 0U,

 `kLPADC_HardwareAverageCount2` = 1U,

 `kLPADC_HardwareAverageCount4` = 2U,

 `kLPADC_HardwareAverageCount8` = 3U,

 `kLPADC_HardwareAverageCount16` = 4U,

 `kLPADC_HardwareAverageCount32` = 5U,

 `kLPADC_HardwareAverageCount64` = 6U,

 `kLPADC_HardwareAverageCount128` = 7U }

 Define enumeration of hardware average selection.
- enum `lpadc.sample_time_mode_t` {

 `kLPADC_SampleTimeADCK3` = 0U,

 `kLPADC_SampleTimeADCK5` = 1U,

 `kLPADC_SampleTimeADCK7` = 2U,

 `kLPADC_SampleTimeADCK11` = 3U,

 `kLPADC_SampleTimeADCK19` = 4U,

 `kLPADC_SampleTimeADCK35` = 5U,

 `kLPADC_SampleTimeADCK67` = 6U,

 `kLPADC_SampleTimeADCK131` = 7U }

 Define enumeration of sample time selection.
- enum `lpadc.hardware_compare_mode_t` {

 `kLPADC_HardwareCompareDisabled` = 0U,

 `kLPADC_HardwareCompareStoreOnTrue` = 2U,

 `kLPADC_HardwareCompareRepeatUntilTrue` = 3U }

 Define enumeration of hardware compare mode.
- enum `lpadc.reference_voltage_source_t` {

```

kLPADC_ReferenceVoltageAlt1 = 0U,
kLPADC_ReferenceVoltageAlt2 = 1U,
kLPADC_ReferenceVoltageAlt3 = 2U }

Define enumeration of reference voltage source.
• enum lpadc_power_level_mode_t {
    kLPADC_PowerLevelAlt1 = 0U,
    kLPADC_PowerLevelAlt2 = 1U,
    kLPADC_PowerLevelAlt3 = 2U,
    kLPADC_PowerLevelAlt4 = 3U }

Define enumeration of power configuration.
• enum lpadc_trigger_priority_policy_t {
    kLPADC_TriggerPriorityPreemptImmediately = 0U,
    kLPADC_TriggerPriorityPreemptSoftly = 1U,
    kLPADC_TriggerPriorityPreemptSubsequently = 2U }

Define enumeration of trigger priority policy.

```

Driver version

- #define FSL_LPADC_DRIVER_VERSION (MAKE_VERSION(2, 5, 0))
LPADC driver version 2.5.0.

Initialization & de-initialization.

- void LPADC_Init (ADC_Type *base, const lpadc_config_t *config)
Initializes the LPADC module.
- void LPADC_GetDefaultConfig (lpadc_config_t *config)
Gets an available pre-defined settings for initial configuration.
- void LPADC_Deinit (ADC_Type *base)
De-initializes the LPADC module.
- static void LPADC_Enable (ADC_Type *base, bool enable)
Switch on/off the LPADC module.
- static void LPADC_DoResetFIFO (ADC_Type *base)
Do reset the conversion FIFO.
- static void LPADC_DoResetConfig (ADC_Type *base)
Do reset the module's configuration.

Status

- static uint32_t LPADC_GetStatusFlags (ADC_Type *base)
Get status flags.
- static void LPADC_ClearStatusFlags (ADC_Type *base, uint32_t mask)
Clear status flags.

Interrupts

- static void LPADC_EnableInterrupts (ADC_Type *base, uint32_t mask)
Enable interrupts.
- static void LPADC_DisableInterrupts (ADC_Type *base, uint32_t mask)
Disable interrupts.

DMA Control

- static void [LPADC_EnableFIFOWatermarkDMA](#) (ADC_Type *base, bool enable)
Switch on/off the DMA trigger for FIFO watermark event.

Trigger and conversion with FIFO.

- static uint32_t [LPADC_GetConvResultCount](#) (ADC_Type *base)
Get the count of result kept in conversion FIFO.
- bool [LPADC_GetConvResult](#) (ADC_Type *base, [lpadc_conv_result_t](#) *result)
Get the result in conversion FIFO.
- void [LPADC_SetConvTriggerConfig](#) (ADC_Type *base, uint32_t triggerId, const [lpadc_conv_trigger_config_t](#) *config)
Configure the conversion trigger source.
- void [LPADC_GetDefaultConvTriggerConfig](#) ([lpadc_conv_trigger_config_t](#) *config)
Gets an available pre-defined settings for trigger's configuration.
- static void [LPADC_DoSoftwareTrigger](#) (ADC_Type *base, uint32_t triggerIdMask)
Do software trigger to conversion command.
- void [LPADC_SetConvCommandConfig](#) (ADC_Type *base, uint32_t commandId, const [lpadc_conv_command_config_t](#) *config)
Configure conversion command.
- void [LPADC_GetDefaultConvCommandConfig](#) ([lpadc_conv_command_config_t](#) *config)
Gets an available pre-defined settings for conversion command's configuration.

21.3 Data Structure Documentation

21.3.1 struct [lpadc_config_t](#)

This structure would used to keep the settings for initialization.

Data Fields

- bool [enableInDozeMode](#)
Control system transition to Stop and Wait power modes while ADC is converting.
- bool [enableAnalogPreliminary](#)
ADC analog circuits are pre-enabled and ready to execute conversions without startup delays(at the cost of higher DC current consumption).
- uint32_t [powerUpDelay](#)
When the analog circuits are not pre-enabled, the ADC analog circuits are only powered while the ADC is active and there is a counted delay defined by this field after an initial trigger transitions the ADC from its Idle state to allow time for the analog circuits to stabilize.
- [lpadc_reference_voltage_source_t](#) [referenceVoltageSource](#)
Selects the voltage reference high used for conversions.
- [lpadc_power_level_mode_t](#) [powerLevelMode](#)
Power Configuration Selection.
- [lpadc_trigger_priority_policy_t](#) [triggerPriorityPolicy](#)
Control how higher priority triggers are handled, see to [lpadc_trigger_priority_policy_mode_t](#).
- bool [enableConvPause](#)
Enables the ADC pausing function.

- `uint32_t convPauseDelay`
Controls the duration of pausing during command execution sequencing.
- `uint32_t FIFOWatermark`
FIFOWatermark is a programmable threshold setting.

Field Documentation

(1) `bool Ipadc_config_t::enableInDozeMode`

When enabled in Doze mode, immediate entries to Wait or Stop are allowed. When disabled, the ADC will wait for the current averaging iteration/FIFO storage to complete before acknowledging stop or wait mode entry.

(2) `bool Ipadc_config_t::enableAnalogPreliminary`

(3) `uint32_t Ipadc_config_t::powerUpDelay`

The startup delay count of (`powerUpDelay * 4`) ADCK cycles must result in a longer delay than the analog startup time.

(4) `Ipadc_reference_voltage_source_t Ipadc_config_t::referenceVoltageSource`

(5) `Ipadc_power_level_mode_t Ipadc_config_t::powerLevelMode`

(6) `Ipadc_trigger_priority_policy_t Ipadc_config_t::triggerPriorityPolicy`

(7) `bool Ipadc_config_t::enableConvPause`

When enabled, a programmable delay is inserted during command execution sequencing between LOOP iterations, between commands in a sequence, and between conversions when command is executing in "Compare Until True" configuration.

(8) `uint32_t Ipadc_config_t::convPauseDelay`

The pause delay is a count of (`convPauseDelay*4`) ADCK cycles. Only available when ADC pausing function is enabled. The available value range is in 9-bit.

(9) `uint32_t Ipadc_config_t::FIFOWatermark`

When the number of datawords stored in the ADC Result FIFO is greater than the value in this field, the ready flag would be asserted to indicate stored data has reached the programmable threshold.

21.3.2 `struct Ipadc_conv_command_config_t`

Data Fields

- `Ipadc_sample_scale_mode_t sampleScaleMode`
Sample scale mode.

- **lpadc_sample_channel_mode_t sampleChannelMode**
Channel sample mode.
- **uint32_t channelNumber**
Channel number; select the channel or channel pair.
- **uint32_t chainedNextCommandNumber**
Selects the next command to be executed after this command completes.
- **bool enableAutoChannelIncrement**
Loop with increment: when disabled, the "loopCount" field selects the number of times the selected channel is converted consecutively; when enabled, the "loopCount" field defines how many consecutive channels are converted as part of the command execution.
- **uint32_t loopCount**
Selects how many times this command executes before finish and transition to the next command or Idle state.
- **lpadc_hardware_average_mode_t hardwareAverageMode**
Hardware average selection.
- **lpadc_sample_time_mode_t sampleTimeMode**
Sample time selection.
- **lpadc_hardware_compare_mode_t hardwareCompareMode**
Hardware compare selection.
- **uint32_t hardwareCompareValueHigh**
Compare Value High.
- **uint32_t hardwareCompareValueLow**
Compare Value Low.
- **bool enableWaitTrigger**
Wait for trigger assertion before execution: when disabled, this command will be automatically executed; when enabled, the active trigger must be asserted again before executing this command.

Field Documentation

- (1) **lpadc_sample_scale_mode_t lpadc_conv_command_config_t::sampleScaleMode**
- (2) **lpadc_sample_channel_mode_t lpadc_conv_command_config_t::sampleChannelMode**
- (3) **uint32_t lpadc_conv_command_config_t::channelNumber**
- (4) **uint32_t lpadc_conv_command_config_t::chainedNextCommandNumber**

1-15 is available, 0 is to terminate the chain after this command.

- (5) **bool lpadc_conv_command_config_t::enableAutoChannelIncrement**
- (6) **uint32_t lpadc_conv_command_config_t::loopCount**

Command executes LOOP+1 times. 0-15 is available.

- (7) **lpadc_hardware_average_mode_t lpadc_conv_command_config_t::hardwareAverageMode**
- (8) **lpadc_sample_time_mode_t lpadc_conv_command_config_t::sampleTimeMode**
- (9) **lpadc_hardware_compare_mode_t lpadc_conv_command_config_t::hardwareCompareMode**

(10) `uint32_t Ipadc_conv_command_config_t::hardwareCompareValueHigh`

The available value range is in 16-bit.

(11) `uint32_t Ipadc_conv_command_config_t::hardwareCompareValueLow`

The available value range is in 16-bit.

(12) `bool Ipadc_conv_command_config_t::enableWaitTrigger`

21.3.3 struct Ipadc_conv_trigger_config_t

Data Fields

- `uint32_t targetCommandId`
Select the command from command buffer to execute upon detect of the associated trigger event.
- `uint32_t delayPower`
Select the trigger delay duration to wait at the start of servicing a trigger event.
- `uint32_t priority`
Sets the priority of the associated trigger source.
- `bool enableHardwareTrigger`
Enable hardware trigger source to initiate conversion on the rising edge of the input trigger source or not.

Field Documentation

(1) `uint32_t Ipadc_conv_trigger_config_t::targetCommandId`

(2) `uint32_t Ipadc_conv_trigger_config_t::delayPower`

When this field is clear, then no delay is incurred. When this field is set to a non-zero value, the duration for the delay is $2^{\text{delayPower}}$ ADCK cycles. The available value range is 4-bit.

(3) `uint32_t Ipadc_conv_trigger_config_t::priority`

If two or more triggers have the same priority level setting, the lower order trigger event has the higher priority. The lower value for this field is for the higher priority, the available value range is 1-bit.

(4) `bool Ipadc_conv_trigger_config_t::enableHardwareTrigger`

The software trigger is always available.

21.3.4 struct Ipadc_conv_result_t

Data Fields

- `uint32_t commandIdSource`
Indicate the command buffer being executed that generated this result.
- `uint32_t loopCountIndex`

- `uint32_t triggerIdSource`
 - Indicate the loop count value during command execution that generated this result.*
- `uint16_t convValue`
 - Indicate the trigger source that initiated a conversion and generated this result.*
 - Data result.*

Field Documentation

- (1) `uint32_t lpadc_conv_result_t::commandIdSource`
- (2) `uint32_t lpadc_conv_result_t::loopCountIndex`
- (3) `uint32_t lpadc_conv_result_t::triggerIdSource`
- (4) `uint16_t lpadc_conv_result_t::convValue`

21.4 Macro Definition Documentation

21.4.1 `#define FSL_LPADC_DRIVER_VERSION (MAKE_VERSION(2, 5, 0))`

21.4.2 `#define LPADC_GET_ACTIVE_COMMAND_STATUS(statusVal) ((statusVal & ADC_STAT_CMDACT_MASK) >> ADC_STAT_CMDACT_SHIFT)`

The statusVal is the return value from [LPADC_GetStatusFlags\(\)](#).

21.4.3 `#define LPADC_GET_ACTIVE_TRIGGER_STATUE(statusVal) ((statusVal & ADC_STAT_TRGACT_MASK) >> ADC_STAT_TRGACT_SHIFT)`

The statusVal is the return value from [LPADC_GetStatusFlags\(\)](#).

21.5 Enumeration Type Documentation

21.5.1 enum _lpadc_status_flags

Enumerator

kLPADC_ResultFIFOOverflowFlag Indicates that more data has been written to the Result FIFO than it can hold.

kLPADC_ResultFIFOReadyFlag Indicates when the number of valid datawords in the result FIFO is greater than the setting watermark level.

21.5.2 enum _lpadc_interrupt_enable

Enumerator

kLPADC_ResultFIFOOverflowInterruptEnable Configures ADC to generate overflow interrupt requests when FOF flag is asserted.

kLPADC_FIFOWatermarkInterruptEnable Configures ADC to generate watermark interrupt requests when RDY flag is asserted.

21.5.3 enum lpadc_sample_scale_mode_t

The sample scale mode is used to reduce the selected ADC analog channel input voltage level by a factor. The maximum possible voltage on the ADC channel input should be considered when selecting a scale mode to ensure that the reducing factor always results voltage level at or below the VREFH reference. This reducing capability allows conversion of analog inputs higher than VREFH. A-side and B-side channel inputs are both scaled using the scale mode.

Enumerator

kLPADC_SamplePartScale Use divided input voltage signal. (Factor of 30/64).

kLPADC_SampleFullScale Full scale (Factor of 1).

21.5.4 enum lpadc_sample_channel_mode_t

The channel sample mode configures the channel with single-end/differential/dual-single-end, side A/B.

Enumerator

kLPADC_SampleChannelSingleEndSideA Single end mode, using side A.

kLPADC_SampleChannelSingleEndSideB Single end mode, using side B.

kLPADC_SampleChannelDiffBothSideAB Differential mode, using A as plus side and B as minus side.

kLPADC_SampleChannelDiffBothSideBA Differential mode, using B as plus side and A as minus side.

21.5.5 enum lpadc_hardware_average_mode_t

It Selects how many ADC conversions are averaged to create the ADC result. An internal storage buffer is used to capture temporary results while the averaging iterations are executed.

Enumerator

kLPADC_HardwareAverageCount1 Single conversion.

kLPADC_HardwareAverageCount2 2 conversions averaged.
kLPADC_HardwareAverageCount4 4 conversions averaged.
kLPADC_HardwareAverageCount8 8 conversions averaged.
kLPADC_HardwareAverageCount16 16 conversions averaged.
kLPADC_HardwareAverageCount32 32 conversions averaged.
kLPADC_HardwareAverageCount64 64 conversions averaged.
kLPADC_HardwareAverageCount128 128 conversions averaged.

21.5.6 enum lpadc_sample_time_mode_t

The shortest sample time maximizes conversion speed for lower impedance inputs. Extending sample time allows higher impedance inputs to be accurately sampled. Longer sample times can also be used to lower overall power consumption when command looping and sequencing is configured and high conversion rates are not required.

Enumerator

kLPADC_SampleTimeADCK3 3 ADCK cycles total sample time.
kLPADC_SampleTimeADCK5 5 ADCK cycles total sample time.
kLPADC_SampleTimeADCK7 7 ADCK cycles total sample time.
kLPADC_SampleTimeADCK11 11 ADCK cycles total sample time.
kLPADC_SampleTimeADCK19 19 ADCK cycles total sample time.
kLPADC_SampleTimeADCK35 35 ADCK cycles total sample time.
kLPADC_SampleTimeADCK67 69 ADCK cycles total sample time.
kLPADC_SampleTimeADCK131 131 ADCK cycles total sample time.

21.5.7 enum lpadc_hardware_compare_mode_t

After an ADC channel input is sampled and converted and any averaging iterations are performed, this mode setting guides operation of the automatic compare function to optionally only store when the compare operation is true. When compare is enabled, the conversion result is compared to the compare values.

Enumerator

kLPADC_HardwareCompareDisabled Compare disabled.
kLPADC_HardwareCompareStoreOnTrue Compare enabled. Store on true.
kLPADC_HardwareCompareRepeatUntilTrue Compare enabled. Repeat channel acquisition until true.

21.5.8 enum lpadc_reference_voltage_source_t

For detail information, need to check the SoC's specification.

Enumerator

- kLPADC_ReferenceVoltageAlt1* Option 1 setting.
- kLPADC_ReferenceVoltageAlt2* Option 2 setting.
- kLPADC_ReferenceVoltageAlt3* Option 3 setting.

21.5.9 enum lpadc_power_level_mode_t

Configures the ADC for power and performance. In the highest power setting the highest conversion rates will be possible. Refer to the device data sheet for power and performance capabilities for each setting.

Enumerator

- kLPADC_PowerLevelAlt1* Lowest power setting.
- kLPADC_PowerLevelAlt2* Next lowest power setting.
- kLPADC_PowerLevelAlt3* ...
- kLPADC_PowerLevelAlt4* Highest power setting.

21.5.10 enum lpadc_trigger_priority_policy_t

This selection controls how higher priority triggers are handled.

Enumerator

- kLPADC_TriggerPriorityPreemptImmediately* If a higher priority trigger is detected during command processing, the current conversion is aborted and the new command specified by the trigger is started.
- kLPADC_TriggerPriorityPreemptSoftly* If a higher priority trigger is received during command processing, the current conversion is completed (including averaging iterations and compare function if enabled) and stored to the result FIFO before the higher priority trigger/command is initiated.
- kLPADC_TriggerPriorityPreemptSubsequently* If a higher priority trigger is received during command processing, the current command will be completed (averaging, looping, compare) before servicing the higher priority trigger.

21.6 Function Documentation

21.6.1 void LPADC_Init (ADC_Type * *base*, const lpadc_config_t * *config*)

Parameters

<i>base</i>	LPADC peripheral base address.
<i>config</i>	Pointer to configuration structure. See "lpadc_config_t".

21.6.2 void LPADC_GetDefaultConfig (lpadc_config_t * *config*)

This function initializes the converter configuration structure with an available settings. The default values are:

```
* config->enableInDozeMode      = true;
* config->enableAnalogPreliminary = false;
* config->powerUpDelay        = 0x80;
* config->referenceVoltageSource = kLPADC_ReferenceVoltageAlt1;
* config->powerLevelMode       = kLPADC_PowerLevelAlt1;
* config->triggerPriorityPolicy = kLPADC_TriggerPriorityPreemptImmediately
;
* config->enableConvPause      = false;
* config->convPauseDelay       = 0U;
* config->FIFOWatermark        = 0U;
*
```

Parameters

<i>config</i>	Pointer to configuration structure.
---------------	-------------------------------------

21.6.3 void LPADC_Deinit (ADC_Type * *base*)

Parameters

<i>base</i>	LPADC peripheral base address.
-------------	--------------------------------

21.6.4 static void LPADC_Enable (ADC_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	LPADC peripheral base address.
<i>enable</i>	switcher to the module.

**21.6.5 static void LPADC_DoResetFIFO (ADC_Type * *base*) [inline],
[static]**

Parameters

<i>base</i>	LPADC peripheral base address.
-------------	--------------------------------

**21.6.6 static void LPADC_DoResetConfig (ADC_Type * *base*) [inline],
[static]**

Reset all ADC internal logic and registers, except the Control Register (ADCx_CTRL).

Parameters

<i>base</i>	LPADC peripheral base address.
-------------	--------------------------------

**21.6.7 static uint32_t LPADC_GetStatusFlags (ADC_Type * *base*) [inline],
[static]**

Parameters

<i>base</i>	LPADC peripheral base address.
-------------	--------------------------------

Returns

status flags' mask. See to [_lpadc_status_flags](#).

**21.6.8 static void LPADC_ClearStatusFlags (ADC_Type * *base*, uint32_t *mask*)
[inline], [static]**

Only the flags can be cleared by writing ADCx_STATUS register would be cleared by this API.

Parameters

<i>base</i>	LPADC peripheral base address.
<i>mask</i>	Mask value for flags to be cleared. See to _lpadc_status_flags .

**21.6.9 static void LPADC_EnableInterrupts (ADC_Type * *base*, uint32_t *mask*)
[inline], [static]**

Parameters

<i>base</i>	LPADC peripheral base address.
<i>mask</i>	Mask value for interrupt events. See to _lpadc_interrupt_enable .

**21.6.10 static void LPADC_DisableInterrupts (ADC_Type * *base*, uint32_t *mask*)
[inline], [static]**

Parameters

<i>base</i>	LPADC peripheral base address.
<i>mask</i>	Mask value for interrupt events. See to _lpadc_interrupt_enable .

**21.6.11 static void LPADC_EnableFIFOWatermarkDMA (ADC_Type * *base*, bool
enable) [inline], [static]**

Parameters

<i>base</i>	LPADC peripheral base address.
<i>enable</i>	Switcher to the event.

**21.6.12 static uint32_t LPADC_GetConvResultCount (ADC_Type * *base*)
[inline], [static]**

Parameters

<i>base</i>	LPADC peripheral base address.
-------------	--------------------------------

Returns

The count of result kept in conversion FIFO.

21.6.13 **bool LPADC_GetConvResult (ADC_Type * *base*, lpadc_conv_result_t * *result*)**

Parameters

<i>base</i>	LPADC peripheral base address.
<i>result</i>	Pointer to structure variable that keeps the conversion result in conversion FIFO.

Returns

Status whether FIFO entry is valid.

21.6.14 **void LPADC_SetConvTriggerConfig (ADC_Type * *base*, uint32_t *triggerId*, const lpadc_conv_trigger_config_t * *config*)**

Each programmable trigger can launch the conversion command in command buffer.

Parameters

<i>base</i>	LPADC peripheral base address.
<i>triggerId</i>	ID for each trigger. Typically, the available value range is from 0.
<i>config</i>	Pointer to configuration structure. See to lpadc_conv_trigger_config_t .

21.6.15 **void LPADC_GetDefaultConvTriggerConfig (lpadc_conv_trigger_config_t * *config*)**

This function initializes the trigger's configuration structure with an available settings. The default values are:

```
* config->commandIdSource      = 0U;
* config->loopCountIndex      = 0U;
* config->triggerIdSource     = 0U;
* config->enableHardwareTrigger = false;
*
```

Parameters

<i>config</i>	Pointer to configuration structure.
---------------	-------------------------------------

21.6.16 static void LPADC_DoSoftwareTrigger (ADC_Type * *base*, uint32_t *triggerIdMask*) [inline], [static]

Parameters

<i>base</i>	LPADC peripheral base address.
<i>triggerIdMask</i>	Mask value for software trigger indexes, which count from zero.

21.6.17 void LPADC_SetConvCommandConfig (ADC_Type * *base*, uint32_t *commandId*, const lpadc_conv_command_config_t * *config*)

Parameters

<i>base</i>	LPADC peripheral base address.
<i>commandId</i>	ID for command in command buffer. Typically, the available value range is 1 - 15.
<i>config</i>	Pointer to configuration structure. See to lpadc_conv_command_config_t .

21.6.18 void LPADC_GetDefaultConvCommandConfig (lpadc_conv_command_config_t * *config*)

This function initializes the conversion command's configuration structure with an available settings. The default values are:

```
* config->sampleScaleMode          = kLPADC_SampleFullScale;
* config->channelSampleMode       = kLPADC_SampleChannelSingleEndSideA
;
* config->channelNumber          = OU;
* config->chainedNextCmdNumber    = OU;
* config->enableAutoChannelIncrement = false;
* config->loopCount              = OU;
* config->hardwareAverageMode    = kLPADC_HardwareAverageCount1;
* config->sampleTimeMode          = kLPADC_SampleTimeADCK3;
* config->hardwareCompareMode    = kLPADC_HardwareCompareDisabled;
* config->hardwareCompareValueHigh = OU;
* config->hardwareCompareValueLow = OU;
* config->conversionResolutionMode = kLPADC_ConversionResolutionStandard;
* config->enableWaitTrigger      = false;
```

Parameters

<i>config</i>	Pointer to configuration structure.
---------------	-------------------------------------

Chapter 22

LPI2C: Low Power Inter-Integrated Circuit Driver

22.1 Overview

Modules

- LPI2C CMSIS Driver
- LPI2C FreeRTOS Driver
- LPI2C Master DMA Driver
- LPI2C Master Driver
- LPI2C Slave Driver

Macros

- `#define I2C_RETRY_TIMES 0U /* Define to zero means keep waiting until the flag is assert/deassert. */`
Retry times for waiting flag.

Enumerations

- `enum {
 kStatus_LPI2C_Busy = MAKE_STATUS(kStatusGroup_LPI2C, 0),
 kStatus_LPI2C_Idle = MAKE_STATUS(kStatusGroup_LPI2C, 1),
 kStatus_LPI2C_Nak = MAKE_STATUS(kStatusGroup_LPI2C, 2),
 kStatus_LPI2C_FifoError = MAKE_STATUS(kStatusGroup_LPI2C, 3),
 kStatus_LPI2C_BitError = MAKE_STATUS(kStatusGroup_LPI2C, 4),
 kStatus_LPI2C_ArbitrationLost = MAKE_STATUS(kStatusGroup_LPI2C, 5),
 kStatus_LPI2C_PinLowTimeout,
 kStatus_LPI2C_NoTransferInProgress,
 kStatus_LPI2C_DmaRequestFail = MAKE_STATUS(kStatusGroup_LPI2C, 8),
 kStatus_LPI2C_Timeout = MAKE_STATUS(kStatusGroup_LPI2C, 9) }
LPI2C status return codes.`

Driver version

- `#define FSL_LPI2C_DRIVER_VERSION (MAKE_VERSION(2, 3, 1))`
LPI2C driver version.

22.2 Macro Definition Documentation

22.2.1 `#define FSL_LPI2C_DRIVER_VERSION (MAKE_VERSION(2, 3, 1))`

22.2.2 #define I2C_RETRY_TIMES 0U /* Define to zero means keep waiting until the flag is assert/deassert. */

22.3 Enumeration Type Documentation

22.3.1 anonymous enum

Enumerator

kStatus_LPI2C_Busy The master is already performing a transfer.

kStatus_LPI2C_Idle The slave driver is idle.

kStatus_LPI2C_Nak The slave device sent a NAK in response to a byte.

kStatus_LPI2C_FifoError FIFO under run or overrun.

kStatus_LPI2C_BitError Transferred bit was not seen on the bus.

kStatus_LPI2C_ArbitrationLost Arbitration lost error.

kStatus_LPI2C_PinLowTimeout SCL or SDA were held low longer than the timeout.

kStatus_LPI2C_NoTransferInProgress Attempt to abort a transfer when one is not in progress.

kStatus_LPI2C_DmaRequestFail DMA request failed.

kStatus_LPI2C_Timeout Timeout polling status flags.

22.4 LPI2C Master Driver

22.4.1 Overview

Data Structures

- struct `lpi2c_master_config_t`
Structure with settings to initialize the LPI2C master module. [More...](#)
- struct `lpi2c_data_match_config_t`
LPI2C master data match configuration structure. [More...](#)
- struct `lpi2c_master_transfer_t`
Non-blocking transfer descriptor structure. [More...](#)
- struct `lpi2c_master_handle_t`
Driver handle for master non-blocking APIs. [More...](#)

Typedefs

- typedef void(* `lpi2c_master_transfer_callback_t`)(LPI2C_Type *base, `lpi2c_master_handle_t` *handle, `status_t` completionStatus, void *userData)
Master completion callback function pointer type.
- typedef void(* `lpi2c_master_isr_t`)(LPI2C_Type *base, void *handle)
Typedef for master interrupt handler, used internally for LPI2C master interrupt and EDMA transactional APIs.

Enumerations

- enum `_lpi2c_master_flags` {

`kLPI2C_MasterTxReadyFlag` = LPI2C_MSR_TDF_MASK,
`kLPI2C_MasterRxReadyFlag` = LPI2C_MSR_RDF_MASK,
`kLPI2C_MasterEndOfPacketFlag` = LPI2C_MSR_EPF_MASK,
`kLPI2C_MasterStopDetectFlag` = LPI2C_MSR_SDF_MASK,
`kLPI2C_MasterNackDetectFlag` = LPI2C_MSR_NDF_MASK,
`kLPI2C_MasterArbitrationLostFlag` = LPI2C_MSR_ALF_MASK,
`kLPI2C_MasterFifoErrFlag` = LPI2C_MSR_FEF_MASK,
`kLPI2C_MasterPinLowTimeoutFlag` = LPI2C_MSR_PLTF_MASK,
`kLPI2C_MasterDataMatchFlag` = LPI2C_MSR_DMF_MASK,
`kLPI2C_MasterBusyFlag` = LPI2C_MSR_MBF_MASK,
`kLPI2C_MasterBusBusyFlag` = LPI2C_MSR_BBF_MASK,
`kLPI2C_MasterClearFlags`,
`kLPI2C_MasterIrqFlags`,
`kLPI2C_MasterErrorFlags` }

LPI2C master peripheral flags.
- enum `lpi2c_direction_t` {

`kLPI2C_Write` = 0U,
`kLPI2C_Read` = 1U }

- *Direction of master and slave transfers.*
- enum `lpi2c_master_pin_config_t` {

 `kLPI2C_2PinOpenDrain` = 0x0U,

 `kLPI2C_2PinOutputOnly` = 0x1U,

 `kLPI2C_2PinPushPull` = 0x2U,

 `kLPI2C_4PinPushPull` = 0x3U,

 `kLPI2C_2PinOpenDrainWithSeparateSlave`,

 `kLPI2C_2PinOutputOnlyWithSeparateSlave`,

 `kLPI2C_2PinPushPullWithSeparateSlave`,

 `kLPI2C_4PinPushPullWithInvertedOutput` = 0x7U }
- LPI2C pin configuration.*
- enum `lpi2c_host_request_source_t` {

 `kLPI2C_HostRequestExternalPin` = 0x0U,

 `kLPI2C_HostRequestInputTrigger` = 0x1U }
- LPI2C master host request selection.*
- enum `lpi2c_host_request_polarity_t` {

 `kLPI2C_HostRequestPinActiveLow` = 0x0U,

 `kLPI2C_HostRequestPinActiveHigh` = 0x1U }
- LPI2C master host request pin polarity configuration.*
- enum `lpi2c_data_match_config_mode_t` {

 `kLPI2C_MatchDisabled` = 0x0U,

 `kLPI2C_1stWordEqualsM0OrM1` = 0x2U,

 `kLPI2C_AnyWordEqualsM0OrM1` = 0x3U,

 `kLPI2C_1stWordEqualsM0And2ndWordEqualsM1`,

 `kLPI2C_AnyWordEqualsM0AndNextWordEqualsM1`,

 `kLPI2C_1stWordAndM1EqualsM0AndM1`,

 `kLPI2C_AnyWordAndM1EqualsM0AndM1` }
- LPI2C master data match configuration modes.*
- enum `_lpi2c_master_transfer_flags` {

 `kLPI2C_TransferDefaultFlag` = 0x00U,

 `kLPI2C_TransferNoStartFlag` = 0x01U,

 `kLPI2C_TransferRepeatedStartFlag` = 0x02U,

 `kLPI2C_TransferNoStopFlag` = 0x04U }
- Transfer option flags.*

Initialization and deinitialization

- void `LPI2C_MasterGetDefaultConfig` (`lpi2c_master_config_t` *`masterConfig`)

 Provides a default configuration for the LPI2C master peripheral.
- void `LPI2C_MasterInit` (`LPI2C_Type` *`base`, const `lpi2c_master_config_t` *`masterConfig`, `uint32_t` `sourceClock_Hz`)

 Initializes the LPI2C master peripheral.
- void `LPI2C_MasterDeinit` (`LPI2C_Type` *`base`)

 Deinitializes the LPI2C master peripheral.
- void `LPI2C_MasterConfigureDataMatch` (`LPI2C_Type` *`base`, const `lpi2c_data_match_config_t` *`matchConfig`)

Configures LPI2C master data match feature.

- **status_t LPI2C_MasterCheckAndClearError** (LPI2C_Type *base, uint32_t status)
- **status_t LPI2C_CheckForBusyBus** (LPI2C_Type *base)
- static void **LPI2C_MasterReset** (LPI2C_Type *base)

Performs a software reset.

- static void **LPI2C_MasterEnable** (LPI2C_Type *base, bool enable)
- Enables or disables the LPI2C module as master.*

Status

- static uint32_t **LPI2C_MasterGetStatusFlags** (LPI2C_Type *base)
Gets the LPI2C master status flags.
- static void **LPI2C_MasterClearStatusFlags** (LPI2C_Type *base, uint32_t statusMask)
Clears the LPI2C master status flag state.

Interrupts

- static void **LPI2C_MasterEnableInterrupts** (LPI2C_Type *base, uint32_t interruptMask)
Enables the LPI2C master interrupt requests.
- static void **LPI2C_MasterDisableInterrupts** (LPI2C_Type *base, uint32_t interruptMask)
Disables the LPI2C master interrupt requests.
- static uint32_t **LPI2C_MasterGetEnabledInterrupts** (LPI2C_Type *base)
Returns the set of currently enabled LPI2C master interrupt requests.

DMA control

- static void **LPI2C_MasterEnableDMA** (LPI2C_Type *base, bool enableTx, bool enableRx)
Enables or disables LPI2C master DMA requests.
- static uint32_t **LPI2C_MasterGetTxFifoAddress** (LPI2C_Type *base)
Gets LPI2C master transmit data register address for DMA transfer.
- static uint32_t **LPI2C_MasterGetRxFifoAddress** (LPI2C_Type *base)
Gets LPI2C master receive data register address for DMA transfer.

FIFO control

- static void **LPI2C_MasterSetWatermarks** (LPI2C_Type *base, size_t txWords, size_t rxWords)
Sets the watermarks for LPI2C master FIFOs.
- static void **LPI2C_MasterGetFifoCounts** (LPI2C_Type *base, size_t *rxCount, size_t *txCount)
Gets the current number of words in the LPI2C master FIFOs.

Bus operations

- void **LPI2C_MasterSetBaudRate** (LPI2C_Type *base, uint32_t sourceClock_Hz, uint32_t baudRate_Hz)

- Sets the I2C bus frequency for master transactions.
- static bool [LPI2C_MasterGetBusIdleState](#) (LPI2C_Type *base)
Returns whether the bus is idle.
- [status_t LPI2C_MasterStart](#) (LPI2C_Type *base, uint8_t address, [lpi2c_direction_t](#) dir)
Sends a START signal and slave address on the I2C bus.
- static [status_t LPI2C_MasterRepeatedStart](#) (LPI2C_Type *base, uint8_t address, [lpi2c_direction_t](#) dir)
Sends a repeated START signal and slave address on the I2C bus.
- [status_t LPI2C_MasterSend](#) (LPI2C_Type *base, void *txBuff, size_t txSize)
Performs a polling send transfer on the I2C bus.
- [status_t LPI2C_MasterReceive](#) (LPI2C_Type *base, void *rxBuff, size_t rxSize)
Performs a polling receive transfer on the I2C bus.
- [status_t LPI2C_MasterStop](#) (LPI2C_Type *base)
Sends a STOP signal on the I2C bus.
- [status_t LPI2C_MasterTransferBlocking](#) (LPI2C_Type *base, [lpi2c_master_transfer_t](#) *transfer)
Performs a master polling transfer on the I2C bus.

Non-blocking

- void [LPI2C_MasterTransferCreateHandle](#) (LPI2C_Type *base, [lpi2c_master_handle_t](#) *handle, [lpi2c_master_transfer_callback_t](#) callback, void *userData)
Creates a new handle for the LPI2C master non-blocking APIs.
- [status_t LPI2C_MasterTransferNonBlocking](#) (LPI2C_Type *base, [lpi2c_master_handle_t](#) *handle, [lpi2c_master_transfer_t](#) *transfer)
Performs a non-blocking transaction on the I2C bus.
- [status_t LPI2C_MasterTransferGetCount](#) (LPI2C_Type *base, [lpi2c_master_handle_t](#) *handle, size_t *count)
Returns number of bytes transferred so far.
- void [LPI2C_MasterTransferAbort](#) (LPI2C_Type *base, [lpi2c_master_handle_t](#) *handle)
Terminates a non-blocking LPI2C master transmission early.

IRQ handler

- void [LPI2C_MasterTransferHandleIRQ](#) (LPI2C_Type *base, void *lpi2cMasterHandle)
Reusable routine to handle master interrupts.

22.4.2 Data Structure Documentation

22.4.2.1 struct lpi2c_master_config_t

This structure holds configuration settings for the LPI2C peripheral. To initialize this structure to reasonable defaults, call the [LPI2C_MasterGetDefaultConfig\(\)](#) function and pass a pointer to your configuration structure instance.

The configuration structure can be made constant so it resides in flash.

Data Fields

- bool `enableMaster`
Whether to enable master mode.
 - bool `enableDoze`
Whether master is enabled in doze mode.
 - bool `debugEnable`
Enable transfers to continue when halted in debug mode.
 - bool `ignoreAck`
Whether to ignore ACK/NACK.
 - `lpi2c_master_pin_config_t pinConfig`
The pin configuration option.
 - `uint32_t baudRate_Hz`
Desired baud rate in Hertz.
 - `uint32_t busIdleTimeout_ns`
Bus idle timeout in nanoseconds.
 - `uint32_t pinLowTimeout_ns`
Pin low timeout in nanoseconds.
 - `uint8_t sdaGlitchFilterWidth_ns`
Width in nanoseconds of glitch filter on SDA pin.
 - `uint8_t sclGlitchFilterWidth_ns`
Width in nanoseconds of glitch filter on SCL pin.
 - struct {
 - bool `enable`
Enable host request.
 - `lpi2c_host_request_source_t source`
Host request source.
 - `lpi2c_host_request_polarity_t polarity`
Host request pin polarity.
} `hostRequest`
- Host request options.*

Field Documentation

- (1) `bool lpi2c_master_config_t::enableMaster`
- (2) `bool lpi2c_master_config_t::enableDoze`
- (3) `bool lpi2c_master_config_t::debugEnable`
- (4) `bool lpi2c_master_config_t::ignoreAck`
- (5) `lpi2c_master_pin_config_t lpi2c_master_config_t::pinConfig`
- (6) `uint32_t lpi2c_master_config_t::baudRate_Hz`
- (7) `uint32_t lpi2c_master_config_t::busIdleTimeout_ns`

Set to 0 to disable.

(8) `uint32_t lpi2c_master_config_t::pinLowTimeout_ns`

Set to 0 to disable.

(9) `uint8_t lpi2c_master_config_t::sdaGlitchFilterWidth_ns`

Set to 0 to disable.

(10) `uint8_t lpi2c_master_config_t::sclGlitchFilterWidth_ns`

Set to 0 to disable.

(11) `bool lpi2c_master_config_t::enable`

(12) `lpi2c_host_request_source_t lpi2c_master_config_t::source`

(13) `lpi2c_host_request_polarity_t lpi2c_master_config_t::polarity`

(14) `struct { ... } lpi2c_master_config_t::hostRequest`

22.4.2.2 struct lpi2c_data_match_config_t

Data Fields

- `lpi2c_data_match_config_mode_t matchMode`
Data match configuration setting.
- `bool rxDataMatchOnly`
When set to true, received data is ignored until a successful match.
- `uint32_t match0`
Match value 0.
- `uint32_t match1`
Match value 1.

Field Documentation

(1) `lpi2c_data_match_config_mode_t lpi2c_data_match_config_t::matchMode`

(2) `bool lpi2c_data_match_config_t::rxDataMatchOnly`

(3) `uint32_t lpi2c_data_match_config_t::match0`

(4) `uint32_t lpi2c_data_match_config_t::match1`

22.4.2.3 struct _lpi2c_master_transfer

This structure is used to pass transaction parameters to the [LPI2C_MasterTransferNonBlocking\(\)](#) API.

Data Fields

- `uint32_t flags`

- **uint16_t slaveAddress**
The 7-bit slave address.
- **lpi2c_direction_t direction**
Either `kLPI2C_Read` or `kLPI2C_Write`.
- **uint32_t subaddress**
Sub address.
- **size_t subaddressSize**
Length of sub address to send in bytes.
- **void * data**
Pointer to data to transfer.
- **size_t dataSize**
Number of bytes to transfer.

Field Documentation

(1) **uint32_t lpi2c_master_transfer_t::flags**

See enumeration `_lpi2c_master_transfer_flags` for available options. Set to 0 or `kLPI2C_TransferDefaultFlag` for normal transfers.

(2) **uint16_t lpi2c_master_transfer_t::slaveAddress**

(3) **lpi2c_direction_t lpi2c_master_transfer_t::direction**

(4) **uint32_t lpi2c_master_transfer_t::subaddress**

Transferred MSB first.

(5) **size_t lpi2c_master_transfer_t::subaddressSize**

Maximum size is 4 bytes.

(6) **void* lpi2c_master_transfer_t::data**

(7) **size_t lpi2c_master_transfer_t::dataSize**

22.4.2.4 struct _lpi2c_master_handle

Note

The contents of this structure are private and subject to change.

Data Fields

- **uint8_t state**
Transfer state machine current state.
- **uint16_t remainingBytes**
Remaining byte count in current state.
- **uint8_t * buf**

- *Buffer pointer for current state.*
- `uint16_t commandBuffer[6]`
LPI2C command sequence.
- `lpi2c_master_transfer_t transfer`
Copy of the current transfer info.
- `lpi2c_master_transfer_callback_t completionCallback`
Callback function pointer.
- `void *userData`
Application data passed to callback.

Field Documentation

- (1) `uint8_t lpi2c_master_handle_t::state`
- (2) `uint16_t lpi2c_master_handle_t::remainingBytes`
- (3) `uint8_t* lpi2c_master_handle_t::buf`
- (4) `uint16_t lpi2c_master_handle_t::commandBuffer[6]`

When all 6 command words are used: Start&addr&write[1 word] + subaddr[4 words] + restart&addr&read[1 word]

- (5) `lpi2c_master_transfer_t lpi2c_master_handle_t::transfer`
- (6) `lpi2c_master_transfer_callback_t lpi2c_master_handle_t::completionCallback`
- (7) `void* lpi2c_master_handle_t::userData`

22.4.3 Typedef Documentation

22.4.3.1 `typedef void(* lpi2c_master_transfer_callback_t)(LPI2C_Type *base, lpi2c_master_handle_t *handle, status_t completionStatus, void *userData)`

This callback is used only for the non-blocking master transfer API. Specify the callback you wish to use in the call to [LPI2C_MasterTransferCreateHandle\(\)](#).

Parameters

<code>base</code>	The LPI2C peripheral base address.
<code>completion-Status</code>	Either kStatus_Success or an error code describing how the transfer completed.

<i>userData</i>	Arbitrary pointer-sized value passed from the application.
-----------------	--

22.4.4 Enumeration Type Documentation

22.4.4.1 enum _lpi2c_master_flags

The following status register flags can be cleared:

- [kLPI2C_MasterEndOfPacketFlag](#)
- [kLPI2C_MasterStopDetectFlag](#)
- [kLPI2C_MasterNackDetectFlag](#)
- [kLPI2C_MasterArbitrationLostFlag](#)
- [kLPI2C_MasterFifoErrFlag](#)
- [kLPI2C_MasterPinLowTimeoutFlag](#)
- [kLPI2C_MasterDataMatchFlag](#)

All flags except [kLPI2C_MasterBusyFlag](#) and [kLPI2C_MasterBusBusyFlag](#) can be enabled as interrupts.

Note

These enums are meant to be OR'd together to form a bit mask.

Enumerator

- kLPI2C_MasterTxReadyFlag* Transmit data flag.
- kLPI2C_MasterRxReadyFlag* Receive data flag.
- kLPI2C_MasterEndOfPacketFlag* End Packet flag.
- kLPI2C_MasterStopDetectFlag* Stop detect flag.
- kLPI2C_MasterNackDetectFlag* NACK detect flag.
- kLPI2C_MasterArbitrationLostFlag* Arbitration lost flag.
- kLPI2C_MasterFifoErrFlag* FIFO error flag.
- kLPI2C_MasterPinLowTimeoutFlag* Pin low timeout flag.
- kLPI2C_MasterDataMatchFlag* Data match flag.
- kLPI2C_MasterBusyFlag* Master busy flag.
- kLPI2C_MasterBusBusyFlag* Bus busy flag.
- kLPI2C_MasterClearFlags* All flags which are cleared by the driver upon starting a transfer.
- kLPI2C_MasterIrqFlags* IRQ sources enabled by the non-blocking transactional API.
- kLPI2C_MasterErrorFlags* Errors to check for.

22.4.4.2 enum lpi2c_direction_t

Enumerator

- kLPI2C_Write* Master transmit.
- kLPI2C_Read* Master receive.

22.4.4.3 enum lpi2c_master_pin_config_t

Enumerator

kLPI2C_2PinOpenDrain LPI2C Configured for 2-pin open drain mode.

kLPI2C_2PinOutputOnly LPI2C Configured for 2-pin output only mode (ultra-fast mode)

kLPI2C_2PinPushPull LPI2C Configured for 2-pin push-pull mode.

kLPI2C_4PinPushPull LPI2C Configured for 4-pin push-pull mode.

kLPI2C_2PinOpenDrainWithSeparateSlave LPI2C Configured for 2-pin open drain mode with separate LPI2C slave.

kLPI2C_2PinOutputOnlyWithSeparateSlave LPI2C Configured for 2-pin output only mode(ultra-fast mode) with separate LPI2C slave.

kLPI2C_2PinPushPullWithSeparateSlave LPI2C Configured for 2-pin push-pull mode with separate LPI2C slave.

kLPI2C_4PinPushPullWithInvertedOutput LPI2C Configured for 4-pin push-pull mode(inverted outputs)

22.4.4.4 enum lpi2c_host_request_source_t

Enumerator

kLPI2C_HostRequestExternalPin Select the LPI2C_HREQ pin as the host request input.

kLPI2C_HostRequestInputTrigger Select the input trigger as the host request input.

22.4.4.5 enum lpi2c_host_request_polarity_t

Enumerator

kLPI2C_HostRequestPinActiveLow Configure the LPI2C_HREQ pin active low.

kLPI2C_HostRequestPinActiveHigh Configure the LPI2C_HREQ pin active high.

22.4.4.6 enum lpi2c_data_match_config_mode_t

Enumerator

kLPI2C_MatchDisabled LPI2C Match Disabled.

kLPI2C_1stWordEqualsM0OrM1 LPI2C Match Enabled and 1st data word equals MATCH0 OR MATCH1.

kLPI2C_AnyWordEqualsM0OrM1 LPI2C Match Enabled and any data word equals MATCH0 OR MATCH1.

kLPI2C_1stWordEqualsM0And2ndWordEqualsM1 LPI2C Match Enabled and 1st data word equals MATCH0, 2nd data equals MATCH1.

kLPI2C_AnyWordEqualsM0AndNextWordEqualsM1 LPI2C Match Enabled and any data word equals MATCH0, next data equals MATCH1.

kLPI2C_1stWordAndM1EqualsM0AndM1 LPI2C Match Enabled and 1st data word and MATCH0 equals MATCH0 and MATCH1.

kLPI2C_AnyWordAndM1EqualsM0AndM1 LPI2C Match Enabled and any data word and MATCH0 equals MATCH0 and MATCH1.

22.4.4.7 enum _lpi2c_master_transfer_flags

Note

These enumerations are intended to be OR'd together to form a bit mask of options for the `_lpi2c_master_transfer::flags` field.

Enumerator

kLPI2C_TransferDefaultFlag Transfer starts with a start signal, stops with a stop signal.

kLPI2C_TransferNoStartFlag Don't send a start condition, address, and sub address.

kLPI2C_TransferRepeatedStartFlag Send a repeated start condition.

kLPI2C_TransferNoStopFlag Don't send a stop condition.

22.4.5 Function Documentation

22.4.5.1 void LPI2C_MasterGetDefaultConfig (`lpi2c_master_config_t * masterConfig`)

This function provides the following default configuration for the LPI2C master peripheral:

```
* masterConfig->enableMaster          = true;
* masterConfig->debugEnable         = false;
* masterConfig->ignoreAck           = false;
* masterConfig->pinConfig           = kLPI2C_2PinOpenDrain;
* masterConfig->baudRate_Hz        = 100000U;
* masterConfig->busIdleTimeout_ns   = 0;
* masterConfig->pinLowTimeout_ns    = 0;
* masterConfig->sdaGlitchFilterWidth_ns = 0;
* masterConfig->sclGlitchFilterWidth_ns = 0;
* masterConfig->hostRequest.enable   = false;
* masterConfig->hostRequest.source    = kLPI2C_HostRequestExternalPin;
* masterConfig->hostRequest.polarity   = kLPI2C_HostRequestPinActiveHigh;
*
```

After calling this function, you can override any settings in order to customize the configuration, prior to initializing the master driver with [LPI2C_MasterInit\(\)](#).

Parameters

out	<i>masterConfig</i>	User provided configuration structure for default values. Refer to lpi2c_master_config_t .
-----	---------------------	--

22.4.5.2 void LPI2C_MasterInit (LPI2C_Type * *base*, const lpi2c_master_config_t * *masterConfig*, uint32_t *sourceClock_Hz*)

This function enables the peripheral clock and initializes the LPI2C master peripheral as described by the user provided configuration. A software reset is performed prior to configuration.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>masterConfig</i>	User provided peripheral configuration. Use LPI2C_MasterGetDefaultConfig() to get a set of defaults that you can override.
<i>sourceClock_Hz</i>	Frequency in Hertz of the LPI2C functional clock. Used to calculate the baud rate divisors, filter widths, and timeout periods.

22.4.5.3 void LPI2C_MasterDeinit (LPI2C_Type * *base*)

This function disables the LPI2C master peripheral and gates the clock. It also performs a software reset to restore the peripheral to reset conditions.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

22.4.5.4 void LPI2C_MasterConfigureDataMatch (LPI2C_Type * *base*, const lpi2c_data_match_config_t * *matchConfig*)

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>matchConfig</i>	Settings for the data match feature.

22.4.5.5 static void LPI2C_MasterReset (LPI2C_Type * *base*) [inline], [static]

Restores the LPI2C master peripheral to reset conditions.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

22.4.5.6 static void LPI2C_MasterEnable (LPI2C_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>enable</i>	Pass true to enable or false to disable the specified LPI2C as master.

22.4.5.7 static uint32_t LPI2C_MasterGetStatusFlags (LPI2C_Type * *base*) [inline], [static]

A bit mask with the state of all LPI2C master status flags is returned. For each flag, the corresponding bit in the return value is set if the flag is asserted.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

State of the status flags:

- 1: related status flag is set.
- 0: related status flag is not set.

See Also

[_lpi2c_master_flags](#)

22.4.5.8 static void LPI2C_MasterClearStatusFlags (LPI2C_Type * *base*, uint32_t *statusMask*) [inline], [static]

The following status register flags can be cleared:

- [kLPI2C_MasterEndOfPacketFlag](#)
- [kLPI2C_MasterStopDetectFlag](#)
- [kLPI2C_MasterNackDetectFlag](#)
- [kLPI2C_MasterArbitrationLostFlag](#)

- kLPI2C_MasterFifoErrFlag
- kLPI2C_MasterPinLowTimeoutFlag
- kLPI2C_MasterDataMatchFlag

Attempts to clear other flags has no effect.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>statusMask</i>	A bitmask of status flags that are to be cleared. The mask is composed of _lpi2c_master_flags enumerators OR'd together. You may pass the result of a previous call to LPI2C_MasterGetStatusFlags() .

See Also

[_lpi2c_master_flags](#).

22.4.5.9 static void LPI2C_MasterEnableInterrupts (LPI2C_Type * *base*, uint32_t *interruptMask*) [inline], [static]

All flags except [kLPI2C_MasterBusyFlag](#) and [kLPI2C_MasterBusBusyFlag](#) can be enabled as interrupts.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>interruptMask</i>	Bit mask of interrupts to enable. See _lpi2c_master_flags for the set of constants that should be OR'd together to form the bit mask.

22.4.5.10 static void LPI2C_MasterDisableInterrupts (LPI2C_Type * *base*, uint32_t *interruptMask*) [inline], [static]

All flags except [kLPI2C_MasterBusyFlag](#) and [kLPI2C_MasterBusBusyFlag](#) can be disabled as interrupts.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>interruptMask</i>	Bit mask of interrupts to disable. See _lpi2c_master_flags for the set of constants that should be OR'd together to form the bit mask.

22.4.5.11 static uint32_t LPI2C_MasterGetEnabledInterrupts (LPI2C_Type * *base*) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

A bitmask composed of _lpi2c_master_flags enumerators OR'd together to indicate the set of enabled interrupts.

22.4.5.12 static void LPI2C_MasterEnableDMA (LPI2C_Type * *base*, bool *enableTx*, bool *enableRx*) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>enableTx</i>	Enable flag for transmit DMA request. Pass true for enable, false for disable.
<i>enableRx</i>	Enable flag for receive DMA request. Pass true for enable, false for disable.

22.4.5.13 static uint32_t LPI2C_MasterGetTxFifoAddress (LPI2C_Type * *base*) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

The LPI2C Master Transmit Data Register address.

22.4.5.14 static uint32_t LPI2C_MasterGetRxFifoAddress (LPI2C_Type * *base*) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

The LPI2C Master Receive Data Register address.

22.4.5.15 static void LPI2C_MasterSetWatermarks (*LPI2C_Type* * *base*, *size_t* *txWords*, *size_t* *rxWords*) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>txWords</i>	Transmit FIFO watermark value in words. The kLPI2C_MasterTxReadyFlag flag is set whenever the number of words in the transmit FIFO is equal or less than <i>txWords</i> . Writing a value equal or greater than the FIFO size is truncated.
<i>rxWords</i>	Receive FIFO watermark value in words. The kLPI2C_MasterRxReadyFlag flag is set whenever the number of words in the receive FIFO is greater than <i>rxWords</i> . Writing a value equal or greater than the FIFO size is truncated.

22.4.5.16 static void LPI2C_MasterGetFifoCounts (*LPI2C_Type* * *base*, *size_t* * *rxCount*, *size_t* * *txCount*) [inline], [static]

Parameters

	<i>base</i>	The LPI2C peripheral base address.
out	<i>txCount</i>	Pointer through which the current number of words in the transmit FIFO is returned. Pass NULL if this value is not required.
out	<i>rxCount</i>	Pointer through which the current number of words in the receive FIFO is returned. Pass NULL if this value is not required.

22.4.5.17 void LPI2C_MasterSetBaudRate (*LPI2C_Type* * *base*, *uint32_t* *sourceClock_Hz*, *uint32_t* *baudRate_Hz*)

The LPI2C master is automatically disabled and re-enabled as necessary to configure the baud rate. Do not call this function during a transfer, or the transfer is aborted.

Note

Please note that the second parameter is the clock frequency of LPI2C module, the third parameter means user configured bus baudrate, this implementation is different from other I2C drivers which use baudrate configuration as second parameter and source clock frequency as third parameter.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>sourceClock_Hz</i>	LPI2C functional clock frequency in Hertz.
<i>baudRate_Hz</i>	Requested bus frequency in Hertz.

22.4.5.18 static bool LPI2C_MasterGetBusIdleState (LPI2C_Type * *base*) [inline], [static]

Requires the master mode to be enabled.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Return values

<i>true</i>	Bus is busy.
<i>false</i>	Bus is idle.

22.4.5.19 status_t LPI2C_MasterStart (LPI2C_Type * *base*, uint8_t *address*, lpi2c_direction_t *dir*)

This function is used to initiate a new master mode transfer. First, the bus state is checked to ensure that another master is not occupying the bus. Then a START signal is transmitted, followed by the 7-bit address specified in the *address* parameter. Note that this function does not actually wait until the START and address are successfully sent on the bus before returning.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>address</i>	7-bit slave device address, in bits [6:0].
<i>dir</i>	Master transfer direction, either kLPI2C_Read or kLPI2C_Write . This parameter is used to set the R/w bit (bit 0) in the transmitted slave address.

Return values

<i>kStatus_Success</i>	START signal and address were successfully enqueued in the transmit FIFO.
<i>kStatus_LPI2C_Busy</i>	Another master is currently utilizing the bus.

22.4.5.20 static status_t LPI2C_MasterRepeatedStart (LPI2C_Type * *base*, uint8_t *address*, lpi2c_direction_t *dir*) [inline], [static]

This function is used to send a Repeated START signal when a transfer is already in progress. Like [LPI2C_MasterStart\(\)](#), it also sends the specified 7-bit address.

Note

This function exists primarily to maintain compatible APIs between LPI2C and I2C drivers, as well as to better document the intent of code that uses these APIs.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>address</i>	7-bit slave device address, in bits [6:0].
<i>dir</i>	Master transfer direction, either kLPI2C_Read or kLPI2C_Write . This parameter is used to set the R/w bit (bit 0) in the transmitted slave address.

Return values

<i>kStatus_Success</i>	Repeated START signal and address were successfully enqueued in the transmit FIFO.
<i>kStatus_LPI2C_Busy</i>	Another master is currently utilizing the bus.

22.4.5.21 status_t LPI2C_MasterSend (LPI2C_Type * *base*, void * *txBuff*, size_t *txSize*)

Sends up to *txSize* number of bytes to the previously addressed slave device. The slave may reply with a NAK to any byte in order to terminate the transfer early. If this happens, this function returns [kStatus_LPI2C_Nak](#).

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>txBuff</i>	The pointer to the data to be transferred.
<i>txSize</i>	The length in bytes of the data to be transferred.

Return values

<i>kStatus_Success</i>	Data was sent successfully.
<i>kStatus_LPI2C_Busy</i>	Another master is currently utilizing the bus.
<i>kStatus_LPI2C_Nak</i>	The slave device sent a NAK in response to a byte.
<i>kStatus_LPI2C_FifoError</i>	FIFO under run or over run.
<i>kStatus_LPI2C_ArbitrationLost</i>	Arbitration lost error.
<i>kStatus_LPI2C_PinLowTimeout</i>	SCL or SDA were held low longer than the timeout.

22.4.5.22 status_t LPI2C_MasterReceive (LPI2C_Type * *base*, void * *rxBuff*, size_t *rxSize*)

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>rxBuff</i>	The pointer to the data to be transferred.
<i>rxSize</i>	The length in bytes of the data to be transferred.

Return values

<i>kStatus_Success</i>	Data was received successfully.
<i>kStatus_LPI2C_Busy</i>	Another master is currently utilizing the bus.
<i>kStatus_LPI2C_Nak</i>	The slave device sent a NAK in response to a byte.
<i>kStatus_LPI2C_FifoError</i>	FIFO under run or overrun.
<i>kStatus_LPI2C_ArbitrationLost</i>	Arbitration lost error.
<i>kStatus_LPI2C_PinLowTimeout</i>	SCL or SDA were held low longer than the timeout.

22.4.5.23 status_t LPI2C_MasterStop (LPI2C_Type * *base*)

This function does not return until the STOP signal is seen on the bus, or an error occurs.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Return values

<i>kStatus_Success</i>	The STOP signal was successfully sent on the bus and the transaction terminated.
<i>kStatus_LPI2C_Busy</i>	Another master is currently utilizing the bus.
<i>kStatus_LPI2C_Nak</i>	The slave device sent a NAK in response to a byte.
<i>kStatus_LPI2C_FifoError</i>	FIFO under run or overrun.
<i>kStatus_LPI2C_ArbitrationLost</i>	Arbitration lost error.
<i>kStatus_LPI2C_PinLowTimeout</i>	SCL or SDA were held low longer than the timeout.

22.4.5.24 status_t LPI2C_MasterTransferBlocking (**LPI2C_Type * base,** **lpi2c_master_transfer_t * transfer**)

Note

The API does not return until the transfer succeeds or fails due to error happens during transfer.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>transfer</i>	Pointer to the transfer structure.

Return values

<i>kStatus_Success</i>	Data was received successfully.
<i>kStatus_LPI2C_Busy</i>	Another master is currently utilizing the bus.
<i>kStatus_LPI2C_Nak</i>	The slave device sent a NAK in response to a byte.
<i>kStatus_LPI2C_FifoError</i>	FIFO under run or overrun.
<i>kStatus_LPI2C_ArbitrationLost</i>	Arbitration lost error.
<i>kStatus_LPI2C_PinLowTimeout</i>	SCL or SDA were held low longer than the timeout.

**22.4.5.25 void LPI2C_MasterTransferCreateHandle (*LPI2C_Type * base*,
*Ipi2c_master_handle_t * handle*, *Ipi2c_master_transfer_callback_t callback*,
*void * userData*)**

The creation of a handle is for use with the non-blocking APIs. Once a handle is created, there is not a corresponding destroy handle. If the user wants to terminate a transfer, the [LPI2C_MasterTransferAbort\(\)](#) API shall be called.

Note

The function also enables the NVIC IRQ for the input LPI2C. Need to notice that on some SoCs the LPI2C IRQ is connected to INTMUX, in this case user needs to enable the associated INTMUX IRQ in application.

Parameters

	<i>base</i>	The LPI2C peripheral base address.
out	<i>handle</i>	Pointer to the LPI2C master driver handle.
	<i>callback</i>	User provided pointer to the asynchronous callback function.
	<i>userData</i>	User provided pointer to the application callback data.

**22.4.5.26 status_t LPI2C_MasterTransferNonBlocking (*LPI2C_Type * base*,
*Ipi2c_master_handle_t * handle*, *Ipi2c_master_transfer_t * transfer*)**

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to the LPI2C master driver handle.
<i>transfer</i>	The pointer to the transfer descriptor.

Return values

<i>kStatus_Success</i>	The transaction was started successfully.
<i>kStatus_LPI2C_Busy</i>	Either another master is currently utilizing the bus, or a non-blocking transaction is already in progress.

**22.4.5.27 status_t LPI2C_MasterTransferGetCount (*LPI2C_Type * base*,
*Ipi2c_master_handle_t * handle*, *size_t * count*)**

Parameters

	<i>base</i>	The LPI2C peripheral base address.
	<i>handle</i>	Pointer to the LPI2C master driver handle.
out	<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Return values

<i>kStatus_Success</i>	
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.

22.4.5.28 void LPI2C_MasterTransferAbort (LPI2C_Type * *base*, Ipi2c_master_handle_t * *handle*)

Note

It is not safe to call this function from an IRQ handler that has a higher priority than the LPI2C peripheral's IRQ priority.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to the LPI2C master driver handle.

Return values

<i>kStatus_Success</i>	A transaction was successfully aborted.
<i>kStatus_LPI2C_Idle</i>	There is not a non-blocking transaction currently in progress.

22.4.5.29 void LPI2C_MasterTransferHandleIRQ (LPI2C_Type * *base*, void * *Ipi2cMasterHandle*)

Note

This function does not need to be called unless you are reimplementing the nonblocking API's interrupt handler routines to add special functionality.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>lpi2cMasterHandle</i>	Pointer to the LPI2C master driver handle.

22.5 LPI2C Slave Driver

22.5.1 Overview

Data Structures

- struct `lpi2c_slave_config_t`
Structure with settings to initialize the LPI2C slave module. [More...](#)
- struct `lpi2c_slave_transfer_t`
LPI2C slave transfer structure. [More...](#)
- struct `lpi2c_slave_handle_t`
LPI2C slave handle structure. [More...](#)

Typedefs

- typedef void(* `lpi2c_slave_transfer_callback_t`)`(LPI2C_Type *base, lpi2c_slave_transfer_t *transfer, void *userData)`
Slave event callback function pointer type.

Enumerations

- enum `_lpi2c_slave_flags` {

`kLPI2C_SlaveTxReadyFlag` = LPI2C_SSR_TDF_MASK,
`kLPI2C_SlaveRxReadyFlag` = LPI2C_SSR_RDF_MASK,
`kLPI2C_SlaveAddressValidFlag` = LPI2C_SSR_AVF_MASK,
`kLPI2C_SlaveTransmitAckFlag` = LPI2C_SSR_TAF_MASK,
`kLPI2C_SlaveRepeatedStartDetectFlag` = LPI2C_SSR_RSF_MASK,
`kLPI2C_SlaveStopDetectFlag` = LPI2C_SSR_SDF_MASK,
`kLPI2C_SlaveBitErrFlag` = LPI2C_SSR_BEF_MASK,
`kLPI2C_SlaveFifoErrFlag` = LPI2C_SSR_FEF_MASK,
`kLPI2C_SlaveAddressMatch0Flag` = LPI2C_SSR_AM0F_MASK,
`kLPI2C_SlaveAddressMatch1Flag` = LPI2C_SSR_AM1F_MASK,
`kLPI2C_SlaveGeneralCallFlag` = LPI2C_SSR_GCF_MASK,
`kLPI2C_SlaveBusyFlag` = LPI2C_SSR_SBF_MASK,
`kLPI2C_SlaveBusBusyFlag` = LPI2C_SSR_BBF_MASK,
`kLPI2C_SlaveClearFlags`,
`kLPI2C_SlaveIrqFlags`,
`kLPI2C_SlaveErrorFlags` = `kLPI2C_SlaveFifoErrFlag | kLPI2C_SlaveBitErrFlag` }

LPI2C slave peripheral flags.
- enum `lpi2c_slave_address_match_t` {

`kLPI2C_MatchAddress0` = 0U,
`kLPI2C_MatchAddress0OrAddress1` = 2U,
`kLPI2C_MatchAddress0ThroughAddress1` = 6U }

LPI2C slave address match options.

- enum `lpi2c_slave_transfer_event_t` {

 `kLPI2C_SlaveAddressMatchEvent` = 0x01U,
`kLPI2C_SlaveTransmitEvent` = 0x02U,
`kLPI2C_SlaveReceiveEvent` = 0x04U,
`kLPI2C_SlaveTransmitAckEvent` = 0x08U,
`kLPI2C_SlaveRepeatedStartEvent` = 0x10U,
`kLPI2C_SlaveCompletionEvent` = 0x20U,
`kLPI2C_SlaveAllEvents` }

Set of events sent to the callback for non blocking slave transfers.

Slave initialization and deinitialization

- void `LPI2C_SlaveGetDefaultConfig` (`lpi2c_slave_config_t` *slaveConfig)
Provides a default configuration for the LPI2C slave peripheral.
- void `LPI2C_SlaveInit` (`LPI2C_Type` *base, const `lpi2c_slave_config_t` *slaveConfig, `uint32_t` sourceClock_Hz)
Initializes the LPI2C slave peripheral.
- void `LPI2C_SlaveDeinit` (`LPI2C_Type` *base)
Deinitializes the LPI2C slave peripheral.
- static void `LPI2C_SlaveReset` (`LPI2C_Type` *base)
Performs a software reset of the LPI2C slave peripheral.
- static void `LPI2C_SlaveEnable` (`LPI2C_Type` *base, bool enable)
Enables or disables the LPI2C module as slave.

Slave status

- static `uint32_t` `LPI2C_SlaveGetStatusFlags` (`LPI2C_Type` *base)
Gets the LPI2C slave status flags.
- static void `LPI2C_SlaveClearStatusFlags` (`LPI2C_Type` *base, `uint32_t` statusMask)
Clears the LPI2C status flag state.

Slave interrupts

- static void `LPI2C_SlaveEnableInterrupts` (`LPI2C_Type` *base, `uint32_t` interruptMask)
Enables the LPI2C slave interrupt requests.
- static void `LPI2C_SlaveDisableInterrupts` (`LPI2C_Type` *base, `uint32_t` interruptMask)
Disables the LPI2C slave interrupt requests.
- static `uint32_t` `LPI2C_SlaveGetEnabledInterrupts` (`LPI2C_Type` *base)
Returns the set of currently enabled LPI2C slave interrupt requests.

Slave DMA control

- static void `LPI2C_SlaveEnableDMA` (`LPI2C_Type` *base, bool enableAddressValid, bool enableRx, bool enableTx)

Enables or disables the LPI2C slave peripheral DMA requests.

Slave bus operations

- static bool [LPI2C_SlaveGetBusIdleState](#) (LPI2C_Type *base)
Returns whether the bus is idle.
- static void [LPI2C_SlaveTransmitAck](#) (LPI2C_Type *base, bool ackOrNack)
Transmits either an ACK or NAK on the I2C bus in response to a byte from the master.
- static uint32_t [LPI2C_SlaveGetReceivedAddress](#) (LPI2C_Type *base)
Returns the slave address sent by the I2C master.
- status_t [LPI2C_SlaveSend](#) (LPI2C_Type *base, void *txBuff, size_t txSize, size_t *actualTxSize)
Performs a polling send transfer on the I2C bus.
- status_t [LPI2C_SlaveReceive](#) (LPI2C_Type *base, void *rxBuff, size_t rxSize, size_t *actualRxSize)
Performs a polling receive transfer on the I2C bus.

Slave non-blocking

- void [LPI2C_SlaveTransferCreateHandle](#) (LPI2C_Type *base, lpi2c_slave_handle_t *handle, [lpi2c_slave_transfer_callback_t](#) callback, void *userData)
Creates a new handle for the LPI2C slave non-blocking APIs.
- status_t [LPI2C_SlaveTransferNonBlocking](#) (LPI2C_Type *base, lpi2c_slave_handle_t *handle, uint32_t eventMask)
Starts accepting slave transfers.
- status_t [LPI2C_SlaveTransferGetCount](#) (LPI2C_Type *base, lpi2c_slave_handle_t *handle, size_t *count)
Gets the slave transfer status during a non-blocking transfer.
- void [LPI2C_SlaveTransferAbort](#) (LPI2C_Type *base, lpi2c_slave_handle_t *handle)
Aborts the slave non-blocking transfers.

Slave IRQ handler

- void [LPI2C_SlaveTransferHandleIRQ](#) (LPI2C_Type *base, lpi2c_slave_handle_t *handle)
Reusable routine to handle slave interrupts.

22.5.2 Data Structure Documentation

22.5.2.1 struct lpi2c_slave_config_t

This structure holds configuration settings for the LPI2C slave peripheral. To initialize this structure to reasonable defaults, call the [LPI2C_SlaveGetDefaultConfig\(\)](#) function and pass a pointer to your configuration structure instance.

The configuration structure can be made constant so it resides in flash.

Data Fields

- bool `enableSlave`
Enable slave mode.
- uint8_t `address0`
Slave's 7-bit address.
- uint8_t `address1`
Alternate slave 7-bit address.
- `lpi2c_slave_address_match_t addressMatchMode`
Address matching options.
- bool `filterDozeEnable`
Enable digital glitch filter in doze mode.
- bool `filterEnable`
Enable digital glitch filter.
- bool `enableGeneralCall`
Enable general call address matching.
- bool `ignoreAck`
Continue transfers after a NACK is detected.
- bool `enableReceivedAddressRead`
Enable reading the address received address as the first byte of data.
- uint32_t `sdaGlitchFilterWidth_ns`
Width in nanoseconds of the digital filter on the SDA signal.
- uint32_t `sclGlitchFilterWidth_ns`
Width in nanoseconds of the digital filter on the SCL signal.
- uint32_t `dataValidDelay_ns`
Width in nanoseconds of the data valid delay.
- uint32_t `clockHoldTime_ns`
Width in nanoseconds of the clock hold time.
- bool `enableAck`
Enables SCL clock stretching during slave-transmit address byte(s) and slave-receiver address and data byte(s) to allow software to write the Transmit ACK Register before the ACK or NACK is transmitted.
- bool `enableTx`
Enables SCL clock stretching when the transmit data flag is set during a slave-transmit transfer.
- bool `enableRx`
Enables SCL clock stretching when receive data flag is set during a slave-receive transfer.
- bool `enableAddress`
Enables SCL clock stretching when the address valid flag is asserted.

Field Documentation

- (1) `bool lpi2c_slave_config_t::enableSlave`
- (2) `uint8_t lpi2c_slave_config_t::address0`
- (3) `uint8_t lpi2c_slave_config_t::address1`
- (4) `lpi2c_slave_address_match_t lpi2c_slave_config_t::addressMatchMode`
- (5) `bool lpi2c_slave_config_t::filterDozeEnable`
- (6) `bool lpi2c_slave_config_t::filterEnable`

(7) **bool lpi2c_slave_config_t::enableGeneralCall**

(8) **bool lpi2c_slave_config_t::enableAck**

Clock stretching occurs when transmitting the 9th bit. When enableAckSCLStall is enabled, there is no need to set either enableRxDataSCLStall or enableAddressSCLStall.

(9) **bool lpi2c_slave_config_t::enableTx**

(10) **bool lpi2c_slave_config_t::enableRx**

(11) **bool lpi2c_slave_config_t::enableAddress**

(12) **bool lpi2c_slave_config_t::ignoreAck**

(13) **bool lpi2c_slave_config_t::enableReceivedAddressRead**

(14) **uint32_t lpi2c_slave_config_t::sdaGlitchFilterWidth_ns**

Set to 0 to disable.

(15) **uint32_t lpi2c_slave_config_t::sclGlitchFilterWidth_ns**

Set to 0 to disable.

(16) **uint32_t lpi2c_slave_config_t::dataValidDelay_ns**

(17) **uint32_t lpi2c_slave_config_t::clockHoldTime_ns**

22.5.2.2 struct lpi2c_slave_transfer_t

Data Fields

- **lpi2c_slave_transfer_event_t event**
Reason the callback is being invoked.
- **uint8_t receivedAddress**
Matching address send by master.
- **uint8_t * data**
Transfer buffer.
- **size_t dataSize**
Transfer size.
- **status_t completionStatus**
Success or error code describing how the transfer completed.
- **size_t transferredCount**
Number of bytes actually transferred since start or last repeated start.

Field Documentation

(1) **lpi2c_slave_transfer_event_t lpi2c_slave_transfer_t::event**

- (2) `uint8_t lpi2c_slave_transfer_t::receivedAddress`
- (3) `status_t lpi2c_slave_transfer_t::completionStatus`

Only applies for [kLPI2C_SlaveCompletionEvent](#).

- (4) `size_t lpi2c_slave_transfer_t::transferredCount`

22.5.2.3 struct _lpi2c_slave_handle

Note

The contents of this structure are private and subject to change.

Data Fields

- `lpi2c_slave_transfer_t transfer`
LPI2C slave transfer copy.
- `bool isBusy`
Whether transfer is busy.
- `bool wasTransmit`
Whether the last transfer was a transmit.
- `uint32_t eventMask`
Mask of enabled events.
- `uint32_t transferredCount`
Count of bytes transferred.
- `lpi2c_slave_transfer_callback_t callback`
Callback function called at transfer event.
- `void *userData`
Callback parameter passed to callback.

Field Documentation

- (1) `lpi2c_slave_transfer_t lpi2c_slave_handle_t::transfer`
- (2) `bool lpi2c_slave_handle_t::isBusy`
- (3) `bool lpi2c_slave_handle_t::wasTransmit`
- (4) `uint32_t lpi2c_slave_handle_t::eventMask`
- (5) `uint32_t lpi2c_slave_handle_t::transferredCount`
- (6) `lpi2c_slave_transfer_callback_t lpi2c_slave_handle_t::callback`
- (7) `void* lpi2c_slave_handle_t::userData`

22.5.3 Typedef Documentation

22.5.3.1 **typedef void(* lpi2c_slave_transfer_callback_t)(LPI2C_Type *base, lpi2c_slave_transfer_t *transfer, void *userData)**

This callback is used only for the slave non-blocking transfer API. To install a callback, use the LPI2C_SlaveSetCallback() function after you have created a handle.

Parameters

<i>base</i>	Base address for the LPI2C instance on which the event occurred.
<i>transfer</i>	Pointer to transfer descriptor containing values passed to and/or from the callback.
<i>userData</i>	Arbitrary pointer-sized value passed from the application.

22.5.4 Enumeration Type Documentation**22.5.4.1 enum _lpi2c_slave_flags**

The following status register flags can be cleared:

- [kLPI2C_SlaveRepeatedStartDetectFlag](#)
- [kLPI2C_SlaveStopDetectFlag](#)
- [kLPI2C_SlaveBitErrFlag](#)
- [kLPI2C_SlaveFifoErrFlag](#)

All flags except [kLPI2C_SlaveBusyFlag](#) and [kLPI2C_SlaveBusBusyFlag](#) can be enabled as interrupts.

Note

These enumerations are meant to be OR'd together to form a bit mask.

Enumerator

- kLPI2C_SlaveTxReadyFlag* Transmit data flag.
kLPI2C_SlaveRxReadyFlag Receive data flag.
kLPI2C_SlaveAddressValidFlag Address valid flag.
kLPI2C_SlaveTransmitAckFlag Transmit ACK flag.
kLPI2C_SlaveRepeatedStartDetectFlag Repeated start detect flag.
kLPI2C_SlaveStopDetectFlag Stop detect flag.
kLPI2C_SlaveBitErrFlag Bit error flag.
kLPI2C_SlaveFifoErrFlag FIFO error flag.
kLPI2C_SlaveAddressMatch0Flag Address match 0 flag.
kLPI2C_SlaveAddressMatch1Flag Address match 1 flag.
kLPI2C_SlaveGeneralCallFlag General call flag.
kLPI2C_SlaveBusyFlag Master busy flag.
kLPI2C_SlaveBusBusyFlag Bus busy flag.
kLPI2C_SlaveClearFlags All flags which are cleared by the driver upon starting a transfer.
kLPI2C_SlaveIrqFlags IRQ sources enabled by the non-blocking transactional API.
kLPI2C_SlaveErrorFlags Errors to check for.

22.5.4.2 enum lpi2c_slave_address_match_t

Enumerator

kLPI2C_MatchAddress0 Match only address 0.

kLPI2C_MatchAddress0OrAddress1 Match either address 0 or address 1.

kLPI2C_MatchAddress0ThroughAddress1 Match a range of slave addresses from address 0 through address 1.

22.5.4.3 enum lpi2c_slave_transfer_event_t

These event enumerations are used for two related purposes. First, a bit mask created by OR'ing together events is passed to [LPI2C_SlaveTransferNonBlocking\(\)](#) in order to specify which events to enable. Then, when the slave callback is invoked, it is passed the current event through its *transfer* parameter.

Note

These enumerations are meant to be OR'd together to form a bit mask of events.

Enumerator

kLPI2C_SlaveAddressMatchEvent Received the slave address after a start or repeated start.

kLPI2C_SlaveTransmitEvent Callback is requested to provide data to transmit (slave-transmitter role).

kLPI2C_SlaveReceiveEvent Callback is requested to provide a buffer in which to place received data (slave-receiver role).

kLPI2C_SlaveTransmitAckEvent Callback needs to either transmit an ACK or NACK.

kLPI2C_SlaveRepeatedStartEvent A repeated start was detected.

kLPI2C_SlaveCompletionEvent A stop was detected, completing the transfer.

kLPI2C_SlaveAllEvents Bit mask of all available events.

22.5.5 Function Documentation

22.5.5.1 void LPI2C_SlaveGetDefaultConfig (lpi2c_slave_config_t * *slaveConfig*)

This function provides the following default configuration for the LPI2C slave peripheral:

```
* slaveConfig->enableSlave          = true;
* slaveConfig->address0            = 0U;
* slaveConfig->address1            = 0U;
* slaveConfig->addressMatchMode   = kLPI2C_MatchAddress0;
* slaveConfig->filterDozeEnable   = true;
* slaveConfig->filterEnable        = true;
* slaveConfig->enableGeneralCall  = false;
* slaveConfig->sclStall.enableAck  = false;
* slaveConfig->sclStall.enableTx   = true;
* slaveConfig->sclStall.enableRx   = true;
* slaveConfig->sclStall.enableAddress = true;
```

```

* slaveConfig->ignoreAck          = false;
* slaveConfig->enableReceivedAddressRead = false;
* slaveConfig->sdaGlitchFilterWidth_ns   = 0;
* slaveConfig->sclGlitchFilterWidth_ns   = 0;
* slaveConfig->dataValidDelay_ns       = 0;
* slaveConfig->clockHoldTime_ns       = 0;
*

```

After calling this function, override any settings to customize the configuration, prior to initializing the master driver with [LPI2C_SlaveInit\(\)](#). Be sure to override at least the *address0* member of the configuration structure with the desired slave address.

Parameters

<i>out</i>	<i>slaveConfig</i>	User provided configuration structure that is set to default values. Refer to lpi2c_slave_config_t .
------------	--------------------	--

22.5.5.2 void LPI2C_SlaveInit (**LPI2C_Type** * *base*, const **lpi2c_slave_config_t** * *slaveConfig*, **uint32_t** *sourceClock_Hz*)

This function enables the peripheral clock and initializes the LPI2C slave peripheral as described by the user provided configuration.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>slaveConfig</i>	User provided peripheral configuration. Use LPI2C_SlaveGetDefaultConfig() to get a set of defaults that you can override.
<i>sourceClock_Hz</i>	Frequency in Hertz of the LPI2C functional clock. Used to calculate the filter widths, data valid delay, and clock hold time.

22.5.5.3 void LPI2C_SlaveDeinit (**LPI2C_Type** * *base*)

This function disables the LPI2C slave peripheral and gates the clock. It also performs a software reset to restore the peripheral to reset conditions.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

22.5.5.4 static void LPI2C_SlaveReset (**LPI2C_Type** * *base*) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

22.5.5.5 static void LPI2C_SlaveEnable (LPI2C_Type * *base*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>enable</i>	Pass true to enable or false to disable the specified LPI2C as slave.

22.5.5.6 static uint32_t LPI2C_SlaveGetStatusFlags (LPI2C_Type * *base*) [inline], [static]

A bit mask with the state of all LPI2C slave status flags is returned. For each flag, the corresponding bit in the return value is set if the flag is asserted.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

State of the status flags:

- 1: related status flag is set.
- 0: related status flag is not set.

See Also

[_lpi2c_slave_flags](#)

22.5.5.7 static void LPI2C_SlaveClearStatusFlags (LPI2C_Type * *base*, uint32_t *statusMask*) [inline], [static]

The following status register flags can be cleared:

- [kLPI2C_SlaveRepeatedStartDetectFlag](#)
- [kLPI2C_SlaveStopDetectFlag](#)
- [kLPI2C_SlaveBitErrFlag](#)
- [kLPI2C_SlaveFifoErrFlag](#)

Attempts to clear other flags has no effect.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>statusMask</i>	A bitmask of status flags that are to be cleared. The mask is composed of _lpi2c_slave_flags enumerators OR'd together. You may pass the result of a previous call to LPI2C_SlaveGetStatusFlags() .

See Also

[_lpi2c_slave_flags](#).

22.5.5.8 static void LPI2C_SlaveEnableInterrupts (LPI2C_Type * *base*, uint32_t *interruptMask*) [inline], [static]

All flags except [kLPI2C_SlaveBusyFlag](#) and [kLPI2C_SlaveBusBusyFlag](#) can be enabled as interrupts.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>interruptMask</i>	Bit mask of interrupts to enable. See _lpi2c_slave_flags for the set of constants that should be OR'd together to form the bit mask.

22.5.5.9 static void LPI2C_SlaveDisableInterrupts (LPI2C_Type * *base*, uint32_t *interruptMask*) [inline], [static]

All flags except [kLPI2C_SlaveBusyFlag](#) and [kLPI2C_SlaveBusBusyFlag](#) can be disabled as interrupts.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>interruptMask</i>	Bit mask of interrupts to disable. See _lpi2c_slave_flags for the set of constants that should be OR'd together to form the bit mask.

22.5.5.10 static uint32_t LPI2C_SlaveGetEnabledInterrupts (LPI2C_Type * *base*) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

A bitmask composed of [_lpi2c_slave_flags](#) enumerators OR'd together to indicate the set of enabled interrupts.

22.5.5.11 static void LPI2C_SlaveEnableDMA (LPI2C_Type * *base*, bool *enableAddressValid*, bool *enableRx*, bool *enableTx*) [inline], [static]

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>enableAddressValid</i>	Enable flag for the address valid DMA request. Pass true for enable, false for disable. The address valid DMA request is shared with the receive data DMA request.
<i>enableRx</i>	Enable flag for the receive data DMA request. Pass true for enable, false for disable.
<i>enableTx</i>	Enable flag for the transmit data DMA request. Pass true for enable, false for disable.

22.5.5.12 static bool LPI2C_SlaveGetBusIdleState (LPI2C_Type * *base*) [inline], [static]

Requires the slave mode to be enabled.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Return values

<i>true</i>	Bus is busy.
<i>false</i>	Bus is idle.

22.5.5.13 static void LPI2C_SlaveTransmitAck (LPI2C_Type * *base*, bool *ackOrNack*) [inline], [static]

Use this function to send an ACK or NAK when the [KLPI2C_SlaveTransmitAckFlag](#) is asserted. This only happens if you enable the sclStall.enableAck field of the [lpi2c_slave_config_t](#) configuration structure used to initialize the slave peripheral.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>ackOrNack</i>	Pass true for an ACK or false for a NAK.

22.5.5.14 static uint32_t LPI2C_SlaveGetReceivedAddress (LPI2C_Type * *base*) [inline], [static]

This function should only be called if the [kLPI2C_SlaveAddressValidFlag](#) is asserted.

Parameters

<i>base</i>	The LPI2C peripheral base address.
-------------	------------------------------------

Returns

The 8-bit address matched by the LPI2C slave. Bit 0 contains the R/w direction bit, and the 7-bit slave address is in the upper 7 bits.

22.5.5.15 status_t LPI2C_SlaveSend (LPI2C_Type * *base*, void * *txBuff*, size_t *txSize*, size_t * *actualTxSize*)

Parameters

	<i>base</i>	The LPI2C peripheral base address.
	<i>txBuff</i>	The pointer to the data to be transferred.
	<i>txSize</i>	The length in bytes of the data to be transferred.
out	<i>actualTxSize</i>	

Returns

Error or success status returned by API.

22.5.5.16 status_t LPI2C_SlaveReceive (LPI2C_Type * *base*, void * *rxBuff*, size_t *rxSize*, size_t * *actualRxSize*)

Parameters

	<i>base</i>	The LPI2C peripheral base address.
	<i>rxBuff</i>	The pointer to the data to be transferred.
	<i>rxSize</i>	The length in bytes of the data to be transferred.
out	<i>actualRxSize</i>	

Returns

Error or success status returned by API.

22.5.5.17 void LPI2C_SlaveTransferCreateHandle (LPI2C_Type * *base*, Ipi2c_slave_handle_t * *handle*, Ipi2c_slave_transfer_callback_t *callback*, void * *userData*)

The creation of a handle is for use with the non-blocking APIs. Once a handle is created, there is not a corresponding destroy handle. If the user wants to terminate a transfer, the [LPI2C_SlaveTransferAbort\(\)](#) API shall be called.

Note

The function also enables the NVIC IRQ for the input LPI2C. Need to notice that on some SoCs the LPI2C IRQ is connected to INTMUX, in this case user needs to enable the associated INTMUX IRQ in application.

Parameters

	<i>base</i>	The LPI2C peripheral base address.
out	<i>handle</i>	Pointer to the LPI2C slave driver handle.
	<i>callback</i>	User provided pointer to the asynchronous callback function.
	<i>userData</i>	User provided pointer to the application callback data.

22.5.5.18 status_t LPI2C_SlaveTransferNonBlocking (LPI2C_Type * *base*, Ipi2c_slave_handle_t * *handle*, uint32_t *eventMask*)

Call this API after calling [I2C_SlaveInit\(\)](#) and [LPI2C_SlaveTransferCreateHandle\(\)](#) to start processing transactions driven by an I2C master. The slave monitors the I2C bus and pass events to the callback that was passed into the call to [LPI2C_SlaveTransferCreateHandle\(\)](#). The callback is always invoked from the interrupt context.

The set of events received by the callback is customizable. To do so, set the *eventMask* parameter to the OR'd combination of [ipi2c_slave_transfer_event_t](#) enumerators for the events you wish to receive. The

`kLPI2C_SlaveTransmitEvent` and `kLPI2C_SlaveReceiveEvent` events are always enabled and do not need to be included in the mask. Alternatively, you can pass 0 to get a default set of only the transmit and receive events that are always enabled. In addition, the `kLPI2C_SlaveAllEvents` constant is provided as a convenient way to enable all events.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to <code>lpi2c_slave_handle_t</code> structure which stores the transfer state.
<i>eventMask</i>	Bit mask formed by OR'ing together <code>lpi2c_slave_transfer_event_t</code> enumerators to specify which events to send to the callback. Other accepted values are 0 to get a default set of only the transmit and receive events, and <code>kLPI2C_SlaveAllEvents</code> to enable all events.

Return values

<code>kStatus_Success</code>	Slave transfers were successfully started.
<code>kStatus_LPI2C_Busy</code>	Slave transfers have already been started on this handle.

22.5.5.19 `status_t LPI2C_SlaveTransferGetCount (LPI2C_Type * base, lpi2c_slave_handle_t * handle, size_t * count)`

Parameters

	<i>base</i>	The LPI2C peripheral base address.
	<i>handle</i>	Pointer to <code>i2c_slave_handle_t</code> structure.
<i>out</i>	<i>count</i>	Pointer to a value to hold the number of bytes transferred. May be NULL if the count is not required.

Return values

<code>kStatus_Success</code>	
<code>kStatus_NoTransferIn-Progress</code>	

22.5.5.20 `void LPI2C_SlaveTransferAbort (LPI2C_Type * base, lpi2c_slave_handle_t * handle)`

Note

This API could be called at any time to stop slave for handling the bus events.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to lpi2c_slave_handle_t structure which stores the transfer state.

Return values

<i>kStatus_Success</i>	
<i>kStatus_LPI2C_Idle</i>	

22.5.5.21 void LPI2C_SlaveTransferHandleIRQ (LPI2C_Type * *base*, lpi2c_slave_handle_t * *handle*)

Note

This function does not need to be called unless you are reimplementing the non blocking API's interrupt handler routines to add special functionality.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to lpi2c_slave_handle_t structure which stores the transfer state.

22.6 LPI2C Master DMA Driver

22.6.1 Overview

Data Structures

- struct `lpi2c_master_edma_handle_t`
Driver handle for master DMA APIs. [More...](#)

Typedefs

- `typedef void(* lpi2c_master_edma_transfer_callback_t)(LPI2C_Type *base, lpi2c_master_edma_handle_t *handle, status_t completionStatus, void *userData)`
Master DMA completion callback function pointer type.

Master DMA

- `void LPI2C_MasterCreateEDMAHandle (LPI2C_Type *base, lpi2c_master_edma_handle_t *handle, edma_handle_t *rxDmaHandle, edma_handle_t *txDmaHandle, lpi2c_master_edma_transfer_callback_t callback, void *userData)`
Create a new handle for the LPI2C master DMA APIs.
- `status_t LPI2C_MasterTransferEDMA (LPI2C_Type *base, lpi2c_master_edma_handle_t *handle, lpi2c_master_transfer_t *transfer)`
Performs a non-blocking DMA-based transaction on the I2C bus.
- `status_t LPI2C_MasterTransferGetCountEDMA (LPI2C_Type *base, lpi2c_master_edma_handle_t *handle, size_t *count)`
Returns number of bytes transferred so far.
- `status_t LPI2C_MasterTransferAbortEDMA (LPI2C_Type *base, lpi2c_master_edma_handle_t *handle)`
Terminates a non-blocking LPI2C master transmission early.

22.6.2 Data Structure Documentation

22.6.2.1 struct _lpi2c_master_edma_handle

Note

The contents of this structure are private and subject to change.

Data Fields

- `LPI2C_Type * base`
LPI2C base pointer.
- `bool isBusy`

- *Transfer state machine current state.*
- `uint8_t nbytes`
eDMA minor byte transfer count initially configured.
- `uint16_t commandBuffer[10]`
LPI2C command sequence.
- `lpi2c_master_transfer_t transfer`
Copy of the current transfer info.
- `lpi2c_master_edma_transfer_callback_t completionCallback`
Callback function pointer.
- `void *userData`
Application data passed to callback.
- `edma_handle_t *rx`
Handle for receive DMA channel.
- `edma_handle_t *tx`
Handle for transmit DMA channel.
- `edma_tcd_t tcds[3]`
Software TCD.

Field Documentation

- (1) `LPI2C_Type* lpi2c_master_edma_handle_t::base`
- (2) `bool lpi2c_master_edma_handle_t::isBusy`
- (3) `uint8_t lpi2c_master_edma_handle_t::nbytes`
- (4) `uint16_t lpi2c_master_edma_handle_t::commandBuffer[10]`

When all 10 command words are used: Start&addr&write[1 word] + subaddr[4 words] + restart&addr&read[1 word] + receive&Size[4 words]

- (5) `lpi2c_master_transfer_t lpi2c_master_edma_handle_t::transfer`
- (6) `lpi2c_master_edma_transfer_callback_t lpi2c_master_edma_handle_t::completionCallback`
- (7) `void* lpi2c_master_edma_handle_t::userData`
- (8) `edma_handle_t* lpi2c_master_edma_handle_t::rx`
- (9) `edma_handle_t* lpi2c_master_edma_handle_t::tx`
- (10) `edma_tcd_t lpi2c_master_edma_handle_t::tcds[3]`

Three are allocated to provide enough room to align to 32-bytes.

22.6.3 Typedef Documentation

**22.6.3.1 `typedef void(* Ipi2c_master_edma_transfer_callback_t)(LPI2C_Type *base,
Ipi2c_master_edma_handle_t *handle, status_t completionStatus, void
*userData)`**

This callback is used only for the non-blocking master transfer API. Specify the callback you wish to use in the call to [LPI2C_MasterCreateEDMAHandle\(\)](#).

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Handle associated with the completed transfer.
<i>completion-Status</i>	Either kStatus_Success or an error code describing how the transfer completed.
<i>userData</i>	Arbitrary pointer-sized value passed from the application.

22.6.4 Function Documentation

22.6.4.1 void LPI2C_MasterCreateEDMAHandle (LPI2C_Type * *base*, Ipi2c_master_edma_handle_t * *handle*, edma_handle_t * *rxDmaHandle*, edma_handle_t * *txDmaHandle*, Ipi2c_master_edma_transfer_callback_t *callback*, void * *userData*)

The creation of a handle is for use with the DMA APIs. Once a handle is created, there is not a corresponding destroy handle. If the user wants to terminate a transfer, the [LPI2C_MasterTransferAbort-EDMA\(\)](#) API shall be called.

For devices where the LPI2C send and receive DMA requests are OR'd together, the *txDmaHandle* parameter is ignored and may be set to NULL.

Parameters

	<i>base</i>	The LPI2C peripheral base address.
out	<i>handle</i>	Pointer to the LPI2C master driver handle.
	<i>rxDmaHandle</i>	Handle for the eDMA receive channel. Created by the user prior to calling this function.
	<i>txDmaHandle</i>	Handle for the eDMA transmit channel. Created by the user prior to calling this function.
	<i>callback</i>	User provided pointer to the asynchronous callback function.
	<i>userData</i>	User provided pointer to the application callback data.

22.6.4.2 status_t LPI2C_MasterTransferEDMA (LPI2C_Type * *base*, Ipi2c_master_edma_handle_t * *handle*, Ipi2c_master_transfer_t * *transfer*)

The callback specified when the *handle* was created is invoked when the transaction has completed.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to the LPI2C master driver handle.
<i>transfer</i>	The pointer to the transfer descriptor.

Return values

<i>kStatus_Success</i>	The transaction was started successfully.
<i>kStatus_LPI2C_Busy</i>	Either another master is currently utilizing the bus, or another DMA transaction is already in progress.

22.6.4.3 status_t LPI2C_MasterTransferGetCountEDMA (**LPI2C_Type * base,** *lpi2c_master_edma_handle_t * handle, size_t * count*)

Parameters

	<i>base</i>	The LPI2C peripheral base address.
	<i>handle</i>	Pointer to the LPI2C master driver handle.
<i>out</i>	<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Return values

<i>kStatus_Success</i>	
<i>kStatus_NoTransferInProgress</i>	There is not a DMA transaction currently in progress.

22.6.4.4 status_t LPI2C_MasterTransferAbortEDMA (**LPI2C_Type * base,** *lpi2c_master_edma_handle_t * handle*)

Note

It is not safe to call this function from an IRQ handler that has a higher priority than the eDMA peripheral's IRQ priority.

Parameters

<i>base</i>	The LPI2C peripheral base address.
<i>handle</i>	Pointer to the LPI2C master driver handle.

Return values

<i>kStatus_Success</i>	A transaction was successfully aborted.
<i>kStatus_LPI2C_Idle</i>	There is not a DMA transaction currently in progress.

22.7 LPI2C FreeRTOS Driver

22.7.1 Overview

Driver version

- #define **FSL_LPI2C_FREERTOS_DRIVER_VERSION** (MAKE_VERSION(2, 3, 0))
LPI2C FreeRTOS driver version.

LPI2C RTOS Operation

- **status_t LPI2C_RRTOS_Init** (lpi2c_rtos_handle_t *handle, LPI2C_Type *base, const lpi2c_master_config_t *masterConfig, uint32_t srcClock_Hz)
Initializes LPI2C.
- **status_t LPI2C_RRTOS_Deinit** (lpi2c_rtos_handle_t *handle)
Deinitializes the LPI2C.
- **status_t LPI2C_RRTOS_Transfer** (lpi2c_rtos_handle_t *handle, lpi2c_master_transfer_t *transfer)
Performs I2C transfer.

22.7.2 Macro Definition Documentation

22.7.2.1 #define FSL_LPI2C_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 3, 0))

22.7.3 Function Documentation

22.7.3.1 **status_t LPI2C_RRTOS_Init (lpi2c_rtos_handle_t * handle, LPI2C_Type * base, const lpi2c_master_config_t * masterConfig, uint32_t srcClock_Hz)**

This function initializes the LPI2C module and related RTOS context.

Parameters

<i>handle</i>	The RTOS LPI2C handle, the pointer to an allocated space for RTOS context.
<i>base</i>	The pointer base address of the LPI2C instance to initialize.
<i>masterConfig</i>	Configuration structure to set-up LPI2C in master mode.
<i>srcClock_Hz</i>	Frequency of input clock of the LPI2C module.

Returns

status of the operation.

22.7.3.2 status_t LPI2C_RTOS_Deinit (*lpi2c_rtos_handle_t * handle*)

This function deinitializes the LPI2C module and related RTOS context.

Parameters

<i>handle</i>	The RTOS LPI2C handle.
---------------	------------------------

22.7.3.3 status_t LPI2C_RTOS_Transfer (*lpi2c_rtos_handle_t * handle,* *lpi2c_master_transfer_t * transfer*)

This function performs an I2C transfer using LPI2C module according to data given in the transfer structure.

Parameters

<i>handle</i>	The RTOS LPI2C handle.
<i>transfer</i>	Structure specifying the transfer parameters.

Returns

status of the operation.

22.8 LPI2C CMSIS Driver

This section describes the programming interface of the LPI2C Cortex Microcontroller Software Interface Standard (CMSIS) driver. And this driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method see <http://www.keil.com/pack/doc/cmsis/Driver/html/index.html>.

The LPI2C CMSIS driver includes transactional APIs.

Transactional APIs are transaction target high-level APIs. The transactional APIs can be used to enable the peripheral quickly and also in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are critical requirements, see the transactional API implementation and write custom code accessing the hardware registers.

22.8.1 LPI2C CMSIS Driver

22.8.1.1 Master Operation in interrupt transactional method

```
void I2C_MasterSignalEvent_t(uint32_t event)
{
    if (event == ARM_I2C_EVENT_TRANSFER_DONE)
    {
        g_MasterCompletionFlag = true;
    }
}
/*Init I2C0*/
Driver_I2C0.Initialize(I2C_MasterSignalEvent_t);

Driver_I2C0.PowerControl(ARM_POWER_FULL);

/*config transmit speed/
Driver_I2C0.Control(ARM_I2C_BUS_SPEED, ARM_I2C_BUS_SPEED_STANDARD);

/*start transmit*/
Driver_I2C0.MasterTransmit(I2C_MASTER_SLAVE_ADDR, g_master_buff, I2C_DATA_LENGTH, false);

/* Wait for transfer completed. */
while (!g_MasterCompletionFlag)
{
}
g_MasterCompletionFlag = false;
```

22.8.1.2 Master Operation in DMA transactional method

```
void I2C_MasterSignalEvent_t(uint32_t event)
{
    /* Transfer done */
    if (event == ARM_I2C_EVENT_TRANSFER_DONE)
    {
        g_MasterCompletionFlag = true;
    }
}

/* DMAMux init and EDMA init. */
DMAMUX_Init(EXAMPLE_LPI2C_DMAMUX_BASEADDR);
```

```

edma_config_t edmaConfig;
EDMA_GetDefaultConfig(&edmaConfig);
EDMA_Init(EXAMPLE_LPI2C_DMA_BASEADDR, &edmaConfig);

/*Init I2C0*/
Driver_I2C0.Initialize(I2C_MasterSignalEvent_t);

Driver_I2C0.PowerControl(ARM_POWER_FULL);

/*config transmit speed*/
Driver_I2C0.Control(ARM_I2C_BUS_SPEED, ARM_I2C_BUS_SPEED_STANDARD);

/*start transfer*/
Driver_I2C0.MasterReceive(I2C_MASTER_SLAVE_ADDR, g_master_buff, I2C_DATA_LENGTH, false);

/* Wait for transfer completed. */
while (!g_MasterCompletionFlag)
{
}
g_MasterCompletionFlag = false;

```

22.8.1.3 Slave Operation in interrupt transactional method

```

void I2C_SlaveSignalEvent_t(uint32_t event)
{
    /* Transfer done */
    if (event == ARM_I2C_EVENT_TRANSFER_DONE)
    {
        g_SlaveCompletionFlag = true;
    }
}

/*Init I2C1*/
Driver_I2C1.Initialize(I2C_SlaveSignalEvent_t);

Driver_I2C1.PowerControl(ARM_POWER_FULL);

/*config slave addr*/
Driver_I2C1.Control(ARM_I2C_OWN_ADDRESS, I2C_MASTER_SLAVE_ADDR);

/*start transfer*/
Driver_I2C1.SlaveReceive(g_slave_buff, I2C_DATA_LENGTH);

/* Wait for transfer completed. */
while (!g_SlaveCompletionFlag)
{
}
g_SlaveCompletionFlag = false;

```

Chapter 23

LPIT: Low-Power Interrupt Timer

23.1 Overview

The MCUXpresso SDK provides a driver for the Low-Power Interrupt Timer (LPIT) of MCUXpresso SDK devices.

23.2 Function groups

The LPIT driver supports operating the module as a time counter.

23.2.1 Initialization and deinitialization

The function [LPIT_Init\(\)](#) initializes the LPIT with specified configurations. The function [LPIT_GetDefaultConfig\(\)](#) gets the default configurations. The initialization function configures the LPIT operation in doze mode and debug mode.

The function [LPIT_SetupChannel\(\)](#) configures the operation of each LPIT channel.

The function [LPIT_Deinit\(\)](#) disables the LPIT module and disables the module clock.

23.2.2 Timer period Operations

The function [LPITR_SetTimerPeriod\(\)](#) sets the timer period in units of count. Timers begin counting down from the value set by this function until it reaches 0.

The function [LPIT_GetCurrentTimerCount\(\)](#) reads the current timer counting value. This function returns the real-time timer counting value, in a range from 0 to a timer period.

The timer period operation functions takes the count value in ticks. User can call the utility macros provided in `fsl_common.h` to convert to microseconds or milliseconds

23.2.3 Start and Stop timer operations

The function [LPIT_StartTimer\(\)](#) starts the timer counting. After calling this function, the timer loads the period value set earlier via the [LPIT_SetPeriod\(\)](#) function and starts counting down to 0. When the timer reaches 0, it generates a trigger pulse and sets the timeout interrupt flag.

The function [LPIT_StopTimer\(\)](#) stops the timer counting.

23.2.4 Status

Provides functions to get and clear the LPIT status.

23.2.5 Interrupt

Provides functions to enable/disable LPIT interrupts and get current enabled interrupts.

23.3 Typical use case

23.3.1 LPIT tick example

Updates the LPIT period and toggles an LED periodically. Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/lpit

Data Structures

- struct [lpit_chnl_params_t](#)
Structure to configure the channel timer. [More...](#)
- struct [lpit_config_t](#)
LPIT configuration structure. [More...](#)

Functions

- static void [LPIT_Reset](#) (LPIT_Type *base)
Performs a software reset on the LPIT module.

Driver version

- enum [lpit_chnl_t](#) {
 kLPIT_Chnl_0 = 0U,
 kLPIT_Chnl_1,
 kLPIT_Chnl_2,
 kLPIT_Chnl_3 }
List of LPIT channels.
- enum [lpit_timer_modes_t](#) {
 kLPIT_PeriodicCounter = 0U,
 kLPIT_DualPeriodicCounter,
 kLPIT_TriggerAccumulator,
 kLPIT_InputCapture }
Mode options available for the LPIT timer.
- enum [lpit_trigger_select_t](#) {

```
kLPIT_Trigger_TimerChn0 = 0U,
kLPIT_Trigger_TimerChn1,
kLPIT_Trigger_TimerChn2,
kLPIT_Trigger_TimerChn3,
kLPIT_Trigger_TimerChn4,
kLPIT_Trigger_TimerChn5,
kLPIT_Trigger_TimerChn6,
kLPIT_Trigger_TimerChn7,
kLPIT_Trigger_TimerChn8,
kLPIT_Trigger_TimerChn9,
kLPIT_Trigger_TimerChn10,
kLPIT_Trigger_TimerChn11,
kLPIT_Trigger_TimerChn12,
kLPIT_Trigger_TimerChn13,
kLPIT_Trigger_TimerChn14,
kLPIT_Trigger_TimerChn15 }
```

Trigger options available.

- enum `lpit_trigger_source_t` {

kLPIT_TriggerSource_External = 0U,

kLPIT_TriggerSource_Internal }

Trigger source options available.

- enum `lpit_interrupt_enable_t` {

kLPIT_Channel0TimerInterruptEnable = (1U << 0),

kLPIT_Channel1TimerInterruptEnable = (1U << 1),

kLPIT_Channel2TimerInterruptEnable = (1U << 2),

kLPIT_Channel3TimerInterruptEnable = (1U << 3) }

List of LPIT interrupts.

- enum `lpit_status_flags_t` {

kLPIT_Channel0TimerFlag = (1U << 0),

kLPIT_Channel1TimerFlag = (1U << 1),

kLPIT_Channel2TimerFlag = (1U << 2),

kLPIT_Channel3TimerFlag = (1U << 3) }

List of LPIT status flags.

- #define `FSL_LPIT_DRIVER_VERSION` (MAKE_VERSION(2, 0, 2))

Version 2.0.2.

Initialization and deinitialization

- void `LPIT_Init` (LPIT_Type *base, const `lpit_config_t` *config)

Ungates the LPIT clock and configures the peripheral for a basic operation.
- void `LPIT_Deinit` (LPIT_Type *base)

Disables the module and gates the LPIT clock.
- void `LPIT_GetDefaultConfig` (`lpit_config_t` *config)

Fills in the LPIT configuration structure with default settings.
- `status_t LPIT_SetupChannel` (LPIT_Type *base, `lpit_chnl_t` channel, const `lpit_chnl_params_t` *chnlSetup)

Sets up an LPIT channel based on the user's preference.

Interrupt Interface

- static void [LPIT_EnableInterrupts](#) (LPIT_Type *base, uint32_t mask)
Enables the selected PIT interrupts.
- static void [LPIT_DisableInterrupts](#) (LPIT_Type *base, uint32_t mask)
Disables the selected PIT interrupts.
- static uint32_t [LPIT_GetEnabledInterrupts](#) (LPIT_Type *base)
Gets the enabled LPIT interrupts.

Status Interface

- static uint32_t [LPIT_GetStatusFlags](#) (LPIT_Type *base)
Gets the LPIT status flags.
- static void [LPIT_ClearStatusFlags](#) (LPIT_Type *base, uint32_t mask)
Clears the LPIT status flags.

Read and Write the timer period

- static void [LPIT_SetTimerPeriod](#) (LPIT_Type *base, lpit_chnl_t channel, uint32_t ticks)
Sets the timer period in units of count.
- static uint32_t [LPIT_GetCurrentTimerCount](#) (LPIT_Type *base, lpit_chnl_t channel)
Reads the current timer counting value.

Timer Start and Stop

- static void [LPIT_StartTimer](#) (LPIT_Type *base, lpit_chnl_t channel)
Starts the timer counting.
- static void [LPIT_StopTimer](#) (LPIT_Type *base, lpit_chnl_t channel)
Stops the timer counting.

23.4 Data Structure Documentation

23.4.1 struct lpit_chnl_params_t

Data Fields

- bool [chainChannel](#)
true: Timer chained to previous timer; false: Timer not chained
- [lpit_timer_modes_t timerMode](#)
Timers mode of operation.
- [lpit_trigger_select_t triggerSelect](#)
Trigger selection for the timer.
- [lpit_trigger_source_t triggerSource](#)
Decides if we use external or internal trigger.
- bool [enableReloadOnTrigger](#)
true: Timer reloads when a trigger is detected; false: No effect
- bool [enableStopOnTimeout](#)
true: Timer will stop after timeout; false: does not stop after timeout
- bool [enableStartOnTrigger](#)
true: Timer starts when a trigger is detected; false: decrement immediately

Field Documentation

- (1) `lpit_timer_modes_t lpit_chnl_params_t::timerMode`
- (2) `lpit_trigger_source_t lpit_chnl_params_t::triggerSource`

23.4.2 struct lpit_config_t

This structure holds the configuration settings for the LPIT peripheral. To initialize this structure to reasonable defaults, call the `LPIT_GetDefaultConfig()` function and pass a pointer to the configuration structure instance.

The configuration structure can be made constant so as to reside in flash.

Data Fields

- bool `enableRunInDebug`
true: Timers run in debug mode; false: Timers stop in debug mode
- bool `enableRunInDoze`
true: Timers run in doze mode; false: Timers stop in doze mode

23.5 Enumeration Type Documentation**23.5.1 enum lpit_chnl_t**

Note

Actual number of available channels is SoC-dependent

Enumerator

- `kLPIT_Chnl_0` LPIT channel number 0.
- `kLPIT_Chnl_1` LPIT channel number 1.
- `kLPIT_Chnl_2` LPIT channel number 2.
- `kLPIT_Chnl_3` LPIT channel number 3.

23.5.2 enum lpit_timer_modes_t

Enumerator

- `kLPIT_PeriodicCounter` Use the all 32-bits, counter loads and decrements to zero.
- `kLPIT_DualPeriodicCounter` Counter loads, lower 16-bits decrement to zero, then upper 16-bits decrement.
- `kLPIT_TriggerAccumulator` Counter loads on first trigger and decrements on each trigger.
- `kLPIT_InputCapture` Counter loads with 0xFFFFFFFF, decrements to zero. It stores the inverse of the current value when a input trigger is detected

23.5.3 enum lpit_trigger_select_t

This is used for both internal and external trigger sources. The actual trigger options available is SoC-specific, user should refer to the reference manual.

Enumerator

<i>kLPIT_Trigger_TimerChn0</i>	Channel 0 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn1</i>	Channel 1 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn2</i>	Channel 2 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn3</i>	Channel 3 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn4</i>	Channel 4 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn5</i>	Channel 5 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn6</i>	Channel 6 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn7</i>	Channel 7 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn8</i>	Channel 8 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn9</i>	Channel 9 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn10</i>	Channel 10 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn11</i>	Channel 11 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn12</i>	Channel 12 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn13</i>	Channel 13 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn14</i>	Channel 14 is selected as a trigger source.
<i>kLPIT_Trigger_TimerChn15</i>	Channel 15 is selected as a trigger source.

23.5.4 enum lpit_trigger_source_t

Enumerator

<i>kLPIT_TriggerSource_External</i>	Use external trigger input.
<i>kLPIT_TriggerSource_Internal</i>	Use internal trigger.

23.5.5 enum lpit_interrupt_enable_t

Note

Number of timer channels are SoC-specific. See the SoC Reference Manual.

Enumerator

<i>kLPIT_Channel0TimerInterruptEnable</i>	Channel 0 Timer interrupt.
<i>kLPIT_Channel1TimerInterruptEnable</i>	Channel 1 Timer interrupt.
<i>kLPIT_Channel2TimerInterruptEnable</i>	Channel 2 Timer interrupt.
<i>kLPIT_Channel3TimerInterruptEnable</i>	Channel 3 Timer interrupt.

23.5.6 enum lpit_status_flags_t

Note

Number of timer channels are SoC-specific. See the SoC Reference Manual.

Enumerator

<i>kLPIT_Channel0TimerFlag</i>	Channel 0 Timer interrupt flag.
<i>kLPIT_Channel1TimerFlag</i>	Channel 1 Timer interrupt flag.
<i>kLPIT_Channel2TimerFlag</i>	Channel 2 Timer interrupt flag.
<i>kLPIT_Channel3TimerFlag</i>	Channel 3 Timer interrupt flag.

23.6 Function Documentation

23.6.1 void LPIT_Init (LPIT_Type * *base*, const lpit_config_t * *config*)

This function issues a software reset to reset all channels and registers except the Module Control register.

Note

This API should be called at the beginning of the application using the LPIT driver.

Parameters

<i>base</i>	LPIT peripheral base address.
<i>config</i>	Pointer to the user configuration structure.

23.6.2 void LPIT_Deinit (LPIT_Type * *base*)

Parameters

<i>base</i>	LPIT peripheral base address.
-------------	-------------------------------

23.6.3 void LPIT_GetDefaultConfig (lpit_config_t * *config*)

The default values are:

```
*     config->enableRunInDebug = false;
*     config->enableRunInDoze = false;
*
```

Parameters

<i>config</i>	Pointer to the user configuration structure.
---------------	--

23.6.4 **status_t LPIT_SetupChannel (LPIT_Type * *base*, lpit_chnl_t *channel*, const lpit_chnl_params_t * *chnlSetup*)**

This function sets up the operation mode to one of the options available in the enumeration [lpit_timer_modes_t](#). It sets the trigger source as either internal or external, trigger selection and the timers behaviour when a timeout occurs. It also chains the timer if a prior timer if requested by the user.

Parameters

<i>base</i>	LPIT peripheral base address.
<i>channel</i>	Channel that is being configured.
<i>chnlSetup</i>	Configuration parameters.

23.6.5 **static void LPIT_EnableInterrupts (LPIT_Type * *base*, uint32_t *mask*) [inline], [static]**

Parameters

<i>base</i>	LPIT peripheral base address.
<i>mask</i>	The interrupts to enable. This is a logical OR of members of the enumeration lpit_interrupt_enable_t

23.6.6 **static void LPIT_DisableInterrupts (LPIT_Type * *base*, uint32_t *mask*) [inline], [static]**

Parameters

<i>base</i>	LPIT peripheral base address.
<i>mask</i>	The interrupts to enable. This is a logical OR of members of the enumeration lpit_interrupt_enable_t

23.6.7 **static uint32_t LPIT_GetEnabledInterrupts (LPIT_Type * *base*)**
[**inline**], [**static**]

Parameters

<i>base</i>	LPIT peripheral base address.
-------------	-------------------------------

Returns

The enabled interrupts. This is the logical OR of members of the enumeration [lpit_interrupt_enable_t](#)

23.6.8 static uint32_t LPIT_GetStatusFlags (LPIT_Type * *base*) [inline], [static]

Parameters

<i>base</i>	LPIT peripheral base address.
-------------	-------------------------------

Returns

The status flags. This is the logical OR of members of the enumeration [lpit_status_flags_t](#)

23.6.9 static void LPIT_ClearStatusFlags (LPIT_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	LPIT peripheral base address.
<i>mask</i>	The status flags to clear. This is a logical OR of members of the enumeration lpit_status_flags_t

23.6.10 static void LPIT_SetTimerPeriod (LPIT_Type * *base*, lpit_chnl_t *channel*, uint32_t *ticks*) [inline], [static]

Timers begin counting down from the value set by this function until it reaches 0, at which point it generates an interrupt and loads this register value again. Writing a new value to this register does not restart the timer. Instead, the value is loaded after the timer expires.

Note

User can call the utility macros provided in `fsl_common.h` to convert to ticks.

Parameters

<i>base</i>	LPIT peripheral base address.
<i>channel</i>	Timer channel number.
<i>ticks</i>	Timer period in units of ticks.

23.6.11 static uint32_t LPIT_GetCurrentTimerCount (LPIT_Type * *base*, lpit_chnl_t *channel*) [inline], [static]

This function returns the real-time timer counting value, in a range from 0 to a timer period.

Note

User can call the utility macros provided in fsl_common.h to convert ticks to microseconds or milliseconds.

Parameters

<i>base</i>	LPIT peripheral base address.
<i>channel</i>	Timer channel number.

Returns

Current timer counting value in ticks.

23.6.12 static void LPIT_StartTimer (LPIT_Type * *base*, lpit_chnl_t *channel*) [inline], [static]

After calling this function, timers load the period value and count down to 0. When the timer reaches 0, it generates a trigger pulse and sets the timeout interrupt flag.

Parameters

<i>base</i>	LPIT peripheral base address.
<i>channel</i>	Timer channel number.

23.6.13 static void LPIT_StopTimer (LPIT_Type * *base*, lpit_chnl_t *channel*) [inline], [static]

Parameters

<i>base</i>	LPIT peripheral base address.
<i>channel</i>	Timer channel number.

23.6.14 static void LPIT_Reset(LPIT_Type * *base*) [inline], [static]

This resets all channels and registers except the Module Control Register.

Parameters

<i>base</i>	LPIT peripheral base address.
-------------	-------------------------------

Chapter 24

LPSPI: Low Power Serial Peripheral Interface

24.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Low Power Serial Peripheral Interface (LPSPI) module of MCUXpresso SDK devices.

Modules

- [LPSPI Peripheral driver](#)

24.2 LPSPI Peripheral driver

24.2.1 Overview

This section describes the programming interface of the LPSPI Peripheral driver. The LPSPI driver configures LPSPI module, provides the functional and transactional interfaces to build the LPSPI application.

24.2.2 Function groups

24.2.2.1 LPSPI Initialization and De-initialization

This function group initializes the default configuration structure for master and slave, initializes the LPSPI master with a master configuration, initializes the LPSPI slave with a slave configuration, and de-initializes the LPSPI module.

24.2.2.2 LPSPI Basic Operation

This function group enables/disables the LPSPI module both interrupt and DMA, gets the data register address for the DMA transfer, sets master and slave, starts and stops the transfer, and so on.

24.2.2.3 LPSPI Transfer Operation

This function group controls the transfer, master send/receive data, and slave send/receive data.

24.2.2.4 LPSPI Status Operation

This function group gets/clears the LPSPI status.

24.2.2.5 LPSPI Block Transfer Operation

This function group transfers a block of data, gets the transfer status, and aborts the transfer.

24.2.3 Typical use case

24.2.3.1 Master Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/lpspi

24.2.3.2 Slave Operation

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/lpspi

Data Structures

- struct `lpspi_master_config_t`
LPSPI master configuration structure. [More...](#)
- struct `lpspi_slave_config_t`
LPSPI slave configuration structure. [More...](#)
- struct `lpspi_transfer_t`
LPSPI master/slave transfer structure. [More...](#)
- struct `lpspi_master_handle_t`
LPSPI master transfer handle structure used for transactional API. [More...](#)
- struct `lpspi_slave_handle_t`
LPSPI slave transfer handle structure used for transactional API. [More...](#)

Macros

- #define `LPSPI_DUMMY_DATA` (0x00U)
LPSPI dummy data if no Tx data.
- #define `SPI_RETRY_TIMES` 0U /* Define to zero means keep waiting until the flag is assert/deassert. */
Retry times for waiting flag.
- #define `LPSPI_MASTER_PCS_SHIFT` (4U)
LPSPI master PCS shift macro , internal used.
- #define `LPSPI_MASTER_PCS_MASK` (0xF0U)
LPSPI master PCS shift macro , internal used.
- #define `LPSPI_SLAVE_PCS_SHIFT` (4U)
LPSPI slave PCS shift macro , internal used.
- #define `LPSPI_SLAVE_PCS_MASK` (0xF0U)
LPSPI slave PCS shift macro , internal used.

Typedefs

- typedef void(* `lpspi_master_transfer_callback_t`)(LPSPI_Type *base, lpspi_master_handle_t *handle, `status_t` status, void *userData)
Master completion callback function pointer type.
- typedef void(* `lpspi_slave_transfer_callback_t`)(LPSPI_Type *base, lpspi_slave_handle_t *handle, `status_t` status, void *userData)
Slave completion callback function pointer type.

Enumerations

- enum {

kStatus_LPSPI_Busy = MAKE_STATUS(kStatusGroup_LPSPI, 0),

kStatus_LPSPI_Error = MAKE_STATUS(kStatusGroup_LPSPI, 1),

kStatus_LPSPI_Idle = MAKE_STATUS(kStatusGroup_LPSPI, 2),

kStatus_LPSPI_OutOfRange = MAKE_STATUS(kStatusGroup_LPSPI, 3),

kStatus_LPSPI_Timeout = MAKE_STATUS(kStatusGroup_LPSPI, 4) }

Status for the LPSPI driver.
 - enum _lpspi_flags {

kLPSPI_TxDataRequestFlag = LPSPI_SR_TDF_MASK,

kLPSPI_RxDataReadyFlag = LPSPI_SR_RDF_MASK,

kLPSPI_WordCompleteFlag = LPSPI_SR_WCF_MASK,

kLPSPI_FrameCompleteFlag = LPSPI_SR_FCF_MASK,

kLPSPI_TransferCompleteFlag = LPSPI_SR_TCF_MASK,

kLPSPI_TransmitErrorFlag = LPSPI_SR_TEF_MASK,

kLPSPI_ReceiveErrorFlag = LPSPI_SR_REF_MASK,

kLPSPI_DataMatchFlag = LPSPI_SR_DMF_MASK,

kLPSPI_ModuleBusyFlag = LPSPI_SR_MBFI_MASK,

kLPSPI_AllStatusFlag }

LPSPI status flags in SPIx_SR register.
 - enum _lpspi_interrupt_enable {

kLPSPI_TxInterruptEnable = LPSPI_IER_TDIE_MASK,

kLPSPI_RxInterruptEnable = LPSPI_IER_RDIE_MASK,

kLPSPI_WordCompleteInterruptEnable = LPSPI_IER_WCIE_MASK,

kLPSPI_FrameCompleteInterruptEnable = LPSPI_IER_FCIE_MASK,

kLPSPI_TransferCompleteInterruptEnable = LPSPI_IER_TCIE_MASK,

kLPSPI_TransmitErrorInterruptEnable = LPSPI_IER_TEIE_MASK,

kLPSPI_ReceiveErrorInterruptEnable = LPSPI_IER_REIE_MASK,

kLPSPI_DataMatchInterruptEnable = LPSPI_IER_DMIE_MASK,

kLPSPI_AllInterruptEnable }

LPSPI interrupt source.
 - enum _lpspi_dma_enable {

kLPSPI_TxDmaEnable = LPSPI_DER_TDDE_MASK,

kLPSPI_RxDmaEnable = LPSPI_DER_RDDE_MASK }
 - enum lpspi_master_slave_mode_t {

kLPSPI_Master = 1U,

kLPSPI_Slave = 0U }
 - enum lpspi_which_pcs_t {

kLPSPI_Pcs0 = 0U,

kLPSPI_Pcs1 = 1U,

kLPSPI_Pcs2 = 2U,

kLPSPI_Pcs3 = 3U }
- LPSPI Peripheral Chip Select (PCS) configuration (which PCS to configure).*

- enum `lpspi_pcs_polarity_config_t` {

 `kLPSPI_PcsActiveHigh` = 1U,

 `kLPSPI_PcsActiveLow` = 0U }

LPSPI Peripheral Chip Select (PCS) Polarity configuration.

- enum `_lpspi_pcs_polarity` {

 `kLPSPI_Pcs0ActiveLow` = 1U << 0,

 `kLPSPI_Pcs1ActiveLow` = 1U << 1,

 `kLPSPI_Pcs2ActiveLow` = 1U << 2,

 `kLPSPI_Pcs3ActiveLow` = 1U << 3,

 `kLPSPI_PcsAllActiveLow` = 0xFU }

LPSPI Peripheral Chip Select (PCS) Polarity.

- enum `lpspi_clock_polarity_t` {

 `kLPSPI_ClockPolarityActiveHigh` = 0U,

 `kLPSPI_ClockPolarityActiveLow` = 1U }

LPSPI clock polarity configuration.

- enum `lpspi_clock_phase_t` {

 `kLPSPI_ClockPhaseFirstEdge` = 0U,

 `kLPSPI_ClockPhaseSecondEdge` = 1U }

LPSPI clock phase configuration.

- enum `lpspi_shift_direction_t` {

 `kLPSPI_MsbFirst` = 0U,

 `kLPSPI_LsbFirst` = 1U }

LPSPI data shifter direction options.

- enum `lpspi_host_request_select_t` {

 `kLPSPI_HostReqExtPin` = 0U,

 `kLPSPI_HostReqInternalTrigger` = 1U }

LPSPI Host Request select configuration.

- enum `lpspi_match_config_t` {

 `kLPSI_MatchDisabled` = 0x0U,

 `kLPSI_1stWordEqualsM0orM1` = 0x2U,

 `kLPSI_AnyWordEqualsM0orM1` = 0x3U,

 `kLPSI_1stWordEqualsM0and2ndWordEqualsM1` = 0x4U,

 `kLPSI_AnyWordEqualsM0andNxtWordEqualsM1` = 0x5U,

 `kLPSI_1stWordAndM1EqualsM0andM1` = 0x6U,

 `kLPSI_AnyWordAndM1EqualsM0andM1` = 0x7U }

LPSPI Match configuration options.

- enum `lpspi_pin_config_t` {

 `kLPSPI_SdiInSdoOut` = 0U,

 `kLPSPI_SdiInSdiOut` = 1U,

 `kLPSPI_SdoInSdoOut` = 2U,

 `kLPSPI_SdoInSdiOut` = 3U }

LPSPI pin (SDO and SDI) configuration.

- enum `lpspi_data_out_config_t` {

 `kLpspiDataOutRetained` = 0U,

 `kLpspiDataOutTristate` = 1U }

LPSPI data output configuration.

- enum `lpspi_transfer_width_t` {

- ```

kLPSPI_SingleBitXfer = 0U,
kLPSPI_TwoBitXfer = 1U,
kLPSPI_FourBitXfer = 2U }
 LPSPI transfer width configuration.
• enum lpspi_delay_type_t {
 kLPSPI_PcsToSck = 1U,
 kLPSPI_LastSckToPcs,
 kLPSPI_BetweenTransfer }

 LPSPI delay type selection.
• enum _lpspi_transfer_config_flag_for_master {
 kLPSPI_MasterPcs0 = 0U << LPSPI_MASTER_PCS_SHIFT,
 kLPSPI_MasterPcs1 = 1U << LPSPI_MASTER_PCS_SHIFT,
 kLPSPI_MasterPcs2 = 2U << LPSPI_MASTER_PCS_SHIFT,
 kLPSPI_MasterPcs3 = 3U << LPSPI_MASTER_PCS_SHIFT,
 kLPSPI_MasterPcsContinuous = 1U << 20,
 kLPSPI_MasterByteSwap }

 Use this enumeration for LPSPI master transfer configFlags.
• enum _lpspi_transfer_config_flag_for_slave {
 kLPSPI_SlavePcs0 = 0U << LPSPI_SLAVE_PCS_SHIFT,
 kLPSPI_SlavePcs1 = 1U << LPSPI_SLAVE_PCS_SHIFT,
 kLPSPI_SlavePcs2 = 2U << LPSPI_SLAVE_PCS_SHIFT,
 kLPSPI_SlavePcs3 = 3U << LPSPI_SLAVE_PCS_SHIFT,
 kLPSPI_SlaveByteSwap }

 Use this enumeration for LPSPI slave transfer configFlags.
• enum _lpspi_transfer_state {
 kLPSPI_Idle = 0x0U,
 kLPSPI_Busy,
 kLPSPI_Error }

 LPSPI transfer state, which is used for LPSPI transactional API state machine.

```

## Variables

- volatile uint8\_t [g\\_lpspiDummyData](#) []
 *Global variable for dummy data value setting.*

## Driver version

- #define [FSL\\_LPSPI\\_DRIVER\\_VERSION](#) (MAKE\_VERSION(2, 2, 1))
 *LPSPI driver version.*

## Initialization and deinitialization

- void [LPSPI\\_MasterInit](#) (LPSPI\_Type \*base, const [lpspi\\_master\\_config\\_t](#) \*masterConfig, uint32\_t srcClock\_Hz)

- **void LPSPI\_MasterGetDefaultConfig (lpspi\_master\_config\_t \*masterConfig)**  
*Sets the lpspi\_master\_config\_t structure to default values.*
- **void LPSPI\_SlaveInit (LPSPI\_Type \*base, const lpspi\_slave\_config\_t \*slaveConfig)**  
*LPSPI slave configuration.*
- **void LPSPI\_SlaveGetDefaultConfig (lpspi\_slave\_config\_t \*slaveConfig)**  
*Sets the lpspi\_slave\_config\_t structure to default values.*
- **void LPSPI\_Deinit (LPSPI\_Type \*base)**  
*De-initializes the LPSPI peripheral.*
- **void LPSPI\_Reset (LPSPI\_Type \*base)**  
*Restores the LPSPI peripheral to reset state.*
- **uint32\_t LPSPIGetInstance (LPSPI\_Type \*base)**  
*Get the LPSPI instance from peripheral base address.*
- **static void LPSPI\_Enable (LPSPI\_Type \*base, bool enable)**  
*Enables the LPSPI peripheral and sets the MCR MDIS to 0.*

## Status

- **static uint32\_t LPSPI\_GetStatusFlags (LPSPI\_Type \*base)**  
*Gets the LPSPI status flag state.*
- **static uint8\_t LPSPI\_GetTxFifoSize (LPSPI\_Type \*base)**  
*Gets the LPSPI Tx FIFO size.*
- **static uint8\_t LPSPI\_GetRxFifoSize (LPSPI\_Type \*base)**  
*Gets the LPSPI Rx FIFO size.*
- **static uint32\_t LPSPI\_GetTxFifoCount (LPSPI\_Type \*base)**  
*Gets the LPSPI Tx FIFO count.*
- **static uint32\_t LPSPI\_GetRxFifoCount (LPSPI\_Type \*base)**  
*Gets the LPSPI Rx FIFO count.*
- **static void LPSPI\_ClearStatusFlags (LPSPI\_Type \*base, uint32\_t statusFlags)**  
*Clears the LPSPI status flag.*

## Interrupts

- **static void LPSPI\_EnableInterrupts (LPSPI\_Type \*base, uint32\_t mask)**  
*Enables the LPSPI interrupts.*
- **static void LPSPI\_DisableInterrupts (LPSPI\_Type \*base, uint32\_t mask)**  
*Disables the LPSPI interrupts.*

## DMA Control

- **static void LPSPI\_EnableDMA (LPSPI\_Type \*base, uint32\_t mask)**  
*Enables the LPSPI DMA request.*
- **static void LPSPI\_DisableDMA (LPSPI\_Type \*base, uint32\_t mask)**  
*Disables the LPSPI DMA request.*
- **static uint32\_t LPSPI\_GetTxRegisterAddress (LPSPI\_Type \*base)**  
*Gets the LPSPI Transmit Data Register address for a DMA operation.*
- **static uint32\_t LPSPI\_GetRxRegisterAddress (LPSPI\_Type \*base)**

*Gets the LPSPI Receive Data Register address for a DMA operation.*

## Bus Operations

- bool [LPSPI\\_CheckTransferArgument](#) (LPSPI\_Type \*base, lpspi\_transfer\_t \*transfer, bool isEdma)  
*Check the argument for transfer.*
- static void [LPSPI\\_SetMasterSlaveMode](#) (LPSPI\_Type \*base, lpspi\_master\_slave\_mode\_t mode)  
*Configures the LPSPI for either master or slave.*
- static void [LPSPI\\_SelectTransferPCS](#) (LPSPI\_Type \*base, lpspi\_which\_pcs\_t select)  
*Configures the peripheral chip select used for the transfer.*
- static void [LPSPI\\_SetPCSContinous](#) (LPSPI\_Type \*base, bool IsContinous)  
*Set the PCS signal to continuous or uncontinuous mode.*
- static bool [LPSPI\\_IsMaster](#) (LPSPI\_Type \*base)  
*Returns whether the LPSPI module is in master mode.*
- static void [LPSPI\\_FlushFifo](#) (LPSPI\_Type \*base, bool flushTxFifo, bool flushRxFifo)  
*Flushes the LPSPI FIFOs.*
- static void [LPSPI\\_SetFifoWatermarks](#) (LPSPI\_Type \*base, uint32\_t txWater, uint32\_t rxWater)  
*Sets the transmit and receive FIFO watermark values.*
- static void [LPSPI\\_SetAllPcsPolarity](#) (LPSPI\_Type \*base, uint32\_t mask)  
*Configures all LPSPI peripheral chip select polarities simultaneously.*
- static void [LPSPI\\_SetFrameSize](#) (LPSPI\_Type \*base, uint32\_t frameSize)  
*Configures the frame size.*
- uint32\_t [LPSPI\\_MasterSetBaudRate](#) (LPSPI\_Type \*base, uint32\_t baudRate\_Bps, uint32\_t srcClock\_Hz, uint32\_t \*tcrPrescaleValue)  
*Sets the LPSPI baud rate in bits per second.*
- void [LPSPI\\_MasterSetDelayScaler](#) (LPSPI\_Type \*base, uint32\_t scaler, lpspi\_delay\_type\_t whichDelay)  
*Manually configures a specific LPSPI delay parameter (module must be disabled to change the delay values).*
- uint32\_t [LPSPI\\_MasterSetDelayTimes](#) (LPSPI\_Type \*base, uint32\_t delayTimeInNanoSec, lpspi\_delay\_type\_t whichDelay, uint32\_t srcClock\_Hz)  
*Calculates the delay based on the desired delay input in nanoseconds (module must be disabled to change the delay values).*
- static void [LPSPI\\_WriteData](#) (LPSPI\_Type \*base, uint32\_t data)  
*Writes data into the transmit data buffer.*
- static uint32\_t [LPSPI\\_ReadData](#) (LPSPI\_Type \*base)  
*Reads data from the data buffer.*
- void [LPSPI\\_SetDummyData](#) (LPSPI\_Type \*base, uint8\_t dummyData)  
*Set up the dummy data.*

## Transactional

- void [LPSPI\\_MasterTransferCreateHandle](#) (LPSPI\_Type \*base, lpspi\_master\_handle\_t \*handle, lpspi\_master\_transfer\_callback\_t callback, void \*userData)  
*Initializes the LPSPI master handle.*
- status\_t [LPSPI\\_MasterTransferBlocking](#) (LPSPI\_Type \*base, lpspi\_transfer\_t \*transfer)  
*LPSPI master transfer data using a polling method.*

- `status_t LPSPI_MasterTransferNonBlocking (LPSPI_Type *base, lpspi_master_handle_t *handle, lpspi_transfer_t *transfer)`  
*LPSPI master transfer data using an interrupt method.*
- `status_t LPSPI_MasterTransferGetCount (LPSPI_Type *base, lpspi_master_handle_t *handle, size_t *count)`  
*Gets the master transfer remaining bytes.*
- `void LPSPI_MasterTransferAbort (LPSPI_Type *base, lpspi_master_handle_t *handle)`  
*LPSPI master abort transfer which uses an interrupt method.*
- `void LPSPI_MasterTransferHandleIRQ (LPSPI_Type *base, lpspi_master_handle_t *handle)`  
*LPSPI Master IRQ handler function.*
- `void LPSPI_SlaveTransferCreateHandle (LPSPI_Type *base, lpspi_slave_handle_t *handle, lpspi_slave_transfer_callback_t callback, void *userData)`  
*Initializes the LPSPI slave handle.*
- `status_t LPSPI_SlaveTransferNonBlocking (LPSPI_Type *base, lpspi_slave_handle_t *handle, lpspi_transfer_t *transfer)`  
*LPSPI slave transfer data using an interrupt method.*
- `status_t LPSPI_SlaveTransferGetCount (LPSPI_Type *base, lpspi_slave_handle_t *handle, size_t *count)`  
*Gets the slave transfer remaining bytes.*
- `void LPSPI_SlaveTransferAbort (LPSPI_Type *base, lpspi_slave_handle_t *handle)`  
*LPSPI slave aborts a transfer which uses an interrupt method.*
- `void LPSPI_SlaveTransferHandleIRQ (LPSPI_Type *base, lpspi_slave_handle_t *handle)`  
*LPSPI Slave IRQ handler function.*

## 24.2.4 Data Structure Documentation

### 24.2.4.1 struct lpspi\_master\_config\_t

#### Data Fields

- `uint32_t baudRate`  
*Baud Rate for LPSPI.*
- `uint32_t bitsPerFrame`  
*Bits per frame, minimum 8, maximum 4096.*
- `lpspi_clock_polarity_t cpol`  
*Clock polarity.*
- `lpspi_clock_phase_t cpha`  
*Clock phase.*
- `lpspi_shift_direction_t direction`  
*MSB or LSB data shift direction.*
- `uint32_t pcsToSckDelayInNanoSec`  
*PCS to SCK delay time in nanoseconds, setting to 0 sets the minimum delay.*
- `uint32_t lastSckToPcsDelayInNanoSec`  
*Last SCK to PCS delay time in nanoseconds, setting to 0 sets the minimum delay.*
- `uint32_t betweenTransferDelayInNanoSec`  
*After the SCK delay time with nanoseconds, setting to 0 sets the minimum delay.*
- `lpspi_which_pcs_t whichPcs`  
*Desired Peripheral Chip Select (PCS).*

- [lpspi\\_pcs\\_polarity\\_config\\_t pcsActiveHighOrLow](#)  
*Desired PCS active high or low.*
- [lpspi\\_pin\\_config\\_t pinCfg](#)  
*Configures which pins are used for input and output data during single bit transfers.*
- [lpspi\\_data\\_out\\_config\\_t dataOutConfig](#)  
*Configures if the output data is tristated between accesses (LPSPI\_PCS is negated).*

## Field Documentation

- (1) [uint32\\_t lpspi\\_master\\_config\\_t::baudRate](#)
- (2) [uint32\\_t lpspi\\_master\\_config\\_t::bitsPerFrame](#)
- (3) [lpspi\\_clock\\_polarity\\_t lpspi\\_master\\_config\\_t::cpol](#)
- (4) [lpspi\\_clock\\_phase\\_t lpspi\\_master\\_config\\_t::cpha](#)
- (5) [lpspi\\_shift\\_direction\\_t lpspi\\_master\\_config\\_t::direction](#)
- (6) [uint32\\_t lpspi\\_master\\_config\\_t::pcsToSckDelayInNanoSec](#)

It sets the boundary value if out of range.

- (7) [uint32\\_t lpspi\\_master\\_config\\_t::lastSckToPcsDelayInNanoSec](#)

It sets the boundary value if out of range.

- (8) [uint32\\_t lpspi\\_master\\_config\\_t::betweenTransferDelayInNanoSec](#)

It sets the boundary value if out of range.

- (9) [lpspi\\_which\\_pcs\\_t lpspi\\_master\\_config\\_t::whichPcs](#)
- (10) [lpspi\\_pin\\_config\\_t lpspi\\_master\\_config\\_t::pinCfg](#)
- (11) [lpspi\\_data\\_out\\_config\\_t lpspi\\_master\\_config\\_t::dataOutConfig](#)

### 24.2.4.2 struct lpspi\_slave\_config\_t

#### Data Fields

- [uint32\\_t bitsPerFrame](#)  
*Bits per frame, minimum 8, maximum 4096.*
- [lpspi\\_clock\\_polarity\\_t cpol](#)  
*Clock polarity.*
- [lpspi\\_clock\\_phase\\_t cpha](#)  
*Clock phase.*
- [lpspi\\_shift\\_direction\\_t direction](#)  
*MSB or LSB data shift direction.*
- [lpspi\\_which\\_pcs\\_t whichPcs](#)  
*Desired Peripheral Chip Select (pcs)*

- [lpspi\\_pcs\\_polarity\\_config\\_t](#) `pcsActiveHighOrLow`  
*Desired PCS active high or low.*
- [lpspi\\_pin\\_config\\_t](#) `pinCfg`  
*Configures which pins are used for input and output data during single bit transfers.*
- [lpspi\\_data\\_out\\_config\\_t](#) `dataOutConfig`  
*Configures if the output data is tristated between accesses (LPSPI\_PCS is negated).*

#### Field Documentation

- (1) `uint32_t lpspi_slave_config_t::bitsPerFrame`
- (2) `lpspi_clock_polarity_t lpspi_slave_config_t::cpol`
- (3) `lpspi_clock_phase_t lpspi_slave_config_t::cpha`
- (4) `lpspi_shift_direction_t lpspi_slave_config_t::direction`
- (5) `lpspi_pin_config_t lpspi_slave_config_t::pinCfg`
- (6) `lpspi_data_out_config_t lpspi_slave_config_t::dataOutConfig`

#### 24.2.4.3 struct `lpspi_transfer_t`

##### Data Fields

- `uint8_t * txData`  
*Send buffer.*
- `uint8_t * rxData`  
*Receive buffer.*
- `volatile size_t dataSize`  
*Transfer bytes.*
- `uint32_t configFlags`  
*Transfer transfer configuration flags.*

#### Field Documentation

- (1) `uint8_t* lpspi_transfer_t::txData`
- (2) `uint8_t* lpspi_transfer_t::rxData`
- (3) `volatile size_t lpspi_transfer_t::dataSize`
- (4) `uint32_t lpspi_transfer_t::configFlags`

Set from `_lpspi_transfer_config_flag_for_master` if the transfer is used for master or `_lpspi_transfer_config_flag_for_slave` enumeration if the transfer is used for slave.

#### 24.2.4.4 struct `_lpspi_master_handle`

Forward declaration of the `_lpspi_master_handle` typedefs.

## Data Fields

- volatile bool **isPcsContinuous**  
*Is PCS continuous in transfer.*
- volatile bool **writeTcrInIsr**  
*A flag that whether should write TCR in ISR.*
- volatile bool **isByteSwap**  
*A flag that whether should byte swap.*
- volatile bool **isTxMask**  
*A flag that whether TCR[TXMSK] is set.*
- volatile uint16\_t **bytesPerFrame**  
*Number of bytes in each frame.*
- volatile uint8\_t **fifoSize**  
*FIFO dataSize.*
- volatile uint8\_t **rxWatermark**  
*Rx watermark.*
- volatile uint8\_t **bytesEachWrite**  
*Bytes for each write TDR.*
- volatile uint8\_t **bytesEachRead**  
*Bytes for each read RDR.*
- uint8\_t \*volatile **txData**  
*Send buffer.*
- uint8\_t \*volatile **rxData**  
*Receive buffer.*
- volatile size\_t **txRemainingByteCount**  
*Number of bytes remaining to send.*
- volatile size\_t **rxRemainingByteCount**  
*Number of bytes remaining to receive.*
- volatile uint32\_t **writeRegRemainingTimes**  
*Write TDR register remaining times.*
- volatile uint32\_t **readRegRemainingTimes**  
*Read RDR register remaining times.*
- uint32\_t **totalByteCount**  
*Number of transfer bytes.*
- uint32\_t **txBuffIfNull**  
*Used if the txData is NULL.*
- volatile uint8\_t **state**  
*LPSPI transfer state , \_lpspi\_transfer\_state.*
- **lpspi\_master\_transfer\_callback\_t callback**  
*Completion callback.*
- void \* **userData**  
*Callback user data.*

## Field Documentation

- (1) **volatile bool lpspi\_master\_handle\_t::isPcsContinuous**
- (2) **volatile bool lpspi\_master\_handle\_t::writeTcrInIsr**
- (3) **volatile bool lpspi\_master\_handle\_t::isByteSwap**

- (4) volatile bool lpspi\_master\_handle\_t::isTxMask
- (5) volatile uint8\_t lpspi\_master\_handle\_t::fifoSize
- (6) volatile uint8\_t lpspi\_master\_handle\_t::rxWatermark
- (7) volatile uint8\_t lpspi\_master\_handle\_t::bytesEachWrite
- (8) volatile uint8\_t lpspi\_master\_handle\_t::bytesEachRead
- (9) uint8\_t\* volatile lpspi\_master\_handle\_t::txData
- (10) uint8\_t\* volatile lpspi\_master\_handle\_t::rxData
- (11) volatile size\_t lpspi\_master\_handle\_t::txRemainingByteCount
- (12) volatile size\_t lpspi\_master\_handle\_t::rxRemainingByteCount
- (13) volatile uint32\_t lpspi\_master\_handle\_t::writeRegRemainingTimes
- (14) volatile uint32\_t lpspi\_master\_handle\_t::readRegRemainingTimes
- (15) uint32\_t lpspi\_master\_handle\_t::txBuffIfNull
- (16) volatile uint8\_t lpspi\_master\_handle\_t::state
- (17) lpspi\_master\_transfer\_callback\_t lpspi\_master\_handle\_t::callback
- (18) void\* lpspi\_master\_handle\_t::userData

#### 24.2.4.5 struct \_lpspi\_slave\_handle

Forward declaration of the [\\_lpspi\\_slave\\_handle](#) typedefs.

#### Data Fields

- volatile bool [isByteSwap](#)  
*A flag that whether should byte swap.*
- volatile uint8\_t [fifoSize](#)  
*FIFO dataSize.*
- volatile uint8\_t [rxWatermark](#)  
*Rx watermark.*
- volatile uint8\_t [bytesEachWrite](#)  
*Bytes for each write TDR.*
- volatile uint8\_t [bytesEachRead](#)  
*Bytes for each read RDR.*
- uint8\_t \*volatile [txData](#)  
*Send buffer.*
- uint8\_t \*volatile [rxData](#)  
*Receive buffer.*

- volatile size\_t **txRemainingByteCount**  
*Number of bytes remaining to send.*
- volatile size\_t **rxRemainingByteCount**  
*Number of bytes remaining to receive.*
- volatile uint32\_t **writeRegRemainingTimes**  
*Write TDR register remaining times.*
- volatile uint32\_t **readRegRemainingTimes**  
*Read RDR register remaining times.*
- uint32\_t **totalByteCount**  
*Number of transfer bytes.*
- volatile uint8\_t **state**  
*LPSPI transfer state , \_lpspi\_transfer\_state.*
- volatile uint32\_t **errorCount**  
*Error count for slave transfer.*
- **lpspi\_slave\_transfer\_callback\_t callback**  
*Completion callback.*
- void \* **userData**  
*Callback user data.*

## Field Documentation

- (1) volatile bool **lpspi\_slave\_handle\_t::isByteSwap**
- (2) volatile uint8\_t **lpspi\_slave\_handle\_t::fifoSize**
- (3) volatile uint8\_t **lpspi\_slave\_handle\_t::rxWatermark**
- (4) volatile uint8\_t **lpspi\_slave\_handle\_t::bytesEachWrite**
- (5) volatile uint8\_t **lpspi\_slave\_handle\_t::bytesEachRead**
- (6) uint8\_t\* volatile **lpspi\_slave\_handle\_t::txData**
- (7) uint8\_t\* volatile **lpspi\_slave\_handle\_t::rxData**
- (8) volatile size\_t **lpspi\_slave\_handle\_t::txRemainingByteCount**
- (9) volatile size\_t **lpspi\_slave\_handle\_t::rxRemainingByteCount**
- (10) volatile uint32\_t **lpspi\_slave\_handle\_t::writeRegRemainingTimes**
- (11) volatile uint32\_t **lpspi\_slave\_handle\_t::readRegRemainingTimes**
- (12) volatile uint8\_t **lpspi\_slave\_handle\_t::state**
- (13) volatile uint32\_t **lpspi\_slave\_handle\_t::errorCount**
- (14) **lpspi\_slave\_transfer\_callback\_t lpspi\_slave\_handle\_t::callback**
- (15) void\* **lpspi\_slave\_handle\_t::userData**

## 24.2.5 Macro Definition Documentation

**24.2.5.1 #define FSL\_LPSPI\_DRIVER\_VERSION (MAKE\_VERSION(2, 2, 1))**

**24.2.5.2 #define LPSPI\_DUMMY\_DATA (0x00U)**

Dummy data used for tx if there is not txData.

**24.2.5.3 #define SPI\_RETRY\_TIMES 0U /\* Define to zero means keep waiting until the flag is assert/deassert. \*/**

**24.2.5.4 #define LPSPI\_MASTER\_PCS\_SHIFT (4U)**

**24.2.5.5 #define LPSPI\_MASTER\_PCS\_MASK (0xF0U)**

**24.2.5.6 #define LPSPI\_SLAVE\_PCS\_SHIFT (4U)**

**24.2.5.7 #define LPSPI\_SLAVE\_PCS\_MASK (0xF0U)**

## 24.2.6 Typedef Documentation

**24.2.6.1 typedef void(\* lpspi\_master\_transfer\_callback\_t)(LPSPI\_Type \*base, lpspi\_master\_handle\_t \*handle, status\_t status, void \*userData)**

Parameters

|                 |                                                                     |
|-----------------|---------------------------------------------------------------------|
| <i>base</i>     | LPSPI peripheral address.                                           |
| <i>handle</i>   | Pointer to the handle for the LPSPI master.                         |
| <i>status</i>   | Success or error code describing whether the transfer is completed. |
| <i>userData</i> | Arbitrary pointer-dataSized value passed from the application.      |

**24.2.6.2 typedef void(\* lpspi\_slave\_transfer\_callback\_t)(LPSPI\_Type \*base, lpspi\_slave\_handle\_t \*handle, status\_t status, void \*userData)**

Parameters

|                 |                                                                     |
|-----------------|---------------------------------------------------------------------|
| <i>base</i>     | LPSPI peripheral address.                                           |
| <i>handle</i>   | Pointer to the handle for the LPSPI slave.                          |
| <i>status</i>   | Success or error code describing whether the transfer is completed. |
| <i>userData</i> | Arbitrary pointer-dataSized value passed from the application.      |

## 24.2.7 Enumeration Type Documentation

### 24.2.7.1 anonymous enum

Enumerator

*kStatus\_LPSPI\_Busy* LPSPI transfer is busy.  
*kStatus\_LPSPI\_Error* LPSPI driver error.  
*kStatus\_LPSPI\_Idle* LPSPI is idle.  
*kStatus\_LPSPI\_OutOfRange* LPSPI transfer out Of range.  
*kStatus\_LPSPI\_Timeout* LPSPI timeout polling status flags.

### 24.2.7.2 enum \_lpspi\_flags

Enumerator

*kLPSPI\_TxDataRequestFlag* Transmit data flag.  
*kLPSPI\_RxDataReadyFlag* Receive data flag.  
*kLPSPI\_WordCompleteFlag* Word Complete flag.  
*kLPSPI\_FrameCompleteFlag* Frame Complete flag.  
*kLPSPI\_TransferCompleteFlag* Transfer Complete flag.  
*kLPSPI\_TransmitErrorFlag* Transmit Error flag (FIFO underrun)  
*kLPSPI\_ReceiveErrorFlag* Receive Error flag (FIFO overrun)  
*kLPSPI\_DataMatchFlag* Data Match flag.  
*kLPSPI\_ModuleBusyFlag* Module Busy flag.  
*kLPSPI\_AllStatusFlag* Used for clearing all w1c status flags.

### 24.2.7.3 enum \_lpspi\_interrupt\_enable

Enumerator

*kLPSPI\_TxInterruptEnable* Transmit data interrupt enable.  
*kLPSPI\_RxInterruptEnable* Receive data interrupt enable.  
*kLPSPI\_WordCompleteInterruptEnable* Word complete interrupt enable.  
*kLPSPI\_FrameCompleteInterruptEnable* Frame complete interrupt enable.  
*kLPSPI\_TransferCompleteInterruptEnable* Transfer complete interrupt enable.

*kLPSPI\_TransmitErrorInterruptEnable* Transmit error interrupt enable(FIFO underrun)  
*kLPSPI\_ReceiveErrorInterruptEnable* Receive Error interrupt enable (FIFO overrun)  
*kLPSPI\_DataMatchInterruptEnable* Data Match interrupt enable.  
*kLPSPI\_AllInterruptEnable* All above interrupts enable.

#### 24.2.7.4 enum \_lpspi\_dma\_enable

Enumerator

*kLPSPI\_TxDmaEnable* Transmit data DMA enable.  
*kLPSPI\_RxDmaEnable* Receive data DMA enable.

#### 24.2.7.5 enum lpspi\_master\_slave\_mode\_t

Enumerator

*kLPSPI\_Master* LPSPI peripheral operates in master mode.  
*kLPSPI\_Slave* LPSPI peripheral operates in slave mode.

#### 24.2.7.6 enum lpspi\_which\_pcs\_t

Enumerator

*kLPSPI\_Pcs0* PCS[0].  
*kLPSPI\_Pcs1* PCS[1].  
*kLPSPI\_Pcs2* PCS[2].  
*kLPSPI\_Pcs3* PCS[3].

#### 24.2.7.7 enum lpspi\_pcs\_polarity\_config\_t

Enumerator

*kLPSPI\_PcsActiveHigh* PCS Active High (idles low)  
*kLPSPI\_PcsActiveLow* PCS Active Low (idles high)

#### 24.2.7.8 enum \_lpspi\_pcs\_polarity

Enumerator

*kLPSPI\_Pcs0ActiveLow* Pcs0 Active Low (idles high).  
*kLPSPI\_Pcs1ActiveLow* Pcs1 Active Low (idles high).

*kLPSPI\_Pcs2ActiveLow* Pcs2 Active Low (idles high).

*kLPSPI\_Pcs3ActiveLow* Pcs3 Active Low (idles high).

*kLPSPI\_PcsAllActiveLow* Pcs0 to Pcs5 Active Low (idles high).

#### 24.2.7.9 enum lpspi\_clock\_polarity\_t

Enumerator

*kLPSPI\_ClockPolarityActiveHigh* CPOL=0. Active-high LPSPI clock (idles low)

*kLPSPI\_ClockPolarityActiveLow* CPOL=1. Active-low LPSPI clock (idles high)

#### 24.2.7.10 enum lpspi\_clock\_phase\_t

Enumerator

*kLPSPI\_ClockPhaseFirstEdge* CPHA=0. Data is captured on the leading edge of the SCK and changed on the following edge.

*kLPSPI\_ClockPhaseSecondEdge* CPHA=1. Data is changed on the leading edge of the SCK and captured on the following edge.

#### 24.2.7.11 enum lpspi\_shift\_direction\_t

Enumerator

*kLPSPI\_MsbFirst* Data transfers start with most significant bit.

*kLPSPI\_LsbFirst* Data transfers start with least significant bit.

#### 24.2.7.12 enum lpspi\_host\_request\_select\_t

Enumerator

*kLPSPI\_HostReqExtPin* Host Request is an ext pin.

*kLPSPI\_HostReqInternalTrigger* Host Request is an internal trigger.

#### 24.2.7.13 enum lpspi\_match\_config\_t

Enumerator

*kLPSI\_MatchDisabled* LPSPI Match Disabled.

*kLPSI\_1stWordEqualsM0orM1* LPSPI Match Enabled.

*kLPSI\_AnyWordEqualsM0orM1* LPSPI Match Enabled.

*kLPSI\_1stWordEqualsM0and2ndWordEqualsM1* LPSPI Match Enabled.  
*kLPSI\_AnyWordEqualsM0andNxtWordEqualsM1* LPSPI Match Enabled.  
*kLPSI\_1stWordAndM1EqualsM0andM1* LPSPI Match Enabled.  
*kLPSI\_AnyWordAndM1EqualsM0andM1* LPSPI Match Enabled.

#### 24.2.7.14 enum lpspi\_pin\_config\_t

Enumerator

*kLPSPISdiInSdoOut* LPSPI SDI input, SDO output.  
*kLPSPISdiInSdiOut* LPSPI SDI input, SDI output.  
*kLPSPISdoInSdoOut* LPSPI SDO input, SDO output.  
*kLPSPISdoInSdiOut* LPSPI SDO input, SDI output.

#### 24.2.7.15 enum lpspi\_data\_out\_config\_t

Enumerator

*kLpSpiDataOutRetained* Data out retains last value when chip select is de-asserted.  
*kLpSpiDataOutTristate* Data out is tristated when chip select is de-asserted.

#### 24.2.7.16 enum lpspi\_transfer\_width\_t

Enumerator

*kLPSPISingleBitXfer* 1-bit shift at a time, data out on SDO, in on SDI (normal mode)  
*kLPSPITwoBitXfer* 2-bits shift out on SDO/SDI and in on SDO/SDI  
*kLPSPIFourBitXfer* 4-bits shift out on SDO/SDI/PCS[3:2] and in on SDO/SDI/PCS[3:2]

#### 24.2.7.17 enum lpspi\_delay\_type\_t

Enumerator

*kLPSPICsToSck* PCS-to-SCK delay.  
*kLPSPILastSckToPcs* Last SCK edge to PCS delay.  
*kLPSPIBetweenTransfer* Delay between transfers.

#### 24.2.7.18 enum \_lpspi\_transfer\_config\_flag\_for\_master

Enumerator

***kLPSPI\_MasterPcs0*** LPSPI master transfer use PCS0 signal.

***kLPSPI\_MasterPcs1*** LPSPI master transfer use PCS1 signal.

***kLPSPI\_MasterPcs2*** LPSPI master transfer use PCS2 signal.

***kLPSPI\_MasterPcs3*** LPSPI master transfer use PCS3 signal.

***kLPSPI\_MasterPcsContinuous*** Is PCS signal continuous.

***kLPSPI\_MasterByteSwap*** Is master swap the byte. For example, when want to send data 1 2 3 4 5 6 7 8 (suppose you set lpspi\_shift\_direction\_t to MSB).

1. If you set bitPerFrame = 8 , no matter the kLPSPI\_MasterByteSwap flag is used or not, the waveform is 1 2 3 4 5 6 7 8.
2. If you set bitPerFrame = 16 : (1) the waveform is 2 1 4 3 6 5 8 7 if you do not use the kLPSPI\_MasterByteSwap flag. (2) the waveform is 1 2 3 4 5 6 7 8 if you use the kLPSPI\_MasterByteSwap flag.
3. If you set bitPerFrame = 32 : (1) the waveform is 4 3 2 1 8 7 6 5 if you do not use the kLPSPI\_MasterByteSwap flag. (2) the waveform is 1 2 3 4 5 6 7 8 if you use the kLPSPI\_MasterByteSwap flag.

#### 24.2.7.19 enum \_lpspi\_transfer\_config\_flag\_for\_slave

Enumerator

***kLPSPI\_SlavePcs0*** LPSPI slave transfer use PCS0 signal.

***kLPSPI\_SlavePcs1*** LPSPI slave transfer use PCS1 signal.

***kLPSPI\_SlavePcs2*** LPSPI slave transfer use PCS2 signal.

***kLPSPI\_SlavePcs3*** LPSPI slave transfer use PCS3 signal.

***kLPSPI\_SlaveByteSwap*** Is slave swap the byte. For example, when want to send data 1 2 3 4 5 6 7 8 (suppose you set lpspi\_shift\_direction\_t to MSB).

1. If you set bitPerFrame = 8 , no matter the kLPSPI\_SlaveByteSwap flag is used or not, the waveform is 1 2 3 4 5 6 7 8.
2. If you set bitPerFrame = 16 : (1) the waveform is 2 1 4 3 6 5 8 7 if you do not use the kLPSPI\_SlaveByteSwap flag. (2) the waveform is 1 2 3 4 5 6 7 8 if you use the kLPSPI\_SlaveByteSwap flag.
3. If you set bitPerFrame = 32 : (1) the waveform is 4 3 2 1 8 7 6 5 if you do not use the kLPSPI\_SlaveByteSwap flag. (2) the waveform is 1 2 3 4 5 6 7 8 if you use the kLPSPI\_SlaveByteSwap flag.

#### 24.2.7.20 enum \_lpspi\_transfer\_state

Enumerator

***kLPSPI\_Idle*** Nothing in the transmitter/receiver.

**kLPSPI\_Busy** Transfer queue is not finished.

**kLPSPI\_Error** Transfer error.

## 24.2.8 Function Documentation

### 24.2.8.1 void LPSPI\_MasterInit ( **LPSPI\_Type** \* *base*, const **lpspi\_master\_config\_t** \* *masterConfig*, **uint32\_t** *srcClock\_Hz* )

Parameters

|                     |                                                              |
|---------------------|--------------------------------------------------------------|
| <i>base</i>         | LPSPI peripheral address.                                    |
| <i>masterConfig</i> | Pointer to structure <a href="#">lpspi_master_config_t</a> . |
| <i>srcClock_Hz</i>  | Module source input clock in Hertz                           |

### 24.2.8.2 void LPSPI\_MasterGetDefaultConfig ( **lpspi\_master\_config\_t** \* *masterConfig* )

This API initializes the configuration structure for [LPSPI\\_MasterInit\(\)](#). The initialized structure can remain unchanged in [LPSPI\\_MasterInit\(\)](#), or can be modified before calling the [LPSPI\\_MasterInit\(\)](#). Example:

```
* lpspi_master_config_t masterConfig;
* LPSPI_MasterGetDefaultConfig(&masterConfig);
*
```

Parameters

|                     |                                                            |
|---------------------|------------------------------------------------------------|
| <i>masterConfig</i> | pointer to <a href="#">lpspi_master_config_t</a> structure |
|---------------------|------------------------------------------------------------|

### 24.2.8.3 void LPSPI\_SlaveInit ( **LPSPI\_Type** \* *base*, const **lpspi\_slave\_config\_t** \* *slaveConfig* )

Parameters

|                    |                                                               |
|--------------------|---------------------------------------------------------------|
| <i>base</i>        | LPSPI peripheral address.                                     |
| <i>slaveConfig</i> | Pointer to a structure <a href="#">lpspi_slave_config_t</a> . |

### 24.2.8.4 void LPSPI\_SlaveGetDefaultConfig ( **lpspi\_slave\_config\_t** \* *slaveConfig* )

This API initializes the configuration structure for [LPSPI\\_SlaveInit\(\)](#). The initialized structure can remain unchanged in [LPSPI\\_SlaveInit\(\)](#) or can be modified before calling the [LPSPI\\_SlaveInit\(\)](#). Example:

```
* lpspi_slave_config_t slaveConfig;
* LPSPI_SlaveGetDefaultConfig(&slaveConfig);
*
```

Parameters

|                    |                                                            |
|--------------------|------------------------------------------------------------|
| <i>slaveConfig</i> | pointer to <a href="#">lpspi_slave_config_t</a> structure. |
|--------------------|------------------------------------------------------------|

#### 24.2.8.5 void LPSPI\_Deinit ( LPSPI\_Type \* *base* )

Call this API to disable the LPSPI clock.

Parameters

|             |                           |
|-------------|---------------------------|
| <i>base</i> | LPSPI peripheral address. |
|-------------|---------------------------|

#### 24.2.8.6 void LPSPI\_Reset ( LPSPI\_Type \* *base* )

Note that this function sets all registers to reset state. As a result, the LPSPI module can't work after calling this API.

Parameters

|             |                           |
|-------------|---------------------------|
| <i>base</i> | LPSPI peripheral address. |
|-------------|---------------------------|

#### 24.2.8.7 uint32\_t LPSPIGetInstance ( LPSPI\_Type \* *base* )

Parameters

|             |                                |
|-------------|--------------------------------|
| <i>base</i> | LPSPI peripheral base address. |
|-------------|--------------------------------|

Returns

LPSPI instance.

#### 24.2.8.8 static void LPSPI\_Enable ( LPSPI\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                                      |
|---------------|------------------------------------------------------|
| <i>base</i>   | LPSPI peripheral address.                            |
| <i>enable</i> | Pass true to enable module, false to disable module. |

#### 24.2.8.9 static uint32\_t LPSPI\_GetStatusFlags ( LPSPI\_Type \* *base* ) [inline], [static]

Parameters

|             |                           |
|-------------|---------------------------|
| <i>base</i> | LPSPI peripheral address. |
|-------------|---------------------------|

Returns

The LPSPI status(in SR register).

#### 24.2.8.10 static uint8\_t LPSPI\_GetTxFifoSize ( LPSPI\_Type \* *base* ) [inline], [static]

Parameters

|             |                           |
|-------------|---------------------------|
| <i>base</i> | LPSPI peripheral address. |
|-------------|---------------------------|

Returns

The LPSPI Tx FIFO size.

#### 24.2.8.11 static uint8\_t LPSPI\_GetRxFifoSize ( LPSPI\_Type \* *base* ) [inline], [static]

Parameters

|             |                           |
|-------------|---------------------------|
| <i>base</i> | LPSPI peripheral address. |
|-------------|---------------------------|

Returns

The LPSPI Rx FIFO size.

#### 24.2.8.12 static uint32\_t LPSPI\_GetTxFifoCount ( LPSPI\_Type \* *base* ) [inline], [static]

Parameters

|             |                           |
|-------------|---------------------------|
| <i>base</i> | LPSPI peripheral address. |
|-------------|---------------------------|

Returns

The number of words in the transmit FIFO.

#### 24.2.8.13 static uint32\_t LPSPI\_GetRxFifoCount ( LPSPI\_Type \* *base* ) [inline], [static]

Parameters

|             |                           |
|-------------|---------------------------|
| <i>base</i> | LPSPI peripheral address. |
|-------------|---------------------------|

Returns

The number of words in the receive FIFO.

#### 24.2.8.14 static void LPSPI\_ClearStatusFlags ( LPSPI\_Type \* *base*, uint32\_t *statusFlags* ) [inline], [static]

This function clears the desired status bit by using a write-1-to-clear. The user passes in the base and the desired status flag bit to clear. The list of status flags is defined in the \_lpspi\_flags. Example usage:

```
* LPSPI_ClearStatusFlags(base, kLPSPI_TxDataRequestFlag|
 kLPSPI_RxDataReadyFlag);
*
```

Parameters

|                    |                                              |
|--------------------|----------------------------------------------|
| <i>base</i>        | LPSPI peripheral address.                    |
| <i>statusFlags</i> | The status flag used from type _lpspi_flags. |

< The status flags are cleared by writing 1 (w1c).

#### 24.2.8.15 static void LPSPI\_EnableInterrupts ( LPSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function configures the various interrupt masks of the LPSPI. The parameters are base and an interrupt mask. Note that, for Tx fill and Rx FIFO drain requests, enabling the interrupt request disables the DMA request.

```
* LPSPI_EnableInterrupts(base, kLPSPI_TxInterruptEnable |
 kLPSPI_RxInterruptEnable);
*
```

Parameters

|             |                                                           |
|-------------|-----------------------------------------------------------|
| <i>base</i> | LPSPI peripheral address.                                 |
| <i>mask</i> | The interrupt mask; Use the enum _lpspi_interrupt_enable. |

#### 24.2.8.16 static void LPSPI\_DisableInterrupts ( LPSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

```
* LPSPI_DisableInterrupts(base, kLPSPI_TxInterruptEnable |
 kLPSPI_RxInterruptEnable);
*
```

Parameters

|             |                                                           |
|-------------|-----------------------------------------------------------|
| <i>base</i> | LPSPI peripheral address.                                 |
| <i>mask</i> | The interrupt mask; Use the enum _lpspi_interrupt_enable. |

#### 24.2.8.17 static void LPSPI\_EnableDMA ( LPSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function configures the Rx and Tx DMA mask of the LPSPI. The parameters are base and a DMA mask.

```
* LPSPI_EnableDMA(base, kLPSPI_TxDmaEnable |
 kLPSPI_RxDmaEnable);
*
```

Parameters

|             |                                                     |
|-------------|-----------------------------------------------------|
| <i>base</i> | LPSPI peripheral address.                           |
| <i>mask</i> | The interrupt mask; Use the enum _lpspi_dma_enable. |

#### 24.2.8.18 static void LPSPI\_DisableDMA ( LPSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

This function configures the Rx and Tx DMA mask of the LPSPI. The parameters are base and a DMA mask.

```
* SPI_DisableDMA(base, kLPSPI_TxDmaEnable |
 kLPSPI_RxDmaEnable);
*
```

Parameters

|             |                                                     |
|-------------|-----------------------------------------------------|
| <i>base</i> | LPSPI peripheral address.                           |
| <i>mask</i> | The interrupt mask; Use the enum _lpspi_dma_enable. |

#### 24.2.8.19 static uint32\_t LPSPI\_GetTxRegisterAddress ( LPSPI\_Type \* *base* ) [inline], [static]

This function gets the LPSPI Transmit Data Register address because this value is needed for the DMA operation. This function can be used for either master or slave mode.

Parameters

|             |                           |
|-------------|---------------------------|
| <i>base</i> | LPSPI peripheral address. |
|-------------|---------------------------|

Returns

The LPSPI Transmit Data Register address.

#### 24.2.8.20 static uint32\_t LPSPI\_GetRxRegisterAddress ( LPSPI\_Type \* *base* ) [inline], [static]

This function gets the LPSPI Receive Data Register address because this value is needed for the DMA operation. This function can be used for either master or slave mode.

Parameters

|             |                           |
|-------------|---------------------------|
| <i>base</i> | LPSPI peripheral address. |
|-------------|---------------------------|

Returns

The LPSPI Receive Data Register address.

#### 24.2.8.21 bool LPSPI\_CheckTransferArgument ( LPSPI\_Type \* *base*, lpspi\_transfer\_t \* *transfer*, bool *isEdma* )

Parameters

|                 |                                                                                 |
|-----------------|---------------------------------------------------------------------------------|
| <i>base</i>     | LPSPI peripheral address.                                                       |
| <i>transfer</i> | the transfer struct to be used.                                                 |
| <i>isEdma</i>   | True to check for EDMA transfer, false to check interrupt non-blocking transfer |

Returns

Return true for right and false for wrong.

#### 24.2.8.22 static void LPSPI\_SetMasterSlaveMode ( LPSPI\_Type \* *base*, lpspi\_master\_slave\_mode\_t *mode* ) [inline], [static]

Note that the CFGR1 should only be written when the LPSPI is disabled (LPSPIx\_CR\_MEN = 0).

Parameters

|             |                                                                   |
|-------------|-------------------------------------------------------------------|
| <i>base</i> | LPSPI peripheral address.                                         |
| <i>mode</i> | Mode setting (master or slave) of type lpspi_master_slave_mode_t. |

#### 24.2.8.23 static void LPSPI\_SelectTransferPCS ( LPSPI\_Type \* *base*, lpspi\_which\_pcs\_t *select* ) [inline], [static]

Parameters

|               |                                                   |
|---------------|---------------------------------------------------|
| <i>base</i>   | LPSPI peripheral address.                         |
| <i>select</i> | LPSPI Peripheral Chip Select (PCS) configuration. |

#### 24.2.8.24 static void LPSPI\_SetPCSContinuous ( LPSPI\_Type \* *base*, bool *IsContinuous* ) [inline], [static]

Note

In master mode, continuous transfer will keep the PCS asserted at the end of the frame size, until a command word is received that starts a new frame. So PCS must be set back to uncontinuous when transfer finishes. In slave mode, when continuous transfer is enabled, the LPSPI will only transmit the first frame size bits, after that the LPSPI will transmit received data back (assuming a 32-bit shift register).

Parameters

|                    |                                                                                     |
|--------------------|-------------------------------------------------------------------------------------|
| <i>base</i>        | LPSPI peripheral address.                                                           |
| <i>IsContinous</i> | True to set the transfer PCS to continuous mode, false to set to uncontinuous mode. |

#### 24.2.8.25 static bool LPSPI\_IsMaster ( LPSPI\_Type \* *base* ) [inline], [static]

Parameters

|             |                           |
|-------------|---------------------------|
| <i>base</i> | LPSPI peripheral address. |
|-------------|---------------------------|

Returns

Returns true if the module is in master mode or false if the module is in slave mode.

#### 24.2.8.26 static void LPSPI\_FlushFifo ( LPSPI\_Type \* *base*, bool *flushTxFifo*, bool *flushRxFifo* ) [inline], [static]

Parameters

|                    |                                                                    |
|--------------------|--------------------------------------------------------------------|
| <i>base</i>        | LPSPI peripheral address.                                          |
| <i>flushTxFifo</i> | Flushes (true) the Tx FIFO, else do not flush (false) the Tx FIFO. |
| <i>flushRxFifo</i> | Flushes (true) the Rx FIFO, else do not flush (false) the Rx FIFO. |

#### 24.2.8.27 static void LPSPI\_SetFifoWatermarks ( LPSPI\_Type \* *base*, uint32\_t *txWater*, uint32\_t *rxWater* ) [inline], [static]

This function allows the user to set the receive and transmit FIFO watermarks. The function does not compare the watermark settings to the FIFO size. The FIFO watermark should not be equal to or greater than the FIFO size. It is up to the higher level driver to make this check.

Parameters

|             |                           |
|-------------|---------------------------|
| <i>base</i> | LPSPI peripheral address. |
|-------------|---------------------------|

|                |                                                                                                |
|----------------|------------------------------------------------------------------------------------------------|
| <i>txWater</i> | The TX FIFO watermark value. Writing a value equal or greater than the FIFO size is truncated. |
| <i>rxWater</i> | The RX FIFO watermark value. Writing a value equal or greater than the FIFO size is truncated. |

#### 24.2.8.28 static void LPSPI\_SetAllPcsPolarity ( LPSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Note that the CFGR1 should only be written when the LPSPI is disabled (LPSPIx\_CR\_MEN = 0).

This is an example: PCS0 and PCS1 set to active low and other PCSs set to active high. Note that the number of PCS is device-specific.

```
* LPSPI_SetAllPcsPolarity(base, kLPSPI_Pcs0ActiveLow |
 kLPSPI_Pcs1ActiveLow);
*
```

Parameters

|             |                                                          |
|-------------|----------------------------------------------------------|
| <i>base</i> | LPSPI peripheral address.                                |
| <i>mask</i> | The PCS polarity mask; Use the enum _lpspi_pcs_polarity. |

#### 24.2.8.29 static void LPSPI\_SetFrameSize ( LPSPI\_Type \* *base*, uint32\_t *frameSize* ) [inline], [static]

The minimum frame size is 8-bits and the maximum frame size is 4096-bits. If the frame size is less than or equal to 32-bits, the word size and frame size are identical. If the frame size is greater than 32-bits, the word size is 32-bits for each word except the last (the last word contains the remainder bits if the frame size is not divisible by 32). The minimum word size is 2-bits. A frame size of 33-bits (or similar) is not supported.

Note 1: The transmit command register should be initialized before enabling the LPSPI in slave mode, although the command register does not update until after the LPSPI is enabled. After it is enabled, the transmit command register should only be changed if the LPSPI is idle.

Note 2: The transmit and command FIFO is a combined FIFO that includes both transmit data and command words. That means the TCR register should be written to when the Tx FIFO is not full.

Parameters

|                  |                                   |
|------------------|-----------------------------------|
| <i>base</i>      | LPSPI peripheral address.         |
| <i>frameSize</i> | The frame size in number of bits. |

#### 24.2.8.30 `uint32_t LPSPI_MasterSetBaudRate ( LPSPI_Type * base, uint32_t baudRate_Bps, uint32_t srcClock_Hz, uint32_t * tcrPrescaleValue )`

This function takes in the desired bitsPerSec (baud rate) and calculates the nearest possible baud rate without exceeding the desired baud rate and returns the calculated baud rate in bits-per-second. It requires the caller to provide the frequency of the module source clock (in Hertz). Note that the baud rate does not go into effect until the Transmit Control Register (TCR) is programmed with the prescale value. Hence, this function returns the prescale tcrPrescaleValue parameter for later programming in the TCR. The higher level peripheral driver should alert the user of an out of range baud rate input.

Note that the LPSPI module must first be disabled before configuring this. Note that the LPSPI module must be configured for master mode before configuring this.

Parameters

|                          |                                                   |
|--------------------------|---------------------------------------------------|
| <i>base</i>              | LPSPI peripheral address.                         |
| <i>baudRate_Bps</i>      | The desired baud rate in bits per second.         |
| <i>srcClock_Hz</i>       | Module source input clock in Hertz.               |
| <i>tcrPrescale-Value</i> | The TCR prescale value needed to program the TCR. |

Returns

The actual calculated baud rate. This function may also return a "0" if the LPSPI is not configured for master mode or if the LPSPI module is not disabled.

#### 24.2.8.31 `void LPSPI_MasterSetDelayScaler ( LPSPI_Type * base, uint32_t scaler, lpspi_delay_type_t whichDelay )`

This function configures the following: SCK to PCS delay, or PCS to SCK delay, or The configurations must occur between the transfer delay.

The delay names are available in type lpspi\_delay\_type\_t.

The user passes the desired delay along with the delay value. This allows the user to directly set the delay values if they have pre-calculated them or if they simply wish to manually increment the value.

Note that the LPSPI module must first be disabled before configuring this. Note that the LPSPI module must be configured for master mode before configuring this.

Parameters

|                   |                                                                     |
|-------------------|---------------------------------------------------------------------|
| <i>base</i>       | LPSPI peripheral address.                                           |
| <i>scaler</i>     | The 8-bit delay value 0x00 to 0xFF (255).                           |
| <i>whichDelay</i> | The desired delay to configure, must be of type lpspi_delay_type_t. |

#### 24.2.8.32 `uint32_t LPSPI_MasterSetDelayTimes ( LPSPI_Type * base, uint32_t delayTimeInNanoSec, lpspi_delay_type_t whichDelay, uint32_t srcClock_Hz )`

This function calculates the values for the following: SCK to PCS delay, or PCS to SCK delay, or The configurations must occur between the transfer delay.

The delay names are available in type `lpspi_delay_type_t`.

The user passes the desired delay and the desired delay value in nano-seconds. The function calculates the value needed for the desired delay parameter and returns the actual calculated delay because an exact delay match may not be possible. In this case, the closest match is calculated without going below the desired delay value input. It is possible to input a very large delay value that exceeds the capability of the part, in which case the maximum supported delay is returned. It is up to the higher level peripheral driver to alert the user of an out of range delay input.

Note that the LPSPI module must be configured for master mode before configuring this. And note that the `delayTime = LPSPI_clockSource / (PRESCALE * Delay_scaler)`.

Parameters

|                                  |                                                                                             |
|----------------------------------|---------------------------------------------------------------------------------------------|
| <code>base</code>                | LPSPI peripheral address.                                                                   |
| <code>delayTimeIn-NanoSec</code> | The desired delay value in nano-seconds.                                                    |
| <code>whichDelay</code>          | The desired delay to configuration, which must be of type <code>lpspi_delay_type_t</code> . |
| <code>srcClock_Hz</code>         | Module source input clock in Hertz.                                                         |

Returns

actual Calculated delay value in nano-seconds.

#### 24.2.8.33 `static void LPSPI_WriteData ( LPSPI_Type * base, uint32_t data ) [inline], [static]`

This function writes data passed in by the user to the Transmit Data Register (TDR). The user can pass up to 32-bits of data to load into the TDR. If the frame size exceeds 32-bits, the user has to manage sending the data one 32-bit word at a time. Any writes to the TDR result in an immediate push to the transmit FIFO. This function can be used for either master or slave modes.

Parameters

|                   |                           |
|-------------------|---------------------------|
| <code>base</code> | LPSPI peripheral address. |
| <code>data</code> | The data word to be sent. |

**24.2.8.34 static uint32\_t LPSPI\_ReadData ( LPSPI\_Type \* *base* ) [inline], [static]**

This function reads the data from the Receive Data Register (RDR). This function can be used for either master or slave mode.

Parameters

|             |                           |
|-------------|---------------------------|
| <i>base</i> | LPSPI peripheral address. |
|-------------|---------------------------|

Returns

The data read from the data buffer.

#### 24.2.8.35 void LPSPI\_SetDummyData ( LPSPI\_Type \* *base*, uint8\_t *dummyData* )

Parameters

|                  |                                                                                                                                                                                                                                                 |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>      | LPSPI peripheral address.                                                                                                                                                                                                                       |
| <i>dummyData</i> | Data to be transferred when tx buffer is NULL. Note: This API has no effect when LPSPI in slave interrupt mode, because driver will set the TXMSK bit to 1 if txData is NULL, no data is loaded from transmit FIFO and output pin is tristated. |

#### 24.2.8.36 void LPSPI\_MasterTransferCreateHandle ( LPSPI\_Type \* *base*, lpspi\_master\_handle\_t \* *handle*, lpspi\_master\_transfer\_callback\_t *callback*, void \* *userData* )

This function initializes the LPSPI handle, which can be used for other LPSPI transactional APIs. Usually, for a specified LPSPI instance, call this API once to get the initialized handle.

Parameters

|                 |                                                |
|-----------------|------------------------------------------------|
| <i>base</i>     | LPSPI peripheral address.                      |
| <i>handle</i>   | LPSPI handle pointer to lpspi_master_handle_t. |
| <i>callback</i> | DSPI callback.                                 |
| <i>userData</i> | callback function parameter.                   |

#### 24.2.8.37 status\_t LPSPI\_MasterTransferBlocking ( LPSPI\_Type \* *base*, lpspi\_transfer\_t \* *transfer* )

This function transfers data using a polling method. This is a blocking function, which does not return until all transfers have been completed.

Note: The transfer data size should be integer multiples of bytesPerFrame if bytesPerFrame is less than or equal to 4. For bytesPerFrame greater than 4: The transfer data size should be equal to bytesPerFrame if the bytesPerFrame is not integer multiples of 4. Otherwise, the transfer data size can be an integer multiple of bytesPerFrame.

Parameters

|                 |                                                        |
|-----------------|--------------------------------------------------------|
| <i>base</i>     | LPSPI peripheral address.                              |
| <i>transfer</i> | pointer to <a href="#">lpspi_transfer_t</a> structure. |

Returns

status of status\_t.

#### 24.2.8.38 status\_t LPSPI\_MasterTransferNonBlocking ( LPSPI\_Type \* *base*,                   lpspi\_master\_handle\_t \* *handle*, lpspi\_transfer\_t \* *transfer* )

This function transfers data using an interrupt method. This is a non-blocking function, which returns right away. When all data is transferred, the callback function is called.

Note: The transfer data size should be integer multiples of bytesPerFrame if bytesPerFrame is less than or equal to 4. For bytesPerFrame greater than 4: The transfer data size should be equal to bytesPerFrame if the bytesPerFrame is not integer multiples of 4. Otherwise, the transfer data size can be an integer multiple of bytesPerFrame.

Parameters

|                 |                                                                             |
|-----------------|-----------------------------------------------------------------------------|
| <i>base</i>     | LPSPI peripheral address.                                                   |
| <i>handle</i>   | pointer to lpspi_master_handle_t structure which stores the transfer state. |
| <i>transfer</i> | pointer to <a href="#">lpspi_transfer_t</a> structure.                      |

Returns

status of status\_t.

#### 24.2.8.39 status\_t LPSPI\_MasterTransferGetCount ( LPSPI\_Type \* *base*,                   lpspi\_master\_handle\_t \* *handle*, size\_t \* *count* )

This function gets the master transfer remaining bytes.

Parameters

|               |                                                                                          |
|---------------|------------------------------------------------------------------------------------------|
| <i>base</i>   | LPSPI peripheral address.                                                                |
| <i>handle</i> | pointer to <code>lpspi_master_handle_t</code> structure which stores the transfer state. |
| <i>count</i>  | Number of bytes transferred so far by the non-blocking transaction.                      |

Returns

status of `status_t`.

#### 24.2.8.40 void LPSPI\_MasterTransferAbort ( `LPSPI_Type * base`, `lpspi_master_handle_t * handle` )

This function aborts a transfer which uses an interrupt method.

Parameters

|               |                                                                                          |
|---------------|------------------------------------------------------------------------------------------|
| <i>base</i>   | LPSPI peripheral address.                                                                |
| <i>handle</i> | pointer to <code>lpspi_master_handle_t</code> structure which stores the transfer state. |

#### 24.2.8.41 void LPSPI\_MasterTransferHandleIRQ ( `LPSPI_Type * base`, `lpspi_master_handle_t * handle` )

This function processes the LPSPI transmit and receive IRQ.

Parameters

|               |                                                                                          |
|---------------|------------------------------------------------------------------------------------------|
| <i>base</i>   | LPSPI peripheral address.                                                                |
| <i>handle</i> | pointer to <code>lpspi_master_handle_t</code> structure which stores the transfer state. |

#### 24.2.8.42 void LPSPI\_SlaveTransferCreateHandle ( `LPSPI_Type * base`, `lpspi_slave_handle_t * handle`, `lpspi_slave_transfer_callback_t callback`, `void * userData` )

This function initializes the LPSPI handle, which can be used for other LPSPI transactional APIs. Usually, for a specified LPSPI instance, call this API once to get the initialized handle.

Parameters

|                 |                                                             |
|-----------------|-------------------------------------------------------------|
| <i>base</i>     | LPSPI peripheral address.                                   |
| <i>handle</i>   | LPSPI handle pointer to <code>lpspi_slave_handle_t</code> . |
| <i>callback</i> | DSPI callback.                                              |
| <i>userData</i> | callback function parameter.                                |

#### 24.2.8.43 `status_t LPSPI_SlaveTransferNonBlocking ( LPSPI_Type * base, lpspi_slave_handle_t * handle, lpspi_transfer_t * transfer )`

This function transfer data using an interrupt method. This is a non-blocking function, which returns right away. When all data is transferred, the callback function is called.

Note: The transfer data size should be integer multiples of bytesPerFrame if bytesPerFrame is less than or equal to 4. For bytesPerFrame greater than 4: The transfer data size should be equal to bytesPerFrame if the bytesPerFrame is not an integer multiple of 4. Otherwise, the transfer data size can be an integer multiple of bytesPerFrame.

Parameters

|                 |                                                                                         |
|-----------------|-----------------------------------------------------------------------------------------|
| <i>base</i>     | LPSPI peripheral address.                                                               |
| <i>handle</i>   | pointer to <code>lpspi_slave_handle_t</code> structure which stores the transfer state. |
| <i>transfer</i> | pointer to <code>lpspi_transfer_t</code> structure.                                     |

Returns

status of `status_t`.

#### 24.2.8.44 `status_t LPSPI_SlaveTransferGetCount ( LPSPI_Type * base, lpspi_slave_handle_t * handle, size_t * count )`

This function gets the slave transfer remaining bytes.

Parameters

|               |                                                                                         |
|---------------|-----------------------------------------------------------------------------------------|
| <i>base</i>   | LPSPI peripheral address.                                                               |
| <i>handle</i> | pointer to <code>lpspi_slave_handle_t</code> structure which stores the transfer state. |
| <i>count</i>  | Number of bytes transferred so far by the non-blocking transaction.                     |

Returns

status of `status_t`.

**24.2.8.45 void LPSPI\_SlaveTransferAbort ( LPSPI\_Type \* *base*, Ispspi\_slave\_handle\_t \* *handle* )**

This function aborts a transfer which uses an interrupt method.

Parameters

|               |                                                                            |
|---------------|----------------------------------------------------------------------------|
| <i>base</i>   | LPSPI peripheral address.                                                  |
| <i>handle</i> | pointer to lpspi_slave_handle_t structure which stores the transfer state. |

#### 24.2.8.46 void LPSPI\_SlaveTransferHandleIRQ ( LPSPI\_Type \* *base*, lpspi\_slave\_handle\_t \* *handle* )

This function processes the LPSPI transmit and receives an IRQ.

Parameters

|               |                                                                            |
|---------------|----------------------------------------------------------------------------|
| <i>base</i>   | LPSPI peripheral address.                                                  |
| <i>handle</i> | pointer to lpspi_slave_handle_t structure which stores the transfer state. |

### 24.2.9 Variable Documentation

#### 24.2.9.1 volatile uint8\_t g\_lpspiDummyData[]

# Chapter 25

## LPTMR: Low-Power Timer

### 25.1 Overview

The MCUXpresso SDK provides a driver for the Low-Power Timer (LPTMR) of MCUXpresso SDK devices.

### 25.2 Function groups

The LPTMR driver supports operating the module as a time counter or as a pulse counter.

#### 25.2.1 Initialization and deinitialization

The function [LPTMR\\_Init\(\)](#) initializes the LPTMR with specified configurations. The function [LPTMR\\_GetDefaultConfig\(\)](#) gets the default configurations. The initialization function configures the LPTMR for a timer or a pulse counter mode mode. It also sets up the LPTMR's free running mode operation and a clock source.

The function [LPTMR\\_DeInit\(\)](#) disables the LPTMR module and gates the module clock.

#### 25.2.2 Timer period Operations

The function [LPTMR\\_SetTimerPeriod\(\)](#) sets the timer period in units of count. Timers counts from 0 to the count value set here.

The function [LPTMR\\_GetCurrentTimerCount\(\)](#) reads the current timer counting value. This function returns the real-time timer counting value ranging from 0 to a timer period.

The timer period operation function takes the count value in ticks. Call the utility macros provided in the `fsl_common.h` file to convert to microseconds or milliseconds.

#### 25.2.3 Start and Stop timer operations

The function [LPTMR\\_StartTimer\(\)](#) starts the timer counting. After calling this function, the timer counts up to the counter value set earlier by using the [LPTMR\\_SetPeriod\(\)](#) function. Each time the timer reaches the count value and increments, it generates a trigger pulse and sets the timeout interrupt flag. An interrupt is also triggered if the timer interrupt is enabled.

The function [LPTMR\\_StopTimer\(\)](#) stops the timer counting and resets the timer's counter register.

## 25.2.4 Status

Provides functions to get and clear the LPTMR status.

## 25.2.5 Interrupt

Provides functions to enable/disable LPTMR interrupts and get the currently enabled interrupts.

## 25.3 Typical use case

### 25.3.1 LPTMR tick example

Updates the LPTMR period and toggles an LED periodically. Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/lptmr

## Data Structures

- struct [lptmr\\_config\\_t](#)  
*LPTMR config structure.* [More...](#)

## Enumerations

- enum [lptmr\\_pin\\_select\\_t](#) {
   
   kLPTMR\_PinSelectInput\_0 = 0x0U,
   
   kLPTMR\_PinSelectInput\_1 = 0x1U,
   
   kLPTMR\_PinSelectInput\_2 = 0x2U,
   
   kLPTMR\_PinSelectInput\_3 = 0x3U }
   
*LPTMR pin selection used in pulse counter mode.*
- enum [lptmr\\_pin\\_polarity\\_t](#) {
   
   kLPTMR\_PinPolarityActiveHigh = 0x0U,
   
   kLPTMR\_PinPolarityActiveLow = 0x1U }
   
*LPTMR pin polarity used in pulse counter mode.*
- enum [lptmr\\_timer\\_mode\\_t](#) {
   
   kLPTMR\_TimerModeTimeCounter = 0x0U,
   
   kLPTMR\_TimerModePulseCounter = 0x1U }
   
*LPTMR timer mode selection.*
- enum [lptmr\\_prescaler\\_glitch\\_value\\_t](#) {

```

kLPTMR_Prescale_Glitch_0 = 0x0U,
kLPTMR_Prescale_Glitch_1 = 0x1U,
kLPTMR_Prescale_Glitch_2 = 0x2U,
kLPTMR_Prescale_Glitch_3 = 0x3U,
kLPTMR_Prescale_Glitch_4 = 0x4U,
kLPTMR_Prescale_Glitch_5 = 0x5U,
kLPTMR_Prescale_Glitch_6 = 0x6U,
kLPTMR_Prescale_Glitch_7 = 0x7U,
kLPTMR_Prescale_Glitch_8 = 0x8U,
kLPTMR_Prescale_Glitch_9 = 0x9U,
kLPTMR_Prescale_Glitch_10 = 0xAU,
kLPTMR_Prescale_Glitch_11 = 0xBU,
kLPTMR_Prescale_Glitch_12 = 0xCU,
kLPTMR_Prescale_Glitch_13 = 0xDU,
kLPTMR_Prescale_Glitch_14 = 0xEU,
kLPTMR_Prescale_Glitch_15 = 0xFU }

```

*LPTMR prescaler/glitch filter values.*

- enum lptmr\_prescaler\_clock\_select\_t {
 kLPTMR\_PrescalerClock\_0 = 0x0U,
 kLPTMR\_PrescalerClock\_1 = 0x1U,
 kLPTMR\_PrescalerClock\_2 = 0x2U,
 kLPTMR\_PrescalerClock\_3 = 0x3U }

*LPTMR prescaler/glitch filter clock select.*

- enum lptmr\_interrupt\_enable\_t { kLPTMR\_TimerInterruptEnable = LPTMR\_CSR\_TIE\_MASK }
- List of the LPTMR interrupts.*
- enum lptmr\_status\_flags\_t { kLPTMR\_TimerCompareFlag = LPTMR\_CSR\_TCF\_MASK }
- List of the LPTMR status flags.*

## Functions

- static void LPTMR\_EnableTimerDMA (LPTMR\_Type \*base, bool enable)  
*Enable or disable timer DMA request.*

## Driver version

- #define FSL\_LPTMR\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 1))  
*Version 2.1.1.*

## Initialization and deinitialization

- void LPTMR\_Init (LPTMR\_Type \*base, const lptmr\_config\_t \*config)  
*Ungates the LPTMR clock and configures the peripheral for a basic operation.*
- void LPTMR\_Deinit (LPTMR\_Type \*base)  
*Gates the LPTMR clock.*
- void LPTMR\_GetDefaultConfig (lptmr\_config\_t \*config)  
*Fills in the LPTMR configuration structure with default settings.*

## Interrupt Interface

- static void [LPTMR\\_EnableInterrupts](#) (LPTMR\_Type \*base, uint32\_t mask)  
*Enables the selected LPTMR interrupts.*
- static void [LPTMR\\_DisableInterrupts](#) (LPTMR\_Type \*base, uint32\_t mask)  
*Disables the selected LPTMR interrupts.*
- static uint32\_t [LPTMR\\_GetEnabledInterrupts](#) (LPTMR\_Type \*base)  
*Gets the enabled LPTMR interrupts.*

## Status Interface

- static uint32\_t [LPTMR\\_GetStatusFlags](#) (LPTMR\_Type \*base)  
*Gets the LPTMR status flags.*
- static void [LPTMR\\_ClearStatusFlags](#) (LPTMR\_Type \*base, uint32\_t mask)  
*Clears the LPTMR status flags.*

## Read and write the timer period

- static void [LPTMR\\_SetTimerPeriod](#) (LPTMR\_Type \*base, uint32\_t ticks)  
*Sets the timer period in units of count.*
- static uint32\_t [LPTMR\\_GetCurrentTimerCount](#) (LPTMR\_Type \*base)  
*Reads the current timer counting value.*

## Timer Start and Stop

- static void [LPTMR\\_StartTimer](#) (LPTMR\_Type \*base)  
*Starts the timer.*
- static void [LPTMR\\_StopTimer](#) (LPTMR\_Type \*base)  
*Stops the timer.*

## 25.4 Data Structure Documentation

### 25.4.1 struct lptmr\_config\_t

This structure holds the configuration settings for the LPTMR peripheral. To initialize this structure to reasonable defaults, call the [LPTMR\\_GetDefaultConfig\(\)](#) function and pass a pointer to your configuration structure instance.

The configuration struct can be made constant so it resides in flash.

## Data Fields

- [lptmr\\_timer\\_mode\\_t timerMode](#)  
*Time counter mode or pulse counter mode.*
- [lptmr\\_pin\\_select\\_t pinSelect](#)  
*LPTMR pulse input pin select; used only in pulse counter mode.*
- [lptmr\\_pin\\_polarity\\_t pinPolarity](#)  
*LPTMR pulse input pin polarity; used only in pulse counter mode.*
- bool [enableFreeRunning](#)

*True: enable free running, counter is reset on overflow False: counter is reset when the compare flag is set.*

- bool [bypassPrescaler](#)  
*True: bypass prescaler; false: use clock from prescaler.*
- [lptmr\\_prescaler\\_clock\\_select\\_t prescalerClockSource](#)  
*LPTMR clock source.*
- [lptmr\\_prescaler\\_glitch\\_value\\_t value](#)  
*Prescaler or glitch filter value.*

## 25.5 Enumeration Type Documentation

### 25.5.1 enum lptmr\_pin\_select\_t

Enumerator

***kLPTMR\_PinSelectInput\_0*** Pulse counter input 0 is selected.

***kLPTMR\_PinSelectInput\_1*** Pulse counter input 1 is selected.

***kLPTMR\_PinSelectInput\_2*** Pulse counter input 2 is selected.

***kLPTMR\_PinSelectInput\_3*** Pulse counter input 3 is selected.

### 25.5.2 enum lptmr\_pin\_polarity\_t

Enumerator

***kLPTMR\_PinPolarityActiveHigh*** Pulse Counter input source is active-high.

***kLPTMR\_PinPolarityActiveLow*** Pulse Counter input source is active-low.

### 25.5.3 enum lptmr\_timer\_mode\_t

Enumerator

***kLPTMR\_TimerModeTimeCounter*** Time Counter mode.

***kLPTMR\_TimerModePulseCounter*** Pulse Counter mode.

### 25.5.4 enum lptmr\_prescaler\_glitch\_value\_t

Enumerator

***kLPTMR\_Prescale\_Glitch\_0*** Prescaler divide 2, glitch filter does not support this setting.

***kLPTMR\_Prescale\_Glitch\_1*** Prescaler divide 4, glitch filter 2.

***kLPTMR\_Prescale\_Glitch\_2*** Prescaler divide 8, glitch filter 4.

***kLPTMR\_Prescale\_Glitch\_3*** Prescaler divide 16, glitch filter 8.

***kLPTMR\_Prescale\_Glitch\_4*** Prescaler divide 32, glitch filter 16.

- kLPTMR\_Prescale\_Glitch\_5* Prescaler divide 64, glitch filter 32.
- kLPTMR\_Prescale\_Glitch\_6* Prescaler divide 128, glitch filter 64.
- kLPTMR\_Prescale\_Glitch\_7* Prescaler divide 256, glitch filter 128.
- kLPTMR\_Prescale\_Glitch\_8* Prescaler divide 512, glitch filter 256.
- kLPTMR\_Prescale\_Glitch\_9* Prescaler divide 1024, glitch filter 512.
- kLPTMR\_Prescale\_Glitch\_10* Prescaler divide 2048 glitch filter 1024.
- kLPTMR\_Prescale\_Glitch\_11* Prescaler divide 4096, glitch filter 2048.
- kLPTMR\_Prescale\_Glitch\_12* Prescaler divide 8192, glitch filter 4096.
- kLPTMR\_Prescale\_Glitch\_13* Prescaler divide 16384, glitch filter 8192.
- kLPTMR\_Prescale\_Glitch\_14* Prescaler divide 32768, glitch filter 16384.
- kLPTMR\_Prescale\_Glitch\_15* Prescaler divide 65536, glitch filter 32768.

### 25.5.5 enum lptmr\_prescaler\_clock\_select\_t

Note

Clock connections are SoC-specific

Enumerator

- kLPTMR\_PrescalerClock\_0* Prescaler/glitch filter clock 0 selected.
- kLPTMR\_PrescalerClock\_1* Prescaler/glitch filter clock 1 selected.
- kLPTMR\_PrescalerClock\_2* Prescaler/glitch filter clock 2 selected.
- kLPTMR\_PrescalerClock\_3* Prescaler/glitch filter clock 3 selected.

### 25.5.6 enum lptmr\_interrupt\_enable\_t

Enumerator

*kLPTMR\_TimerInterruptEnable* Timer interrupt enable.

### 25.5.7 enum lptmr\_status\_flags\_t

Enumerator

*kLPTMR\_TimerCompareFlag* Timer compare flag.

## 25.6 Function Documentation

### 25.6.1 void LPTMR\_Init ( LPTMR\_Type \* *base*, const lptmr\_config\_t \* *config* )

## Note

This API should be called at the beginning of the application using the LPTMR driver.

## Parameters

|               |                                                 |
|---------------|-------------------------------------------------|
| <i>base</i>   | LPTMR peripheral base address                   |
| <i>config</i> | A pointer to the LPTMR configuration structure. |

**25.6.2 void LPTMR\_Deinit ( LPTMR\_Type \* *base* )**

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LPTMR peripheral base address |
|-------------|-------------------------------|

**25.6.3 void LPTMR\_GetDefaultConfig ( lptmr\_config\_t \* *config* )**

The default values are as follows.

```
* config->timerMode = kLPTMR_TimerModeTimeCounter;
* config->pinSelect = kLPTMR_PinSelectInput_0;
* config->pinPolarity = kLPTMR_PinPolarityActiveHigh;
* config->enableFreeRunning = false;
* config->bypassPrescaler = true;
* config->prescalerClockSource = kLPTMR_PrescalerClock_1;
* config->value = kLPTMR_Prescale_Glitch_0;
*
```

## Parameters

|               |                                                 |
|---------------|-------------------------------------------------|
| <i>config</i> | A pointer to the LPTMR configuration structure. |
|---------------|-------------------------------------------------|

**25.6.4 static void LPTMR\_EnableInterrupts ( LPTMR\_Type \* *base*, uint32\_t *mask* )  
[inline], [static]**

## Parameters

|             |                                                                                                                       |
|-------------|-----------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | LPTMR peripheral base address                                                                                         |
| <i>mask</i> | The interrupts to enable. This is a logical OR of members of the enumeration <a href="#">lptmr_interrupt_enable_t</a> |

### 25.6.5 static void LPTMR\_DisableInterrupts ( LPTMR\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

|             |                                                                                                                          |
|-------------|--------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | LPTMR peripheral base address                                                                                            |
| <i>mask</i> | The interrupts to disable. This is a logical OR of members of the enumeration <a href="#">lptmr_interrupt_enable_t</a> . |

### 25.6.6 static uint32\_t LPTMR\_GetEnabledInterrupts ( LPTMR\_Type \* *base* ) [inline], [static]

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LPTMR peripheral base address |
|-------------|-------------------------------|

Returns

The enabled interrupts. This is the logical OR of members of the enumeration [lptmr\\_interrupt\\_enable\\_t](#)

### 25.6.7 static void LPTMR\_EnableTimerDMA ( LPTMR\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                                                                  |
|---------------|----------------------------------------------------------------------------------|
| <i>base</i>   | base LPTMR peripheral base address                                               |
| <i>enable</i> | Switcher of timer DMA feature. "true" means to enable, "false" means to disable. |

### 25.6.8 static uint32\_t LPTMR\_GetStatusFlags ( LPTMR\_Type \* *base* ) [inline], [static]

Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LPTMR peripheral base address |
|-------------|-------------------------------|

Returns

The status flags. This is the logical OR of members of the enumeration [lptmr\\_status\\_flags\\_t](#)

### 25.6.9 static void LPTMR\_ClearStatusFlags ( LPTMR\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

|             |                                                                                                                      |
|-------------|----------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | LPTMR peripheral base address                                                                                        |
| <i>mask</i> | The status flags to clear. This is a logical OR of members of the enumeration <a href="#">lptmr_status_flags_t</a> . |

### 25.6.10 static void LPTMR\_SetTimerPeriod ( LPTMR\_Type \* *base*, uint32\_t *ticks* ) [inline], [static]

Timers counts from 0 until it equals the count value set here. The count value is written to the CMR register.

Note

1. The TCF flag is set with the CNR equals the count provided here and then increments.
2. Call the utility macros provided in the `fsl_common.h` to convert to ticks.

Parameters

|              |                                                                            |
|--------------|----------------------------------------------------------------------------|
| <i>base</i>  | LPTMR peripheral base address                                              |
| <i>ticks</i> | A timer period in units of ticks, which should be equal or greater than 1. |

### 25.6.11 static uint32\_t LPTMR\_GetCurrentTimerCount ( LPTMR\_Type \* *base* ) [inline], [static]

This function returns the real-time timer counting value in a range from 0 to a timer period.

## Note

Call the utility macros provided in the fsl\_common.h to convert ticks to usec or msec.

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LPTMR peripheral base address |
|-------------|-------------------------------|

## Returns

The current counter value in ticks

**25.6.12 static void LPTMR\_StartTimer ( LPTMR\_Type \* *base* ) [inline],  
[static]**

After calling this function, the timer counts up to the CMR register value. Each time the timer reaches the CMR value and then increments, it generates a trigger pulse and sets the timeout interrupt flag. An interrupt is also triggered if the timer interrupt is enabled.

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LPTMR peripheral base address |
|-------------|-------------------------------|

**25.6.13 static void LPTMR\_StopTimer ( LPTMR\_Type \* *base* ) [inline],  
[static]**

This function stops the timer and resets the timer's counter register.

## Parameters

|             |                               |
|-------------|-------------------------------|
| <i>base</i> | LPTMR peripheral base address |
|-------------|-------------------------------|

## Chapter 26

# LPUART: Low Power Universal Asynchronous Receiver-/Transmitter Driver

### 26.1 Overview

#### Modules

- LPUART Driver

## 26.2 LPUART Driver

### 26.2.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Low Power UART (LPUART) module of MCUXpresso SDK devices.

### 26.2.2 Typical use case

#### 26.2.2.1 LPUART Operation

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/lpuart

## Data Structures

- struct [lpuart\\_config\\_t](#)  
*LPUART configuration structure. [More...](#)*
- struct [lpuart\\_transfer\\_t](#)  
*LPUART transfer structure. [More...](#)*
- struct [lpuart\\_handle\\_t](#)  
*LPUART handle structure. [More...](#)*

## Macros

- #define [UART\\_RETRY\\_TIMES](#) 0U /\* Defining to zero means to keep waiting for the flag until it is assert/deassert. \*/  
*Retry times for waiting flag.*

## Typedefs

- typedef void(\* [lpuart\\_transfer\\_callback\\_t](#))(LPUART\_Type \*base, lpuart\_handle\_t \*handle, [status\\_t](#) status, void \*userData)  
*LPUART transfer callback function.*

## Enumerations

- enum {
   
kStatus\_LPUART\_TxBusy = MAKE\_STATUS(kStatusGroup\_LPUART, 0),
   
kStatus\_LPUART\_RxBusy = MAKE\_STATUS(kStatusGroup\_LPUART, 1),
   
kStatus\_LPUART\_TxIdle = MAKE\_STATUS(kStatusGroup\_LPUART, 2),
   
kStatus\_LPUART\_RxIdle = MAKE\_STATUS(kStatusGroup\_LPUART, 3),
   
kStatus\_LPUART\_TxWatermarkTooLarge = MAKE\_STATUS(kStatusGroup\_LPUART, 4),
   
kStatus\_LPUART\_RxWatermarkTooLarge = MAKE\_STATUS(kStatusGroup\_LPUART, 5),
   
kStatus\_LPUART\_FlagCannotClearManually = MAKE\_STATUS(kStatusGroup\_LPUART, 6),
   
kStatus\_LPUART\_Error = MAKE\_STATUS(kStatusGroup\_LPUART, 7),
   
kStatus\_LPUART\_RxRingBufferOverrun,
   
kStatus\_LPUART\_RxHardwareOverrun = MAKE\_STATUS(kStatusGroup\_LPUART, 9),
   
kStatus\_LPUART\_NoiseError = MAKE\_STATUS(kStatusGroup\_LPUART, 10),
   
kStatus\_LPUART\_FramingError = MAKE\_STATUS(kStatusGroup\_LPUART, 11),
   
kStatus\_LPUART\_ParityError = MAKE\_STATUS(kStatusGroup\_LPUART, 12),
   
kStatus\_LPUART\_BaudrateNotSupport,
   
kStatus\_LPUART\_IdleLineDetected = MAKE\_STATUS(kStatusGroup\_LPUART, 14),
   
kStatus\_LPUART\_Timeout = MAKE\_STATUS(kStatusGroup\_LPUART, 15) }

*Error codes for the LPUART driver.*

- enum `lpuart_parity_mode_t` {
   
kLPUART\_ParityDisabled = 0x0U,
   
kLPUART\_ParityEven = 0x2U,
   
kLPUART\_ParityOdd = 0x3U }
- LPUART parity mode.*
- enum `lpuart_data_bits_t` {
   
kLPUART\_EightDataBits = 0x0U,
   
kLPUART\_SevenDataBits = 0x1U }
- LPUART data bits count.*
- enum `lpuart_stop_bit_count_t` {
   
kLPUART\_OneStopBit = 0U,
   
kLPUART\_TwoStopBit = 1U }
- LPUART stop bit count.*
- enum `lpuart_transmit_cts_source_t` {
   
kLPUART\_CtsSourcePin = 0U,
   
kLPUART\_CtsSourceMatchResult = 1U }
- LPUART transmit CTS source.*
- enum `lpuart_transmit_cts_config_t` {
   
kLPUART\_CtsSampleAtStart = 0U,
   
kLPUART\_CtsSampleAtIdle = 1U }
- LPUART transmit CTS configure.*
- enum `lpuart_idle_type_select_t` {
   
kLPUART\_IdleTypeStartBit = 0U,
   
kLPUART\_IdleTypeStopBit = 1U }
- LPUART idle flag type defines when the receiver starts counting.*
- enum `lpuart_idle_config_t` {

```
kLPUART_IdleCharacter1 = 0U,
kLPUART_IdleCharacter2 = 1U,
kLPUART_IdleCharacter4 = 2U,
kLPUART_IdleCharacter8 = 3U,
kLPUART_IdleCharacter16 = 4U,
kLPUART_IdleCharacter32 = 5U,
kLPUART_IdleCharacter64 = 6U,
kLPUART_IdleCharacter128 = 7U }
```

*LPUART idle detected configuration.*

- enum \_lpuart\_interrupt\_enable {

```
kLPUART_LinBreakInterruptEnable = (LPUART_BAUD_LBKDIIE_MASK >> 8U),
kLPUART_RxActiveEdgeInterruptEnable = (LPUART_BAUD_RXEDGIE_MASK >> 8U),
kLPUART_TxDataRegEmptyInterruptEnable = (LPUART_CTRL_TIE_MASK),
kLPUART_TransmissionCompleteInterruptEnable = (LPUART_CTRL_TCIE_MASK),
kLPUART_RxDataRegFullInterruptEnable = (LPUART_CTRL_RIE_MASK),
kLPUART_IdleLineInterruptEnable = (LPUART_CTRL_ILIE_MASK),
kLPUART_RxOverrunInterruptEnable = (LPUART_CTRL_ORIE_MASK),
kLPUART_NoiseErrorInterruptEnable = (LPUART_CTRL_NEIE_MASK),
kLPUART_FramingErrorInterruptEnable = (LPUART_CTRL_FEIE_MASK),
kLPUART_ParityErrorInterruptEnable = (LPUART_CTRL_PEIE_MASK),
kLPUART_Match1InterruptEnable = (LPUART_CTRL_MA1IE_MASK),
kLPUART_Match2InterruptEnable = (LPUART_CTRL_MA2IE_MASK),
kLPUART_TxFifoOverflowInterruptEnable = (LPUART_FIFO_TXOFE_MASK),
kLPUART_RxFifoUnderflowInterruptEnable = (LPUART_FIFO_RXUFE_MASK) }
```

*LPUART interrupt configuration structure, default settings all disabled.*

- enum \_lpuart\_flags {

```
kLPUART_TxDataRegEmptyFlag,
kLPUART_TransmissionCompleteFlag,
kLPUART_RxDataRegFullFlag = (LPUART_STAT_RDRF_MASK),
kLPUART_IdleLineFlag = (LPUART_STAT_IDLE_MASK),
kLPUART_RxOverrunFlag = (LPUART_STAT_OR_MASK),
kLPUART_NoiseErrorFlag = (LPUART_STAT_NF_MASK),
kLPUART_FramingErrorFlag,
kLPUART_ParityErrorFlag = (LPUART_STAT_PF_MASK),
kLPUART_LinBreakFlag = (LPUART_STAT_LBKDIF_MASK),
kLPUART_RxActiveEdgeFlag = (LPUART_STAT_RXEDGIF_MASK),
kLPUART_RxActiveFlag,
kLPUART_DataMatch1Flag,
kLPUART_DataMatch2Flag,
kLPUART_TxFifoEmptyFlag,
kLPUART_RxFifoEmptyFlag,
kLPUART_TxFifoOverflowFlag,
kLPUART_RxFifoUnderflowFlag }
```

*LPUART status flags.*

## Driver version

- `#define FSL_LPUART_DRIVER_VERSION (MAKE_VERSION(2, 5, 2))`  
*LPUART driver version.*

## Software Reset

- `static void LPUART_SoftwareReset (LPUART_Type *base)`  
*Resets the LPUART using software.*

## Initialization and deinitialization

- `status_t LPUART_Init (LPUART_Type *base, const lpuart_config_t *config, uint32_t srcClock_Hz)`  
*Initializes an LPUART instance with the user configuration structure and the peripheral clock.*
- `void LPUART_Deinit (LPUART_Type *base)`  
*Deinitializes a LPUART instance.*
- `void LPUART_GetDefaultConfig (lpuart_config_t *config)`  
*Gets the default configuration structure.*

## Module configuration

- `status_t LPUART_SetBaudRate (LPUART_Type *base, uint32_t baudRate_Bps, uint32_t srcClock_Hz)`  
*Sets the LPUART instance baudrate.*
- `void LPUART_Enable9bitMode (LPUART_Type *base, bool enable)`  
*Enable 9-bit data mode for LPUART.*
- `static void LPUART_SetMatchAddress (LPUART_Type *base, uint16_t address1, uint16_t address2)`  
*Set the LPUART address.*
- `static void LPUART_EnableMatchAddress (LPUART_Type *base, bool match1, bool match2)`  
*Enable the LPUART match address feature.*
- `static void LPUART_SetRxFifoWatermark (LPUART_Type *base, uint8_t water)`  
*Sets the rx FIFO watermark.*
- `static void LPUART_SetTxFifoWatermark (LPUART_Type *base, uint8_t water)`  
*Sets the tx FIFO watermark.*

## Status

- `uint32_t LPUART_GetStatusFlags (LPUART_Type *base)`  
*Gets LPUART status flags.*
- `status_t LPUART_ClearStatusFlags (LPUART_Type *base, uint32_t mask)`  
*Clears status flags with a provided mask.*

## Interrupts

- void [LPUART\\_EnableInterrupts](#) (LPUART\_Type \*base, uint32\_t mask)  
*Enables LPUART interrupts according to a provided mask.*
- void [LPUART\\_DisableInterrupts](#) (LPUART\_Type \*base, uint32\_t mask)  
*Disables LPUART interrupts according to a provided mask.*
- uint32\_t [LPUART\\_GetEnabledInterrupts](#) (LPUART\_Type \*base)  
*Gets enabled LPUART interrupts.*

## DMA Configuration

- static uint32\_t [LPUART\\_GetDataRegisterAddress](#) (LPUART\_Type \*base)  
*Gets the LPUART data register address.*
- static void [LPUART\\_EnableTxDMA](#) (LPUART\_Type \*base, bool enable)  
*Enables or disables the LPUART transmitter DMA request.*
- static void [LPUART\\_EnableRxDMA](#) (LPUART\_Type \*base, bool enable)  
*Enables or disables the LPUART receiver DMA.*

## Bus Operations

- uint32\_t [LPUARTGetInstance](#) (LPUART\_Type \*base)  
*Get the LPUART instance from peripheral base address.*
- static void [LPUART\\_EnableTx](#) (LPUART\_Type \*base, bool enable)  
*Enables or disables the LPUART transmitter.*
- static void [LPUART\\_EnableRx](#) (LPUART\_Type \*base, bool enable)  
*Enables or disables the LPUART receiver.*
- static void [LPUART\\_WriteByte](#) (LPUART\_Type \*base, uint8\_t data)  
*Writes to the transmitter register.*
- static uint8\_t [LPUART\\_ReadByte](#) (LPUART\_Type \*base)  
*Reads the receiver register.*
- static uint8\_t [LPUART\\_GetRxFifoCount](#) (LPUART\_Type \*base)  
*Gets the rx FIFO data count.*
- static uint8\_t [LPUART\\_GetTxFifoCount](#) (LPUART\_Type \*base)  
*Gets the tx FIFO data count.*
- void [LPUART\\_SendAddress](#) (LPUART\_Type \*base, uint8\_t address)  
*Transmit an address frame in 9-bit data mode.*
- status\_t [LPUART\\_WriteBlocking](#) (LPUART\_Type \*base, const uint8\_t \*data, size\_t length)  
*Writes to the transmitter register using a blocking method.*
- status\_t [LPUART\\_ReadBlocking](#) (LPUART\_Type \*base, uint8\_t \*data, size\_t length)  
*Reads the receiver data register using a blocking method.*

## Transactional

- void [LPUART\\_TransferCreateHandle](#) (LPUART\_Type \*base, lpuart\_handle\_t \*handle, [lpuart\\_transfer\\_callback\\_t](#) callback, void \*userData)  
*Initializes the LPUART handle.*

- `status_t LPUART_TransferSendNonBlocking (LPUART_Type *base, lpuart_handle_t *handle, lpuart_transfer_t *xfer)`  
*Transmits a buffer of data using the interrupt method.*
- `void LPUART_TransferStartRingBuffer (LPUART_Type *base, lpuart_handle_t *handle, uint8_t *ringBuffer, size_t ringBufferSize)`  
*Sets up the RX ring buffer.*
- `void LPUART_TransferStopRingBuffer (LPUART_Type *base, lpuart_handle_t *handle)`  
*Aborts the background transfer and uninstalls the ring buffer.*
- `size_t LPUART_TransferGetRxRingBufferLength (LPUART_Type *base, lpuart_handle_t *handle)`  
*Get the length of received data in RX ring buffer.*
- `void LPUART_TransferAbortSend (LPUART_Type *base, lpuart_handle_t *handle)`  
*Aborts the interrupt-driven data transmit.*
- `status_t LPUART_TransferGetSendCount (LPUART_Type *base, lpuart_handle_t *handle, uint32_t *count)`  
*Gets the number of bytes that have been sent out to bus.*
- `status_t LPUART_TransferReceiveNonBlocking (LPUART_Type *base, lpuart_handle_t *handle, lpuart_transfer_t *xfer, size_t *receivedBytes)`  
*Receives a buffer of data using the interrupt method.*
- `void LPUART_TransferAbortReceive (LPUART_Type *base, lpuart_handle_t *handle)`  
*Aborts the interrupt-driven data receiving.*
- `status_t LPUART_TransferGetReceiveCount (LPUART_Type *base, lpuart_handle_t *handle, uint32_t *count)`  
*Gets the number of bytes that have been received.*
- `void LPUART_TransferHandleIRQ (LPUART_Type *base, void *irqHandle)`  
*LPUART IRQ handle function.*
- `void LPUART_TransferHandleErrorIRQ (LPUART_Type *base, void *irqHandle)`  
*LPUART Error IRQ handle function.*

## 26.2.3 Data Structure Documentation

### 26.2.3.1 struct lpuart\_config\_t

#### Data Fields

- `uint32_t baudRate_Bps`  
*LPUART baud rate.*
- `lpuart_parity_mode_t parityMode`  
*Parity mode, disabled (default), even, odd.*
- `lpuart_data_bits_t dataBitsCount`  
*Data bits count, eight (default), seven.*
- `bool isMsb`  
*Data bits order, LSB (default), MSB.*
- `lpuart_stop_bit_count_t stopBitCount`  
*Number of stop bits, 1 stop bit (default) or 2 stop bits.*
- `uint8_t txFifoWatermark`  
*TX FIFO watermark.*
- `uint8_t rxFifoWatermark`

- `bool enableRxRTS`  
*RX RTS enable.*
- `bool enableTxCTS`  
*TX CTS enable.*
- `lpuart_transmit_cts_source_t txCtsSource`  
*TX CTS source.*
- `lpuart_transmit_cts_config_t txCtsConfig`  
*TX CTS configure.*
- `lpuart_idle_type_select_t rxIdleType`  
*RX IDLE type.*
- `lpuart_idle_config_t rxIdleConfig`  
*RX IDLE configuration.*
- `bool enableTx`  
*Enable TX.*
- `bool enableRx`  
*Enable RX.*

### Field Documentation

(1) `lpuart_idle_type_select_t lpuart_config_t::rxIdleType`

(2) `lpuart_idle_config_t lpuart_config_t::rxIdleConfig`

### 26.2.3.2 struct lpuart\_transfer\_t

#### Data Fields

- `size_t dataSize`  
*The byte count to be transfer.*
- `uint8_t * data`  
*The buffer of data to be transfer.*
- `uint8_t * rxData`  
*The buffer to receive data.*
- `const uint8_t * txData`  
*The buffer of data to be sent.*

### Field Documentation

(1) `uint8_t* lpuart_transfer_t::data`

(2) `uint8_t* lpuart_transfer_t::rxData`

(3) `const uint8_t* lpuart_transfer_t::txData`

(4) `size_t lpuart_transfer_t::dataSize`

### 26.2.3.3 struct \_lpuart\_handle

#### Data Fields

- const uint8\_t \*volatile **txData**  
*Address of remaining data to send.*
- volatile size\_t **txDataSize**  
*Size of the remaining data to send.*
- size\_t **txDataSizeAll**  
*Size of the data to send out.*
- uint8\_t \*volatile **rxData**  
*Address of remaining data to receive.*
- volatile size\_t **rxDataSize**  
*Size of the remaining data to receive.*
- size\_t **rxDataSizeAll**  
*Size of the data to receive.*
- uint8\_t \* **rxRingBuffer**  
*Start address of the receiver ring buffer.*
- size\_t **rxRingBufferSize**  
*Size of the ring buffer.*
- volatile uint16\_t **rxRingBufferHead**  
*Index for the driver to store received data into ring buffer.*
- volatile uint16\_t **rxRingBufferTail**  
*Index for the user to get data from the ring buffer.*
- lpuart\_transfer\_callback\_t **callback**  
*Callback function.*
- void \* **userData**  
*LPUART callback function parameter.*
- volatile uint8\_t **txState**  
*TX transfer state.*
- volatile uint8\_t **rxState**  
*RX transfer state.*
- bool **isSevenDataBits**  
*Seven data bits flag.*

#### Field Documentation

- (1) const uint8\_t\* volatile lpuart\_handle\_t::txData
- (2) volatile size\_t lpuart\_handle\_t::txDataSize
- (3) size\_t lpuart\_handle\_t::txDataSizeAll
- (4) uint8\_t\* volatile lpuart\_handle\_t::rxData
- (5) volatile size\_t lpuart\_handle\_t::rxDataSize
- (6) size\_t lpuart\_handle\_t::rxDataSizeAll
- (7) uint8\_t\* lpuart\_handle\_t::rxRingBuffer

- (8) `size_t lpuart_handle_t::rxRingBufferSize`
- (9) `volatile uint16_t lpuart_handle_t::rxRingBufferHead`
- (10) `volatile uint16_t lpuart_handle_t::rxRingBufferTail`
- (11) `lpuart_transfer_callback_t lpuart_handle_t::callback`
- (12) `void* lpuart_handle_t::userData`
- (13) `volatile uint8_t lpuart_handle_t::txState`
- (14) `volatile uint8_t lpuart_handle_t::rxState`
- (15) `bool lpuart_handle_t::isSevenDataBits`

## 26.2.4 Macro Definition Documentation

**26.2.4.1 #define FSL\_LPUART\_DRIVER\_VERSION (MAKE\_VERSION(2, 5, 2))**

**26.2.4.2 #define UART\_RETRY\_TIMES 0U /\* Defining to zero means to keep waiting for the flag until it is assert/deassert. \*/**

## 26.2.5 Typedef Documentation

**26.2.5.1 typedef void(\* lpuart\_transfer\_callback\_t)(LPUART\_Type \*base, lpuart\_handle\_t \*handle, status\_t status, void \*userData)**

## 26.2.6 Enumeration Type Documentation

### 26.2.6.1 anonymous enum

Enumerator

- kStatus\_LPUART\_TxBusy* TX busy.
- kStatus\_LPUART\_RxBusy* RX busy.
- kStatus\_LPUART\_TxIdle* LPUART transmitter is idle.
- kStatus\_LPUART\_RxIdle* LPUART receiver is idle.
- kStatus\_LPUART\_TxWatermarkTooLarge* TX FIFO watermark too large.
- kStatus\_LPUART\_RxWatermarkTooLarge* RX FIFO watermark too large.
- kStatus\_LPUART\_FlagCannotClearManually* Some flag can't manually clear.
- kStatus\_LPUART\_Error* Error happens on LPUART.
- kStatus\_LPUART\_RxRingBufferOverrun* LPUART RX software ring buffer overrun.
- kStatus\_LPUART\_RxHardwareOverrun* LPUART RX receiver overrun.
- kStatus\_LPUART\_NoiseError* LPUART noise error.
- kStatus\_LPUART\_FramingError* LPUART framing error.

*kStatus\_LPUART\_ParityError* LPUART parity error.

*kStatus\_LPUART\_BaudrateNotSupport* Baudrate is not support in current clock source.

*kStatus\_LPUART\_IdleLineDetected* IDLE flag.

*kStatus\_LPUART\_Timeout* LPUART times out.

### 26.2.6.2 enum lpuart\_parity\_mode\_t

Enumerator

*kLPUART\_ParityDisabled* Parity disabled.

*kLPUART\_ParityEven* Parity enabled, type even, bit setting: PE|PT = 10.

*kLPUART\_ParityOdd* Parity enabled, type odd, bit setting: PE|PT = 11.

### 26.2.6.3 enum lpuart\_data\_bits\_t

Enumerator

*kLPUART\_EightDataBits* Eight data bit.

*kLPUART\_SevenDataBits* Seven data bit.

### 26.2.6.4 enum lpuart\_stop\_bit\_count\_t

Enumerator

*kLPUART\_OneStopBit* One stop bit.

*kLPUART\_TwoStopBit* Two stop bits.

### 26.2.6.5 enum lpuart\_transmit\_cts\_source\_t

Enumerator

*kLPUART\_CtsSourcePin* CTS resource is the LPUART\_CTS pin.

*kLPUART\_CtsSourceMatchResult* CTS resource is the match result.

### 26.2.6.6 enum lpuart\_transmit\_cts\_config\_t

Enumerator

*kLPUART\_CtsSampleAtStart* CTS input is sampled at the start of each character.

*kLPUART\_CtsSampleAtIdle* CTS input is sampled when the transmitter is idle.

### 26.2.6.7 enum lpuart\_idle\_type\_select\_t

Enumerator

***kLPUART\_IdleTypeStartBit*** Start counting after a valid start bit.

***kLPUART\_IdleTypeStopBit*** Start counting after a stop bit.

### 26.2.6.8 enum lpuart\_idle\_config\_t

This structure defines the number of idle characters that must be received before the IDLE flag is set.

Enumerator

***kLPUART\_IdleCharacter1*** the number of idle characters.

***kLPUART\_IdleCharacter2*** the number of idle characters.

***kLPUART\_IdleCharacter4*** the number of idle characters.

***kLPUART\_IdleCharacter8*** the number of idle characters.

***kLPUART\_IdleCharacter16*** the number of idle characters.

***kLPUART\_IdleCharacter32*** the number of idle characters.

***kLPUART\_IdleCharacter64*** the number of idle characters.

***kLPUART\_IdleCharacter128*** the number of idle characters.

### 26.2.6.9 enum \_lpuart\_interrupt\_enable

This structure contains the settings for all LPUART interrupt configurations.

Enumerator

***kLPUART\_LinBreakInterruptEnable*** LIN break detect. bit 7

***kLPUART\_RxActiveEdgeInterruptEnable*** Receive Active Edge. bit 6

***kLPUART\_TxDataRegEmptyInterruptEnable*** Transmit data register empty. bit 23

***kLPUART\_TransmissionCompleteInterruptEnable*** Transmission complete. bit 22

***kLPUART\_RxDataRegFullInterruptEnable*** Receiver data register full. bit 21

***kLPUART\_IdleLineInterruptEnable*** Idle line. bit 20

***kLPUART\_RxOverrunInterruptEnable*** Receiver Overrun. bit 27

***kLPUART\_NoiseErrorInterruptEnable*** Noise error flag. bit 26

***kLPUART\_FramingErrorInterruptEnable*** Framing error flag. bit 25

***kLPUART\_ParityErrorInterruptEnable*** Parity error flag. bit 24

***kLPUART\_Match1InterruptEnable*** Parity error flag. bit 15

***kLPUART\_Match2InterruptEnable*** Parity error flag. bit 14

***kLPUART\_TxFifoOverflowInterruptEnable*** Transmit FIFO Overflow. bit 9

***kLPUART\_RxFifoUnderflowInterruptEnable*** Receive FIFO Underflow. bit 8

### 26.2.6.10 enum \_lpuart\_flags

This provides constants for the LPUART status flags for use in the LPUART functions.

Enumerator

***kLPUART\_TxDataRegEmptyFlag*** Transmit data register empty flag, sets when transmit buffer is empty. bit 23

***kLPUART\_TransmissionCompleteFlag*** Transmission complete flag, sets when transmission activity complete. bit 22

***kLPUART\_RxDataRegFullFlag*** Receive data register full flag, sets when the receive data buffer is full. bit 21

***kLPUART\_IdleLineFlag*** Idle line detect flag, sets when idle line detected. bit 20

***kLPUART\_RxOverrunFlag*** Receive Overrun, sets when new data is received before data is read from receive register. bit 19

***kLPUART\_NoiseErrorFlag*** Receive takes 3 samples of each received bit. If any of these samples differ, noise flag sets. bit 18

***kLPUART\_FramingErrorFlag*** Frame error flag, sets if logic 0 was detected where stop bit expected. bit 17

***kLPUART\_ParityErrorFlag*** If parity enabled, sets upon parity error detection. bit 16

***kLPUART\_LinBreakFlag*** LIN break detect interrupt flag, sets when LIN break char detected and LIN circuit enabled. bit 31

***kLPUART\_RxActiveEdgeFlag*** Receive pin active edge interrupt flag, sets when active edge detected. bit 30

***kLPUART\_RxActiveFlag*** Receiver Active Flag (RAF), sets at beginning of valid start. bit 24

***kLPUART\_DataMatch1Flag*** The next character to be read from LPUART\_DATA matches MA1. bit 15

***kLPUART\_DataMatch2Flag*** The next character to be read from LPUART\_DATA matches MA2. bit 14

***kLPUART\_TxFifoEmptyFlag*** TXEMPT bit, sets if transmit buffer is empty. bit 7

***kLPUART\_RxFifoEmptyFlag*** RXEMPT bit, sets if receive buffer is empty. bit 6

***kLPUART\_TxFifoOverflowFlag*** TXOF bit, sets if transmit buffer overflow occurred. bit 1

***kLPUART\_RxFifoUnderflowFlag*** RXUF bit, sets if receive buffer underflow occurred. bit 0

### 26.2.7 Function Documentation

#### 26.2.7.1 static void LPUART\_SoftwareReset ( **LPUART\_Type** \* *base* ) [inline], [static]

This function resets all internal logic and registers except the Global Register. Remains set until cleared by software.

## Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

### 26.2.7.2 status\_t LPUART\_Init ( LPUART\_Type \* *base*, const lpuart\_config\_t \* *config*, uint32\_t *srcClock\_Hz* )

This function configures the LPUART module with user-defined settings. Call the [LPUART\\_GetDefaultConfig\(\)](#) function to configure the configuration structure and get the default configuration. The example below shows how to use this API to configure the LPUART.

```
* lpuart_config_t lpuartConfig;
* lpuartConfig.baudRate_Bps = 115200U;
* lpuartConfig.parityMode = kLPUART_ParityDisabled;
* lpuartConfig.dataBitsCount = kLPUART_EightDataBits;
* lpuartConfig.isMsb = false;
* lpuartConfig.stopBitCount = kLPUART_OneStopBit;
* lpuartConfig.txFifoWatermark = 0;
* lpuartConfig.rxFifoWatermark = 1;
* LPUART_Init(LPUART1, &lpuartConfig, 20000000U);
*
```

## Parameters

|                    |                                                    |
|--------------------|----------------------------------------------------|
| <i>base</i>        | LPUART peripheral base address.                    |
| <i>config</i>      | Pointer to a user-defined configuration structure. |
| <i>srcClock_Hz</i> | LPUART clock source frequency in HZ.               |

## Return values

|                                          |                                                  |
|------------------------------------------|--------------------------------------------------|
| <i>kStatus_LPUART_BaudrateNotSupport</i> | Baudrate is not support in current clock source. |
| <i>kStatus_Success</i>                   | LPUART initialize succeed                        |

### 26.2.7.3 void LPUART\_Deinit ( LPUART\_Type \* *base* )

This function waits for transmit to complete, disables TX and RX, and disables the LPUART clock.

## Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

#### 26.2.7.4 void LPUART\_GetDefaultConfig ( lpuart\_config\_t \* *config* )

This function initializes the LPUART configuration structure to a default value. The default values are:  
: lpuartConfig->baudRate\_Bps = 115200U; lpuartConfig->parityMode = kLPUART\_ParityDisabled;  
lpuartConfig->dataBitsCount = kLPUART\_EightDataBits; lpuartConfig->isMsb = false; lpuartConfig->stopBitCount = kLPUART\_OneStopBit; lpuartConfig->txFifoWatermark = 0; lpuartConfig->rxFifoWatermark = 1; lpuartConfig->rxIdleType = kLPUART\_IdleTypeStartBit; lpuartConfig->rxIdleConfig = kLPUART\_IdleCharacter1; lpuartConfig->enableTx = false; lpuartConfig->enableRx = false;

Parameters

|               |                                       |
|---------------|---------------------------------------|
| <i>config</i> | Pointer to a configuration structure. |
|---------------|---------------------------------------|

#### 26.2.7.5 status\_t LPUART\_SetBaudRate ( LPUART\_Type \* *base*, uint32\_t *baudRate\_Bps*, uint32\_t *srcClock\_Hz* )

This function configures the LPUART module baudrate. This function is used to update the LPUART module baudrate after the LPUART module is initialized by the LPUART\_Init.

```
* LPUART_SetBaudRate(LPUART1, 115200U, 20000000U);
*
```

Parameters

|                     |                                      |
|---------------------|--------------------------------------|
| <i>base</i>         | LPUART peripheral base address.      |
| <i>baudRate_Bps</i> | LPUART baudrate to be set.           |
| <i>srcClock_Hz</i>  | LPUART clock source frequency in HZ. |

Return values

|                                          |                                                        |
|------------------------------------------|--------------------------------------------------------|
| <i>kStatus_LPUART_BaudrateNotSupport</i> | Baudrate is not supported in the current clock source. |
| <i>kStatus_Success</i>                   | Set baudrate succeeded.                                |

#### 26.2.7.6 void LPUART\_Enable9bitMode ( LPUART\_Type \* *base*, bool *enable* )

This function set the 9-bit mode for LPUART module. The 9th bit is not used for parity thus can be modified by user.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | LPUART peripheral base address.   |
| <i>enable</i> | true to enable, false to disable. |

#### 26.2.7.7 static void LPUART\_SetMatchAddress ( LPUART\_Type \* *base*, uint16\_t *address1*, uint16\_t *address2* ) [inline], [static]

This function configures the address for LPUART module that works as slave in 9-bit data mode. One or two address fields can be configured. When the address field's match enable bit is set, the frame it receives with MSB being 1 is considered as an address frame, otherwise it is considered as data frame. Once the address frame matches one of slave's own addresses, this slave is addressed. This address frame and its following data frames are stored in the receive buffer, otherwise the frames will be discarded. To un-address a slave, just send an address frame with unmatched address.

Note

Any LPUART instance joined in the multi-slave system can work as slave. The position of the address mark is the same as the parity bit when parity is enabled for 8 bit and 9 bit data formats.

Parameters

|                 |                                 |
|-----------------|---------------------------------|
| <i>base</i>     | LPUART peripheral base address. |
| <i>address1</i> | LPUART slave address1.          |
| <i>address2</i> | LPUART slave address2.          |

#### 26.2.7.8 static void LPUART\_EnableMatchAddress ( LPUART\_Type \* *base*, bool *match1*, bool *match2* ) [inline], [static]

Parameters

|               |                                                  |
|---------------|--------------------------------------------------|
| <i>base</i>   | LPUART peripheral base address.                  |
| <i>match1</i> | true to enable match address1, false to disable. |
| <i>match2</i> | true to enable match address2, false to disable. |

#### 26.2.7.9 static void LPUART\_SetRxFifoWatermark ( LPUART\_Type \* *base*, uint8\_t *water* ) [inline], [static]

Parameters

|              |                                 |
|--------------|---------------------------------|
| <i>base</i>  | LPUART peripheral base address. |
| <i>water</i> | Rx FIFO watermark.              |

### 26.2.7.10 static void LPUART\_SetTxFifoWatermark ( LPUART\_Type \* *base*, uint8\_t *water* ) [inline], [static]

Parameters

|              |                                 |
|--------------|---------------------------------|
| <i>base</i>  | LPUART peripheral base address. |
| <i>water</i> | Tx FIFO watermark.              |

### 26.2.7.11 uint32\_t LPUART\_GetStatusFlags ( LPUART\_Type \* *base* )

This function gets all LPUART status flags. The flags are returned as the logical OR value of the enumerators `_lpuart_flags`. To check for a specific status, compare the return value with enumerators in the `_lpuart_flags`. For example, to check whether the TX is empty:

```
* if (kLPUART_TxDataRegEmptyFlag &
* LPUART_GetStatusFlags(LPUART1))
* {
* ...
* }
```

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

Returns

LPUART status flags which are ORed by the enumerators in the `_lpuart_flags`.

### 26.2.7.12 status\_t LPUART\_ClearStatusFlags ( LPUART\_Type \* *base*, uint32\_t *mask* )

This function clears LPUART status flags with a provided mask. Automatically cleared flags can't be cleared by this function. Flags that can only be cleared or set by hardware are: kLPUART\_TxDataRegEmptyFlag, kLPUART\_TransmissionCompleteFlag, kLPUART\_RxDataRegFullFlag, kLPUART\_RxActiveFlag, kLPUART\_NoiseErrorInRxDataRegFlag, kLPUART\_ParityErrorInRxDataRegFlag, kLPUART\_TxFifoEmptyFlag, kLPUART\_RxFifoEmptyFlag. Note: This API should be called when the Tx/Rx is idle, otherwise it takes no effects.

## Parameters

|             |                                                                                                                                                     |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i> | LPUART peripheral base address.                                                                                                                     |
| <i>mask</i> | the status flags to be cleared. The user can use the enumerators in the <code>_lpuart_status_flag_t</code> to do the OR operation and get the mask. |

## Returns

0 succeed, others failed.

## Return values

|                                                |                                                                                         |
|------------------------------------------------|-----------------------------------------------------------------------------------------|
| <i>kStatus_LPUART_Flag_CannotClearManually</i> | The flag can't be cleared by this function but it is cleared automatically by hardware. |
| <i>kStatus_Success</i>                         | Status in the mask are cleared.                                                         |

**26.2.7.13 void LPUART\_EnableInterrupts ( LPUART\_Type \* *base*, uint32\_t *mask* )**

This function enables the LPUART interrupts according to a provided mask. The mask is a logical OR of enumeration members. See the [\\_lpuart\\_interrupt\\_enable](#). This examples shows how to enable TX empty interrupt and RX full interrupt:

```
* LPUART_EnableInterrupts(LPUART1,
 kLPUART_TxDataRegEmptyInterruptEnable |
 kLPUART_RxDataRegFullInterruptEnable);
*
```

## Parameters

|             |                                                                                               |
|-------------|-----------------------------------------------------------------------------------------------|
| <i>base</i> | LPUART peripheral base address.                                                               |
| <i>mask</i> | The interrupts to enable. Logical OR of the enumeration <code>_uart_interrupt_enable</code> . |

**26.2.7.14 void LPUART\_DisableInterrupts ( LPUART\_Type \* *base*, uint32\_t *mask* )**

This function disables the LPUART interrupts according to a provided mask. The mask is a logical OR of enumeration members. See [\\_lpuart\\_interrupt\\_enable](#). This example shows how to disable the TX empty interrupt and RX full interrupt:

```
* LPUART_DisableInterrupts(LPUART1,
 kLPUART_TxDataRegEmptyInterruptEnable |
 kLPUART_RxDataRegFullInterruptEnable);
*
```

Parameters

|             |                                                                                     |
|-------------|-------------------------------------------------------------------------------------|
| <i>base</i> | LPUART peripheral base address.                                                     |
| <i>mask</i> | The interrupts to disable. Logical OR of <a href="#">_lpuart_interrupt_enable</a> . |

### 26.2.7.15 uint32\_t LPUART\_GetEnabledInterrupts ( LPUART\_Type \* *base* )

This function gets the enabled LPUART interrupts. The enabled interrupts are returned as the logical OR value of the enumerators [\\_lpuart\\_interrupt\\_enable](#). To check a specific interrupt enable status, compare the return value with enumerators in [\\_lpuart\\_interrupt\\_enable](#). For example, to check whether the TX empty interrupt is enabled:

```
* uint32_t enabledInterrupts = LPUART_GetEnabledInterrupts(LPUART1);
*
* if (kLPUART_TxDataRegEmptyInterruptEnable & enabledInterrupts)
* {
* ...
* }
```

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

Returns

LPUART interrupt flags which are logical OR of the enumerators in [\\_lpuart\\_interrupt\\_enable](#).

### 26.2.7.16 static uint32\_t LPUART\_GetDataRegisterAddress ( LPUART\_Type \* *base* ) [inline], [static]

This function returns the LPUART data register address, which is mainly used by the DMA/eDMA.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

Returns

LPUART data register addresses which are used both by the transmitter and receiver.

### 26.2.7.17 static void LPUART\_EnableTxDMA ( LPUART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the transmit data register empty flag, STAT[TDRE], to generate DMA requests.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | LPUART peripheral base address.   |
| <i>enable</i> | True to enable, false to disable. |

#### 26.2.7.18 static void LPUART\_EnableRxDMA ( LPUART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the receiver data register full flag, STAT[RDRF], to generate DMA requests.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | LPUART peripheral base address.   |
| <i>enable</i> | True to enable, false to disable. |

#### 26.2.7.19 uint32\_t LPUART\_GetInstance ( LPUART\_Type \* *base* )

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

Returns

LPUART instance.

#### 26.2.7.20 static void LPUART\_EnableTx ( LPUART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the LPUART transmitter.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | LPUART peripheral base address.   |
| <i>enable</i> | True to enable, false to disable. |

#### 26.2.7.21 static void LPUART\_EnableRx ( LPUART\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the LPUART receiver.

Parameters

|               |                                   |
|---------------|-----------------------------------|
| <i>base</i>   | LPUART peripheral base address.   |
| <i>enable</i> | True to enable, false to disable. |

### 26.2.7.22 static void LPUART\_WriteByte ( LPUART\_Type \* *base*, uint8\_t *data* ) [inline], [static]

This function writes data to the transmitter register directly. The upper layer must ensure that the TX register is empty or that the TX FIFO has room before calling this function.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
| <i>data</i> | Data write to the TX register.  |

### 26.2.7.23 static uint8\_t LPUART\_ReadByte ( LPUART\_Type \* *base* ) [inline], [static]

This function reads data from the receiver register directly. The upper layer must ensure that the receiver register is full or that the RX FIFO has data before calling this function.

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

Returns

Data read from data register.

### 26.2.7.24 static uint8\_t LPUART\_GetRx\_fifoCount ( LPUART\_Type \* *base* ) [inline], [static]

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

Returns

rx FIFO data count.

#### 26.2.7.25 static uint8\_t LPUART\_GetTxFifoCount ( LPUART\_Type \* *base* ) [inline], [static]

Parameters

|             |                                 |
|-------------|---------------------------------|
| <i>base</i> | LPUART peripheral base address. |
|-------------|---------------------------------|

Returns

tx FIFO data count.

#### 26.2.7.26 void LPUART\_SendAddress ( LPUART\_Type \* *base*, uint8\_t *address* )

Parameters

|                |                                 |
|----------------|---------------------------------|
| <i>base</i>    | LPUART peripheral base address. |
| <i>address</i> | LPUART slave address.           |

#### 26.2.7.27 status\_t LPUART\_WriteBlocking ( LPUART\_Type \* *base*, const uint8\_t \* *data*, size\_t *length* )

This function polls the transmitter register, first waits for the register to be empty or TX FIFO to have room, and writes data to the transmitter buffer, then waits for the dat to be sent out to the bus.

Parameters

|               |                                     |
|---------------|-------------------------------------|
| <i>base</i>   | LPUART peripheral base address.     |
| <i>data</i>   | Start address of the data to write. |
| <i>length</i> | Size of the data to write.          |

Return values

|                                     |                                         |
|-------------------------------------|-----------------------------------------|
| <i>kStatus_LPUART_-<br/>Timeout</i> | Transmission timed out and was aborted. |
| <i>kStatus_Success</i>              | Successfully wrote all data.            |

### 26.2.7.28 **status\_t LPUART\_ReadBlocking ( LPUART\_Type \* *base*, uint8\_t \* *data*, size\_t *length* )**

This function polls the receiver register, waits for the receiver register full or receiver FIFO has data, and reads data from the TX register.

Parameters

|               |                                                         |
|---------------|---------------------------------------------------------|
| <i>base</i>   | LPUART peripheral base address.                         |
| <i>data</i>   | Start address of the buffer to store the received data. |
| <i>length</i> | Size of the buffer.                                     |

Return values

|                                               |                                                 |
|-----------------------------------------------|-------------------------------------------------|
| <i>kStatus_LPUART_Rx-<br/>HardwareOverrun</i> | Receiver overrun happened while receiving data. |
| <i>kStatus_LPUART_Noise-<br/>Error</i>        | Noise error happened while receiving data.      |
| <i>kStatus_LPUART_-<br/>FramingError</i>      | Framing error happened while receiving data.    |
| <i>kStatus_LPUART_Parity-<br/>Error</i>       | Parity error happened while receiving data.     |
| <i>kStatus_LPUART_-<br/>Timeout</i>           | Transmission timed out and was aborted.         |
| <i>kStatus_Success</i>                        | Successfully received all data.                 |

### 26.2.7.29 **void LPUART\_TransferCreateHandle ( LPUART\_Type \* *base*, Ipuart\_handle\_t \* *handle*, Ipuart\_transfer\_callback\_t *callback*, void \* *userData* )**

This function initializes the LPUART handle, which can be used for other LPUART transactional APIs. Usually, for a specified LPUART instance, call this API once to get the initialized handle.

The LPUART driver supports the "background" receiving, which means that user can set up an RX ring buffer optionally. Data received is stored into the ring buffer even when the user doesn't call the [LPUART\\_TransferReceiveNonBlocking\(\)](#) API. If there is already data received in the ring buffer, the user

can get the received data from the ring buffer directly. The ring buffer is disabled if passing NULL as `ringBuffer`.

Parameters

|                 |                                 |
|-----------------|---------------------------------|
| <i>base</i>     | LPUART peripheral base address. |
| <i>handle</i>   | LPUART handle pointer.          |
| <i>callback</i> | Callback function.              |
| <i>userData</i> | User data.                      |

### 26.2.7.30 `status_t LPUART_TransferSendNonBlocking ( LPUART_Type * base, Ipuart_handle_t * handle, Ipuart_transfer_t * xfer )`

This function send data using an interrupt method. This is a non-blocking function, which returns directly without waiting for all data written to the transmitter register. When all data is written to the TX register in the ISR, the LPUART driver calls the callback function and passes the `kStatus_LPUART_TxIdle` as status parameter.

Note

The `kStatus_LPUART_TxIdle` is passed to the upper layer when all data are written to the TX register. However, there is no check to ensure that all the data sent out. Before disabling the T-X, check the `kLPUART_TransmissionCompleteFlag` to ensure that the transmit is finished.

Parameters

|               |                                                                    |
|---------------|--------------------------------------------------------------------|
| <i>base</i>   | LPUART peripheral base address.                                    |
| <i>handle</i> | LPUART handle pointer.                                             |
| <i>xfer</i>   | LPUART transfer structure, see <a href="#">Ipuart_transfer_t</a> . |

Return values

|                                      |                                                                                    |
|--------------------------------------|------------------------------------------------------------------------------------|
| <code>kStatus_Success</code>         | Successfully start the data transmission.                                          |
| <code>kStatus_LPUART_TxBusy</code>   | Previous transmission still not finished, data not all written to the TX register. |
| <code>kStatus_InvalidArgument</code> | Invalid argument.                                                                  |

### 26.2.7.31 `void LPUART_TransferStartRingBuffer ( LPUART_Type * base, Ipuart_handle_t * handle, uint8_t * ringBuffer, size_t ringBufferSize )`

This function sets up the RX ring buffer to a specific UART handle.

When the RX ring buffer is used, data received is stored into the ring buffer even when the user doesn't call the `UART_TransferReceiveNonBlocking()` API. If there is already data received in the ring buffer, the user can get the received data from the ring buffer directly.

#### Note

When using RX ring buffer, one byte is reserved for internal use. In other words, if `ringBufferSize` is 32, then only 31 bytes are used for saving data.

#### Parameters

|                       |                                                                                              |
|-----------------------|----------------------------------------------------------------------------------------------|
| <i>base</i>           | LPUART peripheral base address.                                                              |
| <i>handle</i>         | LPUART handle pointer.                                                                       |
| <i>ringBuffer</i>     | Start address of ring buffer for background receiving. Pass NULL to disable the ring buffer. |
| <i>ringBufferSize</i> | size of the ring buffer.                                                                     |

### 26.2.7.32 void LPUART\_TransferStopRingBuffer ( `LPUART_Type * base, Ipuart_handle_t * handle` )

This function aborts the background transfer and uninstalls the ring buffer.

#### Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |

### 26.2.7.33 size\_t LPUART\_TransferGetRxRingBufferLength ( `LPUART_Type * base, Ipuart_handle_t * handle` )

#### Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |

#### Returns

Length of received data in RX ring buffer.

**26.2.7.34 void LPUART\_TransferAbortSend ( LPUART\_Type \* *base*, Ipuart\_handle\_t \* *handle* )**

This function aborts the interrupt driven data sending. The user can get the remainBtyes to find out how many bytes are not sent out.

Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |

### 26.2.7.35 status\_t LPUART\_TransferGetSendCount ( **LPUART\_Type \* base,**                  **Ipuart\_handle\_t \* handle, uint32\_t \* count** )

This function gets the number of bytes that have been sent out to bus by an interrupt method.

Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |
| <i>count</i>  | Send bytes count.               |

Return values

|                                     |                                                       |
|-------------------------------------|-------------------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No send in progress.                                  |
| <i>kStatus_InvalidArgument</i>      | Parameter is invalid.                                 |
| <i>kStatus_Success</i>              | Get successfully through the parameter <i>count</i> ; |

### 26.2.7.36 status\_t LPUART\_TransferReceiveNonBlocking ( **LPUART\_Type \* base,**                  **Ipuart\_handle\_t \* handle, Ipuart\_transfer\_t \* xfer, size\_t \* receivedBytes** )

This function receives data using an interrupt method. This is a non-blocking function which returns without waiting to ensure that all data are received. If the RX ring buffer is used and not empty, the data in the ring buffer is copied and the parameter *receivedBytes* shows how many bytes are copied from the ring buffer. After copying, if the data in the ring buffer is not enough for read, the receive request is saved by the LPUART driver. When the new data arrives, the receive request is serviced first. When all data is received, the LPUART driver notifies the upper layer through a callback function and passes a status parameter *kStatus\_UART\_RxIdle*. For example, the upper layer needs 10 bytes but there are only 5 bytes in ring buffer. The 5 bytes are copied to *xfer->data*, which returns with the parameter *receivedBytes* set to 5. For the remaining 5 bytes, the newly arrived data is saved from *xfer->data[5]*. When 5 bytes are received, the LPUART driver notifies the upper layer. If the RX ring buffer is not enabled, this function enables the RX and RX interrupt to receive data to *xfer->data*. When all data is received, the upper layer is notified.

Parameters

|                      |                                                               |
|----------------------|---------------------------------------------------------------|
| <i>base</i>          | LPUART peripheral base address.                               |
| <i>handle</i>        | LPUART handle pointer.                                        |
| <i>xfer</i>          | LPUART transfer structure, see <code>uart_transfer_t</code> . |
| <i>receivedBytes</i> | Bytes received from the ring buffer directly.                 |

Return values

|                                |                                                          |
|--------------------------------|----------------------------------------------------------|
| <i>kStatus_Success</i>         | Successfully queue the transfer into the transmit queue. |
| <i>kStatus_LPUART_Rx-Busy</i>  | Previous receive request is not finished.                |
| <i>kStatus_InvalidArgument</i> | Invalid argument.                                        |

### 26.2.7.37 void LPUART\_TransferAbortReceive ( `LPUART_Type * base, Ipuart_handle_t * handle` )

This function aborts the interrupt-driven data receiving. The user can get the remainBytes to find out how many bytes not received yet.

Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |

### 26.2.7.38 status\_t LPUART\_TransferGetReceiveCount ( `LPUART_Type * base, Ipuart_handle_t * handle, uint32_t * count` )

This function gets the number of bytes that have been received.

Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | LPUART peripheral base address. |
| <i>handle</i> | LPUART handle pointer.          |
| <i>count</i>  | Receive bytes count.            |

Return values

|                                     |                                               |
|-------------------------------------|-----------------------------------------------|
| <i>kStatus_NoTransferInProgress</i> | No receive in progress.                       |
| <i>kStatus_InvalidArgument</i>      | Parameter is invalid.                         |
| <i>kStatus_Success</i>              | Get successfully through the parameter count; |

### 26.2.7.39 void LPUART\_TransferHandleIRQ ( LPUART\_Type \* *base*, void \* *irqHandle* )

This function handles the LPUART transmit and receive IRQ request.

Parameters

|                  |                                 |
|------------------|---------------------------------|
| <i>base</i>      | LPUART peripheral base address. |
| <i>irqHandle</i> | LPUART handle pointer.          |

### 26.2.7.40 void LPUART\_TransferHandleErrorIRQ ( LPUART\_Type \* *base*, void \* *irqHandle* )

This function handles the LPUART error IRQ request.

Parameters

|                  |                                 |
|------------------|---------------------------------|
| <i>base</i>      | LPUART peripheral base address. |
| <i>irqHandle</i> | LPUART handle pointer.          |

# Chapter 27

## LTC: LP Trusted Cryptography

### 27.1 Overview

The MCUXpresso SDK provides a peripheral driver for the LP Trusted Cryptography (LTC) module of MCUXpresso SDK devices. LP Trusted Cryptography is a set of cryptographpic hardware accelerator engines that share common registers. LTC architecture can support AES, DES, 3DES, MDHA (SHA), RSA, and ECC. The actual list of implemented cryptographpic hardware accelerator engines depends on the specific microcontroller.

The driver comprises two sets of API functions.

In the first set, blocking synchronous APIs are provided, for all operations supported by LTC hardware. The LTC operations are complete (and results are made availabe for further usage) when a function returns. When called, these functions do not return until an LTC operation is complete. These functions use main CPU for simple polling loops to determine operation complete or error status and also for plaintext or ciphertext data movements. The driver functions are not re-entrant. These functions provide typical interface to upper layer or application software.

In the second set, DMA support for symmetric LTC processing is provided, for AES and DES engines. APIs in the second set use DMA for data movement to and from the LTC input and output FIFOs. By using these functions, main CPU is not used for plaintext or ciphertext data movements (DMA is used instead). Thus, CPU processing power can be used for other application tasks, at cost of decreased maximum data throughput (because of DMA module and transactions management overhead). These functions provide less typical interface, for applications that must offload main CPU while ciphertext or plaintext is being processed, at cost of longer cryptographpic processing time.

### 27.2 LTC Driver Initialization and Configuration

LTC Driver is initialized by calling the `LTC_Init()` function, it enables the LTC module clock in the SIM module. If AES or DES engine is used and the LTC module implementation features the LTC DPA Mask Seed register, seed the DPA mask generator by using the seed from a random number generator. The `LTC_SetDpaMaskSeed()` function is provided to set the DPA mask seed.

### 27.3 Comments about API usage in RTOS

LTC operations provided by this driver are not re-entrant. Thus, application software shall ensure the LTC module operation is not requested from different tasks or interrupt service routines while an operation is in progress.

### 27.4 Comments about API usage in interrupt handler

All APIs can be used from interrupt handler although execution time shall be considered (interrupt latency of equal and lower priority interrupts increases).

## 27.5 LTC Driver Examples

### 27.5.1 Simple examples

Initialize LTC after Power On Reset or reset cycle Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/ltcEncrypt plaintext by DES engine Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/ltc Encrypt plaintext by AES engine Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/ltc Compute keyed hash by AES engine (CMAC) Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/ltc Compute hash by MDHA engine (SHA-256) Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/ltc Compute modular integer exponentiation Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/ltc Compute elliptic curve point multiplication Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/ltc

## Modules

- [LTC Blocking APIs](#)

## Functions

- void [LTC\\_Init](#) (LTC\_Type \*base)  
*Initializes the LTC driver.*
- void [LTC\\_Deinit](#) (LTC\_Type \*base)  
*Deinitializes the LTC driver.*

## Driver version

- #define [FSL\\_LTC\\_DRIVER\\_VERSION](#) (MAKE\_VERSION(2, 0, 15))  
*LTC driver version.*

## 27.6 Macro Definition Documentation

### 27.6.1 #define FSL\_LTC\_DRIVER\_VERSION (MAKE\_VERSION(2, 0, 15))

Version 2.0.15.

Current version: 2.0.14

Change log:

- Version 2.0.1
  - fixed warning during g++ compilation
- Version 2.0.2
  - fixed [KPSDK-10932][LTC][SHA] [LTC\\_HASH\(\)](#) blocks indefinitely when message size exceeds 4080 bytes
- Version 2.0.3
  - fixed LTC\_PKHA\_CompareBigNum() in case an integer argument is an array of all zeroes

- Version 2.0.4
  - constant LTC\_PKHA\_CompareBigNum() processing time
- Version 2.0.5
  - Fix MISRA issues
- Version 2.0.6
  - fixed [KPSDK-23603][LTC] AES Decrypt in ECB and CBC modes fail when ciphertext size > 0xff0 bytes
- Version 2.0.7
  - Fix MISRA-2012 issues
- Version 2.0.8
  - Fix Coverity issues
- Version 2.0.9
  - Fix sign-compare warning in ltc\_set\_context and in ltc\_get\_context
- Version 2.0.10
  - Fix MISRA-2012 issues
- Version 2.0.11
  - Fix MISRA-2012 issues
- Version 2.0.12
  - Fix AES Decrypt in CBC modes fail when used kLTC\_DecryptKey.
- Version 2.0.13
  - Add feature macro FSL\_FEATURE\_LTC\_HAS\_NO\_CLOCK\_CONTROL\_BIT into LTC\_Init function.
- Version 2.0.14
  - Add feature macro FSL\_FEATURE\_LTC\_HAS\_NO\_CLOCK\_CONTROL\_BIT into LTC\_Deinit function.
- Version 2.0.15
  - Fix MISRA-2012 issues

## 27.7 Function Documentation

### 27.7.1 void LTC\_Init ( LTC\_Type \* *base* )

This function initializes the LTC driver.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | LTC peripheral base address |
|-------------|-----------------------------|

### 27.7.2 void LTC\_Deinit ( LTC\_Type \* *base* )

This function deinitializes the LTC driver.

### Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | LTC peripheral base address |
|-------------|-----------------------------|

## 27.8 LTC Blocking APIs

### 27.8.1 Overview

This section describes the programming interface of the LTC Synchronous Blocking functions

### Modules

- [LTC AES driver](#)
- [LTC DES driver](#)
- [LTC HASH driver](#)
- [LTC PKHA driver](#)

## 27.8.2 LTC DES driver

### 27.8.2.1 Overview

This section describes the programming interface of the LTC DES driver.

#### Macros

- `#define LTC_DES_KEY_SIZE 8`  
*LTC DES key size - 64 bits.*
- `#define LTC_DES_IV_SIZE 8`  
*LTC DES IV size - 8 bytes.*

### 27.8.2.2 Macro Definition Documentation

#### 27.8.2.2.1 `#define LTC_DES_KEY_SIZE 8`

## 27.8.3 LTC AES driver

### 27.8.3.1 Overview

This section describes the programming interface of the LTC AES driver.

#### Macros

- `#define LTC_AES_BLOCK_SIZE 16U`  
*AES block size in bytes.*
- `#define LTC_AES_IV_SIZE 16`  
*AES Input Vector size in bytes.*
- `#define LTC_AES_DecryptCtr(base, input, output, size, counter, key, keySize, counterlast, szLeft) LTC_AES_CryptCtr(base, input, output, size, counter, key, keySize, counterlast, szLeft)`  
*AES CTR decrypt is mapped to the AES CTR generic operation.*
- `#define LTC_AES_EncryptCtr(base, input, output, size, counter, key, keySize, counterlast, szLeft) LTC_AES_CryptCtr(base, input, output, size, counter, key, keySize, counterlast, szLeft)`  
*AES CTR encrypt is mapped to the AES CTR generic operation.*

#### Enumerations

- `enum ltc_aes_key_t {  
 kLTC_EncryptKey = 0U,  
 kLTC_DecryptKey = 1U }`  
*Type of AES key for ECB and CBC decrypt operations.*

#### Functions

- `status_t LTC_AES_GenerateDecryptKey (LTC_Type *base, const uint8_t *encryptKey, uint8_t *decryptKey, uint32_t keySize)`  
*Transforms an AES encrypt key (forward AES) into the decrypt key (inverse AES).*
- `status_t LTC_AES_EncryptEcb (LTC_Type *base, const uint8_t *plaintext, uint8_t *ciphertext, uint32_t size, const uint8_t *key, uint32_t keySize)`  
*Encrypts AES using the ECB block mode.*
- `status_t LTC_AES_DecryptEcb (LTC_Type *base, const uint8_t *ciphertext, uint8_t *plaintext, uint32_t size, const uint8_t *key, uint32_t keySize, ltc_aes_key_t keyType)`  
*Decrypts AES using ECB block mode.*
- `status_t LTC_AES_EncryptCbc (LTC_Type *base, const uint8_t *plaintext, uint8_t *ciphertext, uint32_t size, const uint8_t iv[LTC_AES_IV_SIZE], const uint8_t *key, uint32_t keySize)`  
*Encrypts AES using CBC block mode.*
- `status_t LTC_AES_DecryptCbc (LTC_Type *base, const uint8_t *ciphertext, uint8_t *plaintext, uint32_t size, const uint8_t iv[LTC_AES_IV_SIZE], const uint8_t *key, uint32_t keySize, ltc_aes_key_t keyType)`  
*Decrypts AES using CBC block mode.*
- `status_t LTC_AES_CryptCtr (LTC_Type *base, const uint8_t *input, uint8_t *output, uint32_t size, uint8_t counter[LTC_AES_BLOCK_SIZE], const uint8_t *key, uint32_t keySize, uint8_t`

- counterlast[LTC\_AES\_BLOCK\_SIZE], uint32\_t \*szLeft)  
*Encrypts or decrypts AES using CTR block mode.*
- **status\_t LTC\_AES\_EncryptTagCcm** (LTC\_Type \*base, const uint8\_t \*plaintext, uint8\_t \*ciphertext, uint32\_t size, const uint8\_t \*iv, uint32\_t ivSize, const uint8\_t \*aad, uint32\_t aadSize, const uint8\_t \*key, uint32\_t keySize, uint8\_t \*tag, uint32\_t tagSize)  
*Encrypts AES and tags using CCM block mode.*
  - **status\_t LTC\_AES\_DecryptTagCcm** (LTC\_Type \*base, const uint8\_t \*ciphertext, uint8\_t \*plaintext, uint32\_t size, const uint8\_t \*iv, uint32\_t ivSize, const uint8\_t \*aad, uint32\_t aadSize, const uint8\_t \*key, uint32\_t keySize, const uint8\_t \*tag, uint32\_t tagSize)  
*Decrypts AES and authenticates using CCM block mode.*

### 27.8.3.2 Enumeration Type Documentation

#### 27.8.3.2.1 enum ltc\_aes\_key\_t

Enumerator

**kLTC\_EncryptKey** Input key is an encrypt key.

**kLTC\_DecryptKey** Input key is a decrypt key.

### 27.8.3.3 Function Documentation

#### 27.8.3.3.1 status\_t LTC\_AES\_GenerateDecryptKey ( LTC\_Type \* *base*, const uint8\_t \* *encryptKey*, uint8\_t \* *decryptKey*, uint32\_t *keySize* )

Transforms the AES encrypt key (forward AES) into the decrypt key (inverse AES). The key derived by this function can be used as a direct load decrypt key for AES ECB and CBC decryption operations (keyType argument).

Parameters

|            |                   |                                                                       |
|------------|-------------------|-----------------------------------------------------------------------|
|            | <i>base</i>       | LTC peripheral base address                                           |
|            | <i>encryptKey</i> | Input key for decrypt key transformation                              |
| <i>out</i> | <i>decryptKey</i> | Output key, the decrypt form of the AES key.                          |
|            | <i>keySize</i>    | Size of the input key and output key in bytes. Must be 16, 24, or 32. |

Returns

Status from key generation operation

#### 27.8.3.3.2 status\_t LTC\_AES\_EncryptEcb ( LTC\_Type \* *base*, const uint8\_t \* *plaintext*, uint8\_t \* *ciphertext*, uint32\_t *size*, const uint8\_t \* *key*, uint32\_t *keySize* )

Encrypts AES using the ECB block mode.

Parameters

|     |                   |                                                                       |
|-----|-------------------|-----------------------------------------------------------------------|
|     | <i>base</i>       | LTC peripheral base address                                           |
|     | <i>plaintext</i>  | Input plain text to encrypt                                           |
| out | <i>ciphertext</i> | Output cipher text                                                    |
|     | <i>size</i>       | Size of input and output data in bytes. Must be multiple of 16 bytes. |
|     | <i>key</i>        | Input key to use for encryption                                       |
|     | <i>keySize</i>    | Size of the input key, in bytes. Must be 16, 24, or 32.               |

Returns

Status from encrypt operation

**27.8.3.3.3 status\_t LTC\_AES\_DecryptEcb ( LTC\_Type \* *base*, const uint8\_t \* *ciphertext*, uint8\_t \* *plaintext*, uint32\_t *size*, const uint8\_t \* *key*, uint32\_t *keySize*, ltc\_aes\_key\_t *keyType* )**

Decrypts AES using ECB block mode.

Parameters

|     |                   |                                                                                            |
|-----|-------------------|--------------------------------------------------------------------------------------------|
|     | <i>base</i>       | LTC peripheral base address                                                                |
|     | <i>ciphertext</i> | Input cipher text to decrypt                                                               |
| out | <i>plaintext</i>  | Output plain text                                                                          |
|     | <i>size</i>       | Size of input and output data in bytes. Must be multiple of 16 bytes.                      |
|     | <i>key</i>        | Input key.                                                                                 |
|     | <i>keySize</i>    | Size of the input key, in bytes. Must be 16, 24, or 32.                                    |
|     | <i>keyType</i>    | Input type of the key (allows to directly load decrypt key for AES ECB decrypt operation.) |

Returns

Status from decrypt operation

**27.8.3.3.4 status\_t LTC\_AES\_EncryptCbc ( LTC\_Type \* *base*, const uint8\_t \* *plaintext*, uint8\_t \* *ciphertext*, uint32\_t *size*, const uint8\_t iv[LTC\_AES\_IV\_SIZE], const uint8\_t \* *key*, uint32\_t *keySize* )**

Parameters

|     |                   |                                                                       |
|-----|-------------------|-----------------------------------------------------------------------|
|     | <i>base</i>       | LTC peripheral base address                                           |
|     | <i>plaintext</i>  | Input plain text to encrypt                                           |
| out | <i>ciphertext</i> | Output cipher text                                                    |
|     | <i>size</i>       | Size of input and output data in bytes. Must be multiple of 16 bytes. |
|     | <i>iv</i>         | Input initial vector to combine with the first input block.           |
|     | <i>key</i>        | Input key to use for encryption                                       |
|     | <i>keySize</i>    | Size of the input key, in bytes. Must be 16, 24, or 32.               |

Returns

Status from encrypt operation

**27.8.3.3.5 status\_t LTC\_AES\_DecryptCbc ( LTC\_Type \* *base*, const uint8\_t \* *ciphertext*, uint8\_t \* *plaintext*, uint32\_t *size*, const uint8\_t *iv*[LTC\_AES\_IV\_SIZE], const uint8\_t \* *key*, uint32\_t *keySize*, ltc\_aes\_key\_t *keyType* )**

Parameters

|     |                   |                                                                                            |
|-----|-------------------|--------------------------------------------------------------------------------------------|
|     | <i>base</i>       | LTC peripheral base address                                                                |
|     | <i>ciphertext</i> | Input cipher text to decrypt                                                               |
| out | <i>plaintext</i>  | Output plain text                                                                          |
|     | <i>size</i>       | Size of input and output data in bytes. Must be multiple of 16 bytes.                      |
|     | <i>iv</i>         | Input initial vector to combine with the first input block.                                |
|     | <i>key</i>        | Input key to use for decryption                                                            |
|     | <i>keySize</i>    | Size of the input key, in bytes. Must be 16, 24, or 32.                                    |
|     | <i>keyType</i>    | Input type of the key (allows to directly load decrypt key for AES CBC decrypt operation.) |

Returns

Status from decrypt operation

**27.8.3.3.6 status\_t LTC\_AES\_CryptCtr ( LTC\_Type \* *base*, const uint8\_t \* *input*, uint8\_t \* *output*, uint32\_t *size*, uint8\_t *counter*[LTC\_AES\_BLOCK\_SIZE], const uint8\_t \* *key*, uint32\_t *keySize*, uint8\_t *counterlast*[LTC\_AES\_BLOCK\_SIZE], uint32\_t \* *szLeft* )**

Encrypts or decrypts AES using CTR block mode. AES CTR mode uses only forward AES cipher and same algorithm for encryption and decryption. The only difference between encryption and decryption is

that, for encryption, the input argument is plain text and the output argument is cipher text. For decryption, the input argument is cipher text and the output argument is plain text.

#### Parameters

|         |                    |                                                                                                               |
|---------|--------------------|---------------------------------------------------------------------------------------------------------------|
|         | <i>base</i>        | LTC peripheral base address                                                                                   |
|         | <i>input</i>       | Input data for CTR block mode                                                                                 |
| out     | <i>output</i>      | Output data for CTR block mode                                                                                |
|         | <i>size</i>        | Size of input and output data in bytes                                                                        |
| in, out | <i>counter</i>     | Input counter (updates on return)                                                                             |
|         | <i>key</i>         | Input key to use for forward AES cipher                                                                       |
|         | <i>keySize</i>     | Size of the input key, in bytes. Must be 16, 24, or 32.                                                       |
| out     | <i>counterlast</i> | Output cipher of last counter, for chained CTR calls. NULL can be passed if chained calls are not used.       |
| out     | <i>szLeft</i>      | Output number of bytes in left unused in counterlast block. NULL can be passed if chained calls are not used. |

#### Returns

Status from encrypt operation

**27.8.3.3.7 status\_t LTC\_AES\_EncryptTagCcm ( LTC\_Type \* *base*, const uint8\_t \* *plaintext*, uint8\_t \* *ciphertext*, uint32\_t *size*, const uint8\_t \* *iv*, uint32\_t *ivSize*, const uint8\_t \* *aad*, uint32\_t *aadSize*, const uint8\_t \* *key*, uint32\_t *keySize*, uint8\_t \* *tag*, uint32\_t *tagSize* )**

Encrypts AES and optionally tags using CCM block mode.

#### Parameters

|     |                   |                                                                         |
|-----|-------------------|-------------------------------------------------------------------------|
|     | <i>base</i>       | LTC peripheral base address                                             |
|     | <i>plaintext</i>  | Input plain text to encrypt                                             |
| out | <i>ciphertext</i> | Output cipher text.                                                     |
|     | <i>size</i>       | Size of input and output data in bytes. Zero means authentication only. |
|     | <i>iv</i>         | Nonce                                                                   |

|     |                |                                                                                  |
|-----|----------------|----------------------------------------------------------------------------------|
|     | <i>ivSize</i>  | Length of the Nonce in bytes. Must be 7, 8, 9, 10, 11, 12, or 13.                |
|     | <i>aad</i>     | Input additional authentication data. Can be NULL if aadSize is zero.            |
|     | <i>aadSize</i> | Input size in bytes of AAD. Zero means data mode only (authentication skipped).  |
|     | <i>key</i>     | Input key to use for encryption                                                  |
|     | <i>keySize</i> | Size of the input key, in bytes. Must be 16, 24, or 32.                          |
| out | <i>tag</i>     | Generated output tag. Set to NULL to skip tag processing.                        |
|     | <i>tagSize</i> | Input size of the tag to generate, in bytes. Must be 4, 6, 8, 10, 12, 14, or 16. |

Returns

Status from encrypt operation

**27.8.3.3.8 status\_t LTC\_AES\_DecryptTagCcm ( LTC\_Type \* *base*, const uint8\_t \* *ciphertext*, uint8\_t \* *plaintext*, uint32\_t *size*, const uint8\_t \* *iv*, uint32\_t *ivSize*, const uint8\_t \* *aad*, uint32\_t *aadSize*, const uint8\_t \* *key*, uint32\_t *keySize*, const uint8\_t \* *tag*, uint32\_t *tagSize* )**

Decrypts AES and optionally authenticates using CCM block mode.

Parameters

|     |                   |                                                                                 |
|-----|-------------------|---------------------------------------------------------------------------------|
|     | <i>base</i>       | LTC peripheral base address                                                     |
|     | <i>ciphertext</i> | Input cipher text to decrypt                                                    |
| out | <i>plaintext</i>  | Output plain text.                                                              |
|     | <i>size</i>       | Size of input and output data in bytes. Zero means authentication only.         |
|     | <i>iv</i>         | Nonce                                                                           |
|     | <i>ivSize</i>     | Length of the Nonce in bytes. Must be 7, 8, 9, 10, 11, 12, or 13.               |
|     | <i>aad</i>        | Input additional authentication data. Can be NULL if aadSize is zero.           |
|     | <i>aadSize</i>    | Input size in bytes of AAD. Zero means data mode only (authentication skipped). |

|  |                |                                                                                                                |
|--|----------------|----------------------------------------------------------------------------------------------------------------|
|  | <i>key</i>     | Input key to use for decryption                                                                                |
|  | <i>keySize</i> | Size of the input key, in bytes. Must be 16, 24, or 32.                                                        |
|  | <i>tag</i>     | Received tag. Set to NULL to skip tag processing.                                                              |
|  | <i>tagSize</i> | Input size of the received tag to compare with the computed tag, in bytes. Must be 4, 6, 8, 10, 12, 14, or 16. |

Returns

Status from decrypt operation

## 27.8.4 LTC HASH driver

### 27.8.4.1 Overview

This section describes the programming interface of the LTC HASH driver.

#### Data Structures

- struct `ltc_hash_ctx_t`  
*Storage type used to save hash context. [More...](#)*

#### Macros

- `#define LTC_HASH_CTX_SIZE 29`  
*LTC HASH Context size.*

#### Enumerations

- enum `ltc_hash_algo_t` {
   
`kLTC_XcbcMac` = 0,  
`kLTC_Cmac` }  
*Supported cryptographic block cipher functions for HASH creation.*

#### Functions

- `status_t LTC_HASH_Init (LTC_Type *base, ltc_hash_ctx_t *ctx, ltc_hash_algo_t algo, const uint8_t *key, uint32_t keySize)`  
*Initialize HASH context.*
- `status_t LTC_HASH_Update (ltc_hash_ctx_t *ctx, const uint8_t *input, uint32_t inputSize)`  
*Add data to current HASH.*
- `status_t LTC_HASH_Finish (ltc_hash_ctx_t *ctx, uint8_t *output, uint32_t *outputSize)`  
*Finalize hashing.*
- `status_t LTC_HASH (LTC_Type *base, ltc_hash_algo_t algo, const uint8_t *input, uint32_t inputSize, const uint8_t *key, uint32_t keySize, uint8_t *output, uint32_t *outputSize)`  
*Create HASH on given data.*

### 27.8.4.2 Data Structure Documentation

#### 27.8.4.2.1 struct `ltc_hash_ctx_t`

#### 27.8.4.3 Macro Definition Documentation

#### 27.8.4.3.1 `#define LTC_HASH_CTX_SIZE 29`

#### 27.8.4.4 Enumeration Type Documentation

##### 27.8.4.4.1 enum ltc\_hash\_algo\_t

Enumerator

*kLTC\_XcbcMac* XCBC-MAC (AES engine)

*kLTC\_Cmac* CMAC (AES engine)

#### 27.8.4.5 Function Documentation

##### 27.8.4.5.1 status\_t LTC\_HASH\_Init ( LTC\_Type \* *base*, ltc\_hash\_ctx\_t \* *ctx*, ltc\_hash\_algo\_t *algo*, const uint8\_t \* *key*, uint32\_t *keySize* )

This function initialize the HASH. Key shall be supplied if the underlaying algorithm is AES XCBC-MAC or CMAC. Key shall be NULL if the underlaying algorithm is SHA.

For XCBC-MAC, the key length must be 16. For CMAC, the key length can be the AES key lengths supported by AES engine. For MDHA the key length argument is ignored.

Parameters

|            |                |                                                    |
|------------|----------------|----------------------------------------------------|
|            | <i>base</i>    | LTC peripheral base address                        |
| <i>out</i> | <i>ctx</i>     | Output hash context                                |
|            | <i>algo</i>    | Underlaying algorithm to use for hash computation. |
|            | <i>key</i>     | Input key (NULL if underlaying algorithm is SHA)   |
|            | <i>keySize</i> | Size of input key in bytes                         |

Returns

Status of initialization

##### 27.8.4.5.2 status\_t LTC\_HASH\_Update ( ltc\_hash\_ctx\_t \* *ctx*, const uint8\_t \* *input*, uint32\_t *inputSize* )

Add data to current HASH. This can be called repeatedly with an arbitrary amount of data to be hashed.

Parameters

|                |                  |                             |
|----------------|------------------|-----------------------------|
| <i>in, out</i> | <i>ctx</i>       | HASH context                |
|                | <i>input</i>     | Input data                  |
|                | <i>inputSize</i> | Size of input data in bytes |

Returns

Status of the hash update operation

#### 27.8.4.5.3 status\_t LTC\_HASH\_Finish ( *Ltc\_hash\_ctx\_t \* ctx, uint8\_t \* output, uint32\_t \* outputSize* )

Outputs the final hash and erases the context.

Parameters

|                |                   |                                                               |
|----------------|-------------------|---------------------------------------------------------------|
| <i>in, out</i> | <i>ctx</i>        | Input hash context                                            |
| <i>out</i>     | <i>output</i>     | Output hash data                                              |
| <i>out</i>     | <i>outputSize</i> | Output parameter storing the size of the output hash in bytes |

Returns

Status of the hash finish operation

#### 27.8.4.5.4 status\_t LTC\_HASH ( *LTC\_Type \* base, Ltc\_hash\_algo\_t algo, const uint8\_t \* input, uint32\_t inputSize, const uint8\_t \* key, uint32\_t keySize, uint8\_t \* output, uint32\_t \* outputSize* )

Perform the full keyed HASH in one function call.

Parameters

|  |                  |                                                 |
|--|------------------|-------------------------------------------------|
|  | <i>base</i>      | LTC peripheral base address                     |
|  | <i>algo</i>      | Block cipher algorithm to use for CMAC creation |
|  | <i>input</i>     | Input data                                      |
|  | <i>inputSize</i> | Size of input data in bytes                     |

|     |                   |                                                               |
|-----|-------------------|---------------------------------------------------------------|
|     | <i>key</i>        | Input key                                                     |
|     | <i>keySize</i>    | Size of input key in bytes                                    |
| out | <i>output</i>     | Output hash data                                              |
| out | <i>outputSize</i> | Output parameter storing the size of the output hash in bytes |

Returns

Status of the one call hash operation.

## 27.8.5 LTC PKHA driver

### 27.8.5.1 Overview

This section describes the programming interface of the LTC PKHA driver.

### Data Structures

- struct `ltc_pkha_ecc_point_t`  
*PKHA ECC point structure. [More...](#)*

### Enumerations

- enum `ltc_pkha_timing_t` {
   
`kLTC_PKHA_NoTimingEqualized` = 0U,
   
`kLTC_PKHA_TimingEqualized` = 1U }
   
*Use of timing equalized version of a PKHA function.*
- enum `ltc_pkha_f2m_t` {
   
`kLTC_PKHA_IntegerArith` = 0U,
   
`kLTC_PKHA_F2mArith` = 1U }
   
*Integer vs binary polynomial arithmetic selection.*
- enum `ltc_pkha_montgomery_form_t` {
   
`kLTC_PKHA_NormalValue` = 0U,
   
`kLTC_PKHA_MontgomeryFormat` = 1U }
   
*Montgomery or normal PKHA input format.*

### 27.8.5.2 Data Structure Documentation

#### 27.8.5.2.1 struct `ltc_pkha_ecc_point_t`

##### Data Fields

- `uint8_t * X`  
*X coordinate (affine)*
- `uint8_t * Y`  
*Y coordinate (affine)*

### 27.8.5.3 Enumeration Type Documentation

#### 27.8.5.3.1 enum `ltc_pkha_timing_t`

Enumerator

- `kLTC_PKHA_NoTimingEqualized` Normal version of a PKHA operation.  
`kLTC_PKHA_TimingEqualized` Timing-equalized version of a PKHA operation.

### 27.8.5.3.2 enum ltc\_pkha\_f2m\_t

Enumerator

*kLTC\_PKHA\_IntegerArith* Use integer arithmetic.

*kLTC\_PKHA\_F2mArith* Use binary polynomial arithmetic.

### 27.8.5.3.3 enum ltc\_pkha\_montgomery\_form\_t

Enumerator

*kLTC\_PKHA\_NormalValue* PKHA number is normal integer.

*kLTC\_PKHA\_MontgomeryFormat* PKHA number is in montgomery format.

# Chapter 28

## MSMC: Multicore System Mode Controller

### 28.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Multicore System Mode Controller (MSMC) module of MCUXpresso SDK devices.

### 28.2 Typical use case

#### 28.2.1 Set Core 0 from RUN to VLPR mode

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/msmc

#### 28.2.2 Set Core 0 from VLPR/HSRUN to RUN mode

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/msmc

### 28.3 Typical use case

#### 28.3.1 Set Core 0 from RUN to HSRUN mode

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/msmc

#### 28.3.2 Enter wait or stop modes

SMC driver provides APIs to set MCU to different wait modes and stop modes. At the same time, there are pre-function and post-function for the modes setting. The pre-function and post-function are used for:

1. Disable/enable the interrupt through PRIMASK. In practise, there is such scenario: the application sets the wakeup interrupt and calls SMC function [SMC\\_SetPowerModeStop](#) to set MCU to STOP mode, but the wakeup interrupt happens so quickly that the ISR completed before the function [SMC\\_SetPowerModeStop](#), as a result, the MCU enters STOP mode and never be wakeup by the interrupt. In this case, application could first disable interrupt through PRIMASK, then set the wakeup interrupt and enter STOP mode. After wakeup, the first thing is enable the interrupt through PRIMASK. The MCU could still be wakeup when disable interrupt through PRIMASK. The pre- and post- functions handle the PRIMASK inside.

```

SMC_PreEnterStopModes();

/* Enable the wakeup interrupt here. */

SMC_SetPowerModeStop(SMC0, kSMC_PartialStop);

SMC_PostExitStopModes();

```

For other use cases, please refer to the comments of the MSMC driver header file. Some example codes are also provided.

## Files

- file `fsl_msmc.h`

## Data Structures

- struct `smc_reset_pin_filter_config_t`  
*Reset pin filter configuration.* [More...](#)

## Enumerations

- enum `smc_power_mode_protection_t` {
 `kSMC_AllowPowerModeVlls` = SMC\_PMPROT\_AVLLS\_MASK,
 `kSMC_AllowPowerModeLls` = SMC\_PMPROT\_ALLS\_MASK,
 `kSMC_AllowPowerModeVlp` = SMC\_PMPROT\_AVLP\_MASK,
 `kSMC_AllowPowerModeHsrun` = SMC\_PMPROT\_AHSRUN\_MASK,
 `kSMC_AllowPowerModeAll` }
   
*Power Modes Protection.*
- enum `smc_power_state_t` {
 `kSMC_PowerStateRun` = 1U,
 `kSMC_PowerStateStop` = 1U << 1U,
 `kSMC_PowerStateVlpr` = 1U << 2U,
 `kSMC_PowerStateHsrun` = 1U << 7U }
   
*Power Modes in PMSTAT.*
- enum `smc_power_stop_entry_status_t` {
 `kSMC_PowerStopEntryAlt0` = 1U,
 `kSMC_PowerStopEntryAlt1` = 1U << 1,
 `kSMC_PowerStopEntryAlt2` = 1U << 2,
 `kSMC_PowerStopEntryAlt3` = 1U << 3,
 `kSMC_PowerStopEntryAlt4` = 1U << 4,
 `kSMC_PowerStopEntryAlt5` = 1U << 5 }
   
*Power Stop Entry Status in PMSTAT.*
- enum `smc_run_mode_t` {
 `kSMC_RunNormal` = 0U,
 `kSMC_RunVlpr` = 2U,
 `kSMC_Hsrun` = 3U }
   
*Run mode definition.*

- enum `smc_stop_mode_t` {
   
  `kSMC_StopNormal` = 0U,
   
  `kSMC_StopVlps` = 2U,
   
  `kSMC_StopLls` = 3U,
   
  `kSMC_StopVlls` = 4U }
   
    *Stop mode definition.*
- enum `smc_partial_stop_option_t` {
   
  `kSMC_PartialStop` = 0U,
   
  `kSMC_PartialStop1` = 1U,
   
  `kSMC_PartialStop2` = 2U,
   
  `kSMC_PartialStop3` = 3U }
   
    *Partial STOP option.*
- enum { `kStatus_SMC_StopAbort` = MAKE\_STATUS(kStatusGroup\_POWER, 0) }
   
    *SMC configuration status.*
- enum `smc_reset_source_t` {
   
  `kSMC_SourceWakeup` = SMC\_SRS\_WAKEUP\_MASK,
   
  `kSMC_SourcePor` = SMC\_SRS\_POR\_MASK,
   
  `kSMC_SourceLvd` = SMC\_SRS\_LVD\_MASK,
   
  `kSMC_SourceHvd` = SMC\_SRS\_HVD\_MASK,
   
  `kSMC_SourceWarm` = SMC\_SRS\_WARM\_MASK,
   
  `kSMC_SourceFatal` = SMC\_SRS\_FATAL\_MASK,
   
  `kSMC_SourceCore`,
   
  `kSMC_SourcePin` = SMC\_SRS\_PIN\_MASK,
   
  `kSMC_SourceMdm` = SMC\_SRS\_MDM\_MASK,
   
  `kSMC_SourceRstAck` = SMC\_SRS\_RSTACK\_MASK,
   
  `kSMC_SourceStopAck` = SMC\_SRS\_STOPACK\_MASK,
   
  `kSMC_SourceScg` = SMC\_SRS\_SCG\_MASK,
   
  `kSMC_SourceWdog` = SMC\_SRS\_WDOG\_MASK,
   
  `kSMC_SourceSoftware` = SMC\_SRS\_SW\_MASK,
   
  `kSMC_SourceLockup` = SMC\_SRS\_LOCKUP\_MASK,
   
  `kSMC_SourceJtag` = SMC\_SRS\_JTAG\_MASK }
   
    *System Reset Source Name definitions.*
- enum `smc_interrupt_enable_t` {
   
  `kSMC_IntNone` = 0U,
   
  `kSMC_IntPin` = SMC\_SRIE\_PIN\_MASK,
   
  `kSMC_IntMdm` = SMC\_SRIE\_MDM\_MASK,
   
  `kSMC_IntStopAck` = SMC\_SRIE\_STOPACK\_MASK,
   
  `kSMC_IntWdog` = SMC\_SRIE\_WDOG\_MASK,
   
  `kSMC_IntSoftware` = SMC\_SRIE\_SW\_MASK,
   
  `kSMC_IntLockup` = SMC\_SRIE\_LOCKUP\_MASK,
   
  `kSMC_IntAll` }
   
    *System reset interrupt enable bit definitions.*

## Driver version

- #define `FSL_MSMC_DRIVER_VERSION` (MAKE\_VERSION(2, 1, 2))

*MSMC driver version.*

## System mode controller APIs

- static void [SMC\\_SetPowerModeProtection](#) (SMC\_Type \*base, uint8\_t allowedModes)  
*Configures all power mode protection settings.*
- static [smc\\_power\\_state\\_t SMC\\_GetPowerModeState](#) (SMC\_Type \*base)  
*Gets the current power mode status.*
- static void [SMC\\_PreEnterStopModes](#) (void)  
*Prepare to enter stop modes.*
- static void [SMC\\_PostExitStopModes](#) (void)  
*Recovering after wake up from stop modes.*
- static void [SMC\\_PreEnterWaitModes](#) (void)  
*Prepare to enter wait modes.*
- static void [SMC\\_PostExitWaitModes](#) (void)  
*Recovering after wake up from stop modes.*
- [status\\_t SMC\\_SetPowerModeRun](#) (SMC\_Type \*base)  
*Configure the system to RUN power mode.*
- [status\\_t SMC\\_SetPowerModeHsrn](#) (SMC\_Type \*base)  
*Configure the system to HSRUN power mode.*
- [status\\_t SMC\\_SetPowerModeWait](#) (SMC\_Type \*base)  
*Configure the system to WAIT power mode.*
- [status\\_t SMC\\_SetPowerModeStop](#) (SMC\_Type \*base, [smc\\_partial\\_stop\\_option\\_t](#) option)  
*Configure the system to Stop power mode.*
- [status\\_t SMC\\_SetPowerModeVlpr](#) (SMC\_Type \*base)  
*Configure the system to VLPR power mode.*
- [status\\_t SMC\\_SetPowerModeVlpw](#) (SMC\_Type \*base)  
*Configure the system to VLPW power mode.*
- [status\\_t SMC\\_SetPowerModeVlps](#) (SMC\_Type \*base)  
*Configure the system to VLPS power mode.*
- [status\\_t SMC\\_SetPowerModeLls](#) (SMC\_Type \*base)  
*Configure the system to LLS power mode.*
- [status\\_t SMC\\_SetPowerModeVlls](#) (SMC\_Type \*base)  
*Configure the system to VLLS power mode.*
- static uint32\_t [SMC\\_GetPreviousResetSources](#) (SMC\_Type \*base)  
*Gets the reset source status which caused a previous reset.*
- static uint32\_t [SMC\\_GetStickyResetSources](#) (SMC\_Type \*base)  
*Gets the sticky reset source status.*
- static void [SMC\\_ClearStickyResetSources](#) (SMC\_Type \*base, uint32\_t sourceMasks)  
*Clears the sticky reset source status.*
- void [SMC\\_ConfigureResetPinFilter](#) (SMC\_Type \*base, const [smc\\_reset\\_pin\\_filter\\_config\\_t](#) \*config)  
*Configures the reset pin filter.*
- static void [SMC\\_SetSystemResetInterruptConfig](#) (SMC\_Type \*base, uint32\_t intMask)  
*Sets the system reset interrupt configuration.*
- static uint32\_t [SMC\\_GetResetInterruptSourcesStatus](#) (SMC\_Type \*base)  
*Gets the source status of the system reset interrupt.*
- static void [SMC\\_ClearResetInterruptSourcesStatus](#) (SMC\_Type \*base, uint32\_t intMask)  
*Clears the source status of the system reset interrupt.*
- static uint32\_t [SMC\\_GetBootOptionConfig](#) (SMC\_Type \*base)  
*Gets the boot option configuration.*

## 28.4 Data Structure Documentation

### 28.4.1 struct smc\_reset\_pin\_filter\_config\_t

#### Data Fields

- `uint8_t slowClockFilterCount`  
*Reset pin bus clock filter width from 1 to 32 slow clock cycles.*
- `bool enableFilter`  
*Reset pin filter enable/disable.*

#### Field Documentation

(1) `uint8_t smc_reset_pin_filter_config_t::slowClockFilterCount`

(2) `bool smc_reset_pin_filter_config_t::enableFilter`

## 28.5 Macro Definition Documentation

28.5.1 `#define FSL_MSMC_DRIVER_VERSION (MAKE_VERSION(2, 1, 2))`

## 28.6 Enumeration Type Documentation

### 28.6.1 enum smc\_power\_mode\_protection\_t

#### Enumerator

`kSMC_AllowPowerModeVlls` Allow Very-Low-Leakage Stop Mode.

`kSMC_AllowPowerModeLls` Allow Low-Leakage Stop Mode.

`kSMC_AllowPowerModeVlp` Allow Very-Low-Power Mode.

`kSMC_AllowPowerModeHsrun` Allow High Speed Run mode.

`kSMC_AllowPowerModeAll` Allow all power mode.

### 28.6.2 enum smc\_power\_state\_t

#### Enumerator

`kSMC_PowerStateRun` 0000\_0001 - Current power mode is RUN

`kSMC_PowerStateStop` 0000\_0010 - Current power mode is any STOP mode

`kSMC_PowerStateVlpr` 0000\_0100 - Current power mode is VLPR

`kSMC_PowerStateHsrun` 1000\_0000 - Current power mode is HSRUN

### 28.6.3 enum smc\_power\_stop\_entry\_status\_t

Enumerator

- kSMC\_PowerStopEntryAlt0* Indicates a Stop mode entry since this field was last cleared.
- kSMC\_PowerStopEntryAlt1* Indicates the system bus masters acknowledged the Stop mode entry.
- kSMC\_PowerStopEntryAlt2* Indicates the system clock peripherals acknowledged the Stop mode entry.
- kSMC\_PowerStopEntryAlt3* Indicates the bus clock peripherals acknowledged the Stop mode entry.
- kSMC\_PowerStopEntryAlt4* Indicates the slow clock peripherals acknowledged the Stop mode entry.
- kSMC\_PowerStopEntryAlt5* Indicates Stop mode entry completed.

### 28.6.4 enum smc\_run\_mode\_t

Enumerator

- kSMC\_RunNormal* normal RUN mode.
- kSMC\_RunVlpr* Very-Low-Power RUN mode.
- kSMC\_Hsrun* High Speed Run mode (HSRUN).

### 28.6.5 enum smc\_stop\_mode\_t

Enumerator

- kSMC\_StopNormal* Normal STOP mode.
- kSMC\_StopVlps* Very-Low-Power STOP mode.
- kSMC\_StopLls* Low-Leakage Stop mode.
- kSMC\_StopVlls* Very-Low-Leakage Stop mode.

### 28.6.6 enum smc\_partial\_stop\_option\_t

Enumerator

- kSMC\_PartialStop* STOP - Normal Stop mode.
- kSMC\_PartialStop1* Partial Stop with both system and bus clocks disabled.
- kSMC\_PartialStop2* Partial Stop with system clock disabled and bus clock enabled.
- kSMC\_PartialStop3* Partial Stop with system clock enabled and bus clock disabled.

## 28.6.7 anonymous enum

Enumerator

*kStatus\_SMC\_StopAbort* Entering Stop mode is abort.

## 28.6.8 enum smc\_reset\_source\_t

Enumerator

*kSMC\_SourceWakeup* Very low-leakage wakeup reset.

*kSMC\_SourcePor* Power on reset.

*kSMC\_SourceLvd* Low-voltage detect reset.

*kSMC\_SourceHvd* High-voltage detect reset.

*kSMC\_SourceWarm* Warm reset. Warm Reset flag will assert if any of the system reset sources in this register assert (SRS[31:8])

*kSMC\_SourceFatal* Fatal reset.

*kSMC\_SourceCore* Software reset that only reset the core, NOT a sticky system reset source.

*kSMC\_SourcePin* RESET\_B pin reset.

*kSMC\_SourceMdm* MDM reset.

*kSMC\_SourceRstAck* Reset Controller timeout reset.

*kSMC\_SourceStopAck* Stop timeout reset.

*kSMC\_SourceScg* SCG loss of lock or loss of clock.

*kSMC\_SourceWdog* Watchdog reset.

*kSMC\_SourceSoftware* Software reset.

*kSMC\_SourceLockup* Lockup reset. Core lockup or exception.

*kSMC\_SourceJtag* JTAG system reset.

## 28.6.9 enum smc\_interrupt\_enable\_t

Enumerator

*kSMC\_IntNone* No interrupt enabled.

*kSMC\_IntPin* Pin reset interrupt.

*kSMC\_IntMdm* MDM reset interrupt.

*kSMC\_IntStopAck* Stop timeout reset interrupt.

*kSMC\_IntWdog* Watchdog interrupt.

*kSMC\_IntSoftware* Software reset interrupts.

*kSMC\_IntLockup* Lock up interrupt.

*kSMC\_IntAll* All system reset interrupts.

## 28.7 Function Documentation

### 28.7.1 static void SMC\_SetPowerModeProtection ( **SMC\_Type** \* *base*, **uint8\_t** *allowedModes* ) [inline], [static]

This function configures the power mode protection settings for supported power modes in the specified chip family. The available power modes are defined in the smc\_power\_mode\_protection\_t. This should be done at an early system level initialization stage. See the reference manual for details. This register can only write once after the power reset.

The allowed modes are passed as bit map, for example, to allow LLS and VLLS, use SMC\_SetPowerModeProtection(kSMC\_AllowPowerModeLls | kSMC\_AllowPowerModeVlls). To allow all modes, use SMC\_SetPowerModeProtection(kSMC\_AllowPowerModeAll).

Parameters

|                     |                                    |
|---------------------|------------------------------------|
| <i>base</i>         | SMC peripheral base address.       |
| <i>allowedModes</i> | Bitmap of the allowed power modes. |

### 28.7.2 static smc\_power\_state\_t SMC\_GetPowerModeState ( **SMC\_Type** \* *base* ) [inline], [static]

This function returns the current power mode stat. Once application switches the power mode, it should always check the stat to check whether it runs into the specified mode or not. An application should check this mode before switching to a different mode. The system requires that only certain modes can switch to other specific modes. See the reference manual for details and the smc\_power\_state\_t for information about the power stat.

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

Returns

Current power mode status.

### 28.7.3 static void SMC\_PreEnterStopModes ( void ) [inline], [static]

This function should be called before entering STOP/VLPS/LLS/VLLS modes.

### 28.7.4 static void SMC\_PostExitStopModes ( void ) [inline], [static]

This function should be called after wake up from STOP/VLPS/LLS/VLLS modes. It is used together with [SMC\\_PreEnterStopModes](#).

**28.7.5 static void SMC\_PreEnterWaitModes ( void ) [inline], [static]**

This function should be called before entering WAIT/VLPW modes..

**28.7.6 static void SMC\_PostExitWaitModes ( void ) [inline], [static]**

This function should be called after wake up from WAIT/VLPW modes. It is used together with [SMC\\_PreEnterWaitModes](#).

**28.7.7 status\_t SMC\_SetPowerModeRun ( SMC\_Type \* *base* )**

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

Returns

SMC configuration error code.

**28.7.8 status\_t SMC\_SetPowerModeHsrun ( SMC\_Type \* *base* )**

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

Returns

SMC configuration error code.

**28.7.9 status\_t SMC\_SetPowerModeWait ( SMC\_Type \* *base* )**

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

Returns

SMC configuration error code.

### **28.7.10 status\_t SMC\_SetPowerModeStop ( SMC\_Type \* *base*, smc\_partial\_stop\_option\_t *option* )**

Parameters

|               |                              |
|---------------|------------------------------|
| <i>base</i>   | SMC peripheral base address. |
| <i>option</i> | Partial Stop mode option.    |

Returns

SMC configuration error code.

### **28.7.11 status\_t SMC\_SetPowerModeVlpr ( SMC\_Type \* *base* )**

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

Returns

SMC configuration error code.

### **28.7.12 status\_t SMC\_SetPowerModeVlpw ( SMC\_Type \* *base* )**

Parameters

---

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

Returns

SMC configuration error code.

### 28.7.13 status\_t SMC\_SetPowerModeVlps ( SMC\_Type \* *base* )

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

Returns

SMC configuration error code.

### 28.7.14 status\_t SMC\_SetPowerModeLls ( SMC\_Type \* *base* )

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

Returns

SMC configuration error code.

### 28.7.15 status\_t SMC\_SetPowerModeVlls ( SMC\_Type \* *base* )

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

Returns

SMC configuration error code.

### 28.7.16 static uint32\_t SMC\_GetPreviousResetSources ( SMC\_Type \* *base* ) [inline], [static]

This function gets the current reset source status. Use source masks defined in the smc\_reset\_source\_t to get the desired source status.

Example: To get all reset source statuses.

```
resetStatus = SMC_GetPreviousResetSources(SMC0) & kSMC_SourceAll;
```

Example: To test whether the MCU is reset using Watchdog.

```
uint32_t resetStatus;

resetStatus = SMC_GetPreviousResetSources(SMC0) &
 kSMC_SourceWdog;
```

Example: To test multiple reset sources.

```
uint32_t resetStatus;

resetStatus = SMC_GetPreviousResetSources(SMC0) & (
 kSMC_SourceWdog | kSMC_SourcePin);
```

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

Returns

All reset source status bit map.

### 28.7.17 static uint32\_t SMC\_GetStickyResetSources ( SMC\_Type \* *base* ) [inline], [static]

This function gets the current reset source status that has not been cleared by software for some specific source.

Example: To get all reset source statuses.

```
uint32_t resetStatus;

resetStatus = SMC_GetStickyResetSources(SMC0) & kSMC_SourceAll;
```

Example, To test whether the MCU is reset using Watchdog.

```
uint32_t resetStatus;

resetStatus = SMC_GetStickyResetSources(SMC0) &
 kSMC_SourceWdog;
```

Example To test multiple reset sources.

```
uint32_t resetStatus;

resetStatus = SMC_GetStickyResetSources(SMC0) & (
 kSMC_SourceWdog | kSMC_SourcePin);
```

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

Returns

All reset source status bit map.

### 28.7.18 static void SMC\_ClearStickyResetSources ( SMC\_Type \* *base*, uint32\_t *sourceMasks* ) [inline], [static]

This function clears the sticky system reset flags indicated by source masks.

Example: Clears multiple reset sources.

```
SMC_ClearStickyResetSources(SMC0, (kSMC_SourceWdog |
 kSMC_SourcePin));
```

Parameters

|                    |                              |
|--------------------|------------------------------|
| <i>base</i>        | SMC peripheral base address. |
| <i>sourceMasks</i> | reset source status bit map  |

### 28.7.19 void SMC\_ConfigureResetPinFilter ( SMC\_Type \* *base*, const smc\_reset\_pin\_filter\_config\_t \* *config* )

This function sets the reset pin filter including the enablement/disablement and filter width.

Parameters

|               |                                         |
|---------------|-----------------------------------------|
| <i>base</i>   | SMC peripheral base address.            |
| <i>config</i> | Pointer to the configuration structure. |

### 28.7.20 static void SMC\_SetSystemResetInterruptConfig ( SMC\_Type \* *base*, uint32\_t *intMask* ) [inline], [static]

For a graceful shut down, the MSMC supports delaying the assertion of the system reset for a period of time when the reset interrupt is generated. This function can be used to enable the interrupt. The interrupts are passed in as bit mask. See smc\_interrupt\_enable\_t for details. For example, to delay a reset after the WDOG timeout or PIN reset occurs, configure as follows: SMC\_SetSystemResetInterruptConfig(SMC0, (kSMC\_IntWdog | kSMC\_IntPin));

Parameters

|                |                                                                                            |
|----------------|--------------------------------------------------------------------------------------------|
| <i>base</i>    | SMC peripheral base address.                                                               |
| <i>intMask</i> | Bit mask of the system reset interrupts to enable. See smc_interrupt_enable_t for details. |

### 28.7.21 static uint32\_t SMC\_GetResetInterruptSourcesStatus ( SMC\_Type \* *base* ) [inline], [static]

This function gets the source status of the reset interrupt. Use source masks defined in the smc\_interrupt\_enable\_t to get the desired source status.

Example: To get all reset interrupt source statuses.

```
uint32_t interruptStatus;

interruptStatus = SMC_GetResetInterruptSourcesStatus(SMC0) &
 kSMC_IntAll;
```

Example: To test whether the reset interrupt of Watchdog is pending.

```
uint32_t interruptStatus;

interruptStatus = SMC_GetResetInterruptSourcesStatus(SMC0) &
 kSMC_IntWdog;
```

Example: To test multiple reset interrupt sources.

```
uint32_t interruptStatus;

interruptStatus = SMC_GetResetInterruptSourcesStatus(SMC0) & (
 kSMC_IntWdog | kSMC_IntPin);
```

Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

Returns

All reset interrupt source status bit map.

### 28.7.22 static void SMC\_ClearResetInterruptSourcesStatus ( SMC\_Type \* *base*, uint32\_t *intMask* ) [inline], [static]

This function clears the source status of the reset interrupt. Use source masks defined in the smc\_interrupt\_enable\_t to get the desired source status.

Example: To clear all reset interrupt source statuses.

```
uint32_t interruptStatus;
MMC_ClearResetInterruptSourcesStatus(SMC0, kSMC_IntAll);
```

Example, To clear the reset interrupt of Watchdog.

```
uint32_t interruptStatus;
SMC_ClearResetInterruptSourcesStatus(SMC0,
 kSMC_IntWdog);
```

Example, To clear multiple reset interrupt sources status.

```
uint32_t interruptStatus;
SMC_ClearResetInterruptSourcesStatus(SMC0, (
 kSMC_IntWdog | kSMC_IntPin));
```

Parameters

|                |                                                     |
|----------------|-----------------------------------------------------|
| <i>base</i>    | SMC peripheral base address.                        |
| <i>intMask</i> | All reset interrupt source status bit map to clear. |

### 28.7.23 static uint32\_t SMC\_GetBootOptionConfig ( SMC\_Type \* *base* ) [inline], [static]

This function gets the boot option configuration of MSMC.

### Parameters

|             |                              |
|-------------|------------------------------|
| <i>base</i> | SMC peripheral base address. |
|-------------|------------------------------|

### Returns

The boot option configuration. 1 means boot option enabled. 0 means not.

# Chapter 29

## MU: Messaging Unit

### 29.1 Overview

The MCUXpresso SDK provides a driver for the MU module of MCUXpresso SDK devices.

### 29.2 Function description

The MU driver provides these functions:

- Functions to initialize the MU module.
- Functions to send and receive messages.
- Functions for MU flags for both MU sides.
- Functions for status flags and interrupts.
- Other miscellaneous functions.

#### 29.2.1 MU initialization

The function [MU\\_Init\(\)](#) initializes the MU module and enables the MU clock. It should be called before any other MU functions.

The function [MU\\_Deinit\(\)](#) deinitializes the MU module and disables the MU clock. No MU functions can be called after this function.

#### 29.2.2 MU message

The MU message must be sent when the transmit register is empty. The MU driver provides blocking API and non-blocking API to send message.

The [MU\\_SendMsgNonBlocking\(\)](#) function writes a message to the MU transmit register without checking the transmit register status. The upper layer should check that the transmit register is empty before calling this function. This function can be used in the ISR for better performance.

The [MU\\_SendMsg\(\)](#) function is a blocking function. It waits until the transmit register is empty and sends the message.

Correspondingly, there are blocking and non-blocking APIs for receiving a message. The [MU\\_ReadMsgNonBlocking\(\)](#) function is a non-blocking API. The [MU\\_ReadMsg\(\)](#) function is the blocking API.

### 29.2.3 MU flags

The MU driver provides 3-bit general purpose flags. When the flags are set on one side, they are reflected on the other side.

The MU flags must be set when the previous flags have been updated to the other side. The MU driver provides a non-blocking function and a blocking function. The blocking function [MU\\_SetFlags\(\)](#) waits until previous flags have been updated to the other side and then sets flags. The non-blocking function sets the flags directly. Ensure that the kMU\_FlagsUpdatingFlag is not pending before calling this function.

The function [MU\\_GetFlags\(\)](#) gets the MU flags on the current side.

### 29.2.4 Status and interrupt

The function [MU\\_GetStatusFlags\(\)](#) returns all MU status flags. Use the `_mu_status_flags` to check for specific flags, for example, to check RX0 and RX1 register full, use the following code:

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/mu. The receive full flags are cleared automatically after messages are read out. The transmit empty flags are cleared automatically after new messages are written to the transmit register. The general purpose interrupt flags must be cleared manually using the function [MU\\_ClearStatusFlags\(\)](#).

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/mu. To enable or disable a specific interrupt, use [MU\\_EnableInterrupts\(\)](#) and [MU\\_DisableInterrupts\(\)](#) functions. The interrupts to enable or disable should be passed in as a bit mask of the `_mu_interrupt_enable`.

The [MU\\_TriggerInterrupts\(\)](#) function triggers general purpose interrupts and NMI to the other core. The interrupts to trigger are passed in as a bit mask of the `_mu_interrupt_trigger`. If previously triggered interrupts have not been processed by the other side, this function returns an error.

### 29.2.5 MU misc functions

The [MU\\_ResetBothSides\(\)](#) function resets MU at both A and B sides. However, only the A side can call this function.

If a core enters stop mode, the platform clock of this core is disabled by default. The function [MU\\_SetClockOnOtherCoreEnable\(\)](#) forces the other core's platform clock to remain enabled even after that core has entered a stop mode. In this case, the other core's platform clock keeps running until the current core enters stop mode too.

## Enumerations

- enum `_mu_status_flags` {
   
  `kMU_Tx0EmptyFlag` = MU\_TX\_FLAG(1UL << 0U),
   
  `kMU_Tx1EmptyFlag` = MU\_TX\_FLAG(1UL << 1U),
   
  `kMU_Tx2EmptyFlag` = MU\_TX\_FLAG(1UL << 2U),
   
  `kMU_Tx3EmptyFlag` = MU\_TX\_FLAG(1UL << 3U),
   
  `kMU_Rx0FullFlag` = MU\_RX\_FLAG(1UL << 0U),
   
  `kMU_Rx1FullFlag` = MU\_RX\_FLAG(1UL << 1U),
   
  `kMU_Rx2FullFlag` = MU\_RX\_FLAG(1UL << 2U),
   
  `kMU_Rx3FullFlag` = MU\_RX\_FLAG(1UL << 3U),
   
  `kMU_GenInt0Flag` = MU\_GI\_FLAG(1UL << 0U),
   
  `kMU_GenInt1Flag` = MU\_GI\_FLAG(1UL << 1U),
   
  `kMU_GenInt2Flag` = MU\_GI\_FLAG(1UL << 2U),
   
  `kMU_GenInt3Flag` = MU\_GI\_FLAG(1UL << 3U),
   
  `kMU_CoreEventPendingFlag` = MU\_STAT\_FLAG(MU\_SR\_CEP\_MASK),
   
  `kMU_RxFullPendingFlag` = MU\_STAT\_FLAG(MU\_SR\_RFP\_MASK),
   
  `kMU_TxEmptyPendingFlag` = MU\_STAT\_FLAG(MU\_SR\_TEP\_MASK),
   
  `kMU_GenIntPendingFlag` = MU\_STAT\_FLAG(MU\_SR\_GIRP\_MASK),
   
  `kMU_EventPendingFlag` = MU\_STAT\_FLAG(MU\_SR\_EP\_MASK),
   
  `kMU_FlagsUpdatingFlag` = MU\_STAT\_FLAG(MU\_SR\_FUP\_MASK),
   
  `kMU_MuInResetFlag` = MU\_STAT\_FLAG(MU\_SR\_MURS\_MASK),
   
  `kMU_MuResetInterruptFlag` = MU\_STAT\_FLAG(MU\_SR\_MURIP\_MASK),
   
  `kMU_OtherSideEnterRunInterruptFlag` = MU\_CORE\_FLAG(MU\_CSSR0\_RUN\_MASK),
   
  `kMU_OtherSideEnterHaltInterruptFlag` = MU\_CORE\_FLAG(MU\_CSSR0\_HALT\_MASK),
   
  `kMU_OtherSideEnterWaitInterruptFlag` = MU\_CORE\_FLAG(MU\_CSSR0\_WAIT\_MASK),
   
  `kMU_OtherSideEnterStopInterruptFlag` = MU\_CORE\_FLAG(MU\_CSSR0\_STOP\_MASK),
   
  `kMU_OtherSideEnterPowerDownInterruptFlag` = MU\_CORE\_FLAG(MU\_CSSR0\_PD\_MASK),
   
  `kMU_ResetAssertInterruptFlag` = MU\_CORE\_FLAG(MU\_CSSR0\_RAIP\_MASK),
   
  `kMU_HardwareResetInterruptFlag` = MU\_CORE\_FLAG(MU\_CSSR0\_HRIP\_MASK) }
- MU status flags.*
- enum `_mu_interrupt_enable` {

```

kMU_Tx0EmptyInterruptEnable = MU_TX_INTR(1UL << 0U),
kMU_Tx1EmptyInterruptEnable = MU_TX_INTR(1UL << 1U),
kMU_Tx2EmptyInterruptEnable = MU_TX_INTR(1UL << 2U),
kMU_Tx3EmptyInterruptEnable = MU_TX_INTR(1UL << 3U),
kMU_Rx0FullInterruptEnable = MU_RX_INTR(1UL << 0U),
kMU_Rx1FullInterruptEnable = MU_RX_INTR(1UL << 1U),
kMU_Rx2FullInterruptEnable = MU_RX_INTR(1UL << 2U),
kMU_Rx3FullInterruptEnable = MU_RX_INTR(1UL << 3U),
kMU_GenInt0InterruptEnable = MU_GI_INTR(1UL << 0U),
kMU_GenInt1InterruptEnable = MU_GI_INTR(1UL << 1U),
kMU_GenInt2InterruptEnable = MU_GI_INTR(1UL << 2U),
kMU_GenInt3InterruptEnable = MU_GI_INTR(1UL << 3U),
kMU_OtherSideEnterRunInterruptEnable = MU_CORE_INTR(MU_CIER0_RUNIE_MASK),
kMU_OtherSideEnterHaltInterruptEnable = MU_CORE_INTR(MU_CIER0_HALTIE_MASK),
kMU_OtherSideEnterWaitInterruptEnable = MU_CORE_INTR(MU_CIER0_WAITIE_MASK),
kMU_OtherSideEnterStopInterruptEnable = MU_CORE_INTR(MU_CIER0_STOPIE_MASK),
kMU_OtherSideEnterPowerDownInterruptEnable = MU_CORE_INTR(MU_CIER0_PDIE_MASK),
kMU_ResetAssertInterruptEnable = MU_CORE_INTR(MU_CIER0_RAIE_MASK),
kMU_HardwareResetInterruptEnable = MU_CORE_INTR(MU_CIER0_HRIE_MASK),
kMU_MuResetInterruptEnable = MU_MISC_INTR(MU_CR_MURIE_MASK) }

```

*MU interrupt source to enable.*

- enum `_mu_interrupt_trigger` {
   
kMU\_GenInt0InterruptTrigger = 1U << 0U,
   
kMU\_GenInt1InterruptTrigger = 1U << 1U,
   
kMU\_GenInt2InterruptTrigger = 1U << 2U,
   
kMU\_GenInt3InterruptTrigger = 1U << 3U }

*MU interrupt that could be triggered to the other core.*

- enum `_mu_core_status_flags` {
   
kMU\_OtherSideEnterRunFlag = MU\_CSSR0\_RUN\_MASK,
   
kMU\_OtherSideEnterHaltFlag = MU\_CSSR0\_HALT\_MASK,
   
kMU\_OtherSideEnterWaitFlag = MU\_CSSR0\_WAIT\_MASK,
   
kMU\_OtherSideEnterStopFlag = MU\_CSSR0\_STOP\_MASK,
   
kMU\_OtherSideEnterPowerDownFlag = MU\_CSSR0\_PD\_MASK,
   
kMU\_OtherSideEnterResetFlag = MU\_CSSR0\_RAIP\_MASK,
   
kMU\_HardwareResetFlag = MU\_CSSR0\_HRIP\_MASK }

*MU core status flags.*

- enum `mu_msg_reg_index_t`
  
*MU message register index.*

## Driver version

- #define `FSL_MU_DRIVER_VERSION` (`MAKE_VERSION(2, 1, 1)`)
   
*MU driver version.*

## MU initialization.

- void **MU\_Init** (MU\_Type \*base)  
*Initializes the MU module.*
- void **MU\_Deinit** (MU\_Type \*base)  
*De-initializes the MU module.*

## MU Message

- static void **MU\_SendMsgNonBlocking** (MU\_Type \*base, uint32\_t regIndex, uint32\_t msg)  
*Writes a message to the TX register.*
- void **MU\_SendMsg** (MU\_Type \*base, uint32\_t regIndex, uint32\_t msg)  
*Blocks to send a message.*
- static uint32\_t **MU\_ReceiveMsgNonBlocking** (MU\_Type \*base, uint32\_t regIndex)  
*Reads a message from the RX register.*
- uint32\_t **MU\_ReceiveMsg** (MU\_Type \*base, uint32\_t regIndex)  
*Blocks to receive a message.*

## MU Flags

- static void **MU\_SetFlagsNonBlocking** (MU\_Type \*base, uint32\_t flags)  
*Sets the 3-bit MU flags reflect on the other MU side.*
- void **MU\_SetFlags** (MU\_Type \*base, uint32\_t flags)  
*Blocks setting the 3-bit MU flags reflect on the other MU side.*
- static uint32\_t **MU\_GetFlags** (MU\_Type \*base)  
*Gets the current value of the 3-bit MU flags set by the other side.*

## Status and Interrupt.

- static uint32\_t **MU\_GetCoreStatusFlags** (MU\_Type \*base)  
*Gets the MU core status flags.*
- uint32\_t **MU\_GetStatusFlags** (MU\_Type \*base)  
*Gets the MU status flags.*
- static void **MU\_ClearStatusFlags** (MU\_Type \*base, uint32\_t flags)  
*Clears the specific MU status flags.*
- static void **MU\_EnableInterrupts** (MU\_Type \*base, uint32\_t interrupts)  
*Enables the specific MU interrupts.*
- static void **MU\_DisableInterrupts** (MU\_Type \*base, uint32\_t interrupts)  
*Disables the specific MU interrupts.*
- **status\_t MU\_TriggerInterrupts** (MU\_Type \*base, uint32\_t interrupts)  
*Triggers interrupts to the other core.*
- **status\_t MU\_TriggerNmi** (MU\_Type \*base)  
*Triggers NMI to the other core.*
- static void **MU\_ClearNmi** (MU\_Type \*base)  
*Clear non-maskable interrupt (NMI) sent by the other core.*

## MU misc functions

- void **MU\_BootOtherCore** (MU\_Type \*base, mu\_core\_boot\_mode\_t mode)  
*Boots the other core.*
- void **MU\_HoldOtherCoreReset** (MU\_Type \*base)

- static void **MU\_ResetBothSides** (MU\_Type \*base)  
*Holds the other core reset.*
- static void **MU\_SetClockOnOtherCoreEnable** (MU\_Type \*base, bool enable)  
*Resets the MU for both A side and B side.*
- static void **MU\_HardwareResetOtherCore** (MU\_Type \*base, bool waitReset, bool holdReset, mu\_core\_boot\_mode\_t bootMode)  
*Enables or disables the clock on the other core.*
- static void **MU\_MaskHardwareReset** (MU\_Type \*base, bool mask)  
*Hardware reset the other core.*
- static void **MU\_ResetAssertInterruptFlag** (MU\_Type \*base)  
*Mask hardware reset by the other core.*

## 29.3 Macro Definition Documentation

### 29.3.1 #define FSL\_MU\_DRIVER\_VERSION (MAKE\_VERSION(2, 1, 1))

## 29.4 Enumeration Type Documentation

### 29.4.1 enum \_mu\_status\_flags

Enumerator

- kMU\_Tx0EmptyFlag** TX0 empty.
- kMU\_Tx1EmptyFlag** TX1 empty.
- kMU\_Tx2EmptyFlag** TX2 empty.
- kMU\_Tx3EmptyFlag** TX3 empty.
- kMU\_Rx0FullFlag** RX0 full.
- kMU\_Rx1FullFlag** RX1 full.
- kMU\_Rx2FullFlag** RX2 full.
- kMU\_Rx3FullFlag** RX3 full.
- kMU\_GenInt0Flag** General purpose interrupt 0 pending.
- kMU\_GenInt1Flag** General purpose interrupt 0 pending.
- kMU\_GenInt2Flag** General purpose interrupt 0 pending.
- kMU\_GenInt3Flag** General purpose interrupt 0 pending.
- kMU\_CoreEventPendingFlag** The other core mode entry event pending.
- kMU\_RxFullPendingFlag** Any RX full flag is pending.
- kMU\_TxEmptyPendingFlag** Any TX empty flag is pending.
- kMU\_GenIntPendingFlag** Any general interrupt flag is pending.
- kMU\_EventPendingFlag** MU event pending.
- kMU\_FlagsUpdatingFlag** MU flags update is on-going.
- kMU\_MuInResetFlag** MU of any side is in reset.
- kMU\_MuResetInterruptFlag** The other side initializes MU reset.
- kMU\_OtherSideEnterRunInterruptFlag** The other side enters run mode.
- kMU\_OtherSideEnterHaltInterruptFlag** The other side enters halt mode.
- kMU\_OtherSideEnterWaitInterruptFlag** The other side enters wait mode.
- kMU\_OtherSideEnterStopInterruptFlag** The other side enters stop mode.
- kMU\_OtherSideEnterPowerDownInterruptFlag** The other side enters power down mode.
- kMU\_ResetAssertInterruptFlag** The other core reset assert interrupt.

***kMU\_HardwareResetInterruptFlag*** Current side has been hardware reset by the other side.

#### 29.4.2 enum \_mu\_interrupt\_enable

Enumerator

***kMU\_Tx0EmptyInterruptEnable*** TX0 empty.  
***kMU\_Tx1EmptyInterruptEnable*** TX1 empty.  
***kMU\_Tx2EmptyInterruptEnable*** TX2 empty.  
***kMU\_Tx3EmptyInterruptEnable*** TX3 empty.  
***kMU\_Rx0FullInterruptEnable*** RX0 full.  
***kMU\_Rx1FullInterruptEnable*** RX1 full.  
***kMU\_Rx2FullInterruptEnable*** RX2 full.  
***kMU\_Rx3FullInterruptEnable*** RX3 full.  
***kMU\_GenInt0InterruptEnable*** General purpose interrupt 0.  
***kMU\_GenInt1InterruptEnable*** General purpose interrupt 1.  
***kMU\_GenInt2InterruptEnable*** General purpose interrupt 2.  
***kMU\_GenInt3InterruptEnable*** General purpose interrupt 3.  
***kMU\_OtherSideEnterRunInterruptEnable*** The other side enters run mode.  
***kMU\_OtherSideEnterHaltInterruptEnable*** The other side enters halt mode.  
***kMU\_OtherSideEnterWaitInterruptEnable*** The other side enters wait mode.  
***kMU\_OtherSideEnterStopInterruptEnable*** The other side enters stop mode.  
***kMU\_OtherSideEnterPowerDownInterruptEnable*** The other side enters power down mode.  
***kMU\_ResetAssertInterruptEnable*** The other core reset assert interrupt.  
***kMU\_HardwareResetInterruptEnable*** Current side has been hardware reset by the other side.  
***kMU\_MuResetInterruptEnable*** The other side initializes MU reset.

#### 29.4.3 enum \_mu\_interrupt\_trigger

Enumerator

***kMU\_GenInt0InterruptTrigger*** General purpose interrupt 0.  
***kMU\_GenInt1InterruptTrigger*** General purpose interrupt 1.  
***kMU\_GenInt2InterruptTrigger*** General purpose interrupt 2.  
***kMU\_GenInt3InterruptTrigger*** General purpose interrupt 3.

#### 29.4.4 enum \_mu\_core\_status\_flags

Enumerator

***kMU\_OtherSideEnterRunFlag*** The other side in run mode.

- kMU\_OtherSideEnterHaltFlag*** The other side in halt mode.
- kMU\_OtherSideEnterWaitFlag*** The other side in wait mode.
- kMU\_OtherSideEnterStopFlag*** The other side in stop mode.
- kMU\_OtherSideEnterPowerDownFlag*** The other side in power down mode.
- kMU\_OtherSideEnterResetFlag*** The other core entered reset.
- kMU\_HardwareResetFlag*** Current side has been hardware reset by the other side.

## 29.5 Function Documentation

### 29.5.1 void MU\_Init ( MU\_Type \* *base* )

This function enables the MU clock only.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

### 29.5.2 void MU\_Deinit ( MU\_Type \* *base* )

This function disables the MU clock only.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

### 29.5.3 static void MU\_SendMsgNonBlocking ( MU\_Type \* *base*, uint32\_t *regIndex*, uint32\_t *msg* ) [inline], [static]

This function writes a message to the specific TX register. It does not check whether the TX register is empty or not. The upper layer should make sure the TX register is empty before calling this function. This function can be used in ISR for better performance.

```
* while (!(kMU_Tx0EmptyFlag & MU_GetStatusFlags(base))) { } Wait for TX0
 register empty.
* MU_SendMsgNonBlocking(base, kMU_MsgReg0, MSG_VAL); Write message to the TX0
 register.
*
```

Parameters

|                 |                                                             |
|-----------------|-------------------------------------------------------------|
| <i>base</i>     | MU peripheral base address.                                 |
| <i>regIndex</i> | TX register index, see <a href="#">mu_msg_reg_index_t</a> . |
| <i>msg</i>      | Message to send.                                            |

#### 29.5.4 void MU\_SendMsg ( MU\_Type \* *base*, uint32\_t *regIndex*, uint32\_t *msg* )

This function waits until the TX register is empty and sends the message.

Parameters

|                 |                                                             |
|-----------------|-------------------------------------------------------------|
| <i>base</i>     | MU peripheral base address.                                 |
| <i>regIndex</i> | MU message register, see <a href="#">mu_msg_reg_index_t</a> |
| <i>msg</i>      | Message to send.                                            |

#### 29.5.5 static uint32\_t MU\_ReceiveMsgNonBlocking ( MU\_Type \* *base*, uint32\_t *regIndex* ) [inline], [static]

This function reads a message from the specific RX register. It does not check whether the RX register is full or not. The upper layer should make sure the RX register is full before calling this function. This function can be used in ISR for better performance.

```
* uint32_t msg;
* while (!(kMU_Rx0FullFlag & MU_GetStatusFlags(base)))
* {
* } Wait for the RX0 register full.
*
* msg = MU_ReceiveMsgNonBlocking(base, kMU_MsgReg0); Read message from RX0
* register.
*
```

Parameters

|                 |                                                             |
|-----------------|-------------------------------------------------------------|
| <i>base</i>     | MU peripheral base address.                                 |
| <i>regIndex</i> | RX register index, see <a href="#">mu_msg_reg_index_t</a> . |

Returns

The received message.

### 29.5.6 `uint32_t MU_ReceiveMsg ( MU_Type * base, uint32_t regIndex )`

This function waits until the RX register is full and receives the message.

## Parameters

|                 |                                                             |
|-----------------|-------------------------------------------------------------|
| <i>base</i>     | MU peripheral base address.                                 |
| <i>regIndex</i> | MU message register, see <a href="#">mu_msg_reg_index_t</a> |

## Returns

The received message.

### 29.5.7 static void MU\_SetFlagsNonBlocking ( MU\_Type \* *base*, uint32\_t *flags* ) [inline], [static]

This function sets the 3-bit MU flags directly. Every time the 3-bit MU flags are changed, the status flag kMU\_FlagsUpdatingFlag asserts indicating the 3-bit MU flags are updating to the other side. After the 3-bit MU flags are updated, the status flag kMU\_FlagsUpdatingFlag is cleared by hardware. During the flags updating period, the flags cannot be changed. The upper layer should make sure the status flag kMU\_FlagsUpdatingFlag is cleared before calling this function.

```
* while (kMU_FlagsUpdatingFlag & MU_GetStatusFlags(base))
{
} Wait for previous MU flags updating.
*
* MU_SetFlagsNonBlocking(base, 0U); Set the mU flags.
*
```

## Parameters

|              |                             |
|--------------|-----------------------------|
| <i>base</i>  | MU peripheral base address. |
| <i>flags</i> | The 3-bit MU flags to set.  |

### 29.5.8 void MU\_SetFlags ( MU\_Type \* *base*, uint32\_t *flags* )

This function blocks setting the 3-bit MU flags. Every time the 3-bit MU flags are changed, the status flag kMU\_FlagsUpdatingFlag asserts indicating the 3-bit MU flags are updating to the other side. After the 3-bit MU flags are updated, the status flag kMU\_FlagsUpdatingFlag is cleared by hardware. During the flags updating period, the flags cannot be changed. This function waits for the MU status flag kMU\_FlagsUpdatingFlag cleared and sets the 3-bit MU flags.

Parameters

|              |                             |
|--------------|-----------------------------|
| <i>base</i>  | MU peripheral base address. |
| <i>flags</i> | The 3-bit MU flags to set.  |

### 29.5.9 static uint32\_t MU\_GetFlags ( MU\_Type \* *base* ) [inline], [static]

This function gets the current 3-bit MU flags on the current side.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

Returns

*flags* Current value of the 3-bit flags.

### 29.5.10 static uint32\_t MU\_GetCoreStatusFlags ( MU\_Type \* *base* ) [inline], [static]

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

Returns

Bit mask of the MU status flags, see [\\_mu\\_core\\_status\\_flags](#).

### 29.5.11 uint32\_t MU\_GetStatusFlags ( MU\_Type \* *base* )

This function returns the bit mask of the MU status flags. See [\\_mu\\_status\\_flags](#).

```
* uint32_t flags;
* flags = MU_GetStatusFlags(base); Get all status flags.
* if (kMU_Tx0EmptyFlag & flags)
* {
* The TX0 register is empty. Message can be sent.
* MU_SendMsgNonBlocking(base, kMU_MsgReg0, MSG0_VAL);
* }
* if (kMU_Tx1EmptyFlag & flags)
* {
* The TX1 register is empty. Message can be sent.
* MU_SendMsgNonBlocking(base, kMU_MsgReg1, MSG1_VAL);
* }
```

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

Returns

Bit mask of the MU status flags, see `_mu_status_flags`.

### 29.5.12 static void MU\_ClearStatusFlags ( MU\_Type \* *base*, uint32\_t *flags* ) [inline], [static]

This function clears the specific MU status flags. The flags to clear should be passed in as bit mask. See `_mu_status_flags`.

```
* Clear general interrupt 0 and general interrupt 1 pending flags.
* MU_ClearStatusFlags(base, kMU_GenInt0Flag |
* kMU_GenInt1Flag);
*
```

Parameters

|              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>  | MU peripheral base address.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| <i>flags</i> | Bit mask of the MU status flags. See <code>_mu_status_flags</code> . Only the following flags can be cleared by software, other flags are cleared by hardware: <ul style="list-style-type: none"> <li>• <a href="#">kMU_GenInt0Flag</a></li> <li>• <a href="#">kMU_GenInt1Flag</a></li> <li>• <a href="#">kMU_GenInt2Flag</a></li> <li>• <a href="#">kMU_GenInt3Flag</a></li> <li>• <a href="#">kMU_MuResetInterruptFlag</a></li> <li>• <a href="#">kMU_OtherSideEnterRunInterruptFlag</a></li> <li>• <a href="#">kMU_OtherSideEnterHaltInterruptFlag</a></li> <li>• <a href="#">kMU_OtherSideEnterWaitInterruptFlag</a></li> <li>• <a href="#">kMU_OtherSideEnterStopInterruptFlag</a></li> <li>• <a href="#">kMU_OtherSideEnterPowerDownInterruptFlag</a></li> <li>• <a href="#">kMU_ResetAssertInterruptFlag</a></li> <li>• <a href="#">kMU_HardwareResetInterruptFlag</a></li> </ul> |

### 29.5.13 static void MU\_EnableInterrupts ( MU\_Type \* *base*, uint32\_t *interrupts* ) [inline], [static]

This function enables the specific MU interrupts. The interrupts to enable should be passed in as bit mask. See `_mu_interrupt_enable`.

```
* Enable general interrupt 0 and TX0 empty interrupt.
* MU_EnableInterrupts(base, kMU_GenInt0InterruptEnable |
* kMU_Tx0EmptyInterruptEnable);
*
```

## Parameters

|                   |                                                                        |
|-------------------|------------------------------------------------------------------------|
| <i>base</i>       | MU peripheral base address.                                            |
| <i>interrupts</i> | Bit mask of the MU interrupts. See <code>_mu_interrupt_enable</code> . |

### 29.5.14 static void MU\_DisableInterrupts ( MU\_Type \* *base*, uint32\_t *interrupts* ) [inline], [static]

This function disables the specific MU interrupts. The interrupts to disable should be passed in as bit mask. See `_mu_interrupt_enable`.

```
* Disable general interrupt 0 and TX0 empty interrupt.
* MU_DisableInterrupts(base, kMU_GenInt0InterruptEnable |
* kMU_Tx0EmptyInterruptEnable);
*
```

## Parameters

|                   |                                                                        |
|-------------------|------------------------------------------------------------------------|
| <i>base</i>       | MU peripheral base address.                                            |
| <i>interrupts</i> | Bit mask of the MU interrupts. See <code>_mu_interrupt_enable</code> . |

### 29.5.15 status\_t MU\_TriggerInterrupts ( MU\_Type \* *base*, uint32\_t *interrupts* )

This function triggers the specific interrupts to the other core. The interrupts to trigger are passed in as bit mask. See `_mu_interrupt_trigger`. The MU should not trigger an interrupt to the other core when the previous interrupt has not been processed by the other core. This function checks whether the previous interrupts have been processed. If not, it returns an error.

```
* if (kStatus_Success != MU_TriggerInterrupts(base,
* kMU_GenInt0InterruptTrigger |
* kMU_GenInt2InterruptTrigger))
* {
* Previous general purpose interrupt 0 or general purpose interrupt 2
* has not been processed by the other core.
* }
*
```

Parameters

|                   |                                                                                 |
|-------------------|---------------------------------------------------------------------------------|
| <i>base</i>       | MU peripheral base address.                                                     |
| <i>interrupts</i> | Bit mask of the interrupts to trigger. See <code>_mu_interrupt_trigger</code> . |

Return values

|                        |                                              |
|------------------------|----------------------------------------------|
| <i>kStatus_Success</i> | Interrupts have been triggered successfully. |
| <i>kStatus_Fail</i>    | Previous interrupts have not been accepted.  |

### 29.5.16 `status_t MU_TriggerNmi ( MU_Type * base )`

This function triggers the NMI to the other core. The MU should not trigger NMI to the other core when the previous interrupt has not been processed by the other core. This function checks whether the previous interrupts have been processed. If not, it returns an error.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

Return values

|                        |                                              |
|------------------------|----------------------------------------------|
| <i>kStatus_Success</i> | Interrupts have been triggered successfully. |
| <i>kStatus_Fail</i>    | Previous interrupts have not been accepted.  |

### 29.5.17 `static void MU_ClearNmi ( MU_Type * base ) [inline], [static]`

This function clears non-maskable interrupt (NMI) sent by the other core.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

### 29.5.18 `void MU_BootOtherCore ( MU_Type * base, mu_core_boot_mode_t mode )`

This function boots the other core with a boot configuration.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
| <i>mode</i> | The other core boot mode.   |

### 29.5.19 void MU\_HoldOtherCoreReset ( MU\_Type \* *base* )

This function causes the other core to be held in reset following any reset event.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

### 29.5.20 static void MU\_ResetBothSides ( MU\_Type \* *base* ) [inline], [static]

This function resets the MU for both A side and B side. Before reset, it is recommended to interrupt processor B, because this function may affect the ongoing processor B programs.

Parameters

|             |                             |
|-------------|-----------------------------|
| <i>base</i> | MU peripheral base address. |
|-------------|-----------------------------|

### 29.5.21 static void MU\_SetClockOnOtherCoreEnable ( MU\_Type \* *base*, bool *enable* ) [inline], [static]

This function enables or disables the platform clock on the other core when that core enters a stop mode. If disabled, the platform clock for the other core is disabled when it enters stop mode. If enabled, the platform clock keeps running on the other core in stop mode, until this core also enters stop mode.

Parameters

|               |                                                |
|---------------|------------------------------------------------|
| <i>base</i>   | MU peripheral base address.                    |
| <i>enable</i> | Enable or disable the clock on the other core. |

### 29.5.22 void MU\_HardwareResetOtherCore ( MU\_Type \* *base*, bool *waitReset*, bool *holdReset*, mu\_core\_boot\_mode\_t *bootMode* )

This function resets the other core, the other core could mask the hardware reset by calling MU\_MaskHardwareReset. The hardware reset mask feature is only available for some platforms. This function could be used together with MU\_BootOtherCore to control the other core reset workflow.

Example 1: Reset the other core, and no hold reset

```
* MU_HardwareResetOtherCore(MU_A, true, false, bootMode);
*
```

In this example, the core at MU side B will reset with the specified boot mode.

Example 2: Reset the other core and hold it, then boot the other core later.

```
* Here the other core enters reset, and the reset is hold
* MU_HardwareResetOtherCore(MU_A, true, true, modeDontCare);
* Current core boot the other core when necessary.
* MU_BootOtherCore(MU_A, bootMode);
*
```

#### Parameters

|                  |                                                                                                                                                                                                                                                                                                         |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>base</i>      | MU peripheral base address.                                                                                                                                                                                                                                                                             |
| <i>waitReset</i> | Wait the other core enters reset. <ul style="list-style-type: none"> <li>• true: Wait until the other core enters reset, if the other core has masked the hardware reset, then this function will be blocked.</li> <li>• false: Don't wait the reset.</li> </ul>                                        |
| <i>holdReset</i> | Hold the other core reset or not. <ul style="list-style-type: none"> <li>• true: Hold the other core in reset, this function returns directly when the other core enters reset.</li> <li>• false: Don't hold the other core in reset, this function waits until the other core out of reset.</li> </ul> |

|                 |                                                                                            |
|-----------------|--------------------------------------------------------------------------------------------|
| <i>bootMode</i> | Boot mode of the other core, if <code>holdReset</code> is true, this parameter is useless. |
|-----------------|--------------------------------------------------------------------------------------------|

### 29.5.23 static void MU\_MaskHardwareReset ( MU\_Type \* *base*, bool *mask* ) [inline], [static]

The other core could call [MU\\_HardwareResetOtherCore\(\)](#) to reset current core. To mask the reset, call this function and pass in true.

Parameters

|             |                                                                |
|-------------|----------------------------------------------------------------|
| <i>base</i> | MU peripheral base address.                                    |
| <i>mask</i> | Pass true to mask the hardware reset, pass false to unmask it. |

# Chapter 30

## PMC0: Power Management Controller

### 30.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Power Management Controller (PMC) module of MCUXpresso SDK devices. The Power Management Controller (PMC) can be divided in two parts: PMC 0 and PMC 1. The PMC 0 controls the Core 0, its SoG and RAM, and the PMC 1 controls the Core 1, its SoG and RAM. This driver is for PMC 0 only.

The PMC 0 has:

- the high-power (HP) and low-power (LP) Core Regulator;
- the high-power (HP) and low-power (LP) Array Regulator;
- the high-power (HP) and low-power (LP) 1.2V Low Voltage Detector (LVD) monitor (in regulators input);
- the high-power (HP) and low-power (LP) 1.2V High Voltage Detector (HVD) monitor (in regulators input);
- the bandgap;
- the forward bias (FBB) and the reverse back bias (RBB). In addition, the PMC has a 1.8 V POR (Power-On Reset) monitor to assure the voltage level in the Always-On power domain would be in the correct range to the correct functionality of the internal digital and analog blocks. Both PMCs receive requests from the MSMC to change the current power mode. Each PMC allows the customer to choose what features are enabled or disabled for each power mode using the PMC registers.

### 30.2 Typical use case

#### 30.2.1 Turn on the PMC 1 using LDO Regulator

After a POR event, when the PMC 0 is during RUN mode and the PMC 1 is turned off. The procedure to turn on the PMC 1 using the internal LDO Regulator.

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pmc0

#### 30.2.2 Turn on the PMC 1 using the PMIC

After a POR event, when the PMC 0 is during RUN mode and the PMC 1 is turned off. The procedure to turn on the PMC 1 using the external PMIC

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pmc0

### 30.2.3 Turn off the LDO Regulator

When the PMC 1 is during RUN mode, the LDO Regulator can be programmed to be turned off in the next transition from RUN to VLLS power mode. As in VLLS the regulator is disconnected from the load by the switches (switches are OFF), a external regulator can assume the power supply (PMIC).

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pmc0

### 30.2.4 Turn on the LDO Regulator

When the PMC 1 is during VLLS mode, the LDO Regulator can be turned on in a transition to RUN mode.

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pmc0

### 30.2.5 Change the Core Regulator voltage level in PMC 0 RUN or HSRUN mode

To change the Core Regulator voltage level when the PMC 0 is in RUN mode:

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pmc0

To change the Core Regulator voltage level when the PMC 0 is in HSRUN mode:

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pmc0

### 30.2.6 Change the SRAMs power mode during PMC 0 RUN mode

To change the SRAMs power mode during the PMC 0 RUN mode.

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/pmc0

## Files

- file [fsl\\_pmc0.h](#)

## Data Structures

- struct [pmc0\\_hsrn\\_mode\\_config\\_t](#)  
*PMC 0 HSRUN mode configuration.* [More...](#)
- struct [pmc0\\_run\\_mode\\_config\\_t](#)  
*PMC 0 RUN mode configuration.* [More...](#)
- struct [pmc0\\_vlpr\\_mode\\_config\\_t](#)  
*PMC 0 VLPR mode configuration.* [More...](#)
- struct [pmc0\\_stop\\_mode\\_config\\_t](#)  
*PMC 0 STOP mode configuration.* [More...](#)

- struct `pmc0_vlps_mode_config_t`  
*PMC 0 VLPS mode configuration. [More...](#)*
- struct `pmc0_lls_mode_config_t`  
*PMC 0 LLS mode configuration. [More...](#)*
- struct `pmc0_vlls_mode_config_t`  
*PMC 0 VLLS mode configuration. [More...](#)*
- struct `pmc0_bias_config_t`  
*PMC 0 bias configuration. [More...](#)*

## Macros

- `#define CORE_REGULATOR_VOLT_LEVEL_MAX 50U`  
*MAX valid values of Core Regulator Voltage Level.*

## Enumerations

- enum `pmc0_high_volt_detect_monitor_select_t` {
   
`kPMC0_HighVoltDetectLowPowerMonitor = 0U,`
  
`kPMC0_HighVoltDetectHighPowerMonitor = 1U }`
  
*High Voltage Detect Monitor Select.*
- enum `pmc0_low_volt_detect_monitor_select_t` {
   
`kPMC0_LowVoltDetectLowPowerMonitor = 0U,`
  
`kPMC0_LowVoltDetectHighPowerMonitor = 1U }`
  
*Low Voltage Detect Monitor Select.*
- enum `pmc0_core_regulator_select_t` {
   
`kPMC0_CoreLowPowerRegulator = 0U,`
  
`kPMC0_CoreHighPowerRegulator = 1U }`
  
*Core Regulator Select.*
- enum `pmc0_array_regulator_select_t` {
   
`kPMC0_ArrayLowPowerRegulator = 0U,`
  
`kPMC0_ArrayHighPowerRegulator = 1U }`
  
*Array Regulator Select.*
- enum `pmc0_vlls_array_regulator_select_t` {
   
`kPMC0_VllsArrayRegulatorOff = 0U,`
  
`kPMC0_VllsArrayLowPowerRegulator = 2U,`
  
`kPMC0_VllsArrayHighPowerRegulator = 3U }`
  
*VLLS mode array Regulator Select.*
- enum `pmc0_fbb_p_well_voltage_level_select_t` {
   
`kPMC0_FbbPWellNoBiasCondition = 0U,`
  
`kPMC0_FbbPWellVoltageLevelAt50Mv = 1U,`
  
`kPMC0_FbbPWellVoltageLevelAt150Mv = 2U,`
  
`kPMC0_FbbPWellVoltageLevelAt100Mv = 3U,`
  
`kPMC0_FbbPWellVoltageLevelAt350Mv = 4U,`
  
`kPMC0_FbbPWellVoltageLevelAt300Mv = 5U,`
  
`kPMC0_FbbPWellVoltageLevelAt200Mv = 6U,`
  
`kPMC0_FbbPWellVoltageLevelAt250Mv = 7U }`
  
*FBB P-Well voltage level select.*

- enum pmc0\_fbb\_n\_well\_voltage\_level\_select\_t {
 kPMC0\_FbbNWellNoBiasCondition = 0U,
 kPMC0\_FbbNWellVoltageLevelAtMinus50Mv = 1U,
 kPMC0\_FbbNWellVoltageLevelAtMinus150Mv = 2U,
 kPMC0\_FbbNWellVoltageLevelAtMinus100Mv = 3U,
 kPMC0\_FbbNWellVoltageLevelAtMinus350Mv = 4U,
 kPMC0\_FbbNWellVoltageLevelAtMinus300Mv = 5U,
 kPMC0\_FbbNWellVoltageLevelAtMinus200Mv = 6U,
 kPMC0\_FbbNWellVoltageLevelAtMinus250Mv = 7U }

*FBB N-Well voltage level select.*

- enum pmc0\_rbb\_p\_well\_voltage\_level\_select\_t {
 kPMC0\_RBBPWellVoltageLevelAtMinus0\_5V = 0U,
 kPMC0\_RBBPWellVoltageLevelAtMinus0\_6V = 1U,
 kPMC0\_RBBPWellVoltageLevelAtMinus0\_7V = 2U,
 kPMC0\_RBBPWellVoltageLevelAtMinus0\_8V = 3U,
 kPMC0\_RBBPWellVoltageLevelAtMinus0\_9V = 4U,
 kPMC0\_RBBPWellVoltageLevelAtMinus1\_0V = 5U,
 kPMC0\_RBBPWellVoltageLevelAtMinus1\_1V = 6U,
 kPMC0\_RBBPWellVoltageLevelAtMinus1\_2V = 7U,
 kPMC0\_RBBPWellVoltageLevelAtMinus1\_3V = 8U }

*RBB P-Well voltage level select.*

- enum pmc0\_rbb\_n\_well\_voltage\_level\_select\_t {
 kPMC0\_RBBNWellVoltageLevelAt0\_5V = 0U,
 kPMC0\_RBBNWellVoltageLevelAt0\_6V = 1U,
 kPMC0\_RBBNWellVoltageLevelAt0\_7V = 2U,
 kPMC0\_RBBNWellVoltageLevelAt0\_8V = 3U,
 kPMC0\_RBBNWellVoltageLevelAt0\_9V = 4U,
 kPMC0\_RBBNWellVoltageLevelAt1\_0V = 5U,
 kPMC0\_RBBNWellVoltageLevelAt1\_1V = 6U,
 kPMC0\_RBBNWellVoltageLevelAt1\_2V = 7U,
 kPMC0\_RBBNWellVoltageLevelAt1\_3V = 8U }

*RBB N-Well voltage level select.*

- enum \_pmc0\_status\_flags {
 kPMC0\_LowVoltDetectEventFlag,
 kPMC0\_LowVoltDetectValueFlag = PMC0\_STATUS\_LVDV\_MASK,
 kPMC0\_HighVoltDetectEventFlag,
 kPMC0\_HighVoltDetectValueFlag = PMC0\_STATUS\_HVDV\_MASK,
 kPMC0\_CoreRegulatorVoltLevelFlag = PMC0\_STATUS\_COREVLF\_MASK,
 kPMC0\_SramFlag,
 kPMC0\_PMC1VoltageSourceFlag }

*PMC 0 status flags.*

- enum \_pmc0\_power\_mode\_status\_flags {

```
kPMC0_HSRUNModeStatusFlags = 0U,
kPMC0_RUNModeStatusFlags = 1U,
kPMC0_STOPModeStatusFlags = 2U,
kPMC0_VLPRModeStatusFlags = 3U,
kPMC0_VLPSPModeStatusFlags = 4U,
kPMC0_LLSPModeStatusFlags = 5U,
kPMC0_VLLSPModeStatusFlags = 6U }
```

*PMC 0 power mode status flags.*

## Driver version

- #define **FSL\_PMC0\_DRIVER\_VERSION** (MAKE\_VERSION(2, 1, 0))  
*PMC 0 driver version.*

## Power Management Controller Control APIs

- static void **PMC0\_ConfigureHsrunMode** (const **pmc0\_hsun\_mode\_config\_t** \*config)  
*Configure the HSRUN power mode.*
- static void **PMC0\_ConfigureRunMode** (const **pmc0\_run\_mode\_config\_t** \*config)  
*Configure the RUN power mode.*
- static void **PMC0\_ConfigureVlprMode** (const **pmc0\_vlpr\_mode\_config\_t** \*config)  
*Configure the VLPR power mode.*
- static void **PMC0\_ConfigureStopMode** (const **pmc0\_stop\_mode\_config\_t** \*config)  
*Configure the STOP power mode.*
- static void **PMC0\_ConfigureVlpsMode** (const **pmc0\_vlps\_mode\_config\_t** \*config)  
*Configure the VLPS power mode.*
- static void **PMC0\_ConfigureLlsMode** (const **pmc0\_lls\_mode\_config\_t** \*config)  
*Configure the LLS power mode.*
- static void **PMC0\_ConfigureVllsMode** (const **pmc0\_vlls\_mode\_config\_t** \*config)  
*Configure the VLLS power mode.*
- static uint32\_t **PMC0\_GetPMC0PowerModeStatusFlags** (void)  
*Get current power mode of PMC 0.*
- static bool **PMC0\_GetPMC0PowerTransitionStatus** (void)  
*Get the status of PMC 0 power mode transition.*
- static uint32\_t **PMC0\_GetPMC1PowerModeStatusFlags** (void)  
*Get current power mode of PMC 1.*
- static bool **PMC0\_GetPMC1PowerTransitionStatus** (void)  
*Get the status of PMC 1 power mode transition.*
- static uint32\_t **PMC0\_GetStatusFlags** (void)  
*Gets PMC 0 status flags.*
- static void **PMC0\_EnableLowVoltDetectInterrupt** (void)  
*Enables the 1.2V Low-Voltage Detector interrupt.*
- static void **PMC0\_DisableLowVoltDetectInterrupt** (void)  
*Disables the 1.2V Low-Voltage Detector interrupt.*
- static void **PMC0\_ClearLowVoltDetectFlag** (void)  
*Clears the 1.2V Low-Voltage Detector flag.*
- static void **PMC0\_EnableHighVoltDetectInterrupt** (void)  
*Enables the 1.8V High-Voltage Detector interrupt.*
- static void **PMC0\_DisableHighVoltDetectInterrupt** (void)  
*Disables the 1.8V High-Voltage Detector interrupt.*

- static void **PMC0\_ClearHighVoltDetectFlag** (void)  
*Clears the 1.8V High-Voltage Detector flag.*
- static void **PMC0\_EnableLowVoltDetectReset** (bool enable)  
*Enables the 1.2V Low-Voltage Detector reset.*
- static void **PMC0\_EnableHighVoltDetectReset** (bool enable)  
*Enables the 1.8V High-Voltage Detector reset.*
- static void **PMC0\_ClearPadsIsolation** (void)  
*Releases/clears the isolation in the PADS.*
- static void **PMC0\_PowerOnPmc1** (void)  
*Powers on PMC 1.*
- static void **PMC0\_EnableWaitLdoOkSignal** (bool enable)  
*Enables to wait LDO OK signal.*
- static void **PMC0\_EnablePmc1LdoRegulator** (bool enable)  
*Enables PMC 1 LDO Regulator.*
- static void **PMC0\_EnablePmc1RBBMode** (bool enable)  
*Enable the PMC 1 RBB(reverse back bias) mode.*
- static void **PMC0\_SetBiasConfig** (const **pmc0\_bias\_config\_t** \*config)  
*Configure the PMC 0 bias voltage level and enable/disable pull-down.*
- static void **PMC0\_ConfigureSramBankPowerDown** (uint32\_t bankMask)  
*Configures PMC 0 SRAM bank power down.*
- static void **PMC0\_ConfigureSramBankPowerDownStopMode** (uint32\_t bankMask)  
*Configures PMC 0 SRAM bank power down in stop modes.*
- static void **PMC0\_ConfigureSramBankPowerDownStandbyMode** (uint32\_t bankMask)  
*Configures PMC 0 SRAM bank power down in Standby Mode.*
- static void **PMC0\_EnableTemperatureSensor** (bool enable)  
*Enable/disable internal temperature sensor.*
- static void **PMC0\_SetTemperatureSensorMode** (uint8\_t mode)  
*Set temperature sensor mode.*

### 30.3 Data Structure Documentation

#### 30.3.1 struct pmc0\_hsrn\_mode\_config\_t

##### Data Fields

- uint32\_t \_\_pad0\_\_: 16  
*Reserved.*
- uint32\_t coreRegulatorVoltLevel: 6  
*Core Regulator Voltage Level.*
- uint32\_t \_\_pad1\_\_: 2  
*Reserved.*
- uint32\_t enableForwardBias: 1  
*Enable forward bias.*
- uint32\_t \_\_pad2\_\_: 7  
*Reserved.*

##### Field Documentation

(1) uint32\_t pmc0\_hsrn\_mode\_config\_t::\_\_pad0\_\_

- (2) `uint32_t pmc0_hsrn_mode_config_t::coreRegulatorVoltLevel`
- (3) `uint32_t pmc0_hsrn_mode_config_t::__pad1__`
- (4) `uint32_t pmc0_hsrn_mode_config_t::enableForwardBias`
- (5) `uint32_t pmc0_hsrn_mode_config_t::__pad2__`

### 30.3.2 struct pmc0\_run\_mode\_config\_t

#### Data Fields

- `uint32_t __pad0__`: 16  
*Reserved.*
- `uint32_t coreRegulatorVoltLevel`: 6  
*Core Regulator Voltage Level.*
- `uint32_t __pad1__`: 10  
*Reserved.*

#### Field Documentation

- (1) `uint32_t pmc0_run_mode_config_t::__pad0__`
- (2) `uint32_t pmc0_run_mode_config_t::coreRegulatorVoltLevel`
- (3) `uint32_t pmc0_run_mode_config_t::__pad1__`

### 30.3.3 struct pmc0\_vlpr\_mode\_config\_t

#### Data Fields

- `uint32_t arrayRegulatorSelect`: 1  
*Array Regulator Select.*
- `uint32_t __pad0__`: 1  
*Reserved.*
- `uint32_t coreRegulatorSelect`: 1  
*Core Regulator Select.*
- `uint32_t __pad1__`: 1  
*Reserved.*
- `uint32_t lvdMonitorSelect`: 1  
*1.2V LVD Monitor Select.*
- `uint32_t hvdMonitorSelect`: 1  
*1.2V HVD Monitor Select.*
- `uint32_t __pad2__`: 1  
*Reserved.*
- `uint32_t enableForceHpBandgap`: 1  
*Enable force HP band-gap.*
- `uint32_t __pad3__`: 8  
*Reserved.*

- `uint32_t coreRegulatorVoltLevel`: 6  
*Core Regulator Voltage Level.*
- `uint32_t __pad4__`: 6  
*Reserved.*
- `uint32_t enableReverseBackBias`: 1  
*Enable reverse back bias.*
- `uint32_t __pad5__`: 3  
*Reserved.*

**Field Documentation**

- (1) `uint32_t pmc0_vlpr_mode_config_t::arrayRegulatorSelect`  
`pmc0_array_regulator_select_t`
- (2) `uint32_t pmc0_vlpr_mode_config_t::__pad0__`
- (3) `uint32_t pmc0_vlpr_mode_config_t::coreRegulatorSelect`  
`pmc0_core_regulator_select_t`
- (4) `uint32_t pmc0_vlpr_mode_config_t::__pad1__`
- (5) `uint32_t pmc0_vlpr_mode_config_t::lvdMonitorSelect`  
`pmc0_low_volt_detect_monitor_select_t`
- (6) `uint32_t pmc0_vlpr_mode_config_t::hvdMonitorSelect`  
`pmc0_high_volt_detect_monitor_select_t`
- (7) `uint32_t pmc0_vlpr_mode_config_t::__pad2__`
- (8) `uint32_t pmc0_vlpr_mode_config_t::enableForceHpBandgap`
- (9) `uint32_t pmc0_vlpr_mode_config_t::__pad3__`
- (10) `uint32_t pmc0_vlpr_mode_config_t::coreRegulatorVoltLevel`
- (11) `uint32_t pmc0_vlpr_mode_config_t::__pad4__`
- (12) `uint32_t pmc0_vlpr_mode_config_t::enableReverseBackBias`
- (13) `uint32_t pmc0_vlpr_mode_config_t::__pad5__`

**30.3.4 struct pmc0\_stop\_mode\_config\_t****Data Fields**

- `uint32_t __pad0__`: 16

- `uint32_t coreRegulatorVoltLevel`: 6  
*Core Regulator Voltage Level.*
- `uint32_t __pad1__`: 10  
*Reserved.*

## Field Documentation

- (1) `uint32_t pmc0_stop_mode_config_t::__pad0__`
- (2) `uint32_t pmc0_stop_mode_config_t::coreRegulatorVoltLevel`
- (3) `uint32_t pmc0_stop_mode_config_t::__pad1__`

### 30.3.5 struct pmc0\_vlps\_mode\_config\_t

## Data Fields

- `uint32_t arrayRegulatorSelect`: 1  
*Array Regulator Select.*
- `uint32_t __pad0__`: 1  
*Reserved.*
- `uint32_t coreRegulatorSelect`: 1  
*Core Regulator Select.*
- `uint32_t __pad1__`: 1  
*Reserved.*
- `uint32_t lvdMonitorSelect`: 1  
*1.2V LVD Monitor Select.*
- `uint32_t hvdMonitorSelect`: 1  
*1.2V HVD Monitor Select.*
- `uint32_t __pad2__`: 1  
*Reserved.*
- `uint32_t enableForceHpBandgap`: 1  
*Enable force HP band-gap.*
- `uint32_t __pad3__`: 8  
*Reserved.*
- `uint32_t coreRegulatorVoltLevel`: 6  
*Core Regulator Voltage Level.*
- `uint32_t __pad4__`: 6  
*Reserved.*
- `uint32_t enableReverseBackBias`: 1  
*Enable reverse back bias.*
- `uint32_t __pad5__`: 3  
*Reserved.*

## Field Documentation

- (1) `uint32_t pmc0_vlps_mode_config_t::arrayRegulatorSelect`  
`pmc0_array_regulator_select_t`

```

(2) uint32_t pmc0_vlps_mode_config_t::__pad0__
(3) uint32_t pmc0_vlps_mode_config_t::coreRegulatorSelect
pmc0_core_regulator_select_t

(4) uint32_t pmc0_vlps_mode_config_t::__pad1__
(5) uint32_t pmc0_vlps_mode_config_t::lvdMonitorSelect
pmc0_low_volt_detect_monitor_select_t

(6) uint32_t pmc0_vlps_mode_config_t::hvdMonitorSelect
pmc0_high_volt_detect_monitor_select_t

(7) uint32_t pmc0_vlps_mode_config_t::__pad2__
(8) uint32_t pmc0_vlps_mode_config_t::enableForceHpBandgap
(9) uint32_t pmc0_vlps_mode_config_t::__pad3__
(10) uint32_t pmc0_vlps_mode_config_t::coreRegulatorVoltLevel
(11) uint32_t pmc0_vlps_mode_config_t::__pad4__
(12) uint32_t pmc0_vlps_mode_config_t::enableReverseBackBias
(13) uint32_t pmc0_vlps_mode_config_t::__pad5__

```

### 30.3.6 struct pmc0\_lls\_mode\_config\_t

#### Data Fields

- uint32\_t arrayRegulatorSelect: 1  
*Array Regulator Select.*
- uint32\_t \_\_pad0\_\_: 1  
*Reserved.*
- uint32\_t coreRegulatorSelect: 1  
*Core Regulator Select.*
- uint32\_t \_\_pad1\_\_: 1  
*Reserved.*
- uint32\_t lvdMonitorSelect: 1  
*1.2V LVD Monitor Select.*
- uint32\_t hvdMonitorSelect: 1  
*1.2V HVD Monitor Select.*
- uint32\_t \_\_pad2\_\_: 1  
*Reserved.*
- uint32\_t enableForceHpBandgap: 1  
*Enable force HP band-gap.*

- `uint32_t __pad3__`: 8  
*Reserved.*
- `uint32_t coreRegulatorVoltLevel`: 6  
*Core Regulator Voltage Level.*
- `uint32_t __pad4__`: 6  
*Reserved.*
- `uint32_t enableReverseBackBias`: 1  
*Enable reverse back bias.*
- `uint32_t __pad5__`: 3  
*Reserved.*

**Field Documentation**

- (1) `uint32_t pmc0_lls_mode_config_t::arrayRegulatorSelect`  
`pmc0_array_regulator_select_t`
- (2) `uint32_t pmc0_lls_mode_config_t::__pad0__`
- (3) `uint32_t pmc0_lls_mode_config_t::coreRegulatorSelect`  
`pmc0_core_regulator_select_t`
- (4) `uint32_t pmc0_lls_mode_config_t::__pad1__`
- (5) `uint32_t pmc0_lls_mode_config_t::lvdMonitorSelect`  
`pmc0_low_volt_detect_monitor_select_t`
- (6) `uint32_t pmc0_lls_mode_config_t::hvdMonitorSelect`  
`pmc0_high_volt_detect_monitor_select_t`
- (7) `uint32_t pmc0_lls_mode_config_t::__pad2__`
- (8) `uint32_t pmc0_lls_mode_config_t::enableForceHpBandgap`
- (9) `uint32_t pmc0_lls_mode_config_t::__pad3__`
- (10) `uint32_t pmc0_lls_mode_config_t::coreRegulatorVoltLevel`
- (11) `uint32_t pmc0_lls_mode_config_t::__pad4__`
- (12) `uint32_t pmc0_lls_mode_config_t::enableReverseBackBias`
- (13) `uint32_t pmc0_lls_mode_config_t::__pad5__`

### 30.3.7 struct pmc0\_vlls\_mode\_config\_t

#### Data Fields

- `uint32_t arrayRegulatorSelect: 2`  
*Array Regulator Select.*
- `uint32_t __pad0__: 2`  
*Reserved.*
- `uint32_t lvdMonitorSelect: 1`  
*1.2V LVD Monitor Select.*
- `uint32_t hvdMonitorSelect: 1`  
*1.2V HVD Monitor Select.*
- `uint32_t __pad1__: 1`  
*Reserved.*
- `uint32_t enableForceHpBandgap: 1`  
*Enable force HP band-gap.*
- `uint32_t __pad2__: 24`  
*Reserved.*

#### Field Documentation

(1) `uint32_t pmc0_vlls_mode_config_t::arrayRegulatorSelect`

`pmc0_vlls_array_regulator_select_t`

(2) `uint32_t pmc0_vlls_mode_config_t::__pad0__`

(3) `uint32_t pmc0_vlls_mode_config_t::lvdMonitorSelect`

`pmc0_low_volt_detect_monitor_select_t`

(4) `uint32_t pmc0_vlls_mode_config_t::hvdMonitorSelect`

`pmc0_high_volt_detect_monitor_select_t`

(5) `uint32_t pmc0_vlls_mode_config_t::__pad1__`

(6) `uint32_t pmc0_vlls_mode_config_t::enableForceHpBandgap`

(7) `uint32_t pmc0_vlls_mode_config_t::__pad2__`

### 30.3.8 struct pmc0\_bias\_config\_t

#### Data Fields

- `uint32_t __pad0__: 4`  
*Reserved.*
- `uint32_t RBBPWellVoltageLevelSelect: 4`  
*Select PMC0 RBB P-Well voltage level.*

- `uint32_t __pad1__`: 3  
*Reserved.*
- `uint32_t DisableRBBPullDown`: 1  
*Disable RBB pull-down.*
- `uint32_t FBBNWellVoltageLevelSelect`: 4  
*Select PMC0 FBB N-Well voltage level.*
- `uint32_t __pad2__`: 4  
*Reserved.*
- `uint32_t FBBPWellVoltageLevelSelect`: 4  
*Select PMC0 FBB P-Well voltage level.*
- `uint32_t __pad3__`: 4  
*Reserved.*

**Field Documentation**

- (1) `uint32_t pmc0_bias_config_t::__pad0__`
- (2) `uint32_t pmc0_bias_config_t::RBBPWellVoltageLevelSelect`  
`pmc0_rbb_p_well_voltage_level_select_t`
- (3) `uint32_t pmc0_bias_config_t::__pad1__`
- (4) `uint32_t pmc0_bias_config_t::DisableRBBPullDown`  
'1' means to disable pull-down. '0' means to enable pull-down.
- (5) `uint32_t pmc0_bias_config_t::FBBNWellVoltageLevelSelect`  
`pmc0_fbb_n_well_voltage_level_select_t`
- (6) `uint32_t pmc0_bias_config_t::__pad2__`
- (7) `uint32_t pmc0_bias_config_t::FBBPWellVoltageLevelSelect`  
`pmc0_fbb_p_well_voltage_level_select_t`
- (8) `uint32_t pmc0_bias_config_t::__pad3__`

**30.4 Enumeration Type Documentation****30.4.1 enum pmc0\_high\_volt\_detect\_monitor\_select\_t**

Enumerator

`kPMC0_HighVoltDetectLowPowerMonitor` LP monitor is selected.  
`kPMC0_HighVoltDetectHighPowerMonitor` HP monitor is selected.

### 30.4.2 enum pmc0\_low\_volt\_detect\_monitor\_select\_t

Enumerator

*kPMC0\_LowVoltDetectLowPowerMonitor* LP monitor is selected.

*kPMC0\_LowVoltDetectHighPowerMonitor* HP monitor is selected.

### 30.4.3 enum pmc0\_core\_regulator\_select\_t

Enumerator

*kPMC0\_CoreLowPowerRegulator* Core LP regulator is selected.

*kPMC0\_CoreHighPowerRegulator* Core HP regulator is selected.

### 30.4.4 enum pmc0\_array\_regulator\_select\_t

Enumerator

*kPMC0\_ArrayLowPowerRegulator* Array LP regulator is selected.

*kPMC0\_ArrayHighPowerRegulator* Array HP regulator is selected.

### 30.4.5 enum pmc0\_vlls\_array\_regulator\_select\_t

Enumerator

*kPMC0\_VllsArrayRegulatorOff* Array regulator is selected OFF. This is selectable only for VLLS mode.

*kPMC0\_VllsArrayLowPowerRegulator* Array LP regulator is selected.

*kPMC0\_VllsArrayHighPowerRegulator* Array HP regulator is selected.

### 30.4.6 enum pmc0\_fbb\_p\_well\_voltage\_level\_select\_t

Enumerator

*kPMC0\_FbbPWellNoBiasCondition* No BIAS condition is selected.

*kPMC0\_FbbPWellVoltageLevelAt50Mv* Voltage level at 50mV is selected.

*kPMC0\_FbbPWellVoltageLevelAt150Mv* Voltage level at 150mV is selected.

*kPMC0\_FbbPWellVoltageLevelAt100Mv* Voltage level at 100mV is selected.

*kPMC0\_FbbPWellVoltageLevelAt350Mv* Voltage level at 350mV is selected.

*kPMC0\_FbbPWellVoltageLevelAt300Mv* Voltage level at 300mV is selected.

*kPMC0\_FbbPWellVoltageLevelAt200Mv* Voltage level at 200mV is selected.

*kPMC0\_FbbPWellVoltageLevelAt250Mv* Voltage level at 250mV is selected.

**30.4.7 enum pmc0\_fbb\_n\_well\_voltage\_level\_select\_t**

Enumerator

*kPMC0\_FbbNWellNoBiasCondition* No BIAS condition is selected.*kPMC0\_FbbNWellVoltageLevelAtMinus50Mv* Voltage level at -50mV is selected.*kPMC0\_FbbNWellVoltageLevelAtMinus150Mv* Voltage level at -150mV is selected.*kPMC0\_FbbNWellVoltageLevelAtMinus100Mv* Voltage level at -100mV is selected.*kPMC0\_FbbNWellVoltageLevelAtMinus350Mv* Voltage level at -350mV is selected.*kPMC0\_FbbNWellVoltageLevelAtMinus300Mv* Voltage level at -300mV is selected.*kPMC0\_FbbNWellVoltageLevelAtMinus200Mv* Voltage level at -200mV is selected.*kPMC0\_FbbNWellVoltageLevelAtMinus250Mv* Voltage level at -250mV is selected.**30.4.8 enum pmc0\_rbb\_p\_well\_voltage\_level\_select\_t**

Enumerator

*kPMC0\_RBBPWellVoltageLevelAtMinus0\_5V* Voltage level at -0.5V is selected.*kPMC0\_RBBPWellVoltageLevelAtMinus0\_6V* Voltage level at -0.6V is selected.*kPMC0\_RBBPWellVoltageLevelAtMinus0\_7V* Voltage level at -0.7V is selected.*kPMC0\_RBBPWellVoltageLevelAtMinus0\_8V* Voltage level at -0.8V is selected.*kPMC0\_RBBPWellVoltageLevelAtMinus0\_9V* Voltage level at -0.9V is selected.*kPMC0\_RBBPWellVoltageLevelAtMinus1\_0V* Voltage level at -1.0V is selected.*kPMC0\_RBBPWellVoltageLevelAtMinus1\_1V* Voltage level at -1.1V is selected.*kPMC0\_RBBPWellVoltageLevelAtMinus1\_2V* Voltage level at -1.2V is selected.*kPMC0\_RBBPWellVoltageLevelAtMinus1\_3V* Voltage level at -1.3V is selected.**30.4.9 enum pmc0\_rbb\_n\_well\_voltage\_level\_select\_t**

Enumerator

*kPMC0\_RBBNWellVoltageLevelAt0\_5V* Voltage level at 0.5V is selected.*kPMC0\_RBBNWellVoltageLevelAt0\_6V* Voltage level at 0.6V is selected.*kPMC0\_RBBNWellVoltageLevelAt0\_7V* Voltage level at 0.7V is selected.*kPMC0\_RBBNWellVoltageLevelAt0\_8V* Voltage level at 0.8V is selected.*kPMC0\_RBBNWellVoltageLevelAt0\_9V* Voltage level at 0.9V is selected.*kPMC0\_RBBNWellVoltageLevelAt1\_0V* Voltage level at 1.0V is selected.*kPMC0\_RBBNWellVoltageLevelAt1\_1V* Voltage level at 1.1V is selected.*kPMC0\_RBBNWellVoltageLevelAt1\_2V* Voltage level at 1.2V is selected.*kPMC0\_RBBNWellVoltageLevelAt1\_3V* Voltage level at 1.3V is selected.

### 30.4.10 enum \_pmc0\_status\_flags

Enumerator

***kPMC0\_LowVoltDetectEventFlag*** 1.2V Low-Voltage Detector Flag, sets when low-voltage event was detected.

***kPMC0\_LowVoltDetectValueFlag*** 1.2V Low-Voltage Detector Value, sets when current value of the 1.2V LVD monitor output is 1.

***kPMC0\_HighVoltDetectEventFlag*** 1.8V High-Voltage Detector Flag, sets when high-voltage event was detected.

***kPMC0\_HighVoltDetectValueFlag*** 1.8V High-Voltage Detector Value, sets when current value of the 1.8V HVD monitor output is 1.

***kPMC0\_CoreRegulatorVoltLevelFlag*** Core Regulator Voltage Level Flag, sets when core regulator voltage level is changing (not stable).

***kPMC0\_SramFlag*** SRAM Flag, sets when a change mode request is being processed in the SRAMs.

***kPMC0\_PMC1VoltageSourceFlag*** This flag indicates what is the voltage source selected to supply the PMC 1 and where the sense point of the PMC 1's LVD/HVD is placed. '0' means internal LDO supplies the PMC 1. '1' means external PMIC supplies the PMC 1.

### 30.4.11 enum \_pmc0\_power\_mode\_status\_flags

Enumerator

***kPMC0\_HSRUNModeStatusFlags*** The PMC 0 is in HSRUN mode.

***kPMC0\_RUNModeStatusFlags*** The PMC 0 is in RUN mode.

***kPMC0\_STOPModeStatusFlags*** The PMC 0 is in STOP mode.

***kPMC0\_VLPRModeStatusFlags*** The PMC 0 is in VLPR mode.

***kPMC0\_VLPSModeStatusFlags*** The PMC 0 is in VLPS mode.

***kPMC0\_LLSSModeStatusFlags*** The PMC 0 is in LLSS mode.

***kPMC0\_VLLSSModeStatusFlags*** The PMC 0 is in VLLS mode.

## 30.5 Function Documentation

### 30.5.1 static void PMC0\_ConfigureHsrunMode ( const pmc0\_hsruntime\_config\_t \* config ) [inline], [static]

This function configures the HSRUN power mode, including the core regulator voltage Level setting, enable forward bias or not.

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>config</i> | Low-Voltage detect configuration structure. |
|---------------|---------------------------------------------|

### 30.5.2 static void PMC0\_ConfigureRunMode ( const pmc0\_run\_mode\_config\_t \* *config* ) [inline], [static]

This function configures the RUN power mode, including the core regulator voltage Level setting.

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>config</i> | Low-Voltage detect configuration structure. |
|---------------|---------------------------------------------|

### 30.5.3 static void PMC0\_ConfigureVlprMode ( const pmc0\_vlpr\_mode\_config\_t \* *config* ) [inline], [static]

This function configures the VLPR power mode, including the core regulator voltage Level setting, enable reverse back bias or not, turn on force HP band-gap or not, select of HVD/LVD monitor and select of core/array regulator.

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>config</i> | Low-Voltage detect configuration structure. |
|---------------|---------------------------------------------|

### 30.5.4 static void PMC0\_ConfigureStopMode ( const pmc0\_stop\_mode\_config\_t \* *config* ) [inline], [static]

This function configures the STOP power mode, including the core regulator voltage Level setting.

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>config</i> | Low-Voltage detect configuration structure. |
|---------------|---------------------------------------------|

### 30.5.5 static void PMC0\_ConfigureVlpsMode ( const pmc0\_vlps\_mode\_config\_t \* *config* ) [inline], [static]

This function configures the VLPS power mode, including the core regulator voltage Level setting, enable reverse back bias or not, turn on force HP band-gap or not, select of HVD/LVD monitor and select of core/array regulator.

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>config</i> | Low-Voltage detect configuration structure. |
|---------------|---------------------------------------------|

### 30.5.6 static void PMC0\_ConfigureLlsMode ( const pmc0\_lls\_mode\_config\_t \* *config* ) [inline], [static]

This function configures the LLS power mode, including the core regulator voltage Level setting, enable reverse back bias or not, turn on force HP band-gap or not, select of HVD/LVD monitor and select of core/array regulator.

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>config</i> | Low-Voltage detect configuration structure. |
|---------------|---------------------------------------------|

### 30.5.7 static void PMC0\_ConfigureVllsMode ( const pmc0\_vlls\_mode\_config\_t \* *config* ) [inline], [static]

This function configures the VLLS power mode, including turn on force HP band-gap or not, select of HVD/LVD monitor and select of core/array regulator.

The select of array regulator is different from the other mode configurations. PMC 0 VLLS config has three array regulator select options where the others have only the latter two, see [pmc0\\_vlls\\_array\\_regulator\\_select\\_t](#). Three array regulator select options in PMC 0 VLLS config are shown below:

- Regulator is off (diffrentiator)
- LP Regulator is on
- HP Regulator is on

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>config</i> | Low-Voltage detect configuration structure. |
|---------------|---------------------------------------------|

### 30.5.8 static uint32\_t PMC0\_GetPMC0PowerModeStatusFlags ( void ) [inline], [static]

```
* if (kPMCO_HSRUNModeStatusFlags ==
* PMCO_GetPMC0PowerModeStatusFlags(void))
* {
* ...
* }
*
```

Returns

PMC 0 current power mode status flags in the `_pmc0_power_mode_status_flags`.

### **30.5.9 static bool PMC0\_GetPMC0PowerTransitionStatus ( void ) [inline], [static]**

Returns

If return 'true', which means PMC 0 is in a power mode transition. If return 'false', which means PMC 0 is not in a power mode transition.

### **30.5.10 static uint32\_t PMC0\_GetPMC1PowerModeStatusFlags ( void ) [inline], [static]**

```
* if(kPMC0_HSRUNModeStatusFlags ==
* PMC0_GetPMC1PowerModeStatusFlags(void))
* {
* ...
* }
```

Returns

PMC 1 current power mode status flags in the `_pmc0_power_mode_status_flags`.

### **30.5.11 static bool PMC0\_GetPMC1PowerTransitionStatus ( void ) [inline], [static]**

Returns

If return 'true', which means PMC 1 is in a power mode transition. If return 'false', which means PMC 1 is not in a power mode transition.

### **30.5.12 static uint32\_t PMC0\_GetStatusFlags ( void ) [inline], [static]**

This function gets all PMC 0 status flags. The flags are returned as the logical OR value of the enumerators `_pmc0_status_flags`. To check for a specific status, compare the return value with enumerators in the `_pmc0_status_flags`. For example, to check whether core regulator voltage level is changing:

```
* if (kPMC0_CoreRegulatorVoltLevelFlag &
* PMC0_GetStatusFlags(void))
* {
* ...
* }
*
```

Returns

PMC 0 status flags which are ORed by the enumerators in the \_pmc0\_status\_flags.

### **30.5.13 static void PMC0\_EnableLowVoltDetectInterrupt ( void ) [inline], [static]**

This function enables the 1.2V Low-Voltage Detector interrupt.

### **30.5.14 static void PMC0\_DisableLowVoltDetectInterrupt ( void ) [inline], [static]**

This function disables the 1.2V Low-Voltage Detector interrupt.

### **30.5.15 static void PMC0\_ClearLowVoltDetectFlag ( void ) [inline], [static]**

This function enables the 1.2V Low-Voltage Detector flag.

### **30.5.16 static void PMC0\_EnableHighVoltDetectInterrupt ( void ) [inline], [static]**

This function enables the 1.8V High-Voltage Detector interrupt.

### **30.5.17 static void PMC0\_DisableHighVoltDetectInterrupt ( void ) [inline], [static]**

This function disables the 1.8V High-Voltage Detector interrupt.

### **30.5.18 static void PMC0\_ClearHighVoltDetectFlag ( void ) [inline], [static]**

This function enables the 1.8V High-Voltage Detector flag.

**30.5.19 static void PMC0\_EnableLowVoltDetectReset( bool enable ) [inline],  
[static]**

This function enables 1.2V Low-Voltage Detector reset.

Parameters

|               |                                                                                                 |
|---------------|-------------------------------------------------------------------------------------------------|
| <i>enable</i> | Switcher of 1.2V Low-Voltage Detector reset feature. "true" means to enable, "false" means not. |
|---------------|-------------------------------------------------------------------------------------------------|

### 30.5.20 static void PMC0\_EnableHighVoltDetectReset ( bool *enable* ) [inline], [static]

This function enables 1.8V High-Voltage Detector reset.

Parameters

|               |                                                                                                  |
|---------------|--------------------------------------------------------------------------------------------------|
| <i>enable</i> | Switcher of 1.8V High-Voltage Detector reset feature. "true" means to enable, "false" means not. |
|---------------|--------------------------------------------------------------------------------------------------|

### 30.5.21 static void PMC0\_ClearPadsIsolation ( void ) [inline], [static]

This function releases/clears the isolation in the PADS.

The isolation in the pads only will be asserted during LLS/VLLS. On LLS exit, the isolation will release automatically. ISOACK must be set after a VLLS to RUN mode transition has completed.

### 30.5.22 static void PMC0\_PowerOnPmc1 ( void ) [inline], [static]

This function powers on PMC 1.

When this bit field is asserted the PMC 1 is powered on. This bit would take action only once. This bit will be rearmed after a POR event only. NOTE: USB PHY-related interrupt (NVIC/GIC) and wake-up channels (AWIC/WKPU) must be disabled before turning PMC1 on.

### 30.5.23 static void PMC0\_EnableWaitLdoOkSignal ( bool *enable* ) [inline], [static]

This function enables to wait LDO OK signal.

Parameters

|               |                                                                                    |
|---------------|------------------------------------------------------------------------------------|
| <i>enable</i> | Switcher of wait LDO OK signal feature. "true" means to enable, "false" means not. |
|---------------|------------------------------------------------------------------------------------|

### 30.5.24 static void PMC0\_EnablePmc1LdoRegulator ( bool *enable* ) [inline], [static]

This function enables PMC 1 LDO Regulator.

Parameters

|               |                                                                             |
|---------------|-----------------------------------------------------------------------------|
| <i>enable</i> | Switcher of PMC 1 LDO Regulator. "true" means to enable, "false" means not. |
|---------------|-----------------------------------------------------------------------------|

### 30.5.25 static void PMC0\_EnablePmc1RBBMode ( bool *enable* ) [inline], [static]

This function enables PMC1 RBB mode. Since this circuit when enabled has current consumption. It is recommended to use it just in high temperatures when the leakage reduction is much higher than the current consumption.

Parameters

|               |                                                                           |
|---------------|---------------------------------------------------------------------------|
| <i>enable</i> | Switcher of PMC1 RBB mode. "true" means to enable, "false" means disable. |
|---------------|---------------------------------------------------------------------------|

### 30.5.26 static void PMC0\_SetBiasConfig ( const pmc0\_bias\_config\_t \* *config* ) [inline], [static]

This function change the RBB&FBB voltage level and RBB pull-down.

Parameters

|               |                                     |
|---------------|-------------------------------------|
| <i>config</i> | PMC 0 bias configuration structure. |
|---------------|-------------------------------------|

### 30.5.27 static void PMC0\_ConfigureSramBankPowerDown ( uint32\_t *bankMask* ) [inline], [static]

This function configures PMC 0 SRAM bank power down.

The bit i controls the power mode of the PMC 0 SRAM bank i. PMC0\_SRAM\_PD[i] = 1'b0 - PMC 0 SRAM bank i is not affected. PMC0\_SRAM\_PD[i] = 1'b1 - PMC 0 SRAM bank i is in ASD or ARRAY\_SHUTDOWN during all modes, except VLLS. During VLLS is in POWER\_DOWN mode.

## Example

```
* // Enable band 0 and 1 in ASD or ARRAY_SHUTDOWN during all modes except VLLS
* PMC0_ConfigureSramBankPowerDown(0x3U);
*
```

## Parameters

|                 |                                                                      |
|-----------------|----------------------------------------------------------------------|
| <i>bankMask</i> | The bands to enable. Logical OR of all bits of band index to enable. |
|-----------------|----------------------------------------------------------------------|

### 30.5.28 static void PMC0\_ConfigureSramBankPowerDownStopMode ( uint32\_t bankMask ) [inline], [static]

This function configures PMC 0 SRAM bank power down in stop modes.

The bit i controls the PMC 0 SRAM bank i. PMC0\_SRAM\_PDS[i] = 1'b0 - PMC 0 SRAM bank i is not affected. PMC0\_SRAM\_PDS[i] = 1'b1 - PMC 0 SRAM bank i is in ASD or ARRAY\_SHUTDOWN mode during STOP, VLPS and LLS modes. During VLLS is in POWER\_DOWN mode.

## Example

```
* // Enable band 0 and 1 in ASD or ARRAY_SHUTDOWN during STOP, VLPS and LLS modes
* PMC0_ConfigureSramBankPowerDownStopMode(0x3U);
*
```

## Parameters

|                 |                                                                      |
|-----------------|----------------------------------------------------------------------|
| <i>bankMask</i> | The bands to enable. Logical OR of all bits of band index to enable. |
|-----------------|----------------------------------------------------------------------|

### 30.5.29 static void PMC0\_ConfigureSramBankPowerDownStandbyMode ( uint32\_t bankMask ) [inline], [static]

This function configures PMC 0 SRAM bank power down in Standby Mode.

The bit i controls the PMC 0 SRAM bank i. PMC0\_SRAM\_STDY[i] = 1'b0 - PMC 0 SRAM bank i is not affected. PMC0\_SRAM\_STDY[i] = 1'b1 - PMC 0 SRAM bank i is in STANDBY mode during all modes (except VLLS and LLS).

## Example

```
* // Enable band 0 and 1 in STANDBY mode except VLLS and LLS
* PMC0_ConfigureSramBankPowerDownStandbyMode(0x3U);
*
```

Parameters

|                 |                                                                      |
|-----------------|----------------------------------------------------------------------|
| <i>bankMask</i> | The bands to enable. Logical OR of all bits of band index to enable. |
|-----------------|----------------------------------------------------------------------|

### 30.5.30 static void PMC0\_EnableTemperatureSensor( bool *enable* ) [inline], [static]

Parameters

|               |                                                                                                                                                                                                                   |
|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <i>enable</i> | Used to enable/disable internal temperature sensor. <ul style="list-style-type: none"><li>• <b>true</b> Enable internal temperature sensor.</li><li>• <b>false</b> Disable internal temperature sensor.</li></ul> |
|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

### 30.5.31 static void PMC0\_SetTemperatureSensorMode( uint8\_t *mode* ) [inline], [static]

Parameters

|             |                                     |
|-------------|-------------------------------------|
| <i>mode</i> | The temperature sensor mode to set. |
|-------------|-------------------------------------|

# Chapter 31

## PORT: Port Control and Interrupts

### 31.1 Overview

The MCUXpresso SDK provides a driver for the Port Control and Interrupts (PORT) module of MCUXpresso SDK devices.

### Enumerations

- enum `port_interrupt_t` {  
    `kPORT_InterruptOrDMADisabled` = 0x0U,  
    `kPORT_DMARisingEdge` = 0x1U,  
    `kPORT_DMAFallingEdge` = 0x2U,  
    `kPORT_DMAEitherEdge` = 0x3U,  
    `kPORT_FlagRisingEdge` = 0x05U,  
    `kPORT_FlagFallingEdge` = 0x06U,  
    `kPORT_FlagEitherEdge` = 0x07U,  
    `kPORT_InterruptLogicZero` = 0x8U,  
    `kPORT_InterruptRisingEdge` = 0x9U,  
    `kPORT_InterruptFallingEdge` = 0xAU,  
    `kPORT_InterruptEitherEdge` = 0xBU,  
    `kPORT_InterruptLogicOne` = 0xCU,  
    `kPORT_ActiveHighTriggerOutputEnable` = 0xDU,  
    `kPORT_ActiveLowTriggerOutputEnable` = 0xEU }  
    *Configures the interrupt generation condition.*

### Driver version

- #define `FSL_PORT_DRIVER_VERSION` (`MAKE_VERSION(2, 3, 0)`)  
*PORT driver version.*

### 31.2 Macro Definition Documentation

#### 31.2.1 #define `FSL_PORT_DRIVER_VERSION` (`MAKE_VERSION(2, 3, 0)`)

### 31.3 Enumeration Type Documentation

#### 31.3.1 enum `port_interrupt_t`

Enumerator

- `kPORT_InterruptOrDMADisabled` Interrupt/DMA request is disabled.
- `kPORT_DMARisingEdge` DMA request on rising edge.

***kPORT\_DMAFallingEdge*** DMA request on falling edge.

***kPORT\_DMAEitherEdge*** DMA request on either edge.

***kPORT\_FlagRisingEdge*** Flag sets on rising edge.

***kPORT\_FlagFallingEdge*** Flag sets on falling edge.

***kPORT\_FlagEitherEdge*** Flag sets on either edge.

***kPORT\_InterruptLogicZero*** Interrupt when logic zero.

***kPORT\_InterruptRisingEdge*** Interrupt on rising edge.

***kPORT\_InterruptFallingEdge*** Interrupt on falling edge.

***kPORT\_InterruptEitherEdge*** Interrupt on either edge.

***kPORT\_InterruptLogicOne*** Interrupt when logic one.

***kPORT\_ActiveHighTriggerOutputEnable*** Enable active high-trigger output.

***kPORT\_ActiveLowTriggerOutputEnable*** Enable active low-trigger output.

# Chapter 32

## QSPI: Quad Serial Peripheral Interface

### 32.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Quad Serial Peripheral Interface (QSPI) module of MCUXpresso SDK devices.

QSPI driver includes functional APIs and EDMA transactional APIs.

Functional APIs are feature/property target low level APIs. Functional APIs can be used for QSPI initialization/configuration/operation for optimization/customization purpose. Using the functional API requires the knowledge of the QSPI peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. QSPI functional operation groups provide the functional API set.

Transactional APIs are transaction target high level APIs. Transactional APIs can be used to enable the peripheral and in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are a critical requirement, see the transactional API implementation and write a custom code. All transactional APIs use the `qspi_handle_t` as the first parameter. Initialize the handle by calling the [QSPI\\_TransferTxCreateHandleEDMA\(\)](#) or [QSPI\\_TransferRxCreateHandleEDMA\(\)](#) API.

### Modules

- Quad Serial Peripheral Interface Driver

## 32.2 Quad Serial Peripheral Interface Driver

### 32.2.1 Overview

#### Data Structures

- struct `qspi_dqs_config_t`  
*DQS configure features. [More...](#)*
- struct `qspi_flash_timing_t`  
*Flash timing configuration. [More...](#)*
- struct `qspi_config_t`  
*QSPI configuration structure. [More...](#)*
- struct `qspi_flash_config_t`  
*External flash configuration items. [More...](#)*
- struct `qspi_transfer_t`  
*Transfer structure for QSPI. [More...](#)*
- struct `ip_command_config_t`  
*16-bit access reg for IPCR register [More...](#)*

#### Macros

- #define `QSPI_LUT_SEQ`(cmd0, pad0, op0, cmd1, pad1, op1)  
*Macro functions for LUT table.*
- #define `QSPI_CMD` (0x1U)  
*Macro for QSPI LUT command.*
- #define `QSPI_PAD_1` (0x0U)  
*Macro for QSPI PAD.*

#### Enumerations

- enum {
   
  `kStatus_QSPI_Idle` = MAKE\_STATUS(kStatusGroup\_QSPI, 0),
   
  `kStatus_QSPI_Busy` = MAKE\_STATUS(kStatusGroup\_QSPI, 1),
   
  `kStatus_QSPI_Error` = MAKE\_STATUS(kStatusGroup\_QSPI, 2) }
   
*Status structure of QSPI.*
- enum `qspi_read_area_t` {
   
  `kQSPI_ReadAHB` = 0x0U,
   
  `kQSPI_ReadIP` }
   
*QSPI read data area, from IP FIFO or AHB buffer.*
- enum `qspi_command_seq_t` {
   
  `kQSPI_IPSeq` = QuadSPI\_SPTRCLR\_IPPTRC\_MASK,
   
  `kQSPI_BufferSeq` = QuadSPI\_SPTRCLR\_BFPTRC\_MASK }
   
*QSPI command sequence type.*
- enum `qspi_fifo_t` {
   
  `kQSPI_TxFifo` = QuadSPI\_MCR\_CLR\_TXF\_MASK,
   
  `kQSPI_RxFifo` = QuadSPI\_MCR\_CLR\_RXF\_MASK,
   
  `kQSPI_AllFifo` = QuadSPI\_MCR\_CLR\_TXF\_MASK | QuadSPI\_MCR\_CLR\_RXF\_MASK }

- *QSPI buffer type.*
- enum `qspi_endianness_t` {
   
    `kQSPI_64BigEndian` = 0x0U,
   
    `kQSPI_32LittleEndian`,
   
    `kQSPI_32BigEndian`,
   
    `kQSPI_64LittleEndian` }
- *QSPI transfer endianess.*
- enum `_qspi_error_flags` {
   
    `kQSPI_DataLearningFail` = (int)QuadSPI\_FR\_DLPFF\_MASK,
   
    `kQSPI_TxBufferFill` = QuadSPI\_FR\_TBFF\_MASK,
   
    `kQSPI_TxBufferUnderrun` = QuadSPI\_FR\_TBUF\_MASK,
   
    `kQSPI_IllegalInstruction` = QuadSPI\_FR\_ILLINE\_MASK,
   
    `kQSPI_RxBufferOverflow` = QuadSPI\_FR\_RBOF\_MASK,
   
    `kQSPI_RxBufferDrain` = QuadSPI\_FR\_RBDF\_MASK,
   
    `kQSPI_AHBSequenceError` = QuadSPI\_FR\_ABSEF\_MASK,
   
    `kQSPI_AHBIllegalTransaction` = QuadSPI\_FR\_AITEF\_MASK,
   
    `kQSPI_AHBIllegalBurstSize` = QuadSPI\_FR\_AIBSEF\_MASK,
   
    `kQSPI_AHBBufferOverflow` = QuadSPI\_FR\_ABOF\_MASK,
   
    `kQSPI_IPCommandTriggerDuringAHBAccess` = QuadSPI\_FR\_IPAEF\_MASK,
   
    `kQSPI_IPCommandTriggerDuringIPAccess` = QuadSPI\_FR\_IPIEF\_MASK,
   
    `kQSPI_IPCommandTriggerDuringAHBGrant` = QuadSPI\_FR\_IPGEF\_MASK,
   
    `kQSPI_IPCommandTransactionFinished` = QuadSPI\_FR\_TFF\_MASK,
   
    `kQSPI_FlagAll` = (int)0x8C83F8D1U }
- *QSPI error flags.*
- enum `_qspi_flags` {

```

kQSPI_DataLearningSamplePoint = (int)QuadSPI_SR_DLPSMP_MASK,
kQSPI_TxBufferFull = QuadSPI_SR_TXFULL_MASK,
kQSPI_TxDMA = QuadSPI_SR_TXDMA_MASK,
kQSPI_TxWatermark = QuadSPI_SR_TXWA_MASK,
kQSPI_TxBufferEnoughData = QuadSPI_SR_TXEDA_MASK,
kQSPI_RxDMA = QuadSPI_SR_RXDMA_MASK,
kQSPI_RxBufferFull = QuadSPI_SR_RXFULL_MASK,
kQSPI_RxWatermark = QuadSPI_SR_RXWE_MASK,
kQSPI_AHB3BufferFull = QuadSPI_SR_AHB3FUL_MASK,
kQSPI_AHB2BufferFull = QuadSPI_SR_AHB2FUL_MASK,
kQSPI_AHB1BufferFull = QuadSPI_SR_AHB1FUL_MASK,
kQSPI_AHB0BufferFull = QuadSPI_SR_AHB0FUL_MASK,
kQSPI_AHB3BufferNotEmpty = QuadSPI_SR_AHB3NE_MASK,
kQSPI_AHB2BufferNotEmpty = QuadSPI_SR_AHB2NE_MASK,
kQSPI_AHB1BufferNotEmpty = QuadSPI_SR_AHB1NE_MASK,
kQSPI_AHB0BufferNotEmpty = QuadSPI_SR_AHB0NE_MASK,
kQSPI_AHBTransactionPending = QuadSPI_SR_AHBTRN_MASK,
kQSPI_AHBCCommandPriorityGranted = QuadSPI_SR_AHBGNT_MASK,
kQSPI_AHBAccess = QuadSPI_SR_AHB_ACC_MASK,
kQSPI_IPAccess = QuadSPI_SR_IP_ACC_MASK,
kQSPI_Busy = QuadSPI_SR_BUSY_MASK,
kQSPI_StateAll = (int)0xEF897FE7U }

```

*QSPI state bit.*

- enum `_qspi_interrupt_enable` {
 

```

kQSPI_DataLearningFailInterruptEnable,
kQSPI_TxBufferFillInterruptEnable = QuadSPI_RSER_TBFIE_MASK,
kQSPI_TxBufferUnderrunInterruptEnable = QuadSPI_RSER_TBUIE_MASK,
kQSPI_IllegalInstructionInterruptEnable,
kQSPI_RxBufferOverflowInterruptEnable = QuadSPI_RSER_RBOIE_MASK,
kQSPI_RxBufferDrainInterruptEnable = QuadSPI_RSER_RBDIE_MASK,
kQSPI_AHBSequenceErrorInterruptEnable = QuadSPI_RSER_ABSEIE_MASK,
kQSPI_AHBIlegalTransactionInterruptEnable,
kQSPI_AHBIlegalBurstSizeInterruptEnable,
kQSPI_AHBBufferOverflowInterruptEnable = QuadSPI_RSER_ABOIE_MASK,
kQSPI_IPCommandTriggerDuringAHBAccessInterruptEnable,
kQSPI_IPCommandTriggerDuringIPAccessInterruptEnable,
kQSPI_IPCommandTriggerDuringAHBGrantInterruptEnable,
kQSPI_IPCommandTransactionFinishedInterruptEnable,
kQSPI_AllInterruptEnable = (int)0x8C83F8D1U }

```

*QSPI interrupt enable.*

- enum `_qspi_dma_enable` {
 

```

kQSPI_TxBufferFillDMAEnable = QuadSPI_RSER_TBFDE_MASK,
kQSPI_RxBufferDrainDMAEnable = QuadSPI_RSER_RBDDE_MASK,
kQSPI_AlIIDDMAEnable = QuadSPI_RSER_TBFDE_MASK | QuadSPI_RSER_RBDDE_MASK
}

```

- *QSPI DMA request flag.*  
enum `qspi_dqs_phrase_shift_t` {  
  kQSPI\_DQSNoPhraseShift = 0x0U,  
  kQSPI\_DQSPhraseShift45Degree,  
  kQSPI\_DQSPhraseShift90Degree,  
  kQSPI\_DQSPhraseShift135Degree }
  - *Phrase shift number for DQS mode.*  
enum `qspi_dqs_read_sample_clock_t` {  
  kQSPI\_ReadSampleClkInternalLoopback = 0x0U,  
  kQSPI\_ReadSampleClkLoopbackFromDqsPad = 0x1U,  
  kQSPI\_ReadSampleClkExternalInputFromDqsPad = 0x2U }
- Qspi read sampling option.*

## Driver version

- #define `FSL_QSPI_DRIVER_VERSION` (MAKE\_VERSION(2, 2, 3))  
*QSPI driver version 2.2.3.*

## Initialization and deinitialization

- `uint32_t QSPIGetInstance (QuadSPI_Type *base)`  
*Get the instance number for QSPI.*
- `void QSPI_Init (QuadSPI_Type *base, qspi_config_t *config, uint32_t srcClock_Hz)`  
*Initializes the QSPI module and internal state.*
- `void QSPI_GetDefaultQspiConfig (qspi_config_t *config)`  
*Gets default settings for QSPI.*
- `void QSPI_Deinit (QuadSPI_Type *base)`  
*Deinitializes the QSPI module.*
- `void QSPI_SetFlashConfig (QuadSPI_Type *base, qspi_flash_config_t *config)`  
*Configures the serial flash parameter.*
- `void QSPI_SetDqsConfig (QuadSPI_Type *base, qspi_dqs_config_t *config)`  
*Configures the serial flash DQS parameter.*
- `void QSPI_SoftwareReset (QuadSPI_Type *base)`  
*Software reset for the QSPI logic.*
- `static void QSPI_Enable (QuadSPI_Type *base, bool enable)`  
*Enables or disables the QSPI module.*

## Status

- `static uint32_t QSPI_GetStatusFlags (QuadSPI_Type *base)`  
*Gets the state value of QSPI.*
- `static uint32_t QSPI_GetErrorStatusFlags (QuadSPI_Type *base)`  
*Gets QSPI error status flags.*
- `static void QSPI_ClearErrorFlag (QuadSPI_Type *base, uint32_t mask)`  
*Clears the QSPI error flags.*

## Interrupts

- static void [QSPI\\_EnableInterrupts](#) (QuadSPI\_Type \*base, uint32\_t mask)  
*Enables the QSPI interrupts.*
- static void [QSPI\\_DisableInterrupts](#) (QuadSPI\_Type \*base, uint32\_t mask)  
*Disables the QSPI interrupts.*

## DMA Control

- static void [QSPI\\_EnableDMA](#) (QuadSPI\_Type \*base, uint32\_t mask, bool enable)  
*Enables the QSPI DMA source.*
- static uint32\_t [QSPI\\_GetTxDataRegisterAddress](#) (QuadSPI\_Type \*base)  
*Gets the Tx data register address.*
- uint32\_t [QSPI\\_GetRxDataRegisterAddress](#) (QuadSPI\_Type \*base)  
*Gets the Rx data register address used for DMA operation.*

## Bus Operations

- static void [QSPI\\_SetIPCommandAddress](#) (QuadSPI\_Type \*base, uint32\_t addr)  
*Sets the IP command address.*
- static void [QSPI\\_SetIPCommandSize](#) (QuadSPI\_Type \*base, uint32\_t size)  
*Sets the IP command size.*
- void [QSPI\\_ExecuteIPCommand](#) (QuadSPI\_Type \*base, uint32\_t index)  
*Executes IP commands located in LUT table.*
- void [QSPI\\_ExecuteAHBCommand](#) (QuadSPI\_Type \*base, uint32\_t index)  
*Executes AHB commands located in LUT table.*
- void [QSPI\\_UpdateLUT](#) (QuadSPI\_Type \*base, uint32\_t index, uint32\_t \*cmd)  
*Updates the LUT table.*
- static void [QSPI\\_ClearFifo](#) (QuadSPI\_Type \*base, uint32\_t mask)  
*Clears the QSPI FIFO logic.*
- static void [QSPI\\_ClearCommandSequence](#) (QuadSPI\_Type \*base, [qspi\\_command\\_seq\\_t](#) seq)  
*@ brief Clears the command sequence for the IP/buffer command.*
- static void [QSPI\\_EnableDDRMode](#) (QuadSPI\_Type \*base, bool enable)  
*Enable or disable DDR mode.*
- void [QSPI\\_SetReadDataArea](#) (QuadSPI\_Type \*base, [qspi\\_read\\_area\\_t](#) area)  
*@ brief Set the RX buffer readout area.*
- void [QSPI\\_WriteBlocking](#) (QuadSPI\_Type \*base, uint32\_t \*buffer, size\_t size)  
*Sends a buffer of data bytes using a blocking method.*
- static void [QSPI\\_WriteData](#) (QuadSPI\_Type \*base, uint32\_t data)  
*Writes data into FIFO.*
- void [QSPI\\_ReadBlocking](#) (QuadSPI\_Type \*base, uint32\_t \*buffer, size\_t size)  
*Receives a buffer of data bytes using a blocking method.*
- uint32\_t [QSPI\\_ReadData](#) (QuadSPI\_Type \*base)  
*Receives data from data FIFO.*

## Transactional

- static void [QSPI\\_TransferSendBlocking](#) (QuadSPI\_Type \*base, [qspi\\_transfer\\_t](#) \*xfer)  
*Writes data to the QSPI transmit buffer.*
- static void [QSPI\\_TransferReceiveBlocking](#) (QuadSPI\_Type \*base, [qspi\\_transfer\\_t](#) \*xfer)  
*Reads data from the QSPI receive buffer in polling way.*

### 32.2.2 Data Structure Documentation

#### 32.2.2.1 struct qspi\_dqs\_config\_t

##### Data Fields

- uint32\_t [portADelayTapNum](#)  
*Delay chain tap number selection for QSPI port A DQS.*
- [qspi\\_dqs\\_phrase\\_shift\\_t](#) [shift](#)  
*Phase shift for internal DQS generation.*
- [qspi\\_dqs\\_read\\_sample\\_clock\\_t](#) [rxSampleClock](#)  
*Read sample clock for Dqs.*
- bool [enableDQSClkInverse](#)  
*Enable inverse clock for internal DQS generation.*

##### Field Documentation

(1) [qspi\\_dqs\\_read\\_sample\\_clock\\_t](#) [qspi\\_dqs\\_config\\_t::rxSampleClock](#)

#### 32.2.2.2 struct qspi\_flash\_timing\_t

##### Data Fields

- uint32\_t [dataHoldTime](#)  
*Serial flash data in hold time.*
- uint32\_t [CSHoldTime](#)  
*Serial flash CS hold time in terms of serial flash clock cycles.*
- uint32\_t [CSSetupTime](#)  
*Serial flash CS setup time in terms of serial flash clock cycles.*

#### 32.2.2.3 struct qspi\_config\_t

##### Data Fields

- uint32\_t [clockSource](#)  
*Clock source for QSPI module.*
- uint32\_t [baudRate](#)  
*Serial flash clock baud rate.*
- uint8\_t [txWatermark](#)  
*QSPI transmit watermark value.*
- uint8\_t [rxWatermark](#)

*QSPI receive watermark value.*

- `uint32_t AHBbufferSize` [FSL\_FEATURE\_QSPI\_AHB\_BUFFER\_COUNT]  
*AHB buffer size.*
- `uint8_t AHBbufferMaster` [FSL\_FEATURE\_QSPI\_AHB\_BUFFER\_COUNT]  
*AHB buffer master.*
- `bool enableAHBbuffer3AllMaster`  
*Is AHB buffer3 for all master.*
- `qspi_read_area_t area`  
*Which area Rx data readout.*
- `bool enableQspi`  
*Enable QSPI after initialization.*

## Field Documentation

(1) `uint8_t qspi_config_t::rxWatermark`

(2) `uint32_t qspi_config_t::AHBbufferSize[FSL_FEATURE_QSPI_AHB_BUFFER_COUNT]`

(3) `uint8_t qspi_config_t::AHBbufferMaster[FSL_FEATURE_QSPI_AHB_BUFFER_COUNT]`

(4) `bool qspi_config_t::enableAHBbuffer3AllMaster`

### 32.2.2.4 struct qspi\_flash\_config\_t

#### Data Fields

- `uint32_t flashA1Size`  
*Flash A1 size.*
- `uint32_t flashA2Size`  
*Flash A2 size.*
- `uint32_t lookuptable` [FSL\_FEATURE\_QSPI\_LUT\_DEPTH]  
*Flash command in LUT.*
- `uint32_t dataHoldTime`  
*Data line hold time.*
- `uint32_t CSHoldTime`  
*CS line hold time.*
- `uint32_t CSSetupTime`  
*CS line setup time.*
- `uint32_t columnSpace`  
*Column space size.*
- `uint32_t dataLearnValue`  
*Data Learn value if enable data learn.*
- `qspi_endianness_t endian`  
*Flash data endianness.*
- `bool enableWordAddress`  
*If enable word address.*

## Field Documentation

(1) `uint32_t qspi_flash_config_t::dataHoldTime`

- (2) `qspi_endianness_t qspi_flash_config_t::endian`
- (3) `bool qspi_flash_config_t::enableWordAddress`

### 32.2.2.5 struct qspi\_transfer\_t

#### Data Fields

- `uint32_t * data`  
*Pointer to data to transmit.*
- `size_t dataSize`  
*Bytes to be transmit.*

### 32.2.2.6 struct ip\_command\_config\_t

## 32.2.3 Macro Definition Documentation

### 32.2.3.1 #define FSL\_QSPI\_DRIVER\_VERSION (MAKE\_VERSION(2, 2, 3))

## 32.2.4 Enumeration Type Documentation

### 32.2.4.1 anonymous enum

Enumerator

- `kStatus_QSPI_Idle` QSPI is in idle state.
- `kStatus_QSPI_Busy` QSPI is busy.
- `kStatus_QSPI_Error` Error occurred during QSPI transfer.

### 32.2.4.2 enum qspi\_read\_area\_t

Enumerator

- `kQSPI_ReadAHB` QSPI read from AHB buffer.
- `kQSPI_ReadIP` QSPI read from IP FIFO.

### 32.2.4.3 enum qspi\_command\_seq\_t

Enumerator

- `kQSPI_IPSeq` IP command sequence.
- `kQSPI_BufferSeq` Buffer command sequence.

### 32.2.4.4 enum qspi\_fifo\_t

Enumerator

- kQSPI\_TxFifo* QSPI Tx FIFO.
- kQSPI\_RxFifo* QSPI Rx FIFO.
- kQSPI\_AllFifo* QSPI all FIFO, including Tx and Rx.

### 32.2.4.5 enum qspi\_endianness\_t

Enumerator

- kQSPI\_64BigEndian* 64 bits big endian
- kQSPI\_32LittleEndian* 32 bit little endian
- kQSPI\_32BigEndian* 32 bit big endian
- kQSPI\_64LittleEndian* 64 bit little endian

### 32.2.4.6 enum \_qspi\_error\_flags

Enumerator

- kQSPI\_DataLearningFail* Data learning pattern failure flag.
- kQSPI\_TxBufferFill* Tx buffer fill flag.
- kQSPI\_TxBufferUnderrun* Tx buffer underrun flag.
- kQSPI\_IllegalInstruction* Illegal instruction error flag.
- kQSPI\_RxBufferOverflow* Rx buffer overflow flag.
- kQSPI\_RxBufferDrain* Rx buffer drain flag.
- kQSPI\_AHBSequenceError* AHB sequence error flag.
- kQSPI\_AHBIllegalTransaction* AHB illegal transaction error flag.
- kQSPI\_AHBIllegalBurstSize* AHB illegal burst error flag.
- kQSPI\_AHBBufferOverflow* AHB buffer overflow flag.
- kQSPI\_IPCommandTriggerDuringAHBAccess* IP command trigger during AHB access error.
- kQSPI\_IPCommandTriggerDuringIPAccess* IP command trigger cannot be executed.
- kQSPI\_IPCommandTriggerDuringAHBGrant* IP command trigger during AHB grant error.
- kQSPI\_IPCommandTransactionFinished* IP command transaction finished flag.
- kQSPI\_FlagAll* All error flag.

### 32.2.4.7 enum \_qspi\_flags

Enumerator

- kQSPI\_DataLearningSamplePoint* Data learning sample point.
- kQSPI\_TxBufferFull* Tx buffer full flag.

*kQSPI\_TxDMA* Tx DMA is requested or running.  
*kQSPI\_TxWatermark* Tx buffer watermark available.  
*kQSPI\_TxBufferEnoughData* Tx buffer enough data available.  
*kQSPI\_RxDMA* Rx DMA is requesting or running.  
*kQSPI\_RxBufferFull* Rx buffer full.  
*kQSPI\_RxWatermark* Rx buffer watermark exceeded.  
*kQSPI\_AHB3BufferFull* AHB buffer 3 full.  
*kQSPI\_AHB2BufferFull* AHB buffer 2 full.  
*kQSPI\_AHB1BufferFull* AHB buffer 1 full.  
*kQSPI\_AHB0BufferFull* AHB buffer 0 full.  
*kQSPI\_AHB3BufferNotEmpty* AHB buffer 3 not empty.  
*kQSPI\_AHB2BufferNotEmpty* AHB buffer 2 not empty.  
*kQSPI\_AHB1BufferNotEmpty* AHB buffer 1 not empty.  
*kQSPI\_AHB0BufferNotEmpty* AHB buffer 0 not empty.  
*kQSPI\_AHBTransactionPending* AHB access transaction pending.  
*kQSPI\_AHBCmdPriorityGranted* AHB command priority granted.  
*kQSPI\_AHBAccess* AHB access.  
*kQSPI\_IPAccess* IP access.  
*kQSPI\_Busy* Module busy.  
*kQSPI\_StateAll* All flags.

### 32.2.4.8 enum \_qspi\_interrupt\_enable

Enumerator

*kQSPI\_DataLearningFailInterruptEnable* Data learning pattern failure interrupt enable.  
*kQSPI\_TxBufferFillInterruptEnable* Tx buffer fill interrupt enable.  
*kQSPI\_TxBufferUnderrunInterruptEnable* Tx buffer underrun interrupt enable.  
*kQSPI\_IllegalInstructionInterruptEnable* Illegal instruction error interrupt enable.  
*kQSPI\_RxBufferOverflowInterruptEnable* Rx buffer overflow interrupt enable.  
*kQSPI\_RxBufferDrainInterruptEnable* Rx buffer drain interrupt enable.  
*kQSPI\_AHBSequenceErrorInterruptEnable* AHB sequence error interrupt enable.  
*kQSPI\_AHBIIllegalTransactionInterruptEnable* AHB illegal transaction error interrupt enable.  
*kQSPI\_AHBIIllegalBurstSizeInterruptEnable* AHB illegal burst error interrupt enable.  
*kQSPI\_AHBBufferOverflowInterruptEnable* AHB buffer overflow interrupt enable.  
*kQSPI\_IPCommandTriggerDuringAHBAccessInterruptEnable* IP command trigger during AHB access error.  
*kQSPI\_IPCommandTriggerDuringIPAccessInterruptEnable* IP command trigger cannot be executed.  
*kQSPI\_IPCommandTriggerDuringAHBGrantInterruptEnable* IP command trigger during AHB grant error.  
*kQSPI\_IPCommandTransactionFinishedInterruptEnable* IP command transaction finished interrupt enable.  
*kQSPI\_AllInterruptEnable* All error interrupt enable.

### 32.2.4.9 enum \_qspi\_dma\_enable

Enumerator

*kQSPI\_TxBufferFillDMAEnable* Tx buffer fill DMA.

*kQSPI\_RxBufferDrainDMAEnable* Rx buffer drain DMA.

*kQSPI\_AllDDMAEnable* All DMA source.

### 32.2.4.10 enum qspi\_dqs\_phrase\_shift\_t

Enumerator

*kQSPI\_DQSNoPhraseShift* No phase shift.

*kQSPI\_DQSPhraseShift45Degree* Select 45 degree phase shift.

*kQSPI\_DQSPhraseShift90Degree* Select 90 degree phase shift.

*kQSPI\_DQSPhraseShift135Degree* Select 135 degree phase shift.

### 32.2.4.11 enum qspi\_dqs\_read\_sample\_clock\_t

Enumerator

*kQSPI\_ReadSampleClkInternalLoopback* Read sample clock adopts internal loopback mode.

*kQSPI\_ReadSampleClkLoopbackFromDqsPad* Dummy Read strobe generated by QSPI Controller and loopback from DQS pad.

*kQSPI\_ReadSampleClkExternalInputFromDqsPad* Flash provided Read strobe and input from D-QS pad.

## 32.2.5 Function Documentation

### 32.2.5.1 uint32\_t QSPI\_GetInstance ( QuadSPI\_Type \* *base* )

Parameters

|             |                    |
|-------------|--------------------|
| <i>base</i> | QSPI base pointer. |
|-------------|--------------------|

### 32.2.5.2 void QSPI\_Init ( QuadSPI\_Type \* *base*, qspi\_config\_t \* *config*, uint32\_t *srcClock\_Hz* )

This function enables the clock for QSPI and also configures the QSPI with the input configure parameters. Users should call this function before any QSPI operations.

Parameters

|                    |                                    |
|--------------------|------------------------------------|
| <i>base</i>        | Pointer to QuadSPI Type.           |
| <i>config</i>      | QSPI configure structure.          |
| <i>srcClock_Hz</i> | QSPI source clock frequency in Hz. |

### 32.2.5.3 void QSPI\_GetDefaultQspiConfig ( *qspi\_config\_t* \* *config* )

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>config</i> | QSPI configuration structure. |
|---------------|-------------------------------|

### 32.2.5.4 void QSPI\_Deinit ( *QuadSPI\_Type* \* *base* )

Clears the QSPI state and QSPI module registers.

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | Pointer to QuadSPI Type. |
|-------------|--------------------------|

### 32.2.5.5 void QSPI\_SetFlashConfig ( *QuadSPI\_Type* \* *base*, *qspi\_flash\_config\_t* \* *config* )

This function configures the serial flash relevant parameters, such as the size, command, and so on. The flash configuration value cannot have a default value. The user needs to configure it according to the QSPI features.

Parameters

|               |                                 |
|---------------|---------------------------------|
| <i>base</i>   | Pointer to QuadSPI Type.        |
| <i>config</i> | Flash configuration parameters. |

### 32.2.5.6 void QSPI\_SetDqsConfig ( *QuadSPI\_Type* \* *base*, *qspi\_dqs\_config\_t* \* *config* )

This function configures the serial flash DQS relevant parameters, such as the delay chain tap number, . DQS shift phase, whether need to inverse and the rxc sample clock selection.

Parameters

|               |                               |
|---------------|-------------------------------|
| <i>base</i>   | Pointer to QuadSPI Type.      |
| <i>config</i> | Dqs configuration parameters. |

### 32.2.5.7 void QSPI\_SoftwareReset ( QuadSPI\_Type \* *base* )

This function sets the software reset flags for both AHB and buffer domain and resets both AHB buffer and also IP FIFOs.

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | Pointer to QuadSPI Type. |
|-------------|--------------------------|

### 32.2.5.8 static void QSPI\_Enable ( QuadSPI\_Type \* *base*, bool *enable* ) [inline], [static]

Parameters

|               |                                              |
|---------------|----------------------------------------------|
| <i>base</i>   | Pointer to QuadSPI Type.                     |
| <i>enable</i> | True means enable QSPI, false means disable. |

### 32.2.5.9 static uint32\_t QSPI\_GetStatusFlags ( QuadSPI\_Type \* *base* ) [inline], [static]

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | Pointer to QuadSPI Type. |
|-------------|--------------------------|

Returns

status flag, use status flag to AND [\\_qspi\\_flags](#) could get the related status.

### 32.2.5.10 static uint32\_t QSPI\_GetErrorStatusFlags ( QuadSPI\_Type \* *base* ) [inline], [static]

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | Pointer to QuadSPI Type. |
|-------------|--------------------------|

Returns

status flag, use status flag to AND `_qspi_error_flags` could get the related status.

### 32.2.5.11 static void QSPI\_ClearErrorFlag ( QuadSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

|             |                                                                                           |
|-------------|-------------------------------------------------------------------------------------------|
| <i>base</i> | Pointer to QuadSPI Type.                                                                  |
| <i>mask</i> | Which kind of QSPI flags to be cleared, a combination of <code>_qspi_error_flags</code> . |

### 32.2.5.12 static void QSPI\_EnableInterrupts ( QuadSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | Pointer to QuadSPI Type. |
| <i>mask</i> | QSPI interrupt source.   |

### 32.2.5.13 static void QSPI\_DisableInterrupts ( QuadSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | Pointer to QuadSPI Type. |
| <i>mask</i> | QSPI interrupt source.   |

### 32.2.5.14 static void QSPI\_EnableDMA ( QuadSPI\_Type \* *base*, uint32\_t *mask*, bool *enable* ) [inline], [static]

Parameters

|               |                                             |
|---------------|---------------------------------------------|
| <i>base</i>   | Pointer to QuadSPI Type.                    |
| <i>mask</i>   | QSPI DMA source.                            |
| <i>enable</i> | True means enable DMA, false means disable. |

### 32.2.5.15 static uint32\_t QSPI\_GetTxDataRegisterAddress ( QuadSPI\_Type \* *base* ) [inline], [static]

It is used for DMA operation.

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | Pointer to QuadSPI Type. |
|-------------|--------------------------|

Returns

QSPI Tx data register address.

### 32.2.5.16 uint32\_t QSPI\_GetRxDataRegisterAddress ( QuadSPI\_Type \* *base* )

This function returns the Rx data register address or Rx buffer address according to the Rx read area settings.

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | Pointer to QuadSPI Type. |
|-------------|--------------------------|

Returns

QSPI Rx data register address.

### 32.2.5.17 static void QSPI\_SetIPCommandAddress ( QuadSPI\_Type \* *base*, uint32\_t *addr* ) [inline], [static]

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | Pointer to QuadSPI Type. |
| <i>addr</i> | IP command address.      |

**32.2.5.18 static void QSPI\_SetIPCommandSize ( QuadSPI\_Type \* *base*, uint32\_t *size* )  
[inline], [static]**

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | Pointer to QuadSPI Type. |
| <i>size</i> | IP command size.         |

**32.2.5.19 void QSPI\_ExecuteIPCommand ( QuadSPI\_Type \* *base*, uint32\_t *index* )**

Parameters

|              |                                              |
|--------------|----------------------------------------------|
| <i>base</i>  | Pointer to QuadSPI Type.                     |
| <i>index</i> | IP command located in which LUT table index. |

**32.2.5.20 void QSPI\_ExecuteAHBCommand ( QuadSPI\_Type \* *base*, uint32\_t *index* )**

Parameters

|              |                                               |
|--------------|-----------------------------------------------|
| <i>base</i>  | Pointer to QuadSPI Type.                      |
| <i>index</i> | AHB command located in which LUT table index. |

**32.2.5.21 void QSPI\_UpdateLUT ( QuadSPI\_Type \* *base*, uint32\_t *index*, uint32\_t \* *cmd* )**

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | Pointer to QuadSPI Type. |
|-------------|--------------------------|

|              |                                                                            |
|--------------|----------------------------------------------------------------------------|
| <i>index</i> | Which LUT index needs to be located. It should be an integer divided by 4. |
| <i>cmd</i>   | Command sequence array.                                                    |

**32.2.5.22 static void QSPI\_ClearFifo ( QuadSPI\_Type \* *base*, uint32\_t *mask* ) [inline], [static]**

Parameters

|             |                                        |
|-------------|----------------------------------------|
| <i>base</i> | Pointer to QuadSPI Type.               |
| <i>mask</i> | Which kind of QSPI FIFO to be cleared. |

**32.2.5.23 static void QSPI\_ClearCommandSequence ( QuadSPI\_Type \* *base*, qspi\_command\_seq\_t *seq* ) [inline], [static]**

This function can reset the command sequence.

Parameters

|             |                                                                           |
|-------------|---------------------------------------------------------------------------|
| <i>base</i> | QSPI base address.                                                        |
| <i>seq</i>  | Which command sequence need to reset, IP command, buffer command or both. |

**32.2.5.24 static void QSPI\_EnableDDRMode ( QuadSPI\_Type \* *base*, bool *enable* ) [inline], [static]**

Parameters

|               |                                                           |
|---------------|-----------------------------------------------------------|
| <i>base</i>   | QSPI base pointer                                         |
| <i>enable</i> | True means enable DDR mode, false means disable DDR mode. |

**32.2.5.25 void QSPI\_SetReadDataArea ( QuadSPI\_Type \* *base*, qspi\_read\_area\_t *area* )**

This function can set the RX buffer readout, from AHB bus or IP Bus.

Parameters

|             |                                                               |
|-------------|---------------------------------------------------------------|
| <i>base</i> | QSPI base address.                                            |
| <i>area</i> | QSPI Rx buffer readout area. AHB bus buffer or IP bus buffer. |

**32.2.5.26 void QSPI\_WriteBlocking ( QuadSPI\_Type \* *base*, uint32\_t \* *buffer*, size\_t *size* )**

Note

This function blocks via polling until all bytes have been sent.

Parameters

|               |                                  |
|---------------|----------------------------------|
| <i>base</i>   | QSPI base pointer                |
| <i>buffer</i> | The data bytes to send           |
| <i>size</i>   | The number of data bytes to send |

**32.2.5.27 static void QSPI\_WriteData ( QuadSPI\_Type \* *base*, uint32\_t *data* ) [inline], [static]**

Parameters

|             |                        |
|-------------|------------------------|
| <i>base</i> | QSPI base pointer      |
| <i>data</i> | The data bytes to send |

**32.2.5.28 void QSPI\_ReadBlocking ( QuadSPI\_Type \* *base*, uint32\_t \* *buffer*, size\_t *size* )**

Note

This function blocks via polling until all bytes have been sent. Users shall notice that this receive size shall not bigger than 64 bytes. As this interface is used to read flash status registers. For flash contents read, please use AHB bus read, this is much more efficiency.

Parameters

|               |                                     |
|---------------|-------------------------------------|
| <i>base</i>   | QSPI base pointer                   |
| <i>buffer</i> | The data bytes to send              |
| <i>size</i>   | The number of data bytes to receive |

**32.2.5.29 uint32\_t QSPI\_ReadData ( QuadSPI\_Type \* *base* )**

Parameters

|             |                   |
|-------------|-------------------|
| <i>base</i> | QSPI base pointer |
|-------------|-------------------|

Returns

The data in the FIFO.

**32.2.5.30 static void QSPI\_TransferSendBlocking ( QuadSPI\_Type \* *base*, qspi\_transfer\_t \* *xfer* ) [inline], [static]**

This function writes a continuous data to the QSPI transmit FIFO. This function is a block function and can return only when finished. This function uses polling methods.

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | Pointer to QuadSPI Type. |
| <i>xfer</i> | QSPI transfer structure. |

**32.2.5.31 static void QSPI\_TransferReceiveBlocking ( QuadSPI\_Type \* *base*, qspi\_transfer\_t \* *xfer* ) [inline], [static]**

This function reads continuous data from the QSPI receive buffer/FIFO. This function is a blocking function and can return only when finished. This function uses polling methods. Users shall notice that this receive size shall not bigger than 64 bytes. As this interface is used to read flash status registers. For flash contents read, please use AHB bus read, this is much more efficiency.

Parameters

|             |                          |
|-------------|--------------------------|
| <i>base</i> | Pointer to QuadSPI Type. |
| <i>xfer</i> | QSPI transfer structure. |

# Chapter 33

## SAI: Serial Audio Interface

### 33.1 Overview

The MCUXpresso SDK provides a peripheral driver for the Serial Audio Interface (SAI) module of MCUXpresso SDK devices.

SAI driver includes functional APIs and transactional APIs.

Functional APIs target low-level APIs. Functional APIs can be used for SAI initialization, configuration and operation, and for optimization and customization purposes. Using the functional API requires the knowledge of the SAI peripheral and how to organize functional APIs to meet the application requirements. All functional API use the peripheral base address as the first parameter. SAI functional operation groups provide the functional API set.

Transactional APIs target high-level APIs. Transactional APIs can be used to enable the peripheral and in the application if the code size and performance of transactional APIs satisfy the requirements. If the code size and performance are a critical requirement, see the transactional API implementation and write a custom code. All transactional APIs use the `sai_handle_t` as the first parameter. Initialize the handle by calling the [SAI\\_TransferTxCreateHandle\(\)](#) or [SAI\\_TransferRxCreateHandle\(\)](#) API.

Transactional APIs support asynchronous transfer. This means that the functions [SAI\\_TransferSendNonBlocking\(\)](#) and [SAI\\_TransferReceiveNonBlocking\(\)](#) set up the interrupt for data transfer. When the transfer completes, the upper layer is notified through a callback function with the `kStatus_SAI_TxIdle` and `kStatus_SAI_RxIdle` status.

### 33.2 Typical configurations

#### Bit width configuration

SAI driver support 8/16/24/32bits stereo/mono raw audio data transfer. SAI EDMA driver support 8/16/32bits stereo/mono raw audio data transfer, since the EDMA doesn't support 24bit data width, so application should pre-convert the 24bit data to 32bit. SAI DMA driver support 8/16/32bits stereo/mono raw audio data transfer, since the EDMA doesn't support 24bit data width, so application should pre-convert the 24bit data to 32bit. SAI SDMA driver support 8/16/24/32bits stereo/mono raw audio data transfer.

#### Frame configuration

SAI driver support I2S, DSP, Left justified, Right justified, TDM mode. Application can call the api directly: `SAI_GetClassicI2SConfig` `SAI_GetLeftJustifiedConfig` `SAI_GetRightJustifiedConfig` `SAI_GetTDMConfig` `SAI_GetDSPConfig`

### 33.3 Typical use case

#### 33.3.1 SAI Send/receive using an interrupt method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/sai

#### 33.3.2 SAI Send/receive using a DMA method

Refer to the driver examples codes located at <SDK\_ROOT>/boards/<BOARD>/driver\_examples/sai

## Modules

- [SAI Driver](#)
- [SAI EDMA Driver](#)

## 33.4 SAI Driver

### 33.4.1 Overview

#### Data Structures

- struct `sai_config_t`  
*SAI user configuration structure. [More...](#)*
- struct `sai_transfer_format_t`  
*sai transfer format [More...](#)*
- struct `sai_fifo_t`  
*sai fifo configurations [More...](#)*
- struct `sai_bit_clock_t`  
*sai bit clock configurations [More...](#)*
- struct `sai_frame_sync_t`  
*sai frame sync configurations [More...](#)*
- struct `sai_serial_data_t`  
*sai serial data configurations [More...](#)*
- struct `sai_transceiver_t`  
*sai transceiver configurations [More...](#)*
- struct `sai_transfer_t`  
*SAI transfer structure. [More...](#)*
- struct `sai_handle_t`  
*SAI handle structure. [More...](#)*

#### Macros

- #define `SAI_XFER_QUEUE_SIZE` (4U)  
*SAI transfer queue size, user can refine it according to use case.*
- #define `FSL_SAI_HAS_FIFO_EXTEND_FEATURE` 1  
*sai fifo feature*

#### Typedefs

- typedef void(\* `sai_transfer_callback_t` )(I2S\_Type \*base, sai\_handle\_t \*handle, `status_t` status, void \*userData)  
*SAI transfer callback prototype.*

## Enumerations

- enum {
   
kStatus\_SAI\_TxBusy = MAKE\_STATUS(kStatusGroup\_SAI, 0),
   
kStatus\_SAI\_RxBusy = MAKE\_STATUS(kStatusGroup\_SAI, 1),
   
kStatus\_SAI\_TxError = MAKE\_STATUS(kStatusGroup\_SAI, 2),
   
kStatus\_SAI\_RxError = MAKE\_STATUS(kStatusGroup\_SAI, 3),
   
kStatus\_SAI\_QueueFull = MAKE\_STATUS(kStatusGroup\_SAI, 4),
   
kStatus\_SAI\_TxIdle = MAKE\_STATUS(kStatusGroup\_SAI, 5),
   
kStatus\_SAI\_RxIdle = MAKE\_STATUS(kStatusGroup\_SAI, 6) }
   
*\_sai\_status\_t, SAI return status.*
- enum {
   
kSAI\_Channel0Mask = 1 << 0U,
   
kSAI\_Channel1Mask = 1 << 1U,
   
kSAI\_Channel2Mask = 1 << 2U,
   
kSAI\_Channel3Mask = 1 << 3U,
   
kSAI\_Channel4Mask = 1 << 4U,
   
kSAI\_Channel5Mask = 1 << 5U,
   
kSAI\_Channel6Mask = 1 << 6U,
   
kSAI\_Channel7Mask = 1 << 7U }  
*\_sai\_channel\_mask,.sai channel mask value, actual channel numbers is depend soc specific*
- enum **sai\_protocol\_t** {
   
kSAI\_BusLeftJustified = 0x0U,
   
kSAI\_BusRightJustified,
   
kSAI\_BusI2S,
   
kSAI\_BusPCMA,
   
kSAI\_BusPCMB }
- Define the SAI bus type.*
- enum **sai\_master\_slave\_t** {
   
kSAI\_Master = 0x0U,
   
kSAI\_Slave = 0x1U,
   
kSAI\_Bclk\_Master\_FrameSync\_Slave = 0x2U,
   
kSAI\_Bclk\_Slave\_FrameSync\_Master = 0x3U }  
*Master or slave mode.*
- enum **sai\_mono\_stereo\_t** {
   
kSAI\_Stereo = 0x0U,
   
kSAI\_MonoRight,
   
kSAI\_MonoLeft }
- Mono or stereo audio format.*
- enum **sai\_data\_order\_t** {
   
kSAI\_DataLSB = 0x0U,
   
kSAI\_DataMSB }
- SAI data order, MSB or LSB.*
- enum **sai\_clock\_polarity\_t** {

- ```
kSAI_PolarityActiveHigh = 0x0U,
kSAI_PolarityActiveLow = 0x1U,
kSAI_SampleOnFallingEdge = 0x0U,
kSAI_SampleOnRisingEdge = 0x1U }
```

SAI clock polarity, active high or low.
- enum `sai_sync_mode_t` {


```
kSAI_ModeAsync = 0x0U,
kSAI_ModeSync }
```

Synchronous or asynchronous mode.
- enum `sai_bclk_source_t` {


```
kSAI_BclkSourceBusclk = 0x0U,
kSAI_BclkSourceMclkOption1 = 0x1U,
kSAI_BclkSourceMclkOption2 = 0x2U,
kSAI_BclkSourceMclkOption3 = 0x3U,
kSAI_BclkSourceMclkDiv = 0x1U,
kSAI_BclkSourceOtherSai0 = 0x2U,
kSAI_BclkSourceOtherSai1 = 0x3U }
```

Bit clock source.
- enum {


```
kSAI_WordStartInterruptEnable,
kSAI_SyncErrorInterruptEnable = I2S_TCSR_SEIE_MASK,
kSAI_FIFOWarningInterruptEnable = I2S_TCSR_FWIE_MASK,
kSAI_FIFOErrorInterruptEnable = I2S_TCSR_FEIE_MASK,
kSAI_FIFORequestInterruptEnable = I2S_TCSR_FRIE_MASK }
```

_sai_interrupt_enable_t, The SAI interrupt enable flag
- enum {


```
kSAI_FIFOWarningDMAEnable = I2S_TCSR_FWDE_MASK,
kSAI_FIFORequestDMAEnable = I2S_TCSR_FRDE_MASK }
```

_sai_dma_enable_t, The DMA request sources
- enum {


```
kSAI_WordStartFlag = I2S_TCSR_WSF_MASK,
kSAI_SyncErrorFlag = I2S_TCSR_SEF_MASK,
kSAI_FIFOErrorFlag = I2S_TCSR_FEF_MASK,
kSAI_FIFORequestFlag = I2S_TCSR_FRF_MASK,
kSAI_FIFOWarningFlag = I2S_TCSR_FWF_MASK }
```

_sai_flags, The SAI status flag
- enum `sai_reset_type_t` {


```
kSAI_ResetTypeSoftware = I2S_TCSR_SR_MASK,
kSAI_ResetTypeFIFO = I2S_TCSR_FR_MASK,
kSAI_ResetAll = I2S_TCSR_SR_MASK | I2S_TCSR_FR_MASK }
```

The reset type.
- enum `sai_fifo_packing_t` {


```
kSAI_FifoPackingDisabled = 0x0U,
kSAI_FifoPacking8bit = 0x2U,
kSAI_FifoPacking16bit = 0x3U }
```

The SAI packing mode The mode includes 8 bit and 16 bit packing.
- enum `sai_sample_rate_t` {

```
kSAI_SampleRate8KHz = 8000U,
kSAI_SampleRate11025Hz = 11025U,
kSAI_SampleRate12KHz = 12000U,
kSAI_SampleRate16KHz = 16000U,
kSAI_SampleRate22050Hz = 22050U,
kSAI_SampleRate24KHz = 24000U,
kSAI_SampleRate32KHz = 32000U,
kSAI_SampleRate44100Hz = 44100U,
kSAI_SampleRate48KHz = 48000U,
kSAI_SampleRate96KHz = 96000U,
kSAI_SampleRate192KHz = 192000U,
kSAI_SampleRate384KHz = 384000U }
```

Audio sample rate.

- enum `sai_word_width_t` {

kSAI_WordWidth8bits = 8U,

kSAI_WordWidth16bits = 16U,

kSAI_WordWidth24bits = 24U,

kSAI_WordWidth32bits = 32U }

Audio word width.

- enum `sai_data_pin_state_t` {

kSAI_DataPinStateTriState,

kSAI_DataPinStateOutputZero = 1U }
- sai data pin state definition*
- enum `sai_fifo_combine_t` {

kSAI_FifoCombineDisabled = 0U,

kSAI_FifoCombineModeEnabledOnRead,

kSAI_FifoCombineModeEnabledOnWrite,

kSAI_FifoCombineModeEnabledOnReadWrite }
- sai fifo combine mode definition*

- enum `sai_transceiver_type_t` {

kSAI_Transmitter = 0U,

kSAI_Receiver = 1U }
- sai transceiver type*
- enum `sai_frame_sync_len_t` {

kSAI_FrameSyncLenOneBitClk = 0U,

kSAI_FrameSyncLenPerWordWidth = 1U }
- sai frame sync len*

Driver version

- #define `FSL_SAI_DRIVER_VERSION` (`MAKE_VERSION(2, 3, 5)`)
- Version 2.3.5.*

Initialization and deinitialization

- void **SAI_TxInit** (I2S_Type *base, const **sai_config_t** *config)
Initializes the SAI Tx peripheral.
- void **SAI_RxInit** (I2S_Type *base, const **sai_config_t** *config)
Initializes the SAI Rx peripheral.
- void **SAI_TxGetDefaultConfig** (**sai_config_t** *config)
Sets the SAI Tx configuration structure to default values.
- void **SAI_RxGetDefaultConfig** (**sai_config_t** *config)
Sets the SAI Rx configuration structure to default values.
- void **SAI_Init** (I2S_Type *base)
Initializes the SAI peripheral.
- void **SAI_Deinit** (I2S_Type *base)
De-initializes the SAI peripheral.
- void **SAI_TxReset** (I2S_Type *base)
Resets the SAI Tx.
- void **SAI_RxReset** (I2S_Type *base)
Resets the SAI Rx.
- void **SAI_TxEnable** (I2S_Type *base, bool enable)
Enables/disables the SAI Tx.
- void **SAI_RxEnable** (I2S_Type *base, bool enable)
Enables/disables the SAI Rx.
- static void **SAI_TxSetBitClockDirection** (I2S_Type *base, **sai_master_slave_t** masterSlave)
Set Rx bit clock direction.
- static void **SAI_RxSetBitClockDirection** (I2S_Type *base, **sai_master_slave_t** masterSlave)
Set Rx bit clock direction.
- static void **SAI_RxSetFrameSyncDirection** (I2S_Type *base, **sai_master_slave_t** masterSlave)
Set Rx frame sync direction.
- static void **SAI_TxSetFrameSyncDirection** (I2S_Type *base, **sai_master_slave_t** masterSlave)
Set Tx frame sync direction.
- void **SAI_TxSetBitClockRate** (I2S_Type *base, uint32_t sourceClockHz, uint32_t sampleRate, uint32_t bitWidth, uint32_t channelNumbers)
Transmitter bit clock rate configurations.
- void **SAI_RxSetBitClockRate** (I2S_Type *base, uint32_t sourceClockHz, uint32_t sampleRate, uint32_t bitWidth, uint32_t channelNumbers)
Receiver bit clock rate configurations.
- void **SAI_TxSetBitclockConfig** (I2S_Type *base, **sai_master_slave_t** masterSlave, **sai_bit_clock_t** *config)
Transmitter Bit clock configurations.
- void **SAI_RxSetBitclockConfig** (I2S_Type *base, **sai_master_slave_t** masterSlave, **sai_bit_clock_t** *config)
Receiver Bit clock configurations.
- void **SAI_TxSetFifoConfig** (I2S_Type *base, **sai_fifo_t** *config)
SAI transmitter fifo configurations.
- void **SAI_RxSetFifoConfig** (I2S_Type *base, **sai_fifo_t** *config)
SAI receiver fifo configurations.
- void **SAI_TxSetFrameSyncConfig** (I2S_Type *base, **sai_master_slave_t** masterSlave, **sai_frame_sync_t** *config)
SAI transmitter Frame sync configurations.
- void **SAI_RxSetFrameSyncConfig** (I2S_Type *base, **sai_master_slave_t** masterSlave, **sai_frame_sync_t** *config)
SAI receiver Frame sync configurations.

- `sync_t *config`
SAI receiver Frame sync configurations.
- void `SAI_TxSetSerialDataConfig` (I2S_Type *base, `sai_serial_data_t` *config)
SAI transmitter Serial data configurations.
- void `SAI_RxSetSerialDataConfig` (I2S_Type *base, `sai_serial_data_t` *config)
SAI receiver Serial data configurations.
- void `SAI_TxSetConfig` (I2S_Type *base, `sai_transceiver_t` *config)
SAI transmitter configurations.
- void `SAI_RxSetConfig` (I2S_Type *base, `sai_transceiver_t` *config)
SAI receiver configurations.
- void `SAI_GetClassicI2SConfig` (`sai_transceiver_t` *config, `sai_word_width_t` bitWidth, `sai_mono_stereo_t` mode, `uint32_t` saiChannelMask)
Get classic I2S mode configurations.
- void `SAI_GetLeftJustifiedConfig` (`sai_transceiver_t` *config, `sai_word_width_t` bitWidth, `sai_mono_stereo_t` mode, `uint32_t` saiChannelMask)
Get left justified mode configurations.
- void `SAI_GetRightJustifiedConfig` (`sai_transceiver_t` *config, `sai_word_width_t` bitWidth, `sai_mono_stereo_t` mode, `uint32_t` saiChannelMask)
Get right justified mode configurations.
- void `SAI_GetTDMConfig` (`sai_transceiver_t` *config, `sai_frame_sync_len_t` frameSyncWidth, `sai_word_width_t` bitWidth, `uint32_t` dataWordNum, `uint32_t` saiChannelMask)
Get TDM mode configurations.
- void `SAI_GetDSPConfig` (`sai_transceiver_t` *config, `sai_frame_sync_len_t` frameSyncWidth, `sai_word_width_t` bitWidth, `sai_mono_stereo_t` mode, `uint32_t` saiChannelMask)
Get DSP mode configurations.

Status

- static `uint32_t SAI_TxGetStatusFlag` (I2S_Type *base)
Gets the SAI Tx status flag state.
- static void `SAI_TxClearStatusFlags` (I2S_Type *base, `uint32_t` mask)
Clears the SAI Tx status flag state.
- static `uint32_t SAI_RxGetStatusFlag` (I2S_Type *base)
Gets the SAI Rx status flag state.
- static void `SAI_RxClearStatusFlags` (I2S_Type *base, `uint32_t` mask)
Clears the SAI Rx status flag state.
- void `SAI_TxSoftwareReset` (I2S_Type *base, `sai_reset_type_t` type)
Do software reset or FIFO reset .
- void `SAI_RxSoftwareReset` (I2S_Type *base, `sai_reset_type_t` type)
Do software reset or FIFO reset .
- void `SAI_TxSetChannelFIFOMask` (I2S_Type *base, `uint8_t` mask)
Set the Tx channel FIFO enable mask.
- void `SAI_RxSetChannelFIFOMask` (I2S_Type *base, `uint8_t` mask)
Set the Rx channel FIFO enable mask.
- void `SAI_TxSetDataOrder` (I2S_Type *base, `sai_data_order_t` order)
Set the Tx data order.
- void `SAI_RxSetDataOrder` (I2S_Type *base, `sai_data_order_t` order)
Set the Rx data order.
- void `SAI_TxSetBitClockPolarity` (I2S_Type *base, `sai_clock_polarity_t` polarity)

- void [SAI_RxSetBitClockPolarity](#) (I2S_Type *base, sai_clock_polarity_t polarity)
 - Set the Tx data order.*
- void [SAI_TxSetFrameSyncPolarity](#) (I2S_Type *base, sai_clock_polarity_t polarity)
 - Set the Rx data order.*
- void [SAI_RxSetFrameSyncPolarity](#) (I2S_Type *base, sai_clock_polarity_t polarity)
 - Set the Tx data order.*
- void [SAI_TxSetFIFOPacking](#) (I2S_Type *base, sai_fifo_packing_t pack)
 - Set Tx FIFO packing feature.*
- void [SAI_RxSetFIFOPacking](#) (I2S_Type *base, sai_fifo_packing_t pack)
 - Set Rx FIFO packing feature.*
- static void [SAI_TxSetFIFOErrorContinue](#) (I2S_Type *base, bool isEnabled)
 - Set Tx FIFO error continue.*
- static void [SAI_RxSetFIFOErrorContinue](#) (I2S_Type *base, bool isEnabled)
 - Set Rx FIFO error continue.*

Interrupts

- static void [SAI_TxEnableInterrupts](#) (I2S_Type *base, uint32_t mask)
 - Enables the SAI Tx interrupt requests.*
- static void [SAI_RxEnableInterrupts](#) (I2S_Type *base, uint32_t mask)
 - Enables the SAI Rx interrupt requests.*
- static void [SAI_TxDisableInterrupts](#) (I2S_Type *base, uint32_t mask)
 - Disables the SAI Tx interrupt requests.*
- static void [SAI_RxDisableInterrupts](#) (I2S_Type *base, uint32_t mask)
 - Disables the SAI Rx interrupt requests.*

DMA Control

- static void [SAI_TxEnableDMA](#) (I2S_Type *base, uint32_t mask, bool enable)
 - Enables/disables the SAI Tx DMA requests.*
- static void [SAI_RxEnableDMA](#) (I2S_Type *base, uint32_t mask, bool enable)
 - Enables/disables the SAI Rx DMA requests.*
- static uintptr_t [SAI_TxGetDataRegisterAddress](#) (I2S_Type *base, uint32_t channel)
 - Gets the SAI Tx data register address.*
- static uintptr_t [SAI_RxGetDataRegisterAddress](#) (I2S_Type *base, uint32_t channel)
 - Gets the SAI Rx data register address.*

Bus Operations

- void [SAI_TxSetFormat](#) (I2S_Type *base, sai_transfer_format_t *format, uint32_t mclkSourceClockHz, uint32_t bclkSourceClockHz)
 - Configures the SAI Tx audio format.*
- void [SAI_RxSetFormat](#) (I2S_Type *base, sai_transfer_format_t *format, uint32_t mclkSourceClockHz, uint32_t bclkSourceClockHz)
 - Configures the SAI Rx audio format.*

- void **SAI_WriteBlocking** (I2S_Type *base, uint32_t channel, uint32_t bitWidth, uint8_t *buffer, uint32_t size)

Sends data using a blocking method.
- void **SAI_WriteMultiChannelBlocking** (I2S_Type *base, uint32_t channel, uint32_t channelMask, uint32_t bitWidth, uint8_t *buffer, uint32_t size)

Sends data to multi channel using a blocking method.
- static void **SAI_WriteData** (I2S_Type *base, uint32_t channel, uint32_t data)

Writes data into SAI FIFO.
- void **SAI_ReadBlocking** (I2S_Type *base, uint32_t channel, uint32_t bitWidth, uint8_t *buffer, uint32_t size)

Receives data using a blocking method.
- void **SAI_ReadMultiChannelBlocking** (I2S_Type *base, uint32_t channel, uint32_t channelMask, uint32_t bitWidth, uint8_t *buffer, uint32_t size)

Receives multi channel data using a blocking method.
- static uint32_t **SAI_ReadData** (I2S_Type *base, uint32_t channel)

Reads data from the SAI FIFO.

Transactional

- void **SAI_TransferTxCreateHandle** (I2S_Type *base, sai_handle_t *handle, **sai_transfer_callback_t** callback, void *userData)

Initializes the SAI Tx handle.
- void **SAI_TransferRxCreateHandle** (I2S_Type *base, sai_handle_t *handle, **sai_transfer_callback_t** callback, void *userData)

Initializes the SAI Rx handle.
- void **SAI_TransferTxSetConfig** (I2S_Type *base, sai_handle_t *handle, **sai_transceiver_t** *config)

SAI transmitter transfer configurations.
- void **SAI_TransferRxSetConfig** (I2S_Type *base, sai_handle_t *handle, **sai_transceiver_t** *config)

SAI receiver transfer configurations.
- **status_t SAI_TransferTxSetFormat** (I2S_Type *base, sai_handle_t *handle, **sai_transfer_format_t** *format, uint32_t mclkSourceClockHz, uint32_t bclkSourceClockHz)

Configures the SAI Tx audio format.
- **status_t SAI_TransferRxSetFormat** (I2S_Type *base, sai_handle_t *handle, **sai_transfer_format_t** *format, uint32_t mclkSourceClockHz, uint32_t bclkSourceClockHz)

Configures the SAI Rx audio format.
- **status_t SAI_TransferSendNonBlocking** (I2S_Type *base, sai_handle_t *handle, **sai_transfer_t** *xfer)

Performs an interrupt non-blocking send transfer on SAI.
- **status_t SAI_TransferReceiveNonBlocking** (I2S_Type *base, sai_handle_t *handle, **sai_transfer_t** *xfer)

Performs an interrupt non-blocking receive transfer on SAI.
- **status_t SAI_TransferGetSendCount** (I2S_Type *base, sai_handle_t *handle, size_t *count)

Gets a set byte count.
- **status_t SAI_TransferGetReceiveCount** (I2S_Type *base, sai_handle_t *handle, size_t *count)

Gets a received byte count.
- void **SAI_TransferAbortSend** (I2S_Type *base, sai_handle_t *handle)

Aborts the current send.
- void **SAI_TransferAbortReceive** (I2S_Type *base, sai_handle_t *handle)

- Aborts the current IRQ receive.
• void [SAI_TransferTerminateSend](#) (I2S_Type *base, sai_handle_t *handle)
 Terminate all SAI send.
- void [SAI_TransferTerminateReceive](#) (I2S_Type *base, sai_handle_t *handle)
 Terminate all SAI receive.
- void [SAI_TransferTxHandleIRQ](#) (I2S_Type *base, sai_handle_t *handle)
 Tx interrupt handler.
- void [SAI_TransferRxHandleIRQ](#) (I2S_Type *base, sai_handle_t *handle)
 Tx interrupt handler.

33.4.2 Data Structure Documentation

33.4.2.1 struct sai_config_t

Data Fields

- sai_protocol_t protocol
 Audio bus protocol in SAI.
- sai_sync_mode_t syncMode
 SAI sync mode, control Tx/Rx clock sync.
- sai_bclk_source_t bclkSource
 Bit Clock source.
- sai_master_slave_t masterSlave
 Master or slave.

33.4.2.2 struct sai_transfer_format_t

Data Fields

- uint32_t sampleRate_Hz
 Sample rate of audio data.
- uint32_t bitWidth
 Data length of audio data, usually 8/16/24/32 bits.
- sai_mono_stereo_t stereo
 Mono or stereo.
- uint8_t watermark
 Watermark value.
- uint8_t channel
 Transfer start channel.
- uint8_t channelMask
 enabled channel mask value, reference _sai_channel_mask
- uint8_t endChannel
 end channel number
- uint8_t channelNums
 Total enabled channel numbers.
- sai_protocol_t protocol
 Which audio protocol used.
- bool isFrameSyncCompact

True means Frame sync length is configurable according to bitWidth, false means frame sync length is 64 times of bit clock.

Field Documentation

(1) `bool sai_transfer_format_t::isFrameSyncCompact`

33.4.2.3 `struct sai_fifo_t`

Data Fields

- `bool fifoContinueOneError`
fifo continues when error occur
- `sai_fifo_combine_t fifoCombine`
fifo combine mode
- `sai_fifo_packing_t fifoPacking`
fifo packing mode
- `uint8_t fifoWatermark`
fifo watermark

33.4.2.4 `struct sai_bit_clock_t`

Data Fields

- `bool bclkSrcSwap`
bit clock source swap
- `bool bclkInputDelay`
bit clock actually used by the transmitter is delayed by the pad output delay, this has effect of decreasing the data input setup time, but increasing the data output valid time .
- `sai_clock_polarity_t bclkPolarity`
bit clock polarity
- `sai_bclk_source_t bclkSource`
bit Clock source

Field Documentation

(1) `bool sai_bit_clock_t::bclkInputDelay`

33.4.2.5 `struct sai_frame_sync_t`

Data Fields

- `uint8_t frameSyncWidth`
frame sync width in number of bit clocks
- `bool frameSyncEarly`
TRUE is frame sync assert one bit before the first bit of frame FALSE is frame sync assert with the first bit of the frame.
- `sai_clock_polarity_t frameSyncPolarity`
frame sync polarity

33.4.2.6 struct sai_serial_data_t

Data Fields

- **sai_data_pin_state_t dataMode**
sai data pin state when slots masked or channel disabled
- **sai_data_order_t dataOrder**
configure whether the LSB or MSB is transmitted first
- **uint8_t dataWord0Length**
configure the number of bits in the first word in each frame
- **uint8_t dataWordNLength**
configure the number of bits in the each word in each frame, except the first word
- **uint8_t dataWordLength**
used to record the data length for dma transfer
- **uint8_t dataFirstBitShifted**
Configure the bit index for the first bit transmitted for each word in the frame.
- **uint8_t dataWordNum**
configure the number of words in each frame
- **uint32_t dataMaskedWord**
configure whether the transmit word is masked

33.4.2.7 struct sai_transceiver_t

Data Fields

- **sai_serial_data_t serialData**
serial data configurations
- **sai_frame_sync_t frameSync**
ws configurations
- **sai_bit_clock_t bitClock**
bit clock configurations
- **sai_fifo_t fifo**
fifo configurations
- **sai_master_slave_t masterSlave**
transceiver is master or slave
- **sai_sync_mode_t syncMode**
transceiver sync mode
- **uint8_t startChannel**
Transfer start channel.
- **uint8_t channelMask**
enabled channel mask value, reference _sai_channel_mask
- **uint8_t endChannel**
end channel number
- **uint8_t channelNums**
Total enabled channel numbers.

33.4.2.8 struct sai_transfer_t

Data Fields

- `uint8_t * data`
Data start address to transfer.
- `size_t dataSize`
Transfer size.

Field Documentation

- (1) `uint8_t* sai_transfer_t::data`
- (2) `size_t sai_transfer_t::dataSize`

33.4.2.9 struct _sai_handle

Data Fields

- `I2S_Type * base`
base address
- `uint32_t state`
Transfer status.
- `sai_transfer_callback_t callback`
Callback function called at transfer event.
- `void * userData`
Callback parameter passed to callback function.
- `uint8_t bitWidth`
Bit width for transfer, 8/16/24/32 bits.
- `uint8_t channel`
Transfer start channel.
- `uint8_t channelMask`
enabled channel mask value, refernece _sai_channel_mask
- `uint8_t endChannel`
end channel number
- `uint8_t channelNums`
Total enabled channel numbers.
- `sai_transfer_t saiQueue [SAI_XFER_QUEUE_SIZE]`
Transfer queue storing queued transfer.
- `size_t transferSize [SAI_XFER_QUEUE_SIZE]`
Data bytes need to transfer.
- `volatile uint8_t queueUser`
Index for user to queue transfer.
- `volatile uint8_t queueDriver`
Index for driver to get the transfer data and size.
- `uint8_t watermark`
Watermark value.

33.4.3 Macro Definition Documentation

33.4.3.1 #define SAI_XFER_QUEUE_SIZE (4U)

33.4.4 Enumeration Type Documentation

33.4.4.1 anonymous enum

Enumerator

- kStatus_SAI_TxBusy*** SAI Tx is busy.
- kStatus_SAI_RxBusy*** SAI Rx is busy.
- kStatus_SAI_TxError*** SAI Tx FIFO error.
- kStatus_SAI_RxError*** SAI Rx FIFO error.
- kStatus_SAI_QueueFull*** SAI transfer queue is full.
- kStatus_SAI_TxIdle*** SAI Tx is idle.
- kStatus_SAI_RxIdle*** SAI Rx is idle.

33.4.4.2 anonymous enum

Enumerator

- kSAI_Channel0Mask*** channel 0 mask value
- kSAI_Channel1Mask*** channel 1 mask value
- kSAI_Channel2Mask*** channel 2 mask value
- kSAI_Channel3Mask*** channel 3 mask value
- kSAI_Channel4Mask*** channel 4 mask value
- kSAI_Channel5Mask*** channel 5 mask value
- kSAI_Channel6Mask*** channel 6 mask value
- kSAI_Channel7Mask*** channel 7 mask value

33.4.4.3 enum sai_protocol_t

Enumerator

- kSAI_BusLeftJustified*** Uses left justified format.
- kSAI_BusRightJustified*** Uses right justified format.
- kSAI_BusI2S*** Uses I2S format.
- kSAI_BusPCMA*** Uses I2S PCM A format.
- kSAI_BusPCMB*** Uses I2S PCM B format.

33.4.4.4 enum sai_master_slave_t

Enumerator

- kSAI_Master*** Master mode include bclk and frame sync.

kSAI_Slave Slave mode include bclk and frame sync.

kSAI_Bclk_Master_FrameSync_Slave bclk in master mode, frame sync in slave mode

kSAI_Bclk_Slave_FrameSync_Master bclk in slave mode, frame sync in master mode

33.4.4.5 enum sai_mono_stereo_t

Enumerator

kSAI_Stereo Stereo sound.

kSAI_MonoRight Only Right channel have sound.

kSAI_MonoLeft Only left channel have sound.

33.4.4.6 enum sai_data_order_t

Enumerator

kSAI_DataLSB LSB bit transferred first.

kSAI_DataMSB MSB bit transferred first.

33.4.4.7 enum sai_clock_polarity_t

Enumerator

kSAI_PolarityActiveHigh Drive outputs on rising edge.

kSAI_PolarityActiveLow Drive outputs on falling edge.

kSAI_SampleOnFallingEdge Sample inputs on falling edge.

kSAI_SampleOnRisingEdge Sample inputs on rising edge.

33.4.4.8 enum sai_sync_mode_t

Enumerator

kSAI_ModeAsync Asynchronous mode.

kSAI_ModeSync Synchronous mode (with receiver or transmit)

33.4.4.9 enum sai_bclk_source_t

Enumerator

kSAI_BclkSourceBusclk Bit clock using bus clock.

kSAI_BclkSourceMclkOption1 Bit clock MCLK option 1.

kSAI_BclkSourceMclkOption2 Bit clock MCLK option2.
kSAI_BclkSourceMclkOption3 Bit clock MCLK option3.
kSAI_BclkSourceMclkDiv Bit clock using master clock divider.
kSAI_BclkSourceOtherSai0 Bit clock from other SAI device.
kSAI_BclkSourceOtherSai1 Bit clock from other SAI device.

33.4.4.10 anonymous enum

Enumerator

kSAI_WordStartInterruptEnable Word start flag, means the first word in a frame detected.
kSAI_SyncErrorInterruptEnable Sync error flag, means the sync error is detected.
kSAI_FIFOWarningInterruptEnable FIFO warning flag, means the FIFO is empty.
kSAI_FIFOErrorInterruptEnable FIFO error flag.
kSAI_FIFORequestInterruptEnable FIFO request, means reached watermark.

33.4.4.11 anonymous enum

Enumerator

kSAI_FIFOWarningDMAEnable FIFO warning caused by the DMA request.
kSAI_FIFORequestDMAEnable FIFO request caused by the DMA request.

33.4.4.12 anonymous enum

Enumerator

kSAI_WordStartFlag Word start flag, means the first word in a frame detected.
kSAI_SyncErrorFlag Sync error flag, means the sync error is detected.
kSAI_FIFOErrorFlag FIFO error flag.
kSAI_FIFORequestFlag FIFO request flag.
kSAI_FIFOWarningFlag FIFO warning flag.

33.4.4.13 enum sai_reset_type_t

Enumerator

kSAI_ResetTypeSoftware Software reset, reset the logic state.
kSAI_ResetTypeFIFO FIFO reset, reset the FIFO read and write pointer.
kSAI_ResetAll All reset.

33.4.4.14 enum sai_fifo_packing_t

Enumerator

kSAI_FifoPackingDisabled Packing disabled.

kSAI_FifoPacking8bit 8 bit packing enabled

kSAI_FifoPacking16bit 16bit packing enabled

33.4.4.15 enum sai_sample_rate_t

Enumerator

kSAI_SampleRate8KHz Sample rate 8000 Hz.

kSAI_SampleRate11025Hz Sample rate 11025 Hz.

kSAI_SampleRate12KHz Sample rate 12000 Hz.

kSAI_SampleRate16KHz Sample rate 16000 Hz.

kSAI_SampleRate22050Hz Sample rate 22050 Hz.

kSAI_SampleRate24KHz Sample rate 24000 Hz.

kSAI_SampleRate32KHz Sample rate 32000 Hz.

kSAI_SampleRate44100Hz Sample rate 44100 Hz.

kSAI_SampleRate48KHz Sample rate 48000 Hz.

kSAI_SampleRate96KHz Sample rate 96000 Hz.

kSAI_SampleRate192KHz Sample rate 192000 Hz.

kSAI_SampleRate384KHz Sample rate 384000 Hz.

33.4.4.16 enum sai_word_width_t

Enumerator

kSAI_WordWidth8bits Audio data width 8 bits.

kSAI_WordWidth16bits Audio data width 16 bits.

kSAI_WordWidth24bits Audio data width 24 bits.

kSAI_WordWidth32bits Audio data width 32 bits.

33.4.4.17 enum sai_data_pin_state_t

Enumerator

kSAI_DataPinStateTriState transmit data pins are tri-stated when slots are masked or channels are disabled

kSAI_DataPinStateOutputZero transmit data pins are never tri-stated and will output zero when slots are masked or channel disabled

33.4.4.18 enum sai_fifo_combine_t

Enumerator

kSAI_FifoCombineDisabled sai fifo combine mode disabled
kSAI_FifoCombineModeEnabledOnRead sai fifo combine mode enabled on FIFO reads
kSAI_FifoCombineModeEnabledOnWrite sai fifo combine mode enabled on FIFO write
kSAI_FifoCombineModeEnabledOnReadWrite sai fifo combined mode enabled on FIFO read/writes

33.4.4.19 enum sai_transceiver_type_t

Enumerator

kSAI_Transmitter sai transmitter
kSAI_Receiver sai receiver

33.4.4.20 enum sai_frame_sync_len_t

Enumerator

kSAI_FrameSyncLenOneBitClk 1 bit clock frame sync len for DSP mode
kSAI_FrameSyncLenPerWordWidth Frame sync length decided by word width.

33.4.5 Function Documentation

33.4.5.1 void SAI_TxInit (I2S_Type * *base*, const sai_config_t * *config*)

Deprecated Do not use this function. It has been superceded by [SAI_Init](#)

Ungates the SAI clock, resets the module, and configures SAI Tx with a configuration structure. The configuration structure can be custom filled or set with default values by [SAI_TxGetDefaultConfig\(\)](#).

Note

This API should be called at the beginning of the application to use the SAI driver. Otherwise, accessing the SAIM module can cause a hard fault because the clock is not enabled.

Parameters

<i>base</i>	SAI base pointer
<i>config</i>	SAI configuration structure.

33.4.5.2 void SAI_RxInit (I2S_Type * *base*, const sai_config_t * *config*)

Deprecated Do not use this function. It has been superceded by [SAI_Init](#)

Ungates the SAI clock, resets the module, and configures the SAI Rx with a configuration structure. The configuration structure can be custom filled or set with default values by [SAI_RxGetDefaultConfig\(\)](#).

Note

This API should be called at the beginning of the application to use the SAI driver. Otherwise, accessing the SAI module can cause a hard fault because the clock is not enabled.

Parameters

<i>base</i>	SAI base pointer
<i>config</i>	SAI configuration structure.

33.4.5.3 void SAI_TxGetDefaultConfig (sai_config_t * *config*)

Deprecated Do not use this function. It has been superceded by [SAI_GetClassicI2SConfig](#), [SAI_GetLeft-JustifiedConfig](#) , [SAI_GetRightJustifiedConfig](#), [SAI_GetDSPConfig](#), [SAI_GetTDMConfig](#)

This API initializes the configuration structure for use in [SAI_TxConfig\(\)](#). The initialized structure can remain unchanged in [SAI_TxConfig\(\)](#), or it can be modified before calling [SAI_TxConfig\(\)](#). This is an example.

```
sai_config_t config;
SAI_TxGetDefaultConfig(&config);
```

Parameters

<i>config</i>	pointer to master configuration structure
---------------	---

33.4.5.4 void SAI_RxGetDefaultConfig (sai_config_t * *config*)

Deprecated Do not use this function. It has been superceded by [SAI_GetClassicI2SConfig](#), [SAI_GetLeftJustifiedConfig](#), [SAI_GetRightJustifiedConfig](#), [SAI_GetDSPConfig](#), [SAI_GetTDMConfig](#)

This API initializes the configuration structure for use in SAI_RxConfig(). The initialized structure can remain unchanged in SAI_RxConfig() or it can be modified before calling SAI_RxConfig(). This is an example.

```
sai_config_t config;
SAI_RxGetDefaultConfig(&config);
```

Parameters

<i>config</i>	pointer to master configuration structure
---------------	---

33.4.5.5 void SAI_Init (I2S_Type * *base*)

This API gates the SAI clock. The SAI module can't operate unless SAI_Init is called to enable the clock.

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

33.4.5.6 void SAI_Deinit (I2S_Type * *base*)

This API gates the SAI clock. The SAI module can't operate unless SAI_TxInit or SAI_RxInit is called to enable the clock.

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

33.4.5.7 void SAI_TxReset (I2S_Type * *base*)

This function enables the software reset and FIFO reset of SAI Tx. After reset, clear the reset bit.

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

33.4.5.8 void SAI_RxReset (I2S_Type * *base*)

This function enables the software reset and FIFO reset of SAI Rx. After reset, clear the reset bit.

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

33.4.5.9 void SAI_TxEnable (I2S_Type * *base*, bool *enable*)

Parameters

<i>base</i>	SAI base pointer.
<i>enable</i>	True means enable SAI Tx, false means disable.

33.4.5.10 void SAI_RxEnable (I2S_Type * *base*, bool *enable*)

Parameters

<i>base</i>	SAI base pointer.
<i>enable</i>	True means enable SAI Rx, false means disable.

33.4.5.11 static void SAI_TxSetBitClockDirection (I2S_Type * *base*, sai_master_slave_t *masterSlave*) [inline], [static]

Select bit clock direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

<i>masterSlave</i>	reference sai_master_slave_t.
--------------------	-------------------------------

33.4.5.12 static void SAI_RxSetBitClockDirection (I2S_Type * *base*, sai_master_slave_t *masterSlave*) [inline], [static]

Select bit clock direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	reference sai_master_slave_t.

33.4.5.13 static void SAI_RxSetFrameSyncDirection (I2S_Type * *base*, sai_master_slave_t *masterSlave*) [inline], [static]

Select frame sync direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	reference sai_master_slave_t.

33.4.5.14 static void SAI_TxSetFrameSyncDirection (I2S_Type * *base*, sai_master_slave_t *masterSlave*) [inline], [static]

Select frame sync direction, master or slave.

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	reference sai_master_slave_t.

33.4.5.15 void SAI_TxSetBitClockRate (I2S_Type * *base*, uint32_t *sourceClockHz*, uint32_t *sampleRate*, uint32_t *bitWidth*, uint32_t *channelNumbers*)

Parameters

<i>base</i>	SAI base pointer.
<i>sourceClockHz</i>	Bit clock source frequency.
<i>sampleRate</i>	Audio data sample rate.
<i>bitWidth</i>	Audio data bitWidth.
<i>channel-Numbers</i>	Audio channel numbers.

33.4.5.16 void SAI_RxSetBitClockRate (I2S_Type * *base*, uint32_t *sourceClockHz*, uint32_t *sampleRate*, uint32_t *bitWidth*, uint32_t *channelNumbers*)

Parameters

<i>base</i>	SAI base pointer.
<i>sourceClockHz</i>	Bit clock source frequency.
<i>sampleRate</i>	Audio data sample rate.
<i>bitWidth</i>	Audio data bitWidth.
<i>channel-Numbers</i>	Audio channel numbers.

33.4.5.17 void SAI_TxSetBitclockConfig (I2S_Type * *base*, sai_master_slave_t *masterSlave*, sai_bit_clock_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	bit clock other configurations, can be NULL in slave mode.

33.4.5.18 void SAI_RxSetBitclockConfig (I2S_Type * *base*, sai_master_slave_t *masterSlave*, sai_bit_clock_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	bit clock other configurations, can be NULL in slave mode.

33.4.5.19 void SAI_TxSetFifoConfig (I2S_Type * *base*, sai_fifo_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	fifo configurations.

33.4.5.20 void SAI_RxSetFifoConfig (I2S_Type * *base*, sai_fifo_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	fifo configurations.

33.4.5.21 void SAI_TxSetFrameSyncConfig (I2S_Type * *base*, sai_master_slave_t *masterSlave*, sai_frame_sync_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	frame sync configurations, can be NULL in slave mode.

33.4.5.22 void SAI_RxSetFrameSyncConfig (I2S_Type * *base*, sai_master_slave_t *masterSlave*, sai_frame_sync_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>masterSlave</i>	master or slave.
<i>config</i>	frame sync configurations, can be NULL in slave mode.

33.4.5.23 void SAI_TxSetSerialDataConfig (I2S_Type * *base*, sai_serial_data_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	serial data configurations.

33.4.5.24 void SAI_RxSetSerialDataConfig (I2S_Type * *base*, sai_serial_data_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	serial data configurations.

33.4.5.25 void SAI_TxSetConfig (I2S_Type * *base*, sai_transceiver_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
<i>config</i>	transmitter configurations.

33.4.5.26 void SAI_RxSetConfig (I2S_Type * *base*, sai_transceiver_t * *config*)

Parameters

<i>base</i>	SAI base pointer.
-------------	-------------------

<i>config</i>	receiver configurations.
---------------	--------------------------

33.4.5.27 void SAI_GetClassicI2SConfig (*sai_transceiver_t * config*, *sai_word_width_t bitWidth*, *sai_mono_stereo_t mode*, *uint32_t saiChannelMask*)

Parameters

<i>config</i>	transceiver configurations.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

33.4.5.28 void SAI_GetLeftJustifiedConfig (*sai_transceiver_t * config*, *sai_word_width_t bitWidth*, *sai_mono_stereo_t mode*, *uint32_t saiChannelMask*)

Parameters

<i>config</i>	transceiver configurations.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

33.4.5.29 void SAI_GetRightJustifiedConfig (*sai_transceiver_t * config*, *sai_word_width_t bitWidth*, *sai_mono_stereo_t mode*, *uint32_t saiChannelMask*)

Parameters

<i>config</i>	transceiver configurations.
<i>bitWidth</i>	audio data bitWidth.

<i>mode</i>	audio data channel.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

33.4.5.30 void SAI_GetTDMConfig (sai_transceiver_t * *config*, sai_frame_sync_len_t *frameSyncWidth*, sai_word_width_t *bitWidth*, uint32_t *dataWordNum*, uint32_t *saiChannelMask*)

Parameters

<i>config</i>	transceiver configurations.
<i>frameSync-Width</i>	length of frame sync.
<i>bitWidth</i>	audio data word width.
<i>dataWordNum</i>	word number in one frame.
<i>saiChannel-Mask</i>	mask value of the channel to be enable.

33.4.5.31 void SAI_GetDSPConfig (sai_transceiver_t * *config*, sai_frame_sync_len_t *frameSyncWidth*, sai_word_width_t *bitWidth*, sai_mono_stereo_t *mode*, uint32_t *saiChannelMask*)

Note

DSP mode is also called PCM mode which support MODE A and MODE B, DSP/PCM MODE A configuration flow. RX is similiar but uses SAI_RxSetConfig instead of SAI_TxSetConfig:

```
* SAI_GetDSPConfig(config, kSAI_FrameSyncLenOneBitClk, bitWidth,
                   kSAI_Stereo, channelMask)
* config->frameSync.frameSyncEarly = true;
* SAI_TxSetConfig(base, config)
*
```

DSP/PCM MODE B configuration flow for TX. RX is similiar but uses SAI_RxSetConfig instead of SAI_TxSetConfig:

```
* SAI_GetDSPConfig(config, kSAI_FrameSyncLenOneBitClk, bitWidth,
                   kSAI_Stereo, channelMask)
* SAI_TxSetConfig(base, config)
*
```

Parameters

<i>config</i>	transceiver configurations.
<i>frameSyncWidth</i>	length of frame sync.
<i>bitWidth</i>	audio data bitWidth.
<i>mode</i>	audio data channel.
<i>saiChannelMask</i>	mask value of the channel to enable.

33.4.5.32 static uint32_t SAI_TxGetStatusFlag (I2S_Type * *base*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

Returns

SAI Tx status flag value. Use the Status Mask to get the status value needed.

33.4.5.33 static void SAI_TxClearStatusFlags (I2S_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	State mask. It can be a combination of the following source if defined: <ul style="list-style-type: none"> • kSAI_WordStartFlag • kSAI_SyncErrorFlag • kSAI_FIFOErrorFlag

33.4.5.34 static uint32_t SAI_RxGetStatusFlag (I2S_Type * *base*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

Returns

SAI Rx status flag value. Use the Status Mask to get the status value needed.

33.4.5.35 static void SAI_RxClearStatusFlags (I2S_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>State mask. It can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> • kSAI_WordStartFlag • kSAI_SyncErrorFlag • kSAI_FIFOErrorFlag

33.4.5.36 void SAI_TxSoftwareReset (I2S_Type * *base*, sai_reset_type_t *type*)

FIFO reset means clear all the data in the FIFO, and make the FIFO pointer both to 0. Software reset means clear the Tx internal logic, including the bit clock, frame count etc. But software reset will not clear any configuration registers like TCR1~TCR5. This function will also clear all the error flags such as FIFO error, sync error etc.

Parameters

<i>base</i>	SAI base pointer
<i>type</i>	Reset type, FIFO reset or software reset

33.4.5.37 void SAI_RxSoftwareReset (I2S_Type * *base*, sai_reset_type_t *type*)

FIFO reset means clear all the data in the FIFO, and make the FIFO pointer both to 0. Software reset means clear the Rx internal logic, including the bit clock, frame count etc. But software reset will not clear any configuration registers like RCR1~RCR5. This function will also clear all the error flags such as FIFO error, sync error etc.

Parameters

<i>base</i>	SAI base pointer
<i>type</i>	Reset type, FIFO reset or software reset

33.4.5.38 void SAI_TxSetChannelFIFOMask (I2S_Type * *base*, uint8_t *mask*)

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	Channel enable mask, 0 means all channel FIFO disabled, 1 means channel 0 enabled, 3 means both channel 0 and channel 1 enabled.

33.4.5.39 void SAI_RxSetChannelFIFOMask (I2S_Type * *base*, uint8_t *mask*)

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	Channel enable mask, 0 means all channel FIFO disabled, 1 means channel 0 enabled, 3 means both channel 0 and channel 1 enabled.

33.4.5.40 void SAI_TxSetDataOrder (I2S_Type * *base*, sai_data_order_t *order*)

Parameters

<i>base</i>	SAI base pointer
<i>order</i>	Data order MSB or LSB

33.4.5.41 void SAI_RxSetDataOrder (I2S_Type * *base*, sai_data_order_t *order*)

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

<i>order</i>	Data order MSB or LSB
--------------	-----------------------

33.4.5.42 void SAI_TxSetBitClockPolarity (I2S_Type * *base*, sai_clock_polarity_t *polarity*)

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

33.4.5.43 void SAI_RxSetBitClockPolarity (I2S_Type * *base*, sai_clock_polarity_t *polarity*)

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

33.4.5.44 void SAI_TxSetFrameSyncPolarity (I2S_Type * *base*, sai_clock_polarity_t *polarity*)

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

33.4.5.45 void SAI_RxSetFrameSyncPolarity (I2S_Type * *base*, sai_clock_polarity_t *polarity*)

Parameters

<i>base</i>	SAI base pointer
<i>polarity</i>	

33.4.5.46 void SAI_TxSetFIFOPacking (I2S_Type * *base*, sai_fifo_packing_t *pack*)

Parameters

<i>base</i>	SAI base pointer.
<i>pack</i>	FIFO pack type. It is element of sai_fifo_packing_t.

33.4.5.47 void SAI_RxSetFIFOPacking (I2S_Type * *base*, sai_fifo_packing_t *pack*)

Parameters

<i>base</i>	SAI base pointer.
<i>pack</i>	FIFO pack type. It is element of sai_fifo_packing_t.

33.4.5.48 static void SAI_TxSetFIFOErrorContinue (I2S_Type * *base*, bool *isEnabled*) [inline], [static]

FIFO error continue mode means SAI will keep running while FIFO error occurred. If this feature not enabled, SAI will hang and users need to clear FEF flag in TCSR register.

Parameters

<i>base</i>	SAI base pointer.
<i>isEnabled</i>	Is FIFO error continue enabled, true means enable, false means disable.

33.4.5.49 static void SAI_RxSetFIFOErrorContinue (I2S_Type * *base*, bool *isEnabled*) [inline], [static]

FIFO error continue mode means SAI will keep running while FIFO error occurred. If this feature not enabled, SAI will hang and users need to clear FEF flag in RCSR register.

Parameters

<i>base</i>	SAI base pointer.
<i>isEnabled</i>	Is FIFO error continue enabled, true means enable, false means disable.

33.4.5.50 static void SAI_TxEnableInterrupts (I2S_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> • kSAI_WordStartInterruptEnable • kSAI_SyncErrorInterruptEnable • kSAI_FIFOWarningInterruptEnable • kSAI_FIFORequestInterruptEnable • kSAI_FIFOErrorInterruptEnable

33.4.5.51 static void SAI_RxEnableInterrupts (I2S_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> • kSAI_WordStartInterruptEnable • kSAI_SyncErrorInterruptEnable • kSAI_FIFOWarningInterruptEnable • kSAI_FIFORequestInterruptEnable • kSAI_FIFOErrorInterruptEnable

33.4.5.52 static void SAI_TxDisableInterrupts (I2S_Type * *base*, uint32_t *mask*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> • kSAI_WordStartInterruptEnable • kSAI_SyncErrorInterruptEnable • kSAI_FIFOWarningInterruptEnable • kSAI_FIFORequestInterruptEnable • kSAI_FIFOErrorInterruptEnable

**33.4.5.53 static void SAI_RxDisableInterrupts (I2S_Type * *base*, uint32_t *mask*)
[inline], [static]**

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>interrupt source The parameter can be a combination of the following sources if defined.</p> <ul style="list-style-type: none"> • kSAI_WordStartInterruptEnable • kSAI_SyncErrorInterruptEnable • kSAI_FIFOWarningInterruptEnable • kSAI_FIFORequestInterruptEnable • kSAI_FIFOErrorInterruptEnable

**33.4.5.54 static void SAI_TxEnableDMA (I2S_Type * *base*, uint32_t *mask*, bool *enable*)
[inline], [static]**

Parameters

<i>base</i>	SAI base pointer
<i>mask</i>	<p>DMA source The parameter can be combination of the following sources if defined.</p> <ul style="list-style-type: none"> • kSAI_FIFOWarningDMAEnable • kSAI_FIFORequestDMAEnable
<i>enable</i>	True means enable DMA, false means disable DMA.

**33.4.5.55 static void SAI_RxEnableDMA (I2S_Type * *base*, uint32_t *mask*, bool *enable*)
[inline], [static]**

Parameters

<i>base</i>	SAI base pointer
-------------	------------------

<i>mask</i>	DMA source The parameter can be a combination of the following sources if defined. <ul style="list-style-type: none"> • kSAI_FIFOWarningDMAEnable • kSAI_FIFORequestDMAEnable
<i>enable</i>	True means enable DMA, false means disable DMA.

33.4.5.56 static uintptr_t SAI_TxGetDataRegisterAddress (I2S_Type * *base*, uint32_t *channel*) [inline], [static]

This API is used to provide a transfer address for the SAI DMA transfer configuration.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Which data channel used.

Returns

data register address.

33.4.5.57 static uintptr_t SAI_RxGetDataRegisterAddress (I2S_Type * *base*, uint32_t *channel*) [inline], [static]

This API is used to provide a transfer address for the SAI DMA transfer configuration.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Which data channel used.

Returns

data register address.

33.4.5.58 void SAI_TxSetFormat (I2S_Type * *base*, sai_transfer_format_t * *format*, uint32_t *mclkSourceClockHz*, uint32_t *bclkSourceClockHz*)

Deprecated Do not use this function. It has been superceded by [SAI_TxSetConfig](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	SAI base pointer.
<i>format</i>	Pointer to the SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If the bit clock source is a master clock, this value should equal the masterClockHz.

33.4.5.59 void SAI_RxSetFormat (I2S_Type * *base*, sai_transfer_format_t * *format*, uint32_t *mclkSourceClockHz*, uint32_t *bclkSourceClockHz*)

Deprecated Do not use this function. It has been superceded by [SAI_RxSetConfig](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	SAI base pointer.
<i>format</i>	Pointer to the SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If the bit clock source is a master clock, this value should equal the masterClockHz.

33.4.5.60 void SAI_WriteBlocking (I2S_Type * *base*, uint32_t *channel*, uint32_t *bitWidth*, uint8_t * *buffer*, uint32_t *size*)

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be written.
<i>size</i>	Bytes to be written.

33.4.5.61 void SAI_WriteMultiChannelBlocking (I2S_Type * *base*, uint32_t *channel*, uint32_t *channelMask*, uint32_t *bitWidth*, uint8_t * *buffer*, uint32_t *size*)

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>channelMask</i>	channel mask.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be written.
<i>size</i>	Bytes to be written.

33.4.5.62 static void SAI_WriteData (I2S_Type * *base*, uint32_t *channel*, uint32_t *data*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>data</i>	Data needs to be written.

33.4.5.63 void SAI_ReadBlocking (I2S_Type * *base*, uint32_t *channel*, uint32_t *bitWidth*, uint8_t * *buffer*, uint32_t *size*)

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be read.
<i>size</i>	Bytes to be read.

33.4.5.64 void SAI_ReadMultiChannelBlocking (I2S_Type * *base*, uint32_t *channel*, uint32_t *channelMask*, uint32_t *bitWidth*, uint8_t * *buffer*, uint32_t *size*)

Note

This function blocks by polling until data is ready to be sent.

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.
<i>channelMask</i>	channel mask.
<i>bitWidth</i>	How many bits in an audio word; usually 8/16/24/32 bits.
<i>buffer</i>	Pointer to the data to be read.
<i>size</i>	Bytes to be read.

33.4.5.65 static uint32_t SAI_ReadData (I2S_Type * *base*, uint32_t *channel*) [inline], [static]

Parameters

<i>base</i>	SAI base pointer.
<i>channel</i>	Data channel used.

Returns

Data in SAI FIFO.

**33.4.5.66 void SAI_TransferTxCreateHandle (I2S_Type * *base*, sai_handle_t * *handle*,
sai_transfer_callback_t *callback*, void * *userData*)**

This function initializes the Tx handle for the SAI Tx transactional APIs. Call this function once to get the handle initialized.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI handle pointer.
<i>callback</i>	Pointer to the user callback function.
<i>userData</i>	User parameter passed to the callback function

33.4.5.67 void SAI_TransferRxCreateHandle (I2S_Type * *base*, sai_handle_t * *handle*, sai_transfer_callback_t *callback*, void * *userData*)

This function initializes the Rx handle for the SAI Rx transactional APIs. Call this function once to get the handle initialized.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>callback</i>	Pointer to the user callback function.
<i>userData</i>	User parameter passed to the callback function.

33.4.5.68 void SAI_TransferTxSetConfig (I2S_Type * *base*, sai_handle_t * *handle*, sai_transceiver_t * *config*)

This function initializes the Tx, include bit clock, frame sync, master clock, serial data and fifo configurations.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>config</i>	transmitter configurations.

33.4.5.69 void SAI_TransferRxSetConfig (I2S_Type * *base*, sai_handle_t * *handle*, sai_transceiver_t * *config*)

This function initializes the Rx, include bit clock, frame sync, master clock, serial data and fifo configurations.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>config</i>	receiver configurations.

33.4.5.70 status_t SAI_TransferTxSetFormat (I2S_Type * *base*, sai_handle_t * *handle*, sai_transfer_format_t * *format*, uint32_t *mclkSourceClockHz*, uint32_t *bclkSourceClockHz*)

Deprecated Do not use this function. It has been superceded by [SAI_TransferTxSetConfig](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>format</i>	Pointer to the SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If a bit clock source is a master clock, this value should equal the <i>masterClockHz</i> in <i>format</i> .

Returns

Status of this function. Return value is the *status_t*.

33.4.5.71 status_t SAI_TransferRxSetFormat (I2S_Type * *base*, sai_handle_t * *handle*, sai_transfer_format_t * *format*, uint32_t *mclkSourceClockHz*, uint32_t *bclkSourceClockHz*)

Deprecated Do not use this function. It has been superceded by [SAI_TransferRxSetConfig](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI handle pointer.
<i>format</i>	Pointer to the SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If a bit clock source is a master clock, this value should equal the masterClockHz in format.

Returns

Status of this function. Return value is one of status_t.

33.4.5.72 status_t SAI_TransferSendNonBlocking (I2S_Type * *base*, sai_handle_t * *handle*, sai_transfer_t * *xfer*)

Note

This API returns immediately after the transfer initiates. Call the SAI_TxGetTransferStatusIRQ to poll the transfer status and check whether the transfer is finished. If the return status is not kStatus_SAI_Busy, the transfer is finished.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>xfer</i>	Pointer to the sai_transfer_t structure.

Return values

<i>kStatus_Success</i>	Successfully started the data receive.
<i>kStatus_SAI_TxBusy</i>	Previous receive still not finished.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

33.4.5.73 status_t SAI_TransferReceiveNonBlocking (I2S_Type * *base*, sai_handle_t * *handle*, sai_transfer_t * *xfer*)

Note

This API returns immediately after the transfer initiates. Call the SAI_RxGetTransferStatusIRQ to poll the transfer status and check whether the transfer is finished. If the return status is not kStatus__SAI_Busy, the transfer is finished.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>xfer</i>	Pointer to the sai_transfer_t structure.

Return values

<i>kStatus_Success</i>	Successfully started the data receive.
<i>kStatus_SAI_RxBusy</i>	Previous receive still not finished.
<i>kStatus_InvalidArgument</i>	The input parameter is invalid.

33.4.5.74 status_t SAI_TransferGetSendCount (I2S_Type * *base*, sai_handle_t * *handle*, size_t * *count*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>count</i>	Bytes count sent.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.

33.4.5.75 status_t SAI_TransferGetReceiveCount (I2S_Type * *base*, sai_handle_t * *handle*, size_t * *count*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.
<i>count</i>	Bytes count received.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.

33.4.5.76 void SAI_TransferAbortSend (I2S_Type * *base*, sai_handle_t * *handle*)

Note

This API can be called any time when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.

33.4.5.77 void SAI_TransferAbortReceive (I2S_Type * *base*, sai_handle_t * *handle*)

Note

This API can be called when an interrupt non-blocking transfer initiates to abort the transfer early.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	Pointer to the sai_handle_t structure which stores the transfer state.

33.4.5.78 void SAI_TransferTerminateSend (I2S_Type * *base*, sai_handle_t * *handle*)

This function will clear all transfer slots buffered in the sai queue. If users only want to abort the current transfer slot, please call SAI_TransferAbortSend.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

33.4.5.79 void SAI_TransferTerminateReceive (I2S_Type * *base*, sai_handle_t * *handle*)

This function will clear all transfer slots buffered in the sai queue. If users only want to abort the current transfer slot, please call SAI_TransferAbortReceive.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

33.4.5.80 void SAI_TransferTxHandleIRQ (I2S_Type * *base*, sai_handle_t * *handle*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure.

33.4.5.81 void SAI_TransferRxHandleIRQ (I2S_Type * *base*, sai_handle_t * *handle*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	Pointer to the sai_handle_t structure.

Chapter 34

SEMA42: Hardware Semaphores Driver

34.1 Overview

The MCUXpresso SDK provides a driver for the SEMA42 module of MCUXpresso SDK devices.

The SEMA42 driver is used for multicore platforms. Before using the SEMA42, call the [SEMA42_Init\(\)](#) function to initialize the module. Note that this function only enables the clock but does not reset the gates because the module might be used by other processors at the same time. To reset the gates, call either the [SEMA42_ResetGate\(\)](#) or [SEMA42_ResetAllGates\(\)](#) functions. The function [SEMA42_Deinit\(\)](#) deinitializes the SEMA42.

The SEMA42 provides two functions to lock the SEMA42 gate. The function [SEMA42_TryLock\(\)](#) tries to lock the gate. If the gate has been locked by another processor, this function returns an error immediately. The function [SEMA42_Lock\(\)](#) is a blocking method, which waits until the gate is free and locks it.

The [SEMA42_Unlock\(\)](#) unlocks the SEMA42 gate. The gate can only be unlocked by the processor which locked it. If the gate is not locked by the current processor, this function takes no effect. The function [SEMA42_GetGateStatus\(\)](#) returns a status whether the gate is unlocked and which processor locks the gate.

The SEMA42 gate can be reset to unlock forcefully. The function [SEMA42_ResetGate\(\)](#) resets a specific gate. The function [SEMA42_ResetAllGates\(\)](#) resets all gates.

34.2 Typical use case

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/sema42

Macros

- #define [SEMA42_GATE_NUM_RESET_ALL](#) (64U)
The number to reset all SEMA42 gates.
- #define [SEMA42_GATEn](#)(base, n) (((volatile uint8_t *)(&((base)->GATE3)))[(n) ^ 3U])
SEMA42 gate n register address.

Enumerations

- enum {
 [kStatus_SEMA42_Busy](#) = MAKE_STATUS(kStatusGroup_SEMA42, 0),
 [kStatus_SEMA42_Reseting](#) = MAKE_STATUS(kStatusGroup_SEMA42, 1) }
SEMA42 status return codes.
- enum [sema42_gate_status_t](#) {

```

kSEMA42_Unlocked = 0U,
kSEMA42_LockedByProc0 = 1U,
kSEMA42_LockedByProc1 = 2U,
kSEMA42_LockedByProc2 = 3U,
kSEMA42_LockedByProc3 = 4U,
kSEMA42_LockedByProc4 = 5U,
kSEMA42_LockedByProc5 = 6U,
kSEMA42_LockedByProc6 = 7U,
kSEMA42_LockedByProc7 = 8U,
kSEMA42_LockedByProc8 = 9U,
kSEMA42_LockedByProc9 = 10U,
kSEMA42_LockedByProc10 = 11U,
kSEMA42_LockedByProc11 = 12U,
kSEMA42_LockedByProc12 = 13U,
kSEMA42_LockedByProc13 = 14U,
kSEMA42_LockedByProc14 = 15U }

```

SEMA42 gate lock status.

Functions

- void [SEMA42_Init](#) (SEMA42_Type *base)
Initializes the SEMA42 module.
- void [SEMA42_Deinit](#) (SEMA42_Type *base)
De-initializes the SEMA42 module.
- [status_t SEMA42_TryLock](#) (SEMA42_Type *base, uint8_t gateNum, uint8_t procNum)
Tries to lock the SEMA42 gate.
- void [SEMA42_Lock](#) (SEMA42_Type *base, uint8_t gateNum, uint8_t procNum)
Locks the SEMA42 gate.
- static void [SEMA42_Unlock](#) (SEMA42_Type *base, uint8_t gateNum)
Unlocks the SEMA42 gate.
- static [sema42_gate_status_t SEMA42_GetGateStatus](#) (SEMA42_Type *base, uint8_t gateNum)
Gets the status of the SEMA42 gate.
- [status_t SEMA42_ResetGate](#) (SEMA42_Type *base, uint8_t gateNum)
Resets the SEMA42 gate to an unlocked status.
- static [status_t SEMA42_ResetAllGates](#) (SEMA42_Type *base)
Resets all SEMA42 gates to an unlocked status.

Driver version

- #define [FSL_SEMA42_DRIVER_VERSION](#) (MAKE_VERSION(2, 0, 2))
SEMA42 driver version.

34.3 Macro Definition Documentation

34.3.1 #define SEMA42_GATE_NUM_RESET_ALL (64U)

34.3.2 #define SEMA42_GATEEn(*base*, *n*) (((volatile uint8_t *)(&((*base*)->GATE3)))[(*n*) ^ 3U])

The SEMA42 gates are sorted in the order 3, 2, 1, 0, 7, 6, 5, 4, ... not in the order 0, 1, 2, 3, 4, 5, 6, 7, ... The macro SEMA42_GATEEn gets the SEMA42 gate based on the gate index.

The input gate index is XOR'ed with 3U: $0 \wedge 3 = 3$ $1 \wedge 3 = 2$ $2 \wedge 3 = 1$ $3 \wedge 3 = 0$ $4 \wedge 3 = 7$ $5 \wedge 3 = 6$ $6 \wedge 3 = 5$ $7 \wedge 3 = 4$...

34.4 Enumeration Type Documentation

34.4.1 anonymous enum

Enumerator

kStatus_SEMA42_Busy SEMA42 gate has been locked by other processor.

kStatus_SEMA42_Reseting SEMA42 gate reseting is ongoing.

34.4.2 enum sema42_gate_status_t

Enumerator

kSEMA42_Unlocked The gate is unlocked.

kSEMA42_LockedByProc0 The gate is locked by processor 0.

kSEMA42_LockedByProc1 The gate is locked by processor 1.

kSEMA42_LockedByProc2 The gate is locked by processor 2.

kSEMA42_LockedByProc3 The gate is locked by processor 3.

kSEMA42_LockedByProc4 The gate is locked by processor 4.

kSEMA42_LockedByProc5 The gate is locked by processor 5.

kSEMA42_LockedByProc6 The gate is locked by processor 6.

kSEMA42_LockedByProc7 The gate is locked by processor 7.

kSEMA42_LockedByProc8 The gate is locked by processor 8.

kSEMA42_LockedByProc9 The gate is locked by processor 9.

kSEMA42_LockedByProc10 The gate is locked by processor 10.

kSEMA42_LockedByProc11 The gate is locked by processor 11.

kSEMA42_LockedByProc12 The gate is locked by processor 12.

kSEMA42_LockedByProc13 The gate is locked by processor 13.

kSEMA42_LockedByProc14 The gate is locked by processor 14.

34.5 Function Documentation

34.5.1 void SEMA42_Init (SEMA42_Type * *base*)

This function initializes the SEMA42 module. It only enables the clock but does not reset the gates because the module might be used by other processors at the same time. To reset the gates, call either SEMA42_ResetGate or SEMA42_ResetAllGates function.

Parameters

<i>base</i>	SEMA42 peripheral base address.
-------------	---------------------------------

34.5.2 void SEMA42_Deinit (SEMA42_Type * *base*)

This function de-initializes the SEMA42 module. It only disables the clock.

Parameters

<i>base</i>	SEMA42 peripheral base address.
-------------	---------------------------------

34.5.3 status_t SEMA42_TryLock (SEMA42_Type * *base*, uint8_t *gateNum*, uint8_t *procNum*)

This function tries to lock the specific SEMA42 gate. If the gate has been locked by another processor, this function returns an error code.

Parameters

<i>base</i>	SEMA42 peripheral base address.
<i>gateNum</i>	Gate number to lock.
<i>procNum</i>	Current processor number.

Return values

<i>kStatus_Success</i>	Lock the sema42 gate successfully.
<i>kStatus_SEMA42_Busy</i>	Sema42 gate has been locked by another processor.

34.5.4 void SEMA42_Lock (SEMA42_Type * *base*, uint8_t *gateNum*, uint8_t *procNum*)

This function locks the specific SEMA42 gate. If the gate has been locked by other processors, this function waits until it is unlocked and then lock it.

Parameters

<i>base</i>	SEMA42 peripheral base address.
<i>gateNum</i>	Gate number to lock.
<i>procNum</i>	Current processor number.

34.5.5 static void SEMA42_Unlock (SEMA42_Type * *base*, uint8_t *gateNum*) [inline], [static]

This function unlocks the specific SEMA42 gate. It only writes unlock value to the SEMA42 gate register. However, it does not check whether the SEMA42 gate is locked by the current processor or not. As a result, if the SEMA42 gate is not locked by the current processor, this function has no effect.

Parameters

<i>base</i>	SEMA42 peripheral base address.
<i>gateNum</i>	Gate number to unlock.

34.5.6 static sema42_gate_status_t SEMA42_GetGateStatus (SEMA42_Type * *base*, uint8_t *gateNum*) [inline], [static]

This function checks the lock status of a specific SEMA42 gate.

Parameters

<i>base</i>	SEMA42 peripheral base address.
<i>gateNum</i>	Gate number.

Returns

status Current status.

34.5.7 status_t SEMA42_ResetGate (SEMA42_Type * *base*, uint8_t *gateNum*)

This function resets a SEMA42 gate to an unlocked status.

Parameters

<i>base</i>	SEMA42 peripheral base address.
<i>gateNum</i>	Gate number.

Return values

<i>kStatus_Success</i>	SEMA42 gate is reset successfully.
<i>kStatus_SEMA42_Reseting</i>	Some other reset process is ongoing.

34.5.8 static status_t SEMA42_ResetAllGates (SEMA42_Type * *base*) [inline], [static]

This function resets all SEMA42 gate to an unlocked status.

Parameters

<i>base</i>	SEMA42 peripheral base address.
-------------	---------------------------------

Return values

<i>kStatus_Success</i>	SEMA42 is reset successfully.
<i>kStatus_SEMA42_Reseting</i>	Some other reset process is ongoing.

Chapter 35

TPM: Timer PWM Module

35.1 Overview

The MCUXpresso SDK provides a driver for the Timer PWM Module (TPM) of MCUXpresso SDK devices.

The TPM driver supports the generation of PWM signals, input capture, and output compare modes. On some SoCs, the driver supports the generation of combined PWM signals, dual-edge capture, and quadrature decoder modes. The driver also supports configuring each of the TPM fault inputs. The fault input is available only on some SoCs.

35.2 Introduction of TPM

35.2.1 Initialization and deinitialization

The function [TPM_Init\(\)](#) initializes the TPM with a specified configurations. The function [TPM_GetDefaultConfig\(\)](#) gets the default configurations. On some SoCs, the initialization function issues a software reset to reset the TPM internal logic. The initialization function configures the TPM's behavior when it receives a trigger input and its operation in doze and debug modes.

The function [TPM_Deinit\(\)](#) disables the TPM counter and turns off the module clock.

35.2.2 PWM Operations

The function [TPM_SetupPwm\(\)](#) sets up TPM channels for the PWM output. The function can set up the PWM signal properties for multiple channels. Each channel has its own [tpm_chnl_pwm_signal_param_t](#) structure that is used to specify the output signals duty cycle and level-mode. However, the same PWM period and PWM mode is applied to all channels requesting a PWM output. The signal duty cycle is provided as a percentage of the PWM period. Its value should be between 0 and 100 where 0=inactive signal (0% duty cycle) and 100=always active signal (100% duty cycle). When generating a combined PWM signal, the channel number passed refers to a channel pair number, for example 0 refers to channel 0 and 1, 1 refers to channels 2 and 3.

The function [TPM_UpdatePwmDutycycle\(\)](#) updates the PWM signal duty cycle of a particular TPM channel.

The function [TPM_UpdateChnlEdgeLevelSelect\(\)](#) updates the level select bits of a particular TPM channel. This can be used to disable the PWM output when making changes to the PWM signal.

35.2.3 Input capture operations

The function [TPM_SetupInputCapture\(\)](#) sets up a TPM channel for input capture. The user can specify the capture edge.

The function [TPM_SetupDualEdgeCapture\(\)](#) can be used to measure the pulse width of a signal. This is available only for certain SoCs. A channel pair is used during the capture with the input signal coming through a channel that can be configured. The user can specify the capture edge for each channel and any filter value to be used when processing the input signal.

35.2.4 Output compare operations

The function [TPM_SetupOutputCompare\(\)](#) sets up a TPM channel for output comparison. The user can specify the channel output on a successful comparison and a comparison value.

35.2.5 Quad decode

The function [TPM_SetupQuadDecode\(\)](#) sets up TPM channels 0 and 1 for quad decode, which is available only for certain SoCs. The user can specify the quad decode mode, polarity, and filter properties for each input signal.

35.2.6 Fault operation

The function [TPM_SetupFault\(\)](#) sets up the properties for each fault, which is available only for certain SoCs. The user can specify the fault polarity and whether to use a filter on a fault input. The overall fault filter value and fault control mode are set up during initialization.

35.2.7 Status

Provides functions to get and clear the TPM status.

35.2.8 Interrupt

Provides functions to enable/disable TPM interrupts and get current enabled interrupts.

35.3 Typical use case

35.3.1 PWM output

Output the PWM signal on 2 TPM channels with different duty cycles. Periodically update the PWM signal duty cycle. Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/tpm

Data Structures

- struct `tpm_chnl_pwm_signal_param_t`
Options to configure a TPM channel's PWM signal. [More...](#)
- struct `tpm_dual_edge_capture_param_t`
TPM dual edge capture parameters. [More...](#)
- struct `tpm_phase_params_t`
TPM quadrature decode phase parameters. [More...](#)
- struct `tpm_config_t`
TPM config structure. [More...](#)

Macros

- #define `TPM_MAX_COUNTER_VALUE(x)` ((1U != (uint8_t)FSL_FEATURE_TPM_HAS_32BIT_COUNTERn(x)) ? 0xFFFFU : 0xFFFFFFFFU)
Help macro to get the max counter value.

Enumerations

- enum `tpm_chnl_t` {

`kTPM_Chnl_0` = 0U,
`kTPM_Chnl_1`,
`kTPM_Chnl_2`,
`kTPM_Chnl_3`,
`kTPM_Chnl_4`,
`kTPM_Chnl_5`,
`kTPM_Chnl_6`,
`kTPM_Chnl_7` }

List of TPM channels.
- enum `tpm_pwm_mode_t` {

`kTPM_EdgeAlignedPwm` = 0U,
`kTPM_CenterAlignedPwm`,
`kTPM_CombinedPwm` }

TPM PWM operation modes.
- enum `tpm_pwm_level_select_t` {

`kTPM_HighTrue` = 0U,
`kTPM_LowTrue` }

TPM PWM output pulse mode: high-true, low-true or no output.
- enum `tpm_pwm_pause_level_select_t` {

`kTPM_ClearOnPause` = 0U,
`kTPM_SetOnPause` }

TPM PWM output when first enabled or paused: set or clear.

- enum `tpm_chnl_control_bit_mask_t` {

 `kTPM_ChnlELSnAMask` = `TPM_CnSC_ELSA_MASK`,

 `kTPM_ChnlELSnBMask` = `TPM_CnSC_ELSB_MASK`,

 `kTPM_ChnlMSAMask` = `TPM_CnSC_MSA_MASK`,

 `kTPM_ChnlMSBMask` = `TPM_CnSC_MSB_MASK` }

 List of TPM channel modes and level control bit mask.
- enum `tpm_trigger_select_t`

 Trigger sources available.
- enum `tpm_trigger_source_t` {

 `kTPM_TriggerSource_External` = `0U`,

 `kTPM_TriggerSource_Internal` }

 Trigger source options available.
- enum `tpm_ext_trigger_polarity_t` {

 `kTPM_ExtTrigger_Active_High` = `0U`,

 `kTPM_ExtTrigger_Active_Low` }

 External trigger source polarity.
- enum `tpm_output_compare_mode_t` {

 `kTPM_NoOutputSignal` = `(1U << TPM_CnSC_MSA_SHIFT)`,

 `kTPM_ToggleOnMatch` = `((1U << TPM_CnSC_MSA_SHIFT) | (1U << TPM_CnSC_ELSA_SHIFT))`,

 `kTPM_ClearOnMatch` = `((1U << TPM_CnSC_MSA_SHIFT) | (2U << TPM_CnSC_ELSA_SHIFT))`,

 `kTPM_SetOnMatch` = `((1U << TPM_CnSC_MSA_SHIFT) | (3U << TPM_CnSC_ELSA_SHIFT))`,

 `kTPM_HighPulseOutput` = `((3U << TPM_CnSC_MSA_SHIFT) | (1U << TPM_CnSC_ELSA_SHIFT))`,

 `kTPM_LowPulseOutput` = `((3U << TPM_CnSC_MSA_SHIFT) | (2U << TPM_CnSC_ELSA_SHIFT))` }

 TPM output compare modes.
- enum `tpm_input_capture_edge_t` {

 `kTPM_RisingEdge` = `(1U << TPM_CnSC_ELSA_SHIFT)`,

 `kTPM_FallingEdge` = `(2U << TPM_CnSC_ELSA_SHIFT)`,

 `kTPM_RiseAndFallEdge` = `(3U << TPM_CnSC_ELSA_SHIFT)` }

 TPM input capture edge.
- enum `tpm_quad_decode_mode_t` {

 `kTPM_QuadPhaseEncode` = `0U`,

 `kTPM_QuadCountAndDir` }

 TPM quadrature decode modes.
- enum `tpm_phase_polarity_t` {

 `kTPM_QuadPhaseNormal` = `0U`,

 `kTPM_QuadPhaseInvert` }

 TPM quadrature phase polarities.
- enum `tpm_clock_source_t` {

 `kTPM_SystemClock` = `1U`,

 `kTPM_ExternalClock`,

 `kTPM_ExternalInputTriggerClock` }

 TPM clock source selection.

- enum `tpm_clock_prescale_t` {

kTPM_Prescale_Divide_1 = 0U,

kTPM_Prescale_Divide_2,

kTPM_Prescale_Divide_4,

kTPM_Prescale_Divide_8,

kTPM_Prescale_Divide_16,

kTPM_Prescale_Divide_32,

kTPM_Prescale_Divide_64,

kTPM_Prescale_Divide_128 }

TPM prescale value selection for the clock source.

- enum `tpm_interrupt_enable_t` {

kTPM_Chnl0InterruptEnable = (1U << 0),

kTPM_Chnl1InterruptEnable = (1U << 1),

kTPM_Chnl2InterruptEnable = (1U << 2),

kTPM_Chnl3InterruptEnable = (1U << 3),

kTPM_Chnl4InterruptEnable = (1U << 4),

kTPM_Chnl5InterruptEnable = (1U << 5),

kTPM_Chnl6InterruptEnable = (1U << 6),

kTPM_Chnl7InterruptEnable = (1U << 7),

kTPM_TimeOverflowInterruptEnable = (1U << 8) }

List of TPM interrupts.

- enum `tpm_status_flags_t` {

kTPM_Chnl0Flag = (1U << 0),

kTPM_Chnl1Flag = (1U << 1),

kTPM_Chnl2Flag = (1U << 2),

kTPM_Chnl3Flag = (1U << 3),

kTPM_Chnl4Flag = (1U << 4),

kTPM_Chnl5Flag = (1U << 5),

kTPM_Chnl6Flag = (1U << 6),

kTPM_Chnl7Flag = (1U << 7),

kTPM_TimeOverflowFlag = (1U << 8) }

List of TPM flags.

Functions

- static void `TPM_Reset` (TPM_Type *base)
Performs a software reset on the TPM module.

Driver version

- #define `FSL TPM_DRIVER_VERSION` (MAKE_VERSION(2, 2, 0))
TPM driver version 2.2.0.

Initialization and deinitialization

- void `TPM_Init` (TPM_Type *base, const `tpm_config_t` *config)
Ungates the TPM clock and configures the peripheral for basic operation.

- void **TPM_Deinit** (TPM_Type *base)
Stops the counter and gates the TPM clock.
- void **TPM_GetDefaultConfig** (tpm_config_t *config)
Fill in the TPM config struct with the default settings.
- tpm_clock_prescale_t **TPM_CalculateCounterClkDiv** (TPM_Type *base, uint32_t counterPeriod_Hz, uint32_t srcClock_Hz)
Calculates the counter clock prescaler.

Channel mode operations

- status_t **TPM_SetupPwm** (TPM_Type *base, const tpm_chnl_pwm_signal_param_t *chnlParams, uint8_t numOfChnls, tpm_pwm_mode_t mode, uint32_t pwmFreq_Hz, uint32_t srcClock_Hz)
Configures the PWM signal parameters.
- status_t **TPM_UpdatePwmDutyCycle** (TPM_Type *base, tpm_chnl_t chnlNumber, tpm_pwm_mode_t currentPwmMode, uint8_t dutyCyclePercent)
Update the duty cycle of an active PWM signal.
- void **TPM_UpdateChnlEdgeLevelSelect** (TPM_Type *base, tpm_chnl_t chnlNumber, uint8_t level)
Update the edge level selection for a channel.
- static uint8_t **TPM_GetChannelContorlBits** (TPM_Type *base, tpm_chnl_t chnlNumber)
Get the channel control bits value (mode, edge and level bit fileds).
- static void **TPM_DisableChannel** (TPM_Type *base, tpm_chnl_t chnlNumber)
Dsiable the channel.
- static void **TPM_EnableChannel** (TPM_Type *base, tpm_chnl_t chnlNumber, uint8_t control)
Enable the channel according to mode and level configs.
- void **TPM_SetupInputCapture** (TPM_Type *base, tpm_chnl_t chnlNumber, tpm_input_capture_edge_t captureMode)
Enables capturing an input signal on the channel using the function parameters.
- void **TPM_SetupOutputCompare** (TPM_Type *base, tpm_chnl_t chnlNumber, tpm_output_compare_mode_t compareMode, uint32_t compareValue)
Configures the TPM to generate timed pulses.
- void **TPM_SetupDualEdgeCapture** (TPM_Type *base, tpm_chnl_t chnlPairNumber, const tpm_dual_edge_capture_param_t *edgeParam, uint32_t filterValue)
Configures the dual edge capture mode of the TPM.
- void **TPM_SetupQuadDecode** (TPM_Type *base, const tpm_phase_params_t *phaseAParams, const tpm_phase_params_t *phaseBParams, tpm_quad_decode_mode_t quadMode)
Configures the parameters and activates the quadrature decode mode.
- static void **TPM_SetChannelPolarity** (TPM_Type *base, tpm_chnl_t chnlNumber, bool enable)
Set the input and output polarity of each of the channels.
- static void **TPM_EnableChannelExtTrigger** (TPM_Type *base, tpm_chnl_t chnlNumber, bool enable)
Enable external trigger input to be used by channel.

Interrupt Interface

- void **TPM_EnableInterrupts** (TPM_Type *base, uint32_t mask)
Enables the selected TPM interrupts.
- void **TPM_DisableInterrupts** (TPM_Type *base, uint32_t mask)
Disables the selected TPM interrupts.
- uint32_t **TPM_GetEnabledInterrupts** (TPM_Type *base)
Gets the enabled TPM interrupts.

Status Interface

- static uint32_t [TPM_GetChannelValue](#) (TPM_Type *base, [tpm_chnl_t](#) chnlNumber)
Gets the TPM channel value.
- static uint32_t [TPM_GetStatusFlags](#) (TPM_Type *base)
Gets the TPM status flags.
- static void [TPM_ClearStatusFlags](#) (TPM_Type *base, uint32_t mask)
Clears the TPM status flags.

Read and write the timer period

- static void [TPM_SetTimerPeriod](#) (TPM_Type *base, uint32_t ticks)
Sets the timer period in units of ticks.
- static uint32_t [TPM_GetCurrentTimerCount](#) (TPM_Type *base)
Reads the current timer counting value.

Timer Start and Stop

- static void [TPM_StartTimer](#) (TPM_Type *base, [tpm_clock_source_t](#) clockSource)
Starts the TPM counter.
- static void [TPM_StopTimer](#) (TPM_Type *base)
Stops the TPM counter.

35.4 Data Structure Documentation

35.4.1 struct tpm_chnl_pwm_signal_param_t

Data Fields

- [tpm_chnl_t](#) chnlNumber
TPM channel to configure.
- [tpm_pwm_pause_level_select_t](#) pauseLevel
PWM output level when counter first enabled or paused.
- [tpm_pwm_level_select_t](#) level
PWM output active level select.
- uint8_t [dutyCyclePercent](#)
PWM pulse width, value should be between 0 to 100 0=inactive signal(0% duty cycle)...
- uint8_t [firstEdgeDelayPercent](#)
Used only in combined PWM mode to generate asymmetrical PWM.
- bool [enableComplementary](#)
Used only in combined PWM mode.
- [tpm_pwm_pause_level_select_t](#) secPauseLevel
Used only in combined PWM mode.
- uint8_t [deadTimeValue](#) [2]
The dead time value for channel n and n+1 in combined complementary PWM mode.

Field Documentation

(1) [tpm_chnl_t tpm_chnl_pwm_signal_param_t::chnlNumber](#)

In combined mode (available in some SoC's), this represents the channel pair number

(2) uint8_t tpm_chnl_pwm_signal_param_t::dutyCyclePercent

100=always active signal (100% duty cycle)

(3) uint8_t tpm_chnl_pwm_signal_param_t::firstEdgeDelayPercent

Specifies the delay to the first edge in a PWM period. If unsure, leave as 0. Should be specified as percentage of the PWM period, (dutyCyclePercent + firstEdgeDelayPercent) value should be not greater than 100.

(4) bool tpm_chnl_pwm_signal_param_t::enableComplementary

true: The combined channels output complementary signals; false: The combined channels output same signals;

(5) tpm_pwm_pause_level_select_t tpm_chnl_pwm_signal_param_t::secPauseLevel

Define the second channel output level when counter first enabled or paused

(6) uint8_t tpm_chnl_pwm_signal_param_t::deadTimeValue[2]

Deadtime insertion is disabled when this value is zero, otherwise deadtime insertion for channel n/n+1 is configured as (deadTimeValue * 4) clock cycles. deadTimeValue's available range is 0 ~ 15.

35.4.2 struct tpm_dual_edge_capture_param_t

Note

This mode is available only on some SoC's.

Data Fields

- bool [enableSwap](#)
true: Use channel n+1 input, channel n input is ignored; false: Use channel n input, channel n+1 input is ignored
- [tpm_input_capture_edge_t currChanEdgeMode](#)
Input capture edge select for channel n.
- [tpm_input_capture_edge_t nextChanEdgeMode](#)
Input capture edge select for channel n+1.

35.4.3 struct tpm_phase_params_t**Data Fields**

- uint32_t [phaseFilterVal](#)
Filter value, filter is disabled when the value is zero.

- **tpm_phase_polarity_t phasePolarity**
Phase polarity.

35.4.4 struct tpm_config_t

This structure holds the configuration settings for the TPM peripheral. To initialize this structure to reasonable defaults, call the [TPM_GetDefaultConfig\(\)](#) function and pass a pointer to your config structure instance.

The config struct can be made const so it resides in flash

Data Fields

- **tpm_clock_prescale_t prescale**
Select TPM clock prescale value.
- **bool useGlobalTimeBase**
true: The TPM channels use an external global time base (the local counter still use for generate overflow interrupt and DMA request); false: All TPM channels use the local counter as their timebase
- **bool syncGlobalTimeBase**
true: The TPM counter is synchronized to the global time base; false: disabled
- **tpm_trigger_select_t triggerSelect**
Input trigger to use for controlling the counter operation.
- **tpm_trigger_source_t triggerSource**
Decides if we use external or internal trigger.
- **tpm_ext_trigger_polarity_t extTriggerPolarity**
when using external trigger source, need selects the polarity of it.
- **bool enableDoze**
true: TPM counter is paused in doze mode; false: TPM counter continues in doze mode
- **bool enableDebugMode**
true: TPM counter continues in debug mode; false: TPM counter is paused in debug mode
- **bool enableReloadOnTrigger**
true: TPM counter is reloaded on trigger; false: TPM counter not reloaded
- **bool enableStopOnOverflow**
true: TPM counter stops after overflow; false: TPM counter continues running after overflow
- **bool enableStartOnTrigger**
true: TPM counter only starts when a trigger is detected; false: TPM counter starts immediately
- **bool enablePauseOnTrigger**
true: TPM counter will pause while trigger remains asserted; false: TPM counter continues running
- **uint8_t chnlPolarity**
Defines the input/output polarity of the channels in POL register.

Field Documentation

- (1) **tpm_trigger_source_t tpm_config_t::triggerSource**
- (2) **tpm_ext_trigger_polarity_t tpm_config_t::extTriggerPolarity**

35.5 Macro Definition Documentation

35.5.1 #define FSL TPM DRIVER VERSION (MAKE_VERSION(2, 2, 0))

35.6 Enumeration Type Documentation

35.6.1 enum tpm_chnl_t

Note

Actual number of available channels is SoC dependent

Enumerator

- kTPM_Chnl_0* TPM channel number 0.
- kTPM_Chnl_1* TPM channel number 1.
- kTPM_Chnl_2* TPM channel number 2.
- kTPM_Chnl_3* TPM channel number 3.
- kTPM_Chnl_4* TPM channel number 4.
- kTPM_Chnl_5* TPM channel number 5.
- kTPM_Chnl_6* TPM channel number 6.
- kTPM_Chnl_7* TPM channel number 7.

35.6.2 enum tpm_pwm_mode_t

Enumerator

- kTPM_EdgeAlignedPwm* Edge aligned PWM.
- kTPM_CenterAlignedPwm* Center aligned PWM.
- kTPM_CombinedPwm* Combined PWM (Edge-aligned, center-aligned, or asymmetrical PWMs can be obtained in combined mode using different software configurations)

35.6.3 enum tpm_pwm_level_select_t

Note

When the TPM has PWM pause level select feature, the PWM output cannot be turned off by selecting the output level. In this case, the channel must be closed to close the PWM output.

Enumerator

- kTPM_HighTrue* High true pulses.
- kTPM_LowTrue* Low true pulses.

35.6.4 enum tpm_pwm_pause_level_select_t

Enumerator

kTPM_ClearOnPause Clear Output when counter first enabled or paused.*kTPM_SetOnPause* Set Output when counter first enabled or paused.**35.6.5 enum tpm_chnl_control_bit_mask_t**

Enumerator

kTPM_ChnlELSnAMask Channel ELSA bit mask.*kTPM_ChnlELSnBMask* Channel ELSB bit mask.*kTPM_ChnlMSAMask* Channel MSA bit mask.*kTPM_ChnlMSBMask* Channel MSB bit mask.**35.6.6 enum tpm_trigger_select_t**

This is used for both internal & external trigger sources (external trigger sources available in certain SoC's)

Note

The actual trigger sources available is SoC-specific.

35.6.7 enum tpm_trigger_source_t

Note

This selection is available only on some SoC's. For SoC's without this selection, the only trigger source available is internal trigger.

Enumerator

kTPM_TriggerSource_External Use external trigger input.*kTPM_TriggerSource_Internal* Use internal trigger (channel pin input capture)**35.6.8 enum tpm_ext_trigger_polarity_t**

Note

Selects the polarity of the external trigger source.

Enumerator

kTPM_ExtTrigger_Active_High External trigger input is active high.

kTPM_ExtTrigger_Active_Low External trigger input is active low.

35.6.9 enum tpm_output_compare_mode_t

Enumerator

kTPM_NoOutputSignal No channel output when counter reaches CnV.

kTPM_ToggleOnMatch Toggle output.

kTPM_ClearOnMatch Clear output.

kTPM_SetOnMatch Set output.

kTPM_HighPulseOutput Pulse output high.

kTPM_LowPulseOutput Pulse output low.

35.6.10 enum tpm_input_capture_edge_t

Enumerator

kTPM_RisingEdge Capture on rising edge only.

kTPM_FallingEdge Capture on falling edge only.

kTPM_RiseAndFallEdge Capture on rising or falling edge.

35.6.11 enum tpm_quad_decode_mode_t

Note

This mode is available only on some SoC's.

Enumerator

kTPM_QuadPhaseEncode Phase A and Phase B encoding mode.

kTPM_QuadCountAndDir Count and direction encoding mode.

35.6.12 enum tpm_phase_polarity_t

Enumerator

kTPM_QuadPhaseNormal Phase input signal is not inverted.*kTPM_QuadPhaseInvert* Phase input signal is inverted.**35.6.13 enum tpm_clock_source_t**

Enumerator

kTPM_SystemClock System clock.*kTPM_ExternalClock* External TPM_EXTCLK pin clock.*kTPM_ExternalInputTriggerClock* Selected external input trigger clock.**35.6.14 enum tpm_clock_prescale_t**

Enumerator

kTPM_Prescale_Divide_1 Divide by 1.*kTPM_Prescale_Divide_2* Divide by 2.*kTPM_Prescale_Divide_4* Divide by 4.*kTPM_Prescale_Divide_8* Divide by 8.*kTPM_Prescale_Divide_16* Divide by 16.*kTPM_Prescale_Divide_32* Divide by 32.*kTPM_Prescale_Divide_64* Divide by 64.*kTPM_Prescale_Divide_128* Divide by 128.**35.6.15 enum tpm_interrupt_enable_t**

Enumerator

kTPM_Chnl0InterruptEnable Channel 0 interrupt.*kTPM_Chnl1InterruptEnable* Channel 1 interrupt.*kTPM_Chnl2InterruptEnable* Channel 2 interrupt.*kTPM_Chnl3InterruptEnable* Channel 3 interrupt.*kTPM_Chnl4InterruptEnable* Channel 4 interrupt.*kTPM_Chnl5InterruptEnable* Channel 5 interrupt.*kTPM_Chnl6InterruptEnable* Channel 6 interrupt.*kTPM_Chnl7InterruptEnable* Channel 7 interrupt.*kTPM_TimeOverflowInterruptEnable* Time overflow interrupt.

35.6.16 enum tpm_status_flags_t

Enumerator

<i>kTPM_Chnl0Flag</i>	Channel 0 flag.
<i>kTPM_Chnl1Flag</i>	Channel 1 flag.
<i>kTPM_Chnl2Flag</i>	Channel 2 flag.
<i>kTPM_Chnl3Flag</i>	Channel 3 flag.
<i>kTPM_Chnl4Flag</i>	Channel 4 flag.
<i>kTPM_Chnl5Flag</i>	Channel 5 flag.
<i>kTPM_Chnl6Flag</i>	Channel 6 flag.
<i>kTPM_Chnl7Flag</i>	Channel 7 flag.
<i>kTPM_TimeOverflowFlag</i>	Time overflow flag.

35.7 Function Documentation

35.7.1 void TPM_Init (TPM_Type * *base*, const tpm_config_t * *config*)

Note

This API should be called at the beginning of the application using the TPM driver.

Parameters

<i>base</i>	TPM peripheral base address
<i>config</i>	Pointer to user's TPM config structure.

35.7.2 void TPM_Deinit (TPM_Type * *base*)

Parameters

<i>base</i>	TPM peripheral base address
-------------	-----------------------------

35.7.3 void TPM_GetDefaultConfig (tpm_config_t * *config*)

The default values are:

```
* config->prescale = kTPM_Prescale_Divide_1;
* config->useGlobalTimeBase = false;
* config->syncGlobalTimeBase = false;
* config->dozeEnable = false;
* config->dbgMode = false;
* config->enableReloadOnTrigger = false;
* config->enableStopOnOverflow = false;
```

```

*     config->enableStartOnTrigger = false;
*#if FSL_FEATURE TPM HAS_PAUSE_COUNTER_ON_TRIGGER
*     config->enablePauseOnTrigger = false;
#endif
*     config->triggerSelect = kTPM_Trigger_Select_0;
*#if FSL_FEATURE TPM HAS_EXTERNAL_TRIGGER_SELECTION
*     config->triggerSource = kTPM_TriggerSource_External;
*     config->extTriggerPolarity = kTPM_ExtTrigger_Active_High;
#endif
*#if defined(FSL_FEATURE TPM HAS_POL) && FSL_FEATURE TPM HAS_POL
*     config->chnlPolarity = 0U;
#endif
*

```

Parameters

<i>config</i>	Pointer to user's TPM config structure.
---------------	---

35.7.4 **tpm_clock_prescale_t TPM_CalculateCounterClkDiv (TPM_Type * *base*, uint32_t *counterPeriod_Hz*, uint32_t *srcClock_Hz*)**

This function calculates the values for SC[PS].

Parameters

<i>base</i>	TPM peripheral base address
<i>counterPeriod_Hz</i>	The desired frequency in Hz which corresponding to the time when the counter reaches the mod value
<i>srcClock_Hz</i>	TPM counter clock in Hz

return Calculated clock prescaler value.

35.7.5 **status_t TPM_SetupPwm (TPM_Type * *base*, const tpm_chnl_pwm_signal_param_t * *chnlParams*, uint8_t *numOfChnls*, tpm_pwm_mode_t *mode*, uint32_t *pwmFreq_Hz*, uint32_t *srcClock_Hz*)**

User calls this function to configure the PWM signals period, mode, dutycycle and edge. Use this function to configure all the TPM channels that will be used to output a PWM signal

Parameters

<i>base</i>	TPM peripheral base address
-------------	-----------------------------

<i>chnlParams</i>	Array of PWM channel parameters to configure the channel(s)
<i>numOfChnls</i>	Number of channels to configure, this should be the size of the array passed in
<i>mode</i>	PWM operation mode, options available in enumeration tpm_pwm_mode_t
<i>pwmFreq_Hz</i>	PWM signal frequency in Hz
<i>srcClock_Hz</i>	TPM counter clock in Hz

Returns

kStatus_Success if the PWM setup was successful, kStatus_Error on failure

35.7.6 status_t TPM_UpdatePwmDutycycle (**TPM_Type** * *base*, **tpm_chnl_t** *chnlNumber*, **tpm_pwm_mode_t** *currentPwmMode*, **uint8_t** *dutyCyclePercent*)

Parameters

<i>base</i>	TPM peripheral base address
<i>chnlNumber</i>	The channel number. In combined mode, this represents the channel pair number
<i>currentPwmMode</i>	The current PWM mode set during PWM setup
<i>dutyCyclePercent</i>	New PWM pulse width, value should be between 0 to 100 0=inactive signal(0% duty cycle)... 100=active signal (100% duty cycle)

Returns

kStatus_Success if the PWM setup was successful, kStatus_Error on failure

35.7.7 void TPM_UpdateChnlEdgeLevelSelect (**TPM_Type** * *base*, **tpm_chnl_t** *chnlNumber*, **uint8_t** *level*)

Note

When the TPM has PWM pause level select feature (FSL_FEATURE TPM HAS_PAUSE_LEVEL_SELECT = 1), the PWM output cannot be turned off by selecting the output level. In this case, must use TPM_DisableChannel API to close the PWM output.

Parameters

<i>base</i>	TPM peripheral base address
<i>chnlNumber</i>	The channel number
<i>level</i>	The level to be set to the ELSnB:ELSnA field; valid values are 00, 01, 10, 11. See the appropriate SoC reference manual for details about this field.

35.7.8 static uint8_t TPM_GetChannelControlBits (TPM_Type * *base*, tpm_chnl_t *chnlNumber*) [inline], [static]

This function disable the channel by clear all mode and level control bits.

Parameters

<i>base</i>	TPM peripheral base address
<i>chnlNumber</i>	The channel number

Returns

The control bits value. This is the logical OR of members of the enumeration [tpm_chnl_control_bit-mask_t](#).

35.7.9 static void TPM_DisableChannel (TPM_Type * *base*, tpm_chnl_t *chnlNumber*) [inline], [static]

This function disable the channel by clear all mode and level control bits.

Parameters

<i>base</i>	TPM peripheral base address
<i>chnlNumber</i>	The channel number

35.7.10 static void TPM_EnableChannel (TPM_Type * *base*, tpm_chnl_t *chnlNumber*, uint8_t *control*) [inline], [static]

This function enable the channel output according to input mode/level config parameters.

Parameters

<i>base</i>	TPM peripheral base address
<i>chnlNumber</i>	The channel number
<i>control</i>	The control bits value. This is the logical OR of members of the enumeration tpm_chnl_control_bit_mask_t .

35.7.11 void TPM_SetupInputCapture (TPM_Type * *base*, tpm_chnl_t *chnlNumber*, tpm_input_capture_edge_t *captureMode*)

When the edge specified in the captureMode argument occurs on the channel, the TPM counter is captured into the CnV register. The user has to read the CnV register separately to get this value.

Parameters

<i>base</i>	TPM peripheral base address
<i>chnlNumber</i>	The channel number
<i>captureMode</i>	Specifies which edge to capture

35.7.12 void TPM_SetupOutputCompare (TPM_Type * *base*, tpm_chnl_t *chnlNumber*, tpm_output_compare_mode_t *compareMode*, uint32_t *compareValue*)

When the TPM counter matches the value of compareVal argument (this is written into CnV reg), the channel output is changed based on what is specified in the compareMode argument.

Parameters

<i>base</i>	TPM peripheral base address
<i>chnlNumber</i>	The channel number
<i>compareMode</i>	Action to take on the channel output when the compare condition is met
<i>compareValue</i>	Value to be programmed in the CnV register.

35.7.13 **void TPM_SetupDualEdgeCapture (TPM_Type * *base*, tpm_chnl_t *chnlPairNumber*, const tpm_dual_edge_capture_param_t * *edgeParam*, uint32_t *filterValue*)**

This function allows to measure a pulse width of the signal on the input of channel of a channel pair. The filter function is disabled if the filterVal argument passed is zero.

Parameters

<i>base</i>	TPM peripheral base address
<i>chnlPair-Number</i>	The TPM channel pair number; options are 0, 1, 2, 3
<i>edgeParam</i>	Sets up the dual edge capture function
<i>filterValue</i>	Filter value, specify 0 to disable filter.

35.7.14 void TPM_SetupQuadDecode (TPM_Type * *base*, const tpm_phase_params_t * *phaseAParams*, const tpm_phase_params_t * *phaseBParams*, tpm_quad_decode_mode_t *quadMode*)

Parameters

<i>base</i>	TPM peripheral base address
<i>phaseAParams</i>	Phase A configuration parameters
<i>phaseBParams</i>	Phase B configuration parameters
<i>quadMode</i>	Selects encoding mode used in quadrature decoder mode

35.7.15 static void TPM_SetChannelPolarity (TPM_Type * *base*, tpm_chnl_t *chnlNumber*, bool *enable*) [inline], [static]

Parameters

<i>base</i>	TPM peripheral base address
<i>chnlNumber</i>	The channel number
<i>enable</i>	true: Set the channel polarity to active high; false: Set the channel polarity to active low;

35.7.16 static void TPM_EnableChannelExtTrigger (TPM_Type * *base*, tpm_chnl_t *chnlNumber*, bool *enable*) [inline], [static]

In input capture mode, configures the trigger input that is used by the channel to capture the counter value. In output compare or PWM mode, configures the trigger input used to modulate the channel output. When modulating the output, the output is forced to the channel initial value whenever the trigger is not asserted.

Note

No matter how many external trigger sources there are, only input trigger 0 and 1 are used. The even numbered channels share the input trigger 0 and the odd numbered channels share the second input trigger 1.

Parameters

<i>base</i>	TPM peripheral base address
<i>chnlNumber</i>	The channel number
<i>enable</i>	true: Configures trigger input 0 or 1 to be used by channel; false: Trigger input has no effect on the channel

35.7.17 void TPM_EnableInterrupts (TPM_Type * *base*, uint32_t *mask*)

Parameters

<i>base</i>	TPM peripheral base address
<i>mask</i>	The interrupts to enable. This is a logical OR of members of the enumeration tpm_interrupt_enable_t

35.7.18 void TPM_DisableInterrupts (TPM_Type * *base*, uint32_t *mask*)

Parameters

<i>base</i>	TPM peripheral base address
<i>mask</i>	The interrupts to disable. This is a logical OR of members of the enumeration tpm_interrupt_enable_t

35.7.19 uint32_t TPM_GetEnabledInterrupts (TPM_Type * *base*)

Parameters

<i>base</i>	TPM peripheral base address
-------------	-----------------------------

Returns

The enabled interrupts. This is the logical OR of members of the enumeration [tpm_interrupt_enable_t](#)

35.7.20 static uint32_t TPM_GetChannelValue (**TPM_Type** * *base*, **tpm_chnl_t chnlNumber**) [inline], [static]

Note

The TPM channel value contain the captured TPM counter value for the input modes or the match value for the output modes.

Parameters

<i>base</i>	TPM peripheral base address
<i>chnlNumber</i>	The channel number

Returns

The channle CnV regisyer value.

35.7.21 static uint32_t TPM_GetStatusFlags (**TPM_Type** * *base*) [inline], [static]

Parameters

<i>base</i>	TPM peripheral base address
-------------	-----------------------------

Returns

The status flags. This is the logical OR of members of the enumeration [tpm_status_flags_t](#)

35.7.22 static void TPM_ClearStatusFlags (**TPM_Type** * *base*, **uint32_t mask**) [inline], [static]

Parameters

<i>base</i>	TPM peripheral base address
<i>mask</i>	The status flags to clear. This is a logical OR of members of the enumeration tpm_status_flags_t

35.7.23 static void TPM_SetTimerPeriod (**TPM_Type** * *base*, **uint32_t** *ticks*) [**inline**], [**static**]

Timers counts from 0 until it equals the count value set here. The count value is written to the MOD register.

Note

1. This API allows the user to use the TPM module as a timer. Do not mix usage of this API with TPM's PWM setup API's.
2. Call the utility macros provided in the `fsl_common.h` to convert usec or msec to ticks.

Parameters

<i>base</i>	TPM peripheral base address
<i>ticks</i>	A timer period in units of ticks, which should be equal or greater than 1.

35.7.24 static **uint32_t** TPM_GetCurrentTimerCount (**TPM_Type** * *base*) [**inline**], [**static**]

This function returns the real-time timer counting value in a range from 0 to a timer period.

Note

Call the utility macros provided in the `fsl_common.h` to convert ticks to usec or msec.

Parameters

<i>base</i>	TPM peripheral base address
-------------	-----------------------------

Returns

The current counter value in ticks

35.7.25 **static void TPM_StartTimer (TPM_Type * *base*, tpm_clock_source_t *clockSource*) [inline], [static]**

Parameters

<i>base</i>	TPM peripheral base address
<i>clockSource</i>	TPM clock source; once clock source is set the counter will start running

35.7.26 static void TPM_StopTimer (TPM_Type * *base*) [inline], [static]

Parameters

<i>base</i>	TPM peripheral base address
-------------	-----------------------------

35.7.27 static void TPM_Reset (TPM_Type * *base*) [inline], [static]

Reset all internal logic and registers, except the Global Register. Remains set until cleared by software.

Note

TPM software reset is available on certain SoC's only

Parameters

<i>base</i>	TPM peripheral base address
-------------	-----------------------------

Chapter 36

TRGMUX: Trigger Mux Driver

36.1 Overview

The MCUXpresso SDK provides driver for the Trigger Mux (TRGMUX) module of MCUXpresso SDK devices.

36.2 Typical use case

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/trgmux

Enumerations

- enum { `kStatus_TRGMUX_Locked` = MAKE_STATUS(kStatusGroup_TRGMUX, 0) }
TRGMUX configure status.
- enum `trgmux_trigger_input_t` {
 `kTRGMUX_TriggerInput0` = TRGMUX_TRGCFG_SEL0_SHIFT,
 `kTRGMUX_TriggerInput1` = TRGMUX_TRGCFG_SEL1_SHIFT,
 `kTRGMUX_TriggerInput2` = TRGMUX_TRGCFG_SEL2_SHIFT,
 `kTRGMUX_TriggerInput3` = TRGMUX_TRGCFG_SEL3_SHIFT }
Defines the MUX select for peripheral trigger input.

Driver version

- #define `FSL_TRGMUX_DRIVER_VERSION` (MAKE_VERSION(2, 0, 1))
TRGMUX driver version.

TRGMUX Functional Operation

- static void `TRGMUX_LockRegister` (TRGMUX_Type *base, uint32_t index)
Sets the flag of the register which is used to mark writeable.
- `status_t TRGMUX_SetTriggerSource` (TRGMUX_Type *base, uint32_t index, `trgmux_trigger_input_t` input, uint32_t trigger_src)
Configures the trigger source of the appointed peripheral.

36.3 Macro Definition Documentation

36.3.1 #define FSL_TRGMUX_DRIVER_VERSION (MAKE_VERSION(2, 0, 1))

36.4 Enumeration Type Documentation

36.4.1 anonymous enum

Enumerator

kStatus(TRGMUX_Locked) Configure failed for register is locked.

36.4.2 enum trgmux_trigger_input_t

Enumerator

- kTRGMUX_TriggerInput0*** The MUX select for peripheral trigger input 0.
- kTRGMUX_TriggerInput1*** The MUX select for peripheral trigger input 1.
- kTRGMUX_TriggerInput2*** The MUX select for peripheral trigger input 2.
- kTRGMUX_TriggerInput3*** The MUX select for peripheral trigger input 3.

36.5 Function Documentation

36.5.1 static void TRGMUX_LockRegister (***TRGMUX_Type * base***, ***uint32_t index***) [inline], [static]

The function sets the flag of the register which is used to mark writeable. Example:

```
TRGMUX_LockRegister(TRGMUX0, kTRGMUX_Trgmux0Dmamux0);
```

Parameters

<i>base</i>	TRGMUX peripheral base address.
<i>index</i>	The index of the TRGMUX register, see the enum trgmux_device_t defined in <SOC>.h.

36.5.2 status_t TRGMUX_SetTriggerSource (***TRGMUX_Type * base***, ***uint32_t index***, ***trgmux_trigger_input_t input***, ***uint32_t trigger_src***)

The function configures the trigger source of the appointed peripheral. Example:

```
TRGMUX_SetTriggerSource(TRGMUX0, kTRGMUX_Trgmux0Dmamux0,
    kTRGMUX_TriggerInput0, kTRGMUX_SourcePortPin);
```

Parameters

<i>base</i>	TRGMUX peripheral base address.
<i>index</i>	The index of the TRGMUX register, see the enum <code>trgmux_device_t</code> defined in <SOC>.h.
<i>input</i>	The MUX select for peripheral trigger input
<i>trigger_src</i>	The trigger inputs for various peripherals. See the enum <code>trgmux_source_t</code> defined in <SOC>.h.

Return values

<i>kStatus_Success</i>	Configured successfully.
<i>kStatus_TRGMUX_Locked</i>	Configuration failed because the register is locked.

Chapter 37

TRNG: True Random Number Generator

The MCUXpresso SDK provides a peripheral driver for the True Random Number Generator (TRNG) module of MCUXpresso SDK devices.

The True Random Number Generator is a hardware accelerator module that generates a 512-bit entropy as needed by an entropy consuming module or by other post processing functions. A typical entropy consumer is a pseudo random number generator (PRNG) which can be implemented to achieve both true randomness and cryptographic strength random numbers using the TRNG output as its entropy seed. The entropy generated by a TRNG is intended for direct use by functions that generate secret keys, per-message secrets, random challenges, and other similar quantities used in cryptographic algorithms.

37.1 TRNG Initialization

1. Define the TRNG user configuration structure. Use `TRNG_InitUserConfigDefault()` function to set it to default TRNG configuration values.
2. Initialize the TRNG module, call the `TRNG_Init()` function, and pass the user configuration structure. This function automatically enables the TRNG module and its clock. After that, the TRNG is enabled and the entropy generation starts working.
3. To disable the TRNG module, call the `TRNG_Deinit()` function.

37.2 Get random data from TRNG

1. `TRNG_GetRandomData()` function gets random data from the TRNG module.

This example code shows how to initialize and get random data from the TRNG driver.

Refer to the driver examples codes located at `<SDK_ROOT>/boards/<BOARD>/driver_examples/trng`

Chapter 38

TSTMR: Timestamp Timer Driver

38.1 Overview

The MCUXpresso SDK provides a driver for the TSTMR module of MCUXpresso SDK devices.

Functions

- static uint64_t [TSTMR_ReadTimeStamp](#) (TSTMR_Type *base)
Reads the time stamp.
- static void [TSTMR_DelayUs](#) (TSTMR_Type *base, uint32_t delayInUs)
Delays for a specified number of microseconds.

Driver version

- #define [FSL_TSTMR_DRIVER_VERSION](#) ([MAKE_VERSION](#)(2, 0, 0))
Version 2.0.0.

38.2 Function Documentation

38.2.1 static uint64_t TSTMR_ReadTimeStamp (**TSTMR_Type * base**) [[inline](#)], [[static](#)]

This function reads the low and high registers and returns the 56-bit free running counter value. This can be read by software at any time to determine the software ticks.

Parameters

<i>base</i>	TSTMR peripheral base address.
-------------	--------------------------------

Returns

The 56-bit time stamp value.

38.2.2 static void TSTMR_DelayUs (**TSTMR_Type * base**, **uint32_t delayInUs**) [[inline](#)], [[static](#)]

This function repeatedly reads the timestamp register and waits for the user-specified delay value.

Parameters

<i>base</i>	TSTMR peripheral base address.
<i>delayInUs</i>	Delay value in microseconds.

Chapter 39

WDOG32: 32-bit Watchdog Timer

39.1 Overview

The MCUXpresso SDK provides a peripheral driver for the WDOG32 module of MCUXpresso SDK devices.

39.2 Typical use case

Refer to the driver examples codes located at <SDK_ROOT>/boards/<BOARD>/driver_examples/wdog32

Data Structures

- struct [wdog32_work_mode_t](#)
Defines WDOG32 work mode. [More...](#)
- struct [wdog32_config_t](#)
Describes WDOG32 configuration structure. [More...](#)

Enumerations

- enum [wdog32_clock_source_t](#) {
 kWDOG32_ClockSource0 = 0U,
 kWDOG32_ClockSource1 = 1U,
 kWDOG32_ClockSource2 = 2U,
 kWDOG32_ClockSource3 = 3U }
Describes WDOG32 clock source.
- enum [wdog32_clock_prescaler_t](#) {
 kWDOG32_ClockPrescalerDivide1 = 0x0U,
 kWDOG32_ClockPrescalerDivide256 = 0x1U }
Describes the selection of the clock prescaler.
- enum [wdog32_test_mode_t](#) {
 kWDOG32_TestModeDisabled = 0U,
 kWDOG32_UserModeEnabled = 1U,
 kWDOG32_LowByteTest = 2U,
 kWDOG32_HighByteTest = 3U }
Describes WDOG32 test mode.
- enum [_wdog32_interrupt_enable_t](#) { kWDOG32_InterruptEnable = WDOG_CS_INT_MASK }
WDOG32 interrupt configuration structure.
- enum [_wdog32_status_flags_t](#) {
 kWDOG32_RunningFlag = WDOG_CS_EN_MASK,
 kWDOG32_InterruptFlag = WDOG_CS_FLG_MASK }
WDOG32 status flags.

Unlock sequence

- #define **WDOG_FIRST_WORD_OF_UNLOCK** (WDOG_UPDATE_KEY & 0xFFFFU)
First word of unlock sequence.
- #define **WDOG_SECOND_WORD_OF_UNLOCK** ((WDOG_UPDATE_KEY >> 16U) & 0xFF-FFU)
Second word of unlock sequence.

Refresh sequence

- #define **WDOG_FIRST_WORD_OF_REFRESH** (WDOG_REFRESH_KEY & 0xFFFFU)
First word of refresh sequence.
- #define **WDOG_SECOND_WORD_OF_REFRESH** ((WDOG_REFRESH_KEY >> 16U) & 0xFF-FFU)
Second word of refresh sequence.

Driver version

- #define **FSL_WDOG32_DRIVER_VERSION** (MAKE_VERSION(2, 0, 4))
WDOG32 driver version.

WDOG32 Initialization and De-initialization

- void **WDOG32_GetDefaultConfig** (wdog32_config_t *config)
Initializes the WDOG32 configuration structure.
- void **WDOG32_Init** (WDOG_Type *base, const wdog32_config_t *config)
Initializes the WDOG32 module.
- void **WDOG32_Deinit** (WDOG_Type *base)
De-initializes the WDOG32 module.

WDOG32 functional Operation

- void **WDOG32_Unlock** (WDOG_Type *base)
Unlocks the WDOG32 register written.
- void **WDOG32_Enable** (WDOG_Type *base)
Enables the WDOG32 module.
- void **WDOG32_Disable** (WDOG_Type *base)
Disables the WDOG32 module.
- void **WDOG32_EnableInterrupts** (WDOG_Type *base, uint32_t mask)
Enables the WDOG32 interrupt.
- void **WDOG32_DisableInterrupts** (WDOG_Type *base, uint32_t mask)
Disables the WDOG32 interrupt.
- static uint32_t **WDOG32_GetStatusFlags** (WDOG_Type *base)
Gets the WDOG32 all status flags.
- void **WDOG32_ClearStatusFlags** (WDOG_Type *base, uint32_t mask)
Clears the WDOG32 flag.
- void **WDOG32_SetTimeoutValue** (WDOG_Type *base, uint16_t timeoutCount)
Sets the WDOG32 timeout value.
- void **WDOG32_SetWindowValue** (WDOG_Type *base, uint16_t windowValue)
Sets the WDOG32 window value.
- static void **WDOG32_Refresh** (WDOG_Type *base)

- static uint16_t [WDOG32_GetCounterValue](#) (WDOG_Type *base)
Gets the WDOG32 counter value.

39.3 Data Structure Documentation

39.3.1 struct wdog32_work_mode_t

Data Fields

- bool [enableWait](#)
Enables or disables WDOG32 in wait mode.
- bool [enableStop](#)
Enables or disables WDOG32 in stop mode.
- bool [enableDebug](#)
Enables or disables WDOG32 in debug mode.

39.3.2 struct wdog32_config_t

Data Fields

- bool [enableWdog32](#)
Enables or disables WDOG32.
- [wdog32_clock_source_t clockSource](#)
Clock source select.
- [wdog32_clock_prescaler_t prescaler](#)
Clock prescaler value.
- [wdog32_work_mode_t workMode](#)
Configures WDOG32 work mode in debug stop and wait mode.
- [wdog32_test_mode_t testMode](#)
Configures WDOG32 test mode.
- bool [enableUpdate](#)
Update write-once register enable.
- bool [enableInterrupt](#)
Enables or disables WDOG32 interrupt.
- bool [enableWindowMode](#)
Enables or disables WDOG32 window mode.
- uint16_t [windowValue](#)
Window value.
- uint16_t [timeoutValue](#)
Timeout value.

39.4 Macro Definition Documentation

39.4.1 #define FSL_WDOG32_DRIVER_VERSION (MAKE_VERSION(2, 0, 4))

39.5 Enumeration Type Documentation

39.5.1 enum wdog32_clock_source_t

Enumerator

- kWDOG32_ClockSource0* Clock source 0.
- kWDOG32_ClockSource1* Clock source 1.
- kWDOG32_ClockSource2* Clock source 2.
- kWDOG32_ClockSource3* Clock source 3.

39.5.2 enum wdog32_clock_prescaler_t

Enumerator

- kWDOG32_ClockPrescalerDivide1* Divided by 1.
- kWDOG32_ClockPrescalerDivide256* Divided by 256.

39.5.3 enum wdog32_test_mode_t

Enumerator

- kWDOG32_TestModeDisabled* Test Mode disabled.
- kWDOG32_UserModeEnabled* User Mode enabled.
- kWDOG32_LowByteTest* Test Mode enabled, only low byte is used.
- kWDOG32_HighByteTest* Test Mode enabled, only high byte is used.

39.5.4 enum _wdog32_interrupt_enable_t

This structure contains the settings for all of the WDOG32 interrupt configurations.

Enumerator

- kWDOG32_InterruptEnable* Interrupt is generated before forcing a reset.

39.5.5 enum _wdog32_status_flags_t

This structure contains the WDOG32 status flags for use in the WDOG32 functions.

Enumerator

- kWDOG32_RunningFlag* Running flag, set when WDOG32 is enabled.
- kWDOG32_InterruptFlag* Interrupt flag, set when interrupt occurs.

39.6 Function Documentation

39.6.1 void WDOG32_GetDefaultConfig (wdog32_config_t * *config*)

This function initializes the WDOG32 configuration structure to default values. The default values are:

```
* wdog32Config->enableWdog32 = true;
* wdog32Config->clockSource = KWDOG32_ClockSource1;
* wdog32Config->prescaler = KWDOG32_ClockPrescalerDivide1;
* wdog32Config->workMode.enableWait = true;
* wdog32Config->workMode.enableStop = false;
* wdog32Config->workMode.enableDebug = false;
* wdog32Config->testMode = KWDOG32_TestModeDisabled;
* wdog32Config->enableUpdate = true;
* wdog32Config->enableInterrupt = false;
* wdog32Config->enableWindowMode = false;
* wdog32Config->>windowValue = 0U;
* wdog32Config->timeoutValue = 0xFFFFU;
*
```

Parameters

<i>config</i>	Pointer to the WDOG32 configuration structure.
---------------	--

See Also

[wdog32_config_t](#)

39.6.2 void WDOG32_Init (WDOG_Type * *base*, const wdog32_config_t * *config*)

This function initializes the WDOG32. To reconfigure the WDOG32 without forcing a reset first, enableUpdate must be set to true in the configuration.

Example:

```
* wdog32_config_t config;
* WDOG32_GetDefaultConfig(&config);
* config.timeoutValue = 0x7ffU;
* config.enableUpdate = true;
* WDOG32_Init(wdog_base,&config);
*
```

Parameters

<i>base</i>	WDOG32 peripheral base address.
<i>config</i>	The configuration of the WDOG32.

39.6.3 void WDOG32_Deinit (WDOG_Type * *base*)

This function shuts down the WDOG32. Ensure that the WDOG_CS.UPDATE is 1, which means that the register update is enabled.

Parameters

<i>base</i>	WDOG32 peripheral base address.
-------------	---------------------------------

39.6.4 void WDOG32_Unlock (WDOG_Type * *base*)

This function unlocks the WDOG32 register written.

Before starting the unlock sequence and following the configuration, disable the global interrupts. Otherwise, an interrupt could effectively invalidate the unlock sequence and the WCT may expire. After the configuration finishes, re-enable the global interrupts.

Parameters

<i>base</i>	WDOG32 peripheral base address
-------------	--------------------------------

39.6.5 void WDOG32_Enable (WDOG_Type * *base*)

This function writes a value into the WDOG_CS register to enable the WDOG32. The WDOG_CS register is a write-once register. Please check the enableUpdate is set to true for calling [WDOG32_Init](#) to do wdog initialize. Before call the re-configuration APIs, ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

<i>base</i>	WDOG32 peripheral base address.
-------------	---------------------------------

39.6.6 void WDOG32_Disable (WDOG_Type * *base*)

This function writes a value into the WDOG_CS register to disable the WDOG32. The WDOG_CS register is a write-once register. Please check the enableUpdate is set to true for calling [WDOG32_Init](#) to

do wdog initialize. Before call the re-configuration APIs, ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

<i>base</i>	WDOG32 peripheral base address
-------------	--------------------------------

39.6.7 void WDOG32_EnableInterrupts (**WDOG_Type** * *base*, **uint32_t** *mask*)

This function writes a value into the WDOG_CS register to enable the WDOG32 interrupt. The WDOG_CS register is a write-once register. Please check the enableUpdate is set to true for calling [WDOG32_Init](#) to do wdog initialize. Before call the re-configuration APIs, ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

<i>base</i>	WDOG32 peripheral base address.
<i>mask</i>	The interrupts to enable. The parameter can be a combination of the following source if defined: <ul style="list-style-type: none">• kWDOG32_InterruptEnable

39.6.8 void WDOG32_DisableInterrupts (**WDOG_Type** * *base*, **uint32_t** *mask*)

This function writes a value into the WDOG_CS register to disable the WDOG32 interrupt. The WDOG_CS register is a write-once register. Please check the enableUpdate is set to true for calling [WDOG32_Init](#) to do wdog initialize. Before call the re-configuration APIs, ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

<i>base</i>	WDOG32 peripheral base address.
<i>mask</i>	The interrupts to disabled. The parameter can be a combination of the following source if defined: <ul style="list-style-type: none">• kWDOG32_InterruptEnable

39.6.9 static uint32_t WDOG32_GetStatusFlags (**WDOG_Type** * *base*) [inline], [static]

This function gets all status flags.

Example to get the running flag:

```
*     uint32_t status;
*     status = WDOG32_GetStatusFlags(wdog_base) &
*             kWDOG32_RunningFlag;
*
```

Parameters

<i>base</i>	WDOG32 peripheral base address
-------------	--------------------------------

Returns

State of the status flag: asserted (true) or not-asserted (false).

See Also

[_wdog32_status_flags_t](#)

- true: related status flag has been set.
- false: related status flag is not set.

39.6.10 void WDOG32_ClearStatusFlags (**WDOG_Type * *base*, **uint32_t** *mask*)**

This function clears the WDOG32 status flag.

Example to clear an interrupt flag:

```
*     WDOG32_ClearStatusFlags(wdog_base,
*                           kWDOG32_InterruptFlag);
*
```

Parameters

<i>base</i>	WDOG32 peripheral base address.
<i>mask</i>	The status flags to clear. The parameter can be any combination of the following values: <ul style="list-style-type: none"> • kWDOG32_InterruptFlag

39.6.11 void WDOG32_SetTimeoutValue (**WDOG_Type * *base*, **uint16_t** *timeoutCount*)**

This function writes a timeout value into the WDOG_TOVAL register. The WDOG_TOVAL register is a write-once register. To ensure the reconfiguration fits the timing of WCT, unlock function will be called inline.

Parameters

<i>base</i>	WDOG32 peripheral base address
<i>timeoutCount</i>	WDOG32 timeout value, count of WDOG32 clock ticks.

39.6.12 void WDOG32_SetWindowValue (WDOG_Type * *base*, uint16_t *windowValue*)

This function writes a window value into the WDOG_WIN register. The WDOG_WIN register is a write-once register. Please check the enableUpdate is set to true for calling [WDOG32_Init](#) to do wdog initialize. Before call the re-configuration APIs, ensure that the WCT window is still open and this register has not been written in this WCT while the function is called.

Parameters

<i>base</i>	WDOG32 peripheral base address.
<i>windowValue</i>	WDOG32 window value.

39.6.13 static void WDOG32_Refresh (WDOG_Type * *base*) [inline], [static]

This function feeds the WDOG32. This function should be called before the Watchdog timer is in timeout. Otherwise, a reset is asserted.

Parameters

<i>base</i>	WDOG32 peripheral base address
-------------	--------------------------------

39.6.14 static uint16_t WDOG32_GetCounterValue (WDOG_Type * *base*) [inline], [static]

This function gets the WDOG32 counter value.

Parameters

<i>base</i>	WDOG32 peripheral base address.
-------------	---------------------------------

Returns

Current WDOG32 counter value.

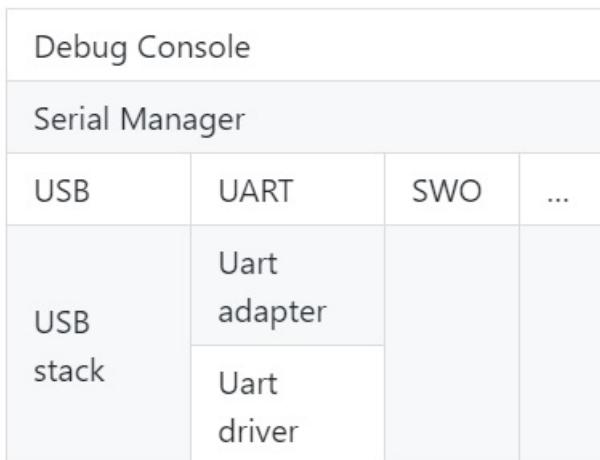
Chapter 40

Debug Console

40.1 Overview

This chapter describes the programming interface of the debug console driver.

The debug console enables debug log messages to be output via the specified peripheral with frequency of the peripheral source clock and base address at the specified baud rate. Additionally, it provides input and output functions to scan and print formatted data. The below picture shows the layout of debug console.



Debug console overview

40.2 Function groups

40.2.1 Initialization

To initialize the debug console, call the [DbgConsole_Init\(\)](#) function with these parameters. This function automatically enables the module and the clock.

```
status_t DbgConsole_Init(uint8_t instance, uint32_t baudRate,  
                         serial_port_type_t device, uint32_t clkSrcFreq);
```

Select the supported debug console hardware device type, such as

```
typedef enum _serial_port_type  
{  
    kSerialPort_Uart = 1U,  
    kSerialPort_UsbCdc,  
    kSerialPort_Swo,  
} serial_port_type_t;
```

After the initialization is successful, stdout and stdin are connected to the selected peripheral. This example shows how to call the [DbgConsole_Init\(\)](#) given the user configuration structure.

```
DbgConsole_Init(BOARD_DEBUG_UART_INSTANCE, BOARD_DEBUG_UART_BAUDRATE, BOARD_DEBUG_UART_TYPE,
                 BOARD_DEBUG_UART_CLK_FREQ);
```

40.2.2 Advanced Feature

The debug console provides input and output functions to scan and print formatted data.

- Support a format specifier for PRINTF following this prototype " %[flags][width][.precision][length]specifier", which is explained below

flags	Description
-	Left-justified within the given field width. Right-justified is the default.
+	Forces to precede the result with a plus or minus sign (+ or -) even for positive numbers. By default, only negative numbers are preceded with a - sign.
(space)	If no sign is written, a blank space is inserted before the value.
#	Used with o, x, or X specifiers the value is preceded with 0, 0x, or 0X respectively for values other than zero. Used with e, E and f, it forces the written output to contain a decimal point even if no digits would follow. By default, if no digits follow, no decimal point is written. Used with g or G the result is the same as with e or E but trailing zeros are not removed.
0	Left-pads the number with zeroes (0) instead of spaces, where padding is specified (see width sub-specifier).

Width	Description
(number)	A minimum number of characters to be printed. If the value to be printed is shorter than this number, the result is padded with blank spaces. The value is not truncated even if the result is larger.
*	The width is not specified in the format string, but as an additional integer value argument preceding the argument that has to be formatted.

.precision	Description
.number	For integer specifiers (d, i, o, u, x, X) precision specifies the minimum number of digits to be written. If the value to be written is shorter than this number, the result is padded with leading zeros. The value is not truncated even if the result is longer. A precision of 0 means that no character is written for the value 0. For e, E, and f specifiers this is the number of digits to be printed after the decimal point. For g and G specifiers This is the maximum number of significant digits to be printed. For s this is the maximum number of characters to be printed. By default, all characters are printed until the ending null character is encountered. For c type it has no effect. When no precision is specified, the default is 1. If the period is specified without an explicit value for precision, 0 is assumed.
.*	The precision is not specified in the format string, but as an additional integer value argument preceding the argument that has to be formatted.

length	Description
Do not support	

specifier	Description
d or i	Signed decimal integer
f	Decimal floating point
F	Decimal floating point capital letters
x	Unsigned hexadecimal integer
X	Unsigned hexadecimal integer capital letters
o	Signed octal
b	Binary value
p	Pointer address
u	Unsigned decimal integer
c	Character
s	String of characters
n	Nothing printed

- Support a format specifier for SCANF following this prototype " %[*][width][length]specifier", which is explained below

*	Description
An optional starting asterisk indicates that the data is to be read from the stream but ignored. In other words, it is not stored in the corresponding argument.	

width	Description
This specifies the maximum number of characters to be read in the current reading operation.	

length	Description
hh	The argument is interpreted as a signed character or unsigned character (only applies to integer specifiers: i, d, o, u, x, and X).
h	The argument is interpreted as a short integer or unsigned short integer (only applies to integer specifiers: i, d, o, u, x, and X).
l	The argument is interpreted as a long integer or unsigned long integer for integer specifiers (i, d, o, u, x, and X) and as a wide character or wide character string for specifiers c and s.
ll	The argument is interpreted as a long long integer or unsigned long long integer for integer specifiers (i, d, o, u, x, and X) and as a wide character or wide character string for specifiers c and s.
L	The argument is interpreted as a long double (only applies to floating point specifiers: e, E, f, g, and G).
j or z or t	Not supported

specifier	Qualifying Input	Type of argument
c	Single character: Reads the next character. If a width different from 1 is specified, the function reads width characters and stores them in the successive locations of the array passed as argument. No null character is appended at the end.	char *
i	Integer: : Number optionally preceded with a + or - sign	int *
d	Decimal integer: Number optionally preceded with a + or - sign	int *
a, A, e, E, f, F, g, G	Floating point: Decimal number containing a decimal point, optionally preceded by a + or - sign and optionally followed by the e or E character and a decimal number. Two examples of valid entries are -732.103 and 7.12e4	float *
o	Octal Integer:	int *
s	String of characters. This reads subsequent characters until a white space is found (white space characters are considered to be blank, newline, and tab).	char *
u	Unsigned decimal integer.	unsigned int *

The debug console has its own printf/scanf/putchar/getchar functions which are defined in the header file.

```
int DbgConsole_Printf(const char *fmt_s, ...);
int DbgConsole_Putchar(int ch);
int DbgConsole_Scanf(char *fmt_ptr, ...);
int DbgConsole_Getchar(void);
```

This utility supports selecting toolchain's printf/scanf or the MCUXpresso SDK printf/scanf.

```
#if SDK_DEBUGCONSOLE == DEBUGCONSOLE_DISABLE /* Disable debug console */
#define PRINTF
#define SCANF
#define PUTCHAR
#define GETCHAR
#elif SDK_DEBUGCONSOLE == DEBUGCONSOLE_REDIRECT_TO_SDK /* Select printf, scanf, putchar, getchar of SDK
```

```

version. */
#define PRINTF DbgConsole_Printf
#define SCANF DbgConsole_Scanf
#define PUTCHAR DbgConsole_Putchar
#define GETCHAR DbgConsole_Getchar
#elif SDK_DEBUGCONSOLE == DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN /* Select printf, scanf, putchar, getchar of
toolchain. */
#define PRINTF printf
#define SCANF scanf
#define PUTCHAR putchar
#define GETCHAR getchar
#endif /* SDK_DEBUGCONSOLE */

```

40.2.3 SDK_DEBUGCONSOLE and SDK_DEBUGCONSOLE_UART

There are two macros `SDK_DEBUGCONSOLE` and `SDK_DEBUGCONSOLE_UART` added to configure `PRINTF` and low level output peripheral.

- The macro `SDK_DEBUGCONSOLE` is used for frontend. Whether debug console redirect to toolchain or SDK or disabled, it decides which is the frontend of the debug console, Tool chain or SDK. The function can be set by the macro `SDK_DEBUGCONSOLE`.
- The macro `SDK_DEBUGCONSOLE_UART` is used for backend. It is used to decide whether provide low level IO implementation to toolchain printf and scanf. For example, within MCUXpresso, if the macro `SDK_DEBUGCONSOLE_UART` is defined, `_sys_write` and `_sys_read` will be used when `_REDLIB_` is defined; `_write` and `_read` will be used in other cases. The macro does not specifically refer to the peripheral "UART". It refers to the external peripheral similar to UART, like as USB CDC, UART, SWO, etc. So if the macro `SDK_DEBUGCONSOLE_UART` is not defined when tool-chain printf is calling, the semihosting will be used.

The following matrix show the effects of `SDK_DEBUGCONSOLE` and `SDK_DEBUGCONSOLE_UART` on `PRINTF` and `printf`. The green mark is the default setting of the debug console.

<code>SDK_DEBUGCONSOLE</code>	<code>SDK_DEBUGCONSOLE_UART</code>	<code>PRINTF</code>	<code>printf</code>
<code>DEBUGCONSOLE_- REDIRECT_TO_SDK</code>	defined	Low level peripheral*	Low level peripheral
<code>DEBUGCONSOLE_- REDIRECT_TO_SDK</code>	undefined	Low level peripheral*	semihost
<code>DEBUGCONSOLE_- REDIRECT_TO_TO- OLCHAIN</code>	defined	Low level peripheral*	Low level peripheral
<code>DEBUGCONSOLE_- REDIRECT_TO_TO- OLCHAIN</code>	undefined	semihost	semihost
<code>DEBUGCONSOLE_- DISABLE</code>	defined	No output	Low level peripheral
<code>DEBUGCONSOLE_- DISABLE</code>	undefined	No output	semihost

- * the **low level peripheral** could be USB CDC, UART, or SWO, and so on.

40.3 Typical use case

Some examples use the PUTCHAR & GETCHAR function

```
ch = GETCHAR();
PUTCHAR(ch);
```

Some examples use the PRINTF function

Statement prints the string format.

```
PRINTF("%s %s\r\n", "Hello", "world!");
```

Statement prints the hexadecimal format/

```
PRINTF("0x%02X hexadecimal number equivalents 255", 255);
```

Statement prints the decimal floating point and unsigned decimal.

```
PRINTF("Execution timer: %s\n\rTime: %u ticks %2.5f milliseconds\n\rDONE\n\r", "1 day", 86400, 86.4);
```

Some examples use the SCANF function

```
PRINTF("Enter a decimal number: ");
SCANF("%d", &i);
PRINTF("\r\nYou have entered %d.\r\n", i, i);
PRINTF("Enter a hexadecimal number: ");
SCANF("%x", &i);
PRINTF("\r\nYou have entered 0x%X (%d).\r\n", i, i);
```

Print out failure messages using MCUXpresso SDK __assert_func:

```
void __assert_func(const char *file, int line, const char *func, const char *failedExpr)
{
    PRINTF("ASSERT ERROR \" %s \": file \"%s\" Line \"%d\" function name \"%s\" \n", failedExpr, file
          , line, func);
    for (;;) {}
}
```

Note:

To use 'printf' and 'scanf' for GNUC Base, add file '**fsl_sbrk.c**' in path: ..\{package}\devices\{subset}\utilities\fsl_sbrk.c to your project.

Macros

- `#define DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN 0U`
Definition select redirect toolchain printf, scanf to uart or not.
- `#define DEBUGCONSOLE_REDIRECT_TO_SDK 1U`
Select SDK version printf, scanf.
- `#define DEBUGCONSOLE_DISABLE 2U`
Disable debugconsole function.
- `#define SDK_DEBUGCONSOLE DEBUGCONSOLE_REDIRECT_TO_SDK`
Definition to select sdk or toolchain printf, scanf.
- `#define PRINTF DbgConsole_Printf`
Definition to select redirect toolchain printf, scanf to uart or not.

Typedefs

- `typedef void(* printfCb)(char *buf, int32_t *indicator, char val, int len)`
A function pointer which is used when format printf log.

Functions

- `int StrFormatPrintf (const char *fmt, va_list ap, char *buf, printfCb cb)`
This function outputs its parameters according to a formatted string.
- `int StrFormatScanf (const char *line_ptr, char *format, va_list args_ptr)`
Converts an input line of ASCII characters based upon a provided string format.

Variables

- `serial_handle_t g_serialHandle`
serial manager handle

Initialization

- `status_t DbgConsole_Init (uint8_t instance, uint32_t baudRate, serial_port_type_t device, uint32_t clkSrcFreq)`
Initializes the peripheral used for debug messages.
- `status_t DbgConsole_Deinit (void)`
De-initializes the peripheral used for debug messages.
- `status_t DbgConsole_EnterLowpower (void)`
Prepares to enter low power consumption.
- `status_t DbgConsole_ExitLowpower (void)`
Restores from low power consumption.
- `int DbgConsole_Printf (const char *fmt_s,...)`
Writes formatted output to the standard output stream.
- `int DbgConsole_Vprintf (const char *fmt_s, va_list formatStringArg)`
Writes formatted output to the standard output stream.
- `int DbgConsole_Putchar (int ch)`
Writes a character to stdout.
- `int DbgConsole_Scanf (char *fmt_s,...)`
Reads formatted data from the standard input stream.
- `int DbgConsole_Getchar (void)`
Reads a character from standard input.

- int `DbgConsole_BlockingPrintf` (const char *fmt_s,...)
Writes formatted output to the standard output stream with the blocking mode.
- int `DbgConsole_BlockingVprintf` (const char *fmt_s, va_list formatStringArg)
Writes formatted output to the standard output stream with the blocking mode.
- status_t `DbgConsole_Flush` (void)
Debug console flush.

40.4 Macro Definition Documentation

40.4.1 #define DEBUGCONSOLE_REDIRECT_TO_TOOLCHAIN 0U

Select toolchain printf and scanf.

40.4.2 #define DEBUGCONSOLE_REDIRECT_TO_SDK 1U

40.4.3 #define DEBUGCONSOLE_DISABLE 2U

40.4.4 #define SDK_DEBUGCONSOLE DEBUGCONSOLE_REDIRECT_TO_SDK

The macro only support to be redefined in project setting.

40.4.5 #define PRINTF DbgConsole_Printf

if SDK_DEBUGCONSOLE defined to 0,it represents select toolchain printf, scanf. if SDK_DEBUGCONSOLE defined to 1,it represents select SDK version printf, scanf. if SDK_DEBUGCONSOLE defined to 2,it represents disable debugconsole function.

40.5 Function Documentation

40.5.1 status_t DbgConsole_Init (uint8_t instance, uint32_t baudRate, serial_port_type_t device, uint32_t clkSrcFreq)

Call this function to enable debug log messages to be output via the specified peripheral initialized by the serial manager module. After this function has returned, stdout and stdin are connected to the selected peripheral.

Parameters

<i>instance</i>	The instance of the module. If the device is kSerialPort_Uart, the instance is UART peripheral instance. The UART hardware peripheral type is determined by UART adapter. For example, if the instance is 1, if the lpuart_adapter.c is added to the current project, the UART peripheral is LPUART1. If the uart_adapter.c is added to the current project, the UART peripheral is UART1.
<i>baudRate</i>	The desired baud rate in bits per second.
<i>device</i>	Low level device type for the debug console, can be one of the following. <ul style="list-style-type: none"> • kSerialPort_Uart, • kSerialPort_UsbCdc
<i>clkSrcFreq</i>	Frequency of peripheral source clock.

Returns

Indicates whether initialization was successful or not.

Return values

<i>kStatus_Success</i>	Execution successfully
------------------------	------------------------

40.5.2 status_t DbgConsole_Deinit (void)

Call this function to disable debug log messages to be output via the specified peripheral initialized by the serial manager module.

Returns

Indicates whether de-initialization was successful or not.

40.5.3 status_t DbgConsole_EnterLowpower (void)

This function is used to prepare to enter low power consumption.

Returns

Indicates whether de-initialization was successful or not.

40.5.4 status_t DbgConsole_ExitLowpower (void)

This function is used to restore from low power consumption.

Returns

Indicates whether de-initialization was successful or not.

40.5.5 int DbgConsole_Printf (const char * *fmt_s*, ...)

Call this function to write a formatted output to the standard output stream.

Parameters

<i>fmt_s</i>	Format control string.
--------------	------------------------

Returns

Returns the number of characters printed or a negative value if an error occurs.

40.5.6 int DbgConsole_Vprintf (const char * *fmt_s*, va_list *formatStringArg*)

Call this function to write a formatted output to the standard output stream.

Parameters

<i>fmt_s</i>	Format control string.
<i>formatString-Arg</i>	Format arguments.

Returns

Returns the number of characters printed or a negative value if an error occurs.

40.5.7 int DbgConsole_Putchar (int *ch*)

Call this function to write a character to stdout.

Parameters

<i>ch</i>	Character to be written.
-----------	--------------------------

Returns

Returns the character written.

40.5.8 int DbgConsole_Scanf (char * *fmt_s*, ...)

Call this function to read formatted data from the standard input stream.

Note

Due the limitation in the BM OSA environment (CPU is blocked in the function, other tasks will not be scheduled), the function cannot be used when the DEBUG_CONSOLE_TRANSFER_NON_B-LOCKING is set in the BM OSA environment. And an error is returned when the function called in this case. The suggestion is that polling the non-blocking function DbgConsole_TryGetchar to get the input char.

Parameters

<i>fmt_s</i>	Format control string.
--------------	------------------------

Returns

Returns the number of fields successfully converted and assigned.

40.5.9 int DbgConsole_Getchar (void)

Call this function to read a character from standard input.

Note

Due the limitation in the BM OSA environment (CPU is blocked in the function, other tasks will not be scheduled), the function cannot be used when the DEBUG_CONSOLE_TRANSFER_NON_B-LOCKING is set in the BM OSA environment. And an error is returned when the function called in this case. The suggestion is that polling the non-blocking function DbgConsole_TryGetchar to get the input char.

Returns

Returns the character read.

40.5.10 int DbgConsole_BlockingPrintf (const char * *fmt_s*, ...)

Call this function to write a formatted output to the standard output stream with the blocking mode. The function will send data with blocking mode no matter the DEBUG_CONSOLE_TRANSFER_NON_BLOCKING set or not. The function could be used in system ISR mode with DEBUG_CONSOLE_TRANSFER_NON_BLOCKING set.

Parameters

<i>fmt_s</i>	Format control string.
--------------	------------------------

Returns

Returns the number of characters printed or a negative value if an error occurs.

40.5.11 int DbgConsole_BlockingVprintf (const char * *fmt_s*, va_list *formatStringArg*)

Call this function to write a formatted output to the standard output stream with the blocking mode. The function will send data with blocking mode no matter the DEBUG_CONSOLE_TRANSFER_NON_BLOCKING set or not. The function could be used in system ISR mode with DEBUG_CONSOLE_TRANSFER_NON_BLOCKING set.

Parameters

<i>fmt_s</i>	Format control string.
<i>formatString-Arg</i>	Format arguments.

Returns

Returns the number of characters printed or a negative value if an error occurs.

40.5.12 status_t DbgConsole_Flush (void)

Call this function to wait the tx buffer empty. If interrupt transfer is using, make sure the global IRQ is enable before call this function This function should be called when 1, before enter power down mode 2, log is required to print to terminal immediately

Returns

Indicates whether wait idle was successful or not.

40.5.13 int StrFormatPrintf (const char * *fmt*, va_list *ap*, char * *buf*, printfCb *cb*)

Note

I/O is performed by calling given function pointer using following (*func_ptr)(c);

Parameters

in	<i>fmt</i>	Format string for printf.
in	<i>ap</i>	Arguments to printf.
in	<i>buf</i>	pointer to the buffer
	<i>cb</i>	print callbk function pointer

Returns

Number of characters to be print

40.5.14 int StrFormatScanf (const char * *line_ptr*, char * *format*, va_list *args_ptr*)

Parameters

in	<i>line_ptr</i>	The input line of ASCII data.
in	<i>format</i>	Format first points to the format string.
in	<i>args_ptr</i>	The list of parameters.

Returns

Number of input items converted and assigned.

Return values

<i>IO_EOF</i>	When line_ptr is empty string "".
---------------	-----------------------------------

Chapter 41

Notification Framework

41.1 Overview

This section describes the programming interface of the Notifier driver.

41.2 Notifier Overview

The Notifier provides a configuration dynamic change service. Based on this service, applications can switch between pre-defined configurations. The Notifier enables drivers and applications to register callback functions to this framework. Each time that the configuration is changed, drivers and applications receive a notification and change their settings. To simplify, the Notifier only supports the static callback registration. This means that, for applications, all callback functions are collected into a static table and passed to the Notifier.

These are the steps for the configuration transition.

1. Before configuration transition, the Notifier sends a "BEFORE" message to the callback table. When this message is received, IP drivers should check whether any current processes can be stopped and stop them. If the processes cannot be stopped, the callback function returns an error.
The Notifier supports two types of transition policies, a graceful policy and a forceful policy. When the graceful policy is used, if some callbacks return an error while sending a "BEFORE" message, the configuration transition stops and the Notifier sends a "RECOVER" message to all drivers that have stopped. Then, these drivers can recover the previous status and continue to work. When the forceful policy is used, drivers are stopped forcefully.
2. After the "BEFORE" message is processed successfully, the system switches to the new configuration.
3. After the configuration changes, the Notifier sends an "AFTER" message to the callback table to notify drivers that the configuration transition is finished.

This example shows how to use the Notifier in the Power Manager application.

```
#include "fsl_notifier.h"

// Definition of the Power Manager callback.
status_t callback0(notifier_notification_block_t *notify, void *data)
{
    status_t ret = kStatus_Success;

    ...
    ...

    return ret;
}
// Definition of the Power Manager user function.
status_t APP_PowerModeSwitch(notifier_user_config_t *targetConfig, void *
    userData)
```

```

{
    ...
    ...
    ...
}

...
...
...
...
...
...
// Main function.
int main(void)
{
    // Define a notifier handle.
    notifier_handle_t powerModeHandle;

    // Callback configuration.
    user_callback_data_t callbackData0;

    notifier_callback_config_t callbackCfg0 = {callback0,
        kNOTIFIER_CallbackBeforeAfter,
        (void *)&callbackData0};

    notifier_callback_config_t callbacks[] = {callbackCfg0};

    // Power mode configurations.
    power_user_config_t vlprConfig;
    power_user_config_t stopConfig;

    notifier_user_config_t *powerConfigs[] = {&vlprConfig, &stopConfig};

    // Definition of a transition to and out the power modes.
    vlprConfig.mode = kAPP_PowerModeVlpr;
    vlprConfig.enableLowPowerWakeUpOnInterrupt = false;

    stopConfig = vlprConfig;
    stopConfig.mode = kAPP_PowerModeStop;

    // Create Notifier handle.
    NOTIFIER_CreateHandle(&powerModeHandle, powerConfigs, 2U, callbacks, 1U,
        APP_PowerModeSwitch, NULL);
    ...

    ...
    // Power mode switch.
    NOTIFIER_switchConfig(&powerModeHandle, targetConfigIndex,
        kNOTIFIER_PolicyAgreement);
}

```

Data Structures

- struct [notifier_notification_block_t](#)
notification block passed to the registered callback function. [More...](#)
- struct [notifier_callback_config_t](#)
Callback configuration structure. [More...](#)
- struct [notifier_handle_t](#)
Notifier handle structure. [More...](#)

Typedefs

- [typedef void notifier_user_config_t](#)
Notifier user configuration type.
- [typedef status_t\(* notifier_user_function_t \)\(notifier_user_config_t *targetConfig, void *userData\)](#)

- *Notifier user function prototype Use this function to execute specific operations in configuration switch.*
typedef status_t(* notifier_callback_t)(notifier_notification_block_t *notify, void *data)
Callback prototype.

Enumerations

- **enum _notifier_status {**
kStatus_NOTIFIER_ErrorNotificationBefore,
kStatus_NOTIFIER_ErrorNotificationAfter }
Notifier error codes.
- **enum notifier_policy_t {**
kNOTIFIER_PolicyAgreement,
kNOTIFIER_PolicyForcible }
Notifier policies.
- **enum notifier_notification_type_t {**
kNOTIFIER_NotifyRecover = 0x00U,
kNOTIFIER_NotifyBefore = 0x01U,
kNOTIFIER_NotifyAfter = 0x02U }
Notification type.
- **enum notifier_callback_type_t {**
kNOTIFIER_CallbackBefore = 0x01U,
kNOTIFIER_CallbackAfter = 0x02U,
kNOTIFIER_CallbackBeforeAfter = 0x03U }
The callback type, which indicates kinds of notification the callback handles.

Functions

- **status_t NOTIFIER_CreateHandle (notifier_handle_t *notifierHandle, notifier_user_config_t **configs, uint8_t configsNumber, notifier_callback_config_t *callbacks, uint8_t callbacksNumber, notifier_user_function_t userFunction, void *userData)**
Creates a Notifier handle.
- **status_t NOTIFIER_SwitchConfig (notifier_handle_t *notifierHandle, uint8_t configIndex, notifier_policy_t policy)**
Switches the configuration according to a pre-defined structure.
- **uint8_t NOTIFIER_GetErrorCallbackIndex (notifier_handle_t *notifierHandle)**
This function returns the last failed notification callback.

41.3 Data Structure Documentation

41.3.1 struct notifier_notification_block_t

Data Fields

- **notifier_user_config_t * targetConfig**
Pointer to target configuration.
- **notifier_policy_t policy**
Configure transition policy.
- **notifier_notification_type_t notifyType**

Configure notification type.

Field Documentation

- (1) **notifier_user_config_t* notifier_notification_block_t::targetConfig**
- (2) **notifier_policy_t notifier_notification_block_t::policy**
- (3) **notifier_notification_type_t notifier_notification_block_t::notifyType**

41.3.2 struct notifier_callback_config_t

This structure holds the configuration of callbacks. Callbacks of this type are expected to be statically allocated. This structure contains the following application-defined data. callback - pointer to the callback function callbackType - specifies when the callback is called callbackData - pointer to the data passed to the callback.

Data Fields

- **notifier_callback_t callback**
Pointer to the callback function.
- **notifier_callback_type_t callbackType**
Callback type.
- **void * callbackData**
Pointer to the data passed to the callback.

Field Documentation

- (1) **notifier_callback_t notifier_callback_config_t::callback**
- (2) **notifier_callback_type_t notifier_callback_config_t::callbackType**
- (3) **void* notifier_callback_config_t::callbackData**

41.3.3 struct notifier_handle_t

Notifier handle structure. Contains data necessary for the Notifier proper function. Stores references to registered configurations, callbacks, information about their numbers, user function, user data, and other internal data. [NOTIFIER_CreateHandle\(\)](#) must be called to initialize this handle.

Data Fields

- **notifier_user_config_t ** configsTable**
Pointer to configure table.
- **uint8_t configsNumber**
Number of configurations.

- `notifier_callback_config_t * callbacksTable`
Pointer to callback table.
- `uint8_t callbacksNumber`
Maximum number of callback configurations.
- `uint8_t errorCallbackIndex`
Index of callback returns error.
- `uint8_t currentConfigIndex`
Index of current configuration.
- `notifier_user_function_t userFunction`
User function.
- `void * userData`
User data passed to user function.

Field Documentation

- (1) `notifier_user_config_t** notifier_handle_t::configsTable`
- (2) `uint8_t notifier_handle_t::configsNumber`
- (3) `notifier_callback_config_t* notifier_handle_t::callbacksTable`
- (4) `uint8_t notifier_handle_t::callbacksNumber`
- (5) `uint8_t notifier_handle_t::errorCallbackIndex`
- (6) `uint8_t notifier_handle_t::currentConfigIndex`
- (7) `notifier_user_function_t notifier_handle_t::userFunction`
- (8) `void* notifier_handle_t::userData`

41.4 Typedef Documentation

41.4.1 `typedef void notifier_user_config_t`

Reference of the user defined configuration is stored in an array; the notifier switches between these configurations based on this array.

41.4.2 `typedef status_t(* notifier_user_function_t)(notifier_user_config_t *targetConfig, void *userData)`

Before and after this function execution, different notification is sent to registered callbacks. If this function returns any error code, `NOTIFIER_SwitchConfig()` exits.

Parameters

<i>targetConfig</i>	target Configuration.
<i>userData</i>	Refers to other specific data passed to user function.

Returns

An error code or kStatus_Success.

41.4.3 **typedef status_t(* notifier_callback_t)(notifier_notification_block_t *notify, void *data)**

Declaration of a callback. It is common for registered callbacks. Reference to function of this type is part of the [notifier_callback_config_t](#) callback configuration structure. Depending on callback type, function of this prototype is called (see [NOTIFIER_SwitchConfig\(\)](#)) before configuration switch, after it or in both use cases to notify about the switch progress (see [notifier_callback_type_t](#)). When called, the type of the notification is passed as a parameter along with the reference to the target configuration structure (see [notifier_notification_block_t](#)) and any data passed during the callback registration. When notified before the configuration switch, depending on the configuration switch policy (see [notifier_policy_t](#)), the callback may deny the execution of the user function by returning an error code different than kStatus_Success (see [NOTIFIER_SwitchConfig\(\)](#)).

Parameters

<i>notify</i>	Notification block.
<i>data</i>	Callback data. Refers to the data passed during callback registration. Intended to pass any driver or application data such as internal state information.

Returns

An error code or kStatus_Success.

41.5 Enumeration Type Documentation

41.5.1 enum _notifier_status

Used as return value of Notifier functions.

Enumerator

kStatus_NOTIFIER_ErrorNotificationBefore An error occurs during send "BEFORE" notification.

kStatus_NOTIFIER_ErrorNotificationAfter An error occurs during send "AFTER" notification.

41.5.2 enum notifier_policy_t

Defines whether the user function execution is forced or not. For `kNOTIFIER_PolicyForcible`, the user function is executed regardless of the callback results, while `kNOTIFIER_PolicyAgreement` policy is used to exit `NOTIFIER_SwitchConfig()` when any of the callbacks returns error code. See also `NOTIFIER_SwitchConfig()` description.

Enumerator

kNOTIFIER_PolicyAgreement `NOTIFIER_SwitchConfig()` method is exited when any of the callbacks returns error code.

kNOTIFIER_PolicyForcible The user function is executed regardless of the results.

41.5.3 enum notifier_notification_type_t

Used to notify registered callbacks

Enumerator

kNOTIFIER_NotifyRecover Notify IP to recover to previous work state.

kNOTIFIER_NotifyBefore Notify IP that configuration setting is going to change.

kNOTIFIER_NotifyAfter Notify IP that configuration setting has been changed.

41.5.4 enum notifier_callback_type_t

Used in the callback configuration structure (`notifier_callback_config_t`) to specify when the registered callback is called during configuration switch initiated by the `NOTIFIER_SwitchConfig()`. Callback can be invoked in following situations.

- Before the configuration switch (Callback return value can affect `NOTIFIER_SwitchConfig()` execution. See the `NOTIFIER_SwitchConfig()` and `notifier_policy_t` documentation).
- After an unsuccessful attempt to switch configuration
- After a successful configuration switch

Enumerator

kNOTIFIER_CallbackBefore Callback handles BEFORE notification.

kNOTIFIER_CallbackAfter Callback handles AFTER notification.

kNOTIFIER_CallbackBeforeAfter Callback handles BEFORE and AFTER notification.

41.6 Function Documentation

41.6.1 **status_t NOTIFIER_CreateHandle (notifier_handle_t * *notifierHandle*,
notifier_user_config_t ** *configs*, uint8_t *configsNumber*, notifier_callback-
_config_t * *callbacks*, uint8_t *callbacksNumber*, notifier_user_function_t
userFunction, void * *userData*)**

Parameters

<i>notifierHandle</i>	A pointer to the notifier handle.
<i>configs</i>	A pointer to an array with references to all configurations which is handled by the Notifier.
<i>configsNumber</i>	Number of configurations. Size of the configuration array.
<i>callbacks</i>	A pointer to an array of callback configurations. If there are no callbacks to register during Notifier initialization, use NULL value.
<i>callbacks-Number</i>	Number of registered callbacks. Size of the callbacks array.
<i>userFunction</i>	User function.
<i>userData</i>	User data passed to user function.

Returns

An error Code or kStatus_Success.

41.6.2 **status_t NOTIFIER_SwitchConfig (notifier_handle_t * *notifierHandle*, uint8_t *configIndex*, notifier_policy_t *policy*)**

This function sets the system to the target configuration. Before transition, the Notifier sends notifications to all callbacks registered to the callback table. Callbacks are invoked in the following order: All registered callbacks are notified ordered by index in the callbacks array. The same order is used for before and after switch notifications. The notifications before the configuration switch can be used to obtain confirmation about the change from registered callbacks. If any registered callback denies the configuration change, further execution of this function depends on the notifier policy: the configuration change is either forced (kNOTIFIER_PolicyForcible) or exited (kNOTIFIER_PolicyAgreement). When configuration change is forced, the result of the before switch notifications are ignored. If an agreement is required, if any callback returns an error code, further notifications before switch notifications are cancelled and all already notified callbacks are re-invoked. The index of the callback which returned error code during pre-switch notifications is stored (any error codes during callbacks re-invocation are ignored) and NOTIFIER_GetErrorCallback() can be used to get it. Regardless of the policies, if any callback returns an error code, an error code indicating in which phase the error occurred is returned when NOTIFIER_SwitchConfig() exits.

Parameters

<i>notifierHandle</i>	pointer to notifier handle
<i>configIndex</i>	Index of the target configuration.
<i>policy</i>	Transaction policy, kNOTIFIER_PolicyAgreement or kNOTIFIER_PolicyForcible.

Returns

An error code or kStatus_Success.

41.6.3 **uint8_t NOTIFIER_GetErrorCallbackIndex (notifier_handle_t * *notifierHandle*)**

This function returns an index of the last callback that failed during the configuration switch while the last [NOTIFIER_SwitchConfig\(\)](#) was called. If the last [NOTIFIER_SwitchConfig\(\)](#) call ended successfully value equal to callbacks number is returned. The returned value represents an index in the array of static call-backs.

Parameters

<i>notifierHandle</i>	Pointer to the notifier handle
-----------------------	--------------------------------

Returns

Callback Index of the last failed callback or value equal to callbacks count.

Chapter 42

Shell

42.1 Overview

This section describes the programming interface of the Shell middleware.

Shell controls MCUs by commands via the specified communication peripheral based on the debug console driver.

42.2 Function groups

42.2.1 Initialization

To initialize the Shell middleware, call the `SHELL_Init()` function with these parameters. This function automatically enables the middleware.

```
shell_status_t SHELL_Init(shell_handle_t shellHandle,  
    serial_handle_t serialHandle, char *prompt);
```

Then, after the initialization was successful, call a command to control MCUs.

This example shows how to call the `SHELL_Init()` given the user configuration structure.

```
SHELL_Init(s_shellHandle, s_serialHandle, "Test@SHELL>");
```

42.2.2 Advanced Feature

- Support to get a character from standard input devices.

```
static shell_status_t SHELL_GetChar(shell_context_handle_t *shellContextHandle, uint8_t *ch);
```

Commands	Description
help	List all the registered commands.
exit	Exit program.

42.2.3 Shell Operation

```
SHELL_Init(s_shellHandle, s_serialHandle, "Test@SHELL>");  
SHELL_Task(s_shellHandle);
```

Data Structures

- struct `shell_command_t`
User command data configuration structure. More...

Macros

- #define `SHELL_NON_BLOCKING_MODE SERIAL_MANAGER_NON_BLOCKING_MODE`
Whether use non-blocking mode.
- #define `SHELL_AUTO_COMPLETE` (1U)
Macro to set on/off auto-complete feature.
- #define `SHELL_BUFFER_SIZE` (64U)
Macro to set console buffer size.
- #define `SHELL_MAX_ARGS` (8U)
Macro to set maximum arguments in command.
- #define `SHELL_HISTORY_COUNT` (3U)
Macro to set maximum count of history commands.
- #define `SHELL_IGNORE_PARAMETER_COUNT` (0xFF)
Macro to bypass arguments check.
- #define `SHELL_HANDLE_SIZE`
The handle size of the shell module.
- #define `SHELL_USE_COMMON_TASK` (0U)
Macro to determine whether use common task.
- #define `SHELL_TASK_PRIORITY` (2U)
Macro to set shell task priority.
- #define `SHELL_TASK_STACK_SIZE` (1000U)
Macro to set shell task stack size.
- #define `SHELL_HANDLE_DEFINE`(name) uint32_t name[((`SHELL_HANDLE_SIZE` + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]
Defines the shell handle.
- #define `SHELL_COMMAND_DEFINE`(command, descriptor, callback, paramInt)
Defines the shell command structure.
- #define `SHELL_COMMAND`(command) &g_shellCommand##command
Gets the shell command pointer.

Typedefs

- typedef void * `shell_handle_t`
The handle of the shell module.
- typedef `shell_status_t`(* `cmd_function_t`)(`shell_handle_t` shellHandle, int32_t argc, char **argv)
User command function prototype.

Enumerations

- enum `shell_status_t` {

`kStatus_SHELL_Success` = kStatus_Success,

`kStatus_SHELL_Error` = MAKE_STATUS(kStatusGroup_SHELL, 1),

`kStatus_SHELL_OpenWriteHandleFailed` = MAKE_STATUS(kStatusGroup_SHELL, 2),

`kStatus_SHELL_OpenReadHandleFailed` = MAKE_STATUS(kStatusGroup_SHELL, 3) }

Shell status.

Shell functional operation

- `shell_status_t SHELL_Init (shell_handle_t shellHandle, serial_handle_t serialHandle, char *prompt)`
Initializes the shell module.
- `shell_status_t SHELL_RegisterCommand (shell_handle_t shellHandle, shell_command_t *shellCommand)`
Registers the shell command.
- `shell_status_t SHELL_UnregisterCommand (shell_command_t *shellCommand)`
Unregisters the shell command.
- `shell_status_t SHELL_Write (shell_handle_t shellHandle, const char *buffer, uint32_t length)`
Sends data to the shell output stream.
- `int SHELL_Printf (shell_handle_t shellHandle, const char *formatString,...)`
Writes formatted output to the shell output stream.
- `shell_status_t SHELL_WriteSynchronization (shell_handle_t shellHandle, const char *buffer, uint32_t length)`
Sends data to the shell output stream with OS synchronization.
- `int SHELL_PrintfSynchronization (shell_handle_t shellHandle, const char *formatString,...)`
Writes formatted output to the shell output stream with OS synchronization.
- `void SHELL_ChangePrompt (shell_handle_t shellHandle, char *prompt)`
Change shell prompt.
- `void SHELL_PrintPrompt (shell_handle_t shellHandle)`
Print shell prompt.
- `void SHELL_Task (shell_handle_t shellHandle)`
The task function for Shell.
- `static bool SHELL_checkRunningInIsr (void)`
Check if code is running in ISR.

42.3 Data Structure Documentation

42.3.1 struct shell_command_t

Data Fields

- `const char * pcCommand`
The command that is executed.
- `char * pcHelpString`
String that describes how to use the command.
- `const cmd_function_t pFuncCallBack`
A pointer to the callback function that returns the output generated by the command.
- `uint8_t cExpectedNumberOfParameters`
Commands expect a fixed number of parameters, which may be zero.
- `list_element_t link`
link of the element

Field Documentation

(1) `const char* shell_command_t::pcCommand`

For example "help". It must be all lower case.

(2) `char* shell_command_t::pcHelpString`

It should start with the command itself, and end with "\r\n". For example "help: Returns a list of all the commands\r\n".

(3) `const cmd_function_t shell_command_t::pFuncCallBack`**(4) `uint8_t shell_command_t::cExpectedNumberOfParameters`****42.4 Macro Definition Documentation****42.4.1 `#define SHELL_NON_BLOCKING_MODE SERIAL_MANAGER_NON_BLOCKING_MODE`****42.4.2 `#define SHELL_AUTO_COMPLETE (1U)`****42.4.3 `#define SHELL_BUFFER_SIZE (64U)`****42.4.4 `#define SHELL_MAX_ARGS (8U)`****42.4.5 `#define SHELL_HISTORY_COUNT (3U)`****42.4.6 `#define SHELL_HANDLE_SIZE`**

Value:

```
(160U + SHELL_HISTORY_COUNT * SHELL_BUFFER_SIZE +
    SHELL_BUFFER_SIZE + SERIAL_MANAGER_READ_HANDLE_SIZE + \
    SERIAL_MANAGER_WRITE_HANDLE_SIZE)
```

It is the sum of the SHELL_HISTORY_COUNT * SHELL_BUFFER_SIZE + SHELL_BUFFER_SIZE + SERIAL_MANAGER_READ_HANDLE_SIZE + SERIAL_MANAGER_WRITE_HANDLE_SIZE

42.4.7 `#define SHELL_USE_COMMON_TASK (0U)`**42.4.8 `#define SHELL_TASK_PRIORITY (2U)`****42.4.9 `#define SHELL_TASK_STACK_SIZE (1000U)`**

42.4.10 #define SHELL_HANDLE_DEFINE(*name*) uint32_t *name*[(**SHELL_HANDLE_SIZE** + sizeof(uint32_t) - 1U) / sizeof(uint32_t)]

This macro is used to define a 4 byte aligned shell handle. Then use "(shell_handle_t)*name*" to get the shell handle.

The macro should be global and could be optional. You could also define shell handle by yourself.

This is an example,

```
* SHELL_HANDLE_DEFINE(shellHandle);
*
```

Parameters

<i>name</i>	The name string of the shell handle.
-------------	--------------------------------------

42.4.11 #define SHELL_COMMAND_DEFINE(*command*, *descriptor*, *callback*, *paramCount*)

Value:

```
\shell_command_t g_shellCommand##command = {
    (#command), (descriptor), (callback), (paramCount), {0},      \
}
```

This macro is used to define the shell command structure [shell_command_t](#). And then uses the macro SHELL_COMMAND to get the command structure pointer. The macro should not be used in any function.

This is a example,

```
* SHELL_COMMAND_DEFINE(exit, "\r\n\"exit\": Exit program\r\n", SHELL_ExitCommand, 0);
* SHELL_RegisterCommand(s_shellHandle, SHELL_COMMAND(exit));
*
```

Parameters

<i>command</i>	The command string of the command. The double quotes do not need. Such as exit for "exit", help for "Help", read for "read".
----------------	--

<i>descriptor</i>	The description of the command is used for showing the command usage when "help" is typing.
<i>callback</i>	The callback of the command is used to handle the command line when the input command is matched.
<i>paramCount</i>	The max parameter count of the current command.

42.4.12 #define SHELL_COMMAND(*command*) &g_shellCommand##*command*

This macro is used to get the shell command pointer. The macro should not be used before the macro SHELL_COMMAND_DEFINE is used.

Parameters

<i>command</i>	The command string of the command. The double quotes do not need. Such as exit for "exit", help for "Help", read for "read".
----------------	--

42.5 Typedef Documentation

42.5.1 typedef shell_status_t(* cmd_function_t)(shell_handle_t shellHandle, int32_t argc, char **argv)

42.6 Enumeration Type Documentation

42.6.1 enum shell_status_t

Enumerator

kStatus_SHELL_Success Success.

kStatus_SHELL_Error Failed.

kStatus_SHELL_OpenWriteHandleFailed Open write handle failed.

kStatus_SHELL_OpenReadHandleFailed Open read handle failed.

42.7 Function Documentation

42.7.1 shell_status_t SHELL_Init (shell_handle_t *shellHandle*, serial_handle_t *serialHandle*, char * *prompt*)

This function must be called before calling all other Shell functions. Call operation the Shell commands with user-defined settings. The example below shows how to set up the Shell and how to call the SHELL_Init function by passing in these parameters. This is an example.

```
* static SHELL_HANDLE_DEFINE(s_shellHandle);
* SHELL_Init((shell_handle_t)s_shellHandle,
*             (serial_handle_t)s_serialHandle, "Test@SHELL>");
*
```

Parameters

<i>shellHandle</i>	Pointer to point to a memory space of size SHELL_HANDLE_SIZE allocated by the caller. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: SHELL_HANDLE_DEFINE(shellHandle) ; or <code>uint32_t shellHandle[((SHELL_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))];</code>
<i>serialHandle</i>	The serial manager module handle pointer.
<i>prompt</i>	The string prompt pointer of Shell. Only the global variable can be passed.

Return values

<i>kStatus_SHELL_Success</i>	The shell initialization succeed.
<i>kStatus_SHELL_Error</i>	An error occurred when the shell is initialized.
<i>kStatus_SHELL_OpenWriteHandleFailed</i>	Open the write handle failed.
<i>kStatus_SHELL_OpenReadHandleFailed</i>	Open the read handle failed.

42.7.2 **shell_status_t SHELL_RegisterCommand (shell_handle_t *shellHandle*, shell_command_t * *shellCommand*)**

This function is used to register the shell command by using the command configuration `shell_command_config_t`. This is a example,

```
* SHELL_COMMAND_DEFINE(exit, "\r\n\"exit\": Exit program\r\n", SHELL_ExitCommand, 0);
* SHELL_RegisterCommand(s_shellHandle, SHELL_COMMAND(exit));
*
```

Parameters

<i>shellHandle</i>	The shell module handle pointer.
<i>shellCommand</i>	The command element.

Return values

<i>kStatus_SHELL_Success</i>	Successfully register the command.
<i>kStatus_SHELL_Error</i>	An error occurred.

42.7.3 shell_status_t SHELL_UnregisterCommand (shell_command_t * *shellCommand*)

This function is used to unregister the shell command.

Parameters

<i>shellCommand</i>	The command element.
---------------------	----------------------

Return values

<i>kStatus_SHELL_Success</i>	Successfully unregister the command.
------------------------------	--------------------------------------

42.7.4 shell_status_t SHELL_Write (shell_handle_t *shellHandle*, const char * *buffer*, uint32_t *length*)

This function is used to send data to the shell output stream.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
<i>buffer</i>	Start address of the data to write.
<i>length</i>	Length of the data to write.

Return values

<i>kStatus_SHELL_Success</i>	Successfully send data.
<i>kStatus_SHELL_Error</i>	An error occurred.

42.7.5 int SHELL_Printf (shell_handle_t *shellHandle*, const char * *formatString*, ...)

Call this function to write a formatted output to the shell output stream.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
<i>formatString</i>	Format string.

Returns

Returns the number of characters printed or a negative value if an error occurs.

42.7.6 **shell_status_t SHELL_WriteSynchronization (shell_handle_t *shellHandle*, const char * *buffer*, uint32_t *length*)**

This function is used to send data to the shell output stream with OS synchronization, note the function could not be called in ISR.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
<i>buffer</i>	Start address of the data to write.
<i>length</i>	Length of the data to write.

Return values

<i>kStatus_SHELL_Success</i>	Successfully send data.
<i>kStatus_SHELL_Error</i>	An error occurred.

42.7.7 **int SHELL_PrintfSynchronization (shell_handle_t *shellHandle*, const char * *formatString*, ...)**

Call this function to write a formatted output to the shell output stream with OS synchronization, note the function could not be called in ISR.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
--------------------	----------------------------------

<i>formatString</i>	Format string.
---------------------	----------------

Returns

Returns the number of characters printed or a negative value if an error occurs.

42.7.8 void **SHELL_ChangePrompt** (**shell_handle_t shellHandle, char * prompt**)

Call this function to change shell prompt.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
<i>prompt</i>	The string which will be used for command prompt

Returns

NULL.

42.7.9 void **SHELL_PrintPrompt** (**shell_handle_t shellHandle**)

Call this function to print shell prompt.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
--------------------	----------------------------------

Returns

NULL.

42.7.10 void **SHELL_Task** (**shell_handle_t shellHandle**)

The task function for Shell; The function should be polled by upper layer. This function does not return until Shell command exit was called.

Parameters

<i>shellHandle</i>	The shell module handle pointer.
--------------------	----------------------------------

42.7.11 static bool SHELL_checkRunningInIsr(void) [inline], [static]

This function is used to check if code running in ISR.

Return values

<i>TRUE</i>	if code runing in ISR.
-------------	------------------------

Chapter 43

CODEC Driver

43.1 Overview

The MCUXpresso SDK provides a codec abstraction driver interface to access codec register.

Modules

- [CODEC Common Driver](#)
- [CODEC I2C Driver](#)
- [Da7212](#)
- [Sgtl5000](#)
- [Wm8960](#)

43.2 CODEC Common Driver

43.2.1 Overview

The codec common driver provides a codec control abstraction interface.

Modules

- CODEC Adapter
- Da7212_adapter
- Sg15000_adapter
- Wm8960_adapter

Data Structures

- struct `codec_config_t`
Initialize structure of the codec. [More...](#)
- struct `codec_capability_t`
codec capability [More...](#)
- struct `codec_handle_t`
Codec handle definition. [More...](#)

Macros

- #define `CODEC_VOLUME_MAX_VALUE` (100U)
codec maximum volume range

Enumerations

- enum {

 `kStatus_CODEC_NotSupport` = MAKE_STATUS(kStatusGroup_CODEC, 0U),

 `kStatus_CODEC_DeviceNotRegistered` = MAKE_STATUS(kStatusGroup_CODEC, 1U),

 `kStatus_CODEC_I2CBusInitialFailed`,

 `kStatus_CODEC_I2CCommandTransferFailed` }

CODEC status.
- enum `codec_audio_protocol_t` {

 `kCODEC_BusI2S` = 0U,

 `kCODEC_BusLeftJustified` = 1U,

 `kCODEC_BusRightJustified` = 2U,

 `kCODEC_BusPCMA` = 3U,

 `kCODEC_BusPCMB` = 4U,

 `kCODEC_BusTDM` = 5U }

AUDIO format definition.

- enum {

kCODEC_AudioSampleRate8KHz = 8000U,

kCODEC_AudioSampleRate11025Hz = 11025U,

kCODEC_AudioSampleRate12KHz = 12000U,

kCODEC_AudioSampleRate16KHz = 16000U,

kCODEC_AudioSampleRate22050Hz = 22050U,

kCODEC_AudioSampleRate24KHz = 24000U,

kCODEC_AudioSampleRate32KHz = 32000U,

kCODEC_AudioSampleRate44100Hz = 44100U,

kCODEC_AudioSampleRate48KHz = 48000U,

kCODEC_AudioSampleRate96KHz = 96000U,

kCODEC_AudioSampleRate192KHz = 192000U,

kCODEC_AudioSampleRate384KHz = 384000U }

audio sample rate definition
- enum {

kCODEC_AudioBitWidth16bit = 16U,

kCODEC_AudioBitWidth20bit = 20U,

kCODEC_AudioBitWidth24bit = 24U,

kCODEC_AudioBitWidth32bit = 32U }

audio bit width
- enum `codec_module_t` {

kCODEC_ModuleADC = 0U,

kCODEC_ModuleDAC = 1U,

kCODEC_ModulePGA = 2U,

kCODEC_ModuleHeadphone = 3U,

kCODEC_ModuleSpeaker = 4U,

kCODEC_ModuleLinein = 5U,

kCODEC_ModuleLineout = 6U,

kCODEC_ModuleVref = 7U,

kCODEC_ModuleMicbias = 8U,

kCODEC_ModuleMic = 9U,

kCODEC_ModuleI2SIn = 10U,

kCODEC_ModuleI2SOut = 11U,

kCODEC_ModuleMixer = 12U }

audio codec module
- enum `codec_module_ctrl_cmd_t` { kCODEC_ModuleSwitchI2SInInterface = 0U }

audio codec module control cmd
- enum {

kCODEC_ModuleI2SInInterfacePCM = 0U,

kCODEC_ModuleI2SInInterfaceDSD = 1U }

audio codec module digital interface
- enum {

kCODEC_RecordSourceDifferentialLine = 1U,

kCODEC_RecordSourceLineInput = 2U,

kCODEC_RecordSourceDifferentialMic = 4U,

kCODEC_RecordSourceDigitalMic = 8U,

```

kCODEC_RecordSourceSingleEndMic = 16U }

    audio codec module record source value

• enum {
    kCODEC_RecordChannelLeft1 = 1U,
    kCODEC_RecordChannelLeft2 = 2U,
    kCODEC_RecordChannelLeft3 = 4U,
    kCODEC_RecordChannelRight1 = 1U,
    kCODEC_RecordChannelRight2 = 2U,
    kCODEC_RecordChannelRight3 = 4U,
    kCODEC_RecordChannelDifferentialPositive1 = 1U,
    kCODEC_RecordChannelDifferentialPositive2 = 2U,
    kCODEC_RecordChannelDifferentialPositive3 = 4U,
    kCODEC_RecordChannelDifferentialNegative1 = 8U,
    kCODEC_RecordChannelDifferentialNegative2 = 16U,
    kCODEC_RecordChannelDifferentialNegative3 = 32U }

    audio codec record channel

• enum {
    kCODEC_PlaySourcePGA = 1U,
    kCODEC_PlaySourceInput = 2U,
    kCODEC_PlaySourceDAC = 4U,
    kCODEC_PlaySourceMixerIn = 1U,
    kCODEC_PlaySourceMixerInLeft = 2U,
    kCODEC_PlaySourceMixerInRight = 4U,
    kCODEC_PlaySourceAux = 8U }

    audio codec module play source value

• enum {
    kCODEC_PlayChannelHeadphoneLeft = 1U,
    kCODEC_PlayChannelHeadphoneRight = 2U,
    kCODEC_PlayChannelSpeakerLeft = 4U,
    kCODEC_PlayChannelSpeakerRight = 8U,
    kCODEC_PlayChannelLineOutLeft = 16U,
    kCODEC_PlayChannelLineOutRight = 32U,
    kCODEC_PlayChannelLeft0 = 1U,
    kCODEC_PlayChannelRight0 = 2U,
    kCODEC_PlayChannelLeft1 = 4U,
    kCODEC_PlayChannelRight1 = 8U,
    kCODEC_PlayChannelLeft2 = 16U,
    kCODEC_PlayChannelRight2 = 32U,
    kCODEC_PlayChannelLeft3 = 64U,
    kCODEC_PlayChannelRight3 = 128U }

    codec play channel

• enum {

```

```
kCODEC_VolumeHeadphoneLeft = 1U,  
kCODEC_VolumeHeadphoneRight = 2U,  
kCODEC_VolumeSpeakerLeft = 4U,  
kCODEC_VolumeSpeakerRight = 8U,  
kCODEC_VolumeLineOutLeft = 16U,  
kCODEC_VolumeLineOutRight = 32U,  
kCODEC_VolumeLeft0 = 1UL << 0U,  
kCODEC_VolumeRight0 = 1UL << 1U,  
kCODEC_VolumeLeft1 = 1UL << 2U,  
kCODEC_VolumeRight1 = 1UL << 3U,  
kCODEC_VolumeLeft2 = 1UL << 4U,  
kCODEC_VolumeRight2 = 1UL << 5U,  
kCODEC_VolumeLeft3 = 1UL << 6U,  
kCODEC_VolumeRight3 = 1UL << 7U,  
kCODEC_VolumeDAC = 1UL << 8U }
```

codec volume setting

- enum {

```

kCODEC_SupportModuleADC = 1U << 0U,
kCODEC_SupportModuleDAC = 1U << 1U,
kCODEC_SupportModulePGA = 1U << 2U,
kCODEC_SupportModuleHeadphone = 1U << 3U,
kCODEC_SupportModuleSpeaker = 1U << 4U,
kCODEC_SupportModuleLinein = 1U << 5U,
kCODEC_SupportModuleLineout = 1U << 6U,
kCODEC_SupportModuleVref = 1U << 7U,
kCODEC_SupportModuleMicbias = 1U << 8U,
kCODEC_SupportModuleMic = 1U << 9U,
kCODEC_SupportModuleI2SIn = 1U << 10U,
kCODEC_SupportModuleI2SOut = 1U << 11U,
kCODEC_SupportModuleMixer = 1U << 12U,
kCODEC_SupportModuleI2SInSwitchInterface = 1U << 13U,
kCODEC_SupportPlayChannelLeft0 = 1U << 0U,
kCODEC_SupportPlayChannelRight0 = 1U << 1U,
kCODEC_SupportPlayChannelLeft1 = 1U << 2U,
kCODEC_SupportPlayChannelRight1 = 1U << 3U,
kCODEC_SupportPlayChannelLeft2 = 1U << 4U,
kCODEC_SupportPlayChannelRight2 = 1U << 5U,
kCODEC_SupportPlayChannelLeft3 = 1U << 6U,
kCODEC_SupportPlayChannelRight3 = 1U << 7U,
kCODEC_SupportPlaySourcePGA = 1U << 8U,
kCODEC_SupportPlaySourceInput = 1U << 9U,
kCODEC_SupportPlaySourceDAC = 1U << 10U,
kCODEC_SupportPlaySourceMixerIn = 1U << 11U,
kCODEC_SupportPlaySourceMixerInLeft = 1U << 12U,
kCODEC_SupportPlaySourceMixerInRight = 1U << 13U,
kCODEC_SupportPlaySourceAux = 1U << 14U,
kCODEC_SupportRecordSourceDifferentialLine = 1U << 0U,
kCODEC_SupportRecordSourceLineInput = 1U << 1U,
kCODEC_SupportRecordSourceDifferentialMic = 1U << 2U,
kCODEC_SupportRecordSourceDigitalMic = 1U << 3U,
kCODEC_SupportRecordSourceSingleEndMic = 1U << 4U,
kCODEC_SupportRecordChannelLeft1 = 1U << 6U,
kCODEC_SupportRecordChannelLeft2 = 1U << 7U,
kCODEC_SupportRecordChannelLeft3 = 1U << 8U,
kCODEC_SupportRecordChannelRight1 = 1U << 9U,
kCODEC_SupportRecordChannelRight2 = 1U << 10U,
kCODEC_SupportRecordChannelRight3 = 1U << 11U }

```

audio codec capability

Functions

- `status_t CODEC_Init (codec_handle_t *handle, codec_config_t *config)`
Codec initialization.
- `status_t CODEC_Deinit (codec_handle_t *handle)`
Codec de-initilization.
- `status_t CODEC_SetFormat (codec_handle_t *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)`
set audio data format.
- `status_t CODEC_ModuleControl (codec_handle_t *handle, codec_module_ctrl_cmd_t cmd, uint32_t data)`
codec module control.
- `status_t CODEC_SetVolume (codec_handle_t *handle, uint32_t channel, uint32_t volume)`
set audio codec pl volume.
- `status_t CODEC_SetMute (codec_handle_t *handle, uint32_t channel, bool mute)`
set audio codec module mute.
- `status_t CODEC_SetPower (codec_handle_t *handle, codec_module_t module, bool powerOn)`
set audio codec power.
- `status_t CODEC_SetRecord (codec_handle_t *handle, uint32_t recordSource)`
codec set record source.
- `status_t CODEC_SetRecordChannel (codec_handle_t *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)`
codec set record channel.
- `status_t CODEC_SetPlay (codec_handle_t *handle, uint32_t playSource)`
codec set play source.

Driver version

- `#define FSL_CODEC_DRIVER_VERSION (MAKE_VERSION(2, 3, 0))`
CLOCK driver version 2.3.0.

43.2.2 Data Structure Documentation

43.2.2.1 struct codec_config_t

Data Fields

- `uint32_t codecDevType`
codec type
- `void *codecDevConfig`
Codec device specific configuration.

43.2.2.2 struct codec_capability_t

Data Fields

- `uint32_t codecModuleCapability`
codec module capability
- `uint32_t codecPlayCapability`
codec play capability
- `uint32_t codecRecordCapability`
codec record capability
- `uint32_t codecVolumeCapability`
codec volume capability

43.2.2.3 struct _codec_handle

codec handle declaration

- Application should allocate a buffer with CODEC_HANDLE_SIZE for handle definition, such as `uint8_t codecHandleBuffer[CODEC_HANDLE_SIZE]; codec_handle_t *codecHandle = codecHandleBuffer;`

Data Fields

- `codec_config_t * codecConfig`
codec configuration function pointer
- `const codec_capability_t * codecCapability`
codec capability
- `uint8_t codecDevHandle [HAL_CODEC_HANDLER_SIZE]`
codec device handle

43.2.3 Macro Definition Documentation

43.2.3.1 #define FSL_CODEC_DRIVER_VERSION (MAKE_VERSION(2, 3, 0))

43.2.4 Enumeration Type Documentation

43.2.4.1 anonymous enum

Enumerator

`kStatus_CODEC_NotSupport` CODEC not support status.

`kStatus_CODEC_DeviceNotRegistered` CODEC device register failed status.

`kStatus_CODEC_I2CBusInitialFailed` CODEC i2c bus initialization failed status.

`kStatus_CODEC_I2CCommandTransferFailed` CODEC i2c bus command transfer failed status.

43.2.4.2 enum codec_audio_protocol_t

Enumerator

- kCODEC_BusI2S* I2S type.
- kCODEC_BusLeftJustified* Left justified mode.
- kCODEC_BusRightJustified* Right justified mode.
- kCODEC_BusPCMA* DSP/PCM A mode.
- kCODEC_BusPCMB* DSP/PCM B mode.
- kCODEC_BusTDM* TDM mode.

43.2.4.3 anonymous enum

Enumerator

- kCODEC_AudioSampleRate8KHz* Sample rate 8000 Hz.
- kCODEC_AudioSampleRate11025Hz* Sample rate 11025 Hz.
- kCODEC_AudioSampleRate12KHz* Sample rate 12000 Hz.
- kCODEC_AudioSampleRate16KHz* Sample rate 16000 Hz.
- kCODEC_AudioSampleRate22050Hz* Sample rate 22050 Hz.
- kCODEC_AudioSampleRate24KHz* Sample rate 24000 Hz.
- kCODEC_AudioSampleRate32KHz* Sample rate 32000 Hz.
- kCODEC_AudioSampleRate44100Hz* Sample rate 44100 Hz.
- kCODEC_AudioSampleRate48KHz* Sample rate 48000 Hz.
- kCODEC_AudioSampleRate96KHz* Sample rate 96000 Hz.
- kCODEC_AudioSampleRate192KHz* Sample rate 192000 Hz.
- kCODEC_AudioSampleRate384KHz* Sample rate 384000 Hz.

43.2.4.4 anonymous enum

Enumerator

- kCODEC_AudioBitWidth16bit* audio bit width 16
- kCODEC_AudioBitWidth20bit* audio bit width 20
- kCODEC_AudioBitWidth24bit* audio bit width 24
- kCODEC_AudioBitWidth32bit* audio bit width 32

43.2.4.5 enum codec_module_t

Enumerator

- kCODEC_ModuleADC* codec module ADC
- kCODEC_ModuleDAC* codec module DAC
- kCODEC_ModulePGA* codec module PGA
- kCODEC_ModuleHeadphone* codec module headphone

kCODEC_ModuleSpeaker codec module speaker
kCODEC_ModuleLinein codec module linein
kCODEC_ModuleLineout codec module lineout
kCODEC_ModuleVref codec module VREF
kCODEC_ModuleMicbias codec module MIC BIAS
kCODEC_ModuleMic codec module MIC
kCODEC_ModuleI2SIn codec module I2S in
kCODEC_ModuleI2SOut codec module I2S out
kCODEC_ModuleMixer codec module mixer

43.2.4.6 enum codec_module_ctrl_cmd_t

Enumerator

kCODEC_ModuleSwitchI2SInInterface module digital interface siwtch.

43.2.4.7 anonymous enum

Enumerator

kCODEC_ModuleI2SInInterfacePCM Pcm interface.
kCODEC_ModuleI2SInInterfaceDSD DSD interface.

43.2.4.8 anonymous enum

Enumerator

kCODEC_RecordSourceDifferentialLine record source from differential line
kCODEC_RecordSourceLineInput record source from line input
kCODEC_RecordSourceDifferentialMic record source from differential mic
kCODEC_RecordSourceDigitalMic record source from digital microphone
kCODEC_RecordSourceSingleEndMic record source from single microphone

43.2.4.9 anonymous enum

Enumerator

kCODEC_RecordChannelLeft1 left record channel 1
kCODEC_RecordChannelLeft2 left record channel 2
kCODEC_RecordChannelLeft3 left record channel 3
kCODEC_RecordChannelRight1 right record channel 1
kCODEC_RecordChannelRight2 right record channel 2
kCODEC_RecordChannelRight3 right record channel 3
kCODEC_RecordChannelDifferentialPositive1 differential positive record channel 1

kCODEC_RecordChannelDifferentialPositive2 differential positive record channel 2
kCODEC_RecordChannelDifferentialPositive3 differential positive record channel 3
kCODEC_RecordChannelDifferentialNegative1 differential negative record channel 1
kCODEC_RecordChannelDifferentialNegative2 differential negative record channel 2
kCODEC_RecordChannelDifferentialNegative3 differential negative record channel 3

43.2.4.10 anonymous enum

Enumerator

kCODEC_PlaySourcePGA play source PGA, bypass ADC
kCODEC_PlaySourceInput play source Input3
kCODEC_PlaySourceDAC play source DAC
kCODEC_PlaySourceMixerIn play source mixer in
kCODEC_PlaySourceMixerInLeft play source mixer in left
kCODEC_PlaySourceMixerInRight play source mixer in right
kCODEC_PlaySourceAux play source mixer in AUX

43.2.4.11 anonymous enum

Enumerator

kCODEC_PlayChannelHeadphoneLeft play channel headphone left
kCODEC_PlayChannelHeadphoneRight play channel headphone right
kCODEC_PlayChannelSpeakerLeft play channel speaker left
kCODEC_PlayChannelSpeakerRight play channel speaker right
kCODEC_PlayChannelLineOutLeft play channel lineout left
kCODEC_PlayChannelLineOutRight play channel lineout right
kCODEC_PlayChannelLeft0 play channel left0
kCODEC_PlayChannelRight0 play channel right0
kCODEC_PlayChannelLeft1 play channel left1
kCODEC_PlayChannelRight1 play channel right1
kCODEC_PlayChannelLeft2 play channel left2
kCODEC_PlayChannelRight2 play channel right2
kCODEC_PlayChannelLeft3 play channel left3
kCODEC_PlayChannelRight3 play channel right3

43.2.4.12 anonymous enum

Enumerator

kCODEC_VolumeHeadphoneLeft headphone left volume
kCODEC_VolumeHeadphoneRight headphone right volume
kCODEC_VolumeSpeakerLeft speaker left volume
kCODEC_VolumeSpeakerRight speaker right volume

kCODEC_VolumeLineOutLeft lineout left volume
kCODEC_VolumeLineOutRight lineout right volume
kCODEC_VolumeLeft0 left0 volume
kCODEC_VolumeRight0 right0 volume
kCODEC_VolumeLeft1 left1 volume
kCODEC_VolumeRight1 right1 volume
kCODEC_VolumeLeft2 left2 volume
kCODEC_VolumeRight2 right2 volume
kCODEC_VolumeLeft3 left3 volume
kCODEC_VolumeRight3 right3 volume
kCODEC_VolumeDAC dac volume

43.2.4.13 anonymous enum

Enumerator

kCODEC_SupportModuleADC codec capability of module ADC
kCODEC_SupportModuleDAC codec capability of module DAC
kCODEC_SupportModulePGA codec capability of module PGA
kCODEC_SupportModuleHeadphone codec capability of module headphone
kCODEC_SupportModuleSpeaker codec capability of module speaker
kCODEC_SupportModuleLinein codec capability of module linein
kCODEC_SupportModuleLineout codec capability of module lineout
kCODEC_SupportModuleVref codec capability of module vref
kCODEC_SupportModuleMicbias codec capability of module mic bias
kCODEC_SupportModuleMic codec capability of module mic bias
kCODEC_SupportModuleI2SIn codec capability of module I2S in
kCODEC_SupportModuleI2SOut codec capability of module I2S out
kCODEC_SupportModuleMixer codec capability of module mixer
kCODEC_SupportModuleI2SInSwitchInterface codec capability of module I2S in switch interface

kCODEC_SupportPlayChannelLeft0 codec capability of play channel left 0
kCODEC_SupportPlayChannelRight0 codec capability of play channel right 0
kCODEC_SupportPlayChannelLeft1 codec capability of play channel left 1
kCODEC_SupportPlayChannelRight1 codec capability of play channel right 1
kCODEC_SupportPlayChannelLeft2 codec capability of play channel left 2
kCODEC_SupportPlayChannelRight2 codec capability of play channel right 2
kCODEC_SupportPlayChannelLeft3 codec capability of play channel left 3
kCODEC_SupportPlayChannelRight3 codec capability of play channel right 3
kCODEC_SupportPlaySourcePGA codec capability of set playback source PGA
kCODEC_SupportPlaySourceInput codec capability of set playback source INPUT
kCODEC_SupportPlaySourceDAC codec capability of set playback source DAC
kCODEC_SupportPlaySourceMixerIn codec capability of set play source Mixer in
kCODEC_SupportPlaySourceMixerInLeft codec capability of set play source Mixer in left
kCODEC_SupportPlaySourceMixerInRight codec capability of set play source Mixer in right

kCODEC_SupportPlaySourceAux codec capability of set play source aux

kCODEC_SupportRecordSourceDifferentialLine codec capability of record source differential line

kCODEC_SupportRecordSourceLineInput codec capability of record source line input

kCODEC_SupportRecordSourceDifferentialMic codec capability of record source differential mic

kCODEC_SupportRecordSourceDigitalMic codec capability of record digital mic

kCODEC_SupportRecordSourceSingleEndMic codec capability of single end mic

kCODEC_SupportRecordChannelLeft1 left record channel 1

kCODEC_SupportRecordChannelLeft2 left record channel 2

kCODEC_SupportRecordChannelLeft3 left record channel 3

kCODEC_SupportRecordChannelRight1 right record channel 1

kCODEC_SupportRecordChannelRight2 right record channel 2

kCODEC_SupportRecordChannelRight3 right record channel 3

43.2.5 Function Documentation

43.2.5.1 status_t CODEC_Init (***codec_handle_t * handle***, ***codec_config_t * config***)

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configurations.

Returns

kStatus_Success is success, else de-initial failed.

43.2.5.2 status_t CODEC_Deinit (***codec_handle_t * handle***)

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus_Success is success, else de-initial failed.

43.2.5.3 status_t CODEC_SetFormat (***codec_handle_t * handle***, ***uint32_t mclk***, ***uint32_t sampleRate***, ***uint32_t bitWidth***)

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus_Success is success, else configure failed.

43.2.5.4 status_t CODEC_ModuleControl (*codec_handle_t * handle*, *codec_module_ctrl_cmd_t cmd*, *uint32_t data*)

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature.

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus_Success is success, else configure failed.

43.2.5.5 status_t CODEC_SetVolume (*codec_handle_t * handle*, *uint32_t channel*, *uint32_t volume*)

Parameters

<i>handle</i>	codec handle.
<i>channel</i>	audio codec volume channel, can be a value or combine value of _codec_volume_-capability or _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus_Success is success, else configure failed.

43.2.5.6 status_t CODEC_SetMute (*codec_handle_t * handle*, *uint32_t channel*, *bool mute*)

Parameters

<i>handle</i>	codec handle.
<i>channel</i>	audio codec volume channel, can be a value or combine value of _codec_volume_-capability or _codec_play_channel.
<i>mute</i>	true is mute, false is unmute.

Returns

kStatus_Success is success, else configure failed.

43.2.5.7 status_t CODEC_SetPower (*codec_handle_t * handle*, *codec_module_t module*, *bool powerOn*)

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus_Success is success, else configure failed.

43.2.5.8 status_t CODEC_SetRecord (*codec_handle_t * handle*, *uint32_t recordSource*)

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus_Success is success, else configure failed.

43.2.5.9 status_t CODEC_SetRecordChannel (*codec_handle_t * handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel*)

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus_Success is success, else configure failed.

43.2.5.10 status_t CODEC_SetPlay (*codec_handle_t * handle, uint32_t playSource*)

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus_Success is success, else configure failed.

43.3 CODEC I2C Driver

43.3.1 Overview

The codec common driver provides a codec control abstraction interface.

Data Structures

- struct `codec_i2c_config_t`
CODEC I2C configurations structure. [More...](#)

Macros

- #define `CODEC_I2C_MASTER_HANDLER_SIZE` HAL_I2C_MASTER_HANDLE_SIZE
codec i2c handler

Enumerations

- enum `codec_reg_addr_t` {

`kCODEC_RegAddr8Bit` = 1U,
`kCODEC_RegAddr16Bit` = 2U }
CODEC device register address type.
- enum `codec_reg_width_t` {

`kCODEC_RegWidth8Bit` = 1U,
`kCODEC_RegWidth16Bit` = 2U,
`kCODEC_RegWidth32Bit` = 4U }
CODEC device register width.

Functions

- `status_t CODEC_I2C_Init` (void *handle, uint32_t i2cInstance, uint32_t i2cBaudrate, uint32_t i2cSourceClockHz)
Codec i2c bus initialization.
- `status_t CODEC_I2C_Deinit` (void *handle)
Codec i2c de-initilization.
- `status_t CODEC_I2C_Send` (void *handle, uint8_t deviceAddress, uint32_t subAddress, uint8_t subaddressSize, uint8_t *txBuff, uint8_t txBuffSize)
codec i2c send function.
- `status_t CODEC_I2C_Receive` (void *handle, uint8_t deviceAddress, uint32_t subAddress, uint8_t subaddressSize, uint8_t *rxBuff, uint8_t rxBuffSize)
codec i2c receive function.

43.3.2 Data Structure Documentation

43.3.2.1 struct codec_i2c_config_t

Data Fields

- uint32_t `codecI2CInstance`
i2c bus instance
- uint32_t `codecI2CSourceClock`
i2c bus source clock frequency

43.3.3 Enumeration Type Documentation

43.3.3.1 enum codec_reg_addr_t

Enumerator

kCODEC_RegAddr8Bit 8-bit register address.
kCODEC_RegAddr16Bit 16-bit register address.

43.3.3.2 enum codec_reg_width_t

Enumerator

kCODEC_RegWidth8Bit 8-bit register width.
kCODEC_RegWidth16Bit 16-bit register width.
kCODEC_RegWidth32Bit 32-bit register width.

43.3.4 Function Documentation

43.3.4.1 status_t CODEC_I2C_Init (void * *handle*, uint32_t *i2cInstance*, uint32_t *i2cBaudrate*, uint32_t *i2cSourceClockHz*)

Parameters

<i>handle</i>	i2c master handle.
<i>i2cInstance</i>	instance number of the i2c bus, such as 0 is corresponding to I2C0.

<i>i2cBaudrate</i>	i2c baudrate.
<i>i2cSource-ClockHz</i>	i2c source clock frequency.

Returns

kStatus_HAL_I2cSuccess is success, else initial failed.

43.3.4.2 status_t CODEC_I2C_Deinit (void * *handle*)

Parameters

<i>handle</i>	i2c master handle.
---------------	--------------------

Returns

kStatus_HAL_I2cSuccess is success, else deinitial failed.

43.3.4.3 status_t CODEC_I2C_Send (void * *handle*, uint8_t *deviceAddress*, uint32_t *subAddress*, uint8_t *subaddressSize*, uint8_t * *txBuff*, uint8_t *txBuffSize*)

Parameters

<i>handle</i>	i2c master handle.
<i>deviceAddress</i>	codec device address.
<i>subAddress</i>	register address.
<i>subaddressSize</i>	register address width.
<i>txBuff</i>	tx buffer pointer.
<i>txBuffSize</i>	tx buffer size.

Returns

kStatus_HAL_I2cSuccess is success, else send failed.

43.3.4.4 status_t CODEC_I2C_Receive (void * *handle*, uint8_t *deviceAddress*, uint32_t *subAddress*, uint8_t *subaddressSize*, uint8_t * *rxBuff*, uint8_t *rxBuffSize*)

Parameters

<i>handle</i>	i2c master handle.
<i>deviceAddress</i>	codec device address.
<i>subAddress</i>	register address.
<i>subaddressSize</i>	register address width.
<i>rxBuff</i>	rx buffer pointer.
<i>rxBuffSize</i>	rx buffer size.

Returns

kStatus_HAL_I2cSuccess is success, else receive failed.

Chapter 44

Serial Manager

44.1 Overview

This chapter describes the programming interface of the serial manager component.

The serial manager component provides a series of APIs to operate different serial port types. The port types it supports are UART, USB CDC and SWO.

Modules

- [Serial_port_swo](#)
- [Serial_port_uart](#)

Data Structures

- struct [serial_manager_config_t](#)
serial manager config structure [More...](#)
- struct [serial_manager_callback_message_t](#)
Callback message structure. [More...](#)

Macros

- #define [SERIAL_MANAGER_NON_BLOCKING_MODE](#) (0U)
Enable or disable serial manager non-blocking mode (1 - enable, 0 - disable)
- #define [SERIAL_MANAGER_RING_BUFFER_FLOWCONTROL](#) (0U)
Enable or ring buffer flow control (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_UART](#) (0U)
Enable or disable uart port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_UART_DMA](#) (0U)
Enable or disable uart dma port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_USBCDC](#) (0U)
Enable or disable USB CDC port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_SWO](#) (0U)
Enable or disable SWO port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_VIRTUAL](#) (0U)
Enable or disable USB CDC virtual port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_RPMSG](#) (0U)
Enable or disable rpmsg port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_SPI_MASTER](#) (0U)
Enable or disable SPI Master port (1 - enable, 0 - disable)
- #define [SERIAL_PORT_TYPE_SPI_SLAVE](#) (0U)
Enable or disable SPI Slave port (1 - enable, 0 - disable)
- #define [SERIAL_MANAGER_TASK_HANDLE_TX](#) (0U)
Enable or disable SerialManager_Task() handle TX to prevent recursive calling.
- #define [SERIAL_MANAGER_WRITE_TIME_DELAY_DEFAULT_VALUE](#) (1U)

- `#define SERIAL_MANAGER_READ_TIME_DELAY_DEFAULT_VALUE (1U)`
Set the default delay time in ms used by SerialManager_WriteTimeDelay().
- `#define SERIAL_MANAGER_TASK_HANDLE_RX_AVAILABLE_NOTIFY (0U)`
Set the default delay time in ms used by SerialManager_ReadTimeDelay().
- `#define SERIAL_MANAGER_WRITE_HANDLE_SIZE (4U)`
Enable or disable SerialManager_Task() handle RX data available notify.
- `#define SERIAL_MANAGER_USE_COMMON_TASK (0U)`
Set serial manager write handle size.
- `SERIAL_PORT_UART_HANDLE_SIZE/SERIAL_PORT_USB_CDC_HANDLE_SIZE + serial manager dedicated size.`
- `#define SERIAL_MANAGER_HANDLE_SIZE (SERIAL_MANAGER_HANDLE_SIZE_TEMP + 12U)`
Macro to determine whether use common task.
- `#define SERIAL_MANAGER_HANDLE_DEFINE(name) uint32_t name[((SERIAL_MANAGER_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]`
Defines the serial manager handle.
- `#define SERIAL_MANAGER_WRITE_HANDLE_DEFINE(name) uint32_t name[((SERIAL_MANAGER_WRITE_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]`
Defines the serial manager write handle.
- `#define SERIAL_MANAGER_READ_HANDLE_DEFINE(name) uint32_t name[((SERIAL_MANAGER_READ_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]`
Defines the serial manager read handle.
- `#define SERIAL_MANAGER_TASK_PRIORITY (2U)`
Macro to set serial manager task priority.
- `#define SERIAL_MANAGER_TASK_STACK_SIZE (1000U)`
Macro to set serial manager task stack size.

TypeDefs

- `typedef void * serial_handle_t`
The handle of the serial manager module.
- `typedef void * serial_write_handle_t`
The write handle of the serial manager module.
- `typedef void * serial_read_handle_t`
The read handle of the serial manager module.
- `typedef void(* serial_manager_callback_t)(void *callbackParam, serial_manager_callback_message_t *message, serial_manager_status_t status)`
callback function

Enumerations

- enum `serial_port_type_t` {

 `kSerialPort_Uart` = 1U,

 `kSerialPort_UsbCdc`,

 `kSerialPort_Swo`,

 `kSerialPort_Virtual`,

 `kSerialPort_Rpmsg`,

 `kSerialPort_UartDma`,

 `kSerialPort_SpiMaster`,

 `kSerialPort_SpiSlave`,

 `kSerialPort_None` }

 serial port type
- enum `serial_manager_type_t` {

 `kSerialManager_NonBlocking` = 0x0U,

 `kSerialManager_Blocking` = 0x8F41U }

 serial manager type
- enum `serial_manager_status_t` {

 `kStatus_SerialManager_Success` = `kStatus_Success`,

 `kStatus_SerialManager_Error` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 1)`,

 `kStatus_SerialManager_Busy` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 2)`,

 `kStatus_SerialManager_Notify` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 3)`,

 `kStatus_SerialManager_Canceled`,

 `kStatus_SerialManager_HandleConflict` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 5)`,

 `kStatus_SerialManager_RingBufferOverflow`,

 `kStatus_SerialManager_NotConnected` = `MAKE_STATUS(kStatusGroup_SERIALMANAGER, 7)` }

 serial manager error code

Functions

- `serial_manager_status_t SerialManager_Init (serial_handle_t serialHandle, const serial_manager_config_t *config)`

Initializes a serial manager module with the serial manager handle and the user configuration structure.
- `serial_manager_status_t SerialManager_Deinit (serial_handle_t serialHandle)`

De-initializes the serial manager module instance.
- `serial_manager_status_t SerialManager_OpenWriteHandle (serial_handle_t serialHandle, serial_write_handle_t writeHandle)`

Opens a writing handle for the serial manager module.
- `serial_manager_status_t SerialManager_CloseWriteHandle (serial_write_handle_t writeHandle)`

Closes a writing handle for the serial manager module.
- `serial_manager_status_t SerialManager_OpenReadHandle (serial_handle_t serialHandle, serial_read_handle_t readHandle)`

Opens a reading handle for the serial manager module.
- `serial_manager_status_t SerialManager_CloseReadHandle (serial_read_handle_t readHandle)`

Closes a reading for the serial manager module.

- `serial_manager_status_t SerialManager_WriteBlocking (serial_write_handle_t writeHandle, uint8_t *buffer, uint32_t length)`
Transmits data with the blocking mode.
- `serial_manager_status_t SerialManager_ReadBlocking (serial_read_handle_t readHandle, uint8_t *buffer, uint32_t length)`
Reads data with the blocking mode.
- `serial_manager_status_t SerialManager_EnterLowpower (serial_handle_t serialHandle)`
Prepares to enter low power consumption.
- `serial_manager_status_t SerialManager_ExitLowpower (serial_handle_t serialHandle)`
Restores from low power consumption.
- static bool `SerialManager_needPollingIsr (void)`
Check if need polling ISR.

44.2 Data Structure Documentation

44.2.1 struct serial_manager_config_t

Data Fields

- `uint8_t * ringBuffer`
Ring buffer address, it is used to buffer data received by the hardware.
- `uint32_t ringBufferSize`
The size of the ring buffer.
- `serial_port_type_t type`
Serial port type.
- `serial_manager_type_t blockType`
Serial manager port type.
- `void * portConfig`
Serial port configuration.

Field Documentation

(1) `uint8_t* serial_manager_config_t::ringBuffer`

Besides, the memory space cannot be free during the lifetime of the serial manager module.

44.2.2 struct serial_manager_callback_message_t

Data Fields

- `uint8_t * buffer`
Transferred buffer.
- `uint32_t length`
Transferred data length.

44.3 Macro Definition Documentation

44.3.1 #define SERIAL_MANAGER_WRITE_TIME_DELAY_DEFAULT_VALUE (1U)

44.3.2 #define SERIAL_MANAGER_READ_TIME_DELAY_DEFAULT_VALUE (1U)

44.3.3 #define SERIAL_MANAGER_USE_COMMON_TASK (0U)

Macro to determine whether use common task.

44.3.4 #define SERIAL_MANAGER_HANDLE_SIZE (SERIAL_MANAGER_HANDLE_SIZE_TEMP + 12U)

Definition of serial manager handle size.

**44.3.5 #define SERIAL_MANAGER_HANDLE_DEFINE(*name*) uint32_t
name[((SERIAL_MANAGER_HANDLE_SIZE + sizeof(uint32_t) - 1U) /
 sizeof(uint32_t))]**

This macro is used to define a 4 byte aligned serial manager handle. Then use "(serial_handle_t)*name*" to get the serial manager handle.

The macro should be global and could be optional. You could also define serial manager handle by yourself.

This is an example,

```
* SERIAL_MANAGER_HANDLE_DEFINE(serialManagerHandle);
*
```

Parameters

<i>name</i>	The name string of the serial manager handle.
-------------	---

**44.3.6 #define SERIAL_MANAGER_WRITE_HANDLE_DEFINE(*name*) uint32_t
name[((SERIAL_MANAGER_WRITE_HANDLE_SIZE + sizeof(uint32_t) -
 1U) / sizeof(uint32_t))]**

This macro is used to define a 4 byte aligned serial manager write handle. Then use "(serial_write_handle_t)*name*" to get the serial manager write handle.

The macro should be global and could be optional. You could also define serial manager write handle by yourself.

This is an example,

```
* SERIAL_MANAGER_WRITE_HANDLE_DEFINE(serialManagerwriteHandle);
*
```

Parameters

<i>name</i>	The name string of the serial manager write handle.
-------------	---

44.3.7 #define SERIAL_MANAGER_READ_HANDLE_DEFINE(*name*) uint32_t name[((SERIAL_MANAGER_READ_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))]

This macro is used to define a 4 byte aligned serial manager read handle. Then use "(serial_read_handle_t)*name*" to get the serial manager read handle.

The macro should be global and could be optional. You could also define serial manager read handle by yourself.

This is an example,

```
* SERIAL_MANAGER_READ_HANDLE_DEFINE(serialManagerReadHandle);
*
```

Parameters

<i>name</i>	The name string of the serial manager read handle.
-------------	--

44.3.8 #define SERIAL_MANAGER_TASK_PRIORITY (2U)

44.3.9 #define SERIAL_MANAGER_TASK_STACK_SIZE (1000U)

44.4 Enumeration Type Documentation

44.4.1 enum serial_port_type_t

Enumerator

- kSerialPort_Uart* Serial port UART.
- kSerialPort_UsbCdc* Serial port USB CDC.
- kSerialPort_Swo* Serial port SWO.
- kSerialPort_Virtual* Serial port Virtual.
- kSerialPort_Rpmsg* Serial port RPMSG.
- kSerialPort_UartDma* Serial port UART DMA.
- kSerialPort_SpiMaster* Serial port SPIMASTER.

kSerialPort_SpiSlave Serial port SPISLAVE.

kSerialPort_None Serial port is none.

44.4.2 enum serial_manager_type_t

Enumerator

kSerialManager_NonBlocking None blocking handle.

kSerialManager_Blocking Blocking handle.

44.4.3 enum serial_manager_status_t

Enumerator

kStatus_SerialManager_Success Success.

kStatus_SerialManager_Error Failed.

kStatus_SerialManager_Busy Busy.

kStatus_SerialManager_Notify Ring buffer is not empty.

kStatus_SerialManager_Canceled the non-blocking request is canceled

kStatus_SerialManager_HandleConflict The handle is opened.

kStatus_SerialManager_RingBufferOverflow The ring buffer is overflowed.

kStatus_SerialManager_NotConnected The host is not connected.

44.5 Function Documentation

44.5.1 serial_manager_status_t SerialManager_Init (serial_handle_t *serialHandle*, const serial_manager_config_t * *config*)

This function configures the Serial Manager module with user-defined settings. The user can configure the configuration structure. The parameter *serialHandle* is a pointer to point to a memory space of size [SERIAL_MANAGER_HANDLE_SIZE](#) allocated by the caller. The Serial Manager module supports three types of serial port, UART (includes UART, USART, LPSCI, LPUART, etc), USB CDC and swo. Please refer to [serial_port_type_t](#) for serial port setting. These three types can be set by using [serial_manager_config_t](#).

Example below shows how to use this API to configure the Serial Manager. For UART,

```
* #define SERIAL_MANAGER_RING_BUFFER_SIZE (256U)
* static SERIAL_MANAGER_HANDLE_DEFINE(s_serialHandle);
* static uint8_t s_ringBuffer[SERIAL_MANAGER_RING_BUFFER_SIZE];
*
* serial_manager_config_t config;
* serial_port_uart_config_t uartConfig;
* config.type = kSerialPort_Uart;
* config.ringBuffer = &s_ringBuffer[0];
* config.ringBufferSize = SERIAL_MANAGER_RING_BUFFER_SIZE;
* uartConfig.instance = 0;
```

```

*   uartConfig.clockRate = 24000000;
*   uartConfig.baudRate = 115200;
*   uartConfig.parityMode = kSerialManager_UartParityDisabled;
*   uartConfig.stopBitCount = kSerialManager_UartOneStopBit;
*   uartConfig.enableRx = 1;
*   uartConfig.enableTx = 1;
*   uartConfig.enableRxRTS = 0;
*   uartConfig.enableTxCTS = 0;
*   config.portConfig = &uartConfig;
*   SerialManager_Init((serial_handle_t)s_serialHandle, &config);
*

```

For USB CDC,

```

*   #define SERIAL_MANAGER_RING_BUFFER_SIZE (256U)
*   static SERIAL_MANAGER_HANDLE_DEFINE(s_serialHandle);
*   static uint8_t s_ringBuffer[SERIAL_MANAGER_RING_BUFFER_SIZE];
*
*   serial_manager_config_t config;
*   serial_port_usb_cdc_config_t usbCdcConfig;
*   config.type = kSerialPort_UsbCdc;
*   config.ringBuffer = &s_ringBuffer[0];
*   config.ringBufferSize = SERIAL_MANAGER_RING_BUFFER_SIZE;
*   usbCdcConfig.controllerIndex = kSerialManager_UsbControllerKhci0;
*   config.portConfig = &usbCdcConfig;
*   SerialManager_Init((serial_handle_t)s_serialHandle, &config);
*

```

Parameters

<i>serialHandle</i>	Pointer to point to a memory space of size SERIAL_MANAGER_HANDLE_SIZE allocated by the caller. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: SERIAL_MANAGER_HANDLE_DEFINE(serialHandle) ; or <code>uint32_t serialHandle[((SERIAL_MANAGER_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))];</code>
<i>config</i>	Pointer to user-defined configuration structure.

Return values

<i>kStatus_SerialManager_Error</i>	An error occurred.
<i>kStatus_SerialManager_Success</i>	The Serial Manager module initialization succeed.

44.5.2 **serial_manager_status_t SerialManager_Deinit (serial_handle_t serialHandle)**

This function de-initializes the serial manager module instance. If the opened writing or reading handle is not closed, the function will return [kStatus_SerialManager_Busy](#).

Parameters

<i>serialHandle</i>	The serial manager module handle pointer.
---------------------	---

Return values

<i>kStatus_SerialManager_-Success</i>	The serial manager de-initialization succeed.
<i>kStatus_SerialManager_-Busy</i>	Opened reading or writing handle is not closed.

44.5.3 **serial_manager_status_t SerialManager_OpenWriteHandle (serial_handle_t *serialHandle*, serial_write_handle_t *writeHandle*)**

This function Opens a writing handle for the serial manager module. If the serial manager needs to be used in different tasks, the task should open a dedicated write handle for itself by calling [SerialManager_OpenWriteHandle](#). Since there can only one buffer for transmission for the writing handle at the same time, multiple writing handles need to be opened when the multiple transmission is needed for a task.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices.
<i>writeHandle</i>	The serial manager module writing handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: SERIAL_MANAGER_WRITE_HANDLE_DEFINE(writeHandle) ; or <code>uint32_t writeHandle[((SERIAL_MANAGER_WRITE_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))];</code>

Return values

<i>kStatus_SerialManager_-Error</i>	An error occurred.
<i>kStatus_SerialManager_-HandleConflict</i>	The writing handle was opened.

<i>kStatus_SerialManager_-Success</i>	The writing handle is opened.
---------------------------------------	-------------------------------

Example below shows how to use this API to write data. For task 1,

```
* static SERIAL_MANAGER_WRITE_HANDLE_DEFINE(s_serialWriteHandle1);
* static uint8_t s_nonBlockingWelcome1[] = "This is non-blocking writing log for task1!\r\n";
* SerialManager_OpenWriteHandle((serial_handle_t)serialHandle
    , (serial_write_handle_t)s_serialWriteHandle1);
* SerialManager_InstallTxCallback((serial_write_handle_t)s_serialWriteHandle1,
    Task1_SerialManagerTxCallback,
    s_serialWriteHandle1);
* SerialManager_WriteNonBlocking((serial_write_handle_t)s_serialWriteHandle1,
    s_nonBlockingWelcome1,
    sizeof(s_nonBlockingWelcome1) - 1U);
*
```

For task 2,

```
* static SERIAL_MANAGER_WRITE_HANDLE_DEFINE(s_serialWriteHandle2);
* static uint8_t s_nonBlockingWelcome2[] = "This is non-blocking writing log for task2!\r\n";
* SerialManager_OpenWriteHandle((serial_handle_t)serialHandle
    , (serial_write_handle_t)s_serialWriteHandle2);
* SerialManager_InstallTxCallback((serial_write_handle_t)s_serialWriteHandle2,
    Task2_SerialManagerTxCallback,
    s_serialWriteHandle2);
* SerialManager_WriteNonBlocking((serial_write_handle_t)s_serialWriteHandle2,
    s_nonBlockingWelcome2,
    sizeof(s_nonBlockingWelcome2) - 1U);
*
```

44.5.4 serial_manager_status_t SerialManager_CloseWriteHandle (serial_write_handle_t *writeHandle*)

This function Closes a writing handle for the serial manager module.

Parameters

<i>writeHandle</i>	The serial manager module writing handle pointer.
--------------------	---

Return values

<i>kStatus_SerialManager_-Success</i>	The writing handle is closed.
---------------------------------------	-------------------------------

44.5.5 serial_manager_status_t SerialManager_OpenReadHandle (serial_handle_t *serialHandle*, serial_read_handle_t *readHandle*)

This function Opens a reading handle for the serial manager module. The reading handle can not be opened multiple at the same time. The error code kStatus_SerialManager_Busy would be returned when

the previous reading handle is not closed. And there can only be one buffer for receiving for the reading handle at the same time.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices.
<i>readHandle</i>	The serial manager module reading handle pointer. The handle should be 4 byte aligned, because unaligned access doesn't be supported on some devices. You can define the handle in the following two ways: SERIAL_MANAGER_READ_HANDLE_DEFINE(readHandle) ; or <code>uint32_t readHandle[((SERIAL_MANAGER_READ_HANDLE_SIZE + sizeof(uint32_t) - 1U) / sizeof(uint32_t))];</code>

Return values

<i>kStatus_SerialManager_Error</i>	An error occurred.
<i>kStatus_SerialManager_Success</i>	The reading handle is opened.
<i>kStatus_SerialManager_Busy</i>	Previous reading handle is not closed.

Example below shows how to use this API to read data.

```
* static SERIAL_MANAGER_READ_HANDLE_DEFINE(s_serialReadHandle);
* SerialManager_OpenReadHandle((serial_handle_t)serialHandle,
*     (serial_read_handle_t)s_serialReadHandle);
* static uint8_t s_nonBlockingBuffer[64];
* SerialManager_InstallRxCallback((serial_read_handle_t)s_serialReadHandle,
*     APP_SerialManagerRxCallback,
*     s_serialReadHandle);
* SerialManager_ReadNonBlocking((serial_read_handle_t)s_serialReadHandle,
*     s_nonBlockingBuffer,
*     sizeof(s_nonBlockingBuffer));
*
```

44.5.6 **serial_manager_status_t SerialManager_CloseReadHandle (serial_read_handle_t *readHandle*)**

This function Closes a reading for the serial manager module.

Parameters

<i>readHandle</i>	The serial manager module reading handle pointer.
-------------------	---

Return values

<i>kStatus_SerialManager_-Success</i>	The reading handle is closed.
---------------------------------------	-------------------------------

44.5.7 `serial_manager_status_t SerialManager_WriteBlocking (serial_write_handle_t writeHandle, uint8_t * buffer, uint32_t length)`

This is a blocking function, which polls the sending queue, waits for the sending queue to be empty. This function sends data using an interrupt method. The interrupt of the hardware could not be disabled. And There can only one buffer for transmission for the writing handle at the same time.

Note

The function `SerialManager_WriteBlocking` and the function `SerialManager_WriteNonBlocking` cannot be used at the same time. And, the function `SerialManager_CancelWriting` cannot be used to abort the transmission of this function.

Parameters

<i>writeHandle</i>	The serial manager module handle pointer.
<i>buffer</i>	Start address of the data to write.
<i>length</i>	Length of the data to write.

Return values

<i>kStatus_SerialManager_-Success</i>	Successfully sent all data.
<i>kStatus_SerialManager_-Busy</i>	Previous transmission still not finished; data not all sent yet.
<i>kStatus_SerialManager_-Error</i>	An error occurred.

44.5.8 `serial_manager_status_t SerialManager_ReadBlocking (serial_read_handle_t readHandle, uint8_t * buffer, uint32_t length)`

This is a blocking function, which polls the receiving buffer, waits for the receiving buffer to be full. This function receives data using an interrupt method. The interrupt of the hardware could not be disabled. And There can only one buffer for receiving for the reading handle at the same time.

Note

The function `SerialManager_ReadBlocking` and the function `SerialManager_ReadNonBlocking` cannot be used at the same time. And, the function `SerialManager_CancelReading` cannot be used to abort the transmission of this function.

Parameters

<i>readHandle</i>	The serial manager module handle pointer.
<i>buffer</i>	Start address of the data to store the received data.
<i>length</i>	The length of the data to be received.

Return values

<i>kStatus_SerialManager_-Success</i>	Successfully received all data.
<i>kStatus_SerialManager_-Busy</i>	Previous transmission still not finished; data not all received yet.
<i>kStatus_SerialManager_-Error</i>	An error occurred.

44.5.9 `serial_manager_status_t SerialManager_EnterLowpower (serial_handle_t serialHandle)`

This function is used to prepare to enter low power consumption.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer.
---------------------	---

Return values

<i>kStatus_SerialManager_-Success</i>	Successful operation.
---------------------------------------	-----------------------

44.5.10 `serial_manager_status_t SerialManager_ExitLowpower (serial_handle_t serialHandle)`

This function is used to restore from low power consumption.

Parameters

<i>serialHandle</i>	The serial manager module handle pointer.
---------------------	---

Return values

<i>kStatus_SerialManager_-Success</i>	Successful operation.
---------------------------------------	-----------------------

44.5.11 static bool SerialManager_needPollingIsr(void) [inline], [static]

This function is used to check if need polling ISR.

Return values

<i>TRUE</i>	if need polling.
-------------	------------------

Chapter 45

Lpspi_cmsis_driver

This section describes the programming interface of the LP SPI Cortex Microcontroller Software Interface Standard (CMSIS) driver. And this driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method please refer to <http://www.-keil.com/pack/doc/cmsis/Driver/html/index.html>.

45.1 Function groups

45.1.1 LP SPI CMSIS GetVersion Operation

This function group will return the DSPI CMSIS Driver version to user.

45.1.2 LP SPI CMSIS GetCapabilities Operation

This function group will return the capabilities of this driver.

45.1.3 LP SPI CMSIS Initialize and Uninitialize Operation

This function will initialize and uninitialized the instance in master mode or slave mode. And this API must be called before you configure an instance or after you Deinit an instance. The right steps to start an instance is that you must initialize the instance which been selected firstly, then you can power on the instance. After these all have been done, you can configure the instance by using control operation. If you want to Uninitialize the instance, you must power off the instance first.

45.1.4 LP SPI Transfer Operation

This function group controls the transfer, master send/receive data, and slave send/receive data.

45.1.5 LP SPI Status Operation

This function group gets the LP SPI transfer status.

45.1.6 LPSPI CMSIS Control Operation

This function can select instance as master mode or slave mode, set baudrate for master mode transfer, get current baudrate of master mode transfer, set transfer data bits and set other control command.

45.2 Typical use case

45.2.1 Master Operation

```
/* Variables */
uint8_t masterRxData[TRANSFER_SIZE] = {0U};
uint8_t masterTxData[TRANSFER_SIZE] = {0U};

/*DSPI master init*/
Driver_SPI0.Initialize(DSPI_MasterSignalEvent_t);
Driver_SPI0.PowerControl(ARM_POWER_FULL);
Driver_SPI0.Control(ARM_SPI_MODE_MASTER, TRANSFER_BAUDRATE);

/* Start master transfer */
Driver_SPI0.Transfer(masterTxData, masterRxData, TRANSFER_SIZE);

/* Master power off */
Driver_SPI0.PowerControl(ARM_POWER_OFF);

/* Master uninitialize */
Driver_SPI0.Uninitialize();
```

45.2.2 Slave Operation

```
/* Variables */
uint8_t slaveRxData[TRANSFER_SIZE] = {0U};
uint8_t slaveTxData[TRANSFER_SIZE] = {0U};

/*DSPI slave init*/
Driver_SPI2.Initialize(DSPI_SlaveSignalEvent_t);
Driver_SPI2.PowerControl(ARM_POWER_FULL);
Driver_SPI2.Control(ARM_SPI_MODE_SLAVE, false);

/* Start slave transfer */
Driver_SPI2.Transfer(slaveTxData, slaveRxData, TRANSFER_SIZE);

/* slave power off */
Driver_SPI2.PowerControl(ARM_POWER_OFF);

/* slave uninitialize */
Driver_SPI2.Uninitialize();
```

Chapter 46

Lpuart_cmsis_driver

This section describes the programming interface of the LPUART Cortex Microcontroller Software Interface Standard (CMSIS) driver. And this driver defines generic peripheral driver interfaces for middleware making it reusable across a wide range of supported microcontroller devices. The API connects microcontroller peripherals with middleware that implements for example communication stacks, file systems, or graphic user interfaces. More information and usage method please refer to <http://www.keil.com/pack/doc/cmsis/Driver/html/index.html>.

The LPUART driver includes transactional APIs.

Transactional APIs can be used to enable the peripheral quickly and in the application if the code size and performance of transactional APIs can satisfy the requirements. If the code size and performance are critical requirements please write custom code.

46.1 Function groups

46.1.1 LPUART CMSIS GetVersion Operation

This function group will return the LPUART CMSIS Driver version to user.

46.1.2 LPUART CMSIS GetCapabilities Operation

This function group will return the capabilities of this driver.

46.1.3 LPUART CMSIS Initialize and Uninitialize Operation

This function will initialize and uninitialized the lpuart instance . And this API must be called before you configure a lpuart instance or after you Deinit a lpuart instance.The right steps to start an instance is that you must initialize the instance which been selected firstly,then you can power on the instance.After these all have been done,you can configure the instance by using control operation.If you want to Uninitialize the instance, you must power off the instance first.

46.1.4 LPUART CMSIS Transfer Operation

This function group controls the transfer, send/receive data.

46.1.5 LPUART CMSIS Status Operation

This function group gets the LPUART transfer status.

46.1.6 LPUART CMSIS Control Operation

This function can configure an instance ,set baudrate for lpuart, get current baudrate ,set transfer data bits and other control command.

Chapter 47

Flexio_edma_i2s

47.1 Overview

Data Structures

- struct `flexio_i2s_edma_handle_t`

FlexIO I2S DMA transfer handle, users should not touch the content of the handle. [More...](#)

Typedefs

- typedef void(* `flexio_i2s_edma_callback_t`)(`FLEXIO_I2S_Type` *base, `flexio_i2s_edma_handle_t` *handle, `status_t` status, void *userData)

FlexIO I2S eDMA transfer callback function for finish and error.

Driver version

- #define `FSL_FLEXIO_I2S_EDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 1, 7)`)

FlexIO I2S EDMA driver version 2.1.7.

eDMA Transactional

- void `FLEXIO_I2S_TransferTxCreateHandleEDMA` (`FLEXIO_I2S_Type` *base, `flexio_i2s_edma_handle_t` *handle, `flexio_i2s_edma_callback_t` callback, void *userData, `edma_handle_t` *dmaHandle)
Initializes the FlexIO I2S eDMA handle.
- void `FLEXIO_I2S_TransferRxCreateHandleEDMA` (`FLEXIO_I2S_Type` *base, `flexio_i2s_edma_handle_t` *handle, `flexio_i2s_edma_callback_t` callback, void *userData, `edma_handle_t` *dmaHandle)
Initializes the FlexIO I2S Rx eDMA handle.
- void `FLEXIO_I2S_TransferSetFormatEDMA` (`FLEXIO_I2S_Type` *base, `flexio_i2s_edma_handle_t` *handle, `flexio_i2s_format_t` *format, uint32_t srcClock_Hz)
Configures the FlexIO I2S Tx audio format.
- `status_t FLEXIO_I2S_TransferSendEDMA` (`FLEXIO_I2S_Type` *base, `flexio_i2s_edma_handle_t` *handle, `flexio_i2s_transfer_t` *xfer)
Performs a non-blocking FlexIO I2S transfer using DMA.
- `status_t FLEXIO_I2S_TransferReceiveEDMA` (`FLEXIO_I2S_Type` *base, `flexio_i2s_edma_handle_t` *handle, `flexio_i2s_transfer_t` *xfer)
Performs a non-blocking FlexIO I2S receive using eDMA.
- void `FLEXIO_I2S_TransferAbortSendEDMA` (`FLEXIO_I2S_Type` *base, `flexio_i2s_edma_handle_t` *handle)
Aborts a FlexIO I2S transfer using eDMA.
- void `FLEXIO_I2S_TransferAbortReceiveEDMA` (`FLEXIO_I2S_Type` *base, `flexio_i2s_edma_handle_t` *handle)
Aborts a FlexIO I2S receive using eDMA.

- **status_t FLEXIO_I2S_TransferGetSendCountEDMA** (**FLEXIO_I2S_Type** *base, **flexio_i2s_edma_handle_t** *handle, **size_t** *count)
Gets the remaining bytes to be sent.
- **status_t FLEXIO_I2S_TransferGetReceiveCountEDMA** (**FLEXIO_I2S_Type** *base, **flexio_i2s_edma_handle_t** *handle, **size_t** *count)
Get the remaining bytes to be received.

47.2 Data Structure Documentation

47.2.1 struct _flexio_i2s_edma_handle

Data Fields

- **edma_handle_t * dmaHandle**
DMA handler for FlexIO I2S send.
- **uint8_t bytesPerFrame**
Bytes in a frame.
- **uint8_t nbytes**
eDMA minor byte transfer count initially configured.
- **uint32_t state**
Internal state for FlexIO I2S eDMA transfer.
- **flexio_i2s_edma_callback_t callback**
Callback for users while transfer finish or error occurred.
- **void * userData**
User callback parameter.
- **edma_tcd_t tcd [FLEXIO_I2S_XFER_QUEUE_SIZE+1U]**
TCD pool for eDMA transfer.
- **flexio_i2s_transfer_t queue [FLEXIO_I2S_XFER_QUEUE_SIZE]**
Transfer queue storing queued transfer.
- **size_t transferSize [FLEXIO_I2S_XFER_QUEUE_SIZE]**
Data bytes need to transfer.
- **volatile uint8_t queueUser**
Index for user to queue transfer.
- **volatile uint8_t queueDriver**
Index for driver to get the transfer data and size.

Field Documentation

- (1) **uint8_t flexio_i2s_edma_handle_t::nbytes**
- (2) **edma_tcd_t flexio_i2s_edma_handle_t::tcd[FLEXIO_I2S_XFER_QUEUE_SIZE+1U]**
- (3) **flexio_i2s_transfer_t flexio_i2s_edma_handle_t::queue[FLEXIO_I2S_XFER_QUEUE_SIZE]**
- (4) **volatile uint8_t flexio_i2s_edma_handle_t::queueUser**

47.3 Macro Definition Documentation

47.3.1 #define FSL_FLEXIO_I2S_EDMA_DRIVER_VERSION (MAKE_VERSION(2, 1, 7))

47.4 Function Documentation

**47.4.1 void FLEXIO_I2S_TransferTxCreateHandleEDMA (FLEXIO_I2S_Type *
base, flexio_i2s_edma_handle_t * *handle*, flexio_i2s_edma_callback_t
callback, void * *userData*, edma_handle_t * *dmaHandle*)**

This function initializes the FlexIO I2S master DMA handle which can be used for other FlexIO I2S master transactional APIs. Usually, for a specified FlexIO I2S instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S eDMA handle pointer.
<i>callback</i>	FlexIO I2S eDMA callback function called while finished a block.
<i>userData</i>	User parameter for callback.
<i>dmaHandle</i>	eDMA handle for FlexIO I2S. This handle is a static value allocated by users.

**47.4.2 void FLEXIO_I2S_TransferRxCreateHandleEDMA (FLEXIO_I2S_Type *
base, flexio_i2s_edma_handle_t * *handle*, flexio_i2s_edma_callback_t
callback, void * *userData*, edma_handle_t * *dmaHandle*)**

This function initializes the FlexIO I2S slave DMA handle which can be used for other FlexIO I2S master transactional APIs. Usually, for a specified FlexIO I2S instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S eDMA handle pointer.
<i>callback</i>	FlexIO I2S eDMA callback function called while finished a block.
<i>userData</i>	User parameter for callback.

<i>dmaHandle</i>	eDMA handle for FlexIO I2S. This handle is a static value allocated by users.
------------------	---

47.4.3 void FLEXIO_I2S_TransferSetFormatEDMA (**FLEXIO_I2S_Type** * *base*, **flexio_i2s_edma_handle_t** * *handle*, **flexio_i2s_format_t** * *format*, **uint32_t** *srcClock_Hz*)

Audio format can be changed in run-time of FlexIO I2S. This function configures the sample rate and audio data format to be transferred. This function also sets the eDMA parameter according to format.

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S eDMA handle pointer
<i>format</i>	Pointer to FlexIO I2S audio data format structure.
<i>srcClock_Hz</i>	FlexIO I2S clock source frequency in Hz, it should be 0 while in slave mode.

47.4.4 status_t FLEXIO_I2S_TransferSendEDMA (**FLEXIO_I2S_Type** * *base*, **flexio_i2s_edma_handle_t** * *handle*, **flexio_i2s_transfer_t** * *xfer*)

Note

This interface returned immediately after transfer initiates. Users should call FLEXIO_I2S_GetTransferStatus to poll the transfer status and check whether the FlexIO I2S transfer is finished.

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S DMA handle pointer.
<i>xfer</i>	Pointer to DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a FlexIO I2S eDMA send successfully.
<i>kStatus_InvalidArgument</i>	The input arguments is invalid.

<i>kStatus_TxBusy</i>	FlexIO I2S is busy sending data.
-----------------------	----------------------------------

47.4.5 **status_t FLEXIO_I2S_TransferReceiveEDMA (FLEXIO_I2S_Type * *base*, flexio_i2s_edma_handle_t * *handle*, flexio_i2s_transfer_t * *xfer*)**

Note

This interface returned immediately after transfer initiates. Users should call FLEXIO_I2S_GetReceiveRemainingBytes to poll the transfer status and check whether the FlexIO I2S transfer is finished.

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S DMA handle pointer.
<i>xfer</i>	Pointer to DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a FlexIO I2S eDMA receive successfully.
<i>kStatus_InvalidArgument</i>	The input arguments is invalid.
<i>kStatus_RxBusy</i>	FlexIO I2S is busy receiving data.

47.4.6 **void FLEXIO_I2S_TransferAbortSendEDMA (FLEXIO_I2S_Type * *base*, flexio_i2s_edma_handle_t * *handle*)**

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S DMA handle pointer.

47.4.7 **void FLEXIO_I2S_TransferAbortReceiveEDMA (FLEXIO_I2S_Type * *base*, flexio_i2s_edma_handle_t * *handle*)**

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S DMA handle pointer.

47.4.8 status_t FLEXIO_I2S_TransferGetSendCountEDMA (**FLEXIO_I2S_Type** * *base*, **flexio_i2s_edma_handle_t** * *handle*, **size_t** * *count*)

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S DMA handle pointer.
<i>count</i>	Bytes sent.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.

47.4.9 status_t FLEXIO_I2S_TransferGetReceiveCountEDMA (**FLEXIO_I2S_Type** * *base*, **flexio_i2s_edma_handle_t** * *handle*, **size_t** * *count*)

Parameters

<i>base</i>	FlexIO I2S peripheral base address.
<i>handle</i>	FlexIO I2S DMA handle pointer.
<i>count</i>	Bytes received.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is not a non-blocking transaction currently in progress.

Chapter 48

Flexio_edma_spi

48.1 Overview

Data Structures

- struct `flexio_spi_master_edma_handle_t`

FlexIO SPI eDMA transfer handle, users should not touch the content of the handle. More...

Typedefs

- typedef `flexio_spi_master_edma_handle_t flexio_spi_slave_edma_handle_t`
Slave handle is the same with master handle.
- typedef void(* `flexio_spi_master_edma_transfer_callback_t`)(`FLEXIO_SPI_Type` *base, `flexio_spi_master_edma_handle_t` *handle, `status_t` status, void *userData)
FlexIO SPI master callback for finished transmit.
- typedef void(* `flexio_spi_slave_edma_transfer_callback_t`)(`FLEXIO_SPI_Type` *base, `flexio_spi_slave_edma_handle_t` *handle, `status_t` status, void *userData)
FlexIO SPI slave callback for finished transmit.

Driver version

- #define `FSL_FLEXIO_SPI_EDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 2, 1)`)
FlexIO SPI EDMA driver version.

eDMA Transactional

- `status_t FLEXIO_SPI_MasterTransferCreateHandleEDMA` (`FLEXIO_SPI_Type` *base, `flexio_spi_master_edma_handle_t` *handle, `flexio_spi_master_edma_transfer_callback_t` callback, void *userData, `edma_handle_t` *txHandle, `edma_handle_t` *rxHandle)
Initializes the FlexIO SPI master eDMA handle.
- `status_t FLEXIO_SPI_MasterTransferEDMA` (`FLEXIO_SPI_Type` *base, `flexio_spi_master_edma_handle_t` *handle, `flexio_spi_transfer_t` *xfer)
Performs a non-blocking FlexIO SPI transfer using eDMA.
- `void FLEXIO_SPI_MasterTransferAbortEDMA` (`FLEXIO_SPI_Type` *base, `flexio_spi_master_edma_handle_t` *handle)
Aborts a FlexIO SPI transfer using eDMA.
- `status_t FLEXIO_SPI_MasterTransferGetCountEDMA` (`FLEXIO_SPI_Type` *base, `flexio_spi_master_edma_handle_t` *handle, `size_t` *count)
Gets the number of bytes transferred so far using FlexIO SPI master eDMA.
- static void `FLEXIO_SPI_SlaveTransferCreateHandleEDMA` (`FLEXIO_SPI_Type` *base, `flexio_spi_slave_edma_handle_t` *handle, `flexio_spi_slave_edma_transfer_callback_t` callback, void *userData, `edma_handle_t` *txHandle, `edma_handle_t` *rxHandle)
Initializes the FlexIO SPI slave eDMA handle.

- **status_t FLEXIO_SPI_SlaveTransferEDMA** (**FLEXIO_SPI_Type** *base, **flexio_spi_slave_edma_handle_t** *handle, **flexio_spi_transfer_t** *xfer)
Performs a non-blocking FlexIO SPI transfer using eDMA.
- **static void FLEXIO_SPI_SlaveTransferAbortEDMA** (**FLEXIO_SPI_Type** *base, **flexio_spi_slave_edma_handle_t** *handle)
Aborts a FlexIO SPI transfer using eDMA.
- **static status_t FLEXIO_SPI_SlaveTransferGetCountEDMA** (**FLEXIO_SPI_Type** *base, **flexio_spi_slave_edma_handle_t** *handle, **size_t** *count)
Gets the number of bytes transferred so far using FlexIO SPI slave eDMA.

48.2 Data Structure Documentation

48.2.1 struct _flexio_spi_master_edma_handle

typedef for **flexio_spi_master_edma_handle_t** in advance.

Data Fields

- **size_t transferSize**
Total bytes to be transferred.
- **uint8_t nbytes**
eDMA minor byte transfer count initially configured.
- **bool txInProgress**
Send transfer in progress.
- **bool rxInProgress**
Receive transfer in progress.
- **edma_handle_t * txHandle**
DMA handler for SPI send.
- **edma_handle_t * rxHandle**
DMA handler for SPI receive.
- **flexio_spi_master_edma_transfer_callback_t callback**
Callback for SPI DMA transfer.
- **void * userData**
User Data for SPI DMA callback.

Field Documentation

- (1) **size_t flexio_spi_master_edma_handle_t::transferSize**
- (2) **uint8_t flexio_spi_master_edma_handle_t::nbytes**

48.3 Macro Definition Documentation

48.3.1 #define FSL_FLEXIO_SPI_EDMA_DRIVER_VERSION (MAKE_VERSION(2, 2, 1))

48.4 Typedef Documentation

48.4.1 typedef flexio_spi_master_edma_handle_t flexio_spi_slave_edma_handle_t**48.5 Function Documentation****48.5.1 status_t FLEXIO_SPI_MasterTransferCreateHandleEDMA (**FLEXIO_SPI_Type** * *base*, **flexio_spi_master_edma_handle_t** * *handle*, **flexio_spi_master_edma_transfer_callback_t** *callback*, **void** * *userData*, **edma_handle_t** * *txHandle*, **edma_handle_t** * *rxHandle*)**

This function initializes the FlexIO SPI master eDMA handle which can be used for other FlexIO SPI master transactional APIs. For a specified FlexIO SPI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	Pointer to FLEXIO_SPI_Type structure.
<i>handle</i>	Pointer to flexio_spi_master_edma_handle_t structure to store the transfer state.
<i>callback</i>	SPI callback, NULL means no callback.
<i>userData</i>	callback function parameter.
<i>txHandle</i>	User requested eDMA handle for FlexIO SPI RX eDMA transfer.
<i>rxHandle</i>	User requested eDMA handle for FlexIO SPI TX eDMA transfer.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO SPI eDMA type/handle table out of range.

48.5.2 status_t FLEXIO_SPI_MasterTransferEDMA (**FLEXIO_SPI_Type * *base*, **flexio_spi_master_edma_handle_t** * *handle*, **flexio_spi_transfer_t** * *xfer*)**

Note

This interface returns immediately after transfer initiates. Call [FLEXIO_SPI_MasterGetTransferCountEDMA](#) to poll the transfer status and check whether the FlexIO SPI transfer is finished.

Parameters

<i>base</i>	Pointer to FLEXIO_SPI_Type structure.
<i>handle</i>	Pointer to <code>flexio_spi_master_edma_handle_t</code> structure to store the transfer state.
<i>xfer</i>	Pointer to FlexIO SPI transfer structure.

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_FLEXIO_SPI_Busy</i>	FlexIO SPI is not idle, is running another transfer.

48.5.3 void [FLEXIO_SPI_MasterTransferAbortEDMA](#) (`FLEXIO_SPI_Type * base,` `flexio_spi_master_edma_handle_t * handle`)

Parameters

<i>base</i>	Pointer to FLEXIO_SPI_Type structure.
<i>handle</i>	FlexIO SPI eDMA handle pointer.

48.5.4 status_t [FLEXIO_SPI_MasterTransferGetCountEDMA](#) (`FLEXIO_SPI_Type * base,` `flexio_spi_master_edma_handle_t * handle,` `size_t * count`)

Parameters

<i>base</i>	Pointer to FLEXIO_SPI_Type structure.
<i>handle</i>	FlexIO SPI eDMA handle pointer.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

48.5.5 static void [FLEXIO_SPI_SlaveTransferCreateHandleEDMA](#) (`FLEXIO_SPI_Type * base,` `flexio_spi_slave_edma_handle_t * handle,` `flexio_spi_slave_edma_transfer_callback_t callback,` `void * userData,` `edma_handle_t * txHandle,` `edma_handle_t * rxHandle`) [inline], [static]

This function initializes the FlexIO SPI slave eDMA handle.

Parameters

<i>base</i>	Pointer to FLEXIO_SPI_Type structure.
<i>handle</i>	Pointer to <code>flexio_spi_slave_edma_handle_t</code> structure to store the transfer state.
<i>callback</i>	SPI callback, NULL means no callback.
<i>userData</i>	callback function parameter.
<i>txHandle</i>	User requested eDMA handle for FlexIO SPI TX eDMA transfer.
<i>rxHandle</i>	User requested eDMA handle for FlexIO SPI RX eDMA transfer.

48.5.6 `status_t FLEXIO_SPI_SlaveTransferEDMA (FLEXIO_SPI_Type * base, flexio_spi_slave_edma_handle_t * handle, flexio_spi_transfer_t * xfer)`

Note

This interface returns immediately after transfer initiates. Call `FLEXIO_SPI_SlaveGetTransferCountEDMA` to poll the transfer status and check whether the FlexIO SPI transfer is finished.

Parameters

<i>base</i>	Pointer to FLEXIO_SPI_Type structure.
<i>handle</i>	Pointer to <code>flexio_spi_slave_edma_handle_t</code> structure to store the transfer state.
<i>xfer</i>	Pointer to FlexIO SPI transfer structure.

Return values

<i>kStatus_Success</i>	Successfully start a transfer.
<i>kStatus_InvalidArgument</i>	Input argument is invalid.
<i>kStatus_FLEXIO_SPI_Busy</i>	FlexIO SPI is not idle, is running another transfer.

48.5.7 `static void FLEXIO_SPI_SlaveTransferAbortEDMA (FLEXIO_SPI_Type * base, flexio_spi_slave_edma_handle_t * handle) [inline], [static]`

Parameters

<i>base</i>	Pointer to FLEXIO_SPI_Type structure.
<i>handle</i>	Pointer to <code>flexio_spi_slave_edma_handle_t</code> structure to store the transfer state.

48.5.8 static status_t FLEXIO_SPI_SlaveTransferGetCountEDMA (
`FLEXIO_SPI_Type * base, flexio_spi_slave_edma_handle_t * handle,`
`size_t * count) [inline], [static]`

Parameters

<i>base</i>	Pointer to FLEXIO_SPI_Type structure.
<i>handle</i>	FlexIO SPI eDMA handle pointer.
<i>count</i>	Number of bytes transferred so far by the non-blocking transaction.

Chapter 49

Flexio_edma_uart

49.1 Overview

Data Structures

- struct `flexio_uart_edma_handle_t`
UART eDMA handle. [More...](#)

Typedefs

- typedef void(* `flexio_uart_edma_transfer_callback_t`)(`FLEXIO_UART_Type` *base, `flexio_uart_edma_handle_t` *handle, `status_t` status, void *userData)
UART transfer callback function.

Driver version

- #define `FSL_FLEXIO_UART_EDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 4, 1)`)
FlexIO UART EDMA driver version.

eDMA transactional

- `status_t FLEXIO_UART_TransferCreateHandleEDMA` (`FLEXIO_UART_Type` *base, `flexio_uart_edma_handle_t` *handle, `flexio_uart_edma_transfer_callback_t` callback, void *userData, `edma_handle_t` *txEdmaHandle, `edma_handle_t` *rxEdmaHandle)
Initializes the UART handle which is used in transactional functions.
- `status_t FLEXIO_UART_TransferSendEDMA` (`FLEXIO_UART_Type` *base, `flexio_uart_edma_handle_t` *handle, `flexio_uart_transfer_t` *xfer)
Sends data using eDMA.
- `status_t FLEXIO_UART_TransferReceiveEDMA` (`FLEXIO_UART_Type` *base, `flexio_uart_edma_handle_t` *handle, `flexio_uart_transfer_t` *xfer)
Receives data using eDMA.
- void `FLEXIO_UART_TransferAbortSendEDMA` (`FLEXIO_UART_Type` *base, `flexio_uart_edma_handle_t` *handle)
Aborts the sent data which using eDMA.
- void `FLEXIO_UART_TransferAbortReceiveEDMA` (`FLEXIO_UART_Type` *base, `flexio_uart_edma_handle_t` *handle)
Aborts the receive data which using eDMA.
- `status_t FLEXIO_UART_TransferGetSendCountEDMA` (`FLEXIO_UART_Type` *base, `flexio_uart_edma_handle_t` *handle, `size_t` *count)
Gets the number of bytes sent out.
- `status_t FLEXIO_UART_TransferGetReceiveCountEDMA` (`FLEXIO_UART_Type` *base, `flexio_uart_edma_handle_t` *handle, `size_t` *count)
Gets the number of bytes received.

49.2 Data Structure Documentation

49.2.1 struct _flexio_uart_edma_handle

Data Fields

- **flexio_uart_edma_transfer_callback_t callback**
Callback function.
- **void *userData**
UART callback function parameter.
- **size_t txDataSizeAll**
Total bytes to be sent.
- **size_t rxDataSizeAll**
Total bytes to be received.
- **edma_handle_t *txEdmaHandle**
The eDMA TX channel used.
- **edma_handle_t *rxEdmaHandle**
The eDMA RX channel used.
- **uint8_t nbytes**
eDMA minor byte transfer count initially configured.
- **volatile uint8_t txState**
TX transfer state.
- **volatile uint8_t rxState**
RX transfer state.

Field Documentation

- (1) **flexio_uart_edma_transfer_callback_t flexio_uart_edma_handle_t::callback**
- (2) **void* flexio_uart_edma_handle_t::userData**
- (3) **size_t flexio_uart_edma_handle_t::txDataSizeAll**
- (4) **size_t flexio_uart_edma_handle_t::rxDataSizeAll**
- (5) **edma_handle_t* flexio_uart_edma_handle_t::txEdmaHandle**
- (6) **edma_handle_t* flexio_uart_edma_handle_t::rxEdmaHandle**
- (7) **uint8_t flexio_uart_edma_handle_t::nbytes**
- (8) **volatile uint8_t flexio_uart_edma_handle_t::txState**

49.3 Macro Definition Documentation

49.3.1 #define FSL_FLEXIO_UART_EDMA_DRIVER_VERSION (MAKE_VERSION(2, 4, 1))

49.4 Typedef Documentation

49.4.1 `typedef void(* flexio_uart_edma_transfer_callback_t)(FLEXIO_UART_Type *base, flexio_uart_edma_handle_t *handle, status_t status, void *userData)`

49.5 Function Documentation

49.5.1 `status_t FLEXIO_UART_TransferCreateHandleEDMA (FLEXIO_UART_Type * base, flexio_uart_edma_handle_t * handle, flexio_uart_edma_transfer_callback_t callback, void * userData, edma_handle_t * txEdmaHandle, edma_handle_t * rxEdmaHandle)`

Parameters

<i>base</i>	Pointer to FLEXIO_UART_Type .
<i>handle</i>	Pointer to <code>flexio_uart_edma_handle_t</code> structure.
<i>callback</i>	The callback function.
<i>userData</i>	The parameter of the callback function.
<i>rxEdmaHandle</i>	User requested DMA handle for RX DMA transfer.
<i>txEdmaHandle</i>	User requested DMA handle for TX DMA transfer.

Return values

<i>kStatus_Success</i>	Successfully create the handle.
<i>kStatus_OutOfRange</i>	The FlexIO SPI eDMA type/handle table out of range.

49.5.2 `status_t FLEXIO_UART_TransferSendEDMA (FLEXIO_UART_Type * base, flexio_uart_edma_handle_t * handle, flexio_uart_transfer_t * xfer)`

This function sends data using eDMA. This is a non-blocking function, which returns right away. When all data is sent out, the send callback function is called.

Parameters

<i>base</i>	Pointer to FLEXIO_UART_Type
<i>handle</i>	UART handle pointer.
<i>xfer</i>	UART eDMA transfer structure, see flexio_uart_transfer_t .

Return values

<i>kStatus_Success</i>	if succeed, others failed.
<i>kStatus_FLEXIO_UART_TxBusy</i>	Previous transfer on going.

49.5.3 **status_t FLEXIO_UART_TransferReceiveEDMA (FLEXIO_UART_Type * *base*, flexio_uart_edma_handle_t * *handle*, flexio_uart_transfer_t * *xfer*)**

This function receives data using eDMA. This is a non-blocking function, which returns right away. When all data is received, the receive callback function is called.

Parameters

<i>base</i>	Pointer to FLEXIO_UART_Type
<i>handle</i>	Pointer to flexio_uart_edma_handle_t structure
<i>xfer</i>	UART eDMA transfer structure, see flexio_uart_transfer_t .

Return values

<i>kStatus_Success</i>	if succeed, others failed.
<i>kStatus_UART_RxBusy</i>	Previous transfer on going.

49.5.4 **void FLEXIO_UART_TransferAbortSendEDMA (FLEXIO_UART_Type * *base*, flexio_uart_edma_handle_t * *handle*)**

This function aborts sent data which using eDMA.

Parameters

<i>base</i>	Pointer to FLEXIO_UART_Type
<i>handle</i>	Pointer to flexio_uart_edma_handle_t structure

49.5.5 **void FLEXIO_UART_TransferAbortReceiveEDMA (FLEXIO_UART_Type * *base*, flexio_uart_edma_handle_t * *handle*)**

This function aborts the receive data which using eDMA.

Parameters

<i>base</i>	Pointer to FLEXIO_UART_Type
<i>handle</i>	Pointer to flexio_uart_edma_handle_t structure

49.5.6 status_t FLEXIO_UART_TransferGetSendCountEDMA ([FLEXIO_UART_Type](#) * *base*, [flexio_uart_edma_handle_t](#) * *handle*, [size_t](#) * *count*)

This function gets the number of bytes sent out.

Parameters

<i>base</i>	Pointer to FLEXIO_UART_Type
<i>handle</i>	Pointer to flexio_uart_edma_handle_t structure
<i>count</i>	Number of bytes sent so far by the non-blocking transaction.

Return values

<i>kStatus_NoTransferIn-Progress</i>	transfer has finished or no transfer in progress.
<i>kStatus_Success</i>	Successfully return the count.

49.5.7 status_t FLEXIO_UART_TransferGetReceiveCountEDMA ([FLEXIO_UART_Type](#) * *base*, [flexio_uart_edma_handle_t](#) * *handle*, [size_t](#) * *count*)

This function gets the number of bytes received.

Parameters

<i>base</i>	Pointer to FLEXIO_UART_Type
<i>handle</i>	Pointer to flexio_uart_edma_handle_t structure
<i>count</i>	Number of bytes received so far by the non-blocking transaction.

Return values

<i>kStatus_NoTransferInProgress</i>	transfer has finished or no transfer in progress.
<i>kStatus_Success</i>	Successfully return the count.

Chapter 50

Lpspi_edma_driver

50.1 Overview

Data Structures

- struct `lpspi_master_edma_handle_t`
LPSPI master eDMA transfer handle structure used for transactional API. [More...](#)
- struct `lpspi_slave_edma_handle_t`
LPSPI slave eDMA transfer handle structure used for transactional API. [More...](#)

Typedefs

- typedef void(* `lpspi_master_edma_transfer_callback_t`)(LPSPI_Type *base, lpspi_master_edma_handle_t *handle, status_t status, void *userData)
Completion callback function pointer type.
- typedef void(* `lpspi_slave_edma_transfer_callback_t`)(LPSPI_Type *base, lpspi_slave_edma_handle_t *handle, status_t status, void *userData)
Completion callback function pointer type.

Functions

- void `LPSPI_MasterTransferCreateHandleEDMA` (LPSPI_Type *base, lpspi_master_edma_handle_t *handle, `lpspi_master_edma_transfer_callback_t` callback, void *userData, `edma_handle_t` *edmaRxRegToRxDataHandle, `edma_handle_t` *edmaTxDataToTxRegHandle)
Initializes the LPSPI master eDMA handle.
- status_t `LPSPI_MasterTransferEDMA` (LPSPI_Type *base, lpspi_master_edma_handle_t *handle, `lpspi_transfer_t` *transfer)
LPSPI master transfers data using eDMA.
- void `LPSPI_MasterTransferAbortEDMA` (LPSPI_Type *base, lpspi_master_edma_handle_t *handle)
LPSPI master aborts a transfer which is using eDMA.
- status_t `LPSPI_MasterTransferGetCountEDMA` (LPSPI_Type *base, lpspi_master_edma_handle_t *handle, size_t *count)
Gets the master eDMA transfer remaining bytes.
- void `LPSPI_SlaveTransferCreateHandleEDMA` (LPSPI_Type *base, lpspi_slave_edma_handle_t *handle, `lpspi_slave_edma_transfer_callback_t` callback, void *userData, `edma_handle_t` *edmaRxRegToRxDataHandle, `edma_handle_t` *edmaTxDataToTxRegHandle)
Initializes the LPSPI slave eDMA handle.
- status_t `LPSPI_SlaveTransferEDMA` (LPSPI_Type *base, lpspi_slave_edma_handle_t *handle, `lpspi_transfer_t` *transfer)
LPSPI slave transfers data using eDMA.
- void `LPSPI_SlaveTransferAbortEDMA` (LPSPI_Type *base, lpspi_slave_edma_handle_t *handle)
LPSPI slave aborts a transfer which is using eDMA.

- **status_t LPSPI_SlaveTransferGetCountEDMA** (LPSPI_Type *base, lpspi_slave_edma_handle_t *handle, size_t *count)
Gets the slave eDMA transfer remaining bytes.

Driver version

- #define **FSL_LPSPI_EDMA_DRIVER_VERSION** (MAKE_VERSION(2, 1, 0))
LPSPI EDMA driver version.

50.2 Data Structure Documentation

50.2.1 struct _lpspi_master_edma_handle

Forward declaration of the **_lpspi_master_edma_handle** typedefs.

Data Fields

- volatile bool **isPcsContinuous**
Is PCS continuous in transfer.
- volatile bool **isByteSwap**
A flag that whether should byte swap.
- volatile uint8_t **fifoSize**
FIFO dataSize.
- volatile uint8_t **rxWatermark**
Rx watermark.
- volatile uint8_t **bytesEachWrite**
Bytes for each write TDR.
- volatile uint8_t **bytesEachRead**
Bytes for each read RDR.
- volatile uint8_t **bytesLastRead**
Bytes for last read RDR.
- volatile bool **isThereExtraRxBytes**
Is there extra RX byte.
- uint8_t *volatile **txData**
Send buffer.
- uint8_t *volatile **rxData**
Receive buffer.
- volatile size_t **txRemainingByteCount**
Number of bytes remaining to send.
- volatile size_t **rxRemainingByteCount**
Number of bytes remaining to receive.
- volatile uint32_t **writeRegRemainingTimes**
Write TDR register remaining times.
- volatile uint32_t **readRegRemainingTimes**
Read RDR register remaining times.
- uint32_t **totalByteCount**
Number of transfer bytes.
- uint32_t **txBuffIfNull**
Used if there is not txData for DMA purpose.

- `uint32_t rxBuffIfNull`
Used if there is not rxData for DMA purpose.
- `uint32_t transmitCommand`
Used to write TCR for DMA purpose.
- `volatile uint8_t state`
LPSPI transfer state , _lpspi_transfer_state.
- `uint8_t nbytes`
eDMA minor byte transfer count initially configured.
- `lpspi_master_edma_transfer_callback_t callback`
Completion callback.
- `void *userData`
Callback user data.
- `edma_handle_t *edmaRxRegToRxDataHandle`
edma_handle_t handle point used for RxReg to RxData buff
- `edma_handle_t *edmaTxDataToTxRegHandle`
edma_handle_t handle point used for TxData to TxReg buff
- `edma_tcd_t lpspiSoftwareTCD [3]`
SoftwareTCD, internal used.

Field Documentation

- (1) `volatile bool lpspi_master_edma_handle_t::isPcsContinuous`
- (2) `volatile bool lpspi_master_edma_handle_t::isByteSwap`
- (3) `volatile uint8_t lpspi_master_edma_handle_t::fifoSize`
- (4) `volatile uint8_t lpspi_master_edma_handle_t::rxWatermark`
- (5) `volatile uint8_t lpspi_master_edma_handle_t::bytesEachWrite`
- (6) `volatile uint8_t lpspi_master_edma_handle_t::bytesEachRead`
- (7) `volatile uint8_t lpspi_master_edma_handle_t::bytesLastRead`
- (8) `volatile bool lpspi_master_edma_handle_t::isThereExtraRxBytes`
- (9) `uint8_t* volatile lpspi_master_edma_handle_t::txData`
- (10) `uint8_t* volatile lpspi_master_edma_handle_t::rxData`
- (11) `volatile size_t lpspi_master_edma_handle_t::txRemainingByteCount`
- (12) `volatile size_t lpspi_master_edma_handle_t::rxRemainingByteCount`
- (13) `volatile uint32_t lpspi_master_edma_handle_t::writeRegRemainingTimes`
- (14) `volatile uint32_t lpspi_master_edma_handle_t::readRegRemainingTimes`
- (15) `uint32_t lpspi_master_edma_handle_t::txBuffIfNull`

- (16) `uint32_t lpspi_master_edma_handle_t::rxBuffIfNull`
- (17) `uint32_t lpspi_master_edma_handle_t::transmitCommand`
- (18) `volatile uint8_t lpspi_master_edma_handle_t::state`
- (19) `uint8_t lpspi_master_edma_handle_t::nbytes`
- (20) `lpspi_master_edma_transfer_callback_t lpspi_master_edma_handle_t::callback`
- (21) `void* lpspi_master_edma_handle_t::userData`

50.2.2 struct _lpspi_slave_edma_handle

Forward declaration of the `_lpspi_slave_edma_handle` typedefs.

Data Fields

- volatile bool `isByteSwap`
A flag that whether should byte swap.
- volatile uint8_t `fifoSize`
FIFO dataSize.
- volatile uint8_t `rxWatermark`
Rx watermark.
- volatile uint8_t `bytesEachWrite`
Bytes for each write TDR.
- volatile uint8_t `bytesEachRead`
Bytes for each read RDR.
- volatile uint8_t `bytesLastRead`
Bytes for last read RDR.
- volatile bool `isThereExtraRxBytes`
Is there extra RX byte.
- uint8_t `nbytes`
eDMA minor byte transfer count initially configured.
- uint8_t *volatile `txData`
Send buffer.
- uint8_t *volatile `rxData`
Receive buffer.
- volatile size_t `txRemainingByteCount`
Number of bytes remaining to send.
- volatile size_t `rxRemainingByteCount`
Number of bytes remaining to receive.
- volatile uint32_t `writeRegRemainingTimes`
Write TDR register remaining times.
- volatile uint32_t `readRegRemainingTimes`
Read RDR register remaining times.
- uint32_t `totalByteCount`
Number of transfer bytes.
- uint32_t `txBuffIfNull`

- `uint32_t rxBuffIfNull`
Used if there is not txData for DMA purpose.
- `volatile uint8_t state`
LPSPI transfer state.
- `uint32_t errorCount`
Error count for slave transfer.
- `lpspi_slave_edma_transfer_callback_t callback`
Completion callback.
- `void *userData`
Callback user data.
- `edma_handle_t *edmaRxRegToRxDataHandle`
edma_handle_t handle point used for RxReg to RxData buff
- `edma_handle_t *edmaTxDataToTxRegHandle`
edma_handle_t handle point used for TxData to TxReg
- `edma_tcd_t lpspiSoftwareTCD [2]`
SoftwareTCD, internal used.

Field Documentation

- (1) `volatile bool lpspi_slave_edma_handle_t::isByteSwap`
- (2) `volatile uint8_t lpspi_slave_edma_handle_t::fifoSize`
- (3) `volatile uint8_t lpspi_slave_edma_handle_t::rxWatermark`
- (4) `volatile uint8_t lpspi_slave_edma_handle_t::bytesEachWrite`
- (5) `volatile uint8_t lpspi_slave_edma_handle_t::bytesEachRead`
- (6) `volatile uint8_t lpspi_slave_edma_handle_t::bytesLastRead`
- (7) `volatile bool lpspi_slave_edma_handle_t::isThereExtraRxBytes`
- (8) `uint8_t lpspi_slave_edma_handle_t::nbytes`
- (9) `uint8_t* volatile lpspi_slave_edma_handle_t::txData`
- (10) `uint8_t* volatile lpspi_slave_edma_handle_t::rxData`
- (11) `volatile size_t lpspi_slave_edma_handle_t::txRemainingByteCount`
- (12) `volatile size_t lpspi_slave_edma_handle_t::rxRemainingByteCount`
- (13) `volatile uint32_t lpspi_slave_edma_handle_t::writeRegRemainingTimes`
- (14) `volatile uint32_t lpspi_slave_edma_handle_t::readRegRemainingTimes`
- (15) `uint32_t lpspi_slave_edma_handle_t::txBuffIfNull`
- (16) `uint32_t lpspi_slave_edma_handle_t::rxBuffIfNull`

- (17) `volatile uint8_t lpspi_slave_edma_handle_t::state`
- (18) `uint32_t lpspi_slave_edma_handle_t::errorCount`
- (19) `lpspi_slave_edma_transfer_callback_t lpspi_slave_edma_handle_t::callback`
- (20) `void* lpspi_slave_edma_handle_t::userData`

50.3 Macro Definition Documentation

50.3.1 `#define FSL_LPSPI_EDMA_DRIVER_VERSION (MAKE_VERSION(2, 1, 0))`

50.4 Typedef Documentation

50.4.1 `typedef void(* lpspi_master_edma_transfer_callback_t)(LPSPI_Type *base, lpspi_master_edma_handle_t *handle, status_t status, void *userData)`

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	Pointer to the handle for the LPSPI master.
<i>status</i>	Success or error code describing whether the transfer completed.
<i>userData</i>	Arbitrary pointer-dataSized value passed from the application.

50.4.2 `typedef void(* lpspi_slave_edma_transfer_callback_t)(LPSPI_Type *base, lpspi_slave_edma_handle_t *handle, status_t status, void *userData)`

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	Pointer to the handle for the LPSPI slave.
<i>status</i>	Success or error code describing whether the transfer completed.
<i>userData</i>	Arbitrary pointer-dataSized value passed from the application.

50.5 Function Documentation

50.5.1 void LPSPI_MasterTransferCreateHandleEDMA (*LPSPI_Type* * *base*, *lpspi_master_edma_handle_t* * *handle*, *lpspi_master_edma_transfer_callback_t* *callback*, *void* * *userData*, *edma_handle_t* * *edmaRxRegToRxDataHandle*, *edma_handle_t* * *edmaTxDataToTxRegHandle*)

This function initializes the LPSPI eDMA handle which can be used for other LPSPI transactional APIs. Usually, for a specified LPSPI instance, call this API once to get the initialized handle.

Note that the LPSPI eDMA has a separated (Rx and Rx as two sources) or shared (Rx and Tx are the same source) DMA request source. (1) For a separated DMA request source, enable and set the Rx DMAMUX source for edmaRxRegToRxDataHandle and Tx DMAMUX source for edmaIntermediaryToTxRegHandle. (2) For a shared DMA request source, enable and set the Rx/Rx DMAMUX source for edmaRxRegToRxDataHandle.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	LPSPI handle pointer to <i>lpspi_master_edma_handle_t</i> .
<i>callback</i>	LPSPI callback.
<i>userData</i>	callback function parameter.
<i>edmaRxRegToRxDataHandle</i>	edmaRxRegToRxDataHandle pointer to <i>edma_handle_t</i> .
<i>edmaTxDataToTxRegHandle</i>	edmaTxDataToTxRegHandle pointer to <i>edma_handle_t</i> .

50.5.2 *status_t* LPSPI_MasterTransferEDMA (*LPSPI_Type* * *base*, *lpspi_master_edma_handle_t* * *handle*, *lpspi_transfer_t* * *transfer*)

This function transfers data using eDMA. This is a non-blocking function, which returns right away. When all data is transferred, the callback function is called.

Note: The transfer data size should be an integer multiple of bytesPerFrame if bytesPerFrame is less than or equal to 4. For bytesPerFrame greater than 4: The transfer data size should be equal to bytesPerFrame if the bytesPerFrame is not an integer multiple of 4. Otherwise, the transfer data size can be an integer multiple of bytesPerFrame.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to <code>lpspi_master_edma_handle_t</code> structure which stores the transfer state.
<i>transfer</i>	pointer to <code>lpspi_transfer_t</code> structure.

Returns

status of `status_t`.

50.5.3 `void LPSPI_MasterTransferAbortEDMA (LPSPI_Type * base, lpspi_master_edma_handle_t * handle)`

This function aborts a transfer which is using eDMA.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to <code>lpspi_master_edma_handle_t</code> structure which stores the transfer state.

50.5.4 `status_t LPSPI_MasterTransferGetCountEDMA (LPSPI_Type * base, lpspi_master_edma_handle_t * handle, size_t * count)`

This function gets the master eDMA transfer remaining bytes.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to <code>lpspi_master_edma_handle_t</code> structure which stores the transfer state.
<i>count</i>	Number of bytes transferred so far by the EDMA transaction.

Returns

status of `status_t`.

50.5.5 `void LPSPI_SlaveTransferCreateHandleEDMA (LPSPI_Type * base, lpspi_slave_edma_handle_t * handle, lpspi_slave_edma_transfer_callback_t callback, void * userData, edma_handle_t * edmaRxRegToRxDataHandle, edma_handle_t * edmaTxDataToTxRegHandle)`

This function initializes the LPSPI eDMA handle which can be used for other LPSPI transactional APIs. Usually, for a specified LPSPI instance, call this API once to get the initialized handle.

Note that LPSPI eDMA has a separated (Rx and Tx as two sources) or shared (Rx and Tx as the same source) DMA request source.

(1) For a separated DMA request source, enable and set the Rx DMAMUX source for edmaRxRegToRxDataHandle and Tx DMAMUX source for edmaTxDataToTxRegHandle. (2) For a shared DMA request source, enable and set the Rx/Rx DMAMUX source for edmaRxRegToRxDataHandle .

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	LPSPI handle pointer to lpspi_slave_edma_handle_t.
<i>callback</i>	LPSPI callback.
<i>userData</i>	callback function parameter.
<i>edmaRxRegToRxDataHandle</i>	edmaRxRegToRxDataHandle pointer to edma_handle_t .
<i>edmaTxDataToTxRegHandle</i>	edmaTxDataToTxRegHandle pointer to edma_handle_t .

50.5.6 status_t LPSPI_SlaveTransferEDMA (**LPSPI_Type** * *base*, **lpspi_slave_edma_handle_t** * *handle*, **lpspi_transfer_t** * *transfer*)

This function transfers data using eDMA. This is a non-blocking function, which return right away. When all data is transferred, the callback function is called.

Note: The transfer data size should be an integer multiple of bytesPerFrame if bytesPerFrame is less than or equal to 4. For bytesPerFrame greater than 4: The transfer data size should be equal to bytesPerFrame if the bytesPerFrame is not an integer multiple of 4. Otherwise, the transfer data size can be an integer multiple of bytesPerFrame.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to lpspi_slave_edma_handle_t structure which stores the transfer state.
<i>transfer</i>	pointer to lpspi_transfer_t structure.

Returns

status of status_t.

50.5.7 void LPSPI_SlaveTransferAbortEDMA (LPSPI_Type * *base*, lpspi_slave_edma_handle_t * *handle*)

This function aborts a transfer which is using eDMA.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to lpspi_slave_edma_handle_t structure which stores the transfer state.

50.5.8 status_t LPSPI_SlaveTransferGetCountEDMA (LPSPI_Type * *base*, lpspi_slave_edma_handle_t * *handle*, size_t * *count*)

This function gets the slave eDMA transfer remaining bytes.

Parameters

<i>base</i>	LPSPI peripheral base address.
<i>handle</i>	pointer to lpspi_slave_edma_handle_t structure which stores the transfer state.
<i>count</i>	Number of bytes transferred so far by the eDMA transaction.

Returns

status of status_t.

Chapter 51

LPSPI FreeRTOS Driver

51.1 Overview

Driver version

- #define `FSL_LPSPI_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 0, 5))`
LPSPI FreeRTOS driver version 2.0.5.

LPSPI RTOS Operation

- `status_t LPSPI_RTOS_Init (lpspi_rtos_handle_t *handle, LPSPI_Type *base, const lpspi_master_config_t *masterConfig, uint32_t srcClock_Hz)`
Initializes LPSPI.
- `status_t LPSPI_RTOS_Deinit (lpspi_rtos_handle_t *handle)`
Deinitializes the LPSPI.
- `status_t LPSPI_RTOS_Transfer (lpspi_rtos_handle_t *handle, lpspi_transfer_t *transfer)`
Performs SPI transfer.

51.2 Macro Definition Documentation

51.2.1 #define `FSL_LPSPI_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 0, 5))`

51.3 Function Documentation

51.3.1 `status_t LPSPI_RTOS_Init (lpspi_rtos_handle_t * handle, LPSPI_Type * base, const lpspi_master_config_t * masterConfig, uint32_t srcClock_Hz)`

This function initializes the LPSPI module and related RTOS context.

Parameters

<i>handle</i>	The RTOS LPSPI handle, the pointer to an allocated space for RTOS context.
<i>base</i>	The pointer base address of the LPSPI instance to initialize.
<i>masterConfig</i>	Configuration structure to set-up LPSPI in master mode.

<i>srcClock_Hz</i>	Frequency of input clock of the LPSPI module.
--------------------	---

Returns

status of the operation.

51.3.2 status_t LPSPI_RTOS_Deinit (*Ipspi_rtos_handle_t * handle*)

This function deinitializes the LPSPI module and related RTOS context.

Parameters

<i>handle</i>	The RTOS LPSPI handle.
---------------	------------------------

51.3.3 status_t LPSPI_RTOS_Transfer (*Ipspi_rtos_handle_t * handle*, *Ipspi_transfer_t * transfer*)

This function performs an SPI transfer according to data given in the transfer structure.

Parameters

<i>handle</i>	The RTOS LPSPI handle.
<i>transfer</i>	Structure specifying the transfer parameters.

Returns

status of the operation.

Chapter 52

Lpuart_edma_driver

52.1 Overview

Data Structures

- struct `lpuart_edma_handle_t`
LPUART eDMA handle. [More...](#)

Typedefs

- typedef void(* `lpuart_edma_transfer_callback_t`)
(LPUART_Type *base, lpuart_edma_handle_t *handle, `status_t` status, void *userData)
LPUART transfer callback function.

Driver version

- #define `FSL_LPUART_EDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 5, 2)`)
LPUART EDMA driver version.

eDMA transactional

- void `LPUART_TransferCreateHandleEDMA` (LPUART_Type *base, lpuart_edma_handle_t *handle, `lpuart_edma_transfer_callback_t` callback, void *userData, `edma_handle_t` *txEdmaHandle, `edma_handle_t` *rxEdmaHandle)
Initializes the LPUART handle which is used in transactional functions.
- `status_t LPUART_SendEDMA` (LPUART_Type *base, lpuart_edma_handle_t *handle, `lpuart_transfer_t` *xfer)
Sends data using eDMA.
- `status_t LPUART_ReceiveEDMA` (LPUART_Type *base, lpuart_edma_handle_t *handle, `lpuart_transfer_t` *xfer)
Receives data using eDMA.
- void `LPUART_TransferAbortSendEDMA` (LPUART_Type *base, lpuart_edma_handle_t *handle)
Aborts the sent data using eDMA.
- void `LPUART_TransferAbortReceiveEDMA` (LPUART_Type *base, lpuart_edma_handle_t *handle)
Aborts the received data using eDMA.
- `status_t LPUART_TransferGetSendCountEDMA` (LPUART_Type *base, lpuart_edma_handle_t *handle, uint32_t *count)
Gets the number of bytes written to the LPUART TX register.
- `status_t LPUART_TransferGetReceiveCountEDMA` (LPUART_Type *base, lpuart_edma_handle_t *handle, uint32_t *count)
Gets the number of received bytes.
- void `LPUART_TransferEdmaHandleIRQ` (LPUART_Type *base, void *lpuartEdmaHandle)
LPUART eDMA IRQ handle function.

52.2 Data Structure Documentation

52.2.1 struct _lpuart_edma_handle

Data Fields

- `lpuart_edma_transfer_callback_t callback`
Callback function.
- `void *userData`
LPUART callback function parameter.
- `size_t rxDataSizeAll`
Size of the data to receive.
- `size_t txDataSizeAll`
Size of the data to send out.
- `edma_handle_t *txEdmaHandle`
The eDMA TX channel used.
- `edma_handle_t *rxEdmaHandle`
The eDMA RX channel used.
- `uint8_t nbytes`
eDMA minor byte transfer count initially configured.
- `volatile uint8_t txState`
TX transfer state.
- `volatile uint8_t rxState`
RX transfer state.

Field Documentation

- (1) `lpuart_edma_transfer_callback_t lpuart_edma_handle_t::callback`
- (2) `void* lpuart_edma_handle_t::userData`
- (3) `size_t lpuart_edma_handle_t::rxDataSizeAll`
- (4) `size_t lpuart_edma_handle_t::txDataSizeAll`
- (5) `edma_handle_t* lpuart_edma_handle_t::txEdmaHandle`
- (6) `edma_handle_t* lpuart_edma_handle_t::rxEdmaHandle`
- (7) `uint8_t lpuart_edma_handle_t::nbytes`
- (8) `volatile uint8_t lpuart_edma_handle_t::txState`

52.3 Macro Definition Documentation

52.3.1 #define FSL_LPUART_EDMA_DRIVER_VERSION (MAKE_VERSION(2, 5, 2))

52.4 Typedef Documentation

52.4.1 `typedef void(* lpuart_edma_transfer_callback_t)(LPUART_Type *base, lpuart_edma_handle_t *handle, status_t status, void *userData)`

52.5 Function Documentation

52.5.1 `void LPUART_TransferCreateHandleEDMA (LPUART_Type * base, lpuart_edma_handle_t * handle, lpuart_edma_transfer_callback_t callback, void * userData, edma_handle_t * txEdmaHandle, edma_handle_t * rxEdmaHandle)`

Note

This function disables all LPUART interrupts.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	Pointer to lpuart_edma_handle_t structure.
<i>callback</i>	Callback function.
<i>userData</i>	User data.
<i>txEdmaHandle</i>	User requested DMA handle for TX DMA transfer.
<i>rxEdmaHandle</i>	User requested DMA handle for RX DMA transfer.

52.5.2 `status_t LPUART_SendEDMA (LPUART_Type * base, lpuart_edma_handle_t * handle, lpuart_transfer_t * xfer)`

This function sends data using eDMA. This is a non-blocking function, which returns right away. When all data is sent, the send callback function is called.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.
<i>xfer</i>	LPUART eDMA transfer structure. See lpuart_transfer_t .

Return values

<i>kStatus_Success</i>	if succeed, others failed.
<i>kStatus_LPUART_TxBusy</i>	Previous transfer on going.
<i>kStatus_InvalidArgument</i>	Invalid argument.

52.5.3 **status_t LPUART_ReceiveEDMA (LPUART_Type * *base*, lpuart_edma_handle_t * *handle*, lpuart_transfer_t * *xfer*)**

This function receives data using eDMA. This is non-blocking function, which returns right away. When all data is received, the receive callback function is called.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	Pointer to lpuart_edma_handle_t structure.
<i>xfer</i>	LPUART eDMA transfer structure, see lpuart_transfer_t .

Return values

<i>kStatus_Success</i>	if succeed, others fail.
<i>kStatus_LPUART_Rx-Busy</i>	Previous transfer ongoing.
<i>kStatus_InvalidArgument</i>	Invalid argument.

52.5.4 **void LPUART_TransferAbortSendEDMA (LPUART_Type * *base*, lpuart_edma_handle_t * *handle*)**

This function aborts the sent data using eDMA.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	Pointer to lpuart_edma_handle_t structure.

52.5.5 **void LPUART_TransferAbortReceiveEDMA (LPUART_Type * *base*, lpuart_edma_handle_t * *handle*)**

This function aborts the received data using eDMA.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	Pointer to lpuart_edma_handle_t structure.

52.5.6 status_t LPUART_TransferGetSendCountEDMA (LPUART_Type * *base*, lpuart_edma_handle_t * *handle*, uint32_t * *count*)

This function gets the number of bytes written to the LPUART TX register by DMA.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.
<i>count</i>	Send bytes count.

Return values

<i>kStatus_NoTransferInProgress</i>	No send in progress.
<i>kStatus_InvalidArgument</i>	Parameter is invalid.
<i>kStatus_Success</i>	Get successfully through the parameter <i>count</i> ;

52.5.7 status_t LPUART_TransferGetReceiveCountEDMA (LPUART_Type * *base*, lpuart_edma_handle_t * *handle*, uint32_t * *count*)

This function gets the number of received bytes.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>handle</i>	LPUART handle pointer.
<i>count</i>	Receive bytes count.

Return values

<i>kStatus_NoTransferInProgress</i>	No receive in progress.
<i>kStatus_InvalidArgument</i>	Parameter is invalid.
<i>kStatus_Success</i>	Get successfully through the parameter count;

52.5.8 void LPUART_TransferEdmaHandleIRQ (LPUART_Type * *base*, void * *lpuartEdmaHandle*)

This function handles the LPUART tx complete IRQ request and invoke user callback. It is not set to static so that it can be used in user application.

Note

This function is used as default IRQ handler by double weak mechanism. If user's specific IRQ handler is implemented, make sure this function is invoked in the handler.

Parameters

<i>base</i>	LPUART peripheral base address.
<i>lpuartEdmaHandle</i>	LPUART handle pointer.

Chapter 53

Lpuart_freertos_driver

53.1 Overview

Data Structures

- struct [lpuart_rtos_config_t](#)
LPUART RTOS configuration structure. [More...](#)

Driver version

- #define [FSL_LPUART_FREERTOS_DRIVER_VERSION](#) (MAKE_VERSION(2, 6, 0))
LPUART FreeRTOS driver version.

LPUART RTOS Operation

- int [LPUART_RTOS_Init](#) (lpuart_rtos_handle_t *handle, lpuart_handle_t *t_handle, const [lpuart_rtos_config_t](#) *cfg)
Initializes an LPUART instance for operation in RTOS.
- int [LPUART_RTOS_Deinit](#) (lpuart_rtos_handle_t *handle)
Deinitializes an LPUART instance for operation.

LPUART transactional Operation

- int [LPUART_RTOS_Send](#) (lpuart_rtos_handle_t *handle, uint8_t *buffer, uint32_t length)
Sends data in the background.
- int [LPUART_RTOS_Receive](#) (lpuart_rtos_handle_t *handle, uint8_t *buffer, uint32_t length, size_t *received)
Receives data.
- int [LPUART_RTOS_SetRxTimeout](#) (lpuart_rtos_handle_t *handle, uint32_t rx_timeout_constant_ms, uint32_t rx_timeout_multiplier_ms)
Set RX timeout in runtime.
- int [LPUART_RTOS_SetTxTimeout](#) (lpuart_rtos_handle_t *handle, uint32_t tx_timeout_constant_ms, uint32_t tx_timeout_multiplier_ms)
Set TX timeout in runtime.

53.2 Data Structure Documentation

53.2.1 struct [lpuart_rtos_config_t](#)

Data Fields

- LPUART_Type * base
UART base address.

- `uint32_t srclk`
UART source clock in Hz.
- `uint32_t baudrate`
Desired communication speed.
- `lpuart_parity_mode_t parity`
Parity setting.
- `lpuart_stop_bit_count_t stopbits`
Number of stop bits to use.
- `uint8_t * buffer`
Buffer for background reception.
- `uint32_t buffer_size`
Size of buffer for background reception.
- `uint32_t rx_timeout_constant_ms`
RX timeout applied per receive.
- `uint32_t rx_timeout_multiplier_ms`
RX timeout added for each byte of the receive.
- `uint32_t tx_timeout_constant_ms`
TX timeout applied per transmission.
- `uint32_t tx_timeout_multiplier_ms`
TX timeout added for each byte of the transmission.
- `bool enableRxRTS`
RX RTS enable.
- `bool enableTxCTS`
TX CTS enable.
- `lpuart_transmit_cts_source_t txCtsSource`
TX CTS source.
- `lpuart_transmit_cts_config_t txCtsConfig`
TX CTS configure.

Field Documentation

- (1) `uint32_t lpuart_rtos_config_t::rx_timeout_multiplier_ms`
- (2) `uint32_t lpuart_rtos_config_t::tx_timeout_multiplier_ms`

53.3 Macro Definition Documentation

`#define FSL_LPUART_FREERTOS_DRIVER_VERSION (MAKE_VERSION(2, 6, 0))`

53.4 Function Documentation

`int LPUART_RTOS_Init (lpuart_rtos_handle_t * handle, lpuart_handle_t * t_handle, const lpuart_rtos_config_t * cfg)`

Parameters

<i>handle</i>	The RTOS LPUART handle, the pointer to an allocated space for RTOS context.
<i>t_handle</i>	The pointer to an allocated space to store the transactional layer internal state.
<i>cfg</i>	The pointer to the parameters required to configure the LPUART after initialization.

Returns

0 succeed, others failed

53.4.2 int LPUART_RTOS_Deinit (*Ipuart_rtos_handle_t * handle*)

This function deinitializes the LPUART module, sets all register value to the reset value, and releases the resources.

Parameters

<i>handle</i>	The RTOS LPUART handle.
---------------	-------------------------

53.4.3 int LPUART_RTOS_Send (*Ipuart_rtos_handle_t * handle, uint8_t * buffer, uint32_t length*)

This function sends data. It is an synchronous API. If the hardware buffer is full, the task is in the blocked state.

Parameters

<i>handle</i>	The RTOS LPUART handle.
<i>buffer</i>	The pointer to buffer to send.
<i>length</i>	The number of bytes to send.

53.4.4 int LPUART_RTOS_Receive (*Ipuart_rtos_handle_t * handle, uint8_t * buffer, uint32_t length, size_t * received*)

This function receives data from LPUART. It is an synchronous API. If any data is immediately available it is returned immediately and the number of bytes received.

Parameters

<i>handle</i>	The RTOS LPUART handle.
<i>buffer</i>	The pointer to buffer where to write received data.
<i>length</i>	The number of bytes to receive.
<i>received</i>	The pointer to a variable of size_t where the number of received data is filled.

53.4.5 int LPUART_RTOS_SetRxTimeout (Ipuart_rtos_handle_t * *handle*, uint32_t *rx_timeout_constant_ms*, uint32_t *rx_timeout_multiplier_ms*)

This function can modify RX timeout between initialization and receive.

param handle The RTOS LPUART handle. param rx_timeout_constant_ms RX timeout applied per receive. param rx_timeout_multiplier_ms RX timeout added for each byte of the receive.

53.4.6 int LPUART_RTOS_SetTxTimeout (Ipuart_rtos_handle_t * *handle*, uint32_t *tx_timeout_constant_ms*, uint32_t *tx_timeout_multiplier_ms*)

This function can modify TX timeout between initialization and send.

param handle The RTOS LPUART handle. param tx_timeout_constant_ms TX timeout applied per transmission. param tx_timeout_multiplier_ms TX timeout added for each byte of the transmission.

Chapter 54

Ltc_edma_driver

54.1 Overview

Data Structures

- struct [ltc_edma_handle_t](#)
LTC eDMA handle. [More...](#)

Typedefs

- typedef void(* [ltc_edma_callback_t](#))(LTC_Type *base, ltc_edma_handle_t *handle, [status_t](#) status, void *userData)
LTC eDMA callback function.
- typedef [status_t](#)(* [ltc_edma_state_machine_t](#))(LTC_Type *base, ltc_edma_handle_t *handle)
LTC eDMA state machine function.

Functions

- void [LTC_CreateHandleEDMA](#) (LTC_Type *base, ltc_edma_handle_t *handle, [ltc_edma_callback_t](#) callback, void *userData, [edma_handle_t](#) *inputFifoEdmaHandle, [edma_handle_t](#) *outputFifoEdmaHandle)
Init the LTC eDMA handle which is used in transactional functions.

Driver version

- #define [FSL_LTC_EDMA_DRIVER_VERSION](#) ([MAKE_VERSION](#)(2, 0, 15))
LTC EDMA driver version.

54.2 Data Structure Documentation

54.2.1 struct _ltc_edma_handle

It is defined only for private usage inside LTC eDMA driver.

Data Fields

- [ltc_edma_callback_t](#) [callback](#)
Callback function.
- void * [userData](#)
LTC callback function parameter.
- [edma_handle_t](#) * [inputFifoEdmaHandle](#)
The eDMA TX channel used.

- **edma_handle_t * outputFifoEdmaHandle**
The eDMA RX channel used.
- **ltc_edma_state_machine_t state_machine**
State machine.
- **uint32_t state**
Internal state.
- **const uint8_t * inData**
Input data.
- **uint8_t * outData**
Output data.
- **uint32_t size**
Size of input and output data in bytes.
- **uint32_t modeReg**
LTC mode register.
- **uint8_t * counter**
Input counter (updates on return)
- **const uint8_t * key**
Input key to use for forward AES cipher.
- **uint32_t keySize**
Size of the input key, in bytes.
- **uint8_t * counterlast**
Output cipher of last counter, for chained CTR calls.
- **uint32_t * szLeft**
Output number of bytes in left unused in counterlast block.
- **uint32_t lastSize**
Last size.

Field Documentation

- (1) **ltc_edma_callback_t ltc_edma_handle_t::callback**
- (2) **void* ltc_edma_handle_t::userData**
- (3) **edma_handle_t* ltc_edma_handle_t::inputFifoEdmaHandle**
- (4) **edma_handle_t* ltc_edma_handle_t::outputFifoEdmaHandle**
- (5) **ltc_edma_state_machine_t ltc_edma_handle_t::state_machine**
- (6) **uint32_t ltc_edma_handle_t::state**
- (7) **const uint8_t* ltc_edma_handle_t::inData**
- (8) **uint8_t* ltc_edma_handle_t::outData**
- (9) **uint32_t ltc_edma_handle_t::size**
- (10) **uint32_t ltc_edma_handle_t::modeReg**

(11) `uint32_t ltc_edma_handle_t::keySize`

Must be 16, 24, or 32.

(12) `uint8_t* ltc_edma_handle_t::counterlast`

NULL can be passed if chained calls are not used.

(13) `uint32_t* ltc_edma_handle_t::szLeft`

NULL can be passed if chained calls are not used.

(14) `uint32_t ltc_edma_handle_t::lastSize`

54.3 Macro Definition Documentation

54.3.1 #define FSL_LTC_EDMA_DRIVER_VERSION (MAKE_VERSION(2, 0, 15))

Version 2.0.15.

54.4 Typedef Documentation

54.4.1 typedef void(* ltc_edma_callback_t)(LTC_Type *base, ltc_edma_handle_t *handle, status_t status, void *userData)

54.4.2 typedef status_t(* ltc_edma_state_machine_t)(LTC_Type *base, ltc_edma_handle_t *handle)

It is defined only for private usage inside LTC eDMA driver.

54.5 Function Documentation

54.5.1 void LTC_CreateHandleEDMA (LTC_Type * *base*, ltc_edma_handle_t * *handle*, ltc_edma_callback_t *callback*, void * *userData*, edma_handle_t * *inputFifoEdmaHandle*, edma_handle_t * *outputFifoEdmaHandle*)

Parameters

<i>base</i>	LTC module base address
<i>handle</i>	Pointer to ltc_edma_handle_t structure

<i>callback</i>	Callback function, NULL means no callback.
<i>userData</i>	Callback function parameter.
<i>inputFifo- EdmaHandle</i>	User requested eDMA handle for Input FIFO eDMA.
<i>outputFifo- EdmaHandle</i>	User requested eDMA handle for Output FIFO eDMA.

Chapter 55

Ltc_edma_driver_aes

55.1 Overview

Macros

- #define `LTC_AES_DecryptCtrEDMA`(base, handle, input, output, size, counter, key, keySize, counterlast, szLeft) `LTC_AES_CryptCtrEDMA`(base, handle, input, output, size, counter, key, keySize, counterlast, szLeft)
AES CTR decrypt is mapped to the AES CTR generic operation.
- #define `LTC_AES_EncryptCtrEDMA`(base, handle, input, output, size, counter, key, keySize, counterlast, szLeft) `LTC_AES_CryptCtrEDMA`(base, handle, input, output, size, counter, key, keySize, counterlast, szLeft)
AES CTR encrypt is mapped to the AES CTR generic operation.

Functions

- `status_t LTC_AES_EncryptEcbEDMA` (`LTC_Type *base`, `ltc_edma_handle_t *handle`, `const uint8_t *plaintext`, `uint8_t *ciphertext`, `uint32_t size`, `const uint8_t *key`, `uint32_t keySize`)
Encrypts AES using the ECB block mode.
- `status_t LTC_AES_DecryptEcbEDMA` (`LTC_Type *base`, `ltc_edma_handle_t *handle`, `const uint8_t *ciphertext`, `uint8_t *plaintext`, `uint32_t size`, `const uint8_t *key`, `uint32_t keySize`, `ltc_aes_key_t keyType`)
Decrypts AES using ECB block mode.
- `status_t LTC_AES_EncryptCbcEDMA` (`LTC_Type *base`, `ltc_edma_handle_t *handle`, `const uint8_t *plaintext`, `uint8_t *ciphertext`, `uint32_t size`, `const uint8_t iv[LTC_AES_IV_SIZE]`, `const uint8_t *key`, `uint32_t keySize`)
Encrypts AES using CBC block mode.
- `status_t LTC_AES_DecryptCbcEDMA` (`LTC_Type *base`, `ltc_edma_handle_t *handle`, `const uint8_t *ciphertext`, `uint8_t *plaintext`, `uint32_t size`, `const uint8_t iv[LTC_AES_IV_SIZE]`, `const uint8_t *key`, `uint32_t keySize`, `ltc_aes_key_t keyType`)
Decrypts AES using CBC block mode.
- `status_t LTC_AES_CryptCtrEDMA` (`LTC_Type *base`, `ltc_edma_handle_t *handle`, `const uint8_t *input`, `uint8_t *output`, `uint32_t size`, `uint8_t counter[LTC_AES_BLOCK_SIZE]`, `const uint8_t *key`, `uint32_t keySize`, `uint8_t counterlast[LTC_AES_BLOCK_SIZE]`, `uint32_t *szLeft`)
Encrypts or decrypts AES using CTR block mode.

55.2 Function Documentation

55.2.1 `status_t LTC_AES_EncryptEcbEDMA (LTC_Type * base, ltc_edma_handle_t * handle, const uint8_t * plaintext, uint8_t * ciphertext, uint32_t size, const uint8_t * key, uint32_t keySize)`

Encrypts AES using the ECB block mode.

Parameters

	<i>base</i>	LTC peripheral base address
	<i>handle</i>	pointer to <code>ltc_edma_handle_t</code> structure which stores the transaction state.
	<i>plaintext</i>	Input plain text to encrypt
out	<i>ciphertext</i>	Output cipher text
	<i>size</i>	Size of input and output data in bytes. Must be multiple of 16 bytes.
	<i>key</i>	Input key to use for encryption
	<i>keySize</i>	Size of the input key, in bytes. Must be 16, 24, or 32.

Returns

Status from encrypt operation

55.2.2 `status_t LTC_AES_DecryptEcbEDMA (LTC_Type * base, ltc_edma_handle_t * handle, const uint8_t * ciphertext, uint8_t * plaintext, uint32_t size, const uint8_t * key, uint32_t keySize, ltc_aes_key_t keyType)`

Decrypts AES using ECB block mode.

Parameters

	<i>base</i>	LTC peripheral base address
	<i>handle</i>	pointer to <code>ltc_edma_handle_t</code> structure which stores the transaction state.
	<i>ciphertext</i>	Input cipher text to decrypt
out	<i>plaintext</i>	Output plain text
	<i>size</i>	Size of input and output data in bytes. Must be multiple of 16 bytes.
	<i>key</i>	Input key.
	<i>keySize</i>	Size of the input key, in bytes. Must be 16, 24, or 32.
	<i>keyType</i>	Input type of the key (allows to directly load decrypt key for AES ECB decrypt operation.)

Returns

Status from decrypt operation

55.2.3 `status_t LTC_AES_EncryptCbcEDMA(LTC_Type * base, ltc_edma_handle_t * handle, const uint8_t * plaintext, uint8_t * ciphertext, uint32_t size, const uint8_t iv[LTC_AES_IV_SIZE], const uint8_t * key, uint32_t keySize)`

Parameters

	<i>base</i>	LTC peripheral base address
	<i>handle</i>	pointer to ltc_edma_handle_t structure which stores the transaction state.
	<i>plaintext</i>	Input plain text to encrypt
out	<i>ciphertext</i>	Output cipher text
	<i>size</i>	Size of input and output data in bytes. Must be multiple of 16 bytes.
	<i>iv</i>	Input initial vector to combine with the first input block.
	<i>key</i>	Input key to use for encryption
	<i>keySize</i>	Size of the input key, in bytes. Must be 16, 24, or 32.

Returns

Status from encrypt operation

**55.2.4 status_t LTC_AES_DecryptCbcEDMA (LTC_Type * *base*,
ltc_edma_handle_t * *handle*, const uint8_t * *ciphertext*, uint8_t * *plaintext*,
 uint32_t *size*, const uint8_t *iv*[LTC_AES_IV_SIZE], const uint8_t * *key*,
 uint32_t *keySize*, *ltc_aes_key_t* *keyType*)**

Parameters

	<i>base</i>	LTC peripheral base address
	<i>handle</i>	pointer to ltc_edma_handle_t structure which stores the transaction state.
	<i>ciphertext</i>	Input cipher text to decrypt
out	<i>plaintext</i>	Output plain text
	<i>size</i>	Size of input and output data in bytes. Must be multiple of 16 bytes.
	<i>iv</i>	Input initial vector to combine with the first input block.
	<i>key</i>	Input key to use for decryption

	<i>keySize</i>	Size of the input key, in bytes. Must be 16, 24, or 32.
	<i>keyType</i>	Input type of the key (allows to directly load decrypt key for AES CBC decrypt operation.)

Returns

Status from decrypt operation

55.2.5 status_t LTC_AES_CryptCtrEDMA (LTC_Type * *base*, ltc_edma_handle_t * *handle*, const uint8_t * *input*, uint8_t * *output*, uint32_t *size*, uint8_t *counter*[LTC_AES_BLOCK_SIZE], const uint8_t * *key*, uint32_t *keySize*, uint8_t *counterlast*[LTC_AES_BLOCK_SIZE], uint32_t * *szLeft*)

Encrypts or decrypts AES using CTR block mode. AES CTR mode uses only forward AES cipher and same algorithm for encryption and decryption. The only difference between encryption and decryption is that, for encryption, the input argument is plain text and the output argument is cipher text. For decryption, the input argument is cipher text and the output argument is plain text.

Parameters

	<i>base</i>	LTC peripheral base address
	<i>handle</i>	pointer to ltc_edma_handle_t structure which stores the transaction state.
	<i>input</i>	Input data for CTR block mode
out	<i>output</i>	Output data for CTR block mode
	<i>size</i>	Size of input and output data in bytes
in,out	<i>counter</i>	Input counter (updates on return)
	<i>key</i>	Input key to use for forward AES cipher
	<i>keySize</i>	Size of the input key, in bytes. Must be 16, 24, or 32.
out	<i>counterlast</i>	Output cipher of last counter, for chained CTR calls. NULL can be passed if chained calls are not used.

out	<i>szLeft</i>	Output number of bytes in left unused in counterlast block. NULL can be passed if chained calls are not used.
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Returns

Status from encrypt operation

Chapter 56

Qspi_edma_driver

56.1 Overview

Data Structures

- struct `qspi_edma_handle_t`
QSPI DMA transfer handle, users should not touch the content of the handle. [More...](#)

Typedefs

- typedef void(* `qspi_edma_callback_t`)(QuadSPI_Type *base, qspi_edma_handle_t *handle, `status_t` status, void *userData)
QSPI eDMA transfer callback function for finish and error.

Driver version

- #define `FSL_QSPI_EDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 2, 2)`)
QSPI EDMA driver version 2.2.2.

eDMA Transactional

- void `QSPI_TransferTxCreateHandleEDMA` (QuadSPI_Type *base, qspi_edma_handle_t *handle, `qspi_edma_callback_t` callback, void *userData, `edma_handle_t` *dmaHandle)
Initializes the QSPI handle for send which is used in transactional functions and set the callback.
- void `QSPI_TransferRxCreateHandleEDMA` (QuadSPI_Type *base, qspi_edma_handle_t *handle, `qspi_edma_callback_t` callback, void *userData, `edma_handle_t` *dmaHandle)
Initializes the QSPI handle for receive which is used in transactional functions and set the callback.
- `status_t QSPI_TransferSendEDMA` (QuadSPI_Type *base, qspi_edma_handle_t *handle, `qspi_transfer_t` *xfer)
Transfers QSPI data using an eDMA non-blocking method.
- `status_t QSPI_TransferReceiveEDMA` (QuadSPI_Type *base, qspi_edma_handle_t *handle, `qspi_transfer_t` *xfer)
Receives data using an eDMA non-blocking method.
- void `QSPI_TransferAbortSendEDMA` (QuadSPI_Type *base, qspi_edma_handle_t *handle)
Aborts the sent data using eDMA.
- void `QSPI_TransferAbortReceiveEDMA` (QuadSPI_Type *base, qspi_edma_handle_t *handle)
Aborts the receive data using eDMA.
- `status_t QSPI_TransferGetSendCountEDMA` (QuadSPI_Type *base, qspi_edma_handle_t *handle, `size_t` *count)
Gets the transferred counts of send.
- `status_t QSPI_TransferGetReceiveCountEDMA` (QuadSPI_Type *base, qspi_edma_handle_t *handle, `size_t` *count)
Gets the status of the receive transfer.

56.2 Data Structure Documentation

56.2.1 struct _qspi_edma_handle

Data Fields

- `edma_handle_t * dmaHandle`
eDMA handler for QSPI send.
- `size_t transferSize`
Bytes need to transfer.
- `uint8_t nbytes`
eDMA minor byte transfer count initially configured.
- `uint8_t count`
The transfer data count in a DMA request.
- `uint32_t state`
Internal state for QSPI eDMA transfer.
- `qspi_edma_callback_t callback`
Callback for users while transfer finish or error occurred.
- `void * userData`
User callback parameter.

Field Documentation

- (1) `size_t qspi_edma_handle_t::transferSize`
- (2) `uint8_t qspi_edma_handle_t::nbytes`

56.3 Macro Definition Documentation

56.3.1 #define FSL_QSPI_EDMA_DRIVER_VERSION (MAKE_VERSION(2, 2, 2))

56.4 Function Documentation

56.4.1 void QSPI_TransferTxCreateHandleEDMA (`QuadSPI_Type * base,` `qspi_edma_handle_t * handle, qspi_edma_callback_t callback, void *` `userData, edma_handle_t * dmaHandle`)

Parameters

<code>base</code>	QSPI peripheral base address
<code>handle</code>	Pointer to <code>qspi_edma_handle_t</code> structure

<i>callback</i>	QSPI callback, NULL means no callback.
<i>userData</i>	User callback function data.
<i>dmaHandle</i>	User requested eDMA handle for eDMA transfer

56.4.2 void QSPI_TransferRxCreateHandleEDMA (QuadSPI_Type * *base*, qspi_edma_handle_t * *handle*, qspi_edma_callback_t *callback*, void * *userData*, edma_handle_t * *dmaHandle*)

Parameters

<i>base</i>	QSPI peripheral base address
<i>handle</i>	Pointer to qspi_edma_handle_t structure
<i>callback</i>	QSPI callback, NULL means no callback.
<i>userData</i>	User callback function data.
<i>dmaHandle</i>	User requested eDMA handle for eDMA transfer

56.4.3 status_t QSPI_TransferSendEDMA (QuadSPI_Type * *base*, qspi_edma_handle_t * *handle*, qspi_transfer_t * *xfer*)

This function writes data to the QSPI transmit FIFO. This function is non-blocking.

Parameters

<i>base</i>	Pointer to QuadSPI Type.
<i>handle</i>	Pointer to qspi_edma_handle_t structure
<i>xfer</i>	QSPI transfer structure.

56.4.4 status_t QSPI_TransferReceiveEDMA (QuadSPI_Type * *base*, qspi_edma_handle_t * *handle*, qspi_transfer_t * *xfer*)

This function receive data from the QSPI receive buffer/FIFO. This function is non-blocking. Users shall notice that this receive size shall not bigger than 64 bytes. As this interface is used to read flash status registers. For flash contents read, please use AHB bus read, this is much more efficiency.

Parameters

<i>base</i>	Pointer to QuadSPI Type.
<i>handle</i>	Pointer to qspi_edma_handle_t structure
<i>xfer</i>	QSPI transfer structure.

56.4.5 void QSPI_TransferAbortSendEDMA (QuadSPI_Type * *base*, qspi_edma_handle_t * *handle*)

This function aborts the sent data using eDMA.

Parameters

<i>base</i>	QSPI peripheral base address.
<i>handle</i>	Pointer to qspi_edma_handle_t structure

56.4.6 void QSPI_TransferAbortReceiveEDMA (QuadSPI_Type * *base*, qspi_edma_handle_t * *handle*)

This function abort receive data which using eDMA.

Parameters

<i>base</i>	QSPI peripheral base address.
<i>handle</i>	Pointer to qspi_edma_handle_t structure

56.4.7 status_t QSPI_TransferGetSendCountEDMA (QuadSPI_Type * *base*, qspi_edma_handle_t * *handle*, size_t * *count*)

Parameters

<i>base</i>	Pointer to QuadSPI Type.
<i>handle</i>	Pointer to qspi_edma_handle_t structure.

<i>count</i>	Bytes sent.
--------------	-------------

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferInProgress</i>	There is not a non-blocking transaction currently in progress.

56.4.8 **status_t QSPI_TransferGetReceiveCountEDMA (QuadSPI_Type * *base*, qspi_edma_handle_t * *handle*, size_t * *count*)**

Parameters

<i>base</i>	Pointer to QuadSPI Type.
<i>handle</i>	Pointer to qspi_edma_handle_t structure
<i>count</i>	Bytes received.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferInProgress</i>	There is not a non-blocking transaction currently in progress.

56.5 SAI EDMA Driver

56.5.1 Overview

Data Structures

- struct `sai_edma_handle_t`
SAI DMA transfer handle, users should not touch the content of the handle. [More...](#)

Typedefs

- typedef void(* `sai_edma_callback_t`)(I2S_Type *base, sai_edma_handle_t *handle, `status_t` status, void *userData)
SAI eDMA transfer callback function for finish and error.

Driver version

- #define `FSL_SAI_EDMA_DRIVER_VERSION` (`MAKE_VERSION(2, 5, 0)`)
Version 2.5.0.

eDMA Transactional

- void `SAI_TransferTxCreateHandleEDMA` (I2S_Type *base, sai_edma_handle_t *handle, `sai_edma_callback_t` callback, void *userData, `edma_handle_t` *txDmaHandle)
Initializes the SAI eDMA handle.
- void `SAI_TransferRxCreateHandleEDMA` (I2S_Type *base, sai_edma_handle_t *handle, `sai_edma_callback_t` callback, void *userData, `edma_handle_t` *rxDmaHandle)
Initializes the SAI Rx eDMA handle.
- void `SAI_TransferTxSetFormatEDMA` (I2S_Type *base, sai_edma_handle_t *handle, `sai_transfer_format_t` *format, uint32_t mclkSourceClockHz, uint32_t bclkSourceClockHz)
Configures the SAI Tx audio format.
- void `SAI_TransferRxSetFormatEDMA` (I2S_Type *base, sai_edma_handle_t *handle, `sai_transfer_format_t` *format, uint32_t mclkSourceClockHz, uint32_t bclkSourceClockHz)
Configures the SAI Rx audio format.
- void `SAI_TransferTxSetConfigEDMA` (I2S_Type *base, sai_edma_handle_t *handle, `sai_transceiver_t` *saiConfig)
Configures the SAI Tx.
- void `SAI_TransferRxSetConfigEDMA` (I2S_Type *base, sai_edma_handle_t *handle, `sai_transceiver_t` *saiConfig)
Configures the SAI Rx.
- `status_t SAI_TransferSendEDMA` (I2S_Type *base, sai_edma_handle_t *handle, `sai_transfer_t` *xfer)
Performs a non-blocking SAI transfer using DMA.
- `status_t SAI_TransferReceiveEDMA` (I2S_Type *base, sai_edma_handle_t *handle, `sai_transfer_t` *xfer)

- *Performs a non-blocking SAI receive using eDMA.*
- **status_t SAI_TransferSendLoopEDMA** (I2S_Type *base, sai_edma_handle_t *handle, sai_transfer_t *xfer, uint32_t loopTransferCount)
 - Performs a non-blocking SAI loop transfer using eDMA.*
- **status_t SAI_TransferReceiveLoopEDMA** (I2S_Type *base, sai_edma_handle_t *handle, sai_transfer_t *xfer, uint32_t loopTransferCount)
 - Performs a non-blocking SAI loop transfer using eDMA.*
- **void SAI_TransferTerminateSendEDMA** (I2S_Type *base, sai_edma_handle_t *handle)
 - Terminate all SAI send.*
- **void SAI_TransferTerminateReceiveEDMA** (I2S_Type *base, sai_edma_handle_t *handle)
 - Terminate all SAI receive.*
- **void SAI_TransferAbortSendEDMA** (I2S_Type *base, sai_edma_handle_t *handle)
 - Aborts a SAI transfer using eDMA.*
- **void SAI_TransferAbortReceiveEDMA** (I2S_Type *base, sai_edma_handle_t *handle)
 - Aborts a SAI receive using eDMA.*
- **status_t SAI_TransferGetSendCountEDMA** (I2S_Type *base, sai_edma_handle_t *handle, size_t *count)
 - Gets byte count sent by SAI.*
- **status_t SAI_TransferGetReceiveCountEDMA** (I2S_Type *base, sai_edma_handle_t *handle, size_t *count)
 - Gets byte count received by SAI.*
- **uint32_t SAI_TransferGetValidTransferSlotsEDMA** (I2S_Type *base, sai_edma_handle_t *handle)
 - Gets valid transfer slot.*

56.5.2 Data Structure Documentation

56.5.2.1 struct sai_edma_handle

Data Fields

- **edma_handle_t * dmaHandle**
 - DMA handler for SAI send.*
- **uint8_t nbytes**
 - eDMA minor byte transfer count initially configured.*
- **uint8_t bytesPerFrame**
 - Bytes in a frame.*
- **uint8_t channelMask**
 - Enabled channel mask value, reference _sai_channel_mask.*
- **uint8_t channelNums**
 - total enabled channel nums*
- **uint8_t channel**
 - Which data channel.*
- **uint8_t count**
 - The transfer data count in a DMA request.*
- **uint32_t state**
 - Internal state for SAI eDMA transfer.*
- **sai_edma_callback_t callback**
 - Callback for users while transfer finish or error occurs.*
- **void * userData**

- *User callback parameter.*
- `uint8_t tcd [(SAI_XFER_QUEUE_SIZE+1U)*sizeof(edma_tcd_t)]`
TCD pool for eDMA transfer.
- `sai_transfer_t saiQueue [SAI_XFER_QUEUE_SIZE]`
Transfer queue storing queued transfer.
- `size_t transferSize [SAI_XFER_QUEUE_SIZE]`
Data bytes need to transfer.
- `volatile uint8_t queueUser`
Index for user to queue transfer.
- `volatile uint8_t queueDriver`
Index for driver to get the transfer data and size.

Field Documentation

- (1) `uint8_t sai_edma_handle_t::nbytes`
- (2) `uint8_t sai_edma_handle_t::tcd[(SAI_XFER_QUEUE_SIZE+1U)*sizeof(edma_tcd_t)]`
- (3) `sai_transfer_t sai_edma_handle_t::saiQueue[SAI_XFER_QUEUE_SIZE]`
- (4) `volatile uint8_t sai_edma_handle_t::queueUser`

56.5.3 Function Documentation

56.5.3.1 void SAI_TransferTxCreateHandleEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*, sai_edma_callback_t *callback*, void * *userData*, edma_handle_t * *txDmaHandle*)

This function initializes the SAI master DMA handle, which can be used for other SAI master transactional APIs. Usually, for a specified SAI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>base</i>	SAI peripheral base address.
<i>callback</i>	Pointer to user callback function.
<i>userData</i>	User parameter passed to the callback function.
<i>txDmaHandle</i>	eDMA handle pointer, this handle shall be static allocated by users.

56.5.3.2 void SAI_TransferRxCreateHandleEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*, sai_edma_callback_t *callback*, void * *userData*, edma_handle_t * *rxDmaHandle*)

This function initializes the SAI slave DMA handle, which can be used for other SAI master transactional APIs. Usually, for a specified SAI instance, call this API once to get the initialized handle.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>base</i>	SAI peripheral base address.
<i>callback</i>	Pointer to user callback function.
<i>userData</i>	User parameter passed to the callback function.
<i>rxDmaHandle</i>	eDMA handle pointer, this handle shall be static allocated by users.

56.5.3.3 void SAI_TransferTxSetFormatEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*, sai_transfer_format_t * *format*, uint32_t *mclkSourceClockHz*, uint32_t *bclkSourceClockHz*)

Deprecated Do not use this function. It has been superceded by [SAI_TransferTxSetConfigEDMA](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred. This function also sets the eDMA parameter according to formatting requirements.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>format</i>	Pointer to SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If bit clock source is master clock, this value should equals to masterClockHz in format.

Return values

<i>kStatus_Success</i>	Audio format set successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.

56.5.3.4 void SAI_TransferRxSetFormatEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*, sai_transfer_format_t * *format*, uint32_t *mclkSourceClockHz*, uint32_t *bclkSourceClockHz*)

Deprecated Do not use this function. It has been superceded by [SAI_TransferRxSetConfigEDMA](#)

The audio format can be changed at run-time. This function configures the sample rate and audio data format to be transferred. This function also sets the eDMA parameter according to formatting requirements.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>format</i>	Pointer to SAI audio data format structure.
<i>mclkSource-ClockHz</i>	SAI master clock source frequency in Hz.
<i>bclkSource-ClockHz</i>	SAI bit clock source frequency in Hz. If a bit clock source is the master clock, this value should equal to <i>masterClockHz</i> in format.

Return values

<i>kStatus_Success</i>	Audio format set successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.

56.5.3.5 void SAI_TransferTxSetConfigEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*, sai_transceiver_t * *saiConfig*)

Note

SAI eDMA supports data transfer in multiple SAI channels if the FIFO Combine feature is supported. To activate the multi-channel transfer enable SAI channels by filling the channelMask of *sai_transceiver_t* with the corresponding values of *_sai_channel_mask* enum, enable the FIFO Combine mode by assigning *kSAI_FifoCombineModeEnabledOnWrite* to the *fifoCombine* member of *sai_fifo_combine_t* which is a member of *sai_transceiver_t*. This is an example of multi-channel data transfer configuration step.

```
*   sai_transceiver_t config;
*   SAI_GetClassicI2SConfig(&config, kSAI_WordWidth16bits,
*                           kSAI_Stereo, kSAI_Channel0Mask|kSAI_Channel1Mask);
*   config fifo fifoCombine = kSAI_FifoCombineModeEnabledOnWrite
*   ;
*   SAI_TransferTxSetConfigEDMA(I2S0, &edmaHandle, &config);
*
```

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>saiConfig</i>	sai configurations.

56.5.3.6 void SAI_TransferRxSetConfigEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*, sai_transceiver_t * *saiConfig*)

Note

SAI eDMA supports data transfer in a multiple SAI channels if the FIFO Combine feature is supported. To activate the multi-channel transfer enable SAI channels by filling the channelMask of *sai_transceiver_t* with the corresponding values of _sai_channel_mask enum, enable the FIFO Combine mode by assigning kSAI_FifoCombineModeEnabledOnRead to the fifoCombine member of *sai_fifo_combine_t* which is a member of *sai_transceiver_t*. This is an example of multi-channel data transfer configuration step.

```
*     sai_transceiver_t config;
*     SAI_GetClassicI2SConfig(&config, kSAI_WordWidth16bits,
*                             kSAI_Stereo, kSAI_Channel0Mask|kSAI_Channel1Mask);
*     config fifo.fifoCombine = kSAI_FifoCombineModeEnabledOnRead
*     ;
*     SAI_TransferRxSetConfigEDMA(I2S0, &edmaHandle, &config);
*
```

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>saiConfig</i>	sai configurations.

56.5.3.7 status_t SAI_TransferSendEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*, sai_transfer_t * *xfer*)

Note

This interface returns immediately after the transfer initiates. Call SAI_GetTransferStatus to poll the transfer status and check whether the SAI transfer is finished.

This function support multi channel transfer,

1. for the sai IP support fifo combine mode, application should enable the fifo combine mode, no limitation on channel numbers
2. for the sai IP not support fifo combine mode, sai edma provide another solution which using EDMA modulo feature, but support 2 or 4 channels only.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>xfer</i>	Pointer to the DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a SAI eDMA send successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.
<i>kStatus_TxBusy</i>	SAI is busy sending data.

56.5.3.8 status_t SAI_TransferReceiveEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*, sai_transfer_t * *xfer*)

Note

This interface returns immediately after the transfer initiates. Call the SAI_GetReceiveRemainingBytes to poll the transfer status and check whether the SAI transfer is finished.

This function support multi channel transfer,

1. for the sai IP support fifo combine mode, application should enable the fifo combine mode, no limitation on channel numbers
2. for the sai IP not support fifo combine mode, sai edma provide another solution which using EDMA modulo feature, but support 2 or 4 channels only.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI eDMA handle pointer.
<i>xfer</i>	Pointer to DMA transfer structure.

Return values

<i>kStatus_Success</i>	Start a SAI eDMA receive successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.

<i>kStatus_RxBusy</i>	SAI is busy receiving data.
-----------------------	-----------------------------

56.5.3.9 status_t SAI_TransferSendLoopEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*, sai_transfer_t * *xfer*, uint32_t *loopTransferCount*)

Note

This function support loop transfer only,such as A->B->...->A, application must be aware of that the more counts of the loop transfer, then more tcd memory required, as the function use the tcd pool in sai_edma_handle_t, so application could redefine the SAI_XFER_QUEUE_SIZE to determine the proper TCD pool size.

Once the loop transfer start, application can use function SAI_TransferAbortSendEDMA to stop the loop transfer.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>xfer</i>	Pointer to the DMA transfer structure, should be a array with elements counts ≥ 1 (loopTransferCount).
<i>loopTransfer-Count</i>	the counts of xfer array.

Return values

<i>kStatus_Success</i>	Start a SAI eDMA send successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.

56.5.3.10 status_t SAI_TransferReceiveLoopEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*, sai_transfer_t * *xfer*, uint32_t *loopTransferCount*)

Note

This function support loop transfer only,such as A->B->...->A, application must be aware of that the more counts of the loop transfer, then more tcd memory required, as the function use the tcd pool in sai_edma_handle_t, so application could redefine the SAI_XFER_QUEUE_SIZE to determine the proper TCD pool size.

Once the loop transfer start, application can use function SAI_TransferAbortReceiveEDMA to stop the loop transfer.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>xfer</i>	Pointer to the DMA transfer structure, should be a array with elements counts ≥ 1 (loopTransferCount).
<i>loopTransfer-Count</i>	the counts of xfer array.

Return values

<i>kStatus_Success</i>	Start a SAI eDMA receive successfully.
<i>kStatus_InvalidArgument</i>	The input argument is invalid.

56.5.3.11 void SAI_TransferTerminateSendEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*)

This function will clear all transfer slots buffered in the sai queue. If users only want to abort the current transfer slot, please call SAI_TransferAbortSendEDMA.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

56.5.3.12 void SAI_TransferTerminateReceiveEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*)

This function will clear all transfer slots buffered in the sai queue. If users only want to abort the current transfer slot, please call SAI_TransferAbortReceiveEDMA.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

56.5.3.13 void SAI_TransferAbortSendEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*)

This function only aborts the current transfer slots, the other transfer slots' information still kept in the handler. If users want to terminate all transfer slots, just call SAI_TransferTerminateSendEDMA.

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.

56.5.3.14 void SAI_TransferAbortReceiveEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*)

This function only aborts the current transfer slots, the other transfer slots' information still kept in the handler. If users want to terminate all transfer slots, just call SAI_TransferTerminateReceiveEDMA.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI eDMA handle pointer.

56.5.3.15 status_t SAI_TransferGetSendCountEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*, size_t * *count*)

Parameters

<i>base</i>	SAI base pointer.
<i>handle</i>	SAI eDMA handle pointer.
<i>count</i>	Bytes count sent by SAI.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is no non-blocking transaction in progress.

56.5.3.16 status_t SAI_TransferGetReceiveCountEDMA (I2S_Type * *base*, sai_edma_handle_t * *handle*, size_t * *count*)

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI eDMA handle pointer.
<i>count</i>	Bytes count received by SAI.

Return values

<i>kStatus_Success</i>	Succeed get the transfer count.
<i>kStatus_NoTransferIn-Progress</i>	There is no non-blocking transaction in progress.

56.5.3.17 `uint32_t SAI_TransferGetValidTransferSlotsEDMA (I2S_Type * base, sai_edma_handle_t * handle)`

This function can be used to query the valid transfer request slot that the application can submit. It should be called in the critical section, that means the application could call it in the corresponding callback function or disable IRQ before calling it in the application, otherwise, the returned value may not correct.

Parameters

<i>base</i>	SAI base pointer
<i>handle</i>	SAI eDMA handle pointer.

Return values

<i>valid</i>	slot count that application submit.
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56.6 Da7212

56.6.1 Overview

Data Structures

- struct `da7212_pll_config_t`
`da7212 pll configuration` *More...*
- struct `da7212_audio_format_t`
`da7212 audio format` *More...*
- struct `da7212_config_t`
`DA7212 configure structure.` *More...*
- struct `da7212_handle_t`
`da7212 codec handler` *More...*

Macros

- `#define DA7212_I2C_HANDLER_SIZE CODEC_I2C_MASTER_HANDLER_SIZE`
`da7212 handle size`
- `#define DA7212_ADDRESS (0x1A)`
`DA7212 I2C address.`
- `#define DA7212_HEADPHONE_MAX_VOLUME_VALUE 0x3FU`
`da7212 volume setting range`

Enumerations

- enum `da7212_Input_t` {

`kDA7212_Input_AUX` = 0x0,
`kDA7212_Input_MIC1_Dig`,
`kDA7212_Input_MIC1_An`,
`kDA7212_Input_MIC2` }
`DA7212 input source select.`
- enum `_da7212_play_channel` {

`kDA7212_HeadphoneLeft` = 1U,
`kDA7212_HeadphoneRight` = 2U,
`kDA7212_Speaker` = 4U }
`da7212 play channel`
- enum `da7212_Output_t` {

`kDA7212_Output_HP` = 0x0,
`kDA7212_Output_SP` }
`DA7212 output device select.`
- enum `_da7212_module` {

`kDA7212_ModuleADC`,
`kDA7212_ModuleDAC`,
`kDA7212_ModuleHeadphone`,
`kDA7212_ModuleSpeaker` }

- *DA7212 module.*
- enum `da7212_dac_source_t` {

 `kDA7212_DACSourceADC` = 0x0U,

 `kDA7212_DACSourceInputStream` = 0x3U }
- DA7212 functionality.*
- enum `da7212_volume_t` {

 `kDA7212_DACGainMute` = 0x7,

 `kDA7212_DACGainM72DB` = 0x17,

 `kDA7212_DACGainM60DB` = 0x1F,

 `kDA7212_DACGainM54DB` = 0x27,

 `kDA7212_DACGainM48DB` = 0x2F,

 `kDA7212_DACGainM42DB` = 0x37,

 `kDA7212_DACGainM36DB` = 0x3F,

 `kDA7212_DACGainM30DB` = 0x47,

 `kDA7212_DACGainM24DB` = 0x4F,

 `kDA7212_DACGainM18DB` = 0x57,

 `kDA7212_DACGainM12DB` = 0x5F,

 `kDA7212_DACGainM6DB` = 0x67,

 `kDA7212_DACGain0DB` = 0x6F,

 `kDA7212_DACGain6DB` = 0x77,

 `kDA7212_DACGain12DB` = 0x7F }
- DA7212 volume.*
- enum `da7212_protocol_t` {

 `kDA7212_BusI2S` = 0x0,

 `kDA7212_BusLeftJustified`,

 `kDA7212_BusRightJustified`,

 `kDA7212_BusDSPMode` }
- The audio data transfer protocol choice.*
- enum `da7212_sys_clk_source_t` {

 `kDA7212_SysClkSourceMCLK` = 0U,

 `kDA7212_SysClkSourcePLL` = 1U << 14 }
- da7212 system clock source*
- enum `da7212_pll_clk_source_t` { `kDA7212_PLLClkSourceMCLK` = 0U }
- DA7212 pll clock source.*
- enum `da7212_pll_out_clk_t` {

 `kDA7212_PLLOutputClk11289600` = 11289600U,

 `kDA7212_PLLOutputClk12288000` = 12288000U }
- DA7212 output clock frequency.*
- enum `da7212_master_bits_t` {

 `kDA7212_MasterBits32PerFrame` = 0U,

 `kDA7212_MasterBits64PerFrame` = 1U,

 `kDA7212_MasterBits128PerFrame` = 2U,

 `kDA7212_MasterBits256PerFrame` = 3U }
- master mode bits per frame*

Functions

- `status_t DA7212_Init (da7212_handle_t *handle, da7212_config_t *codecConfig)`
DA7212 initialize function.
- `status_t DA7212_ConfigAudioFormat (da7212_handle_t *handle, uint32_t masterClock_Hz, uint32_t sampleRate_Hz, uint32_t dataBits)`
Set DA7212 audio format.
- `status_t DA7212_SetPLLConfig (da7212_handle_t *handle, da7212_pll_config_t *config)`
DA7212 set PLL configuration This function will enable the GPIO1 FLL clock output function, so user can see the generated fll output clock frequency from WM8904 GPIO1.
- `void DA7212_ChangeHPVolume (da7212_handle_t *handle, da7212_volume_t volume)`
Set DA7212 playback volume.
- `void DA7212_Mute (da7212_handle_t *handle, bool isMuted)`
Mute or unmute DA7212.
- `void DA7212_ChangeInput (da7212_handle_t *handle, da7212_Input_t DA7212_Input)`
Set the input data source of DA7212.
- `void DA7212_ChangeOutput (da7212_handle_t *handle, da7212_Output_t DA7212_Output)`
Set the output device of DA7212.
- `status_t DA7212_SetChannelVolume (da7212_handle_t *handle, uint32_t channel, uint32_t volume)`
Set module volume.
- `status_t DA7212_SetChannelMute (da7212_handle_t *handle, uint32_t channel, bool isMute)`
Set module mute.
- `status_t DA7212_SetProtocol (da7212_handle_t *handle, da7212_protocol_t protocol)`
Set protocol for DA7212.
- `status_t DA7212_SetMasterModeBits (da7212_handle_t *handle, uint32_t bitWidth)`
Set master mode bits per frame for DA7212.
- `status_t DA7212_WriteRegister (da7212_handle_t *handle, uint8_t u8Register, uint8_t u8RegisterData)`
Write a register for DA7212.
- `status_t DA7212_ReadRegister (da7212_handle_t *handle, uint8_t u8Register, uint8_t *pu8RegisterData)`
Get a register value of DA7212.
- `status_t DA7212_Deinit (da7212_handle_t *handle)`
Deinit DA7212.

Driver version

- `#define FSL_DA7212_DRIVER_VERSION (MAKE_VERSION(2, 2, 2))`
CLOCK driver version 2.2.2.

56.6.2 Data Structure Documentation

56.6.2.1 struct da7212_pll_config_t

Data Fields

- `da7212_pll_clk_source_t source`
pll reference clock source
- `uint32_t refClock_HZ`
pll reference clock frequency
- `da7212_pll_out_clk_t outputClock_HZ`
pll output clock frequency

56.6.2.2 struct da7212_audio_format_t

Data Fields

- `uint32_t mclk_HZ`
master clock frequency
- `uint32_t sampleRate`
sample rate
- `uint32_t bitWidth`
bit width
- `bool isBclkInvert`
bit clock invertet

56.6.2.3 struct da7212_config_t

Data Fields

- `bool isMaster`
If DA7212 is master, true means master, false means slave.
- `da7212_protocol_t protocol`
Audio bus format, can be I2S, LJ, RJ or DSP mode.
- `da7212_dac_source_t dacSource`
DA7212 data source.
- `da7212_audio_format_t format`
audio format
- `uint8_t slaveAddress`
device address
- `codec_i2c_config_t i2cConfig`
i2c configuration
- `da7212_sys_clk_source_t sysClkSource`
system clock source
- `da7212_pll_config_t * pll`
pll configuration

Field Documentation

(1) `bool da7212_config_t::isMaster`

- (2) da7212_protocol_t da7212_config_t::protocol
- (3) da7212_dac_source_t da7212_config_t::dacSource

56.6.2.4 struct da7212_handle_t

Data Fields

- da7212_config_t * config
da7212 config pointer
- uint8_t i2cHandle [DA7212_I2C_HANDLER_SIZE]
i2c handle

56.6.3 Macro Definition Documentation

56.6.3.1 #define FSL_DA7212_DRIVER_VERSION (MAKE_VERSION(2, 2, 2))

56.6.4 Enumeration Type Documentation

56.6.4.1 enum da7212_Input_t

Enumerator

- kDA7212_Input_AUX* Input from AUX.
- kDA7212_Input_MIC1_Dig* Input from MIC1 Digital.
- kDA7212_Input_MIC1_An* Input from Mic1 Analog.
- kDA7212_Input_MIC2* Input from MIC2.

56.6.4.2 enum _da7212_play_channel

Enumerator

- kDA7212_HeadphoneLeft* headphone left
- kDA7212_HeadphoneRight* headphone right
- kDA7212_Speaker* speaker channel

56.6.4.3 enum da7212_Output_t

Enumerator

- kDA7212_Output_HP* Output to headphone.
- kDA7212_Output_SP* Output to speaker.

56.6.4.4 enum _da7212_module

Enumerator

kDA7212_ModuleADC module ADC
kDA7212_ModuleDAC module DAC
kDA7212_ModuleHeadphone module headphone
kDA7212_ModuleSpeaker module speaker

56.6.4.5 enum da7212_dac_source_t

Enumerator

kDA7212_DACSourceADC DAC source from ADC.
kDA7212_DACSourceInputStream DAC source from.

56.6.4.6 enum da7212_volume_t

Enumerator

kDA7212_DACGainMute Mute DAC.
kDA7212_DACGainM72DB DAC volume -72db.
kDA7212_DACGainM60DB DAC volume -60db.
kDA7212_DACGainM54DB DAC volume -54db.
kDA7212_DACGainM48DB DAC volume -48db.
kDA7212_DACGainM42DB DAC volume -42db.
kDA7212_DACGainM36DB DAC volume -36db.
kDA7212_DACGainM30DB DAC volume -30db.
kDA7212_DACGainM24DB DAC volume -24db.
kDA7212_DACGainM18DB DAC volume -18db.
kDA7212_DACGainM12DB DAC volume -12db.
kDA7212_DACGainM6DB DAC volume -6db.
kDA7212_DACGain0DB DAC volume +0db.
kDA7212_DACGain6DB DAC volume +6db.
kDA7212_DACGain12DB DAC volume +12db.

56.6.4.7 enum da7212_protocol_t

Enumerator

kDA7212_BusI2S I2S Type.
kDA7212_BusLeftJustified Left justified.
kDA7212_BusRightJustified Right Justified.
kDA7212_BusDSPMode DSP mode.

56.6.4.8 enum da7212_sys_clk_source_t

Enumerator

kDA7212_SysClkSourceMCLK da7212 system clock soure from MCLK

kDA7212_SysClkSourcePLL da7212 system clock soure from pLL

56.6.4.9 enum da7212_pll_clk_source_t

Enumerator

kDA7212_PLLClkSourceMCLK DA7212 PLL clock source from MCLK.

56.6.4.10 enum da7212_pll_out_clk_t

Enumerator

kDA7212_PLLOutputClk11289600 output 112896000U

kDA7212_PLLOutputClk12288000 output 12288000U

56.6.4.11 enum da7212_master_bits_t

Enumerator

kDA7212_MasterBits32PerFrame master mode bits32 per frame

kDA7212_MasterBits64PerFrame master mode bits64 per frame

kDA7212_MasterBits128PerFrame master mode bits128 per frame

kDA7212_MasterBits256PerFrame master mode bits256 per frame

56.6.5 Function Documentation

56.6.5.1 status_t DA7212_Init (*da7212_handle_t * handle*, *da7212_config_t * codecConfig*)

Parameters

<i>handle</i>	DA7212 handle pointer.
---------------	------------------------

<i>codecConfig</i>	Codec configure structure. This parameter can be NULL, if NULL, set as default settings. The default setting: <pre>* sgtl_init_t codec_config * codec_config.route = kDA7212_RoutePlayback * codec_config.bus = kDA7212_BusI2S * codec_config.isMaster = false *</pre>
--------------------	---

56.6.5.2 status_t DA7212_ConfigAudioFormat (*da7212_handle_t * handle, uint32_t masterClock_Hz, uint32_t sampleRate_Hz, uint32_t dataBits*)

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>masterClock_Hz</i>	Master clock frequency in Hz. If DA7212 is slave, use the frequency of master, if DA7212 as master, it should be 1228000 while sample rate frequency is 8k/12K/16-K/24K/32K/48K/96K, 11289600 whie sample rate is 11.025K/22.05K/44.1K
<i>sampleRate_Hz</i>	Sample rate frequency in Hz.
<i>dataBits</i>	How many bits in a word of a audio frame, DA7212 only supports 16/20/24/32 bits.

56.6.5.3 status_t DA7212_SetPLLConfig (*da7212_handle_t * handle, da7212_pll_config_t * config*)

Parameters

<i>handle</i>	DA7212 handler pointer.
<i>config</i>	PLL configuration pointer.

56.6.5.4 void DA7212_ChangeHPVolume (*da7212_handle_t * handle, da7212_volume_t volume*)

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>volume</i>	The volume of playback.

56.6.5.5 void DA7212_Mute (*da7212_handle_t * handle, bool isMuted*)

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>isMuted</i>	True means mute, false means unmute.

56.6.5.6 void DA7212_ChangeInput (*da7212_handle_t * handle, da7212_Input_t DA7212_Input*)

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>DA7212_Input</i>	Input data source.

56.6.5.7 void DA7212_ChangeOutput (*da7212_handle_t * handle, da7212_Output_t DA7212_Output*)

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>DA7212_Output</i>	Output device of DA7212.

56.6.5.8 status_t DA7212_SetChannelVolume (*da7212_handle_t * handle, uint32_t channel, uint32_t volume*)

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>channel</i>	shoule be a value of _da7212_channel.
<i>volume</i>	volume range 0 - 0x3F mapped to range -57dB - 6dB.

56.6.5.9 status_t DA7212_SetChannelMute (*da7212_handle_t * handle, uint32_t channel, bool isMute*)

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>channel</i>	shoule be a value of _da7212_channel.
<i>isMute</i>	true is mute, false is unmute.

56.6.5.10 status_t DA7212_SetProtocol (*da7212_handle_t * handle, da7212_protocol_t protocol*)

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>protocol</i>	da7212_protocol_t.

56.6.5.11 status_t DA7212_SetMasterModeBits (*da7212_handle_t * handle, uint32_t bitWidth*)

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>bitWidth</i>	audio data bitwidth.

56.6.5.12 status_t DA7212_WriteRegister (*da7212_handle_t * handle, uint8_t u8Register, uint8_t u8RegisterData*)

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>u8Register</i>	DA7212 register address to be written.
<i>u8RegisterData</i>	Data to be written into register

56.6.5.13 status_t DA7212_ReadRegister (*da7212_handle_t * handle*, *uint8_t u8Register*, *uint8_t * pu8RegisterData*)

Parameters

<i>handle</i>	DA7212 handle pointer.
<i>u8Register</i>	DA7212 register address to be read.
<i>pu8RegisterData</i>	Pointer where the read out value to be stored.

56.6.5.14 status_t DA7212_Deinit (*da7212_handle_t * handle*)

Parameters

<i>handle</i>	DA7212 handle pointer.
---------------	------------------------

56.6.6 Da7212_adapter

56.6.6.1 Overview

Macros

- #define **HAL_CODEC_DA7212_HANDLER_SIZE** (**DA7212_I2C_HANDLER_SIZE** + 4)
codec handler size

Functions

- **status_t HAL_CODEC_DA7212_Init** (void *handle, void *config)
Codec initilization.
- **status_t HAL_CODEC_DA7212_Deinit** (void *handle)
Codec de-initilization.
- **status_t HAL_CODEC_DA7212_SetFormat** (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)
set audio data format.
- **status_t HAL_CODEC_DA7212_SetVolume** (void *handle, uint32_t playChannel, uint32_t volume)
set audio codec module volume.
- **status_t HAL_CODEC_DA7212_SetMute** (void *handle, uint32_t playChannel, bool isMute)
set audio codec module mute.
- **status_t HAL_CODEC_DA7212_SetPower** (void *handle, uint32_t module, bool powerOn)
set audio codec module power.
- **status_t HAL_CODEC_DA7212_SetRecord** (void *handle, uint32_t recordSource)
codec set record source.
- **status_t HAL_CODEC_DA7212_SetRecordChannel** (void *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)
codec set record channel.
- **status_t HAL_CODEC_DA7212_SetPlay** (void *handle, uint32_t playSource)
codec set play source.
- **status_t HAL_CODEC_DA7212_ModuleControl** (void *handle, uint32_t cmd, uint32_t data)
codec module control.
- static **status_t HAL_CODEC_Init** (void *handle, void *config)
Codec initilization.
- static **status_t HAL_CODEC_Deinit** (void *handle)
Codec de-initilization.
- static **status_t HAL_CODEC_SetFormat** (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)
set audio data format.
- static **status_t HAL_CODEC_SetVolume** (void *handle, uint32_t playChannel, uint32_t volume)
set audio codec module volume.
- static **status_t HAL_CODEC_SetMute** (void *handle, uint32_t playChannel, bool isMute)
set audio codec module mute.
- static **status_t HAL_CODEC_SetPower** (void *handle, uint32_t module, bool powerOn)
set audio codec module power.
- static **status_t HAL_CODEC_SetRecord** (void *handle, uint32_t recordSource)
codec set record source.

- static `status_t HAL_CODEC_SetRecordChannel` (void *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)
codec set record channel.
- static `status_t HAL_CODEC_SetPlay` (void *handle, uint32_t playSource)
codec set play source.
- static `status_t HAL_CODEC_ModuleControl` (void *handle, uint32_t cmd, uint32_t data)
codec module control.

56.6.6.2 Function Documentation

56.6.6.2.1 `status_t HAL_CODEC_DA7212_Init(void * handle, void * config)`

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

`kStatus_Success` is success, else initial failed.

56.6.6.2.2 `status_t HAL_CODEC_DA7212_Deinit(void * handle)`

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

`kStatus_Success` is success, else de-initial failed.

56.6.6.2.3 `status_t HAL_CODEC_DA7212_SetFormat(void * handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)`

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.4 status_t HAL_CODEC_DA7212_SetVolume (void * *handle*, uint32_t *playChannel*, uint32_t *volume*)

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.5 status_t HAL_CODEC_DA7212_SetMute (void * *handle*, uint32_t *playChannel*, bool *isMute*)

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.6 status_t HAL_CODEC_DA7212_SetPower (void * *handle*, uint32_t *module*, bool *powerOn*)

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.7 status_t HAL_CODEC_DA7212_SetRecord (void * *handle*, uint32_t *recordSource*)

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.8 status_t HAL_CODEC_DA7212_SetRecordChannel (void * *handle*, uint32_t *leftRecordChannel*, uint32_t *rightRecordChannel*)

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.9 status_t HAL_CODEC_DA7212_SetPlay (void * *handle*, uint32_t *playSource*)

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.10 **status_t HAL_CODEC_DA7212_ModuleControl (void * *handle*, uint32_t *cmd*, uint32_t *data*)**

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.11 **static status_t HAL_CODEC_Init (void * *handle*, void * *config*) [inline], [static]**

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus_Success is success, else initial failed.

56.6.6.2.12 **static status_t HAL_CODEC_Deinit (void * *handle*) [inline], [static]**

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus_Success is success, else de-initial failed.

56.6.6.2.13 static status_t HAL_CODEC_SetFormat(void * *handle*, uint32_t *mclk*, uint32_t *sampleRate*, uint32_t *bitWidth*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.14 static status_t HAL_CODEC_SetVolume(void * *handle*, uint32_t *playChannel*, uint32_t *volume*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.15 static status_t HAL_CODEC_SetMute(void * *handle*, uint32_t *playChannel*, bool *isMute*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.16 static status_t HAL_CODEC_SetPower (void * *handle*, uint32_t *module*, bool *powerOn*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.17 static status_t HAL_CODEC_SetRecord (void * *handle*, uint32_t *recordSource*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.18 static status_t HAL_CODEC_SetRecordChannel (void * *handle*, uint32_t *leftRecordChannel*, uint32_t *rightRecordChannel*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.19 static status_t HAL_CODEC_SetPlay (void * *handle*, uint32_t *playSource*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus_Success is success, else configure failed.

56.6.6.2.20 static status_t HAL_CODEC_ModuleControl (void * *handle*, uint32_t *cmd*, uint32_t *data*) [inline], [static]

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus_Success is success, else configure failed.

56.6.7 CODEC Adapter

56.6.7.1 Overview

Enumerations

- enum {

kCODEC_WM8904,
 kCODEC_WM8960,
 kCODEC_WM8524,
 kCODEC_SGTL5000,
 kCODEC_DA7212,
 kCODEC_CS42888,
 kCODEC_CS42448,
 kCODEC_AK4497,
 kCODEC_AK4458,
 kCODEC_TFA9XXX,
 kCODEC_TFA9896 }

codec type

56.6.7.2 Enumeration Type Documentation

56.6.7.2.1 anonymous enum

Enumerator

<i>kCODEC_WM8904</i>	wm8904
<i>kCODEC_WM8960</i>	wm8960
<i>kCODEC_WM8524</i>	wm8524
<i>kCODEC_SGTL5000</i>	sgtl5000
<i>kCODEC_DA7212</i>	da7212
<i>kCODEC_CS42888</i>	CS42888.
<i>kCODEC_CS42448</i>	CS42448.
<i>kCODEC_AK4497</i>	AK4497.
<i>kCODEC_AK4458</i>	ak4458
<i>kCODEC_TFA9XXX</i>	tfa9xxx
<i>kCODEC_TFA9896</i>	tfa9896

56.6.8 Sgtl5000_adapter

56.6.8.1 Overview

Macros

- #define `HAL_CODEC_SGTL_HANDLER_SIZE` (`SGTL_I2C_HANDLER_SIZE + 4`)
codec handler size

Functions

- `status_t HAL_CODEC_SGTL5000_Init` (void *handle, void *config)
Codec initilization.
- `status_t HAL_CODEC_SGTL5000_Deinit` (void *handle)
Codec de-initilization.
- `status_t HAL_CODEC_SGTL5000_SetFormat` (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)
set audio data format.
- `status_t HAL_CODEC_SGTL5000_SetVolume` (void *handle, uint32_t playChannel, uint32_t volume)
set audio codec module volume.
- `status_t HAL_CODEC_SGTL5000_SetMute` (void *handle, uint32_t playChannel, bool isMute)
set audio codec module mute.
- `status_t HAL_CODEC_SGTL5000_SetPower` (void *handle, uint32_t module, bool powerOn)
set audio codec module power.
- `status_t HAL_CODEC_SGTL5000_SetRecord` (void *handle, uint32_t recordSource)
codec set record source.
- `status_t HAL_CODEC_SGTL5000_SetRecordChannel` (void *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)
codec set record channel.
- `status_t HAL_CODEC_SGTL5000_SetPlay` (void *handle, uint32_t playSource)
codec set play source.
- `status_t HAL_CODEC_SGTL5000_ModuleControl` (void *handle, uint32_t cmd, uint32_t data)
codec module control.
- static `status_t HAL_CODEC_Init` (void *handle, void *config)
Codec initilization.
- static `status_t HAL_CODEC_Deinit` (void *handle)
Codec de-initilization.
- static `status_t HAL_CODEC_SetFormat` (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)
set audio data format.
- static `status_t HAL_CODEC_SetVolume` (void *handle, uint32_t playChannel, uint32_t volume)
set audio codec module volume.
- static `status_t HAL_CODEC_SetMute` (void *handle, uint32_t playChannel, bool isMute)
set audio codec module mute.
- static `status_t HAL_CODEC_SetPower` (void *handle, uint32_t module, bool powerOn)
set audio codec module power.
- static `status_t HAL_CODEC_SetRecord` (void *handle, uint32_t recordSource)
codec set record source.

- static `status_t HAL_CODEC_SetRecordChannel` (void *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)
codec set record channel.
- static `status_t HAL_CODEC_SetPlay` (void *handle, uint32_t playSource)
codec set play source.
- static `status_t HAL_CODEC_ModuleControl` (void *handle, uint32_t cmd, uint32_t data)
codec module control.

56.6.8.2 Function Documentation

56.6.8.2.1 `status_t HAL_CODEC_SGTL5000_Init(void * handle, void * config)`

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

`kStatus_Success` is success, else initial failed.

56.6.8.2.2 `status_t HAL_CODEC_SGTL5000_Deinit(void * handle)`

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

`kStatus_Success` is success, else de-initial failed.

56.6.8.2.3 `status_t HAL_CODEC_SGTL5000_SetFormat(void * handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)`

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.4 status_t HAL_CODEC_SGTL5000_SetVolume (void * *handle*, uint32_t *playChannel*, uint32_t *volume*)

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.5 status_t HAL_CODEC_SGTL5000_SetMute (void * *handle*, uint32_t *playChannel*, bool *isMute*)

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.6 status_t HAL_CODEC_SGTL5000_SetPower (void * *handle*, uint32_t *module*, bool *powerOn*)

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.7 status_t HAL_CODEC_SGTL5000_SetRecord (void * *handle*, uint32_t *recordSource*)

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.8 status_t HAL_CODEC_SGTL5000_SetRecordChannel (void * *handle*, uint32_t *leftRecordChannel*, uint32_t *rightRecordChannel*)

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.9 status_t HAL_CODEC_SGTL5000_SetPlay (void * *handle*, uint32_t *playSource*)

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.10 status_t HAL_CODEC_SGTL5000_ModuleControl (void * *handle*, uint32_t *cmd*, uint32_t *data*)

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.11 static status_t HAL_CODEC_Init (void * *handle*, void * *config*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus_Success is success, else initial failed.

56.6.8.2.12 static status_t HAL_CODEC_Deinit (void * *handle*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus_Success is success, else de-initial failed.

56.6.8.2.13 static status_t HAL_CODEC_SetFormat(void * *handle*, uint32_t *mclk*, uint32_t *sampleRate*, uint32_t *bitWidth*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.14 static status_t HAL_CODEC_SetVolume(void * *handle*, uint32_t *playChannel*, uint32_t *volume*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.15 static status_t HAL_CODEC_SetMute(void * *handle*, uint32_t *playChannel*, bool *isMute*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.16 static status_t HAL_CODEC_SetPower (void * *handle*, uint32_t *module*, bool *powerOn*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.17 static status_t HAL_CODEC_SetRecord (void * *handle*, uint32_t *recordSource*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.18 static status_t HAL_CODEC_SetRecordChannel (void * *handle*, uint32_t *leftRecordChannel*, uint32_t *rightRecordChannel*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.19 static status_t HAL_CODEC_SetPlay (void * *handle*, uint32_t *playSource*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus_Success is success, else configure failed.

56.6.8.2.20 static status_t HAL_CODEC_ModuleControl (void * *handle*, uint32_t *cmd*, uint32_t *data*) [inline], [static]

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus_Success is success, else configure failed.

56.6.9 Wm8960_adapter

56.6.9.1 Overview

Macros

- `#define HAL_CODEC_WM8960_HANDLER_SIZE (WM8960_I2C_HANDLER_SIZE + 4)`
codec handler size

Functions

- `status_t HAL_CODEC_WM8960_Init (void *handle, void *config)`
Codec initilization.
- `status_t HAL_CODEC_WM8960_Deinit (void *handle)`
Codec de-initilization.
- `status_t HAL_CODEC_WM8960_SetFormat (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)`
set audio data format.
- `status_t HAL_CODEC_WM8960_SetVolume (void *handle, uint32_t playChannel, uint32_t volume)`
set audio codec module volume.
- `status_t HAL_CODEC_WM8960_SetMute (void *handle, uint32_t playChannel, bool isMute)`
set audio codec module mute.
- `status_t HAL_CODEC_WM8960_SetPower (void *handle, uint32_t module, bool powerOn)`
set audio codec module power.
- `status_t HAL_CODEC_WM8960_SetRecord (void *handle, uint32_t recordSource)`
codec set record source.
- `status_t HAL_CODEC_WM8960_SetRecordChannel (void *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)`
codec set record channel.
- `status_t HAL_CODEC_WM8960_SetPlay (void *handle, uint32_t playSource)`
codec set play source.
- `status_t HAL_CODEC_WM8960_ModuleControl (void *handle, uint32_t cmd, uint32_t data)`
codec module control.
- `static status_t HAL_CODEC_Init (void *handle, void *config)`
Codec initilization.
- `static status_t HAL_CODEC_Deinit (void *handle)`
Codec de-initilization.
- `static status_t HAL_CODEC_SetFormat (void *handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)`
set audio data format.
- `static status_t HAL_CODEC_SetVolume (void *handle, uint32_t playChannel, uint32_t volume)`
set audio codec module volume.
- `static status_t HAL_CODEC_SetMute (void *handle, uint32_t playChannel, bool isMute)`
set audio codec module mute.
- `static status_t HAL_CODEC_SetPower (void *handle, uint32_t module, bool powerOn)`
set audio codec module power.
- `static status_t HAL_CODEC_SetRecord (void *handle, uint32_t recordSource)`
codec set record source.

- static `status_t HAL_CODEC_SetRecordChannel` (void *handle, uint32_t leftRecordChannel, uint32_t rightRecordChannel)
codec set record channel.
- static `status_t HAL_CODEC_SetPlay` (void *handle, uint32_t playSource)
codec set play source.
- static `status_t HAL_CODEC_ModuleControl` (void *handle, uint32_t cmd, uint32_t data)
codec module control.

56.6.9.2 Function Documentation

56.6.9.2.1 `status_t HAL_CODEC_WM8960_Init(void * handle, void * config)`

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

`kStatus_Success` is success, else initial failed.

56.6.9.2.2 `status_t HAL_CODEC_WM8960_Deinit(void * handle)`

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

`kStatus_Success` is success, else de-initial failed.

56.6.9.2.3 `status_t HAL_CODEC_WM8960_SetFormat(void * handle, uint32_t mclk, uint32_t sampleRate, uint32_t bitWidth)`

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.4 status_t HAL_CODEC_WM8960_SetVolume (void * *handle*, uint32_t *playChannel*, uint32_t *volume*)

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.5 status_t HAL_CODEC_WM8960_SetMute (void * *handle*, uint32_t *playChannel*, bool *isMute*)

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.6 status_t HAL_CODEC_WM8960_SetPower (void * *handle*, uint32_t *module*, bool *powerOn*)

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.7 status_t HAL_CODEC_WM8960_SetRecord (void * *handle*, uint32_t *recordSource*)

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.8 status_t HAL_CODEC_WM8960_SetRecordChannel (void * *handle*, uint32_t *leftRecordChannel*, uint32_t *rightRecordChannel*)

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.9 status_t HAL_CODEC_WM8960_SetPlay (void * *handle*, uint32_t *playSource*)

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.10 status_t HAL_CODEC_WM8960_ModuleControl (void * *handle*, uint32_t *cmd*, uint32_t *data*)

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.11 static status_t HAL_CODEC_Init (void * *handle*, void * *config*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>config</i>	codec configuration.

Returns

kStatus_Success is success, else initial failed.

56.6.9.2.12 static status_t HAL_CODEC_Deinit (void * *handle*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
---------------	---------------

Returns

kStatus_Success is success, else de-initial failed.

56.6.9.2.13 static status_t HAL_CODEC_SetFormat(void * *handle*, uint32_t *mclk*, uint32_t *sampleRate*, uint32_t *bitWidth*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>mclk</i>	master clock frequency in HZ.
<i>sampleRate</i>	sample rate in HZ.
<i>bitWidth</i>	bit width.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.14 static status_t HAL_CODEC_SetVolume(void * *handle*, uint32_t *playChannel*, uint32_t *volume*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>volume</i>	volume value, support 0 ~ 100, 0 is mute, 100 is the maximum volume value.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.15 static status_t HAL_CODEC_SetMute(void * *handle*, uint32_t *playChannel*, bool *isMute*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playChannel</i>	audio codec play channel, can be a value or combine value of _codec_play_channel.
<i>isMute</i>	true is mute, false is unmute.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.16 static status_t HAL_CODEC_SetPower (void * *handle*, uint32_t *module*, bool *powerOn*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>module</i>	audio codec module.
<i>powerOn</i>	true is power on, false is power down.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.17 static status_t HAL_CODEC_SetRecord (void * *handle*, uint32_t *recordSource*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>recordSource</i>	audio codec record source, can be a value or combine value of _codec_record_source.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.18 static status_t HAL_CODEC_SetRecordChannel (void * *handle*, uint32_t *leftRecordChannel*, uint32_t *rightRecordChannel*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>leftRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value or combine value of member in _codec_record_channel.
<i>rightRecord-Channel</i>	audio codec record channel, reference _codec_record_channel, can be a value combine of member in _codec_record_channel.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.19 static status_t HAL_CODEC_SetPlay (void * *handle*, uint32_t *playSource*) [inline], [static]

Parameters

<i>handle</i>	codec handle.
<i>playSource</i>	audio codec play source, can be a value or combine value of _codec_play_source.

Returns

kStatus_Success is success, else configure failed.

56.6.9.2.20 static status_t HAL_CODEC_ModuleControl (void * *handle*, uint32_t *cmd*, uint32_t *data*) [inline], [static]

This function is used for codec module control, support switch digital interface cmd, can be expand to support codec module specific feature

Parameters

<i>handle</i>	codec handle.
<i>cmd</i>	module control cmd, reference _codec_module_ctrl_cmd.
<i>data</i>	value to write, when cmd is kCODEC_ModuleRecordSourceChannel, the data should be a value combine of channel and source, please reference macro CODEC_MODULE_RECORD_SOURCE_CHANNEL(source, LP, LN, RP, RN), reference codec specific driver for detail configurations.

Returns

kStatus_Success is success, else configure failed.

56.7 Sgtl5000

56.7.1 Overview

Data Structures

- struct `sgtl_audio_format_t`
Audio format configuration. [More...](#)
- struct `sgtl_config_t`
Initailize structure of sgtl5000. [More...](#)
- struct `sgtl_handle_t`
SGTL codec handler. [More...](#)

Macros

- #define `CHIP_ID` 0x0000U
Define the register address of sgtl5000.
- #define `SGTL5000_HEADPHONE_MAX_VOLUME_VALUE` 0x7FU
SGTL5000 volume setting range.
- #define `SGTL5000_I2C_ADDR` 0x0A
SGTL5000 I2C address.
- #define `SGTL_I2C_HANDLER_SIZE` CODEC_I2C_MASTER_HANDLER_SIZE
sgtl handle size
- #define `SGTL_I2C_BITRATE` 100000U
sgtl i2c baudrate

Enumerations

- enum `sgtl_module_t` {

 `kSGTL_ModuleADC` = 0x0,
`kSGTL_ModuleDAC`,
`kSGTL_ModuleDAP`,
`kSGTL_ModuleHP`,
`kSGTL_ModuleI2SIN`,
`kSGTL_ModuleI2SOUT`,
`kSGTL_ModuleLineIn`,
`kSGTL_ModuleLineOut`,
`kSGTL_ModuleMicin` }

Modules in Sglt5000 board.
- enum `sgtl_route_t` {

 `kSGTL_RouteBypass` = 0x0,
`kSGTL_RoutePlayback`,
`kSGTL_RoutePlaybackandRecord`,
`kSGTL_RoutePlaybackwithDAP`,
`kSGTL_RoutePlaybackwithDAPandRecord`,
`kSGTL_RouteRecord` }

- *Sgtl5000 data route.*
- enum `sgtl_protocol_t` {

 `kSGTL_BusI2S` = 0x0,

 `kSGTL_BusLeftJustified`,

 `kSGTL_BusRightJustified`,

 `kSGTL_BusPCMA`,

 `kSGTL_BusPCMB` }
- The audio data transfer protocol choice.*
- enum {

 `kSGTL_HeadphoneLeft` = 0,

 `kSGTL_HeadphoneRight` = 1,

 `kSGTL_LineoutLeft` = 2,

 `kSGTL_LineoutRight` = 3 }
- sgtl play channel*
- enum {

 `kSGTL_RecordSourceLineIn` = 0U,

 `kSGTL_RecordSourceMic` = 1U }
- sgtl record source _sgtl_record_source*
- enum {

 `kSGTL_PlaySourceLineIn` = 0U,

 `kSGTL_PlaySourceDAC` = 1U }
- sgtl play source _stgl_play_source*
- enum `sgtl_sclk_edge_t` {

 `kSGTL_SclkValidEdgeRising` = 0U,

 `kSGTL_SclkValidEdgeFailling` = 1U }
- SGTL SCLK valid edge.*

Functions

- `status_t SGTL_Init (sgtl_handle_t *handle, sgtl_config_t *config)`
sgtl5000 initialize function.
- `status_t SGTL_SetDataRoute (sgtl_handle_t *handle, sgtl_route_t route)`
Set audio data route in sgtl5000.
- `status_t SGTL_SetProtocol (sgtl_handle_t *handle, sgtl_protocol_t protocol)`
Set the audio transfer protocol.
- `void SGTL_SetMasterSlave (sgtl_handle_t *handle, bool master)`
Set sgtl5000 as master or slave.
- `status_t SGTL_SetVolume (sgtl_handle_t *handle, sgtl_module_t module, uint32_t volume)`
Set the volume of different modules in sgtl5000.
- `uint32_t SGTL_GetVolume (sgtl_handle_t *handle, sgtl_module_t module)`
Get the volume of different modules in sgtl5000.
- `status_t SGTL_SetMute (sgtl_handle_t *handle, sgtl_module_t module, bool mute)`
Mute/unmute modules in sgtl5000.
- `status_t SGTL_EnableModule (sgtl_handle_t *handle, sgtl_module_t module)`
Enable expected devices.
- `status_t SGTL_DisableModule (sgtl_handle_t *handle, sgtl_module_t module)`
Disable expected devices.
- `status_t SGTL_Deinit (sgtl_handle_t *handle)`

Deinit the sgtl5000 codec.

- **status_t SGTL_ConfigDataFormat** (*sgtl_handle_t* *handle, *uint32_t* mclk, *uint32_t* sample_rate, *uint32_t* bits)
Configure the data format of audio data.
- **status_t SGTL_SetPlay** (*sgtl_handle_t* *handle, *uint32_t* playSource)
select SGTL codec play source.
- **status_t SGTL_SetRecord** (*sgtl_handle_t* *handle, *uint32_t* recordSource)
select SGTL codec record source.
- **status_t SGTL_WriteReg** (*sgtl_handle_t* *handle, *uint16_t* reg, *uint16_t* val)
Write register to sgtl using I2C.
- **status_t SGTL_ReadReg** (*sgtl_handle_t* *handle, *uint16_t* reg, *uint16_t* *val)
Read register from sgtl using I2C.
- **status_t SGTL_ModifyReg** (*sgtl_handle_t* *handle, *uint16_t* reg, *uint16_t* clr_mask, *uint16_t* val)
Modify some bits in the register using I2C.

Driver version

- #define **FSL_SGTL5000_DRIVER_VERSION** (**MAKE_VERSION**(2, 1, 1))
CLOCK driver version 2.1.1.

56.7.2 Data Structure Documentation

56.7.2.1 struct sgtl_audio_format_t

Data Fields

- **uint32_t mclk_HZ**
master clock
- **uint32_t sampleRate**
Sample rate.
- **uint32_t bitWidth**
Bit width.
- **sgtl_sclk_edge_t sclkEdge**
sclk valid edge

56.7.2.2 struct sgtl_config_t

Data Fields

- **sgtl_route_t route**
Audio data route.
- **sgtl_protocol_t bus**
Audio transfer protocol.
- **bool master_slave**
Master or slave.
- **sgtl_audio_format_t format**
audio format

- `uint8_t slaveAddress`
code device slave address
- `codec_i2c_config_t i2cConfig`
i2c bus configuration

Field Documentation

(1) `sgtl_route_t sgtl_config_t::route`

(2) `bool sgtl_config_t::master_slave`

True means master, false means slave.

56.7.2.3 struct sgtl_handle_t

Data Fields

- `sgtl_config_t * config`
sgtl config pointer
- `uint8_t i2cHandle [SGTL_I2C_HANDLER_SIZE]`
i2c handle

56.7.3 Macro Definition Documentation

56.7.3.1 `#define FSL_SGTL5000_DRIVER_VERSION (MAKE_VERSION(2, 1, 1))`

56.7.3.2 `#define CHIP_ID 0x0000U`

56.7.3.3 `#define SGTL5000_I2C_ADDR 0x0A`

56.7.4 Enumeration Type Documentation

56.7.4.1 enum sgtl_module_t

Enumerator

- `kSGTL_ModuleADC` ADC module in SGTL5000.
- `kSGTL_ModuleDAC` DAC module in SGTL5000.
- `kSGTL_ModuleDAP` DAP module in SGTL5000.
- `kSGTL_ModuleHP` Headphone module in SGTL5000.
- `kSGTL_ModuleI2SIN` I2S-IN module in SGTL5000.
- `kSGTL_ModuleI2SOUT` I2S-OUT module in SGTL5000.
- `kSGTL_ModuleLineIn` Line-in module in SGTL5000.
- `kSGTL_ModuleLineOut` Line-out module in SGTL5000.
- `kSGTL_ModuleMicin` Microphone module in SGTL5000.

56.7.4.2 enum sgtl_route_t

Note

Only provide some typical data route, not all route listed. Users cannot combine any routes, once a new route is set, the previous one would be replaced.

Enumerator

- kSGTL_RouteBypass* LINEIN->Headphone.
- kSGTL_RoutePlayback* I2SIN->DAC->Headphone.
- kSGTL_RoutePlaybackandRecord* I2SIN->DAC->Headphone, LINEIN->ADC->I2SOUT.
- kSGTL_RoutePlaybackwithDAP* I2SIN->DAP->DAC->Headphone.
- kSGTL_RoutePlaybackwithDAPandRecord* I2SIN->DAP->DAC->HP, LINEIN->ADC->I2SOUT.
- kSGTL_RouteRecord* LINEIN->ADC->I2SOUT.

56.7.4.3 enum sgtl_protocol_t

Sgtl5000 only supports I2S format and PCM format.

Enumerator

- kSGTL_BusI2S* I2S Type.
- kSGTL_BusLeftJustified* Left justified.
- kSGTL_BusRightJustified* Right Justified.
- kSGTL_BusPCMA* PCMA.
- kSGTL_BusPCMB* PCMB.

56.7.4.4 anonymous enum

Enumerator

- kSGTL_HeadphoneLeft* headphone left channel
- kSGTL_HeadphoneRight* headphone right channel
- kSGTL_LineoutLeft* lineout left channel
- kSGTL_LineoutRight* lineout right channel

56.7.4.5 anonymous enum

Enumerator

- kSGTL_RecordSourceLineIn* record source line in
- kSGTL_RecordSourceMic* record source single end

56.7.4.6 anonymous enum

Enumerator

kSGTL_PlaySourceLineIn play source line in
kSGTL_PlaySourceDAC play source line in

56.7.4.7 enum sgtl_sclk_edge_t

Enumerator

kSGTL_SclkValidEdgeRising SCLK valid edge.
kSGTL_SclkValidEdgeFailling SCLK failling edge.

56.7.5 Function Documentation

56.7.5.1 status_t SGTL_Init(sgtl_handle_t * *handle*, sgtl_config_t * *config*)

This function calls SGTL_I2CInit(), and in this function, some configurations are fixed. The second parameter can be NULL. If users want to change the SGTL5000 settings, a configure structure should be prepared.

Note

If the codec_config is NULL, it would initialize sgtl5000 using default settings. The default setting:

```
* sgtl_init_t codec_config
* codec_config.route = kSGTL_RoutePlaybackandRecord
* codec_config.bus = kSGTL_BusI2S
* codec_config.master = slave
*
```

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>config</i>	sgtl5000 configuration structure. If this pointer equals to NULL, it means using the default configuration.

Returns

Initialization status

56.7.5.2 status_t SGTL_SetDataRoute (sgtl_handle_t * *handle*, sgtl_route_t *route*)

This function would set the data route according to route. The route cannot be combined, as all route would enable different modules.

Note

If a new route is set, the previous route would not work.

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>route</i>	Audio data route in sgtl5000.

56.7.5.3 status_t SGTL_SetProtocol (sgtl_handle_t * *handle*, sgtl_protocol_t *protocol*)

Sgtl5000 only supports I2S, I2S left, I2S right, PCM A, PCM B format.

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>protocol</i>	Audio data transfer protocol.

56.7.5.4 void SGTL_SetMasterSlave (sgtl_handle_t * *handle*, bool *master*)

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>master</i>	1 represent master, 0 represent slave.

56.7.5.5 status_t SGTL_SetVolume (sgtl_handle_t * *handle*, sgtl_module_t *module*, uint32_t *volume*)

This function would set the volume of sgtl5000 modules. This interface set module volume. The function assume that left channel and right channel has the same volume.

kSGTL_ModuleADC volume range: 0 - 0xF, 0dB - 22.5dB
kSGTL_ModuleDAC volume range: 0x3C - 0xF0, 0dB - -90dB
kSGTL_ModuleHP volume range: 0 - 0x7F, 12dB - -51.5dB
kSGTL_ModuleLineOut volume range: 0 - 0x1F, 0.5dB steps

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>module</i>	Sgtl5000 module, such as DAC, ADC and etc.
<i>volume</i>	Volume value need to be set. The value is the exact value in register.

56.7.5.6 `uint32_t SGTL_GetVolume (sgtl_handle_t * handle, sgtl_module_t module)`

This function gets the volume of sgtl5000 modules. This interface get DAC module volume. The function assume that left channel and right channel has the same volume.

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>module</i>	Sgtl5000 module, such as DAC, ADC and etc.

Returns

Module value, the value is exact value in register.

56.7.5.7 `status_t SGTL_SetMute (sgtl_handle_t * handle, sgtl_module_t module, bool mute)`

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>module</i>	Sgtl5000 module, such as DAC, ADC and etc.
<i>mute</i>	True means mute, and false means unmute.

56.7.5.8 `status_t SGTL_EnableModule (sgtl_handle_t * handle, sgtl_module_t module)`

Parameters

<i>handle</i>	Sgtl5000 handle structure.
---------------	----------------------------

<i>module</i>	Module expected to enable.
---------------	----------------------------

56.7.5.9 status_t SGTL_DisableModule (*sgtl_handle_t * handle, sgtl_module_t module*)

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>module</i>	Module expected to enable.

56.7.5.10 status_t SGTL_Deinit (*sgtl_handle_t * handle*)

Shut down Sgtl5000 modules.

Parameters

<i>handle</i>	Sgtl5000 handle structure pointer.
---------------	------------------------------------

56.7.5.11 status_t SGTL_ConfigDataFormat (*sgtl_handle_t * handle, uint32_t mclk, uint32_t sample_rate, uint32_t bits*)

This function would configure the registers about the sample rate, bit depths.

Parameters

<i>handle</i>	Sgtl5000 handle structure pointer.
<i>mclk</i>	Master clock frequency of I2S.
<i>sample_rate</i>	Sample rate of audio file running in sgtl5000. Sgtl5000 now supports 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k and 96k sample rate.
<i>bits</i>	Bit depth of audio file (Sgtl5000 only supports 16bit, 20bit, 24bit and 32 bit in HW).

56.7.5.12 status_t SGTL_SetPlay (*sgtl_handle_t * handle, uint32_t playSource*)

Parameters

<i>handle</i>	Sgtl5000 handle structure pointer.
<i>playSource</i>	play source value, reference _sgtl_play_source.

Returns

kStatus_Success, else failed.

56.7.5.13 status_t SGTL_SetRecord (*sgtl_handle_t * handle, uint32_t recordSource*)

Parameters

<i>handle</i>	Sgtl5000 handle structure pointer.
<i>recordSource</i>	record source value, reference _sgtl_record_source.

Returns

kStatus_Success, else failed.

56.7.5.14 status_t SGTL_WriteReg (*sgtl_handle_t * handle, uint16_t reg, uint16_t val*)

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>reg</i>	The register address in sgtl.
<i>val</i>	Value needs to write into the register.

56.7.5.15 status_t SGTL_ReadReg (*sgtl_handle_t * handle, uint16_t reg, uint16_t * val*)

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>reg</i>	The register address in sgtl.

<i>val</i>	Value written to.
------------	-------------------

56.7.5.16 status_t SGTL_ModifyReg (*srtl_handle_t * handle, uint16_t reg, uint16_t clr_mask, uint16_t val*)

Parameters

<i>handle</i>	Sgtl5000 handle structure.
<i>reg</i>	The register address in srtl.
<i>clr_mask</i>	The mask code for the bits want to write. The bit you want to write should be 0.
<i>val</i>	Value needs to write into the register.

56.8 Wm8960

56.8.1 Overview

Data Structures

- struct `wm8960_audio_format_t`
wm8960 audio format [More...](#)
- struct `wm8960_master_sysclk_config_t`
wm8960 master system clock configuration [More...](#)
- struct `wm8960_config_t`
Initialize structure of WM8960. [More...](#)
- struct `wm8960_handle_t`
wm8960 codec handler [More...](#)

Macros

- #define `WM8960_I2C_HANDLER_SIZE` CODEC_I2C_MASTER_HANDLER_SIZE
wm8960 handle size
- #define `WM8960_LINVOL` 0x0U
Define the register address of WM8960.
- #define `WM8960_CACHEREGNUM` 56U
Cache register number.
- #define `WM8960_CLOCK2_BCLK_DIV_MASK` 0xFU
WM8960 CLOCK2 bits.
- #define `WM8960_IFACE1_FORMAT_MASK` 0x03U
WM8960_IFACE1 FORMAT bits.
- #define `WM8960_IFACE1_WL_MASK` 0x0CU
WM8960_IFACE1 WL bits.
- #define `WM8960_IFACE1_LRP_MASK` 0x10U
WM8960_IFACE1 LRP bit.
- #define `WM8960_IFACE1_DLRSWAP_MASK` 0x20U
WM8960_IFACE1 DLRSWAP bit.
- #define `WM8960_IFACE1_MS_MASK` 0x40U
WM8960_IFACE1 MS bit.
- #define `WM8960_IFACE1_BCLKINV_MASK` 0x80U
WM8960_IFACE1 BCLKINV bit.
- #define `WM8960_IFACE1_ALRSWAP_MASK` 0x100U
WM8960_IFACE1 ALRSWAP bit.
- #define `WM8960_POWER1_VREF_MASK` 0x40U
WM8960_POWER1.
- #define `WM8960_POWER2_DACL_MASK` 0x100U
WM8960_POWER2.
- #define `WM8960_I2C_ADDR` 0x1A
WM8960 I2C address.
- #define `WM8960_I2C_BAUDRATE` (100000U)
WM8960 I2C baudrate.
- #define `WM8960_ADC_MAX_VOLUME_vVALUE` 0xFFU
WM8960 maximum volume value.

Enumerations

- enum `wm8960_module_t` {

 `kWM8960_ModuleADC` = 0,

 `kWM8960_ModuleDAC` = 1,

 `kWM8960_ModuleVREF` = 2,

 `kWM8960_ModuleHP` = 3,

 `kWM8960_ModuleMICB` = 4,

 `kWM8960_ModuleMIC` = 5,

 `kWM8960_ModuleLineIn` = 6,

 `kWM8960_ModuleLineOut` = 7,

 `kWM8960_ModuleSpeaker` = 8,

 `kWM8960_ModuleOMIX` = 9
 }

Modules in WM8960 board.
- enum {

 `kWM8960_HeadphoneLeft` = 1,

 `kWM8960_HeadphoneRight` = 2,

 `kWM8960_SpeakerLeft` = 4,

 `kWM8960_SpeakerRight` = 8
 }

wm8960 play channel
- enum `wm8960_play_source_t` {

 `kWM8960_PlaySourcePGA` = 1,

 `kWM8960_PlaySourceInput` = 2,

 `kWM8960_PlaySourceDAC` = 4
 }

wm8960 play source
- enum `wm8960_route_t` {

 `kWM8960_RouteBypass` = 0,

 `kWM8960_RoutePlayback` = 1,

 `kWM8960_RoutePlaybackandRecord` = 2,

 `kWM8960_RouteRecord` = 5
 }

WM8960 data route.
- enum `wm8960_protocol_t` {

 `kWM8960_BusI2S` = 2,

 `kWM8960_BusLeftJustified` = 1,

 `kWM8960_BusRightJustified` = 0,

 `kWM8960_BusPCMA` = 3,

 `kWM8960_BusPCMB` = 3 | (1 << 4)
 }

The audio data transfer protocol choice.
- enum `wm8960_input_t` {

 `kWM8960_InputClosed` = 0,

 `kWM8960_InputSingleEndedMic` = 1,

 `kWM8960_InputDifferentialMicInput2` = 2,

 `kWM8960_InputDifferentialMicInput3` = 3,

 `kWM8960_InputLineINPUT2` = 4,

 `kWM8960_InputLineINPUT3` = 5
 }

wm8960 input source

- enum {

kWM8960_AudioSampleRate8KHz = 8000U,
 kWM8960_AudioSampleRate11025Hz = 11025U,
 kWM8960_AudioSampleRate12KHz = 12000U,
 kWM8960_AudioSampleRate16KHz = 16000U,
 kWM8960_AudioSampleRate22050Hz = 22050U,
 kWM8960_AudioSampleRate24KHz = 24000U,
 kWM8960_AudioSampleRate32KHz = 32000U,
 kWM8960_AudioSampleRate44100Hz = 44100U,
 kWM8960_AudioSampleRate48KHz = 48000U,
 kWM8960_AudioSampleRate96KHz = 96000U,
 kWM8960_AudioSampleRate192KHz = 192000U,
 kWM8960_AudioSampleRate384KHz = 384000U }

audio sample rate definition
 - enum {

kWM8960_AudioBitWidth16bit = 16U,
 kWM8960_AudioBitWidth20bit = 20U,
 kWM8960_AudioBitWidth24bit = 24U,
 kWM8960_AudioBitWidth32bit = 32U }

audio bit width
 - enum **wm8960_sysclk_source_t** {

kWM8960_SysClkSourceMclk = 0U,
 kWM8960_SysClkSourceInternalPLL = 1U }
- wm8960 sysclk source*

Functions

- status_t **WM8960_Init** (wm8960_handle_t *handle, const **wm8960_config_t** *config)
WM8960 initialize function.
- status_t **WM8960_Deinit** (wm8960_handle_t *handle)
Deinit the WM8960 codec.
- status_t **WM8960_SetDataRoute** (wm8960_handle_t *handle, **wm8960_route_t** route)
Set audio data route in WM8960.
- status_t **WM8960_SetLeftInput** (wm8960_handle_t *handle, **wm8960_input_t** input)
Set left audio input source in WM8960.
- status_t **WM8960_SetRightInput** (wm8960_handle_t *handle, **wm8960_input_t** input)
Set right audio input source in WM8960.
- status_t **WM8960_SetProtocol** (wm8960_handle_t *handle, **wm8960_protocol_t** protocol)
Set the audio transfer protocol.
- void **WM8960_SetMasterSlave** (wm8960_handle_t *handle, bool master)
Set WM8960 as master or slave.
- status_t **WM8960_SetVolume** (wm8960_handle_t *handle, **wm8960_module_t** module, uint32_t volume)
Set the volume of different modules in WM8960.
- uint32_t **WM8960_GetVolume** (wm8960_handle_t *handle, **wm8960_module_t** module)
Get the volume of different modules in WM8960.
- status_t **WM8960_SetMute** (wm8960_handle_t *handle, **wm8960_module_t** module, bool is-

Enabled)

Mute modules in WM8960.

- **status_t WM8960_SetModule** (`wm8960_handle_t` *handle, `wm8960_module_t` module, bool isEnabled)

Enable/disable expected devices.
- **status_t WM8960_SetPlay** (`wm8960_handle_t` *handle, `uint32_t` playSource)

SET the WM8960 play source.
- **status_t WM8960_ConfigDataFormat** (`wm8960_handle_t` *handle, `uint32_t` sysclk, `uint32_t` sample_rate, `uint32_t` bits)

Configure the data format of audio data.
- **status_t WM8960_SetJackDetect** (`wm8960_handle_t` *handle, bool isEnabled)

Enable/disable jack detect feature.
- **status_t WM8960_WriteReg** (`wm8960_handle_t` *handle, `uint8_t` reg, `uint16_t` val)

Write register to WM8960 using I2C.
- **status_t WM8960_ReadReg** (`uint8_t` reg, `uint16_t` *val)

Read register from WM8960 using I2C.
- **status_t WM8960_ModifyReg** (`wm8960_handle_t` *handle, `uint8_t` reg, `uint16_t` mask, `uint16_t` val)

Modify some bits in the register using I2C.

Driver version

- #define **FSL_WM8960_DRIVER_VERSION** (`MAKE_VERSION(2, 2, 0)`)

CLOCK driver version 2.2.0.

56.8.2 Data Structure Documentation

56.8.2.1 struct `wm8960_audio_format_t`

Data Fields

- `uint32_t mclk_HZ`
master clock frequency
- `uint32_t sampleRate`
sample rate
- `uint32_t bitWidth`
bit width

56.8.2.2 struct `wm8960_master_sysclk_config_t`

Data Fields

- `wm8960_sysclk_source_t sysclkSource`
sysclk source
- `uint32_t sysclkFreq`
PLL output frequency value.

56.8.2.3 struct `wm8960_config_t`

Data Fields

- `wm8960_route_t route`
Audio data route.
- `wm8960_protocol_t bus`
Audio transfer protocol.
- `wm8960_audio_format_t format`
Audio format.
- `bool master_slave`
Master or slave.
- `wm8960_master_sysclk_config_t masterClock`
master clock configurations
- `bool enableSpeaker`
True means enable class D speaker as output, false means no.
- `wm8960_input_t leftInputSource`
Left input source for WM8960.
- `wm8960_input_t rightInputSource`
Right input source for WM8960.
- `wm8960_play_source_t playSource`
play source
- `uint8_t slaveAddress`
wm8960 device address
- `codec_i2c_config_t i2cConfig`
i2c configuration

Field Documentation

(1) `wm8960_route_t wm8960_config_t::route`

(2) `bool wm8960_config_t::master_slave`

56.8.2.4 struct `wm8960_handle_t`

Data Fields

- `const wm8960_config_t * config`
wm8904 config pointer
- `uint8_t i2cHandle [WM8960_I2C_HANDLER_SIZE]`
i2c handle

56.8.3 Macro Definition Documentation

56.8.3.1 #define `WM8960_LINVOL 0x0U`

56.8.3.2 #define `WM8960_I2C_ADDR 0x1A`

56.8.4 Enumeration Type Documentation

56.8.4.1 enum `wm8960_module_t`

Enumerator

- kWM8960_ModuleADC* ADC module in WM8960.
- kWM8960_ModuleDAC* DAC module in WM8960.
- kWM8960_ModuleVREF* VREF module.
- kWM8960_ModuleHP* Headphone.
- kWM8960_ModuleMICB* Mic bias.
- kWM8960_ModuleMIC* Input Mic.
- kWM8960_ModuleLineIn* Analog in PGA.
- kWM8960_ModuleLineOut* Line out module.
- kWM8960_ModuleSpeaker* Speaker module.
- kWM8960_ModuleOMIX* Output mixer.

56.8.4.2 anonymous enum

Enumerator

- kWM8960_HeadphoneLeft* wm8960 headphone left channel
- kWM8960_HeadphoneRight* wm8960 headphone right channel
- kWM8960_SpeakerLeft* wm8960 speaker left channel
- kWM8960_SpeakerRight* wm8960 speaker right channel

56.8.4.3 enum `wm8960_play_source_t`

Enumerator

- kWM8960_PlaySourcePGA* wm8960 play source PGA
- kWM8960_PlaySourceInput* wm8960 play source Input
- kWM8960_PlaySourceDAC* wm8960 play source DAC

56.8.4.4 enum `wm8960_route_t`

Only provide some typical data route, not all route listed. Note: Users cannot combine any routes, once a new route is set, the previous one would be replaced.

Enumerator

- kWM8960_RouteBypass* LINEIN->Headphone.
- kWM8960_RoutePlayback* I2SIN->DAC->Headphone.
- kWM8960_RoutePlaybackandRecord* I2SIN->DAC->Headphone, LINEIN->ADC->I2SOUT.
- kWM8960_RouteRecord* LINEIN->ADC->I2SOUT.

56.8.4.5 enum `wm8960_protocol_t`

WM8960 only supports I2S format and PCM format.

Enumerator

- kWM8960_BusI2S* I2S type.
- kWM8960_BusLeftJustified* Left justified mode.
- kWM8960_BusRightJustified* Right justified mode.
- kWM8960_BusPCMA* PCM A mode.
- kWM8960_BusPCMB* PCM B mode.

56.8.4.6 enum `wm8960_input_t`

Enumerator

- kWM8960_InputClosed* Input device is closed.
- kWM8960_InputSingleEndedMic* Input as single ended mic, only use L/RINPUT1.
- kWM8960_InputDifferentialMicInput2* Input as differential mic, use L/RINPUT1 and L/RINPUT2.
- kWM8960_InputDifferentialMicInput3* Input as differential mic, use L/RINPUT1 and L/RINPUT3.
- kWM8960_InputLineINPUT2* Input as line input, only use L/RINPUT2.
- kWM8960_InputLineINPUT3* Input as line input, only use L/RINPUT3.

56.8.4.7 anonymous enum

Enumerator

- kWM8960_AudioSampleRate8KHz* Sample rate 8000 Hz.
- kWM8960_AudioSampleRate11025Hz* Sample rate 11025 Hz.
- kWM8960_AudioSampleRate12KHz* Sample rate 12000 Hz.
- kWM8960_AudioSampleRate16KHz* Sample rate 16000 Hz.
- kWM8960_AudioSampleRate22050Hz* Sample rate 22050 Hz.
- kWM8960_AudioSampleRate24KHz* Sample rate 24000 Hz.
- kWM8960_AudioSampleRate32KHz* Sample rate 32000 Hz.
- kWM8960_AudioSampleRate44100Hz* Sample rate 44100 Hz.
- kWM8960_AudioSampleRate48KHz* Sample rate 48000 Hz.
- kWM8960_AudioSampleRate96KHz* Sample rate 96000 Hz.
- kWM8960_AudioSampleRate192KHz* Sample rate 192000 Hz.
- kWM8960_AudioSampleRate384KHz* Sample rate 384000 Hz.

56.8.4.8 anonymous enum

Enumerator

<i>kWM8960_AudioBitWidth16bit</i>	audio bit width 16
<i>kWM8960_AudioBitWidth20bit</i>	audio bit width 20
<i>kWM8960_AudioBitWidth24bit</i>	audio bit width 24
<i>kWM8960_AudioBitWidth32bit</i>	audio bit width 32

56.8.4.9 enum **wm8960_sysclk_source_t**

Enumerator

<i>kWM8960_SysClkSourceMclk</i>	sysclk source from external MCLK
<i>kWM8960_SysClkSourceInternalPLL</i>	sysclk source from internal PLL

56.8.5 Function Documentation

56.8.5.1 status_t **WM8960_Init** (**wm8960_handle_t * handle**, **const wm8960_config_t * config**)

The second parameter is NULL to WM8960 in this version. If users want to change the settings, they have to use `wm8960_write_reg()` or `wm8960_modify_reg()` to set the register value of WM8960. Note-: If the `codec_config` is NULL, it would initialize WM8960 using default settings. The default setting: `codec_config->route = kWM8960_RoutePlaybackandRecord` `codec_config->bus = kWM8960_BusI2S` `codec_config->master = slave`

Parameters

<i>handle</i>	WM8960 handle structure.
<i>config</i>	WM8960 configuration structure.

56.8.5.2 status_t **WM8960_Deinit** (**wm8960_handle_t * handle**)

This function close all modules in WM8960 to save power.

Parameters

<i>handle</i>	WM8960 handle structure pointer.
---------------	----------------------------------

56.8.5.3 status_t WM8960_SetDataRoute (*wm8960_handle_t * handle*, *wm8960_route_t route*)

This function would set the data route according to route. The route cannot be combined, as all route would enable different modules. Note: If a new route is set, the previous route would not work.

Parameters

<i>handle</i>	WM8960 handle structure.
<i>route</i>	Audio data route in WM8960.

56.8.5.4 status_t WM8960_SetLeftInput (`wm8960_handle_t * handle, wm8960_input_t input`)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>input</i>	Audio input source.

56.8.5.5 status_t WM8960_SetRightInput (`wm8960_handle_t * handle, wm8960_input_t input`)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>input</i>	Audio input source.

56.8.5.6 status_t WM8960_SetProtocol (`wm8960_handle_t * handle, wm8960_protocol_t protocol`)

WM8960 only supports I2S, left justified, right justified, PCM A, PCM B format.

Parameters

<i>handle</i>	WM8960 handle structure.
<i>protocol</i>	Audio data transfer protocol.

56.8.5.7 void WM8960_SetMasterSlave (`wm8960_handle_t * handle, bool master`)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>master</i>	1 represent master, 0 represent slave.

56.8.5.8 status_t WM8960_SetVolume (*wm8960_handle_t * handle, wm8960_module_t module, uint32_t volume*)

This function would set the volume of WM8960 modules. Uses need to appoint the module. The function assume that left channel and right channel has the same volume.

Module:kWM8960_ModuleADC, volume range value: 0 is mute, 1-255 is -97db to 30db Module:kWM8960_ModuleDAC, volume range value: 0 is mute, 1-255 is -127db to 0db Module:kWM8960_ModuleHP, volume range value: 0 - 2F is mute, 0x30 - 0x7F is -73db to 6db Module:kWM8960_ModuleLineIn, volume range value: 0 - 0x3F is -17.25db to 30db Module:kWM8960_ModuleSpeaker, volume range value: 0 - 2F is mute, 0x30 - 0x7F is -73db to 6db

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Module to set volume, it can be ADC, DAC, Headphone and so on.
<i>volume</i>	Volume value need to be set.

56.8.5.9 uint32_t WM8960_GetVolume (*wm8960_handle_t * handle, wm8960_module_t module*)

This function gets the volume of WM8960 modules. Uses need to appoint the module. The function assume that left channel and right channel has the same volume.

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Module to set volume, it can be ADC, DAC, Headphone and so on.

Returns

Volume value of the module.

56.8.5.10 status_t WM8960_SetMute (*wm8960_handle_t * handle, wm8960_module_t module, bool isEnabled*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Modules need to be mute.
<i>isEnabled</i>	Mute or unmute, 1 represent mute.

56.8.5.11 status_t WM8960_SetModule (*wm8960_handle_t * handle, wm8960_module_t module, bool isEnabled*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>module</i>	Module expected to enable.
<i>isEnabled</i>	Enable or disable moudles.

56.8.5.12 status_t WM8960_SetPlay (*wm8960_handle_t * handle, uint32_t playSource*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>playSource</i>	play source , can be a value combine of kWM8960_ModuleHeadphoneSourcePG-A, kWM8960_ModuleHeadphoneSourceDAC, kWM8960_ModulePlaySourceInput, kWM8960_ModulePlayMonoRight, kWM8960_ModulePlayMonoLeft.

Returns

kStatus_WM8904_Success if successful, different code otherwise..

56.8.5.13 status_t WM8960_ConfigDataFormat (*wm8960_handle_t * handle, uint32_t sysclk, uint32_t sample_rate, uint32_t bits*)

This function would configure the registers about the sample rate, bit depths.

Parameters

<i>handle</i>	WM8960 handle structure pointer.
<i>sysclk</i>	system clock of the codec which can be generated by MCLK or PLL output.
<i>sample_rate</i>	Sample rate of audio file running in WM8960. WM8960 now supports 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k and 96k sample rate.
<i>bits</i>	Bit depth of audio file (WM8960 only supports 16bit, 20bit, 24bit and 32 bit in HW).

56.8.5.14 status_t WM8960_SetJackDetect (*wm8960_handle_t * handle, bool isEnabled*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>isEnabled</i>	Enable or disable moudles.

56.8.5.15 status_t WM8960_WriteReg (*wm8960_handle_t * handle, uint8_t reg, uint16_t val*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>reg</i>	The register address in WM8960.
<i>val</i>	Value needs to write into the register.

56.8.5.16 status_t WM8960_ReadReg (*uint8_t reg, uint16_t * val*)

Parameters

<i>reg</i>	The register address in WM8960.
<i>val</i>	Value written to.

56.8.5.17 status_t WM8960_ModifyReg (*wm8960_handle_t * handle, uint8_t reg, uint16_t mask, uint16_t val*)

Parameters

<i>handle</i>	WM8960 handle structure.
<i>reg</i>	The register address in WM8960.
<i>mask</i>	The mask code for the bits want to write. The bit you want to write should be 0.
<i>val</i>	Value needs to write into the register.

56.9 Serial_port_swo

56.9.1 Overview

Data Structures

- struct `serial_port_swo_config_t`
serial port swo config struct [More...](#)

Macros

- #define `SERIAL_PORT_SWO_HANDLE_SIZE` (12U)
serial port swo handle size

Enumerations

- enum `serial_port_swo_protocol_t` {

`kSerialManager_SwoProtocolManchester` = 1U,
`kSerialManager_SwoProtocolNrz` = 2U }

serial port swo protocol

56.9.2 Data Structure Documentation

56.9.2.1 struct serial_port_swo_config_t

Data Fields

- `uint32_t clockRate`
clock rate
- `uint32_t baudRate`
baud rate
- `uint32_t port`
Port used to transfer data.
- `serial_port_swo_protocol_t protocol`
SWO protocol.

56.9.3 Enumeration Type Documentation

56.9.3.1 enum serial_port_swo_protocol_t

Enumerator

`kSerialManager_SwoProtocolManchester` SWO Manchester protocol.
`kSerialManager_SwoProtocolNrz` SWO UART/NRZ protocol.

56.10 Serial_port_uart

56.10.1 Overview

Macros

- #define **SERIAL_PORT_UART_DMA_RECEIVE_DATA_LENGTH** (64U)
serial port uart handle size
- #define **SERIAL_USE_CONFIGURE_STRUCTURE** (0U)
Enable or disable the configure structure pointer.

Enumerations

- enum **serial_port_uart_parity_mode_t** {

 kSerialManager_UartParityDisabled = 0x0U,

 kSerialManager_UartParityEven = 0x2U,

 kSerialManager_UartParityOdd = 0x3U }

serial port uart parity mode
- enum **serial_port_uart_stop_bit_count_t** {

 kSerialManager_UartOneStopBit = 0U,

 kSerialManager_UartTwoStopBit = 1U }

serial port uart stop bit count

56.10.2 Enumeration Type Documentation

56.10.2.1 enum serial_port_uart_parity_mode_t

Enumerator

kSerialManager_UartParityDisabled Parity disabled.
kSerialManager_UartParityEven Parity even enabled.
kSerialManager_UartParityOdd Parity odd enabled.

56.10.2.2 enum serial_port_uart_stop_bit_count_t

Enumerator

kSerialManager_UartOneStopBit One stop bit.
kSerialManager_UartTwoStopBit Two stop bits.

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