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### Revision History

Revision	Date	Author	Change Description
1.0	04/07/2015	P. Gandhi	Formal Release



# 1 Introduction

This document describes the pin mapping for the Ampak WSDB-750-GN Wi-Fi Module.

## 1.1 About this Document

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This document describes the mapping of the pins for the Ayla Enabled Module to the pins on the Ampak WSDB-750GN Wi-Fi Network Controller Module.

## 1.2 Intended Audience

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This document is intended for module manufacturers who want to configure Ayla Devices.

## 1.3 Related Documentation

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- Ayla Module/MCU Interface Specification, AY006MSP0.

## 2 Signal pin-outs

The pin mapping for the Ayla Enabled Module and the associated WSDB-750GN module pin names, pin numbers are shown below in Table 1.

Table 1. Module Pin Mapping

Ayla Signal Name	WSDB-750GN Pin Name	WSDB-750GN Module Pin	I/O	Description
SPI_SSN	PB1	36	I	SPI Slave Select
SPI_SCK	PB0	37	I	SPI Clock
SPI_MOSI	PB8	31	I	SPI Master Out Slave In
SPI_MISO	PA12	27	O	SPI Master In Slave Out
UART_TX	PA2	8	O	UART Transmit
UART_RX	PA3	12	I	UART Receive
UART_CTS	PA0	14	I	UART CTS
UART_RTS	PA1	9	O	UART RTS
READY_N	PA11	35	O	Module Initialized
INTR_N	PA4	38	O	Interrupt output
RESET_N	MICRO_RST_N	13	I/O	Module Reset
LINK_N	PB14	33	O	ADS Link Status
WKUP	PA0	14	I	Wake Up Module
VDD	VDD	40	PI	DC supply for Module
GND	GND	20	-	Ground

### 3 Additional pins

Some of the additional pins on the WSDB-750GN module required for normal operation are listed below in Table 2.

Table 2. Additional Module Pins

WSDB-750GN Pin Name	WSDB-750GN Module Pin	I/O	Description
VBAT	10	PI	Power supply for backup circuitry

## 4 Programming pins

The pins on the WSDB-750GN module required to program and update the firmware are listed below in Table 3. These pins are optional and required only to provide the ability to perform firmware download to the module.

Table 3. Programming Pins

WSDB-750GN Pin Name	WSDB-750GN Module Pin
UART_TX	30
UART_RX	29
JTMS	26
JTCK	25



## 5 Programming header

The pins required to flash and update the module along with the recommended header configuration is shown in Figure 1.

Figure 1. Programming header

MICRO_RST_N	1	2	VDD
JTMS	3	4	UART_RX
GND	5	6	UART_TX
JTCK	7	8	GND



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