Application Note

Pin Mapping for Murata Type-1LD Wi-Fi Module

For Murata LBEE5PA1LD

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Contact Information

Ayla Networks TECHNICAL SUPPORT and SALES

Contact Technical Support: http://help.aylasupport.com
or via email at support@aylanetworks.com

Contact Sales: https://www.aylanetworks.com/company/contact-us

Ayla Networks REGIONAL OFFICES

GREATER CHINA
Shenzhen
Room 310-311
City University of Hong Kong
Research Institute Building
No. 8 Yuexing 1st Road
High-Tech Industrial Park
Nanshan District
Shenzhen, China
Phone: 0755-86581520

HEADQUARTERS
Silicon Valley
4250 Burton Drive, Suite 100
Santa Clara, CA 95054
United States
Phone: +1 408 830 9844
Fax: +1 408 716 2621

JAPAN
Room #701,
No.2 Ueno Building 3-7-18,
Shin-Yokohama, Kohoku Ward
Yokohama City, 222-0033 Japan
Telephone: 045-594-8406

EUROPE
Munich
Building 64.07
Room EG.A.076 / 14b
Rupert-Mayer-Str. 44
D-81379 München
Germany

TAIWAN
Taipei
5F No. 250 Sec. 1
Neihu Road, Neihu District
Taipei 11493, Taiwan

For a Complete Contact List of Our Offices in the US, China, Europe, Taiwan, and Japan:
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Revision History

Revision	Date	Author	Change Description
1	2017/Nov/30	Gokul R.	Initial document
2	2018/Oct/16	Deepanker P.	Corrections to pin mapping for SPI and READY_N Added information about OSC and BOOT0 pins

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1 Introduction

This document describes the pin mapping for the Ayla features of the Murata Type-1LD, including descriptions of the Ayla signals present on each of the Type-1LD pins.

1.1 Intended Audience

This document is intended for programmers and hardware engineers that need to connect the Murata Type-1LD module to other hardware components.

1.2 Related Documentation

Setup for Murata Type 1LD Module *(AY006ULD)*

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2 Signal Pin-outs

Ayla Signal Name	Module Pin Name	Module Pin	Daughtercard Connector Pin	I/O	Description
SPI_SSN	PA4	41	23	I/O	SPI Slave Select
SPI_SCK	PA5	40	25	I/O	SPI Clock
SPI_MOSI	PA7	39	26	I/O	SPI Master Out Slave In
SPI_MISO	PA6	42	24	I/O	SPI Master In Slave Out
MCU_UART_TX	PA9	24	16	O	MCU UART Transmit
MCU_UART_RX	PA10	25	15	I	MCU UART Receive
MCU_UART_CTSn	PA11	26	14	I	MCU UART CTS
MCU_UART_RTSn	PA12	27	11	O	MCU UART RTS
READY_N	PC4	59	43	O	Module Initialized
INTR_N	PC5	49	28	O	Interrupt Output
RESET_N	nRESET	32	18	I	Module Reset
LINK_N		-			
WKUP		-			

3 Additional Pins

Module Pin Name	Module Pin	Daughtercard Connector Pin	Description
VDD_WLAN	4	59	3V DC Supply for Module
VDD_IO_MCU	34	31	3V DC Supply for Module
OSC32_OUT	1	-	32 kHz Oscillator Output
OSC32_IN	2	-	32 kHz Oscillator Input
GND	3, 5, 10, 12, 13, 23, 33, 35, 46-48, 64-70	5, 6, 12, 13, 21, 22, 29, 30, 32, 33, 45, 46, 57, 58, 61-64	
BOOT0	38	47	Must be grounded

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4 Programming Pins

The pins required to program, configure and update the firmware are listed below.

Ayla Signal Name	Module Pin Name	Module Pin	Daughtercard Connector Pin
CONSOLE_UART_TX	PC6	37	35
CONSOLE_UART_RX	PC7	36	36
SWDIO	PA13	20	38
SWDCLK	PA14	21	42

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4250 Burton Drive, Santa Clara, CA 95054
Phone: +1 408 830 9844
Fax: +1 408 716 2621