U1B

FMC_D2	164	PD0	PG0	77	FMC_A10
FMC_D3	165	PD1	PG1	78	FMC_A11
	166	PD2	PG2	129	
SPI2_SCK	167	PD3	PG3	130	
	168	PD4	PG4	131	FMC_BA0
	169	PD5	PG5	132	FMC_BA1
SPI3_MOSI	172	PD6	PG6	133	
	173	PD7	PG7	134	
FMC_D13	108	PD8	PG8	135	FMC_SDCLK
FMC_D14	109	PD9	PG9	178	
FMC_D15	110	PD10	PG10	179	
	111	PD11	PG11	180	
ENC3_I	112	TIM4_CH1	PG12	181	LCD_B4
ENC3_Q	113	TIM4_CH2	PG13	182	SPI6_SCK
FMC_D0	116	PD14	PG14	183	SPI6_MOSI
FMC_D1	117	PD15	PG15	191	FMC_SDNCAS
FMC_NBL0	200	PE0			
FMC_NBL1	201	PE1			
SPI4_SCK	1	PE2	PH2	46	
	2	PE3	PH3	47	FMC_SDNE0
LCD_B0	3	PE4	PH4	48	
SPI4_MISO	4	PE5	PH5	49	FMC_SDNWE
SPI4_MOSI	5	PE6	PH6	96	SPI5_SCK
FMC_D4	79	PE7	PH7	97	SPI5_MISO
FMC_D5	80	PE8	PH8	98	FMC_D16
FMC_D6	81	PE9	PH9	99	FMC_D17
FMC_D7	84	PE10	PH10	100	FMC_D18
FMC_D8	85	PE11	PH11	101	FMC_D19
FMC_D9	86	PE12	PH12	102	FMC_D20
FMC_D10	87	PE13	PH13	151	FMC_D21
FMC_D11	88	PE14	PH14	152	FMC_D22
FMC_D12	89	PE15	PH15	153	FMC_D23
FMC_A0	16	PF0	PI0	154	FMC_D24
FMC_A1	17	PF1	PI1	155	FMC_D25
FMC_A2	18	PF2	PI2	156	FMC_D26
FMC_A3	22	PF3	PI3	157	FMC_D27
FMC_A4	23	PF4	PI4	205	
FMC_A5	24	PF5	PI5	206	
	27	PF6	PI6	207	FMC_D28
SPI5_SCK	28	PF7	PI7	208	FMC_D29
SPI5_MISO	29	PF8	PI8	7	LCD_DISP
SPI5_MOSI	30	PF9	PI9	11	FMC_D30
ADC3	31	ADC3	PI10	12	FMC_D31
FMC_SDNRAS	70	PF11	PI11	13	LCD_INT
FMC_A6	71	PF12	PI12	19	LCD_HSYNC
FMC_A7	74	PF13	PI13	20	LCD_VSYNC
FMC_A8	75	PF14	PI14	21	LCD_CLK
FMC_A9	76	PF15	PI15	64	LCD_R0

STM32F746BGT6

U1A

ENC1_I	43	TIM2_CH1	ADC1	35	ADC1
ENC1_Q	44	TIM2_CH2	PC1	36	SPI2_MOSI
	45	PA2	PC2	37	SPI2_MISO
	50	PA3	PC3	38	FMC_SDCKE0
DAC1	53	DAC1	PC4	57	
DAC2	54	DAC2	ADC2	58	ADC2
ENC2_I	55	TIM3_CH1	TIM8_CH1	138	ENC4_I
ENC2_Q	56	TIM3_CH2	TIM8_CH2	139	ENC4_Q
MCO1	142	PA8	PC8	140	
SPI2_SCK	143	PA9	PC9	141	MCO2
	144	PA10	PC10	161	SPI3_SCK
OTG_FS_N	145	PA11	PC11	162	SPI3_MISO
OTG_FS_P	146	PA12	PC12	163	SPI3_MOSI
SWDIO	147	PA13	PC13	8	
SWCLK	159	PA14			
TIM2_CH1	160	PA15			
RF_DATA0	61	PB0	PJ0	65	LCD_R1
RF_DATA1	62	PB1	PJ1	66	LCD_R2
RF_DATA2	63	PB2	PJ2	67	LCD_R3
RF_DATA3	192	PB3	PJ3	68	LCD_R4
RF_DATA4	193	PB4	PJ4	69	LCD_R5
RF_DATA5	194	PB5	PJ5	95	LCD_R6
RF_DATA6	195	PB6	PJ6	118	LCD_R7
RF_DATA7	196	PB7	PJ7	119	LCD_G0
RF_DATA8	198	PB8	PJ8	120	LCD_G1
RF_DATA9	199	PB9	PJ9	121	LCD_G2
RF_DATA10	90	PB10	PJ10	122	LCD_G3
RF_DATA11	91	PB11	PJ11	123	LCD_G4
RF_DATA12	104	PB12	PJ12	174	
RF_DATA13	105	PB13	PJ13	175	LCD_B1
RF_DATA14	106	PB14	PJ14	176	LCD_B2
RF_DATA15	107	PB15	PJ15	177	LCD_B3
			PK0	126	LCD_G5
			PK1	127	LCD_G6
			PK2	128	LCD_G7
			PK3	186	LCD_BL_CTRL
			PK4	187	LCD_B5
			PK5	188	LCD_B6
			PK6	189	LCD_B7
			PK7	190	LCD_DE

STM32F746BGT6

ToDo:
- LCD_DISP needed ?
- LCD_INT, move anywhere
- see if MCO1/2 could clock the FPGA/QU/ADC
- I2S port for Codec ?
- free GPIOs for scanned keyboard matrix ?
- I2C port for misc HW ?
- UART TX for debug print
- full USART for ESP8266 ?
- do we need HW spi for simple control ?

- allocate second USB port - not possible, port B taken

Encoders Interface
ENC1_I
ENC1_Q
ENC2_I
ENC2_Q
ENC3_I
ENC3_Q
ENC4_I
ENC4_Q

SDRAM Interface
FMC_A[0..11]
FMC_D[0..31]
FMC_SDNWE
FMC_SDNRAS
FMC_SDNCAS
FMC_SDCLK
FMC_BA0
FMC_BA1
FMC_SDNE0
FMC_SDCKE0
FMC_NBL0
FMC_NBL1

LCD Interface
LCD_R[0..7]
LCD_G[0..7]
LCD_B[0..7]
LCD_BL_CTRL
LCD_HSYNC
LCD_CLK
LCD_VSYNC
LCD_DISP
LCD_DE
LCD_INT

QU Config Interface
QU_PLL_LOCK
QU_CCI_OVFL
QU_TX_ENABLE
QU_PDCLK
QU_CS
QU_CLK
QU_SDIO
QU_IO_UPDATE

candidates, one direction only
no need for MISO
SPI6_SCK
SPI6_MOSI
the rest - any GPIO

ToDo: wire it!

RX/TX Data Bus
RF_DATA[0..15]

FPGA Config Interface
FPGA_CONF_DONE
FPGA_N_STATUS
FPGA_N_CONFIG
FPGA_DCLK
FPGA_DATA0

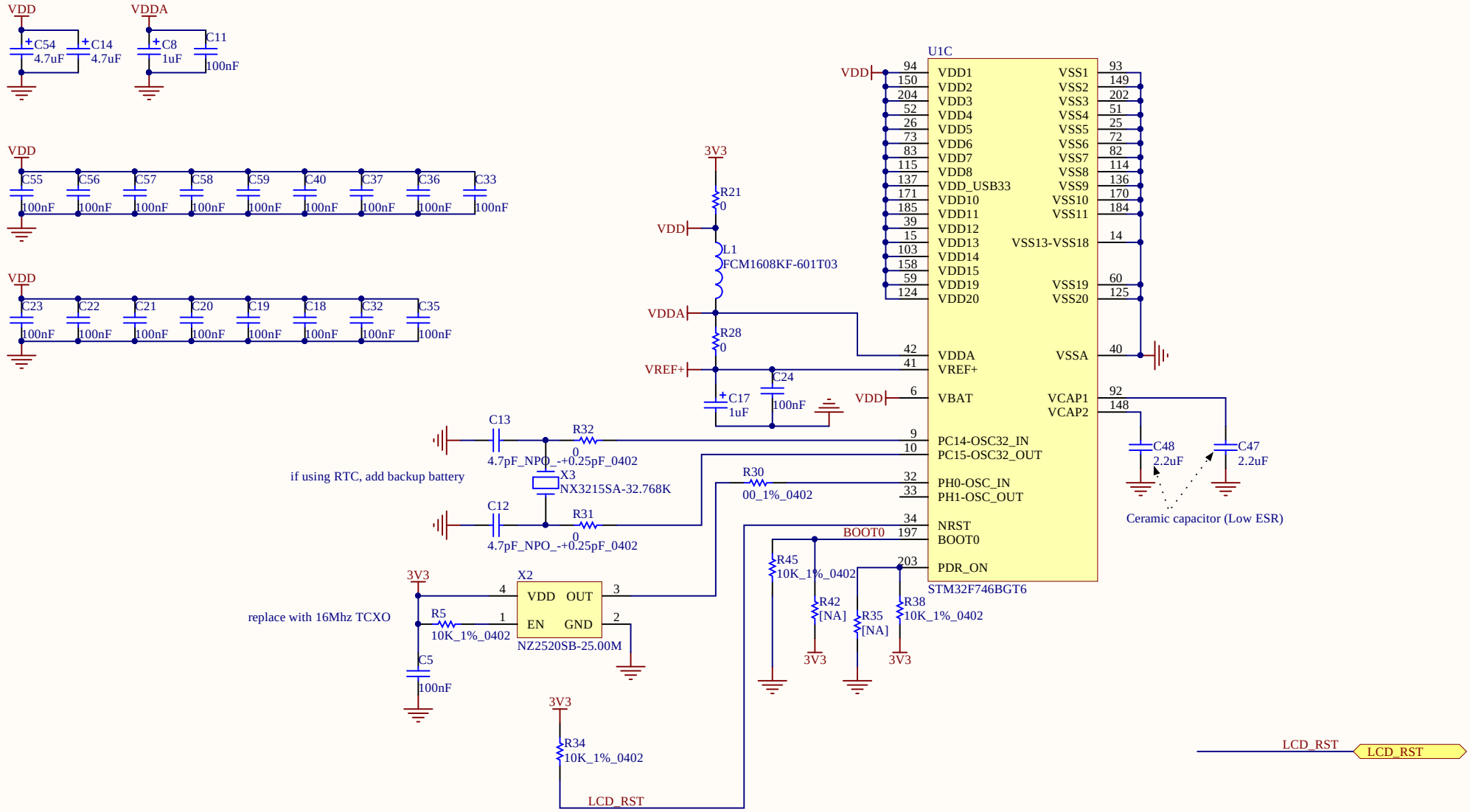
ToDo: wire it!

ADC1
ADC2
ADC3
DAC1
DAC2

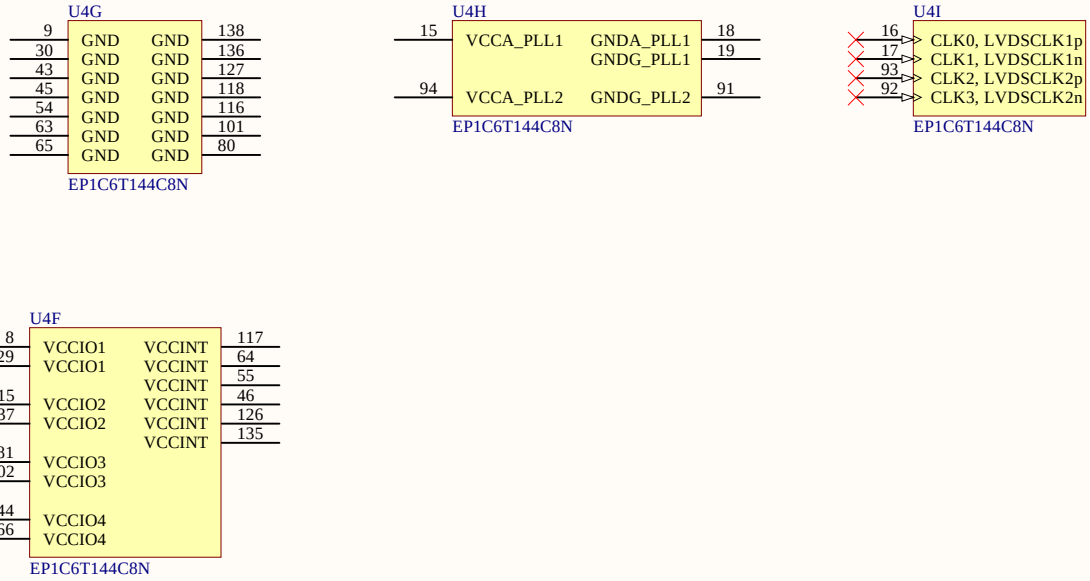
OTG_FS_N
OTG_FS_P

Program Interface
SWDIO
SWCLK

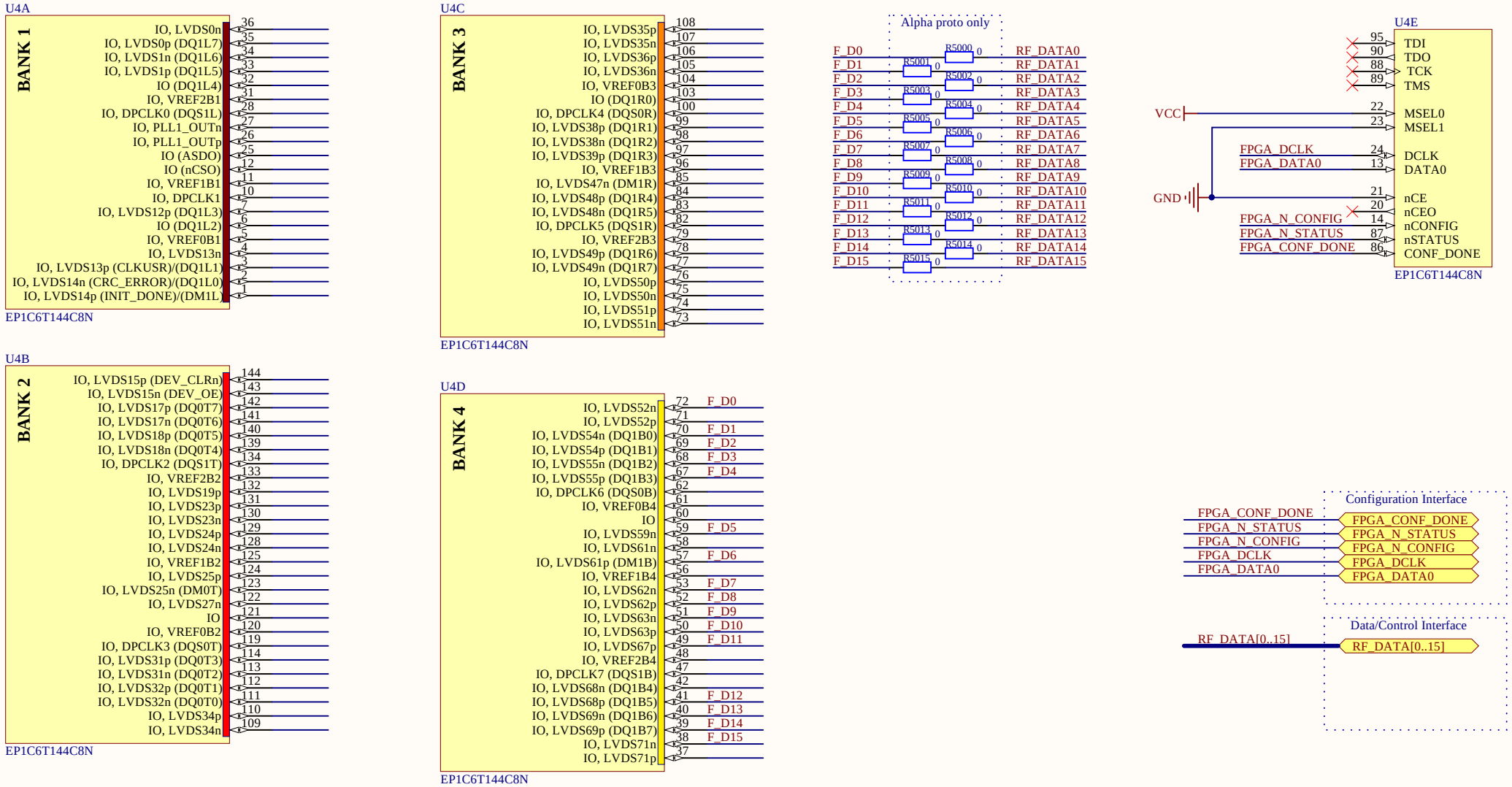
mcHF Pro QRP Transceiver Logic board	STM32 ports usage	*K Atanassov M0NKA*
Date: 09/06/2016 Revision: 0.1	Sheet 2 of 10	
File: C:\Projects\mcHF Pro\pcb\logic\Schematics\logic_cpu_ports.SchDoc		



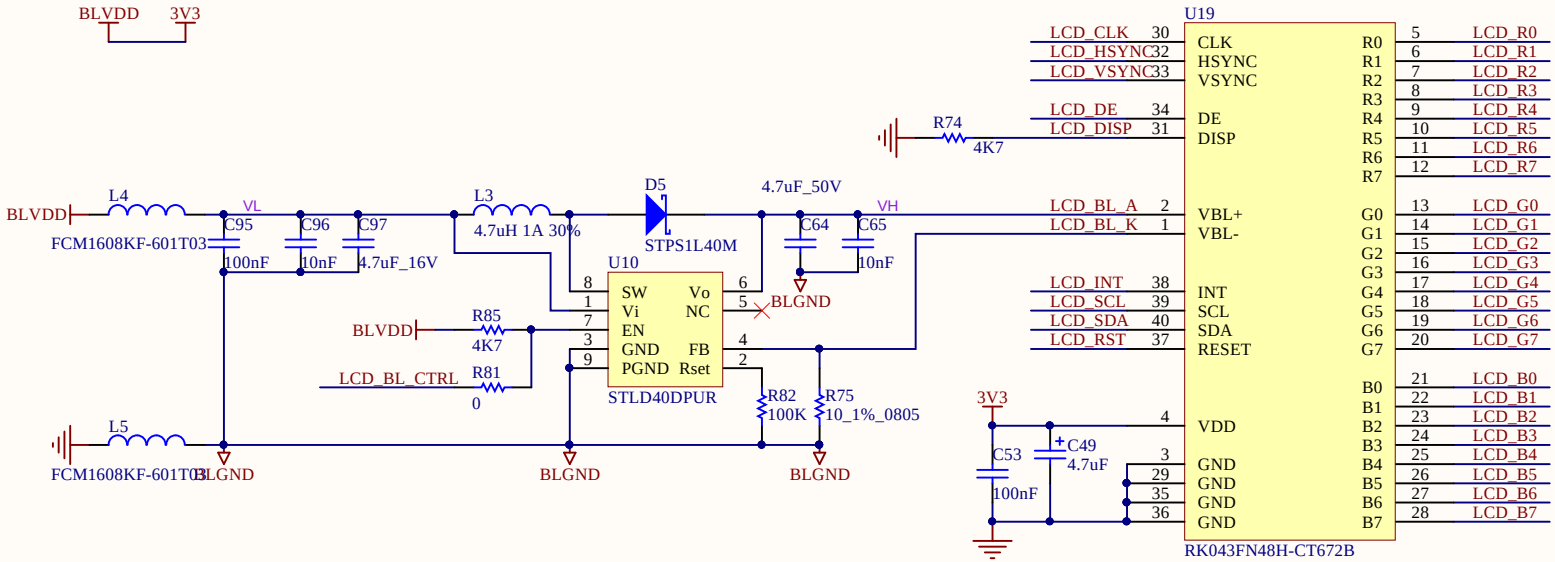
mcHF Pro QRP Transceiver Logic board	STM32 power and clock	*K Atanassov M0NKA*
Date: 09/06/2016 Revision: 0.1	Sheet 3 of 10	
File: C:\Projects\mcHF Pro\pcb\logic\Schematics\logic_cpu_power_and_clocks.SchDoc		



mcHF Pro QRP Transceiver Logic board	FPGA Power	*K Atanassov M0NKA*
Date: 09/06/2016 Revision: 0.1 Sheet 8 of 10		
File: C:\Projects\mcHF Pro\pcb\logic\Schematics\logic_fpga_power.SchDoc		


U4A
BANK 1
IO, LVDS0n
IO, LVDS0p (DQ1L7)
IO, LVDS1n (DQ1L6)
IO, LVDS1p (DQ1L5)
IO (DQ1L4)
IO, VREF2B1
IO, DPCLK0 (DQS1L)
IO, PLL1_OUTn
IO, PLL1_OUTp
IO (ASDO)
IO (nCSO)
IO, VREF1B1
IO, DPCLK1
IO, LVDS12p (DQ1L3)
IO (DQ1L2)
IO, VREF0B1
IO, LVDS13n
IO, LVDS13p (CLKUSR)/(DQ1L1)
IO, LVDS14n (CRC_ERROR)/(DQ1L0)
IO, LVDS14p (INIT_DONE)/(DM1L)
36 35 34 33 32 31 28 27 26 25 12 11 10 7 6 5 4 3 2 1
EP1C6T144C8N
U4B
BANK 2
IO, LVDS15p (DEV_CLRn)
IO, LVDS15n (DEV_OE)
IO, LVDS17p (DQ0T7)
IO, LVDS17n (DQ0T6)
IO, LVDS18p (DQ0T5)
IO, LVDS18n (DQ0T4)
IO, DPCLK2 (DQS1T)
IO, VREF2B2
IO, LVDS19p
IO, LVDS23p
IO, LVDS23n
IO, LVDS24p
IO, LVDS24n
IO, VREF1B2
IO, LVDS25p
IO, LVDS25n (DM0T)
IO, LVDS27n
IO
IO, VREF0B2
IO, DPCLK3 (DQS0T)
IO, LVDS31p (DQ0T3)
IO, LVDS31n (DQ0T2)
IO, LVDS32p (DQ0T1)
IO, LVDS32n (DQ0T0)
IO, LVDS34p
IO, LVDS34n
144 143 142 141 140 139 134 133 132 131 130 129 128 125 124 123 122 121 120 119 114 113 112 111 110 109
EP1C6T144C8N
U4C
BANK 3
IO, LVDS35p
IO, LVDS35n
IO, LVDS36p
IO, LVDS36n
IO, VREF0B3
IO (DQ1R0)
IO, DPCLK4 (DQS0R)
IO, LVDS38p (DQ1R1)
IO, LVDS38n (DQ1R2)
IO, LVDS39p (DQ1R3)
IO, VREF1B3
IO, LVDS47n (DM1R)
IO, LVDS48p (DQ1R4)
IO, LVDS48n (DQ1R5)
IO, DPCLK5 (DQS1R)
IO, VREF2B3
IO, LVDS49p (DQ1R6)
IO, LVDS49n (DQ1R7)
IO, LVDS50p
IO, LVDS50n
IO, LVDS51p
IO, LVDS51n
108 107 106 105 104 103 100 99 98 97 96 85 84 83 82 79 78 77 76 75 74 73
EP1C6T144C8N
U4D
BANK 4
IO, LVDS52n
IO, LVDS52p
IO, LVDS54n (DQ1B0)
IO, LVDS54p (DQ1B1)
IO, LVDS55n (DQ1B2)
IO, LVDS55p (DQ1B3)
IO, DPCLK6 (DQS0B)
IO, VREF0B4
IO
IO, LVDS59n
IO, LVDS61n
IO, LVDS61p (DM1B)
IO, VREF1B4
IO, LVDS62n
IO, LVDS62p
IO, LVDS63n
IO, LVDS63p
IO, LVDS67p
IO, VREF2B4
IO, DPCLK7 (DQS1B)
IO, LVDS68n (DQ1B4)
IO, LVDS68p (DQ1B5)
IO, LVDS69n (DQ1B6)
IO, LVDS69p (DQ1B7)
IO, LVDS71n
IO, LVDS71p
72 F_D0
71
70 F_D1
69 F_D2
68 F_D3
67 F_D4
62
61
60
59 F_D5
58
57 F_D6
56
53 F_D7
52 F_D8
51 F_D9
50 F_D10
49 F_D11
48
47
42
41 F_D12
40 F_D13
39 F_D14
38 F_D15
37
EP1C6T144C8N
Alpha proto only
F_D0 R5000 0 RF_DATA0
F_D1 R5001 0 RF_DATA1
F_D2 R5002 0 RF_DATA2
F_D3 R5003 0 RF_DATA3
F_D4 R5004 0 RF_DATA4
F_D5 R5005 0 RF_DATA5
F_D6 R5006 0 RF_DATA6
F_D7 R5007 0 RF_DATA7
F_D8 R5008 0 RF_DATA8
F_D9 R5009 0 RF_DATA9
F_D10 R5010 0 RF_DATA10
F_D11 R5011 0 RF_DATA11
F_D12 R5012 0 RF_DATA12
F_D13 R5013 0 RF_DATA13
F_D14 R5014 0 RF_DATA14
F_D15 R5015 0 RF_DATA15
U4E
TDI 95
TDO 90
TCK 88
TMS 89
VCC
MSEL0 22
MSEL1 23
FPGA_DCLK
DCLK 24
FPGA_DATA0
DATA0 13
GND
nCE 21
nCEO 20
FPGA_N_CONFIG
nCONFIG 14
FPGA_N_STATUS
nSTATUS 87
FPGA_CONF_DONE
CONF_DONE 86
EP1C6T144C8N
Configuration Interface
FPGA_CONF_DONE
FPGA_N_STATUS
FPGA_N_CONFIG
FPGA_DCLK
FPGA_DATA0
Data/Control Interface
RF_DATA[0..15]
mcHF Pro QRP Transceiver Logic board
FPGA Data and Control
K Atanassov
M0NKA
Date: 09/06/2016 Revision: 0.1
Sheet 9 of 10
File: C:\Projects\mcHF Pro\pcb\logic\Schematics\logic_fpga_signal.SchDoc

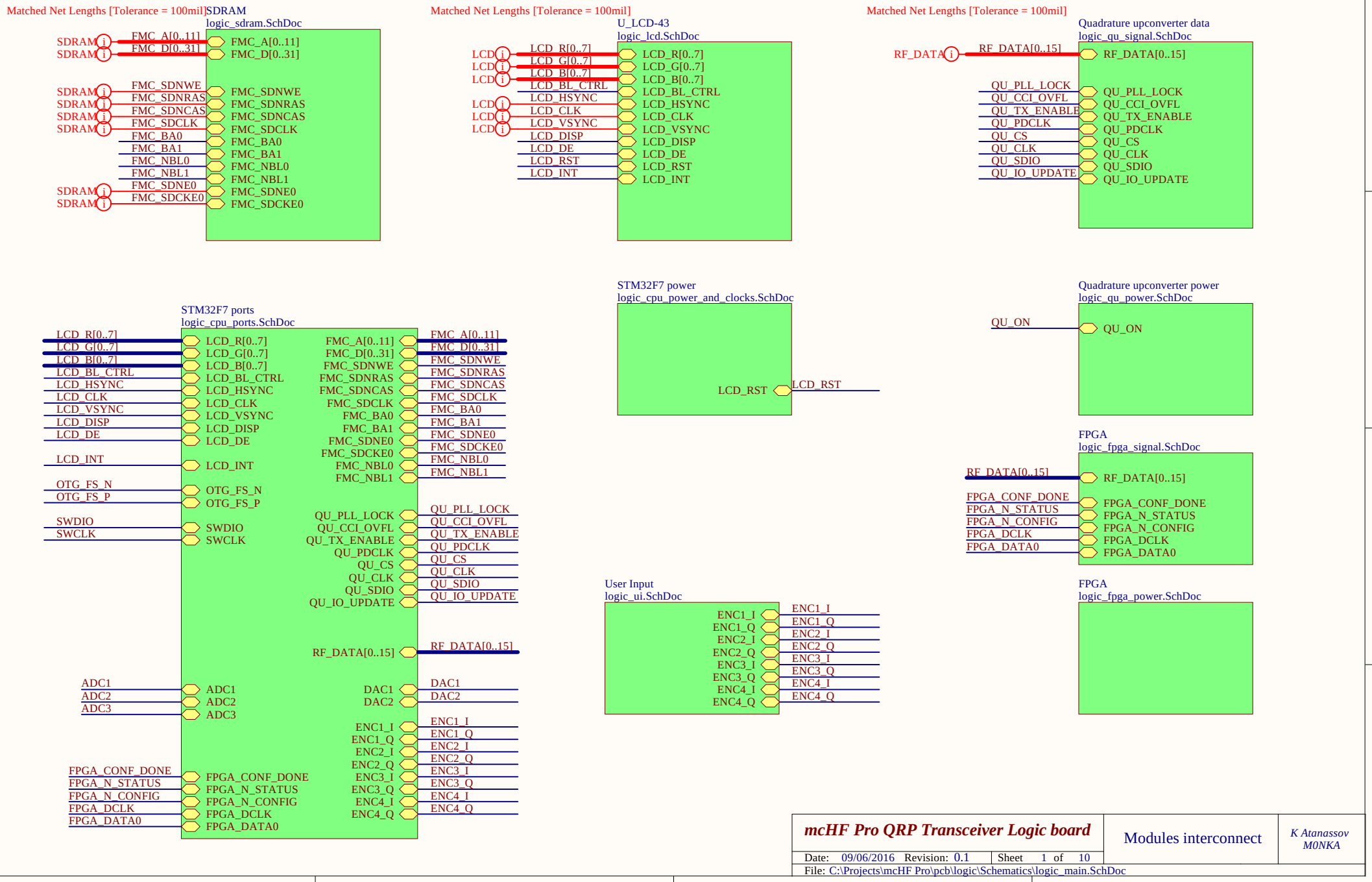
need complete rework for 5 inch LCD

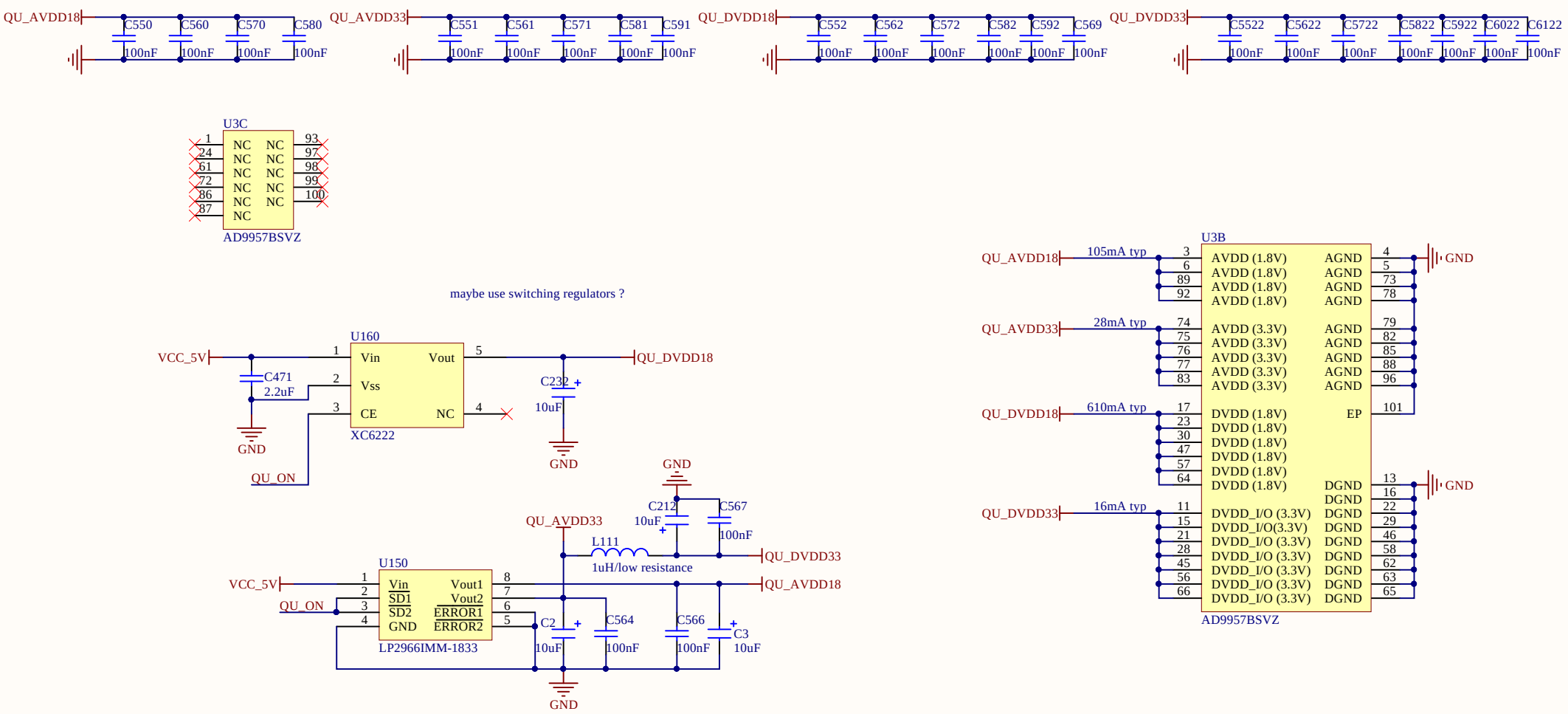


ToDo: Draw footprint

LCD_G[0..7]
LCD_B[0..7]
LCD_R[0..7]
LCD_BL_CTRL
LCD_CLK
LCD_HSYNC
LCD_VSYNC
LCD_DE
LCD_DISP
LCD_INT
LCD_RST

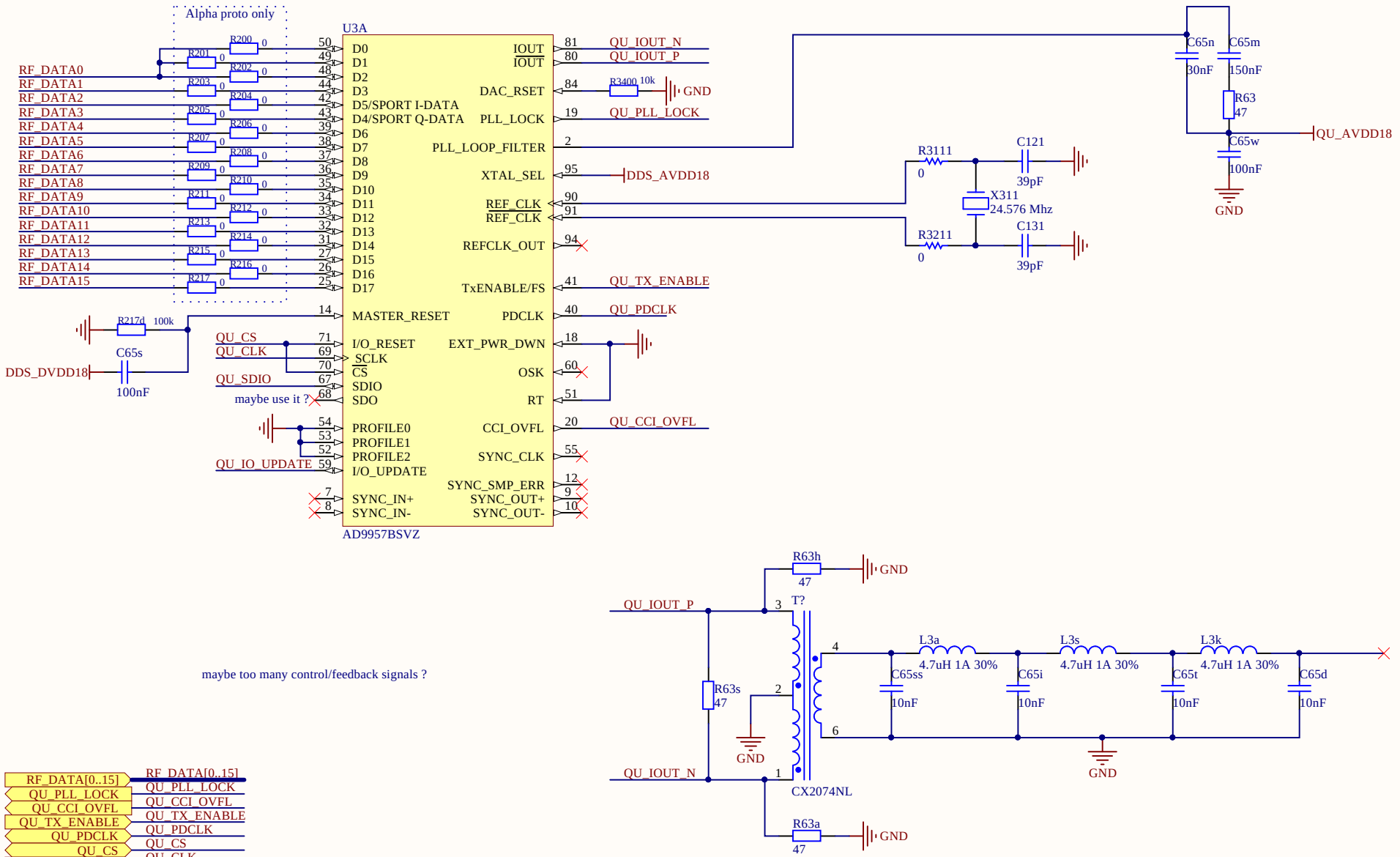
mcHF Pro QRP Transceiver Logic board	LCD	*K Atanassov M0NKA*
Date: 09/06/2016 Revision: 0.1	Sheet 5 of 10	
File: C:\Projects\mcHF Pro\pcb\logic\Schematics\logic_lcd.SchDoc		


Matched Net Lengths [Tolerance = 100mil]
SDRAM
logic_sdram.SchDoc
FMC_A[0..11]
FMC_D[0..31]
FMC_SDNWE
FMC_SDNRAS
FMC_SDNCAS
FMC_SDCLK
FMC_BA0
FMC_BA1
FMC_NBL0
FMC_NBL1
FMC_SDNE0
FMC_SDCKE0
Matched Net Lengths [Tolerance = 100mil]
U_LCD-43
logic_lcd.SchDoc
LCD_R[0..7]
LCD_G[0..7]
LCD_B[0..7]
LCD_BL_CTRL
LCD_HSYNC
LCD_CLK
LCD_VSYNC
LCD_DISP
LCD_DE
LCD_RST
LCD_INT
Matched Net Lengths [Tolerance = 100mil]
Quadrature upconverter data
logic_qu_signal.SchDoc
RF_DATA[0..15]
QU_PLL_LOCK
QU_CCI_OVFL
QU_TX_ENABLE
QU_PDCLK
QU_CS
QU_CLK
QU_SDIO
QU_IO_UPDATE
STM32F7 ports
logic_cpu_ports.SchDoc
LCD_R[0..7]
LCD_G[0..7]
LCD_B[0..7]
LCD_BL_CTRL
LCD_HSYNC
LCD_CLK
LCD_VSYNC
LCD_DISP
LCD_DE
LCD_INT
OTG_FS_N
OTG_FS_P
SWDIO
SWCLK
FMC_A[0..11]
FMC_D[0..31]
FMC_SDNWE
FMC_SDNRAS
FMC_SDNCAS
FMC_SDCLK
FMC_BA0
FMC_BA1
FMC_SDNE0
FMC_SDCKE0
FMC_NBL0
FMC_NBL1
QU_PLL_LOCK
QU_CCI_OVFL
QU_TX_ENABLE
QU_PDCLK
QU_CS
QU_CLK
QU_SDIO
QU_IO_UPDATE
RF_DATA[0..15]
ADC1
ADC2
ADC3
DAC1
DAC2
ENC1_I
ENC1_Q
ENC2_I
ENC2_Q
ENC3_I
ENC3_Q
ENC4_I
ENC4_Q
FPGA_CONF_DONE
FPGA_N_STATUS
FPGA_N_CONFIG
FPGA_DCLK
FPGA_DATA0
STM32F7 power
logic_cpu_power_and_clocks.SchDoc
LCD_RST
Quadrature upconverter power
logic_qu_power.SchDoc
QU_ON
FPGA
logic_fpga_signal.SchDoc
RF_DATA[0..15]
FPGA_CONF_DONE
FPGA_N_STATUS
FPGA_N_CONFIG
FPGA_DCLK
FPGA_DATA0
User Input
logic_ui.SchDoc
ENC1_I
ENC1_Q
ENC2_I
ENC2_Q
ENC3_I
ENC3_Q
ENC4_I
ENC4_Q
FPGA
logic_fpga_power.SchDoc
mcHF Pro QRP Transceiver Logic board
Modules interconnect
K Atanassov
M0NKA
Date: 09/06/2016 Revision: 0.1
Sheet 1 of 10
File: C:\Projects\mcHF Pro\pcb\logic\Schematics\logic_main.SchDoc

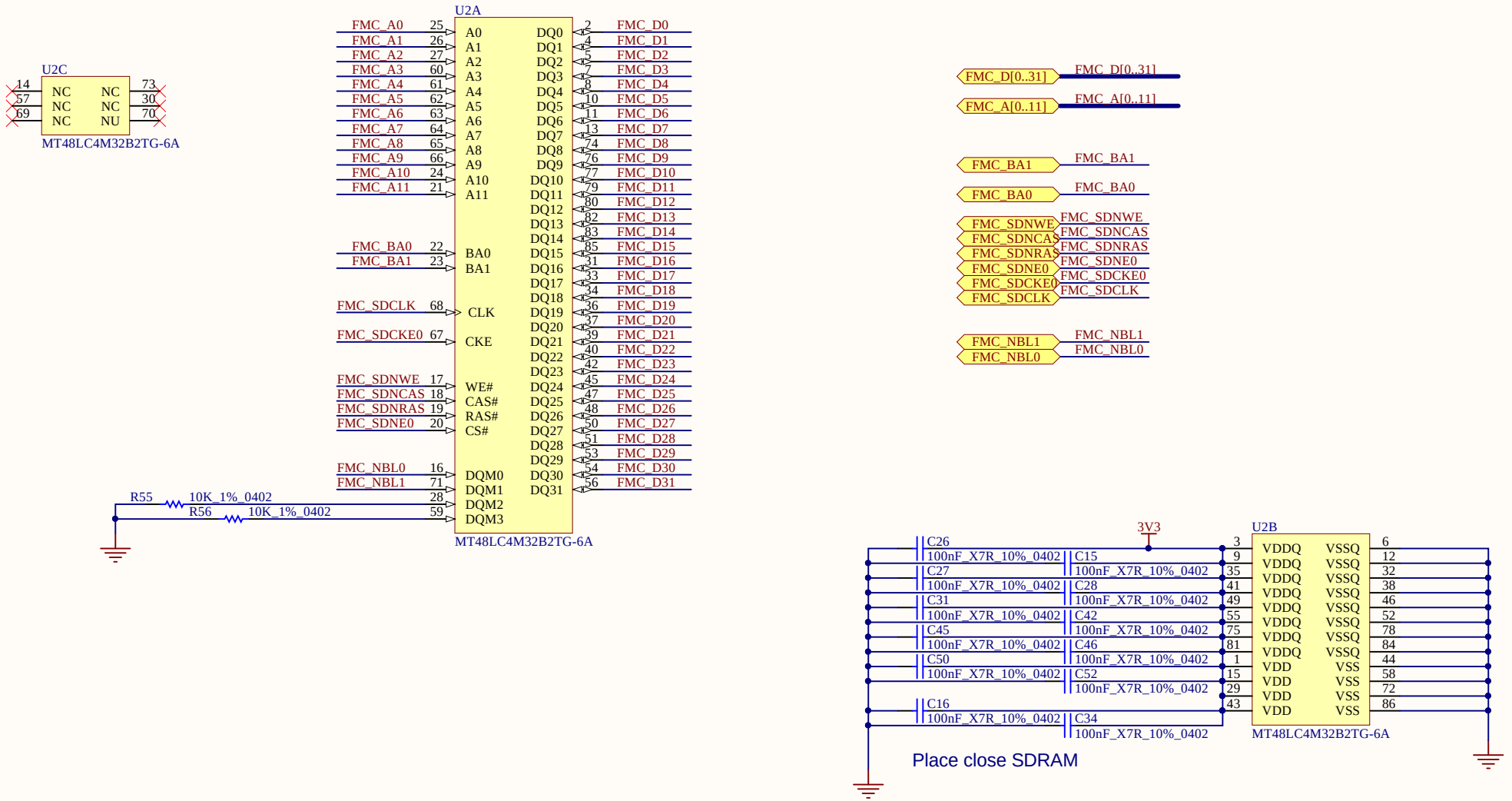


QU_ON QU_ON

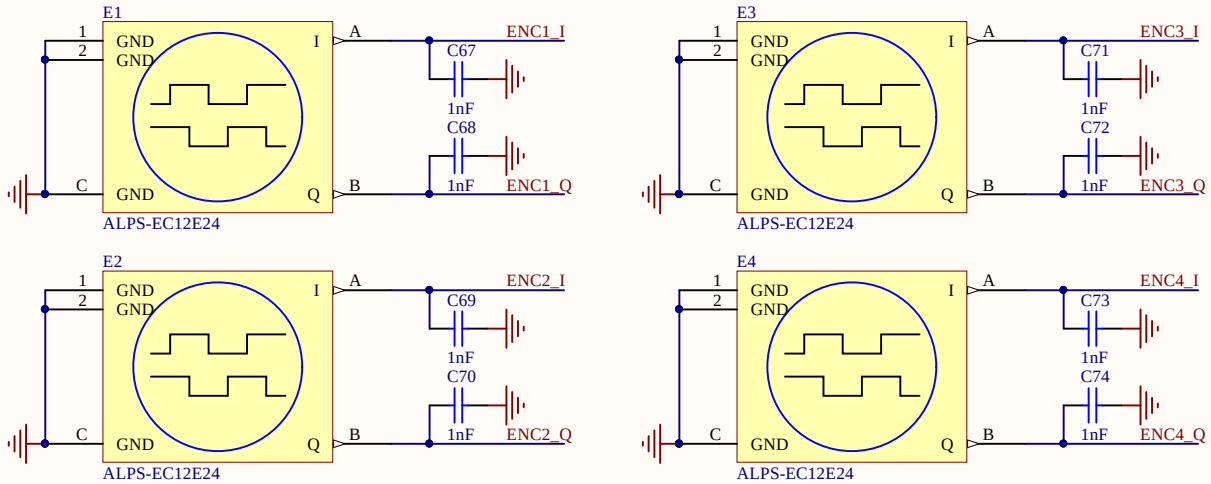
mcHF Pro QRP Transceiver Logic board	Quadrature Upconverter Power	*K Atanassov M0NKA*
Date: 09/06/2016 Revision: 0.1	Sheet 7 of 10	
File: C:\Projects\mcHF Pro\pcb\logic\Schematics\logic_qu_power.SchDoc		

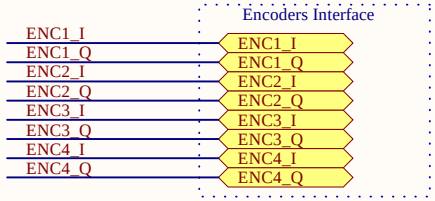


mcHF Pro QRP Transceiver Logic board	Quadrature Upconverter Data and Output	*K Atanassov M0NKA*
Date: 09/06/2016 Revision: 0.1	Sheet 6 of 10	
File: C:\Projects\mcHF Pro\pcb\logic\Schematics\logic_qu_signal.SchDoc		



mcHF Pro QRP Transceiver Logic board	SDRAM	*K Atanassov M0NKA*
Date: 09/06/2016 Revision: 0.1	Sheet 4 of 10	
File: C:\Projects\mcHF Pro\pcb\logic\Schematics\logic_sdram.SchDoc		





mcHF Pro QRP Transceiver Logic board	User Interface	*K Atanassov M0NKA*
Date: 09/06/2016 Revision: 0.1	Sheet 10 of 10	
File: C:\Projects\mcHF Pro\pcb\logic\Schematics\logic_ui.SchDoc		