1. Description

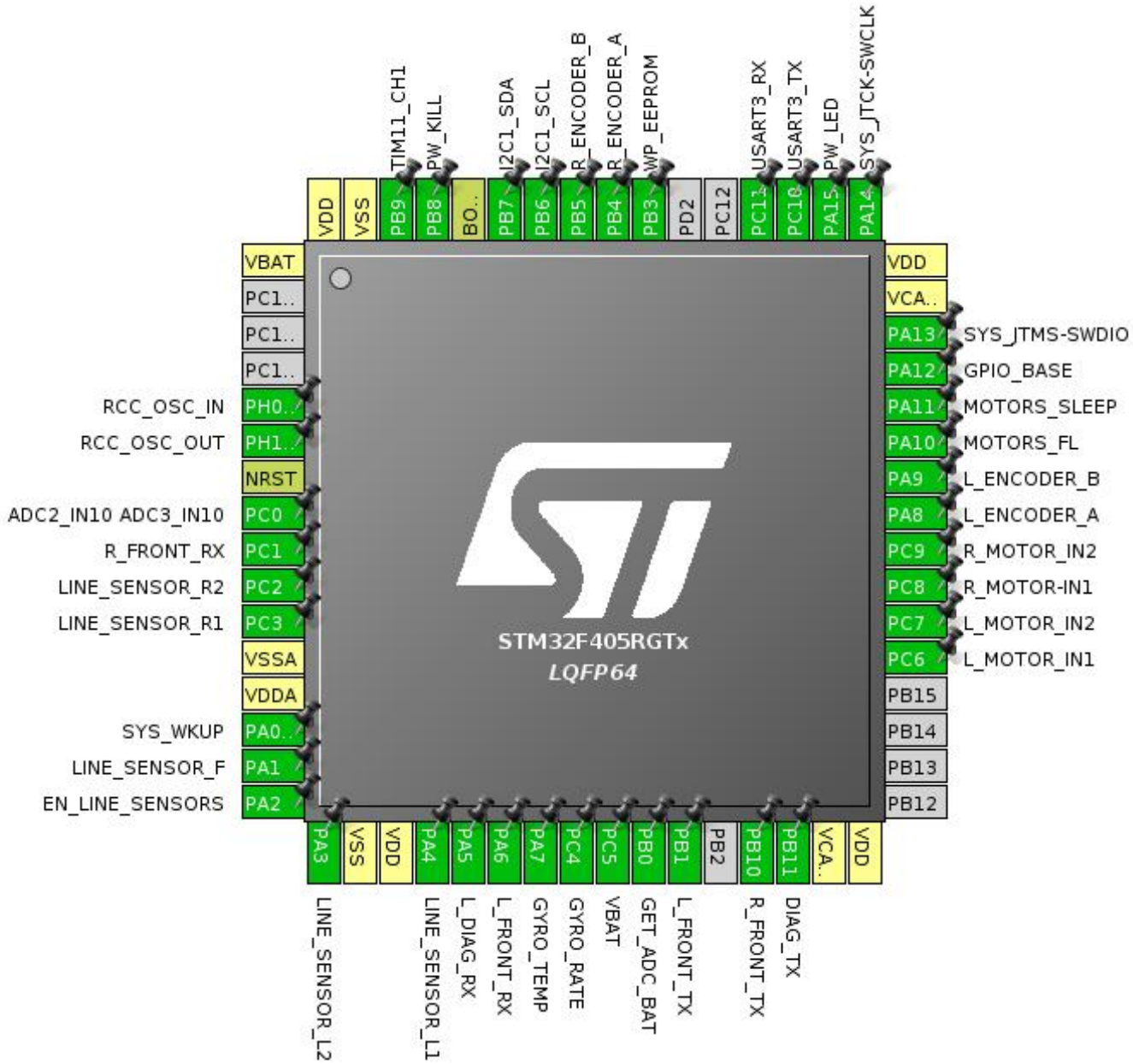
1.1. Project

Project Name	ZHONX_III
Board Name	No information
Generated with:	STM32CubeMX 4.9.0
Date	07/19/2015

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F405/415
MCU name	STM32F405RGTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0	I/O	ADC2_IN10, ADC3_IN10	
9	PC1	I/O	ADC2_IN11	R_FRONT_RX
10	PC2	I/O	ADC3_IN12	LINE_SENSOR_R2
11	PC3	I/O	ADC2_IN13	LINE_SENSOR_R1
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	SYS_WKUP	
15	PA1	I/O	ADC3_IN1	LINE_SENSOR_F
16	PA2 *	I/O	GPIO_Output	EN_LINE_SENSORS
17	PA3	I/O	ADC3_IN3	LINE_SENSOR_L2
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC2_IN4	LINE_SENSOR_L1
21	PA5	I/O	ADC2_IN5	L_DIAG_RX
22	PA6	I/O	ADC2_IN6	L_FRONT_RX
23	PA7	I/O	ADC1_IN7	GYRO_TEMP
24	PC4	I/O	ADC1_IN14	GYRO_RATE
25	PC5	I/O	ADC1_IN15	VBAT
26	PB0 *	I/O	GPIO_Output	GET_ADC_BAT
27	PB1 *	I/O	GPIO_Output	L_FRONT_TX
29	PB10 *	I/O	GPIO_Output	R_FRONT_TX
30	PB11 *	I/O	GPIO_Output	DIAG_TX
31	VCAP_1	Power		
32	VDD	Power		
37	PC6	I/O	TIM8_CH1	L_MOTOR_IN1
38	PC7	I/O	TIM8_CH2	L_MOTOR_IN2
39	PC8	I/O	TIM8_CH3	R_MOTOR-IN1
40	PC9	I/O	TIM8_CH4	R_MOTOR_IN2
41	PA8	I/O	TIM1_CH1	L_ENCODER_A
42	PA9	I/O	TIM1_CH2	L_ENCODER_B
43	PA10 *	I/O	GPIO_Input	MOTORS_FL
44	PA11 *	I/O	GPIO_Output	MOTORS_SLEEP

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
45	PA12 *	I/O	GPIO_Input	GPIO_BASE
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VCAP_2	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
50	PA15 *	I/O	GPIO_Output	PW_LED
51	PC10	I/O	USART3_TX	
52	PC11	I/O	USART3_RX	
55	PB3 *	I/O	GPIO_Output	WP_EEPROM
56	PB4	I/O	TIM3_CH1	R_ENCODER_A
57	PB5	I/O	TIM3_CH2	R_ENCODER_B
58	PB6	I/O	I2C1_SCL	
59	PB7	I/O	I2C1_SDA	
60	BOOT0	Boot		
61	PB8 *	I/O	GPIO_Input	PW_KILL
62	PB9	I/O	TIM11_CH1	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. IPs and Middleware Configuration

4.1. ADC1

mode: IN7

mode: IN14

mode: IN15

mode: Temperature Sensor Channel

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	**Enabled ***
Number Of Discontinuous Conversions	**3 ***
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADCgroup:

Number Of Conversion	**3 ***
External Trigger Conversion Edge	**Trigger detection on the rising edge ***
External Trigger Conversion Source	**Timer 4 Capture Compare 4 event ***
Number Of Conversions	**1 ***
External Trigger Edge	**Trigger detection on the rising edge ***
External Trigger Source	**Timer 5 Trigger Out event ***
Number Of Conversion	**3 ***
External Trigger Conversion Edge	**Trigger detection on the rising edge ***
External Trigger Conversion Source	**Timer 4 Capture Compare 4 event ***
Number Of Conversion	**3 ***
External Trigger Conversion Edge	**Trigger detection on the rising edge ***
External Trigger Conversion Source	**Timer 4 Capture Compare 4 event ***
Number Of Conversion	**3 ***
External Trigger Conversion Edge	**Trigger detection on the rising edge ***

External Trigger Conversion Source	**Timer 4 Capture Compare 4 event ***
Number Of Conversions	**1 ***
External Trigger Edge	**Trigger detection on the rising edge ***
External Trigger Source	**Timer 5 Trigger Out event ***
Number Of Conversion	**3 ***
External Trigger Conversion Edge	**Trigger detection on the rising edge ***
External Trigger Conversion Source	**Timer 4 Capture Compare 4 event ***
Injected Conversion Mode	None
Injected Conversion Mode	None

WatchDog:

Enable Analog WatchDog Mode	false

ADC_Regular_ConversionMode:

Rank	1
Channel	**Channel 7 ***
Sampling Time	**28 Cycles ***
Rank	**3 ***
Channel	**Channel 15 ***
Sampling Time	**28 Cycles ***
Rank	**2 ***
Channel	**Channel Temperature Sensor ***
Sampling Time	**28 Cycles ***
Rank	1
Channel	**Channel 7 ***
Sampling Time	**28 Cycles ***

ADC_Injected_ConversionMode:

Rank	1
Channel	**Channel 14 ***
Sampling Time	3 Cycles
Injected Offset	0

4.2. ADC2

mode: IN4

mode: IN5

mode: IN6

mode: IN10

mode: IN11

mode: IN13

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADCgroup:

Number Of Conversion	1
External Trigger Conversion Edge	None
Number Of Conversions	0
Number Of Conversions	0
Number Of Conversions	0
Number Of Conversions	0
Number Of Conversion	1
External Trigger Conversion Edge	None
Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

ADC_Injected_ConversionMode:

Rank	**2 ***
Channel	**Channel 13 ***
Sampling Time	**15 Cycles ***
Injected Offset	0
Rank	**2 ***
Channel	**Channel 11 ***
Sampling Time	**15 Cycles ***
Injected Offset	0
Rank	1
Channel	**Channel 4 ***
Sampling Time	**15 Cycles ***
Injected Offset	0

Rank	1
Channel	**Channel 4 ***
Sampling Time	**15 Cycles ***
Injected Offset	0

ADC_Regular_ConversionMode:

Rank	1
Channel	**Channel 6 ***
Sampling Time	**144 Cycles ***

4.3. ADC3

mode: IN1

mode: IN3

mode: IN10

mode: IN12

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADCgroup:

Number Of Conversion	**3 ***
External Trigger Conversion Edge	None
Number Of Conversions	0
Number Of Conversions	0
Number Of Conversions	0
Number Of Conversion	**3 ***
External Trigger Conversion Edge	None
Number Of Conversion	**3 ***
External Trigger Conversion Edge	None
Number Of Conversions	0
Number Of Conversion	**3 ***

External Trigger Conversion Edge	None

WatchDog:

Enable Analog WatchDog Mode	false

ADC_Injected_ConversionMode:

Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	**15 Cycles ***
Injected Offset	0
Rank	1
Channel	**Channel 3 ***
Sampling Time	**15 Cycles ***
Injected Offset	0
Rank	**3 ***
Channel	**Channel 10 ***
Sampling Time	**15 Cycles ***
Injected Offset	0

ADC_Regular_ConversionMode:

Rank	**3 ***
Channel	**Channel 10 ***
Sampling Time	**28 Cycles ***
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	**15 Cycles ***
Rank	1
Channel	**Channel 3 ***
Sampling Time	**15 Cycles ***

4.4. I2C1

I2C: I2C

Master Features:

I2C Speed Mode	**Fast Mode ***
I2C Clock Speed (Hz)	400000
Fast Mode Duty Cycle	Duty cycle Tlow/Thigh = 2

Slave Features:

Clock No Stretch Mode	**Enabled ***

Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	**Enabled ***

4.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

4.6. RNG

mode: Activated

4.7. RTC

WakeUp: Internal WakeUp

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Wake UP:

Wake Up Clock	RTCCLK / 16
Wake Up Counter	0

4.8. SYS

Debug: Serial Wire Debug (SWD)

mode: System Wake-Up

4.9. TIM1

Combined Channels: Encoder Mode

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2047 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	**Division by 8 ***
Input Filter	**3 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	**Division by 8 ***
Input Filter	**3 ***

4.10. TIM2

Clock Source : Internal Clock

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up

Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

4.11. TIM3

Combined Channels: Encoder Mode

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2047 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	**Division by 8 ***
Input Filter	**3 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	**Division by 8 ***
Input Filter	**3 ***

4.12. TIM4

mode: Clock Source

Counter Settings:

Prescaler (PSC - 16 bits value)	**1800 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10 ***

Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

4.13. TIM5

mode: Clock Source

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

4.14. TIM6

mode: Activated

Counter Settings:

Prescaler (PSC - 16 bits value)	**60000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

4.15. TIM7

mode: Activated

Counter Settings:

Prescaler (PSC - 16 bits value)	**60000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

4.16. TIM8

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: Output Compare CH3

Channel4: PWM Generation CH4

Counter Settings:

Prescaler (PSC - 16 bits value)	**4 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	**Low ***

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

Output Compare Channel 3:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	**500 ***
Fast Mode	**Enable ***
CH Polarity	**Low ***
CH Idle State	**Set ***

4.17. TIM10

mode: Activated

Counter Settings:

Prescaler (PSC - 16 bits value)	**60000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10 ***
Internal Clock Division (CKD)	No Division

4.18. TIM11

mode: Activated

Channel1: PWM Generation CH1

Counter Settings:

Prescaler (PSC - 16 bits value)	**10000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100 ***
Internal Clock Division (CKD)	No Division

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**50 ***
Fast Mode	Disable
CH Polarity	**Low ***

4.19. USART3

Mode: Asynchronous

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

* User modified value

5. System Configuration

5.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA7	ADC1_IN7	Analog mode	No pull-up and no pull-down	n/a	GYRO_TEMP
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	GYRO_RATE
	PC5	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	VBAT
ADC2	PC0	ADC2_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PC1	ADC2_IN11	Analog mode	No pull-up and no pull-down	n/a	R_FRONT_RX
	PC3	ADC2_IN13	Analog mode	No pull-up and no pull-down	n/a	LINE_SENSOR_R1
	PA4	ADC2_IN4	Analog mode	No pull-up and no pull-down	n/a	LINE_SENSOR_L1
	PA5	ADC2_IN5	Analog mode	No pull-up and no pull-down	n/a	L_DIAG_RX
	PA6	ADC2_IN6	Analog mode	No pull-up and no pull-down	n/a	L_FRONT_RX
ADC3	PC0	ADC3_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PC2	ADC3_IN12	Analog mode	No pull-up and no pull-down	n/a	LINE_SENSOR_R2
	PA1	ADC3_IN1	Analog mode	No pull-up and no pull-down	n/a	LINE_SENSOR_F
	PA3	ADC3_IN3	Analog mode	No pull-up and no pull-down	n/a	LINE_SENSOR_L2
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Fast ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Fast ***	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA0-WKUP	SYS_WKUP	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	L_ENCODER_A
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	L_ENCODER_B
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	R_ENCODER_A
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	R_ENCODER_B
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	**Fast ***	L_MOTOR_IN1
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	L_MOTOR_IN2
	PC8	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	R_MOTOR-IN1
	PC9	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	**Fast ***	R_MOTOR_IN2
TIM11	PB9	TIM11_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
USART3	PC10	USART3_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PC11	USART3_RX	Alternate Function Push Pull	Pull-up	**High ***	
GPIO	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EN_LINE_SENSORS
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GET_ADC_BAT
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	L_FRONT_TX
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	R_FRONT_TX
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	DIAG_TX
	PA10	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	MOTORS_FL
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTORS_SLEEP
	PA12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPIO_BASE
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PW_LED
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WP_EEPROM
	PB8	GPIO_Input	Input mode	**Pull-up ***	n/a	PW_KILL

5.2. DMA configuration

DMA request	Stream	Direction	Priority
I2C1_TX	DMA1_Stream6	Memory To Peripheral	**Medium ***
I2C1_RX	DMA1_Stream5	Peripheral To Memory	**Medium ***
USART3_RX	DMA1_Stream1	Peripheral To Memory	Low
USART3_TX	DMA1_Stream3	Memory To Peripheral	Low
ADC1	DMA2_Stream0	Peripheral To Memory	Low

I2C1_TX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
PeripheralIncrement:	Disable
MemoryIncrement:	**Enable ***
Peripheral Data Width:	Byte

I2C1_RX: DMA1_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
PeripheralIncrement:	Disable
MemoryIncrement:	**Enable ***
Peripheral Data Width:	Byte

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
PeripheralIncrement:	Disable
MemoryIncrement:	**Enable ***
Peripheral Data Width:	Byte

USART3_TX: DMA1_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
PeripheralIncrement:	Disable

MemoryIncrement:	**Enable ***
Peripheral Data Width:	Byte

ADC1: DMA2_Stream0 DMA request Settings:

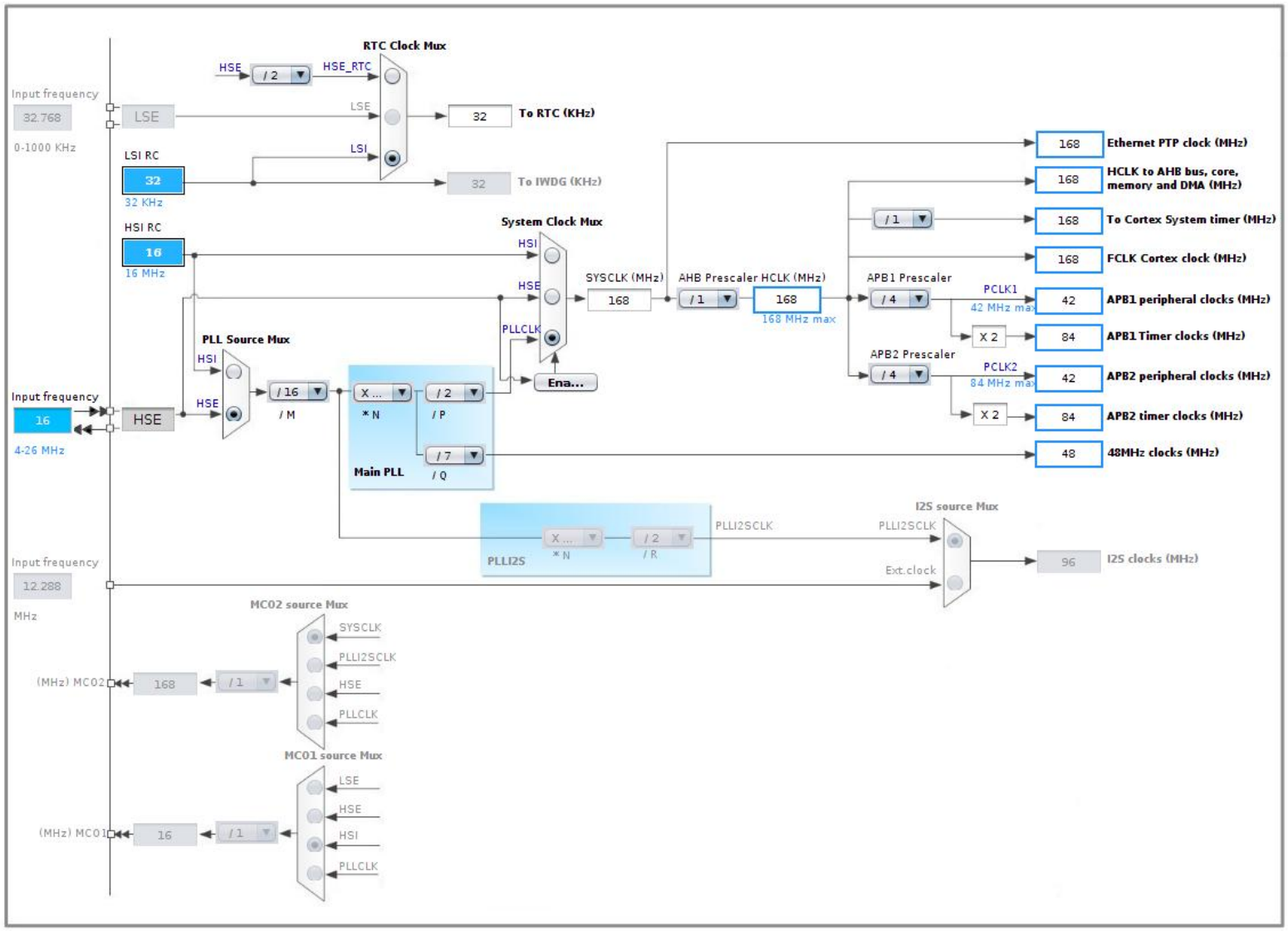
Mode:	**Circular ***
Use fifo:	Disable
PeripheralIncrement:	Disable
MemoryIncrement:	**Enable ***
Peripheral Data Width:	**Half Word ***

5.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	0	0
RTC Wakeup interrupt through the EXTI Line22 interrupt	true	0	0
RCC global interrupt	true	0	0
DMA1 Stream1 global interrupt	true	0	0
DMA1 Stream3 global interrupt	true	0	0
DMA1 Stream5 global interrupt	true	0	7
DMA1 Stream6 global interrupt	true	0	7
ADC1, ADC2 and ADC3 global interrupts	true	0	5
TIM1 Update interrupt and TIM10 global interrupt	true	0	3
TIM2 global interrupt	true	0	2
TIM3 global interrupt	true	0	3
TIM4 global interrupt	true	0	7
USART3 global interrupt	true	1	6
TIM5 global interrupt	true	0	1
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	7
TIM7 global interrupt	true	0	4
DMA2 Stream0 global interrupt	true	0	7
Non Maskable Interrupt	unused		
Memory management fault	unused		
Pre-fetch fault, memory access fault	unused		
Undefined instruction or illegal state	unused		
Debug Monitor	unused		
TIM1 Break interrupt and TIM9 global interrupt	unused		
TIM1 Trigger and Commutation interrupts and TIM11 global interrupt	unused		
TIM1 Capture Compare interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
TIM8 Break interrupt and TIM12 global interrupt	unused		
TIM8 Update interrupt and TIM13 global interrupt	unused		
TIM8 Trigger and Commutation interrupts and TIM14 global interrupt	unused		
TIM8 Capture Compare interrupt	unused		
HASH and RNG global interrupt	unused		

*** User modified value**

6. Clock Tree Configuration



7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F405/415
MCU	STM32F405RGTx
Datasheet	022152_Rev5

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	ZHONX_III
Project Folder	/home/zhonx/workspace/ZHONX_III/CubeMX
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F4 V1.7.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

8.3. Toolchains Settings

Name	Value
Compiler Optimizations	Balanced Size/Speed