Table 1: Slices and delay for Adder

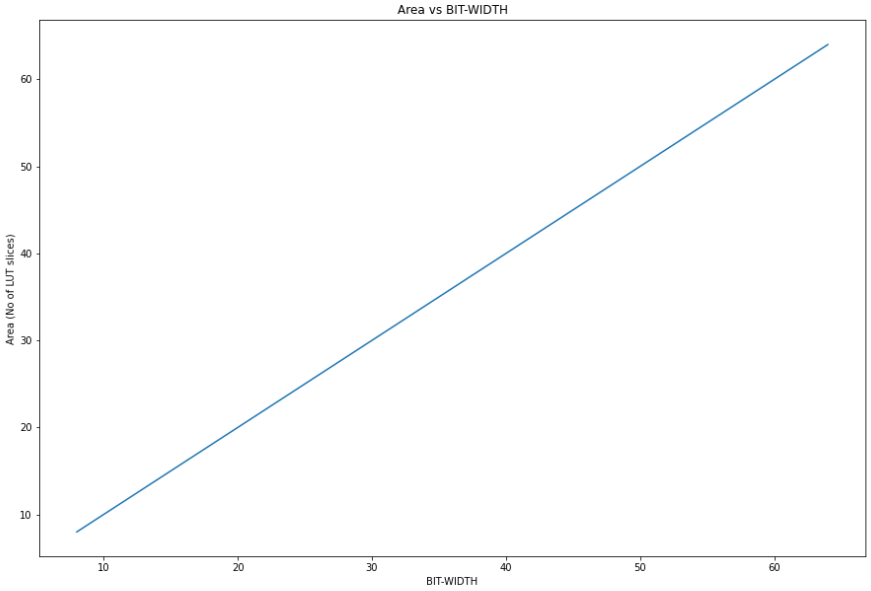
Parameter: **DSIZE**	BIT-WIDTH	No of LUT slices	Delay in ns
8	8	8	5.725
16	16	16	5.877
32	32	32	6.181
64	64	64	6.789

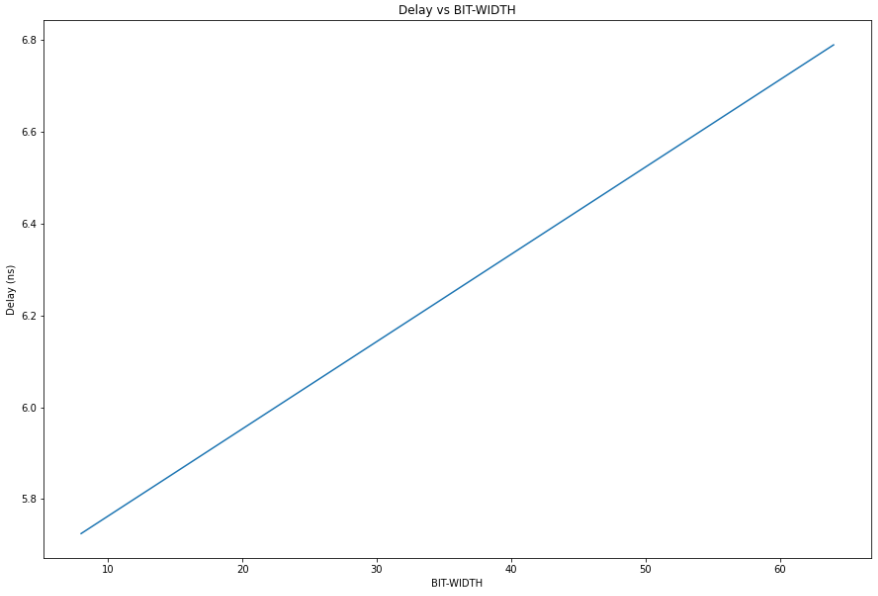
Table 2: Slices and delay for Multiplier

Parameter: **DSIZE**	BIT-WIDTH	No of LUT slices	Delay in ns
8	8	41	8.550
16	16	177	9.955
32	32	737	11.780
64	64	3009	13.845

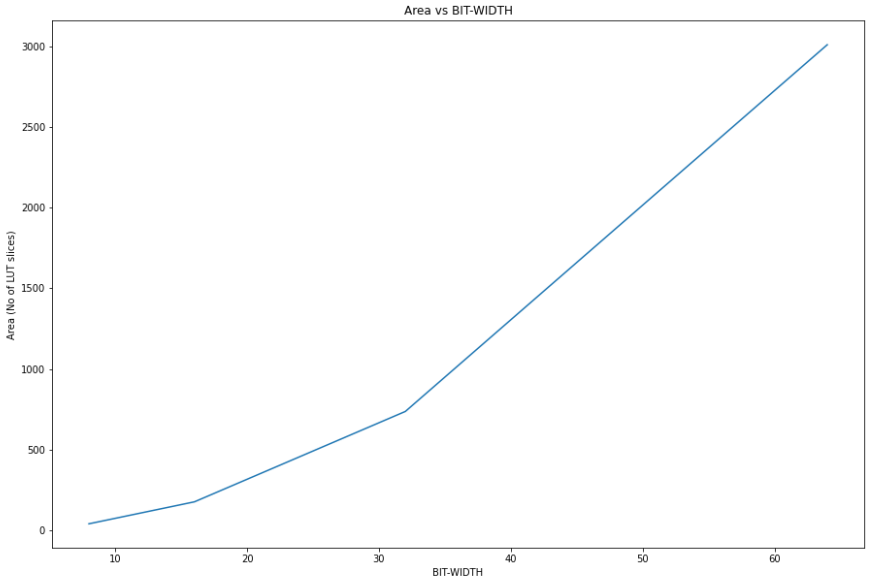
Evaluation 1

Adder Module





Multiplier Module



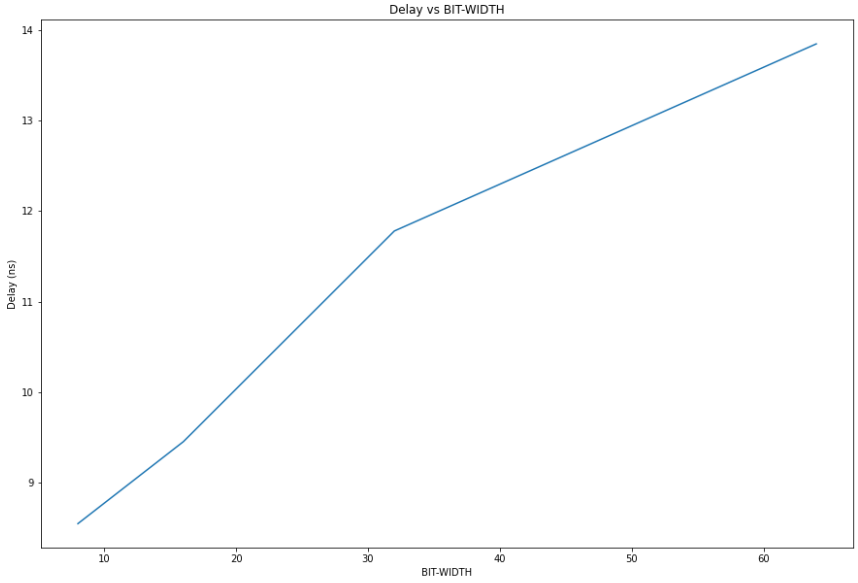


Table 2: Slices and delay for ALU Module

Parameter: **DSIZE**	BIT-WIDTH	No of LUT slices	Delay in ns
8	8	16	6.856
16	16	32	7.286
32	32	64	7.931
64	64	128	8.845

Evaluation 2

ALU Module