Detuning Filter Bank

(from Holzbauer & Schappert, 11/15/2016)

Discrete-time State Space Realization

General form for a system whose outputs and internal states depend linearly on the inputs and internal states

u is the detuning

y is the piezo drive signal

x are estimates of the amplitudes of the cavity mechanical modes

$\mathbf{A}$ can be decomposed into a 2×2 block diagonal matrix, ideal for implementation in an FPGA firmware

$$\begin{aligned} x_{k+1} &= \mathbf{A}x_k \quad\;\; + \mathbf{B}u_k \\ y_{k+1} &= \mathbf{C}x_{k+1} + \mathbf{D}u_k \end{aligned}$$

$$\mathbf{A}^{(j)} = \begin{bmatrix} e^{-\Delta t/\tau_j}\cos\omega_j\Delta t & e^{-\Delta t/\tau_j}\sin\omega_j\Delta t \\ -e^{-\Delta t/\tau_j}\sin\omega_j\Delta t & e^{-\Delta t/\tau_j}\cos\omega_j\Delta t \end{bmatrix}$$

$$\mathbf{B}^{(j)} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$$

$$\mathbf{C}^{(j)} = \begin{bmatrix} G^{(j)}\cos\psi^{(j)} & G^{(j)}\sin\psi^{(j)} \end{bmatrix}$$

Filter Bank: LBNL Implementation

This exact filter bank abstraction was also implemented in LBNL's `res-onator.v`, first checked into git in June, 2014.

For analysis purposes, slightly rearrange these equations. Use a_R and a_I for the real and imaginary parts of $\exp((-1/\tau_j + i\omega_j)\Delta t))$, and use z as the time step operator, to get

$$\begin{pmatrix} z - a_R & -a_I \\ a_I & z - a_R \end{pmatrix} \begin{pmatrix} x_0 \\ x_1 \end{pmatrix} = \begin{pmatrix} u \\ 0 \end{pmatrix}$$

$$\begin{pmatrix} x_0 \\ x_1 \end{pmatrix} = \frac{1}{D} \begin{pmatrix} z - a_R & a_I \\ -a_I & z - a_R \end{pmatrix} \begin{pmatrix} u \\ 0 \end{pmatrix}$$

where D is the determinant $(z - a_R)^2 + a_I^2$. D correctly has roots at a and a^*. Using g_R and g_I as the real and imaginary parts of $G^{(j)} \exp i\psi^{(j)}$,

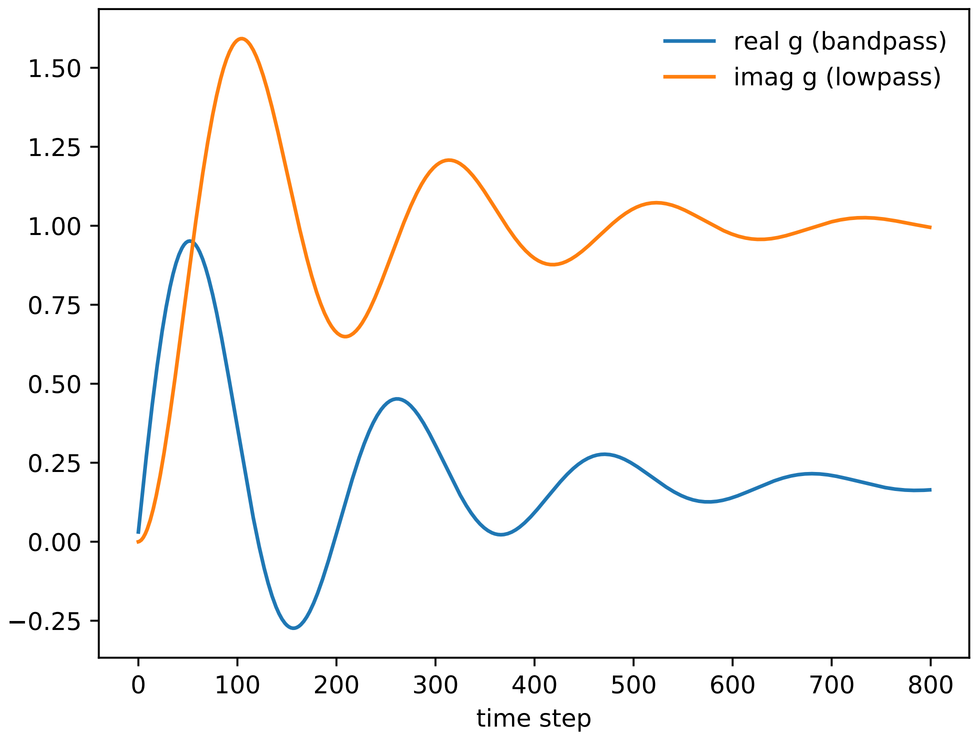
$$y = g_R x_0 + g_I x_1$$

$$y = \frac{g_R(z - a_R) - g_I a_I}{z^2 - 2a_R z + a_R^2 + a_I^2} b_0 u \quad .$$

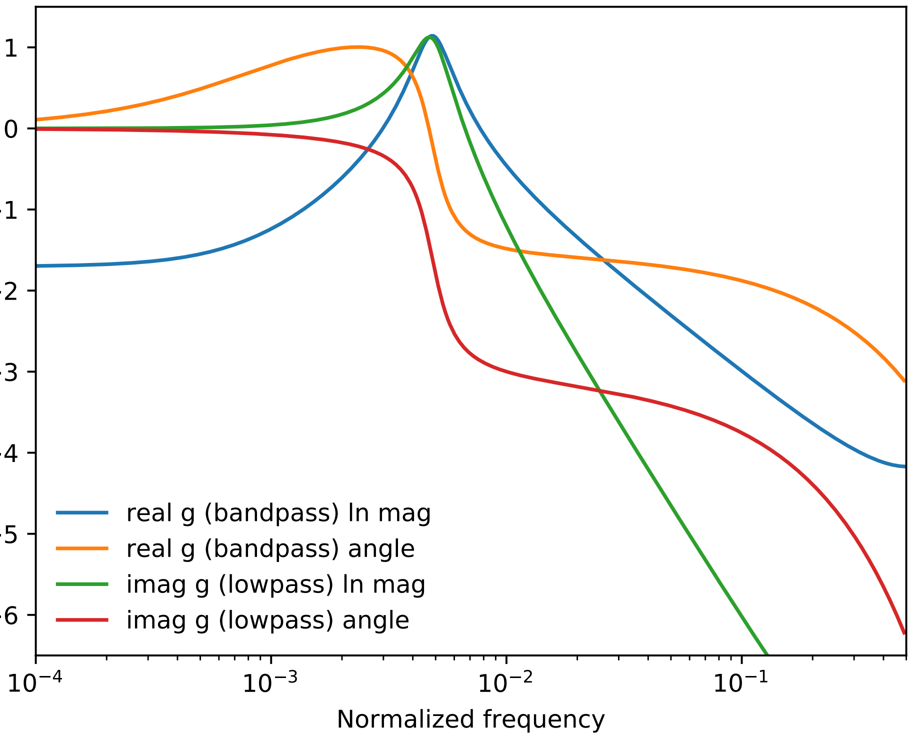
We also need to take note that in `resonator.v`, the value of b is run through a pseudo-floating-point shifter shared with $1 - a_R$ and a_R. To maintain precision on $1 - a_R$ and a_R, at least for $Q > 0.5$, a useful value to choose for b_0 is that which gives unity DC gain for the low-pass filter (imaginary g) case,

$$b_0 = \frac{1 - 2a_R + a_R^2 a_I^2}{|a_I|} \quad .$$

Example time and frequency domain plots are shown for $a = \exp(-0.005 + 0.03i)$.



real g (bandpass)
imag g (lowpass)
1.50
1.25
1.00
0.75
0.50
0.25
0.00
−0.25
0
100
200
300
400
500
600
700
800
time step



real g (bandpass) ln mag
real g (bandpass) angle
imag g (lowpass) ln mag
imag g (lowpass) angle
1
0
−1
−2
−3
−4
−5
−6
10^{-4}
10^{-3}
10^{-2}
10^{-1}
Normalized frequency

Explicitly, the iteration expression in `resonator.v` is scaled according to

$$x_{k+1} = x_k + (Fx_k + Bv_k) \cdot 4^{s-9}$$

where s is an integer shift value, $0 \leq s \leq 7$. Hence

$$F = (a - 1) \cdot 4^{9-s}$$

$$B = b \cdot 4^{9-s}$$

and s is chosen as the largest value such that the (absolute values of) register values F and v remain less than one.

In the previous example, $a - 1 = -0.005435 + 0.029846i$ and $b = 0.030836$, so choose $s = 7$, giving scaled values

$$\begin{aligned} F_R &= -0.08696 \\ F_I &= 0.47753 \\ B_R &= 0.49337 \quad . \end{aligned}$$

To get physical (signed integer) 18-bit register values, scale these real numbers by 2^{17}. The full-scale negative value (-2^{17}) is not valid for any coefficient register.

Absolute values of $1 - a_R$, a_I, and $b \geq 1/16$ are not supported.

The imaginary part sign convention for g used in `dot_prod.v`, and therefore `afilter_siso.v`, is inverted compared with the rest of this document.

It can be noted in the graphs above that the filter gain can exceed unity. The state vector x is internally saturated to stay (absolute value) less than one, which will corrupt the frequency response if encountered. This condition is detected in the hardware, and is made available for external monitoring via `afilter_siso`'s `res_clip` port. Mitigation involves reducing the value of b.

The implementation is heavily pipelined, and quite capable of clocking at 200 MHz in a 7-series Xilinx chip.