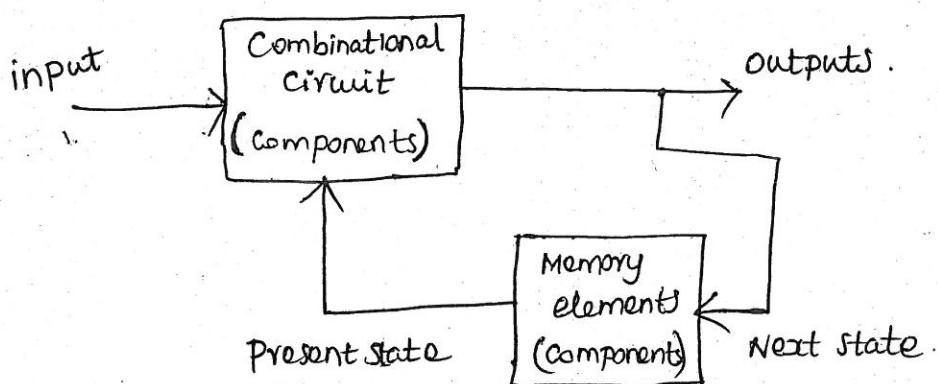


Unit - IV - Sequential logic Circuit

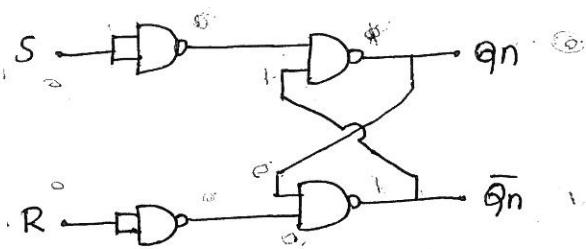
Sequential Circuit:



- Output of Sequential Circuits are not only dependent on the present input conditions but they also depend upon the past history of these inputs. The past history is provided by feedback from the output back to the input.
- The information stored in the memory elements at any given time defines the present state of the Sequential Circuit.
- The present state and external input determine the outputs and the next state of the Sequential Circuit.

Latches	Flip-flops.
<ul style="list-style-type: none">(i) A latch checks all its inputs continuously & change its output accordingly at any time.(ii) No clock is used.(iii) Used in asynchronous sequential logic circuit.	<ul style="list-style-type: none">(1) Flip-flop samples its inputs & changes its outputs only at a time as determined by a clock signal.(2) A clock is used.(3) Used in synchronous sequential circuit.

SR - Latch:-



Case 1:- If $S=0; R=0$

- * If Q_n as 0, then $Q_{n+1} = 0$. } Both present & future outputs
 $(\overline{Q_{n+1}} = 1)$ are same. So state of operation
- * If Q_n as 1, then $Q_{n+1} = 1$. } is no change.
 $(\overline{Q_{n+1}} = 0)$

Case 2:- If $S=0; R=1$

- * If Q_n as 0, then $Q_{n+1} = 0$. } Here whatever may be the input
 $(\overline{Q_{n+1}} = 1)$ for Q_n , the future output Q_{n+1}
- * If Q_n as 1, then $Q_{n+1} = 0$. } is 0. the state operation Reset.
 $(\overline{Q_{n+1}} = 1)$

Case 3:- If $S=1, R=0$.

- * If Q_n as 0, then $Q_{n+1} = 1$. } Whatever may be the present input
 $(\overline{Q_{n+1}} = 0)$ for Q_n , the future output Q_{n+1} is
- * If Q_n as 1, then $Q_{n+1} = 1$. } 1. so, the state of operation is set.
 $(\overline{Q_{n+1}} = 0)$

Case 4:- If $S=1, R=1$

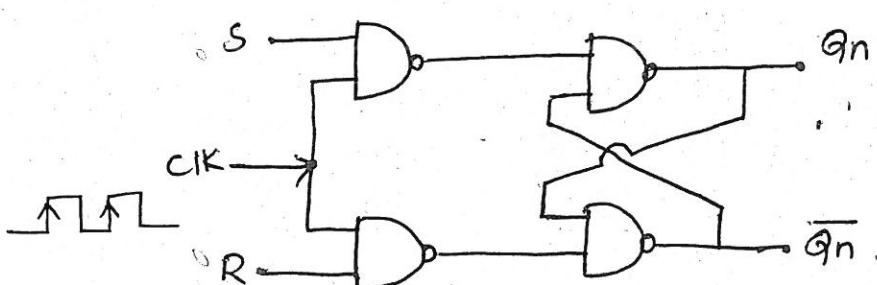
- * If Q_n as 0, then $Q_{n+1} = 1$. } Here both Q_{n+1} & $\overline{Q_{n+1}}$ (both) are same.
 $(\overline{Q_{n+1}} = 1)$
- * If Q_n as 1, then $Q_{n+1} = 1$. } Which is a indeterminate (Invalid state).
 $(\overline{Q_{n+1}} = 1)$

Truth Table:

S	R	Q_n	Q_{n+1}	State.
0	0	0	0	No change.
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	X	Invalid.
1	1	1	X	

S-R - Flip flop:-

→ The circuit is similar to SR latch, extra here we adding the clock pulse (CP). On the positive edge of the clock pulse, The circuit responds to the S and R inputs.



→ When $S=0, R=0$, the clk pulse is high (1). Then If the present output Q_n is 0, the output $Q_{n+1}=0$. If the Q_n is 1, the future output is 1. The state of operation is no change.

Truth Table

CLK	S	R	Q_n	Q_{n+1}	State
1	0	0	0	0	No change.
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	X	X	Invalid.
1	1	1	X	X	(Indeterminate)

Characteristic equation:-

$s \overline{R} \overline{q}_n$ $\overline{R} q_n$ $R \overline{q}_n$ $R q_n$

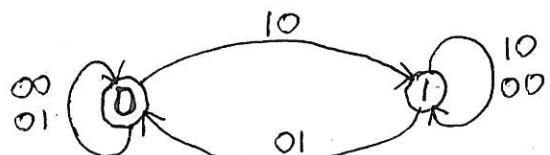
\overline{s}	$\overline{R} \overline{q}_n$	$\overline{R} q_n$	$R \overline{q}_n$	$R q_n$
0	0	1	0	0
1	1	X	X	X
s	4	5	6	7

$Q_{n+1} = s + \overline{R} Q_n$

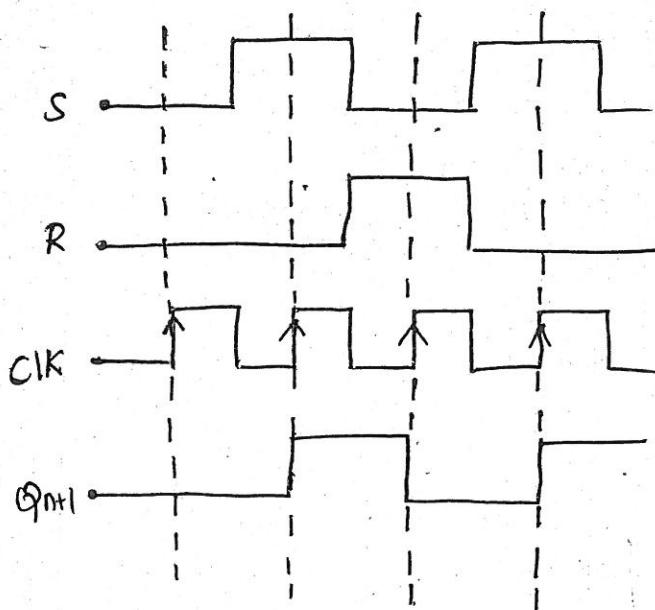
State Diagram

Excitation Table

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

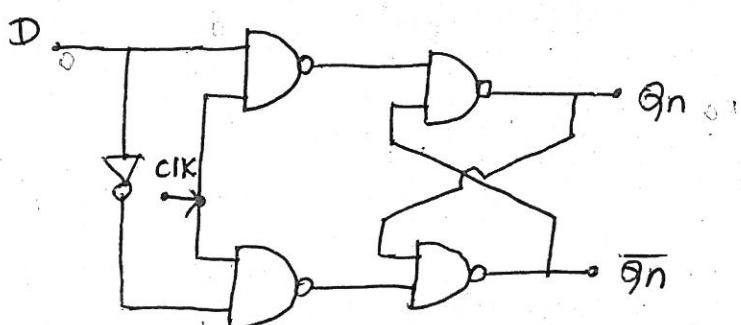


Waveform:-



D-Flip-flop :-

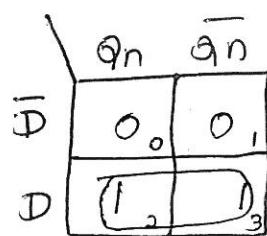
- A flip-flop whose output follows its data input when the clock is active is called as D-flip-flop.
- In S-R flipflop, when both inputs are same, the output either does not change (or) invalid. [$00 \rightarrow$ no change, $11 \rightarrow$ invalid].
- These input conditions can be avoided by making them complements of each other. The input is called D.



Truth Table

clk	D	Qn	Qn+1	State.
0	X	X	X	NO operation.
0	X	X	X	
1	0	0	0	Reset.
1	0	1	0	
1	1	0	1	Set.
1	1	1	1	

Characteristic equation

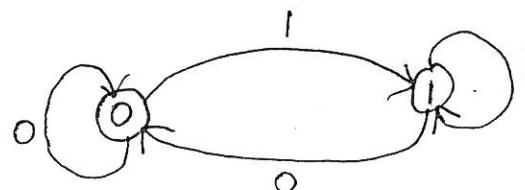


$$Q_{n+1} = D$$

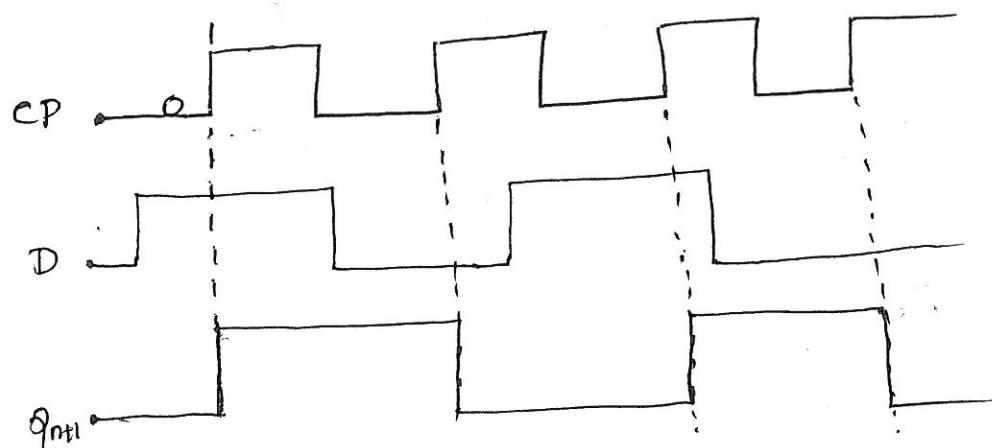
Excitation Table :-

Qn	Qn+1	D
0	0	0
0	1	1
1	0	0
1	1	1

State Diagram.

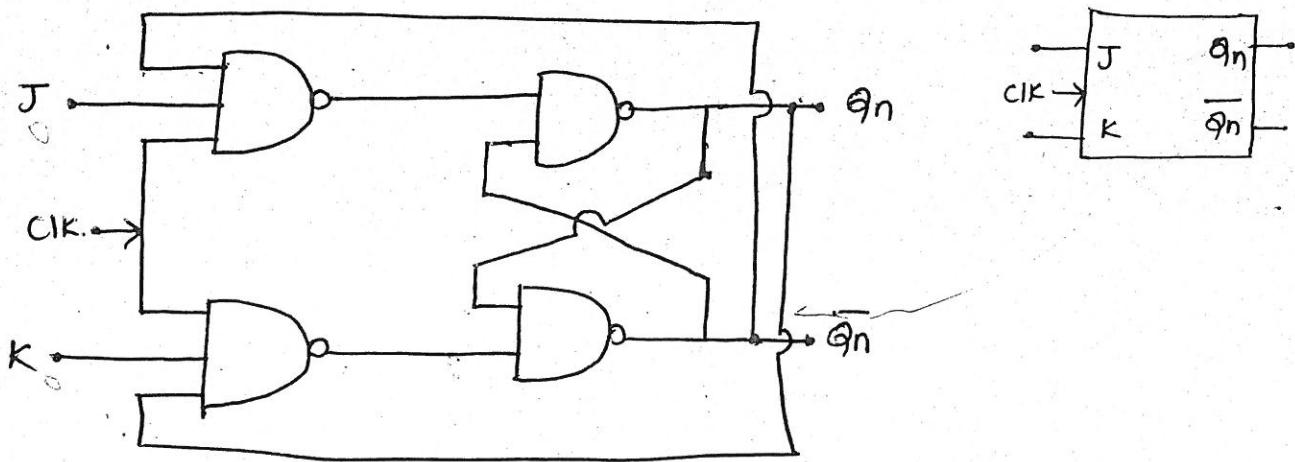


Waveform.



JK - flip flop :-

- JK flip-flop is a refinement of SR - flip flop. In SR flip flop, when both inputs are high (11). The output is indeterminate condition is produced.
- But in JK flip flop, indeterminate condition is changed to toggle state condition, by connecting \bar{Q}_n and Q_n outputs are back to the J and K excitation inputs.



Truth Table

clk	J	K	Q_n	Q_{n+1}	State.
1	0	0	0	0	No change
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set.
1	1	0	1	1	
1	1	1	0	1	Toggle.
1	1	1	1	0	

Characteristic equation.

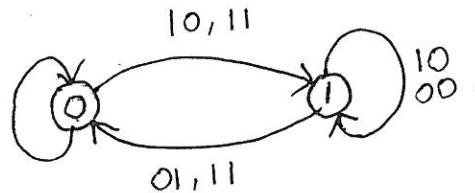
J	Kan	$\bar{K}an$	$\bar{K}an$	Kan	Kan	$\bar{K}an$
\bar{J}	0	1	1	0	0	2
\bar{J}	0	1	1	1	1	6
J	4	5	5	7	7	6

$$Q_{n+1} = \bar{K}Q_n + JK$$

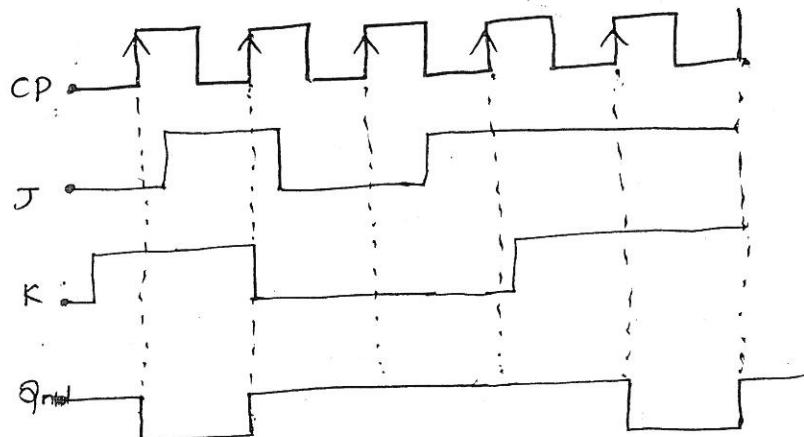
Excitation Table.

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

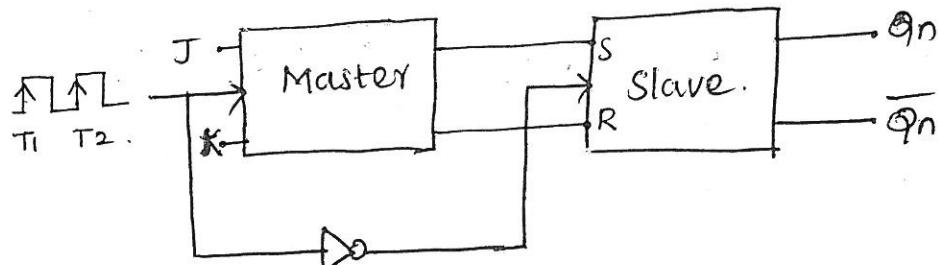
State Diagram.



Waveform.



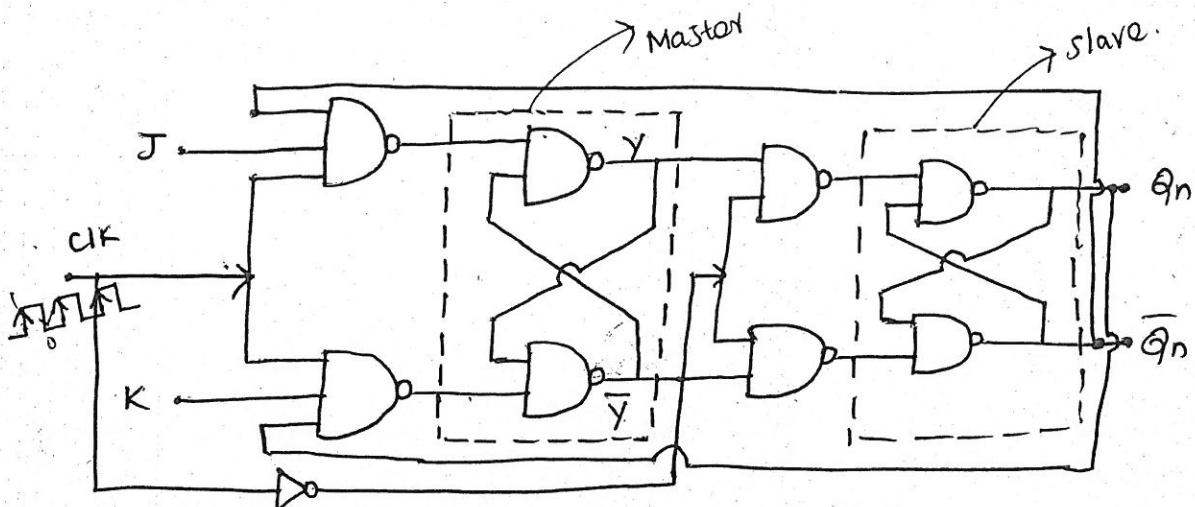
Master-Slave J-K Flip-flop:-



→ It consists of clocked JK flip flop as master and clocked SR flip flop as slave. The output of master flip flop is fed as an input of Slave FF.

→ Clock signal is connected directly to the master flip-flop, but it is connected through inverter to the slave flipflop.

→ So, the circuit accepts input data when clock signal is "High", and passes the data to the output on the falling-edge of the clock sig



→ When $J=1$ & $K=0$, the master sets on the positive clock. The high y output of the master drives the S input of the slave, so at -ve clock slave sets, copying action of master.

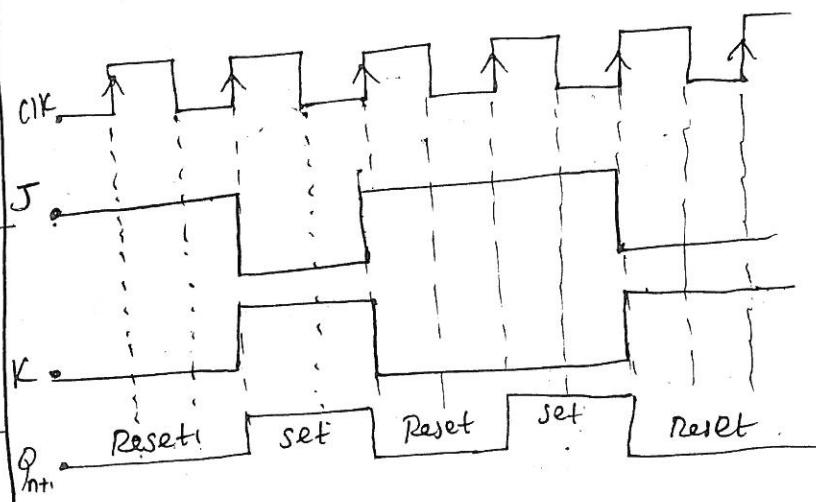
→ When $J=0$, & $K=1$, the master resets on the positive clock. The \bar{y} output of master goes to the R input of slave. Therefore, at negative clock slave resets, → again copying action of the master.

→ When $J=1$, $K=1$, master toggles on the positive clock and slave then copies the o/p of master on -ve clock. At this instant, feedback inputs to the master ff are complemented but ^{as} it is negative half of the CP master ff is inactive. This prevents the race around condition.

Truth Table :-

C	I	K	Q _n	J	Y	Q _{n+1}
↓	0	0	0	0	0	NC
↓	0	0	0	0	NC	0
↑	0	0	1	0	0	NC
↓	0	0	1	0	NC	0
↑	0	1	0	1	1	NC
↓	0	1	0	NC	1	
↑	0	1	1	1	1	NC
↓	0	1	1	NC	1	
↑	1	0	0	1	1	NC
↓	1	0	0	NC	1	
↑	1	0	1	0	0	NC
↓	1	0	1	NC	0	
↑	1	1	0	1	1	NC
↓	1	1	0	NC	1	
↑	1	1	1	0	0	NC
↓	1	1	1	NC	0	

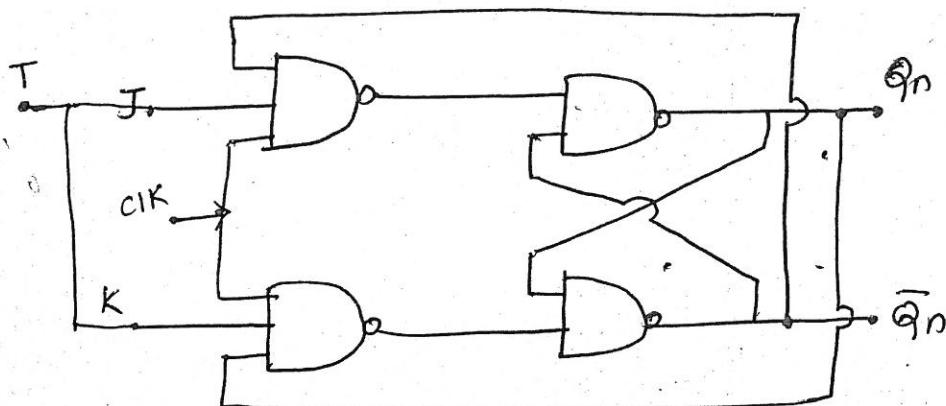
waveform



T Flip-flop (Toggle FF) :-

→ It is a modification of JK. Which is made by connecting J and K terminals together.

J and K terminals together.



Truth Table

Clk	T	Qn	Qn+1	State
0	X	X	X	No operation
1	0	0	0	No change
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	

Characteristic equation

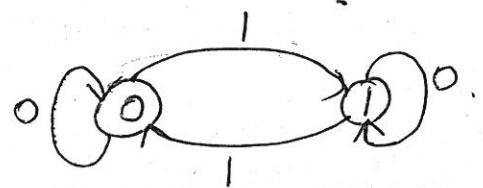
	Qn	Qn
T	0	1
T	1	0

$$Q_{n+1} = \bar{T}Q_n + T\bar{Q}_n$$

State Diagram

Excitation Table -

Qn	Qn+1	T
0	0	0
0	1	1
1	0	1
1	1	0

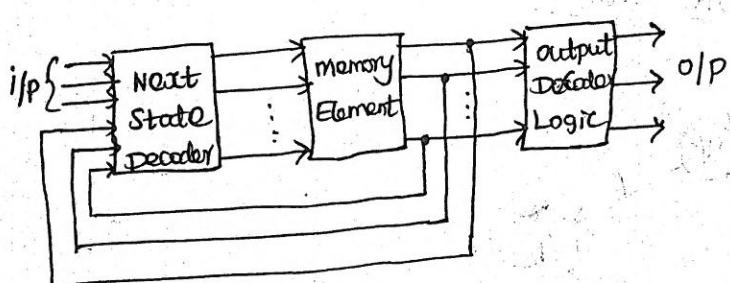


Synchronous Sequential Circuits (SSC):

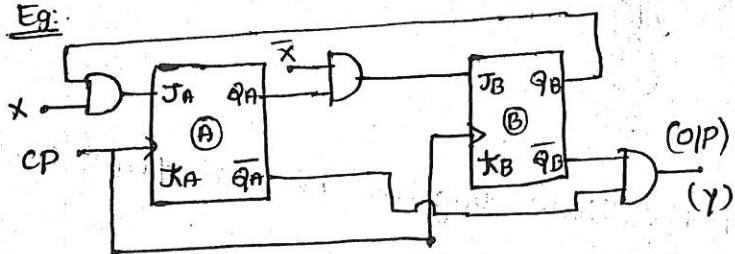
Moore Circuit

→ Output depends on present state of flip-flop.

[If the input changes, the output doesn't change]



Eg:-

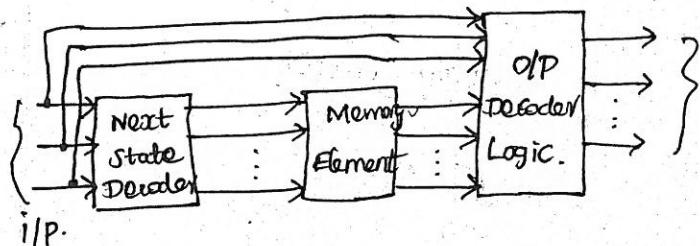


→ It requires more no. of states for implementing the same function.

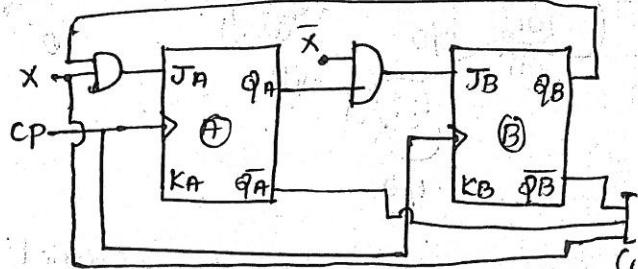
Mealy circuit

→ If Input changes, the output changes.

→ Output depends on present state of flip-flop and input values.



Eg:-



→ It requires Less no. of states for implementing the same function.

State Diagram:-

→ It is a pictorial representation of behaviour of a sequential circuit.

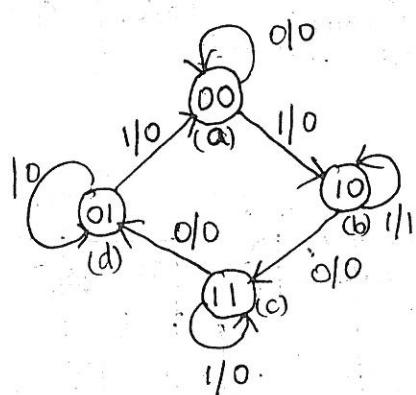
State:- → State of a sequential circuit machine is defined as the content of memory, i.e., Machine state is defined by q outputs. It is represented by circle.

→ Transition between states is given by directed lines connecting the circles.

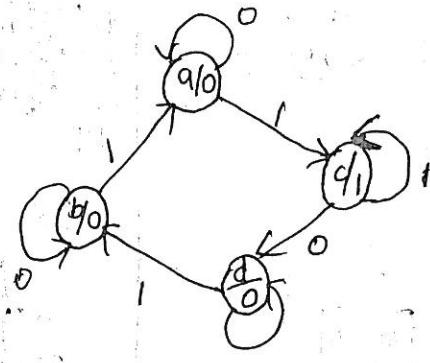
→ Binary number tells the state represented by circle. I/O implies input value, $0 \rightarrow$ output value.

→ In Moore Ckt, the number near the line gives the input that causes transition. The output is indicated within the circle. [Output depends on only present state & not depends input].

Mealy Circuit



Moore circuit



State Table: → The information in the State diagram is translated into State Table.

State table [Tabular Form].

→ It represents relationship b/w input, output and FF States.

State Table for Mealy State Diagram:-

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
00-a	00	10	0	0
10-b	11	10	0	1
11-c	01	11	0	0
01-d	01	00	0	0

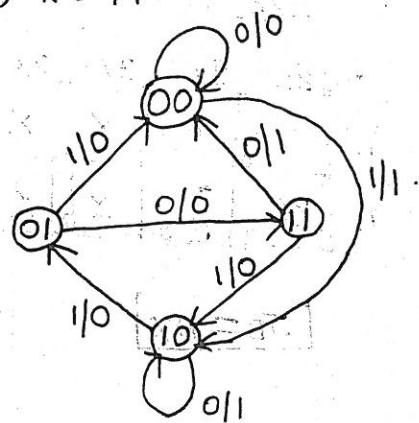
State table for Moore Circuit :-

Present State	Next state		output (Y)
	$x=0$	$x=1$	
a	a	c	0
b	b	a	0
c	d	c	1
d	b	d	0

State Assignment :- → The change from one state to another. i.e., performed by flip-flops. To determine the FF functions the states must be represented in binary values [Not-alphabets].

Problem on Design using Mealy MODEL :-

- (1). A sequential circuit has one input and one output, for the state diagram shown. Design the Sequential circuit with a) D-FF b) T-FF c) JK-FF d) R-S-FF.



Soln:-

State Table .

Present state (AB)	Next state		output	
	$x=0$ (A B)	$x=1$ (A B)	$x=0$ (Y)	$x=1$ (Y)
00	00	00	1	0
01	11	00	0	0
10	10	01	1	0
11	00	10	1	0

1) Using JK FF:-

Present state (A B)	Input (X)	Next state (A B)	Flip-Flop Input				Output (Y)
			JA	KA	JB	KB	
00	0	00	0	X	0	X	0
00	1	10	1	X	0	X	1
01	0	11	1	X	X	0	0
01	1	00	0	X	X	1	0
10	0	10	X	0	0	X	1
10	1	01	X	1	1	X	0
11	0	00	X	1	X	1	1
11	1	10	X	0	X	1	0

JK Excitation Table

Qn	qntl	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

By using K-map simplification the FF input functions and O/P function are obtained.

K-map Simplification:-

<u>JA</u>			
$\bar{B}X$	$\bar{B}X$	BX	$B\bar{X}$
0	1	0	1
X_4	X_5	X_2	X_1

$$JA = \bar{B}X + B\bar{X}$$

<u>KA</u>			
$\bar{B}X$	$\bar{B}X$	BX	$B\bar{X}$
A	X ₀	X ₁	X ₃
A	0 ₄	1 ₅	0 ₂

$$KA = \bar{B}X + B\bar{X}$$

<u>JB</u>			
$\bar{B}X$	$\bar{B}X$	BX	$B\bar{X}$
A	0 ₀	0 ₁	X ₃
A	0 ₄	1 ₅	X ₆

$$JB = AX$$

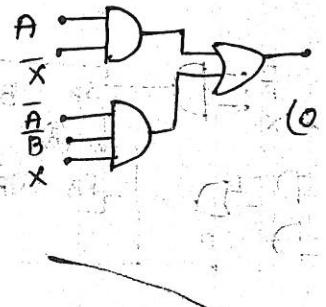
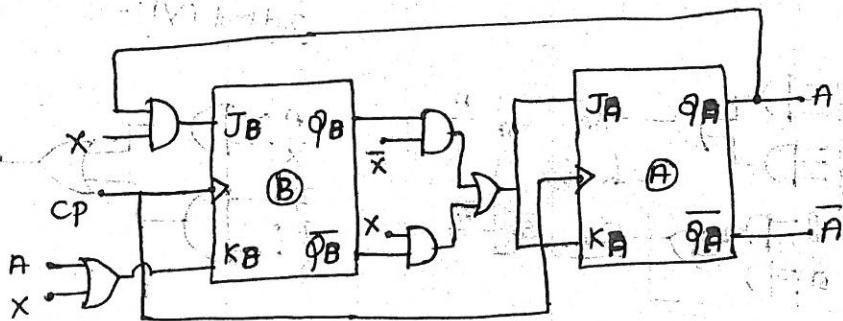
<u>KB</u>			
$\bar{B}X$	$\bar{B}X$	BX	$B\bar{X}$
X ₀	X ₁	1 ₃	0 ₂
X ₄	X ₅	1 ₇	1 ₆

$$KB = A + X$$

$\bar{B}X$	$\bar{B}X$	BX	$B\bar{X}$
A	0 ₀	1 ₁	0 ₃
A	1 ₄	0 ₅	0 ₇

$$y = A\bar{X} + \bar{A}\bar{B}X$$

Logic diagram:



(b). Using R-S FF:-

Present State (AB)	Input (X)	Next state (AB)	FF - inputs				output Y
			SA	RA	SB	RB	
00	0	00	0	X	0	X	0
00	1	10	1	0	0	X	1
01	0	11	1	0	X	0	0
01	1	00	0	X	0	1	0
10	0	10	X	0	0	X	1
10	1	01	0	1	1	0	0
11	0	00	0	1	0	1	1
11	1	10	X	0	0	1	0

SR - Excitation

Q	Anti	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

K-map simplification

<u>SA</u>				
$\bar{B}x$	$\bar{B}x$	Bx	$B\bar{x}$	
\bar{A}	0 ₀	1 ₁	0 ₃	1 ₂
A	X ₄	0 ₅	X ₇	0 ₆

$$SA = \bar{A}\bar{B}x + \bar{A}B\bar{x}$$

<u>RA</u>				
$\bar{B}x$	$\bar{B}x$	Bx	$B\bar{x}$	
\bar{A}	X ₀	0 ₁	X ₃	0 ₂
A	0 ₄	1 ₅	0 ₇	1 ₆

$$RA = \bar{A}\bar{B}x + A\bar{B}\bar{x}$$

<u>SB</u>				
$\bar{B}x$	$\bar{B}x$	Bx	$B\bar{x}$	
\bar{A}	0 ₀	0 ₁	0 ₃	X ₂
A	0 ₄	1 ₅	0 ₇	0 ₆

$$SB = A\bar{B}x$$

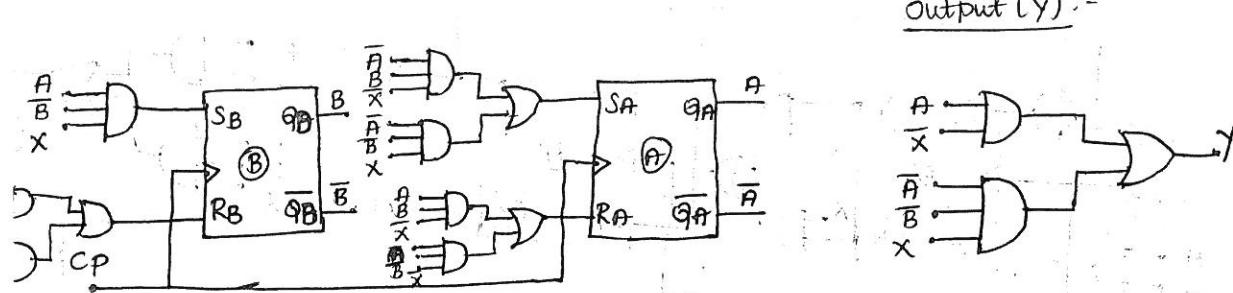
<u>RB</u>				
$\bar{B}x$	$\bar{B}x$	Bx	$B\bar{x}$	
\bar{A}	X ₀	X ₁	1 ₃	0 ₂
A	X ₄	0 ₅	1 ₂	1 ₁

$$RB = AB + BX$$

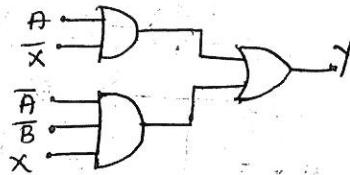
<u>Y</u>				
$\bar{B}x$	$\bar{B}x$	Bx	$B\bar{x}$	
\bar{A}	0 ₀	1 ₁	0 ₃	0 ₂
A	1 ₁	0 ₀	0 ₂	1 ₁

$$Y = A\bar{x} + \bar{A}B\bar{x}$$

Logic diagram:-



Output (Y) :-



(C). Using T-FF:-

Present State (AB)	Input (x)	Next State (AB)	Flip-Flop Input TA TB	Output (Y)
00	0	00	0 0	0
00	1	10	1 0	1
01	0	11	1 0	0
01	1	00	0 1	0
10	0	10	0 0	1
10	1	01	1 1	0
11	0	00	1 1	1
11	1	10	0 1	0

T-FF - Excitation Table.

Q _n	Q _{n+1}	f
0	0	0
0	1	1
1	0	1
1	1	0

K-map Simplification:-

TA

$\bar{B}x$	$\bar{B}x$	Bx	$B\bar{x}$
0 ₀	1 ₁	0 ₃	1 ₂
0 ₄	1 ₅	0 ₇	1 ₆

TB

$\bar{B}\bar{x}$	$\bar{B}x$	Bx	$B\bar{x}$	
\bar{A}	0 ₀	0 ₁	1 ₃	0 ₂
A	0 ₄	1 ₅	1 ₇	1 ₆

output (Y)

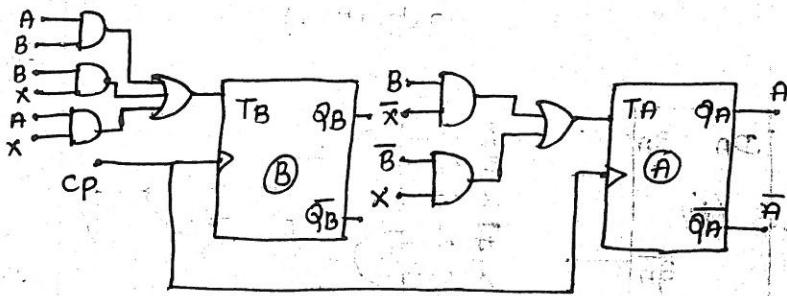
$\bar{B}\bar{x}$	$\bar{B}x$	Bx	$B\bar{x}$	
\bar{A}	0 ₀	1 ₁	0 ₃	0 ₂
A	1 ₄	0 ₅	0 ₇	1 ₆

$$T_A = \bar{B}x + \bar{B}\bar{x}$$

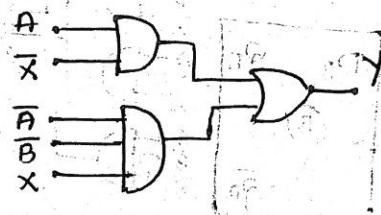
$$T_B = Ax + Bx + AB$$

$$Y = Ax + \bar{A}\bar{B}x$$

Logic diagram:-



Output (Y)



(D). Using D-FF:-

Present state (AB)	Input (X)	Next state (AB)	Flip-flop input DA DB	Output (Y)
00	0	00	0 0	0
00	1	10	1 0	1
01	0	11	1 1	0
01	1	00	0 0	0
10	0	10	1 0	1
10	1	01	0 1	0
11	0	00	0 0	1
11	1	10	1 0	0

DFF Excitation Tab

Q _n	Q _{n+1}	J
0	0	0
0	1	1
1	0	0
1	1	1

K-map Simplification

DA

	$\bar{B}x$	$\bar{B}x$	Bx	$B\bar{x}$
\bar{A}	0 ₀	1 ₁	0 ₃	1 ₂
A	1 ₄	0 ₅	1 ₇	0 ₆

DB

	$\bar{B}x$	$\bar{B}x$	Bx	$B\bar{x}$
\bar{A}	0 ₀	0 ₁	0 ₃	1 ₂
A	0 ₄	1 ₅	0 ₇	0 ₆

y (output)

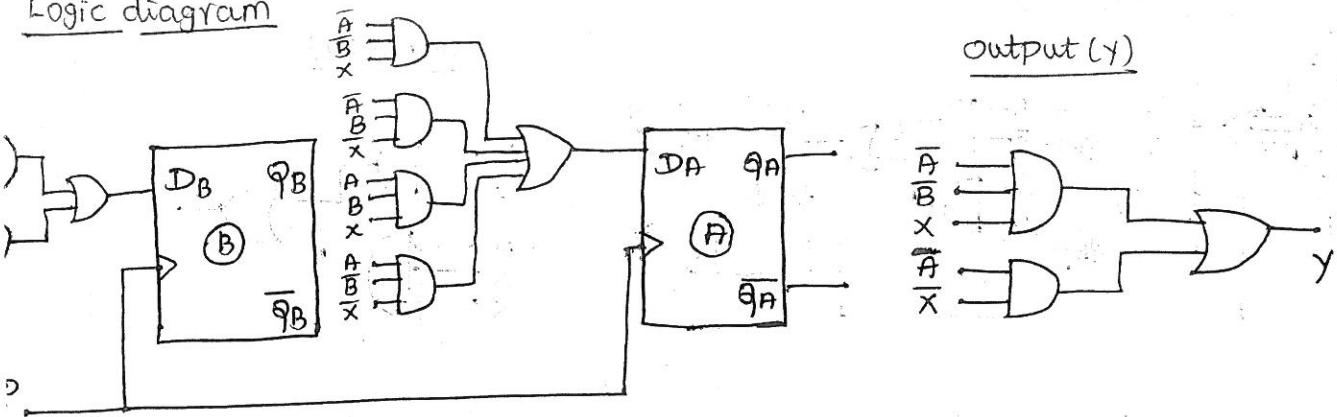
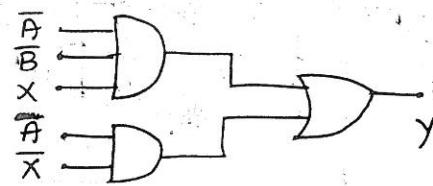
	$\bar{B}x$	$\bar{B}x$	Bx	$B\bar{x}$
\bar{A}	0 ₀	1 ₁	0 ₃	0 ₂
A	1 ₄	0 ₅	0 ₇	1 ₆

$$DA = \bar{A}\bar{B}\bar{x} + \bar{A}\bar{B}x + ABx + \bar{A}B\bar{x}$$

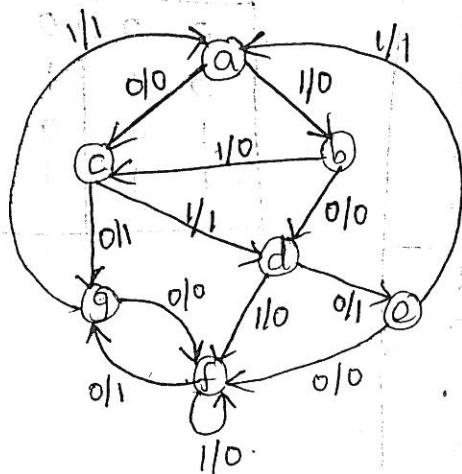
$$DB = \bar{A}B\bar{x} + A\bar{B}\bar{x}$$

$$y = A\bar{x} + \bar{A}Bx$$

(2)

Logic diagramOutput (Y)

1. Design a clocked sequential circuit for state diagram shown below.
[using D-FF]

Soln:- State Table $(g=2) \rightarrow \text{changes}$

Present State	Next State		Output (Y)	
	$x=0$	$x=1$	$x=0$	$x=1$
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
d	f	f	1	0
e	(f)	a	0	1
f	e	f	0	0
g	f	a	0	1

Reduced State Table:- $(f=d) \rightarrow \text{changes.}$

Present State	Next State		Output (Y)	
	$x=0$	$x=1$	$x=0$	$x=1$
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
d	e	(f)	1	0
e	(f)	a	0	1
f	e	f	0	0

Final State Table:-

Present State	Next State		Output (Y)	
	$x=0$	$x=1$	$x=0$	$x=1$
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
d	e	d	1	0
e	d	a	0	1

It contains 5 State variables, so for implement, no. of FF required is 3.

$a = 000, b = 001, c = 010, d = 011, e = 100$.

Excitation Table:-

Present State A B C	Input(x) (X)	Next State. A B C			FF - Input D _A D _B D _C			Output (Y)
		A	B	C	D _A	D _B	D _C	
0 0 0	0	0	1	0	0	1	0	0
0 0 0	1	0	0	1	0	0	1	0
0 0 1	0	0	1	1	0	1	1	0
0 0 1	1	0	1	0	0	1	0	0
0 1 0	0	1	0	0	1	0	0	1
0 1 0	1	0	1	1	0	1	1	1
0 1 1	0	1	0	0	1	0	0	1
0 1 1	1	0	1	1	0	1	1	0
1 0 0	0	0	1	1	0	1	1	0
1 0 0	1	0	0	0	0	0	0	1

K-map Simplification:-

D_A

	$\bar{C}\bar{X}$	$\bar{C}X$	$C\bar{X}$	CX
$\bar{A}\bar{B}$	0 ₀	0 ₁	0 ₃	0 ₂
$\bar{A}B$	1 ₄	0 ₅	0 ₇	1 ₆
$A\bar{B}$	X ₁₂	X ₁₃	X ₁₅	X ₁₄
AB	0 ₈	0 ₉	X ₁₁	X ₁₀

D_B

	$\bar{C}\bar{X}$	$\bar{C}X$	$C\bar{X}$	CX
$\bar{A}\bar{B}$	1 ₀	0 ₁	1 ₃	1 ₂
$\bar{A}B$	0 ₄	1 ₅	1 ₇	0 ₆
$A\bar{B}$	X ₁₂	X ₁₃	X ₁₅	X ₁₄
AB	1 ₈	0 ₉	X ₁₁	X ₁₀

D_C

	$\bar{C}\bar{X}$	$\bar{C}X$	$C\bar{X}$	CX
$\bar{A}\bar{B}$	0 ₀	1 ₁	0 ₃	1 ₂
$\bar{A}B$	0 ₄	1 ₅	1 ₇	0 ₆
$A\bar{B}$	X ₁₂	X ₁₃	X ₁₅	X ₁₄
AB	1 ₈	0 ₉	X ₁₁	X ₁₀

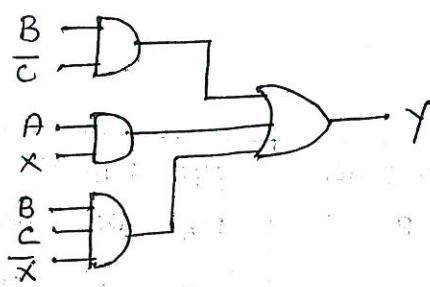
$$D_A = B\bar{C}\bar{X} + BC\bar{X}$$

$$D_B = CX + B\bar{X} + \bar{B}\bar{X} +$$

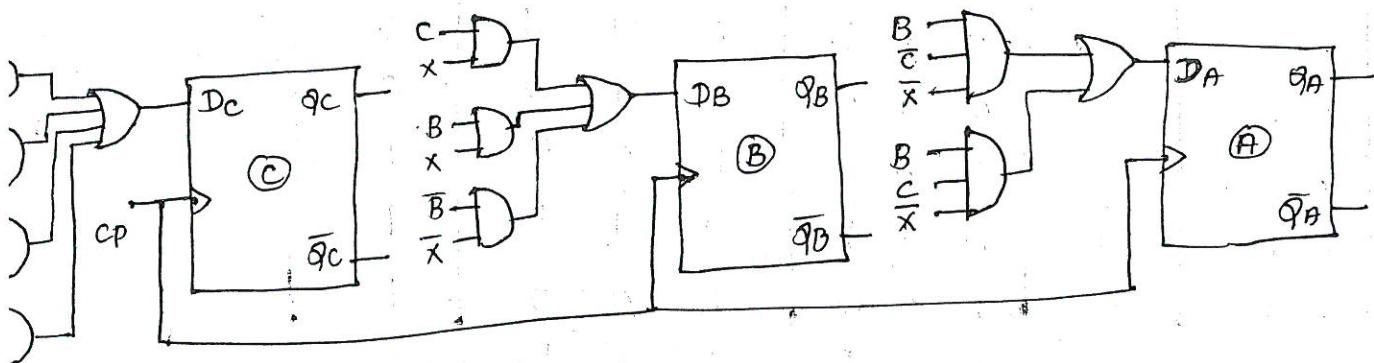
$$D_C = BX + \bar{A}\bar{B}X + \bar{B}C\bar{X} + \bar{A}C\bar{X}$$

$\bar{C}X$	$\bar{C}X$	CX	$C\bar{X}$
0 ₀	0 ₁	0 ₃	0 ₂
1 ₄	1 ₅	0 ₇	1 ₆
X ₁₂	X ₁₃	X ₁₅	X ₁₄
0 ₈	1 ₉	X ₁₈	X ₁₀

Output(Y)

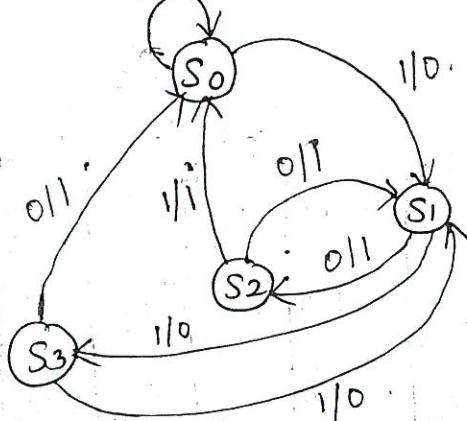


$$Z = B\bar{C} + AX + BC\bar{X}$$



- 3). Design the Sequential Circuit using JK-FF, for the state diagram shown.

0/0



Soln: State Table

Present state	Next state		output (Y)	
	$x=0$	$x=1$	$x=0$	$x=1$
S_0	S_0	S_1	0	0
S_1	S_2	S_3	1	0
S_2	S_1	S_0	1	1
S_3	S_0	S_1	1	0

→ Assign the state variables $s_0 = 00$; $s_1 = 01$; $s_2 = 10$; $s_3 = 11$

Excitation Table :- (JK-FF)

Present State (A,B)	Input (X)	Next State (A,B)	FF - Inputs.		Output (Y)
			J _A	K _A	
00	0	00	0 X	0 X	0
00	1	01	0 X	1 X	0
01	0	10	1 X	X 1	1
01	1	11	1 X	X 0	0
10	0	01	X 1	1 X	1
10	1	00	X 1	0 X	1
11	0	00	X 1	X 1	1
11	1	01	X 1	X 0	0

K-map Simplification:

JA

		$\bar{B}X$		$\bar{B}X$		BX		$B\bar{X}$	
		0 ₀	0 ₁	1 ₃	1 ₂	0 ₀	0 ₁	1 ₃	1 ₂
		X ₄	X ₅	X ₇	X ₆	X ₄	X ₅	X ₇	X ₆
0	0	0 ₀	0 ₁	1 ₃	1 ₂	0 ₀	0 ₁	1 ₃	1 ₂
1	0	X ₄	X ₅	X ₇	X ₆	X ₄	X ₅	X ₇	X ₆

$$JA = B$$

KA

		$\bar{B}X$		$\bar{B}X$		BX		$B\bar{X}$	
		0 ₀	0 ₁	1 ₃	1 ₂	0 ₀	0 ₁	1 ₃	1 ₂
		X ₀	X ₁	X ₃	X ₂	X ₀	X ₁	X ₃	X ₂
0	0	0 ₀	0 ₁	1 ₃	1 ₂	0 ₀	0 ₁	1 ₃	1 ₂
1	0	X ₀	X ₁	X ₃	X ₂	X ₀	X ₁	X ₃	X ₂

$$KA = I$$

JB

		$\bar{B}X$		$\bar{B}X$		BX		$B\bar{X}$	
		0 ₀	0 ₁	1 ₃	1 ₂	0 ₀	0 ₁	1 ₃	1 ₂
		X ₄	X ₅	X ₇	X ₆	X ₄	X ₅	X ₇	X ₆
0	0	0 ₀	0 ₁	1 ₃	1 ₂	0 ₀	0 ₁	1 ₃	1 ₂
1	0	X ₄	X ₅	X ₇	X ₆	X ₄	X ₅	X ₇	X ₆

KB

		$\bar{B}X$		$\bar{B}X$		BX		$B\bar{X}$	
		0 ₀	0 ₁	1 ₃	1 ₂	0 ₀	0 ₁	1 ₃	1 ₂
		X ₄	X ₅	X ₇	X ₆	X ₄	X ₅	X ₇	X ₆
0	0	0 ₀	0 ₁	1 ₃	1 ₂	0 ₀	0 ₁	1 ₃	1 ₂
1	0	X ₄	X ₅	X ₇	X ₆	X ₄	X ₅	X ₇	X ₆

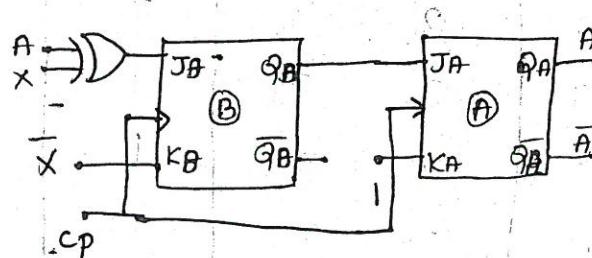
$$KB = \bar{X}$$

output (Y)

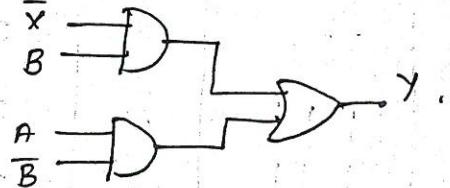
		$\bar{B}X$		$\bar{B}X$		BX		$B\bar{X}$	
		0 ₀	0 ₁	1 ₃	1 ₂	0 ₀	0 ₁	1 ₃	1 ₂
		X ₄	X ₅	X ₇	X ₆	X ₄	X ₅	X ₇	X ₆
0	0	0 ₀	0 ₁	1 ₃	1 ₂	0 ₀	0 ₁	1 ₃	1 ₂
1	0	X ₄	X ₅	X ₇	X ₆	X ₄	X ₅	X ₇	X ₆

$$Y = \bar{X}B + AB$$

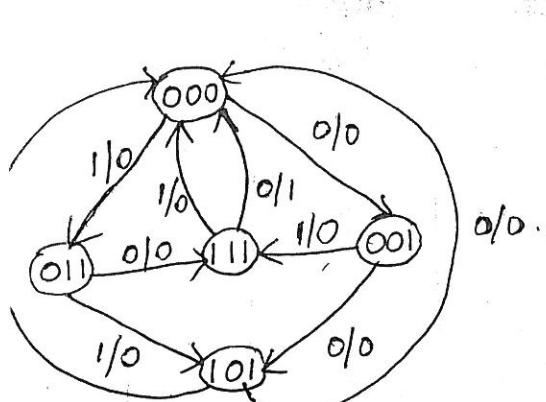
Logic Diagram:



Output:



Design syn. sequential circuit for the given State diagram using D-flip-flop.



State Table

Present state (A B C)	Next state		output(y)	
	x=0	x=1	x=0	x=1
0 0 0	0 0 1	0 1 1	0	0
0 0 1	1 0 1	1 1 1	0	0
0 1 1	1 1 1	1 0 1	0	0
1 0 1	0 0 0	0 0 0	0	1
1 1 1	0 0 0	0 0 0	1	0

Excitation Table

Present State (A B C)	input (x)	Next state (A B C)	Flip-Flop Input DA DB DC.	output (y)
0 0 0	0	0 0 1	0 0 1	0
0 0 0	1	0 1 1	0 1 1	0
0 0 1	0	1 0 1	1 0 1	0
0 0 1	1	1 1 1	1 1 1	0
0 1 1	0	1 1 1	1 1 1	0
0 1 1	1	1 0 1	1 0 1	0
1 0 1	0	0 0 0	0 0 0	0
1 0 1	1	0 0 0	0 0 0	1
1 1 1	0	0 0 0	0 0 0	1
1 1 1	1	0 0 0	0 0 0	0

K-mapp-Simplification :-

		$\bar{C}X$	$\bar{C}X$	CX	$C\bar{X}$
		$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
0	0	0	1	1	1
X ₄	X ₅	X ₇	X ₆	X ₁₂	X ₁₃
X ₁₂	X ₁₃	0 ₁₅	0 ₁₄	0 ₁₁	0 ₁₀
X ₈	X ₉	0 ₁₁	0 ₁₀		

$$D_A = \bar{A}C$$

		$\bar{C}X$	$\bar{C}X$	CX	$C\bar{X}$
		$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
0	0	1	1	3	2
X ₄	X ₅	X ₇	X ₆	0 ₂	1 ₆
X ₁₂	X ₁₃	X ₁₅	X ₁₄	0 ₁₅	0 ₁₄
X ₈	X ₉	0 ₁₁	0 ₁₀	0 ₁₀	0 ₁₁

$$D_B = \bar{A}\bar{B}X + \bar{A}B\bar{X}$$

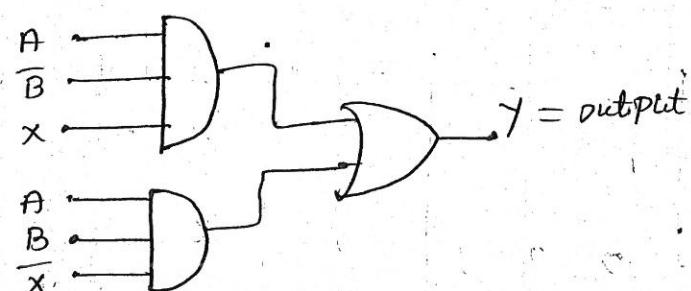
		$\bar{C}X$	$\bar{C}X$	CX	$C\bar{X}$
		$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
1	0	1	1	1	3
X ₄	X ₅	X ₇	X ₆	1 ₇	1 ₁
X ₁₂	X ₁₃	X ₁₅	X ₁₄	0 ₁₅	0 ₁₄
X ₈	X ₉	0 ₁₁	0 ₁₀	0 ₁₁	0 ₁₀

$$D_C = \bar{A}$$

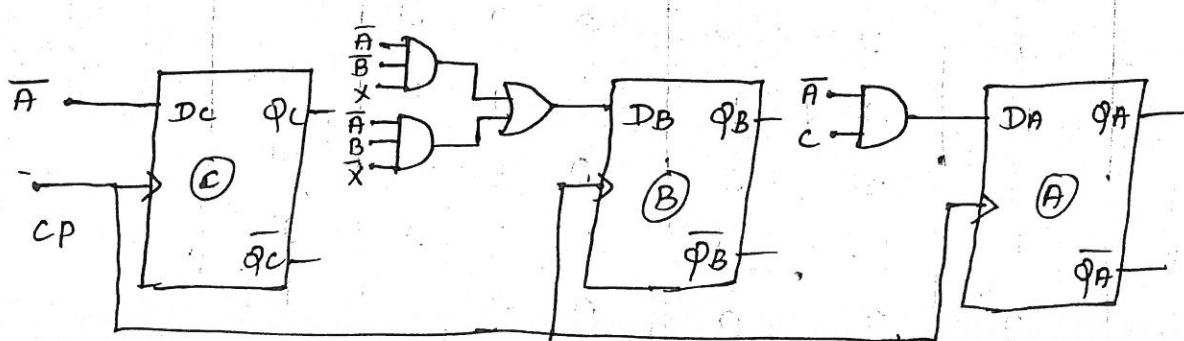
		$\bar{C}X$	$\bar{C}X$	CX	$C\bar{X}$
		$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
0	0	0	1	0	2
X ₄	X ₅	X ₇	X ₆	0 ₇	0 ₆
X ₁₂	X ₁₃	X ₁₅	X ₁₄	1 ₁₄	
X ₈	X ₉	X ₁₁	X ₁₀	0 ₁₀	0 ₁₁

$$Y = \bar{A}\bar{B}X + AB\bar{X}$$

Output (Y)

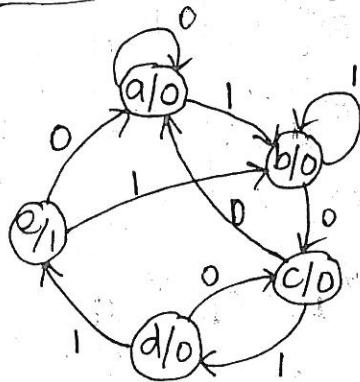


Logic Diagram



Draw the state diagram, write state transition table and design moore state machine using D-FF to detect the given sequence 1011.

State diagram:



State Table:-

Present State	Next state		output (Y)
	x=0	x=1	
a	a	b	0
b	c	b	0
c	a	d	0
d	c	e	0
e	a	b	1

State assignment: a=000, b=001, c=010, d=011, e=100.

State Transition Table:-

Present State (A B C)	Input X	Next state (A B C)	FF - Inputs (DA DB DC)	output (Y)
0 0 0	0	0 0 0	0 0 0	0
0 0 0	1	0 0 1	0 0 1	0
0 0 1	0	0 1 0	0 1 0	0
0 0 1	1	0 0 1	0 0 1	0
0 1 0	0	0 0 0	0 0 0	0
0 1 0	1	0 1 1	0 1 1	0
0 1 1	0	0 1 0	0 1 0	0
0 1 1	1	1 0 0	1 0 0	0
1 0 0	0	0 0 0	0 0 0	1
1 0 0	1	0 0 1	0 0 1	1

K-map simplification:-

DA

	$\bar{C}X$	$\bar{C}X$	CX	$C\bar{X}$
$\bar{A}\bar{B}$	0 ₀	0 ₁	0 ₃	0 ₂
$\bar{A}B$	0 ₄	0 ₅	1 ₇	0 ₆
$A\bar{B}$	X ₁₂	X ₁₃	X ₁₄	X ₁₅
AB	0 ₈	0 ₉	X ₁₁	X ₁₀

$$DA = BCX$$

Y

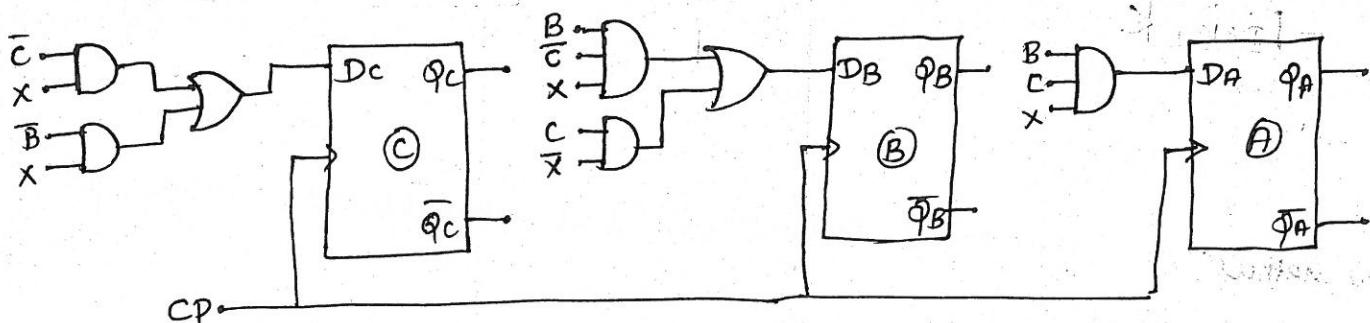
	$\bar{C}X$	$\bar{C}X$	CX	$C\bar{X}$
$\bar{A}\bar{B}$	0 ₀	0 ₁	0 ₃	0 ₂
$\bar{A}B$	0 ₄	0 ₅	0 ₇	0 ₆
$A\bar{B}$	X ₁₂	X ₁₃	X ₁₅	X ₁₄
AB	1 ₈	1 ₉	X ₁₁	X ₁₀

$$Y = A$$

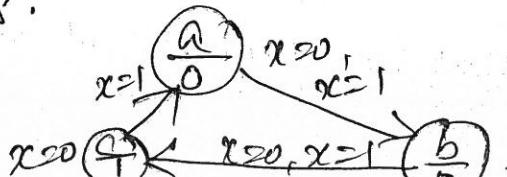
Output(y):-

$$A \rightarrow Y$$

Logic Diagram:-

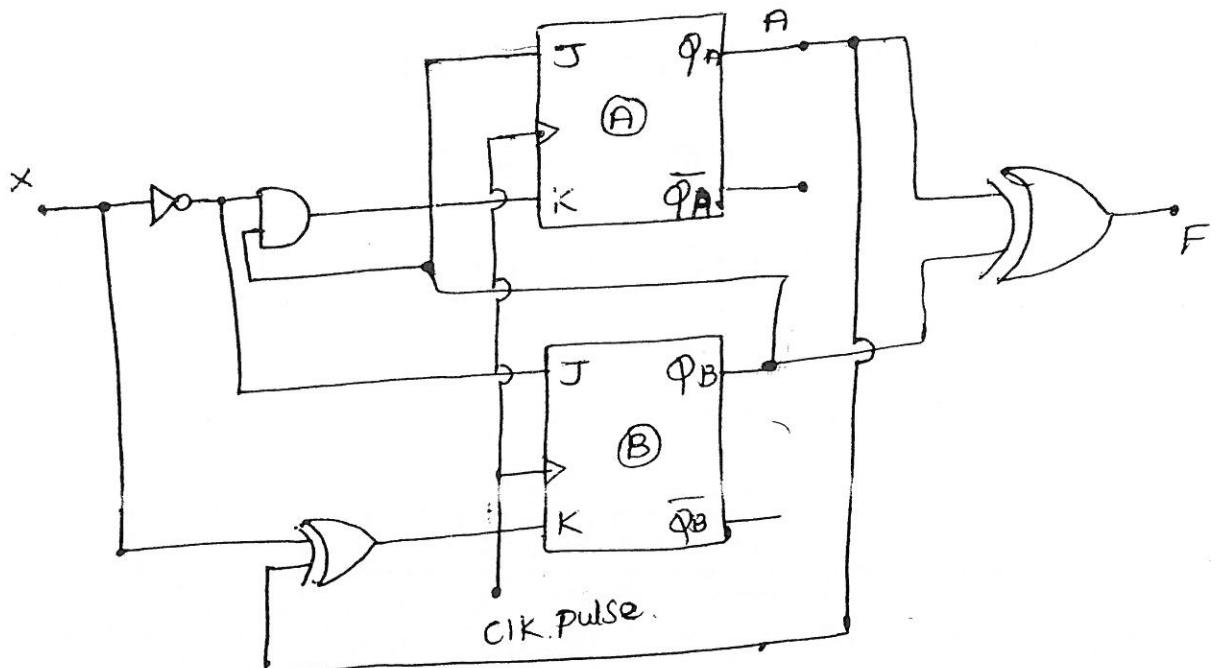


> Reduce the Sequential Circuit for the State diagram shown in fig.



Analysis of Sequential Circuit

Construct the transition table, state table and state diagram for the moore sequential circuit given below.



Soln:

Step 1: Determine flip flop input and output equations from the given sequential circuit.

$$F = A \oplus B$$

$$J_A = B, \quad K_A = \bar{X}B$$

$$J_B = \bar{X}, \quad K_B = X \oplus A$$

Characteristics Equation

$$\text{SR-FF: } Q_{n+1} = S + \bar{R}Q_n$$

$$\text{D-FF: } Q_{n+1} = D$$

$$\text{JK-FF: } Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

$$\text{T-FF: } Q_{n+1} = T\bar{Q}_n + \bar{T}Q_n$$

Step 2: Derive Next State Equations, [Given Seq. circuit is]

J-K FF

$$\varphi_{n+1} = J\bar{\varphi}_n + \bar{K}\varphi_n$$

$$\therefore A^+ = \varphi_A^+ \Rightarrow JA\bar{\varphi}_A + \bar{KA}\varphi_A$$

$$= B\bar{\varphi}_A + \bar{X}_B \cdot \varphi_A$$

$$= B\bar{\varphi}_A + (X + \bar{B})\varphi_A \Rightarrow$$

$$A^+ = \varphi_A^+ = B\bar{A} + XA + A\bar{B}$$

$$\therefore B^+ = \varphi_B^+ \Rightarrow JB\bar{\varphi}_B + \bar{KB}\varphi_B$$

$$\hookrightarrow XBA + \bar{X}B\bar{A} + XAB + (\cancel{XAB} + \cancel{A\bar{B}})$$

$$= \bar{X}\bar{\varphi}_B + \bar{X}\cancel{A}\varphi_B$$

$$B^+ = \varphi_B^+ \Rightarrow \bar{X}\bar{B} + XAB + \bar{X}\bar{A}B \rightarrow \begin{matrix} \bar{X}\bar{A}B \\ 0 \\ \end{matrix} + \begin{matrix} XAB \\ 1 \\ \end{matrix} + \begin{matrix} \bar{X}\bar{A}B \\ 2 \\ \end{matrix} + \begin{matrix} XAB \\ 3 \\ \end{matrix}$$

Step 3:- plot Next state mapping for each FF.

For A^+

	AB	00	01	11	10
X	0	0	1	0	1
	1	0	1	1	1

For B^+

	AB	00	01	10	11
X	0	1	1	0	1
	1	0	0	1	0

P4:- plot transition table

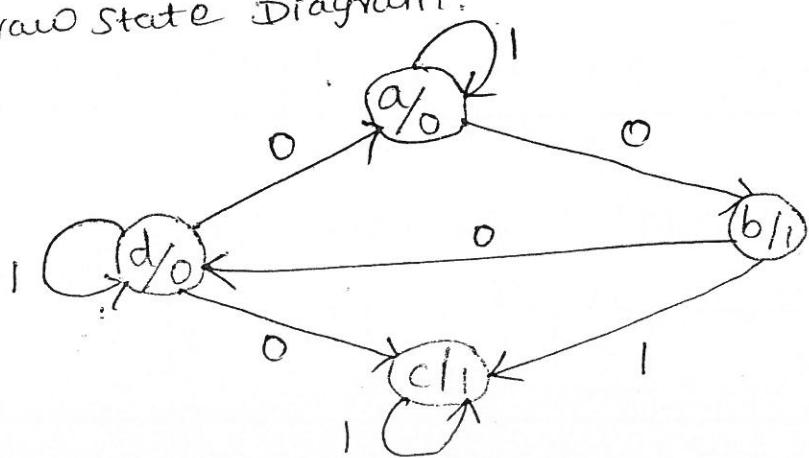
[By combining the above 2
next state mapping]

Present State	Next state.		Output $F = (A \oplus B)$
	$x=0$	$x=1$	
A B	$A + B^+$	$A + B^+$	
0 0	0 1	0 0	0
0 1	1 1	1 0	1
1 0	1 1	1 0	1
1 1	0 0	1 1	0

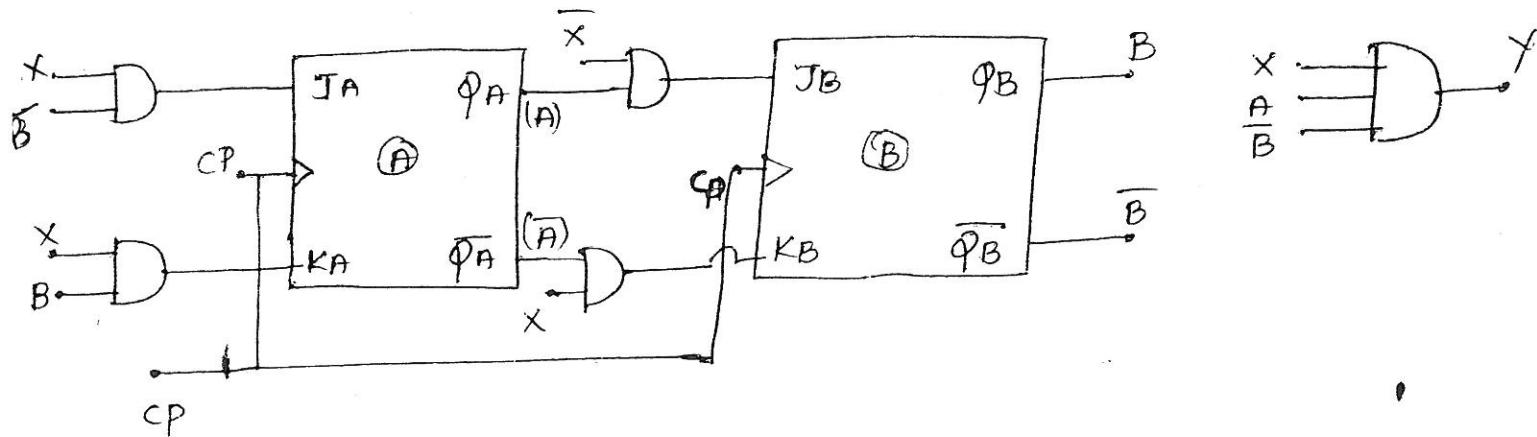
Step 5: State Table, [Assigning From Transition Table
 $a=00, b=01, c=10, d=11$]

present state (AB)	Next state		output
	$x=0$ $A + B^+$	$x=1$ $A + B^+$	(F)
a	b	a	0
b	d	c	1
c	d	c	1
d	a	d	0

Step 6: Draw State Diagram.



construct the transition Table, state table and state diagram for the mealy sequential circuit.



Soln:-

Step 1 :- Determine the FF input and outputs from the given circuit.

$$Y = XAB, \quad J_A = X\bar{B}, \quad K_A = \bar{X}B, \quad J_B = \bar{A}X, \quad K_B = \bar{A}X$$

Step 2 :- Derive next state equation, [J-K FF]

$$\text{characteristics eqn is, } (Q_{n+1}) = J\bar{Q}_n + \bar{K}Q_n.$$

$$\begin{aligned} Q_A^{n+1} \Rightarrow A^{n+1} &= J_A \bar{Q}_A + \bar{K}_A Q_A \\ &= X\bar{B}\bar{Q}_A + \bar{X}B Q_A \\ &= X\bar{B}\bar{A} + (X+\bar{B})A \end{aligned}$$

$Q_A^{n+1} = A^{n+1} = X\bar{B}\bar{A} + XA + \bar{A}B.$
$\begin{matrix} 1 & 0 & 0 \\ XAB & X\bar{A}B & X\bar{A}\bar{B} \\ 1 & 1 & 0 \end{matrix}$

$$\begin{aligned} Q_B^{n+1} &= B^{n+1} = J_B \bar{Q}_B + \bar{K}_B Q_B \\ &= A\bar{X}\bar{B} + (\bar{A}X)B \\ &= A\bar{X}\bar{B} + (A+\bar{X})B \end{aligned}$$

$B^{n+1} = A\bar{X}\bar{B} + AB + BX.$
--

Step 3 : Next State mapping for each FF

For A^t

X\bar{A}B	00	01	11	10
0	0	0	0	1
1	1	0	1	1

For B^t

X\bar{A}B	00	01	11	10
0	0	1	1	1
1	0	0	1	0

Step 4: plot Transition Table,

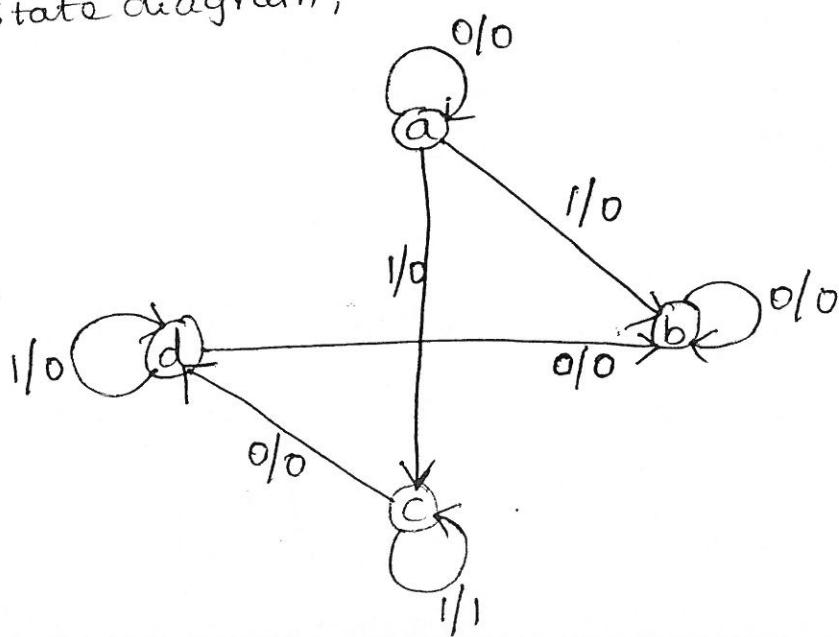
Present state (AB)	Next state		Output	
	$x=0$ $A+B^+$	$x=1$ $A+B^+$	$y = A\bar{B}X$ $x=0 \quad x=1$	
00	00	10	0 0	
01	01	00	0 0	
10	11	10	0 1	
11	01	11	0 0	

Step 5: plot State Table

Assign values, $a = 00, b = 01, c = 10, d = 11$

Present state (AB)	Next state		Output (y) $A+B^+$
	$x=0$ $A+B^+$	$x=1$ $A+B^+$	
a	a	c	0 0
b	b	a	0 0
c	d	c	0 1
d	b	d	0 0

Step 6: State diagram,



3) A sequential circuit with 2-D-FF's \rightarrow A and B and inputs X and output Y is specified by the following next state and output equations,

$$A(t+1) = AX + BX$$

$$B(t+1) = \bar{A}X$$

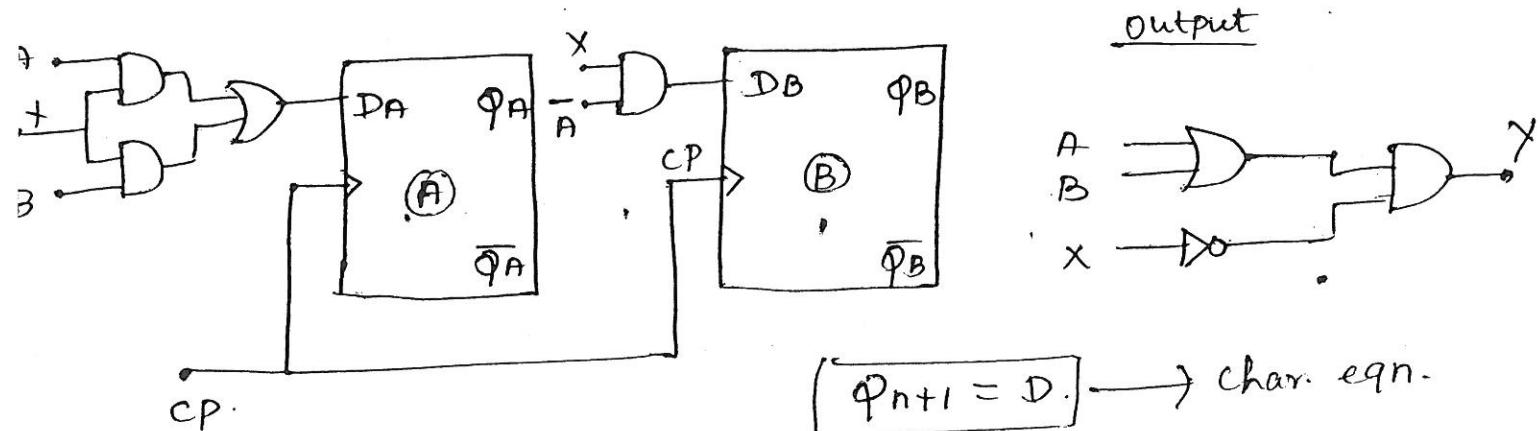
$$Y = (A+B)\bar{X}$$

(i) Draw the logic diagram of the circuit

(ii) Derive the State Table

(iii) Plot State Diagram.

Soln: (i) Logic diagram,



(ii) State Table mapping

		AB			
		00	01	11	10
X	0	0	0	0	0
	1	0	1	1	1

		AB			
		00	01	11	10
X	0	0	0	0	0
	1	1	1	0	0

transition Table

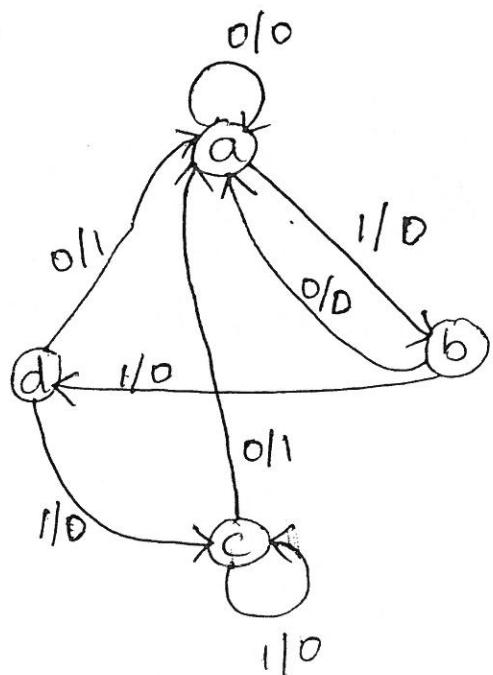
Present state AB	Next state		output (Y)	
	X=0 $A+B^+$	X=1 $A+B^+$	X=0	X=1
			!	!
00	00	01	0	0
01	00	11	1	0
10	00	10	1	0
11	00	10	1	0

State Table

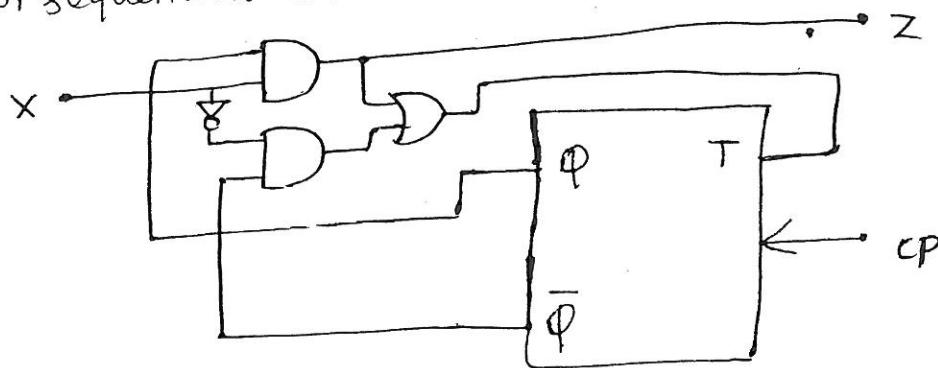
Let, $a = 00$, $b = 01$, $c = 10$, $d = 11$

present state (ab)	Next state		output	
	X=0 $a+b^+$	X=1 $a+b^+$	(Y) X=0	X=1
			0	0
a	a	b	0	0
b	a	d	1	0
c	a	c	1	0
d	a	c	1	0

(iii) State diagram



) Construct transition table, State table & state diagram for sequential circuit.



Soln:-

Step 1: Determine the FF input and output for the given circuit.

$$T_A = X\bar{Q}_A + \bar{X}\bar{\bar{Q}}_A$$

$$Z = Q_A \bullet X$$

Step 2: Derive the next state equations [for T-FF]

$$Q^+ = T\bar{Q} + \bar{T}Q$$

$$Q_A^+ = T_A\bar{Q}_A + \bar{T}_A\bar{Q}_A$$

$$= (X\bar{Q}_A + \bar{X}\bar{\bar{Q}}_A) \oplus Q \quad (\text{simplify})$$

$Q_A^+ = (\bar{X}\bar{Q}_A + \bar{X}Q_A)$

Step 3: Plot Next state mapping for each FF.

For Q_A^+

Q_A	X	0	1
0		1	0
1		1	0

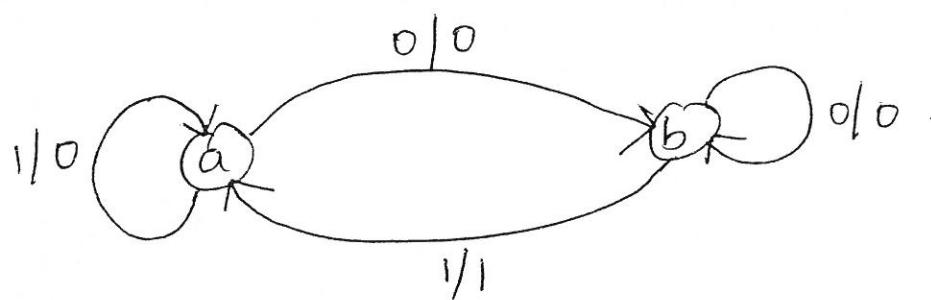
Step 4: plot Transition table

present state (q_A)	Next state		output (Z)	
	$x=0$ (q_A^+)	$x=1$ (q_A^+)	$x=0$	$x=1$
0	1	0	0	0
1	1	0	0	1

Step 5: State Table. [Assign, $a=0, b=1$]

present state (q_A)	Next state		output (Z)	
	$x=0$ (q_A^+)	$x=1$ (q_A^+)	$x=0$	$x=1$
a	b	a	0	0
b	b	a	0	1

Step 6: State diagram.



Unit - III - Asynchronous Sequential Circuits

Asynchronous Sequential Circuit.

the change of internal state occurs when there is a change in input variables.

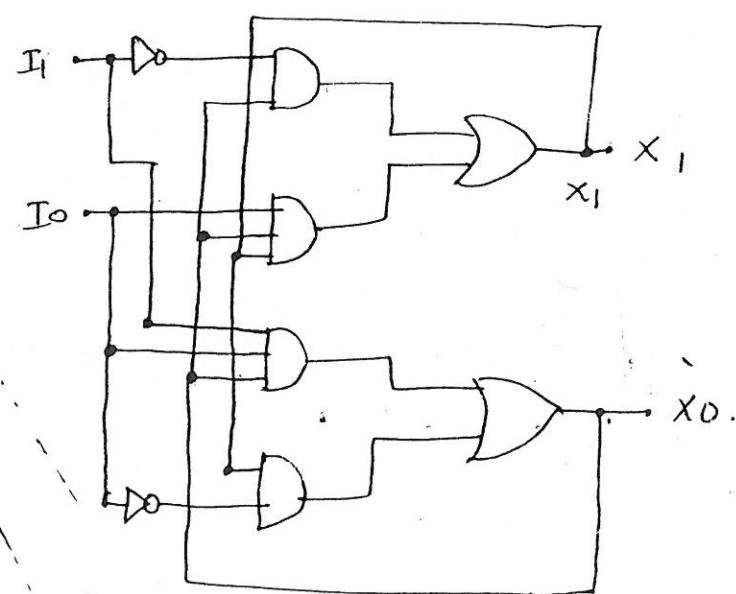
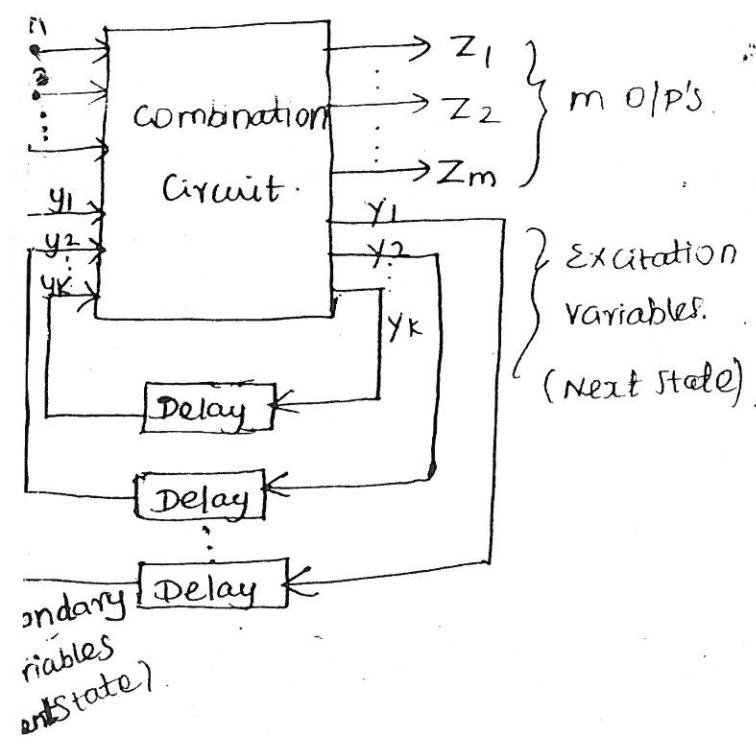
3/p

- The memory elements in asynchronous seq. circuits are either unclocked FF (or) Time delay elements.

These circuits are used in circuits where the speed of operation is more.

Block Diagram:-

Eg:-



no methods.

7 - 9

2 -

Fundamental mode circuit

Pulse mode circuit.

It consists of combinational logic circuit and delay elements connected form feedback loops.

K-map simplification :-

DA

	$\bar{C}\bar{X}$	$\bar{C}X$	CX	$C\bar{X}$
$\bar{A}\bar{B}$	0 ₀	0 ₁	0 ₃	0 ₂
$\bar{A}B$	0 ₄	0 ₅	1 ₇	0 ₆
$A\bar{B}$	X ₁₂	X ₁₃	X ₁₄	X ₁₅
AB	0 ₈	0 ₉	X ₁₁	X ₁₀

$$DA = BCX$$

Y

	$\bar{C}\bar{X}$	$\bar{C}X$	CX	$C\bar{X}$
$\bar{A}\bar{B}$	0 ₀	0 ₁	0 ₃	0 ₂
$\bar{A}B$	0 ₄	0 ₅	0 ₇	0 ₆
$A\bar{B}$	X ₁₂	X ₁₃	X ₁₅	X ₁₄
AB	1 ₈	1 ₉	X ₁₁	X ₁₀

$$Y = A$$

DB

	$\bar{C}\bar{X}$	$\bar{C}X$	CX	$C\bar{X}$
$\bar{A}\bar{B}$	0 ₀	0 ₁	0 ₃	1 ₂
$\bar{A}B$	0 ₄	1 ₅	0 ₇	1 ₆
$A\bar{B}$	X ₁₂	X ₁₃	X ₁₄	X ₁₅
AB	0 ₈	0 ₉	X ₁₁	X ₁₀

$$DB = B\bar{C}X + C\bar{X}$$

DC

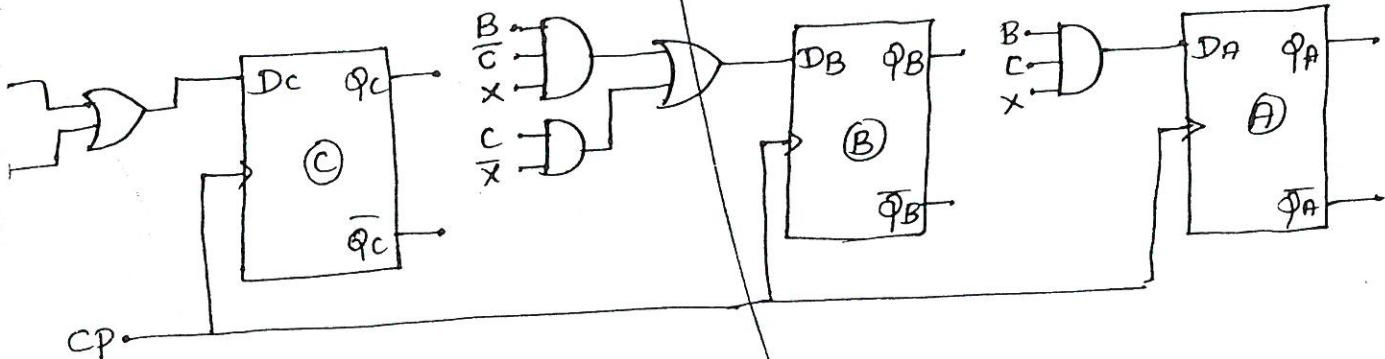
	$\bar{C}\bar{X}$	$\bar{C}X$	CX
$\bar{A}\bar{B}$	0 ₀	1 ₁	1 ₃
$\bar{A}B$	0 ₄	1 ₅	0 ₇
$A\bar{B}$	X ₁₂	X ₁₃	X ₁₄
AB	0 ₈	1 ₉	X ₁₁

~~$$DC = \bar{C}X + \bar{B}X$$~~

Output(y) :-



Logic Diagram :-



- There are n -input variables and m -output variables and k -internal states.
- We can consider the delay elements are providing short term memory for the sequential circuit.
- In gate type circuit, the propagation delay that exists in the combinational circuit path from input to output provides sufficient delay along the feedback loop, so that no specific elements are actually inserted in the feedback path.
- Present state as → secondary variables and, Next state as → excitation variables.
- In steady state condition excitation and secondary variables are same, but during transition they are difficult.

Fundamental mode circuit:-

The i/p variables change only when the circuit is stable.

only one input variable can change at a given ^{instant.} time.

Input are levels and not pulses.

Iso mode circuit:-

Input variables are pulses instead of levels.

The width of the pulse is long enough for the circuit to respond to the i/p. The pulse width must not be so long that it is still present after the new state is reached.

Problems on Analysis of Asynchronous Sequential Circuit

An asynchronous sequential circuit has 2 internal states and one output. the excitation and output function describing the circuit as follows,

$$y_1 = x_1 x_2 + x_1 y_2 + x_2 y_1$$

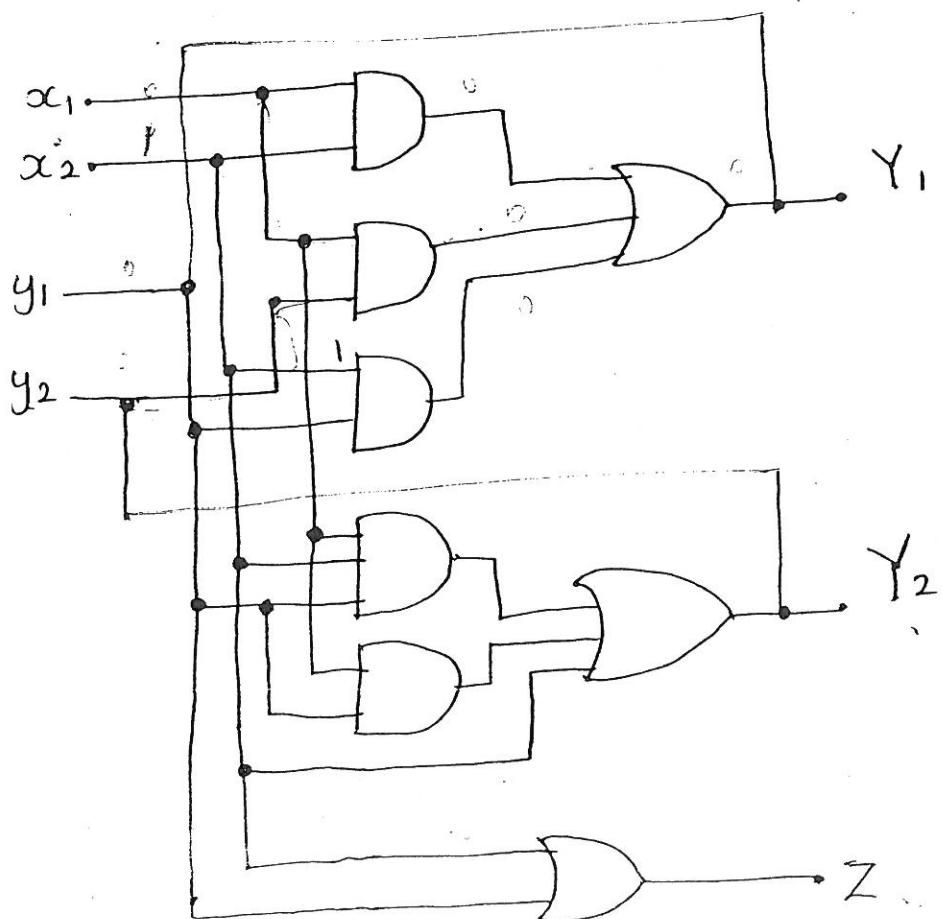
$$y_2 = x_2 + x_1 y_1 y_2 + x_1 y_1$$

$$z = x_2 + y_1$$

) Draw the logic diagram of the circuit, (i) Derive the transition table and output map.

Oln:-

Logic Diagram



Truth Table

Present States (Both input & present)				Next State	Stable state Yes/No.	Output (Z)
x_1	x_2	y_1	y_2	y_1	y_2	
0 0	0 0	0	0	0	0	0
0 0	0 1	0	0	0	0	0
0 0	1 0	0	0	0	0	1
0 0	1 1	0	0	0	0	1
0 1	0 0	0	1	0	0	1
0 1	0 1	0	1	0	1	1
0 1	1 0	1	1	1	0	1
0 1	1 1	1	1	1	1	1
1 0	0 0	0	0	0	1	0
1 0	0 1	1	0	1	0	0
1 0	1 0	0	1	0	1	1
1 0	1 1	1	1	1	1	1
1 1	0 0	1	1	1	0	1
1 1	0 1	1	1	1	0	1
1 1	1 0	1	1	1	0	1
1 1	1 1	1	1	1	1	1

Transition table map

sent at y ₂	x ₁ , x ₂ (Input state)	y ₁ , y ₂ (Output state)			
		00	01	11	10
00	00	00	01	11	00
01	00	01	11	10	-
11	00	11	11	11	01
10	00	11	11	01	-

Output map

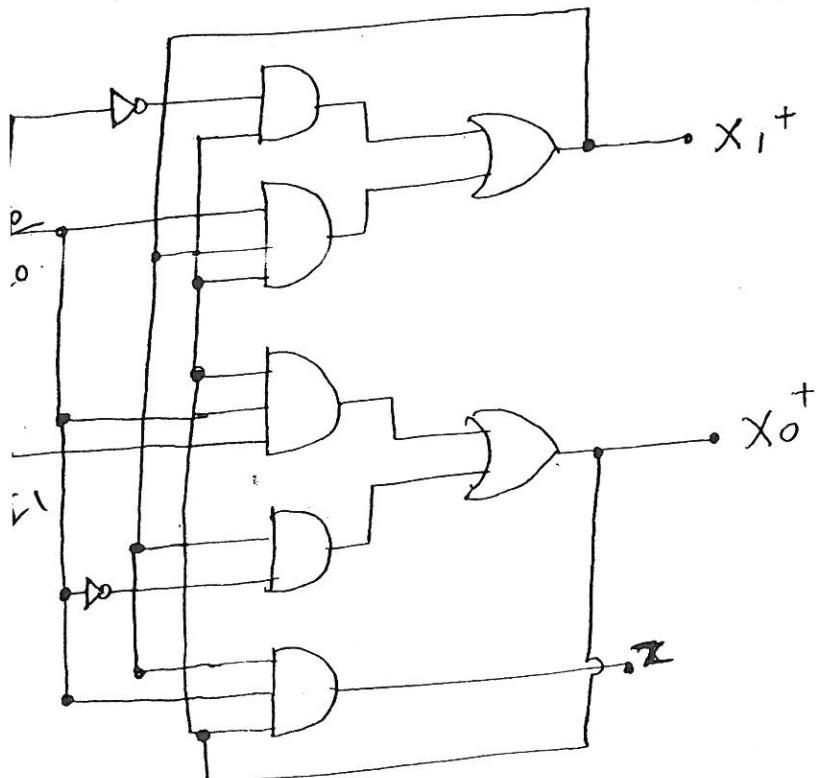
y ₁ , y ₂	x ₁ , x ₂			
	00	01	11	10
00	0	-	-	0
01	-	1	-	-
11	-	1	1	1
10	-	-	-	-

1 An asynchronous sequential circuit as described by the following excitation + output function.

$$\begin{aligned} x_1^+ &= x_0 \bar{x}_1 + x_0 x_1 I_{10} \\ x_0^+ &= x_0 I_{10} x_1 + x_1 \bar{I}_{10} \\ z &= x_0 x_1 I_{10} \end{aligned} \quad \left. \begin{array}{l} \text{→ Draw the logic diagram of circuit} \\ \text{& Derive transition table & output map} \end{array} \right\}$$

2:-

Logic diagram:-



transition K-map Table

I_{10}	00	01	11	10
00	00	00	00	00
10	10	10	01	00
(11)	10	(11)	01	
01	00	00	01	

Output Table map

I_{10}	00	01	11	10
00	0	0	0	0
01	-	-	0	-
11	0	-	1	-
10	-	-	-	-

Truth Table

Present State Table		Next states	Stable state yes/no	Output (z)
$x_1 x_0$	$I_1 I_0$	$x_1^+ x_0^+$		
00	00	00	yes	0
00	01	00	yes	0
00	10	00	yes	0
00	11	00	yes	0
01	00	10	no	0
01	01	10	no	0
01	10	01	yes	0
01	11	00	no	0
10	00	11	yes	0
10	01	10	no	1
10	10	11	yes	1
10	11	01	no	0
11	00	01	no	0
11	01	00	no	0
11	10	00	no	0
11	11	01	no	0

An asynchronous sequential circuit is described by the following excitation & output function.

$$Y = x_1 x_2 + (x_1 + x_2) Y$$

$$Z = Y$$

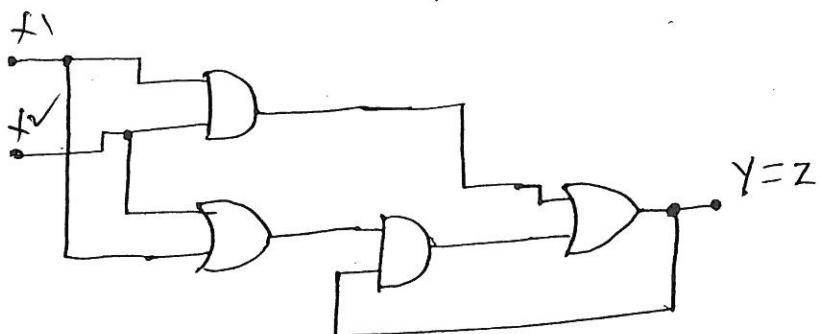
- } {
- (i) Draw logic diagram of circuit.
 - (ii) Derive the transition table & output map.

73, 89, 133, 161, 173, 191

233, 234, 245, 246, 273, 28

205, 313, 321

Logic diagram :-



Truth Table :-

Present State.	Next State (Y)	Stable total State. Yes / No	(Output) Z.
$x_1 \ x_2 \ y$			
0 0 0	0	yes	0
0 0 1	0	No	0
0 1 0	0	yes	0
0 1 1	1	yes	1
1 0 0	0	yes	0
1 0 1	1	yes	1
1 1 0	1	No	1
1 1 1	1	yes.	1

transition Table

y	$x_1 x_2$			
	00	01	11	10
0	0	0	1	0
1	0	1	1	1

Output Map.

y	$x_1 x_2$			
	00	01	11	10
0	0	0	-	0
1	-	1	1	1

Design of Asynchronous sequential circuit:-

- Draw the state diagram for the given problem statement.
- Then construct primitive flow table from the state diagram (or) problem statement
- State assignment is made (only binary values).
- The primitive flow table is realised using appropriate logic elements.

(1) Design an asynchronous sequential circuit with 2 inputs x and y , and one output z . Whenever y is 1, input x is transferred to z . When y is 0, the output does not change for any change in x .

Soln:-

$$xy = 00, z = 0.$$

$$y=1 \Rightarrow \boxed{x=z}$$

$$y=0 \Rightarrow \boxed{z = \text{No change}}$$

$$\boxed{\text{State A}} \Rightarrow xy = 00, z = 0 \rightarrow \textcircled{A}$$

$$xy = 01, z = 0 \rightarrow \textcircled{B}$$

$$xy = 10, z = 0 \rightarrow \textcircled{C}$$

$$\boxed{\text{State B}} \Rightarrow xy = 01, z = 0 \rightarrow \textcircled{B}$$

$$xy = 00, z = 0 \rightarrow \textcircled{A}$$

$$xy = 11, z = 1 \rightarrow \textcircled{D}$$

$$\boxed{\text{State C}} \Rightarrow xy = 10, z = 0 \rightarrow \textcircled{C}$$

$$xy = 00, z = 0 \rightarrow \textcircled{A}$$

$$xy = 11, z = 1 \rightarrow \textcircled{D}$$

$$\boxed{\text{State D}} \Rightarrow xy = 11, z = 1 \rightarrow \textcircled{D}$$

$$xy = 10, z = 1 \rightarrow \textcircled{E}$$

$$xy = 01, z = 0 \rightarrow \textcircled{B}$$

$$\boxed{\text{State F}} \Rightarrow xy = 00, z = 1 \rightarrow$$

$$xy = 01, z = 0 \rightarrow$$

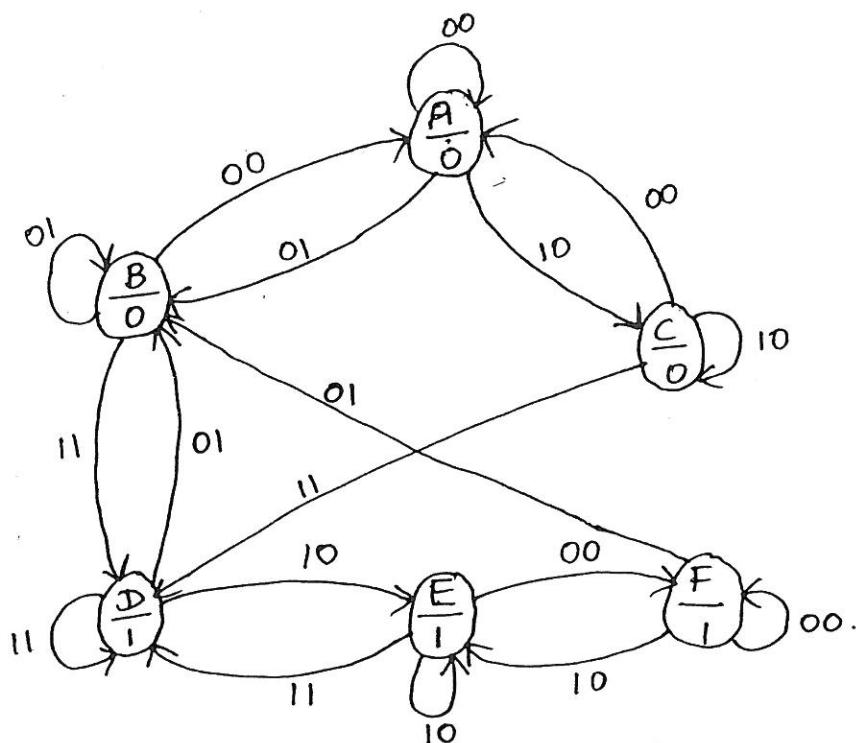
$$xy = 10, z = 1 \rightarrow$$

$$\boxed{\text{State E}} \Rightarrow xy = 10, z = 1 \rightarrow \textcircled{E}$$

$$xy = 00, z = 1 \rightarrow \textcircled{F}$$

$$xy = 11, z = 1 \rightarrow \textcircled{D}$$

State Diagram :-



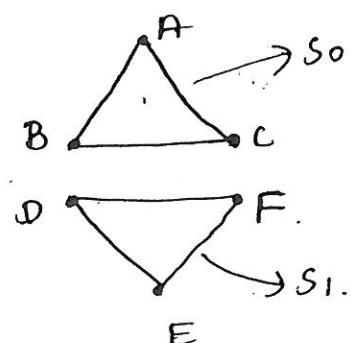
Reduced Primitive Table.

Present State(F)	Next state and output.			
	(xy) 00	(xy) 01	(xy) 10	(xy) 11
(A,B,C)	(B,10)	(B,10)	(C,0)	D,-
(D,E,F)	(F,11)	B,-	(E,11)	(D,11)

Primitive Flow Table :-

Present State. (F).	Next State, Output z for xy inputs.			
	00.	01	10	11
A	(A,10)	B,-	C,-	-,-
B	A,-	(B,0)	-,-	D,-
C	A,-	-,-	(C,0)	D,-
D	-,-	B,-	E,-	(D,1)
E	F,-	-,-	(E,1)	D,-
F	(F,11)	B,-	E,-	-,-

→ For reducing primitive flow table → Use merger graph.



$$(A, B, C) \rightarrow S_0$$

$$(D, E, F) \rightarrow S_1.$$

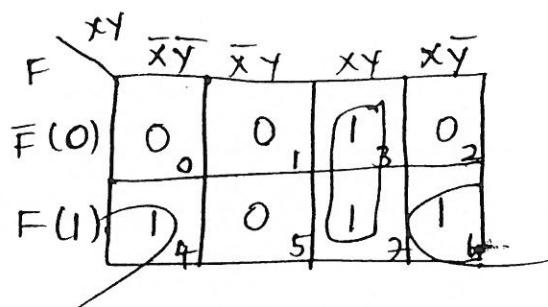
State assignment $\rightarrow S_0 = 0, S_1 = 1$.

Reduced primitive flow Table :-

Present State (F)	Next State & output Z for input xy.			
	(xy) 00	(xy) 01	(xy) 10	(xy) 11
(S ₀) 0	S ₀ 0, 0	S ₀ 0, 0	S ₀ 0, 0	S ₁ 1, -
(S ₁) 1	S ₁ 1, 1	S ₀ 0, -	S ₁ 1, 1	S ₁ 1, 1

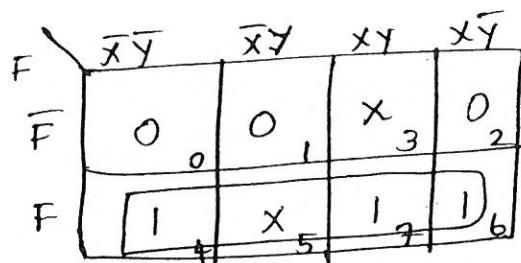
K-map Simplification :-

For Next state



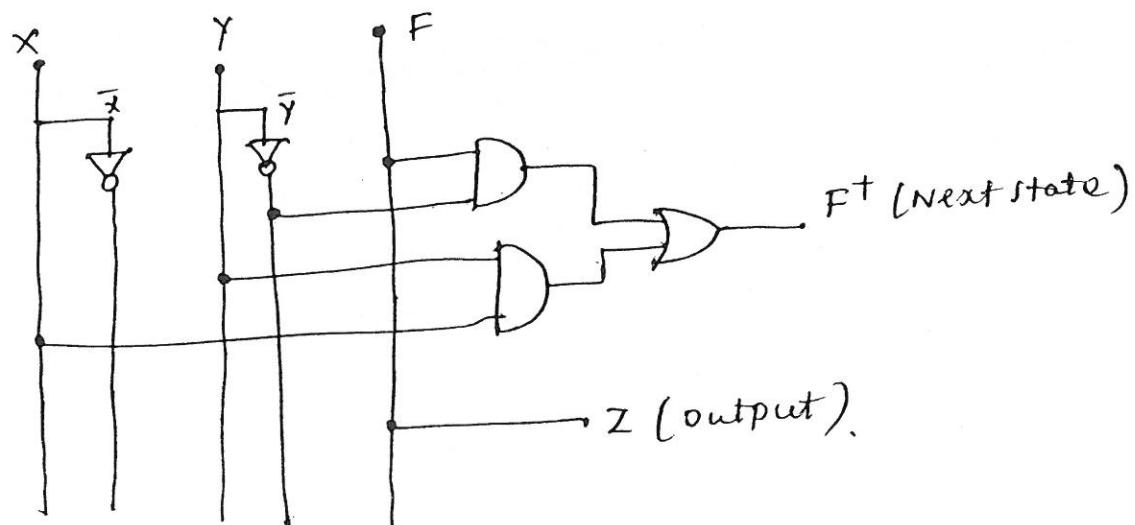
$$F^+ = F\bar{Y} + XY$$

for output Z



$$Z = F$$

Logic Diagram :-



2)

Design an asynchronous sequential circuit that has 2 inputs x and y , and a single output z which is to behave in the following manner. Initially both i/p's & o/p are zero. Whenever $x=1$ & $y=0$, z becomes 1 and whenever $x=0$ & $y=1$, z becomes 0. When inputs are zero or one ($x=y=0$, $x=y=1$), the output z does not change (It remains in the previous state) static input values are not to have any effect in changing the z -output. The logic s/m changes state on the rising edges of the 2 inputs.

Soln:-

Initial condition, $xy=00, z=0 \rightarrow A$.

State-A: $xy=00, z=0 \rightarrow A$

$xy=01, z=0 \rightarrow B$

$xy=10, z=1 \rightarrow C$.

conditions,

$x=0, y=1, z=0$

$x=1, y=0, z=1$

$x=1, y=1, z=0$

$x=0, y=0, z=1$

no change

State-B:

$xy=01, z=0 \rightarrow B$

$xy=00, z=0 \rightarrow A$

$xy=11, z=0 \rightarrow D$

State-C:

$xy=10, z=1 \rightarrow C$

$xy=00, z=1 \rightarrow E$

$xy=11, z=1 \rightarrow F$

State-D:

$xy=11, z=0 \rightarrow D$

$xy=10, z=1 \rightarrow C$

$xy=01, z=0 \rightarrow B$

State - E: $XY = 00, Z = 1 \rightarrow (E)$

$XY = 01, Z = 0 \rightarrow (B)$

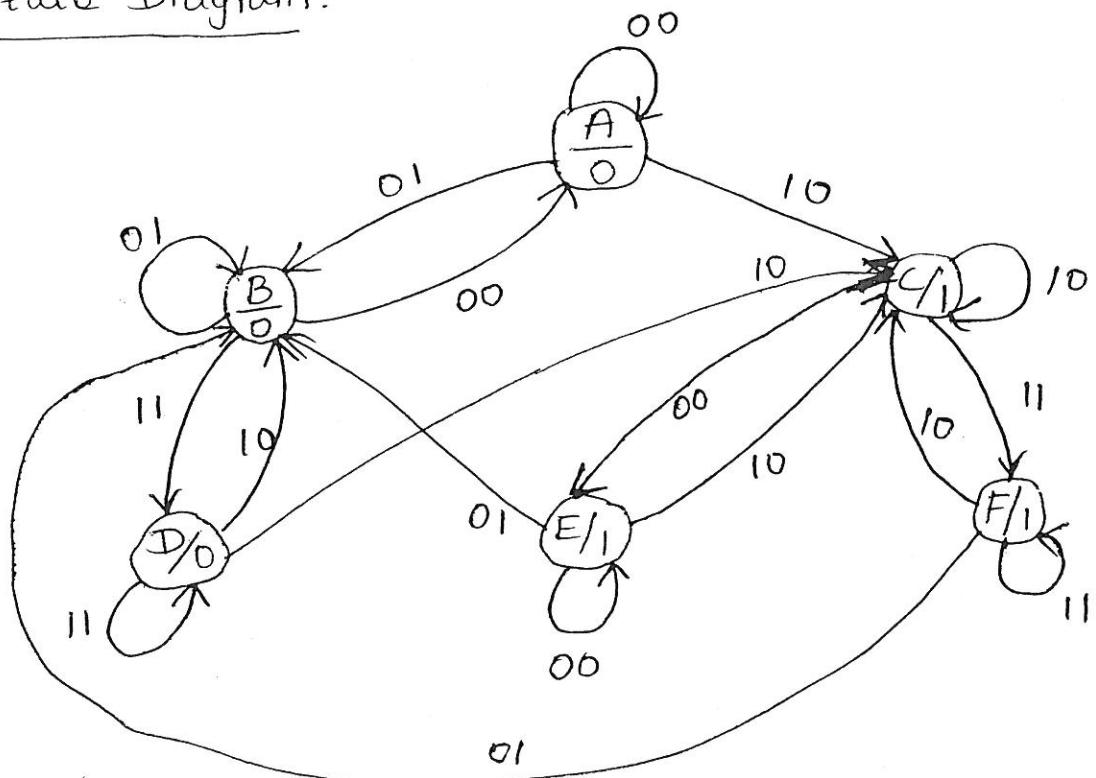
$XY = 10, Z = 1 \rightarrow (D)$

State - F: $XY = 11, Z = 1 \rightarrow (F)$

$XY = 10, Z = 1 \rightarrow (C)$

$XY = 01, Z = 0 \rightarrow (B)$

State Diagram:



Primitive Flow Table

Present State (F)	Next state, o/p(z) for inputs xy			
	00	01	10	11
A	(A, 0)	B, -	C, -	-, -
B	A, -	(B, 0)	-, -	D, -
C	E, -	-, -	(C, 1)	F, -
D	-, -	B, -	C, -	(D, 0)
E	(E, 1)	B, -	C, -	-, -
F	-, -	B, -	C, -	(F, 1)

non-critical :- → If final stable state that the circuit reaches does not depend on the order in which state variable changes it is not harmful & is called non-critical.

critical :- → If final stable state depends on the order in which the state variable changes, the race condition is harmful and is called critical.

→ non-critical cases must be avoided for proper operation.

Cycles :- → A cycle occurs when an asynchronous circuit makes transition through a series of unstable states.

Design an asynchronous sequential circuit that has 2 inputs x_2 and x_1 , and one output Z . When $x_1=0$ the output Z is 0. The first change in x_2 that occurs while x_1 is 1 will cause output Z ~~will remain 1~~ ^{is 1, op Z will} remain 1 while x_1 returns to 0.

Soln:- Input initial conditions $x_2x_1=00$, $Z=0$. — (A)
conditions, $x_1=0$, $\Rightarrow Z=0$.

State-A: $x_2x_1=00$, $Z=0$ — (A)

$x_2x_1=01$, $Z=0$ — (B)

$x_2x_1=10$, $Z=0$ — (C)

State-B: $x_2x_1=01$, $Z=0$ — (B)

$x_2x_1=11$, $Z=1$ — (D)

$x_2x_1=00$, $Z=0$ — (A)

State - C

$x_2x_1 = 10, z = 0 \longrightarrow C$

$x_2x_1 = 11, z = 0 \longrightarrow E$

$x_2x_1 = 00, z = 0 \longrightarrow A$

State - D

$x_2x_1 = 11, z = 1 \longrightarrow D$

$x_2x_1 = 01, z = 1 \longrightarrow F$

$x_2x_1 = 10, z = 0 \longrightarrow C$

State - E

$x_2x_1 = 11, z = 0 \longrightarrow E$

$x_2x_1 = 01, z = 1 \longrightarrow F$

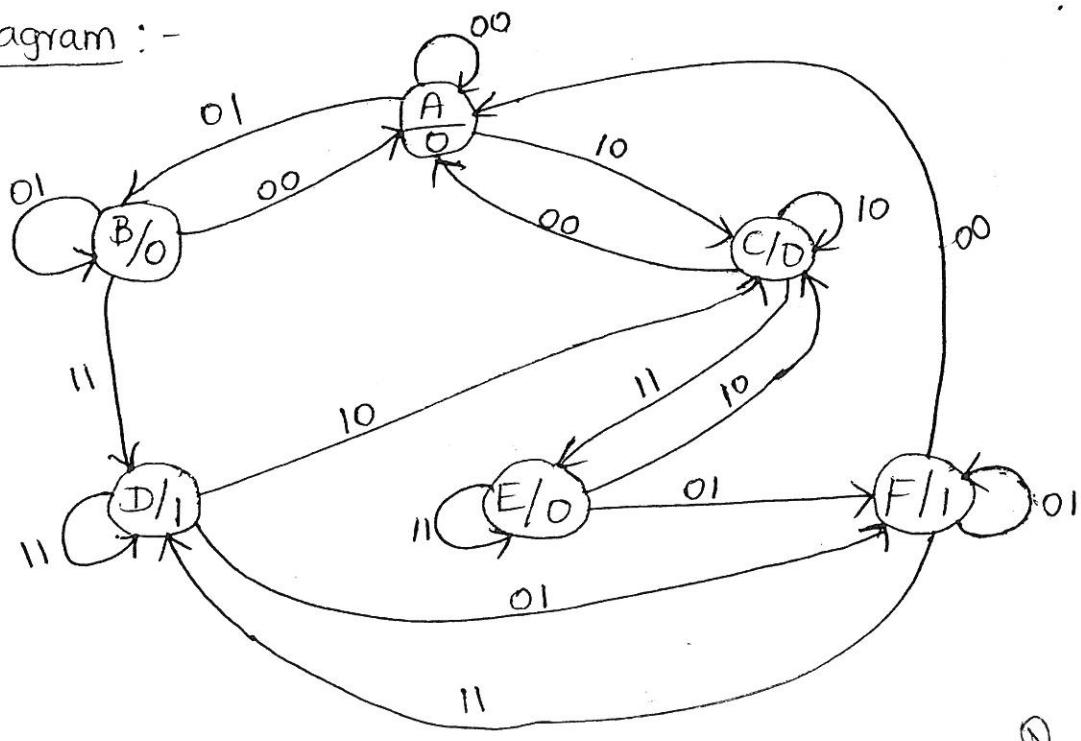
$x_2x_1 = 10, z = 0 \longrightarrow C$

State - F :-

$x_2x_1 = 01, z = 1 \longrightarrow F$

$x_2x_1 = 00, z = 0 \longrightarrow A$

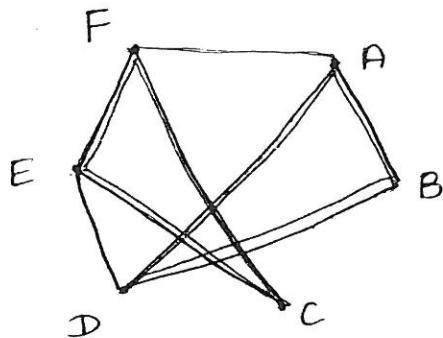
$x_2x_1 = 11, z = 1 \longrightarrow D$

State Diagram :-

(2)

Merger Graph

→ To reduce the primitive Flow Table.



$$① \Rightarrow A, B, D \Rightarrow S_0$$

$$② \Rightarrow C, E, F \Rightarrow S_1$$

Reduced primitive Flow Table

present State	Next state, O/P(Z) for XY			
(F)	00	01	10	11
S_0	$S_0, 0$	$S_0, 0$	$S_1, -$	$S_0, 0$
S_1	$S_1, 1$	$S_0, -$	$S_1, 1$	$S_1, 1$

Let, $S_0 = 0, S_1 = 1$.

Present State	Next state, O/P for XY			
(F)	00	01	10	11
0	0, 0	0, 0	1, -	0, 0
1	1, 1	0, -	1, 1	1, 1

K-map Simplification,

	$\bar{X}\bar{Y}$	$\bar{X}Y$	XY	$X\bar{Y}$
F for F^+	\bar{F}	0	0	1
F	1	0	1	0

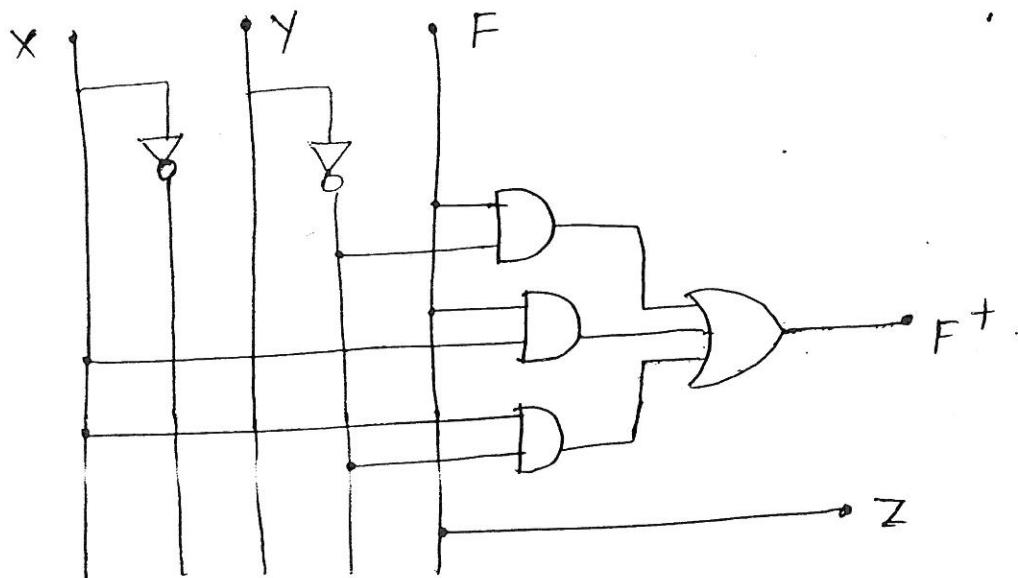
$$F^+ = F\bar{Y} + F\bar{X} + X\bar{Y}$$

For - Z

	$\bar{x}\bar{y}$	$\bar{x}y$	$x\bar{y}$	xy
F	0	0	0	X
F	1	X	1	1

$$Z = F$$

Logic Diagram :



Problems in Asynchronous Circuit:

- (i) Races ↗ Non-critical
 ↘ critical.
- (ii) cycles
- (iii) Hazards.

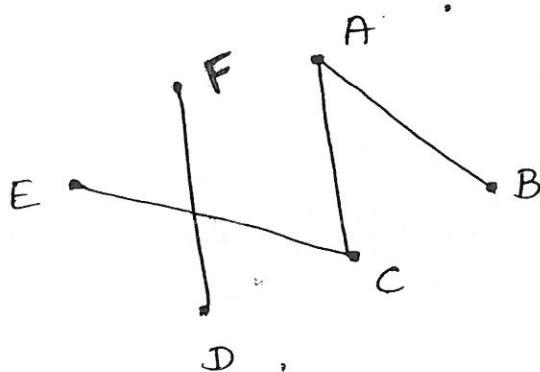
Races → When 2 (or) more binary state variables change their value in response to change in input variables it is called race condition.

Races ↗ Critical Race
 ↘ Non-critical Race.

Primitive Flow Table :-

Present State (F)	Next state, output (Z) for XY.			
	00	01	10	11
A	(A), 0	B, -	C, -	-, -
B	A, -	(B), 0	-, -	D, -
C	A, -	-, -	(C), 0	E, -
D	-, -	F, -	C, -	(D), 1
E	-, -	F, -	C, -	(E), 0
F	A, -	(F), 1	-, -	D, -

Moser Graph :-



$(A, B) \rightarrow S_0 (00)$ } \rightarrow From moser graph gives 2 compatible
 $(C, E) \rightarrow S_1 (01)$ } pairs of as a sets of maximum
 $(D, F) \rightarrow S_2 (10)$ } compatabilities.

Reduced primitive Flow Table :-

Present State (F)	Next state, output (Z) for XY			
	00	01	10	11
00 S0	(S0), 0	(S0), 0	S1, -	S2, -
01 S1	S0, -	S3, -	(S1), 0	(S1), 0
10 S2	S0, -	(S2), 1	S1, - S3, -	(S2), 1
11 S3	-, -	S2, -	S1, -	-, -

Let, S0 = 00

$$\left. \begin{array}{l} \{ S_1 = 01 \\ S_2 = 10 \} \\ S_3 = 11 \end{array} \right\}$$

→ S3 can be find by comparing S1(01) and S2(10).

→ Critical racing may occurs while changing from 10 to 01 (or) 01 to 10

Reduced primitive Flow Table :-

Present state (F) (F2 F1)	Next state, O/P (Z) for XY			
	00	01	10	11
00	(00), 0	(00), 0	01, -	10, -
01	00, -	11, -	(01), 0	(01), 0
10	00, -	(10), 1	11, -	(10), 1
11	-, -	(10), -	01, -	-, -

K-map Simplification

For F_2^+

	$\bar{x}_2\bar{x}_1$	\bar{x}_2x_1	$x_2\bar{x}_1$	x_2x_1
$\bar{F}_2\bar{F}_1$	0	0	1	0
\bar{F}_2F_1	0	1	0	0
$F_2\bar{F}_1$	x	1	x	0
$F_2\bar{F}_1$	0	1	1	1

For F_1^+

	$\bar{x}_2\bar{x}_1$	\bar{x}_2x_1	$x_2\bar{x}_1$	x_2x_1
$\bar{F}_2\bar{F}_1$	0	0	0	1
\bar{F}_2F_1	0	1	1	1
$F_2\bar{F}_1$	x	0	x	1
$F_2\bar{F}_1$	0	0	0	1

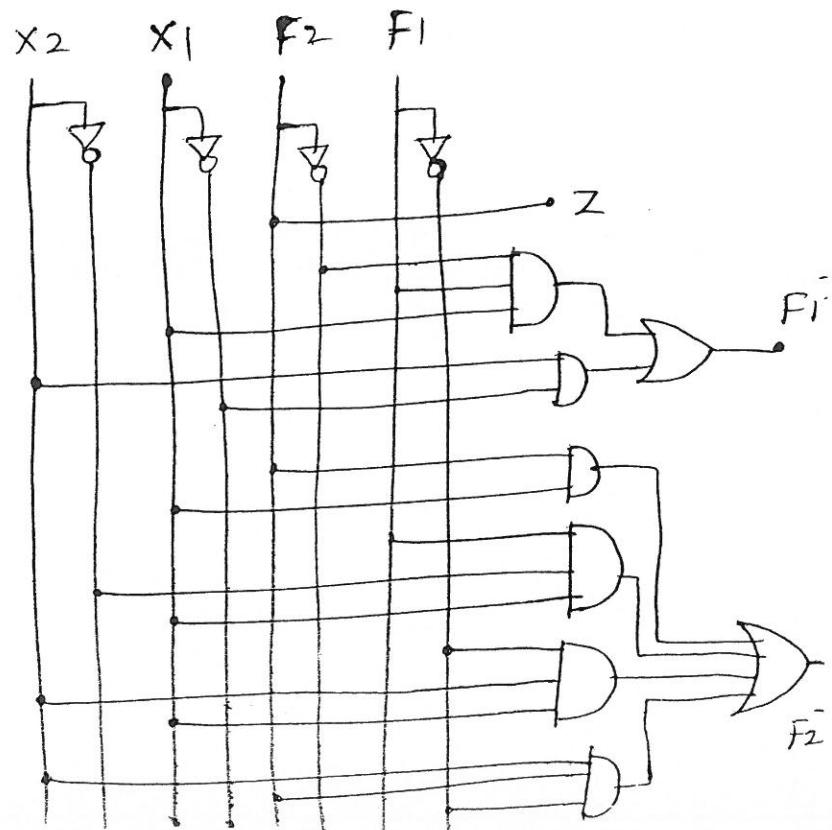
$$F_2^+ = F_2x_1 + F_1\bar{x}_2x_1 + \bar{F}_1x_2\bar{x}_1 + x_2F_2\bar{F}_1$$

$$F_1^+ = x_2\bar{x}_1 + \bar{F}_2F_1x_1$$

For Z :-

	$\bar{x}_2\bar{x}_1$	\bar{x}_2x_1	$x_2\bar{x}_1$	x_2x_1
\bar{F}_1	0	0	x	x
\bar{F}_1	x	x	0	0
\bar{F}_1	x	x	x	x
$\bar{F}_2\bar{F}_1$	x	1	1	x

$$F_2 = Z$$



Logic Diagram.



Design a gated latch circuit with 2 i/p's G_T (gate) and D (Data) and one output Q. The gated latch is a memory element that accepts the value D when G_T=1 and retains this value after G_T goes to 0. Once G_T=0, a change in D does not change the value of output Q.

Soln: At (A) State

$$DG = 00, Q = 0 \longrightarrow A$$

$$DG = 01, Q = 0 \longrightarrow B$$

$$DG = 10, Q = 0 \longrightarrow C$$

At (B) State

$$DG = 01, Q = 0 \longrightarrow B$$

$$DG = 00, Q = 0 \longrightarrow A$$

$$DG = 11, Q = 1 \longrightarrow D$$

At (C) State

$$DG = 10, Q = 0 \longrightarrow C$$

$$DG = 00, Q = 0 \longrightarrow A$$

$$DG = 11, Q = 1 \longrightarrow D$$

At (D) State

$$DG = 11, Q = 1 \longrightarrow D$$

$$DG = 01, Q = 0 \longrightarrow B$$

$$DG = 10, Q = 1 \longrightarrow E$$

At (E) State

$$DG = 10, Q = 1 \longrightarrow E$$

$$DG = 00, Q = 1 \longrightarrow F$$

$$DG = 11, Q = 1 \longrightarrow D$$

At (F) State

$$DG = 00, Q = 1 \longrightarrow F$$

$$DG = 01, Q = 0 \longrightarrow B$$

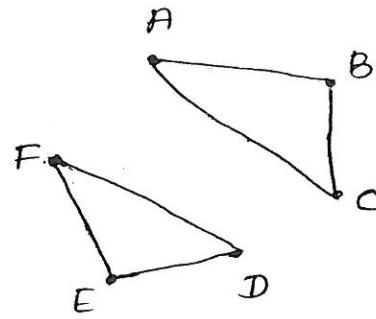
$$DG = 10, Q = 1 \longrightarrow E$$

Primitive Flow Table:

D	G	Q
0	0	0
0	1	0
1	0	0

Present State	Next State for i/P DG + O/P(Q)			
	00	01	11	10
A	(A), 0	B, -	-, -	C, -
B	A, -	(B), 0	D, -	-, -
C	A, -	-, -	D, -	(C), 0
D	-, -	B, -	(D), 1	E, -
E	F, -	-, -	D, -	(E), 1
F	(F), 1	B, -	-, -	E, -

Merges Graph:



$$A, B, C = S_0 = 0$$

$$D, E, F = S_1 = 1.$$

Reduced Primitive Flow Table:

Present State	Next state for inputs (DG) & output Q.			
	00	01	11	10
S_0 (0)	$S_0, 0$ ①	$S_0, 0$ ②	$S_0, -$ ①	$S_0, 0$ ②
S_1 (1)	$S_1, 1$ ①	$S_0, -$ ②	$S_1, 1$ ①	$S_1, 1$ ②

For y: (next state).

y	DG	00	01	11	10
0	0	0	0	1	0
1	1	0	1	1	1

$$Y = y\bar{G} + DG$$

For -Q (output)

y	DG	00	01	11	10
0	0	0	0	X	0
1	1	X	1	1	1

$$Y = \bar{Q}$$

Logic diagram:

