26/10/2021

#### COA ASSIGNMENT - I

2 marks:

1. What are the types of basic instruction formats? Explain it with example.

Those are 4 types of basic instruction formats. They are: (i) Zow address instruction

- (ii) One address instruction
  - (iii) Two address instruction
  - (iv) Three address instruction

#### (i) Zero Address Instruction:

The absolute address of the openand is held in a special register that is automatically incremented or decremented to point to the top of the stack.

Eg: PUSH T-A

PUSH T-B

ADD T(A+B)

#### (ii) One Address Instruction:

This uses an implied accumulater register for data manipulation. One operand is in accumulater and the other is in the register or memory location. Eg: LOAD A ADD B

#### (iii) Two Address Instruction:

fields. One address field is common and can be used either for source or destination and the other address field for source. Eq: MOV R, A

ADD R, B

#### (iv) Three Address Instruction:

gield. One address field is used for destination and the other two address fields for source.

Eg! ADD R, A, B

Explain Indirect Addressing Mode with example.

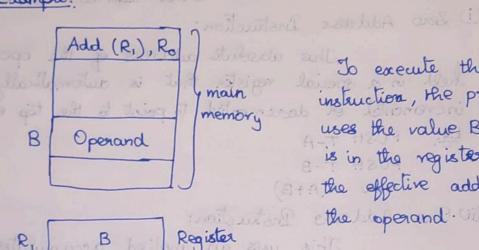
\*. The effective address of the operand is the content of a register or memory location whose address appears in the instruction

\*. The register or memory location that contains the address of the operand is called a pointer.

\*. The instruction does not give the open and its address explicitly.

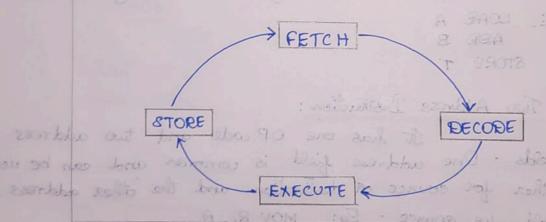
#### Example: while will (1)

162H1 M. K. F.



To execute the memory instruction, the processor uses the value B, which is in the register R, as at the effective address of Register the operand.

3. Draw the flow of Instruction Cycle.



4. Define Register mode and absolute mode with example. (iv) Three Address Brother:

\* Register Mode : 10 and 201 de

The operand is the content of a processor register. The address of the register is given in the instruction. Eg: MOV LOC Ra

#### \* Absolute mode: : : Mahandan santita and (1)

The openand is in the memory location and the address of this is given in the instruction Eq: MOV LOC, Row weeks two modes. Processed registers are used as temporary storage location where the data in a register are accessed using the register mode.

5. What one the various types of operation required for instruction?

- and CPU registers.
  - (ii) Arithmetic and logical operations on data.
- (iii) Program sequencing and control.
  - Input Output Transfers.

10 marks: (any a)

Describe in detail about different instruction types and instruction sequencing.

- (i) Zero Address Instruction
- (ii) One Address Instruction
- (iii) Two Address Instruction
- (iv) Three Address Instruction

### (i) Zeno Address Instruction:

The absolute address of the operand is held in a special register that is automatically incremented on decremented to point the location of the top of the stack. Eg: PUSH T-A PUSH T-B AND T(A+B)

#### (ii) One Address Instruction:

This uses an implied accumulater register for data manipulation. One operand is accumulator and the other is in the register or memory location. Eq: LOAD A

#### (iii) Two Address Instruction;

It has one operand cade and two address fields. One address field is common and can be used either for source or destination and the other address field is used for sounce. Eg: MOV R., A

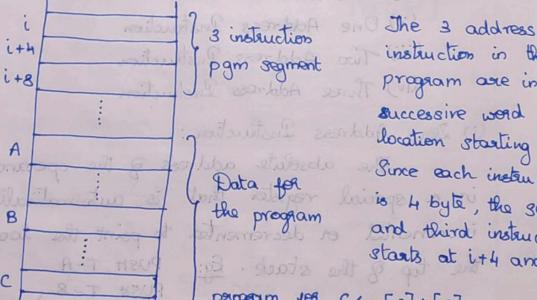
#### (iv) Three Address Instruction:

It has one operand code and three address fields. One address field is used for destination and two address fields for source Eq: ADD R., E, F

### \* Instruction Sequencing: (50 puro) : 20 very 01

Straight Line Sequencing line lines is adversed

Consider C ( [A] + [B]. We assume that the word length is 32 bits and the memory is Leva Address Instruction . shapeson bbo



pgm segment instruction in the program are in successive word attention starting at i. Since each instruction Data for is 4 byte, the second and third instruction starts at i+4 and i+8

paragram for C+[A]+[B]

The processes contains a register called program counter (PC) which holds the address of the instruction to be executed next.

To begin executing a program the address & the instruction must be placed in the program counter (PC).

Thus, the program control circuit uses the information in the PC to fetch and execute instruction one at a time in order of increasing address. This is called straight line sequencing.

During the execution of each instruction the PC is incremented by 4 to point the next instruction. Executing a given program is a two phase procedure:

(i) Instruction Fetch, (ii) Instruction Execute.

#### (i) Instruction Fetch:

The instruction is getched from the memory location whose address is in the PC. The instruction is placed in the instruction register (IR).

#### (ii) Instruction Execute:

The instruction in the IR is examined to determine which operation is to be performed. The specified operation is performed by the process or. This often involves fetching operands from the memory location or from processor register, performing an ALV operation and storing the result in the destination location or destination register.

Branching:

Consider the task of adding a list of 'n' numbers. The address of the momory location

containing 'n' numbers, are symbolically given as NUM!, NUM &, ..., NUM n and separate address instruction is used to add each number to the content of the register Ro. After all the numbers are added the result is placed in the memory location ones sum. Instead of using a long list of address instruction, it is possible to place the single instruction in the pragram. The loop is a straight line sequence of instruction and executes as many times as needed.

To begin executive a program the address of

the instruction must be placed in the program

	10000000	1	-1
i	MOV NUM 1, Ro	] (20	P MOV NUM I, R,
i+4	ADD NUM 2, Ro		Class Ro
i+8	APP NUM3, Ro	( d)	Determine the address &
	(91) ilsiper (18)		"NEXT" number and add
		5/	"NEXT" number to R,
i+4n-4	ADD NUM n, Ro MOV Ro, SUM	30	twood Decrement a R,
i+4n	MOV Ro, SUM	de la	BRANCH >0, loop
· ham	roped and at si	ration	MOV Ro, SUM
1		BUM	i wallorga loilisage
10 500L	org aft yd form	N	Si warmada and le
NOWI	is from the men	NUM	pridety as lova retip
num 2	The production	NUM 2	er recessory mary to
wal	the destination		and string the resi
NUMn		NUM n	destination register
NUMn		NUM n	Bronding .

rumbers. The address of the memory location

It starts at location loop and ends at instruction BRANCH > O loop. Assume that the number of entities in the list n is stead in memory location N.

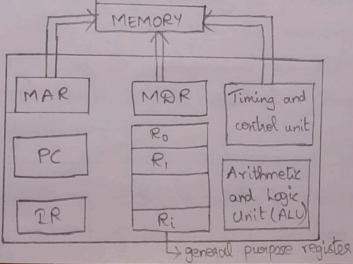
Register R, is used as the counter to determine the number of times the loop is executed. Hence, the content & the location N is loaded into register R, at the beginning of the program.

Within the body of the loop, the instruction Decrement R, reduces the content of R, by each time to the loop. Execution of the loop is repeated as long as the result of the decrement operation is greater than zero.

Branch instruction loads a new value into the PC . As a result, the processor tetches and executes instructions at the new address called BRANCH TARGET.

A conditional branch instruction causes a branch only if the specific condition is satisfied. If the condition is not satisfied, the PC is incremented in normal way and the next instruction in sequential address is getched and executed.

2. Explain about memory location, memory address and memory operations in detail.



The program or task is performed with a group of instructions. The instructions are stored in the memory.

### 1 byte → 8 bils

A collection of n bits is reported to as a word, where 'n' is the word length.

The MAR holds the add ross of the data, whereas, MDR holds the Data.

Accessing the information or data has to be done using the bit or byte address.

Since we cannot operate or access the bits separately, we use continuous memory locations. The address is usually numbers from 0 to 2k-1.

(i) Byte Addressibility: If the word contains 32 bits, the allocations auc 0, 4, 8, .... 30 on. For a register bit data 0,1, 2....

## (ii) Big - Endian and Little- Endian:

\*Big - Endian > Lower byte address is stored at Most Significant Bit (MSB)

\*. Little - Endian > Lower byte address is stored at how 2 Least Significant Bit (LSB)

# (iii) Word Allignment: listels is waitered promon

Address is alligned in the memory if they begin at a byte address (i.e) multiple number of bytes in a word. There can be unaligned words also. Number of bytes in a world is in powers of 2.

### (iv) Accessing numbers, characters and character strings:

A number usually occupies one word. All are accessed by the address. End of a string is used to convey the last character of the string.

### Memory Operations:

Jo porterm operations, the instructions and data are stored in the memory location. Processer circuits transfer the operands and results from memory to processer and vice versa.

Two basic operations - Load and Store.

Load operation is used to read the instruction and data from the memory to processor.

Store operation destroyes the previous content from processes to memory. It sends the location along with the data that has to be transferred.