Part-A

1. A TTL circuit with totem pole output has

   a) High output impedance

   b) Low output impedance

   c.) Very high output impedance

   d) Low speed operation

2. The digital logic family which has minimum power dissipation is

   a. TTL

   b. RTL

   c. DTL

   d. CMOS

3. The logic family which has highest noise margin is

   a. TTL

   b. ITL

   c. MOS

   d. CMOS

4. The fastest saturated logic family ------

   a. TTL

   b. ILL

   c. MOS

   d. ECL

5. The integrated circuit used in watches and calculators are of ----------

   a. Transistor Transistor Logic

   b. Emitter Coupled Logic

   c. Metal Oxide Semiconductor Logic

   d. Complementary Metal Oxide Semiconductor Logic

6. In RTL NOR gate, the output is at logic 1 only when all the inputs are at _____

   a) logic 0

   b) logic 1

   c) +10V

   d) Floating

7. The role of the _____ is to convert the collector current into a voltage in RTL.

   a) Collector resistor

   b) Base resistor

c) Capacitor

d) Inductor

8. Which of following is not advantage of RTL is _____

a) It uses a maximum number of resistors

b) It results in high power dissipation

c) High noise creation

d) It uses minimum number of transistors

9. The additional transistor and diode is used to increase DTL ---------

a. Size

b. Fan-in

c. Fan-out

d. Speed

10. The main advantage of TTL with Totem pole output as compared to other TTL types are ---------

a. Higher fan-in and higher fan-out

b. Fast switching and low power dissipation

c. Higher noise margin

d. Lower cost

11. Speed of operation of digital ICs are specified in terms of _____.

A. Fan-in

B. Fan-out

C. Propogation delay

D. Noise Margin

ANSWER: C

12. The expression for power dissipation of logic gates is given by _____

A. $I_{cc(avg)} * V_{cc} * n$

B. $I_{ccH} * V_{cc} * n$

C. $I_{ccL} * V_{cc} * n$

D. $I_{ccH} * V_{cc}$

ANSWER: A

13. Transistor acts a _____ gate in digital IC.

A. AND

B. OR

C. NOT

D. NAND

ANSWER: C

14. Medium Scale Integration IC chips refers to _____gates/chip

A. 10

B. 100

C. 530

D. 1000

ANSWER: B

15. MOSFET is a _____

a) Current controlled device

b) Voltage controlled device

c) Uncontrolled device

d) Pressure controlled device

Ans: B

16. MOSFETs are widely used in digital circuits due to

a) Less noise

b) Low power consumption

c) More power consumption

d) Less reliability

Ans: B

17. MOSFET stands for

a) Metal oxide surface FET

b) Metal oxide selenium FET

c) Metal oxide silicon FET

d) Metal oxide semiconductor FET

Ans: D

18. Transfer characteristics of MOSFET is drawn between

a) Vds Vs Id, keeping Vgs constant

b) Vds Vs Ig, keeping Vgs constant

c) Vgs Vs Id, Keeping Vds constant

d) Vgs Vs Ig, Keeping Vds constant

Ans: C

19. Which of the following is not a terminal of MOSFET?

a) Drain

b) Source

c) Base

d) Gate

Ans: C

20. Inverter, with identical transistors, has

a) High tPHL

b) High tPLH

c) Equal tPHL and tPLH

d) Low tPLH

Ans: C

21. NMOS device is turned ‘ON’ by applying

a) Positive gate to source voltage

b) Negative gate to source voltage

c) Positive gate to drain voltage

d) Negative gate to drain voltage

Ans: A

22. CMOS logic circuit of inverter has

a) One PMOS and One NMOS

b) Two PMOS

c) Two NMOS

d) One PMOS

Ans: A

23. What is the equivalent to Binary 1 in the negative logic convention?

a) Vdd

b) 0

c) -Vdd

d) 2Vdd

Ans: B

24. What is the role of p-MOS transistor in CMOS logic circuit?

a) Load

b) Pull down network

c) Pull up network

d) Not used in CMOS circuits

Ans: C

25. The time required for a gate or inverter to change its state is called

a. Rise time
b. Decay time
c. Propagation time
d. Charging time

26. The time required for a pulse to change from 10 to 90 percent of its maximum value is called

a. Rise time
b. Decay time
c. Propagation time
d. Operating Speed

27.The maximum frequency at which digital data can be applied to gate is called

a. Operating Speed
b. Propagation Speed
c. Binary level transaction period
d. Charging time

28.The time required for a pulse to decrease from 90 to 10 per cent of its maximum value is called

a. Rise time
b. Decay time
c. Binary level transaction period
d. Propagation Delay

29. Which of the following is also known as tri-state?

a. output port
b. input port
c. parallel port
d. output-input port

30. The third state of Tri-state buffer mainly known as?

a. High-resistance
b. Low-Impedance
c. Low-Resistance
d. High-Impedance

31.The primary purpose of a three-state buffer is usually

a. to provide isolation between the input device and the data bus

b. to provide the sink or source current required by any device connected to its output without loading down the output device

c. temporary data storage

d. to control data flow

32. When is it important to use a three-state buffer?

a. **when two or more outputs are connected to the same input**

b. when all outputs are normally HIGH

c. when all outputs are normally LOW

d. when two or more outputs are connected to two or more inputs

32.FPGA is used for

a) Analog circuit design

b) Digital logic circuit design

c) AC circuit design

d) DC circuit Design

33.FPGA device are _____ type.

a) SROM

b) EPROM

c) SLD

d) PLD

34.FPGA stands for…

a) Field Program Gate Array

b) First Program Gate Array

c) Field Programmable Gate Array

d) First programmable Gate Array

35.In FPGA the Vertical and horizontal directions are separated by_____

a) A channel

b) A line

c) A flip-flop

d) A strobe

36. Which of the following can be the name of an entity?

a) NAND

b) Nand_gate

c) Nand gate

d) AND

37 The default mode for a port variable in Hardware descriptive language is

a) IN

b) OUT

c) INOUT

d) BUFFER

38. In HDL Which of the following is the basic building block of a design?

a) Architecture

b) Entity

c) Process

d) Package

39. A package in VHDL consists of _____

a) Commonly used architectures

b) Commonly used tools

c) Commonly used data types and subroutines

d) Commonly used syntax and variables

40. The major drawback in behavioral modeling is _____

a) Asynchronous delays

b) Simulation

c) No delay

d) Supports single driver only

41. In structural modeling which is the following statement is used?

a) portmap()

b) process()

c) if-else

d) case

42. Under which modelling the functionality of the logic system and basic blocks are described?

a) Behavioral

b) Structural

c) Dataflow

d) Component

43. In Structural modelling the Ports are also known as _____ to the component.

a) Structure

b) Behavior

c) Function

d) Interface

44. The depletion N-channel MOSFET

a. Can be operated as a JFET with zero gate voltage
b. Can be operated as an enhancement MOSFET by applying +ve bias to gate
c. Can be operated as an enhancement MOSFET by applying -ve bias to gate
d. Cannot be operated as an enhancement MOSFET

Ans: B

45. Which action plays a significant role in enhancing the conductivity of channel by inducing the free electrons especially in enhancement mode of N-channel MOSFET?

a) Filter action
b) Inductor action
c) Capacitor action
d) Resistor action

Ans: C

46. Why is the N-channel MOSFET considered better than the P-channel MOSFET?

A) Low noise levels
B) TTL compatibility
C) Lower input impedance
D) Faster operation

Ans: D

47 . What is the value of typical threshold voltage CMOS inverter?

A) 0.001 to 0.002 Vdd
B) 0.001 to 0.02 Vdd
C) 0.01 to 0.02 Vd
D) 0.1 to 0.2 Vd

Ans: D

48 .When both nMOS and pMOS transistors of CMOS logic design are in OFF condition, the output is:

A) 1 or Vdd or HIGH state
B) 0 or ground or LOW state
C) High impedance or floating(Z)
D) Either 1 or 0

Ans:C

Part –B (2 Marks)

1. Which type of logic gate is the faster? Explain
2. Why ECL logic faster than TTL
3. What is mean by multiple emitter transistor
4. Why is the CMOS switching speed greater than PMOS/NMOS
5. What is a tri-state gate
6. Explain the purpose of the totem pole output stage used in a TTL gate
7. Define fan-in and fan-out
8. Why does the propagation delay occur in logic circuit?
9. State the advantage and disadvantage of CMOS family.
10. State the advantage and disadvantage of ECL family.
11. Define noise margin
12. What do you mean by logic level? Explain the positive logic and negative logic systems?
13. Mention the important characteristics of digital ICs
14. What is the major difference between ECL and TTL?
15. Give the syntax for VHDL architecture declaration.
16. What are the main components of a VHDL description?

Part C (3 Mark)

1. Draw and briefly explain the output characteristics of MOSFET.
2. Draw the NAND gate circuit and its truth table, using CMOS logic.
3. Write short notes on PMOS device.
4. Compare: RTL and TTL.
5. Explain the operation of open collector TTL.
6. Write short a note on types of TTL configurations.
7. Determine the High state Noise Margin of a standard TTL gate having the following currents as follows: V_{OH}=2.4 V,V_{IH}=2 V,V_{OL}=0.4 V,V_{IL}=0.8 V,
8. How many 7400 chips would it take to consume a power of a 100 watt light bulb when I_{CCH} is at 12 mA?
9. What is meant by ‘speed power product’ in IC digital logic families? . Is lower value of speed power product desirable? Justify