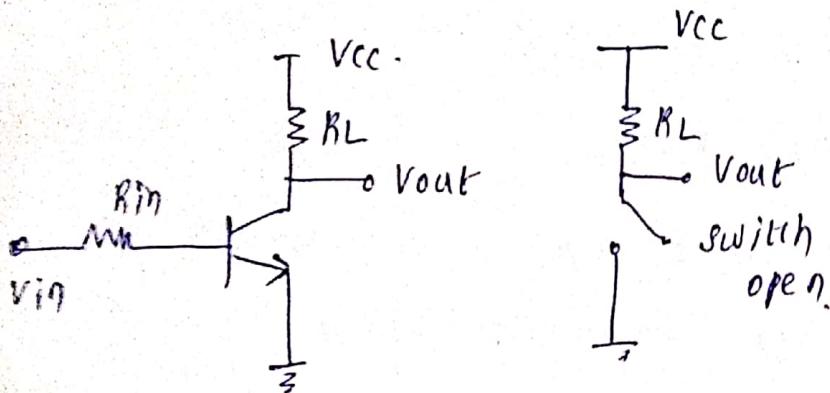


LOGIC FAMILIESS-1 Transistor as a switch

→ Transistor switches can be used to switch a low voltage DC device on or off by using a transistor in its saturated or cut-off state.

→ If connects and disconnects load R_L from source V_{in} . Ideally, transistor must not allow any current to flow through load R_L corresponding to switch in open position i.e; transistor must be biased to cut-off.

→ The whole of the voltage V_{in} must get connected across R_L corresponding to switch in closed position. i.e; transistor must be driven in saturation. (cont.)

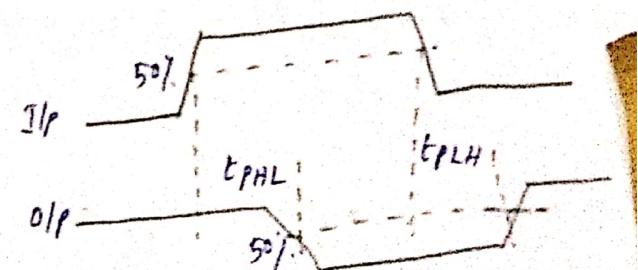
→ for a practical transistor switch, current through load R_L is negligibly small in OFF state and the voltage across R_L is slightly less than V_{in} because of very small voltage appearing across switch.

- If it is used in CB configuration, the ilp emitter current required to operate the switch is nearly as large as the collector current being switched, while in CC config, the ilp voltage required to operate the switch is nearly as large as supply voltage.
- In CC config, ilp voltage required to operate the switch is nearly as large as supply voltage.
- In CE config, ilp switching signal is very small in comparison with current or voltage being switched.
- CE is the most useful and therefore most commonly used config for transistor switch.

Characteristics of digital IC's

(a) speed of operation - speed of a circuit is specified in terms of propagation delay.

- The delay times are measured between 50% voltage levels of ilp and olp waveforms.



- There are 2 delay times,

t_{PHL} - when olp goes from high state to low

t_{PLH} - when olp goes from low to high

- The propagation delay time of logic gate is taken as average of these 2 delay times.

3. Power dissipation - This is amount of power dissipated in an IC. It is determined by current, I_{CC} , that it draws from V_{CC} supply and is given by $V_{CC} \times I_{CC}$.

I_{CC} is avg value of $I_{CC(0)}$ and $I_{CC(1)}$ specified in mw.

(3) figure of merit - It is defined as product of speed and power.

- The speed is specified in terms of propagation delay time expressed in ns

Figure of merit = propagation delay (ns) \times power (mW)
[pico Joules]
PJ

- Digital circuit must have high speed, low delay,

(4) fan-out - This is no. of similar gates which can be driven by a gate.

- High fan out is advantageous because it reduces need for additional drivers to drive more gates.

(5) current and voltage parameters

High level input voltage V_{IH} - Min. ilp voltage which is recognised by gate as logic 1

Low level input voltage V_{IL} - Max ilp voltage which is recognised by gate as logic 0.

High level output voltage V_{OH} - Min. voltage available at o/p corresponding to logic 1.

Low level output voltage V_{OL} - Max. voltage available at o/p corresponding to logic 0.

High level input current I_{IH} - Min. current which must be supplied by driving source corresponding to 1 level voltage.

Low level input current I_{IL} - Min. current which must be supplied by driving source corresponding to 0 level voltage.

High level output current I_{OH} - This is max. current which gate can sink in 1 level.

Low level output current I_{OL} - Max. current which gate can sink in 0 level.

High level supply current $I_{CC(1)}$ - This is supply current when o/p of gate is at logic 1.

Low level supply current $I_{CC(0)}$ - Supply current when o/p of gate is at logic 0.

(6) Noise immunity - Stray electric and magnetic fields may induce unwanted voltages known as noise, on the connecting wires b/w logic circuits.

- The circuit's ability to tolerate noise signals is referred to as noise immunity, a quantitative measure of which is called noise margin.

7) operating temperature - The range to which a diode functions properly must be known.

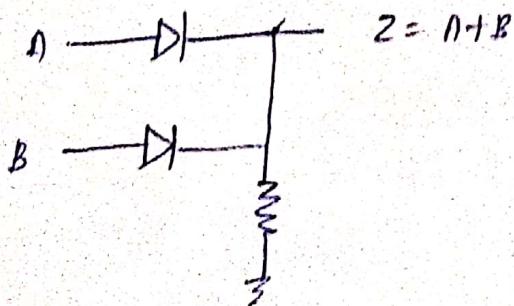
Accepted ranges are 0 to $+70^{\circ}\text{C}$ for consumer and industrial applications

-55°C to $+125^{\circ}\text{C}$ - Military purpose

8) power supply requirements - The supply voltages and the amount of power required by an IC are important characteristics required to choose proper power supply.

-2 Diode Logic (DL)

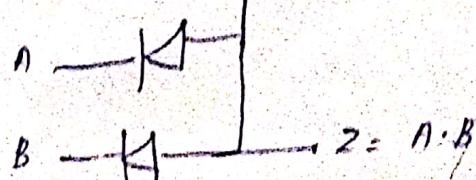
Diode logic OR gate



$$Z = A + B$$

Diode logic

AND gate



$$Z = A \cdot B$$

→ The diode will conduct current in one direction, but not in the other. So it acts as a switch.

→ Logic 1 - $+5\text{V}$

Logic 0 - Ground or 0V

OR gate → If both inputs are left unconnected or both at logic 0, output 2 will also be 0V.

- If either input is raised to +5V, the diode will become forward biased and it conducts. This forces output to logic 1.
- If both are 1, then output is also logic 1.

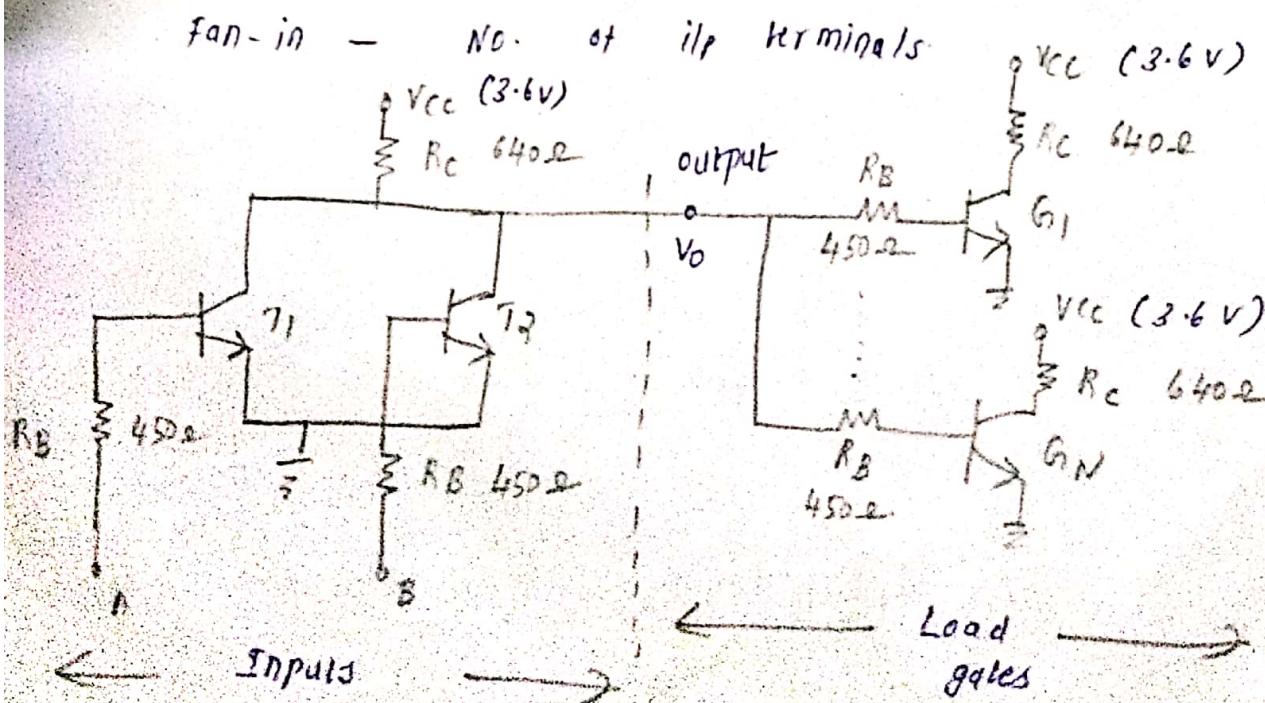
AND gate

- If both inputs are unconnected or if they are at logic 1, output will be high.
- If either input is grounded or 0, that diode will conduct and pull output to logic 0.

When DL gates are cascaded, additional problems occur.
DL is used only for single gates.

Resistor - Transistor Logic (RTL)

- consists of resistors and transistors and was earliest logic family to be integrated.



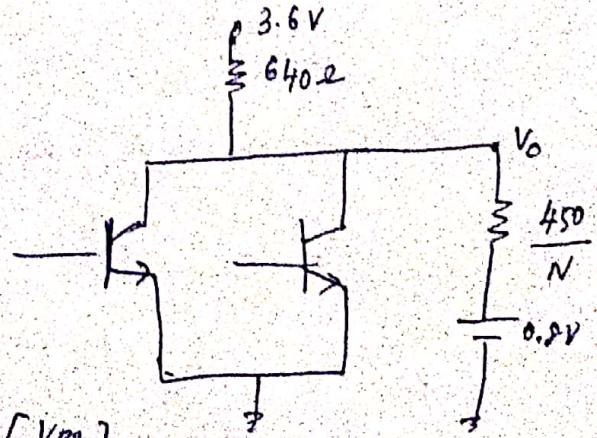
operation

- If i_{lp} is applied to A and B terminals.
- voltage corresponding to Low level should be low enough to drive corresponding transistors to cut-off.
- High level should be high enough to drive corresponding transistor to saturation.
- If both i_{lp} s are Low, T_1 and T_2 are cut-off and o/p is high. A high level on any i_{lp} will drive corresponding transistor to saturation causing o/p to go Low.
- The Low level o/p voltage is V_{CEsat} of a transistor ($\approx 0.2V$) and high level o/p voltage depends on no. of gates connected to o/p.

Loading considerations

- If all i_{lp} s to the gate are Low, o/p is high and if gate is not driving any other gate. ie; no load is connected, the o/p voltage will be slightly less than V_{CC} .

When N gates are driven, load will be equivalent to a resistor of value $\frac{450}{N}$ in series with voltage source of $0.8V [V_{BB}]$



$$I_B = \left[\frac{3.6 - 0.8}{640 + \frac{450}{N}} \right] \quad \frac{1}{N} = \frac{0.8}{640N + 450}$$

$$I_{C\text{ sat}} = \frac{3.6 - 0.8}{640} = 5.31 \text{ mA}$$

Value of N must satisfy,

$$h_{FE} \cdot I_B \geq I_{Csat}$$

Noise margins

When o/p is in 0 state, $V_o = 0.2V$.

If this voltage becomes about $0.5V$, load transistor comes to conduction which causes malfunction of circuit.

\therefore Logic 0 noise margin $DO \approx 0.3V$

Logic 1 noise margin depends upon no. of gates being driven.

for $N=5$,

$$V_o = \frac{90}{90+640} \times (3.6) + \frac{640}{90+640} \times (0.8)$$

$$= 1.14 V$$

For $h_{FE}=10$, total base current required by load transistors to be driven into saturation will be

$$5 \times \left(\frac{5.31}{10} \right) \text{ mA}$$

Propagation delay time

When o/p of gate is in Low state, all the load transistors are cut-off and base emitter junction of

(5)

each of these transistors appears to be capacitor.

When α_{LP} has to change from low to high due to changes in i_{LR} , it will do so with a time constant given by,

$$\left(\frac{640 + 450}{N} \right) NC = (640N + 450)C$$

Current source logic

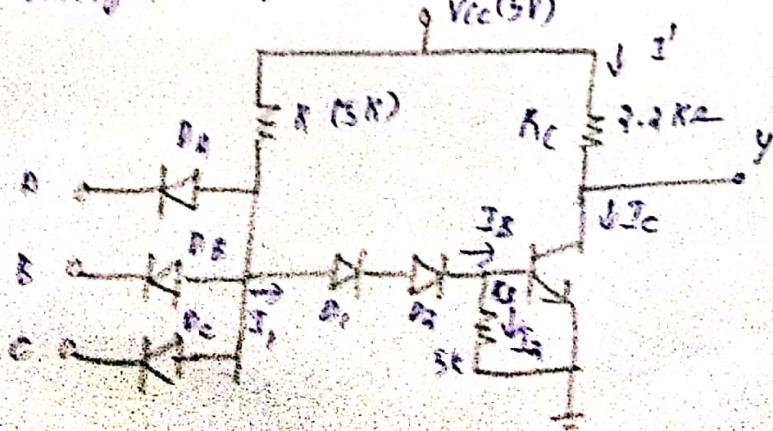
The gate supplies current to load transistors when in 1 level, whereas leakage current of load transistor flow through T_1 or T_2 in 0 level. Since source current is greater than sink current, it is known as current source logic.

S-D Diode Transistor Logic (DTL)

→ complex than RTL but has greater fanout and improved noise margins.

DLS Adv

→ slower speed and hence DTL is modified and emerged as TTL.



Operation

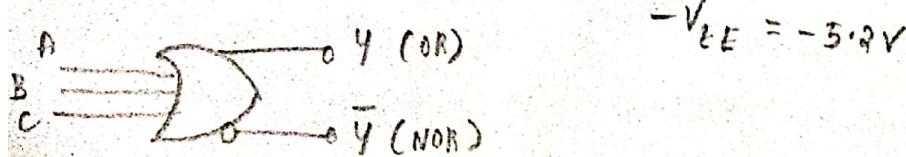
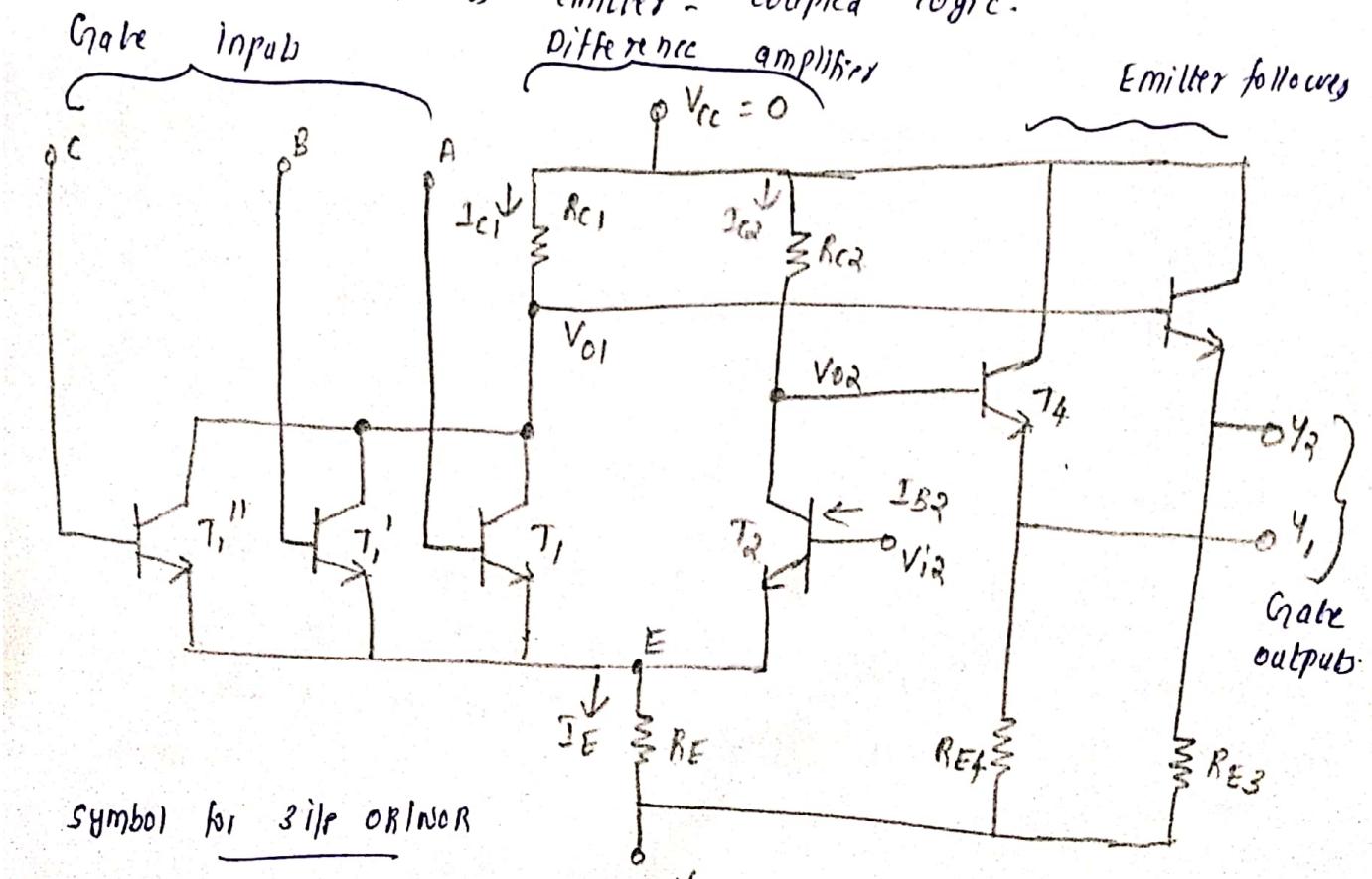
- The basic DTL gate is NAND gate
- A 3 ilp NAND gate driving N similar gates is shown. The ilp diodes D_A , D_B and D_C conduct through resistor R , if corresponding ilp is in low state, while corresponding to high state the diode is nonconducting.
- If atleast one of the ilps is Low, diode connected to this ilp conducts and V_D is above low level voltage at the ilp.
- The output of transistor is V_{CC} , if all 3 ilps are in High state, the ilp diodes are cut-off and consequently current flowing from V_{CC} through R should be sufficient to drive T in saturation.
∴ o/p of T is $V_{CE,SAT}$.

Propagation Delay

- Delays are associated with turning ON and turning OFF delay of o/p transistor.
- The turn-off delay is larger than turn-on delay.
- The propagation delay of commercially available DTL gates are of order of 30 to 80ns.

Emitter coupled Logic (ECL)

- Fastest of all logic families and is used in applications where very high speed is essential.
- Propagation delay is less than 1ns per gate.
- ECL is realised using difference amplifier in which emitters of 2 transistors are connected and hence it is known as emitter-coupled logic.



→ Emitter followers are used for d.c level shifting of outputs so that $V(0)$ and $V(1)$ are same for inputs and outputs.

→ Y_1 corresponds to OR logic and Y_2 to NOR logic.

- Additional transistors are used in parallel to T_1 to get required fan-in.
- In ECL, the end of the supply is connected to ground compared to other logic families in which +ve end of supply is grounded.
- This is done to minimise effect of noise induced in power supply and protection of gate from short circuit developing between collector of a gate and ground.
- The voltage corresponding to $V_{(O)} = V_{(I)}$ on both negative due to the end of supply being connected to ground.

Fan-out

If all the inputs are low, the input transistors are cut-off. Therefore i_{lp} resistance is very high. If an i_{lp} is high, the input resistance is that of emitter follower which is also high.

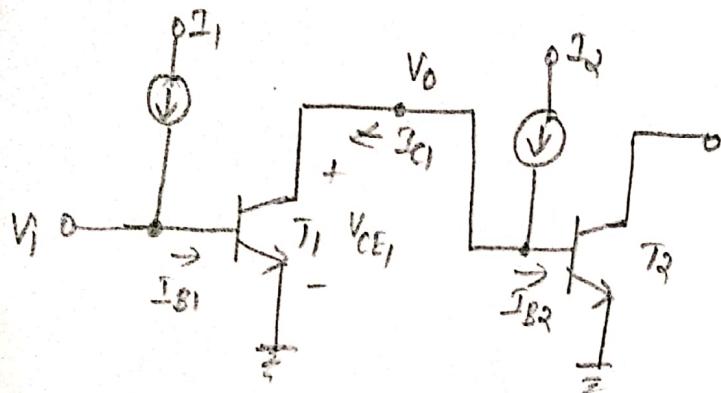
The i_{lp} resistance is either that of an emitter follower or forward resistance of a diode which is always low. Because of low i_{lp} impedance and high i_{lp} impedance, fan-out is large.

(7)

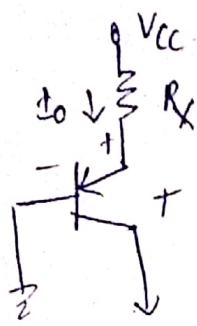
Integrated-Injection Logic (I²L)

- I²L is simple, uses very small silicon chip area, consumes very little power, easy to fabricate.
- Used for medium and large scale integration.

I²L inverter



- If input V_i is at Low logic level ($V_i \approx 0$), T_1 is off so that $I_{B1} = 0$. The input source acts as a sink for current I_1 . $\therefore I_2$ flows through base of T_2 driving it to saturation.
- When T_1 is off and T_2 is on, $V_{BE2} = V_{CE1} \approx 0.8V$
- If input is High logic level ($V_i \approx 0.8V$), the base current I_{B1} will have 2 components, one of them being I_1 , and other is due to source V_i and consequently T_1 saturates.
- $\therefore V_{CE1} = V_{CE,sat} \approx 0.2V$, which drives T_2 to cut-off and T_1 acts as sink for I_2 . V_o is complement to that of V_i so it acts as inverter.



- The resistor R_B required to inject base current would require a large silicon area if fabricated on the chip, it can be eliminated by replacing it with current source.
- The grounded p-n-p transistor acts as current source, which is referred as current injector.
- R_x is external to the chip and I_0 is given by,

$$I_0 = \frac{V_{CC} - V_{EB}}{R_x}$$

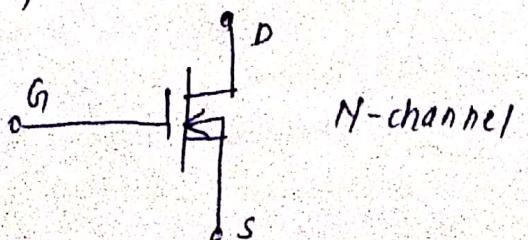
Characteristics of MOSFET

- 4 terminal device with source, gate, drain and body.
- Body is connected to source, making it a 3-terminal device.
- Voltage controlled device

2 modes

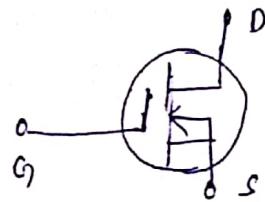
(1) Depletion mode

When there is no voltage on gate, the channel shows its max. conductance. As the voltage on gate is either +ve or -ve, the channel conductivity decreases.



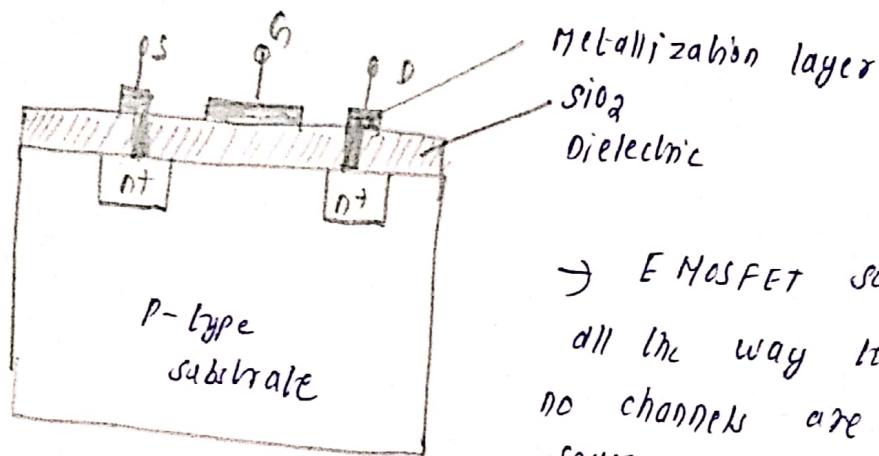
⑧) Enhancement mode

When there is no voltage on the gate, the device does not conduct. When applied voltage is more, the device conducts more.



Construction

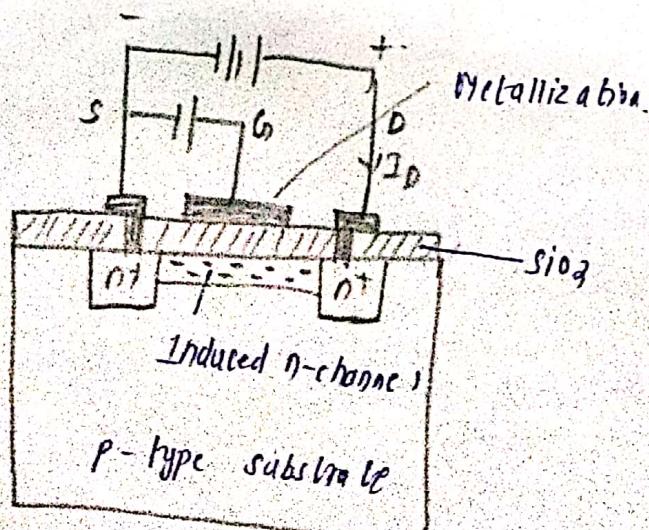
N-channel E MOSFET.



→ E MOSFET substrate extends all the way to SiO_2 and no channels are doped between source and drain.

→ Channels are electrically induced in these MOSFET, when a gate-source voltage V_{GS} is applied to it.

Operation of N-channel E MOSFET



Cutoff

- When $V_{GS} = 0$, it does not conduct.
- No channel
- $I_{DS} = 0$
- $V_{GS} <$ threshold voltage
- Source and drain has free \bar{e} and body has free holes
- Junctions b/w body and source or drain are reverse biased.

Linear

- Channel formed, $I_{DS} \propto$ with V_{GS}

- Gate V is greater than threshold v
 - Now an inversion region of \bar{e} called channel connects source and drain creating a conductive path.
- The no. of carriers and conductivity \propto with gate v.
The potential difference b/w drain and source is

$$V_{DS} = V_{GS} - V_{GD}$$

- When the potential is applied to drain, I_{DS} flows through channel from drain to source.
The current increases with both V_{DS} and V_{GS} .

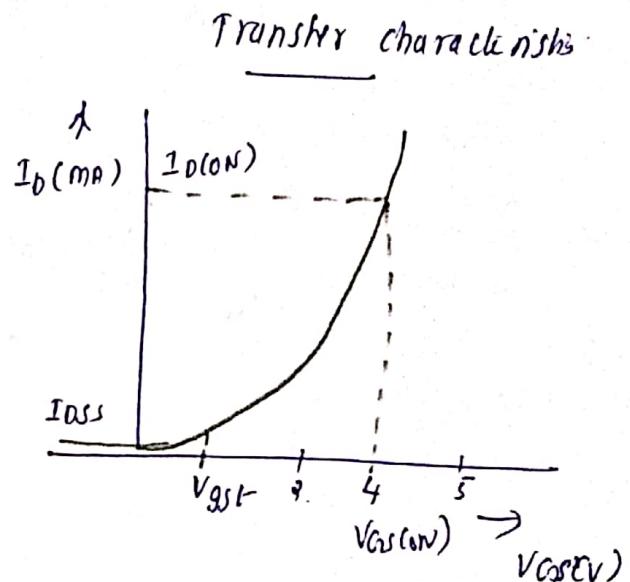
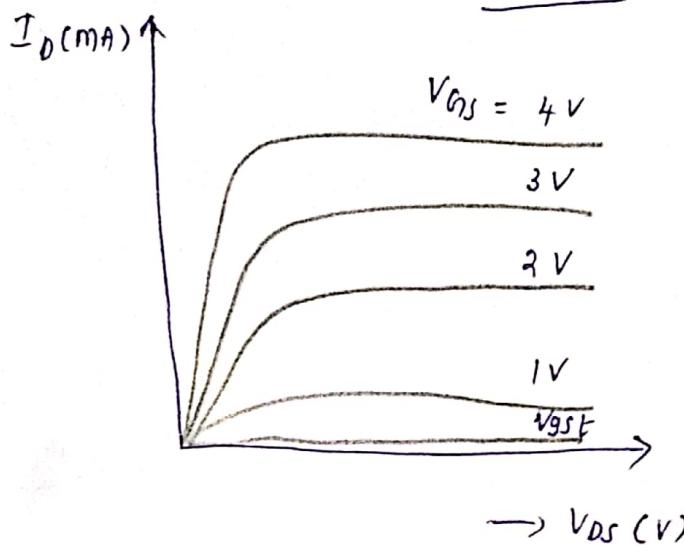
Saturation

- If V_{DS} becomes larger than that $V_{GD} < V_L$, channel is no longer inverted. Near the drain and becomes pinched off.

⑨

→ As \bar{e} reaches the end of the channel, they are injected into depletion region near drain and accelerated towards drain.

→ Above this, I_{ds} is controlled only by gate V and ceases to be influenced by drain. This is saturation. Drain characteristic



$$I_{ds} = 0 \quad V_{gs} < V_t \quad - \text{cutoff}$$

$$\beta \left(V_{gs} - V_t - \frac{V_{ds}}{\alpha} \right) V_{ds}$$

$$\frac{\beta}{2} (V_{gs} - V_t)^2$$

$$V_{ds} < V_{dsat} - \text{Linear}$$

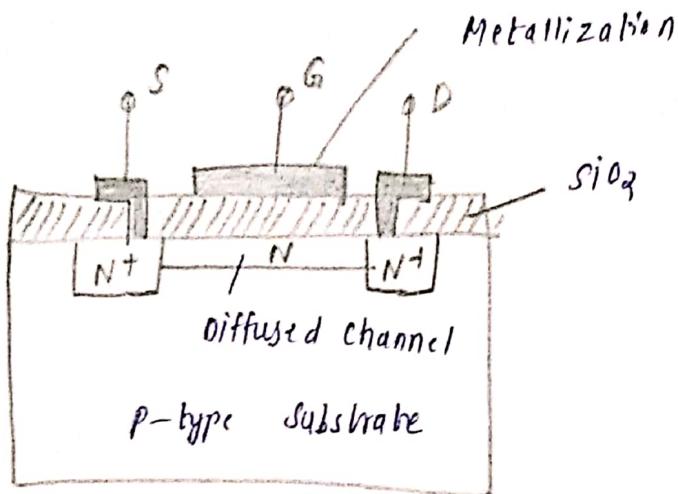
$$V_{ds} > V_{dsat} - \text{Saturation}$$

Depletion type MOSFET

Construction

→ consists of highly doped p-type substrate into which heavily doped n-type is diffused forming source and drain

→ N-channel is formed by diffusion b/w S and D.



→ A thin layer of SiO_2 is grown over entire surface and holes are cut through SiO_2 to make contact with N-type blocks.

operation

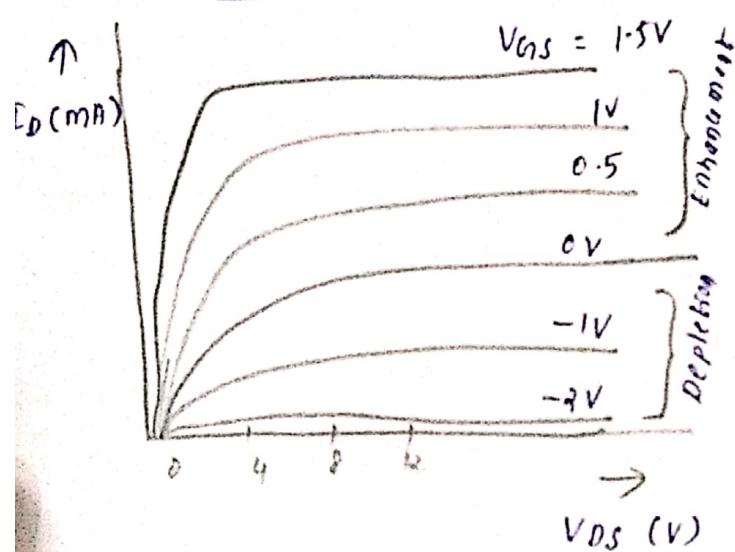
- can be operated with either positive or negative gate
- When gate is +ve w.r.t. source , it operates in enhancement mode .
- when gate is -ve w.r.t source , it operates in depletion mode .
- when drain is +ve , a drain current will flow , even with zero gate potential and it is operating in enhancement mode .
- when gate is -ve , gate repels -ve charge carried out of N-channel . This creates a depletion region in Nc channel and therefore

(16)

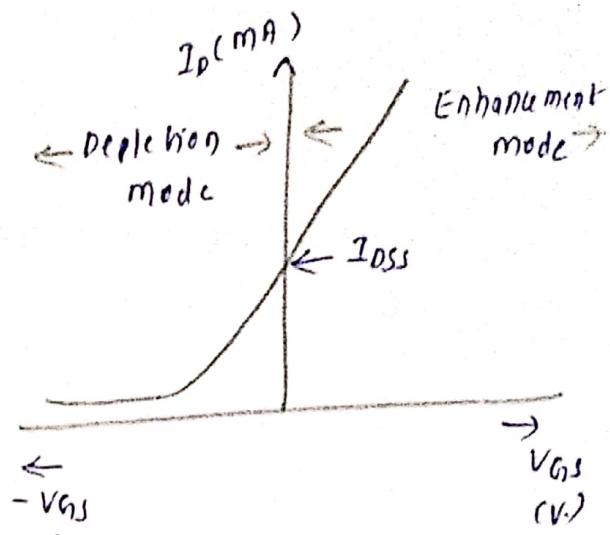
increases channel resistance and reduces drain current.

- The more -ve the gate, the less drain current. too much -ve gate voltage can pinch-off the channel.

Drain characteristics



Transfer characteristics



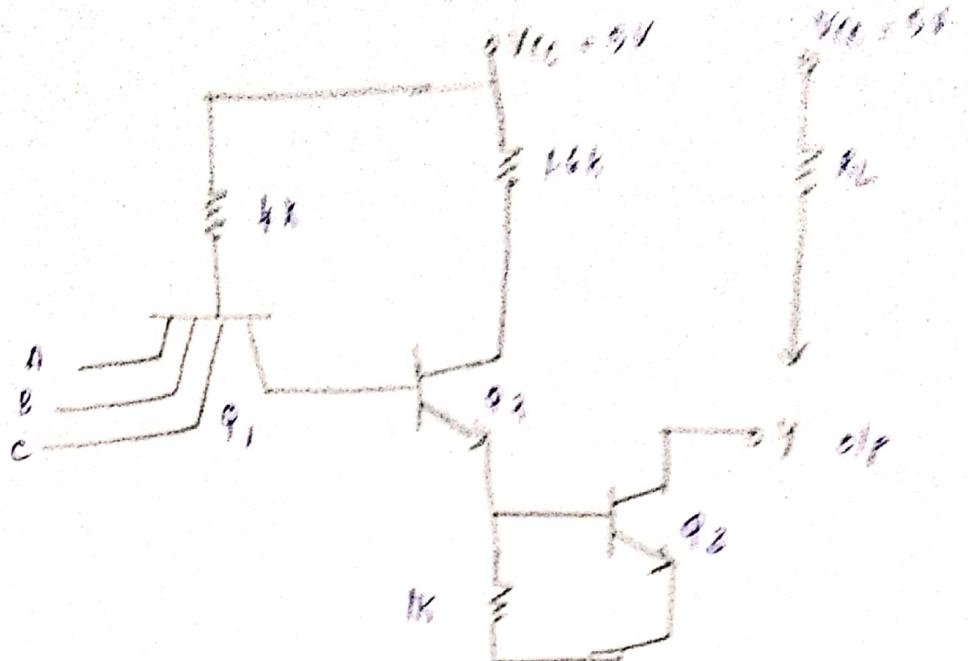
I_{DSS} - Drain current with shorted gate

Transistor - Transistor (TTL)

- NAND is the basic building block of logic family.
- types of o/p configuration
 - open collector output
 - totem pole output
 - Tristate output

(i) standard TTL with open collector output

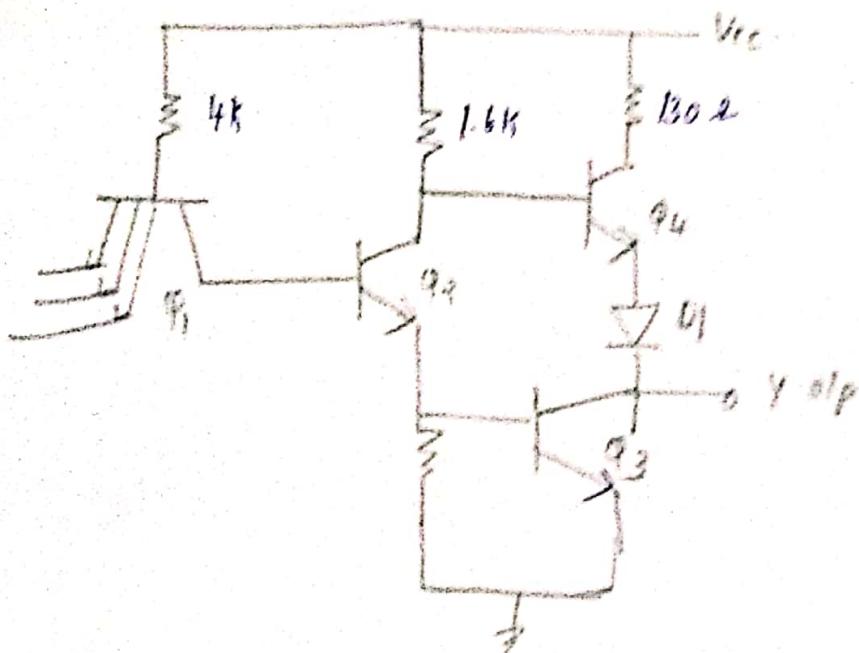
- TTL NAND is the modified form of DTL gate



- Φ_1 is multiple emitter transistor and the logic inputs are applied to emitters of Φ_1 .
- Inputs behave like input diodes in DTL.
- The base collector junction acts as another pn junction diode [similar to diode Φ_1 in DTL]
- Φ_2 replaces Φ_2 in DTL.
- o/p of TTL gate is taken from open collector of Φ_3 .
- Resistor is connected externally at the collector of Φ_3 to V_{CC} , to maintain o/p voltage (V_{OY}) to high when Φ_3 is cut-off.
- External resistor is termed as pull-up resistor.
- When all inputs are high, base emitter of Φ_1 is FB and voltage at base of Φ_3 is higher than $2.1V$. Φ_2 - driven to saturation and also Φ_3 .
- o/p voltage at y is $V_{OY} = 0.2V$ (saturation)
- Gate operation (NAND) is obtained if either all inputs are high, o/p is low and when any 1 input is low, o/p is high.

TTL with Totem pole configuration

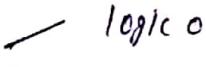
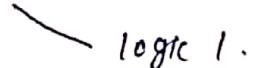
- Same as open - collector , except for o/p transistor Q_4 , a diode D_1 and resistor $R_{0.2}$ at collector of Q_4 .
- It is called as totem pole o/p config , because Q_4 sits upon Q_3 . Base of Q_4 is driven by collector of Q_2 .



- 3 voltage levels of TTL are 0.2V for low level and 3.4V to 5V for high level.
- If any I_{lp} is low, base emitter junction Q_1 becomes PB .
- Voltage level at base of $Q_1 = 0.2V + V_{BE}$
 $\approx 0.9V$
- It is not sufficient to drive Q_2 and Q_3 . So they are in cut-off.
- Voltage at base of Q_1 drives Q_2 and Q_3 into sat.
 $V_{BE\text{ of } Q_3} + V_{BE\text{ of } Q_2} + \text{diode drop of } D_1$
 $= 0.7 + 0.7 + 0.7 = 2.1V$
 o/p is logic high

- When all inputs are high, voltage at base of Φ_1 is higher than $2.1V$
- Emitter base junction is FB, and Φ_2, Φ_3 are driven to saturation. V_{CE} at Y (saturation) = $0.2V$
- Voltage at collector of Φ_2 is equal to one V_{BE} drop of Φ_2 ie; $0.7 + 0.2 = 0.9V$. This is applied to Φ_4 base and not sufficient to drive Φ_4 .
- Voltage required to drive Φ_4 is V_{CE} at Φ_3 (sat) + Φ_1 drop + V_{BE} drop of Φ_4) = $0.2 + 0.7 + 0.7 = 1.6V$.
 - ∵ Φ_4 is in cut-off.
- While Φ_3 is in saturation, I_C is available from connected loads at o/p.
- The gate confirms NAND func, as when any of inputs is low, o/p is high and if all inputs are high, o/p is low.

(3) TTL gate with Tristate output

Tristate gate allows wired connections at the o/p's to form a common bus system. All logic gates have 2 o/p states  logic 0  logic 1.

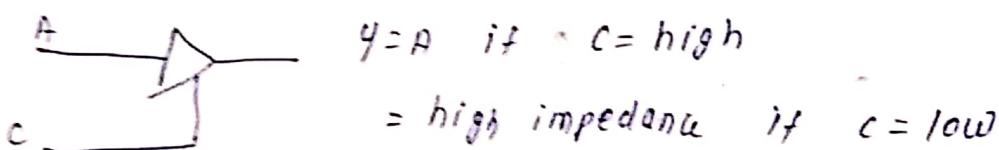
But In-state implies

- (i) A low-level state or logic 0, when lower \oplus is ON and upper \oplus is OFF.

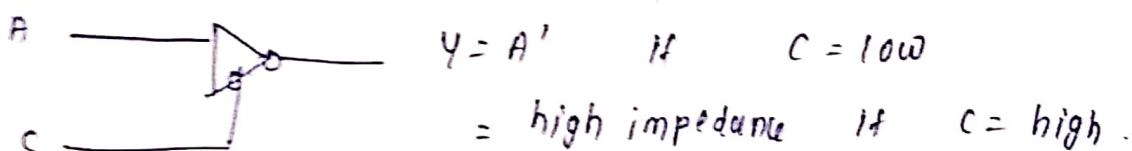
- (2)
- 2) A high level (or) logic 1, when lower (7) is off and upper (7) is on.
 - 3) A 3rd state when both (7) are off. It is open circuit or high impedance state, which allows direct wiring connection of many ops on a common line.

Tristate eliminates need of open-collector gates in common bus config.

a) Tri-state buffer gate

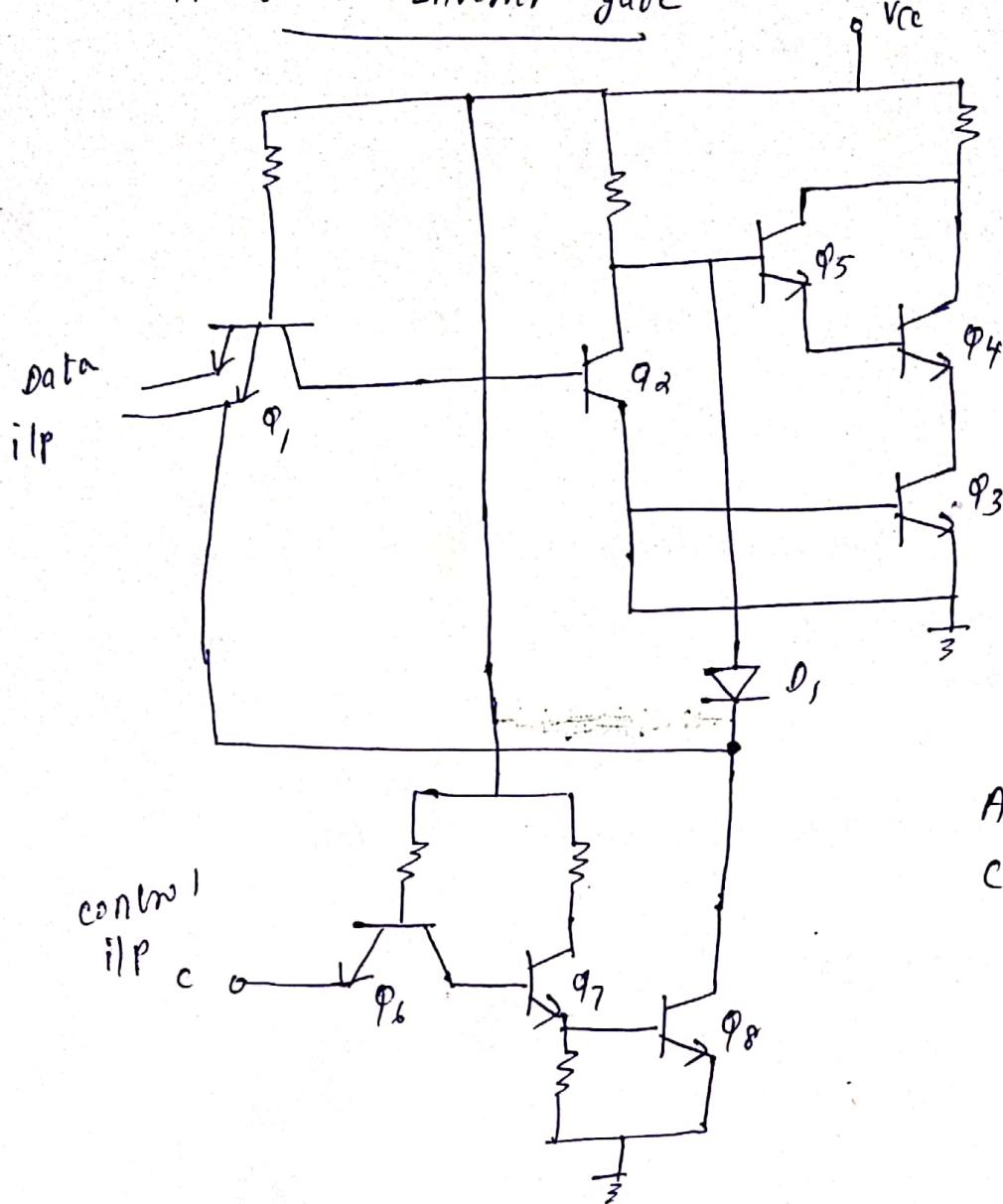


b) Tri-state inverter gate



- Tri-state gate consists of extra I/P called control (or) enable input
- When control I/P is at logic 0, the gate performs normal operation.
- When control I/P is 1, o/p of gate goes to tri-state (or) high impedance state regardless of I/P A.
- Gates with reverse control logic is also available

Tri-state Inverter gate



- $\varphi_6, \varphi_7, \varphi_8$ - will perform mistake circuit to form open collector inverter and is connected to collector of φ_7 thro' D_1 .
- φ_1 to φ_5 associated with data input forms a logic pole TTL OR.
- when C is low, φ_6 is FB and base current and base voltage is not available to make φ_7 ON. ∵ φ_8 is OFF and no current flows thro' collector of φ_8 and D_1 .

- φ_8 has no effect on operation of gate and o/p
 γ depends on data n .
- When C is high, φ_L is BB and φ_B is SB .
 Voltage at base of φ_7 is high and sufficient current is available to make φ_7 on and φ_8 on and driven to saturation.
 Current will flow thru' collector of φ_8 and D_1 .
 ∵ voltage at collector of φ_7 is diode drop + V_{CE} of φ_7 = $0.7 + 0.2 = 0.9V$.
- This voltage level keeps φ_5 and φ_4 off which requires atleast 2 V_{BE} drops i.e. $1.4V$ to turn them on.
- Saturation of φ_8 exhibits low h_f to one of emitters of φ_1 forcing transistors φ_3 and φ_4 to turn off.
- Both totem pole transistors φ_3 and φ_4 are off and o/p behaves like open circuit with high impedance state.