Part A

1. _____ are devices capable of storing binary information

A. Storage elements

B. Transfer Agents

C. Amplifiers

D. Decoders

ANSWER A

2. The sequential circuit receives binary information from external inputs that, together with the _____ of the storage elements, determine the binary value of the outputs.

A. Present state

B. Previous State

C. Next state

D. No state

ANSWER A

3. A flip-flop is a binary storage device capable of storing _____ bit of information.

A. 1

B. 2

C. 3

D. 4

ANSWER A

4. The storage elements used in asynchronous sequential circuits are called _____.

A. Clocks

B. Latches

C. Flip flops

D. Decoders

ANSWER B

5. In this logic, output depends not only on the current inputs but also on the past input values. It needs some type of memory to remember the past input values

A. Logical Circuit

B. Connected Circuit

C. Sequential Circuit

D. Parallel Circuit

ANSWER C

6 Which of the following is correct for a gated D-type flip-flop?

a) The Q output is either SET or RESET as soon as the D input goes HIGH or LOW

b) The output complement follows the input when enabled

c) Only one of the inputs can be HIGH at a time

d) The output toggles if one of the inputs is held HIGH

Answer: a

7 When an inverter is placed between both inputs of an SR flip-flop, then resulting flip-flop is

A. JK flip-flop

B. D flip-flop

C. SR flip-flop

D. Master slave JK flip-flop

ANSWER: B

8 The main difference between JK and RS flip-flop is that

A. JK flip flop needs a clock pulse

B. There is a feedback in JK lip-lop

C. JK flip-flop accepts both inputs as 1

D. JK flip-flop is acronym of Junction cathode multivibrator

ANSWER: C

9 Which statement describes the BEST operation of a negative-edge-triggered D flip-flop?

a) The logic level at the D input is transferred to Q on NGT of CLK

b) The Q output is ALWAYS identical to the CLK input if the D input is HIGH

c) The Q output is ALWAYS identical to the D input when CLK = PGT

d) The Q output is ALWAYS identical to the D input

Answer: a

10 In D flip-flop, if clock input is LOW, the D input _____

a) Has no effect

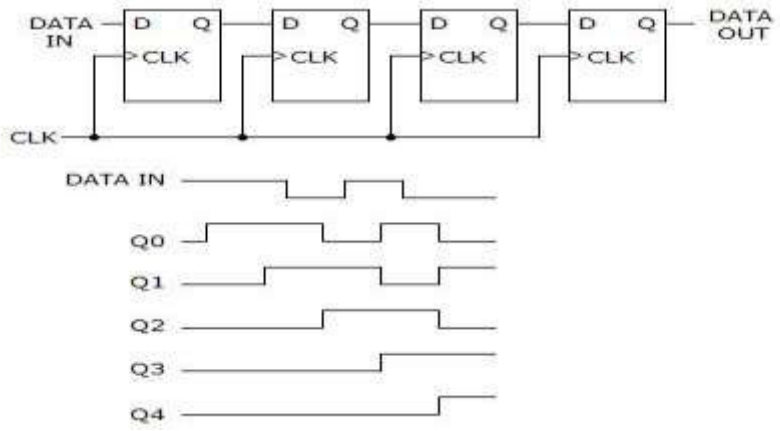
b) Goes high

c) Goes low

d) Has effect

Answer: a

11. The circuit given below fails to produce data output. The individual flip-flops are checked with a logic probe and pulser, and each check OK. What could be causing the problem?



A. The data output line may be grounded.

B. One of the clock input lines may be open.

C. One of the interconnect lines between two stages may have a solder bridge to ground.

D. One of the flip-flops may have a solder bridge between its input and V_{cc}.

ANSWER B

12 Which is the prohibited state/ condition in S-R latch and needs to be avoided due to unpredictable nature of output?

a. S = R = 0

b. S = 0, R = 1

c. S = 1, R = 0

d. S = R = 1

Answer: d

13 Which among the following is not a mode of Flip Flop representation?

a. Characteristic Equations

b. Excitation Tables

c. Finite State Machines (FSM)

d. Variable Entered Mapping (VEM)

Answer: d

14 In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in

A. Q=0, Q'=1

B. Q=1, Q'=0

C. Q=1, Q'=1

D. Indeterminate states

ANSWER C

15. In a positive edge triggered JK flip flop, a low J and low K produces?

a) High State

b) Low state

c) Toggle state

d) No Change state

Answer: D

16. The characteristic equation of J-K flip-flop is _____

a) Q(n+1)=JQ(n)+K'Q(n)

b) Q(n+1)=J'Q(n)+KQ'(n)

c) Q(n+1)=JQ'(n)+KQ(n)

d) Q(n+1)=JQ'(n)+K'Q(n)

Answer: D

17. In J-K flip-flop, the function K=J is used to realize _____

a) D flip-flop

b) S-R flip-flop

c) T flip-flop

d) S-K flip-flop

Answer: C

18. What does the triangle on the clock input of a J-K flip-flop mean?

a) Level enabled

b) Edge triggered

c) Both Level enabled & Edge triggered

d) Level triggered

Answer: B

19. A master slave Flipflop has the characteristics that

a) Change in the input immediately reflected in the output

b) Change in the output occurs when the state of master is affected

c) Change in the output occurs when the state of the slave is affected

d) Both the master and slave states are affected at the same time

Answer: C

20 A positive edge-triggered D flip-flop is connected to a positive edge-triggered JK flipflop as follows. The Q output of the D flip-flop is connected to both the J and K inputs of the JK flip-flop, while the Q output of the JK flip-flop is connected to the input of the D flip-flop.

Initially, the output of the D flip-flop is set to logic one and the output of the JK flip-flop is cleared. Which one of the following is the bit sequence (including the initial state) generated at the Q output of the JK flip-flop when the flip-flops are connected to a free-running common clock? Assume that J = K = 1 is the toggle mode and J = K = 0 is the state-holding mode of the JK flip-flop. Both the flip-flops have non-zero propagation delays.

a) 0110110…
b) 0100100…
c) 011101110…
d) 011001100…

Answer: A

21. There are _____ Main types of sequential circuits

A. 1
B. 2
C. 3
D. 4

ANSWER B

22. In Sequential circuits the output states depend upon

A. Past input states
B. Present input states
C. Present as well as past input
D. No state

ANSWER B

23. The sequential circuit is also called _____

A. Flip-flop
B. Latch
C. Strobe
D. Adder

ANSWER B

24. The design procedure of a sequential circuit is based on

A. 7 steps
B. 8 steps
C. 9 steps
D. 10 steps

ANSWER C

25. The state of the flip flop can be switched by changing its

A. Input signal

B. Output signal

C. Momentary signals

D. No signal

26. The operation of the basic flip flop can be changed by providing some additional Control

A. Input

B. output

C. Inverter

D. shift

27. Two states are said to be equal if they have the same

A. inputs

B. Next state

C. outputs

D. Mid-state

28. The time sequence for flip flop can be enumerated by_____

A. State table

B. Map

C. Truth table

D. Graphs

29. In Moore models, the output is the function of only

A. Present state

B. Input state

C. Next state

D. Mid state

30. The flip-flops can be construed with two

A. NAND Gates

B. XOR Gates

C. AND Gates

D. NOT Gates

31. Unused states are treated as Don't cares conditions during the

A. Design of a circuit

B. Execution

C. Plus trigger

D. Edge trigger

32. In mealy models output are the functions of both

A. Present state

B. Input state

C. Next state

D. Both input and present state.

33. A J-K lip-lop has its J-input connected to logic level 1 and its input to the Q output pulse is fed to its clock input the flip-flop will now

A. Change its state at each clock pulse

B. Go to state 1 and stay there

C. Go to state 0 and stay there

D. Retain its present state

34. When an inverter is placed between both inputs of an SR flip-flop, then resulting flip-flop is

A. JK flip-flop

B. D flip-flop

C. SR flip-flop

D. Master slave JK flip-flop

35. If the input J is connected through K input of J-K, then flip-flop will behave as a

a. D type flip-flop

b. T type flip-flop

c. S-R flip-flop

d. Master slave JK flip-flop

36. The table, which is not part of the analysis of asynchronous sequential circuits

A.Transition Table

B. Flow Table

C. State Table

D. Excitation Table

37 In asynchronous circuit, the changes occur with the change of

A. input

B. output

C. clock pulse

D. time

38 The present states and next state of asynchronous circuits are also called

A. secondary variables

B. primary variables

C. excitation variables

D. short term memory

39 In all the cases final stable state is

A. changed

B. same

C. inverted

D. undefined

40 A ripple counter's speed is limited by the propagation delay of _____

a) Each flip-flop

b) All flip-flops and gates

c) The flip-flops only with gates

d) Only circuit gates

41 How many flip-flops are required to construct a decade counter?

a) 4

b) 8

c) 5

d) 10

42 The time sequence for flip flop can be enumerated by_____

A. State table

B. Map

C. Truth table

D. Graphs

43. How many flip-flops are required to make a MOD-32 binary counter?

A. 3

B. 45

C. 5

D. 6

44 It is difficult to design asynchronous sequential circuit because

A. External clock is to be provided

B. It is more complex

C. common clock pulse

D. Generally they involve stability problem

45 A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(total)) is _____

A. 12 ms

B. 24 ns

C. 48 ns

D. 60 ns

46 How many different states does a 3-bit asynchronous counter have?

A. 2

B. 4

C. 8

D. 16

47. A Condition occurs when an Asynchronous sequential circuit changes two or more binary states variables

A. deadlock condition

B. Running condition

C. Race condition

D. No change

48. A 4-bit ripple counter consists of flip-flops, which each have a propagation delay from clock to Q output of 15 ns. For the counter to recycle from 1111 to 0000, it takes a total of _____

A. 15 ns

B. 30 ns

C. 45 ns

D. 60 ns

49. Internal propagation delay of asynchronous counter is removed by _____

A. Ripple counter

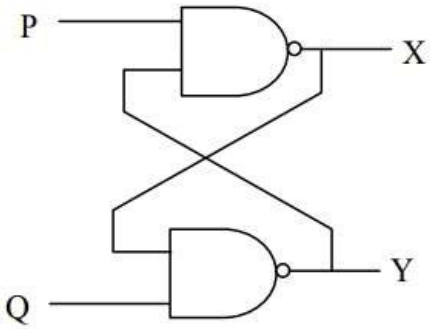
B. Ring counter

C. Modulus counter

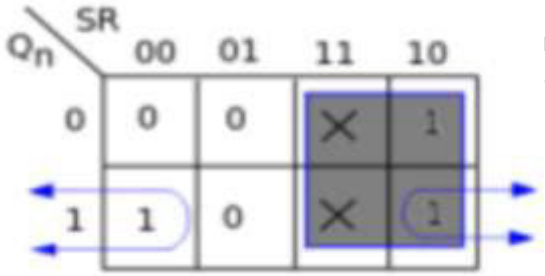
D. Synchronous counter

Part B (2 Mark)

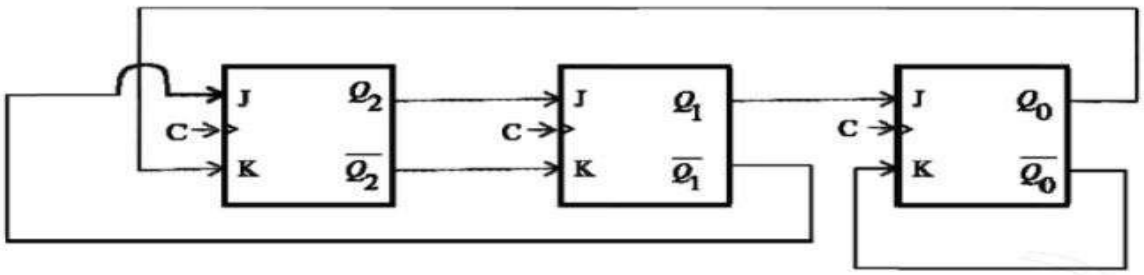
1. In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is: P = Q = "0". If the input condition is changed simultaneously to P = Q = "1", the outputs X and Y are



2 What would be the characteristic equation of SR latch corresponding to the K-map schematic shown below?



3. The below sequential circuit is built using JK flip-flops is initialized with Q2Q1Q0 = 000. The state sequence for this circuit for the next 3 clock cycle is



4 Discuss the difference between combinational and sequential circuit

5 what is the difference between two types of edge triggering

6 what is mean by edge triggering

7 differentiate synchronous and asynchronous sequential circuit.

8 What do you mean by critical and non- critical races? How can they be avoided?

9 what is a master slave flip flop

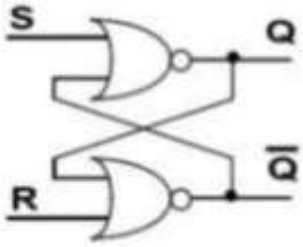
10 If the frequency of a T flip flop is 2000 kHz, what will be the output frequency? Give reason for your answer.

11 Define state table.

12 Why is state reduction necessary?

Part C (3 Mark)

1. Analyze the following Circuit

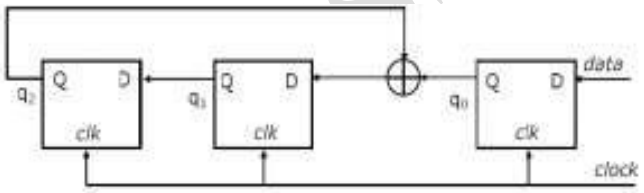


(i). Is the above circuit is combinational Logic Circuit?

(ii). Differentiate combinational Logic Circuit and Sequential Logic Circuit.

(iii). Give the truth table of above circuit

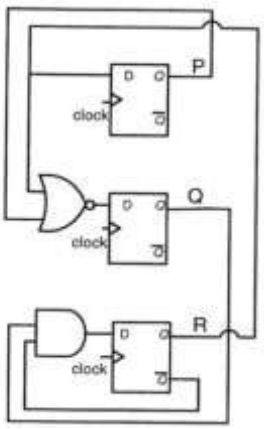
2. Consider the circuit in the diagram. The $\oplus$ operator represents Ex-OR. The D flipflops are initialized to zeroes (cleared)



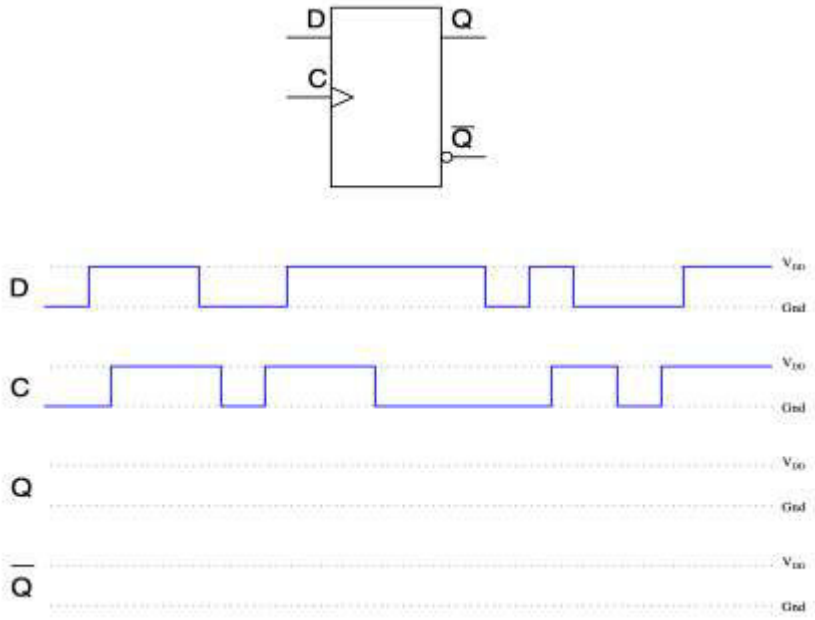
.

The following data: 100110000 is supplied to the "data" terminal in nine clock cycles. After that the values of q2q1q0 are:

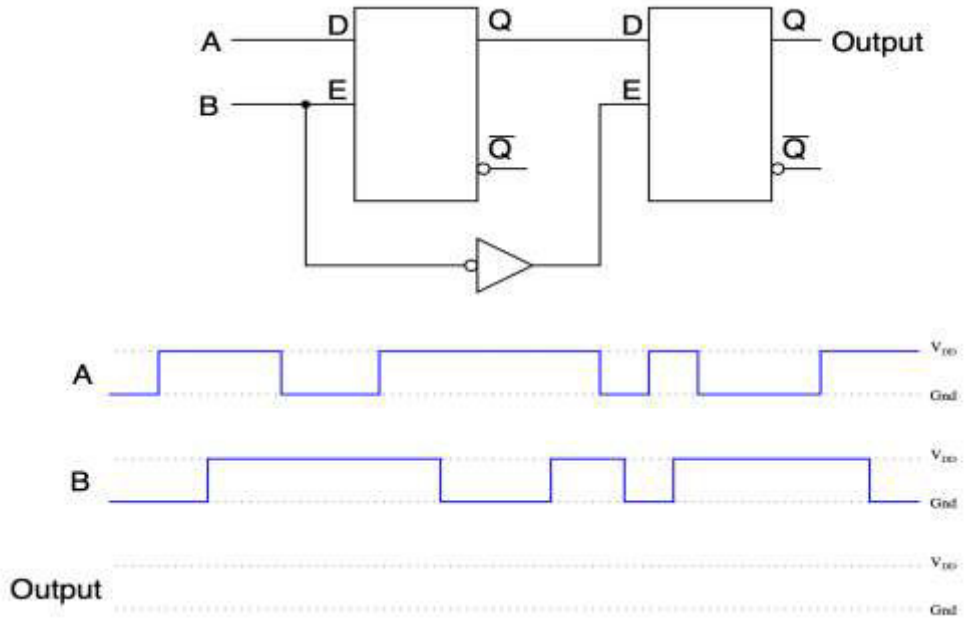
3 Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration. If at some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge?



4 Determine the output states for this D flip-flop, given the pulse inputs shown:

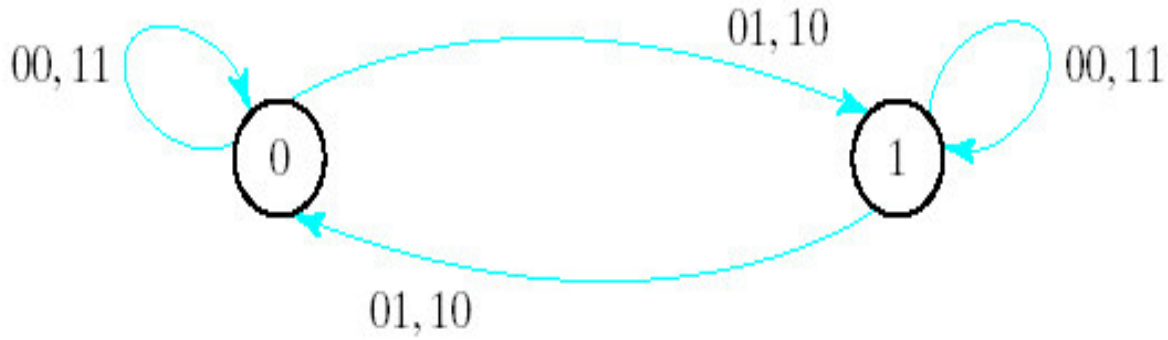


5 Determine the final output states over time for the following circuit, built from D-type gated latches:

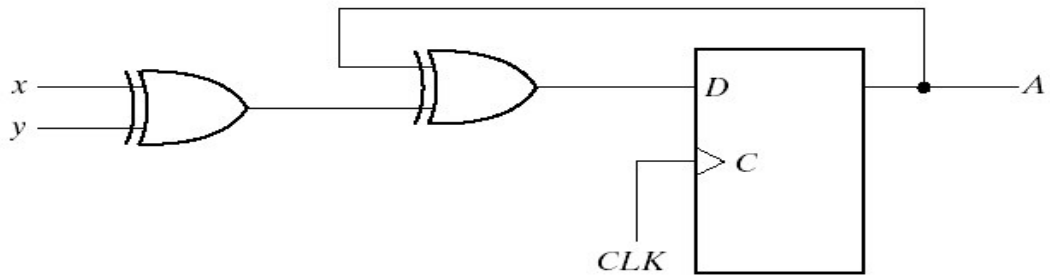


6 How do you eliminate the race around condition in a JK flip-flop and also realize JK flip-flop using D flip-flop.?

7 Construct state table for following state diagram



8. Analysis this circuit and provide the state table and state diagram for this circuit.



(a) Circuit diagram

9 Draw the logic diagram of Master slave JK flip flop

10 Give the characteristics equation and state diagram of JK flip flop

11 Give the excitation table of SR flip flop

12 Give the excitation table of JK flip flop

1 The output of the sequential circuit depends upon _____
a.Present input
b.Past input
c.Present input and present state
d.Past Output

2 The standard form of S-R flip flop is
a.Simple-Reset
b.Set Reset
c.Single-Reset
d.double-Reset

3 Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?
a.Low input voltages
b.Synchronous operation
c.Gate impedance
d.Cross coupling

4 The basic latch consists of _____
a.Two inverters
b.Two comparators
c.Two amplifiers
d.Two adders

5 Flip flop is
a.edge triggered
b.level triggered
c.positive edge triggered
d.positive level triggered

6 The around condition in J-K flip-flop occurs if,
a.J=0,k=0,Clk=1
b.J=0,k=1,Clk=1
c.J=1,k=1,Clk=1
d.J=1,k=0,Clk=1

7 When the set is disabled and reset is enabled in S-R flip flop then the output will be _____
a.Set
b.Reset
c.No change
d.Indeterminate

8 _____ are the applications of flip flop
a.Registers
b.Counters
c.Storage devices
d.Options a,b,c

9 The Asynchronous sequential circuit has
a.No delay
b.Delay
c.Minimum delay
d.Maximum delay

10 The states in Asynchronous sequential circuit flow table is represented by
a. Numbers
b. Letters
c.Alphanumeric
d.Special characters

1 The input to a latch is
a.inputs,clock
b.inputs,clear
c.inputs,enable
d.Both a and b

2 The standard form of D flip flop?
a.Data
b.Deterministic
c.Delay
d.Data and Delay

3 The toggle condition occurs in JK flip flop when
a.J=1, K=1
b.J=0, K=0
c.J=1, K=0
d.J=0, K=1

4 The inputs of the SR, JK, and D flip flop are the _____ inputs
a.Bidirectional
b.Unidirectional
c.Synchronous
d.Asynchronous

5 The Master Slave JK Flip Flop is designed with
a.4 Nand gates
b.4 Nor gates
c.8 Nand gates
d.8 Nor gates

6 The flip flop works with _____
a.Binary inputs
b.Clock signal
c.Clear signal
d.Both a and b

7 The standard form of T flip flop?
a.Trigger
b.Toggle
c.Trigger or toggled
d.Partially triggered

8 The operation mode steady state condition in Asynchronous sequential circuit is given by
a.current states
b.next states
c.previous states
d.Both a and b

9 The states in Asynchronous sequential circuit flow table is represented by
a. Numbers
b. Letters
c.Alphanumeric
d.Special characters

10 The relationship that exists among the inputs, outputs, present states and next states is given by
a.Truth table

b.State table
c.Flow table
d.Transition table