**Part – A**

1. The logical expression Y=AB+AC+BC is known as
   A. Standard Sum of Product form
   B. Sum of Product form
   C. standard Product of Sum form
   D. Product of Sum form

   ANSWER: B
2. The number of cells in 6 variable K-map is
   A. 4
   B. 16
   C. 32
   D. 64

   ANSWER: D
3. On a K-Map, grouping the 0s produces
   A. SoP expression
   B. PoS expression
   C. a don't care condition
   D. AND-OR expression

   ANSWER: B
4. In K map, for M variable, ____ cells are required.
   A. M
   B. $2^M$
   C. $2^{2M}$
   D. M*M

   ANSWER: B
5. In Boolean algebra XY+XY' +X'Y is equal to
   A. X
   B. Y
   C. XY
   D. X+Y

   ANSWER: D
6. Simplified form of A + A'B +A'B'C +A'B'C'D is equal to
   A. A
   B. A+B

C. A+B+C

D. A+B+C+D

ANSWER: D

7. The code used for labeling the cells of a K-map is

A. 8-4-2-1 binary

B. Hexadecimal

C. Grey

D. Octal

Answer C

8. The Quine– McClusky method of minimization of a logic expression is a (i) graphical method (ii) algebraic method (iii) tabular method (iv) a computer-oriented algorithm The correct answers are

A. (iii) and (iv)

B. (ii) and (iv)

C. (i) and (iii)

D. (i) and (ii)

Answer: A

9. In simplification of a Boolean function of n variables, a group of 2m adjacent 1s leads to a term with

A. m – 1 literals less than the total number of variables

B. m + 1 literals less than the total number of variables

C. n + m literals

D. n – m literals

Answer: D

10. Which one of the following devices has a greater number of inputs than outputs?

(a) encoder

(b) decoder

(c) multiplexer

(d) demultiplexer

Ans: (c)

11. What is the number of selection lines required in a single input, n-output demultiplexer?

(a) 2

(b) n

(c) 2^n

(d) log(base-2) n

Ans: (d)

12. A 1-to-8 demultiplexer has _____ select input lines.

(a) 2

(b) 3

(c) 8

(d) 4

Ans: (b)

13. A 32 to 1 multiplexer has the following terminals

(a) 32 outputs, one input and 5 control signals

(b) 32 inputs, one output and 5 control signals

(c) 5 inputs, one control signal and 32 outputs

(d) 5 inputs 32 control signals and one output

Ans:(b)

14. The following switching function is to be implemented using multiplexer $f = \sum m(1, 2, 4, 8, 14, 45)$. What is the size of multiplexer?

(a) 8-to-1 line

(b) 16-to-1 line

(c) 32-to-1 line

(d) 64-to-1 line

Ans: (d)

15. In 16:4 priority encoder, highest priority is given on

(a) A

(b) 0

(c) 9

(d) F

Ans: (d)

16. The following switching function is to be implemented using decoder.

$f = \sum m(1, 2, 4, 8, 14)$. What is the size of decoder?

(a) 2-to-4 line

(b) 3-to-8 line

(c) 4-to-16 line

(d) 5-to-32 line

Ans: (c)

17. Size of decoder needed to design 16-to-1 line multiplexer.

(a) 2-to-4 line decoder

(b) 3-to-8 line decoder

(c) 4-to-16 line decoder

(d) 5-to-32 line decoder

Ans: (c)

18. ABCD decoder has

(a) Four input lines and 16 output lines

(b) Four selection lines, one input line and 16 output lines

(c) Sixteen input lines and four output lines

(d) Four input lines and ten output lines

Ans: (a)

19. Full adder circuit adds _____number of bits at a time

a) 5

b) 2

c) 5

d) 3

ANSWER :D

20. The Half adder circuit is implemented by

A) Using one XOR and one AND gate

B) Using one XNOR and one OR gate

C) Using two XOR and one AND gate

D) Using two XNOR and one OR gate

ANSWER :A

21. How many full adder required to design 4 -bit parallel adder ?

A) 2

B) 4

C) 5

D) 3

ANSWER :B

22. The half subtractor logical expression for borrow is

A) A XOR B

B) AB

C) A'B

D) A’B’

ANSWER : C

23. The carry propagation delay reduced by

A)Carry look ahead adder

B) Full addrer

C) Full subtractor

D) 4 -bit parallel adder

Answer: A

24. The output sum expression for carry look ahead adder is

A) $S_i = P_i + C_i$

B) $S_i = G_i + P_i C_i$

C) $S_i = P_i$ XOR $C_i$

D) $S_i = G_i$ XOR $P_i C_i$

ANSWER: C

25. Decimal adder is also called as

A) Binary adder

B) 4 – bit parallel adder

C) Carry look ahead adder

D) BCD adder

ANSWER: D

26. The carry output of the lower order stage is connected to the carry input of the next higher order stage will be

A) Ripple carry adder

B) full adder

C) Half adder

D) Decimal adder

ANSWER : A

27. The carry of the 4-bit parallel adder is connected to 1 then the carry -output is

A) That carry-out will be LOW

B) That carry-out will be HIGH

C) A one will be added to the final result

D) The carry-out is ignored

ANSWER: C

28. The four-bit parallel adder will perform subtraction by

A) Inverting the outputs

B) Inverting the carry-in

C) Inverting the second inputs

D) Inverting the carry-out

ANSWER: C

29. In 4-bit full adder the carry propagation delay is

A) cumulative for each stage and limits the speed at which arithmetic operations are performed

B) normally not a consideration because the delays are usually in the nanosecond range

C) Decreases in direct ratio to the total number of full-adder stages

D) Increases in direct ratio to the total number of full-adder stages, but is not a factor in limiting the speed of arithmetic operations

ANSWER: A

30. In decimal adder,the decimal number 10 is represented as _____

A) 10100000

B) 01010111

C) 00010000

D) 00101011

ANSWER: C

31. A three-digit decimal number of needs _____ for illustration in the BCD format.

a) 3 bits

b) 6 bits

c) 12 bits

d) 24 bits

ANSWER: C

32. In BCD adder A = 0101 and B = 1001. find the output Y.

A. 1110

B. 0001 0100

C. 1111

D. 0000 1110

ANSWER :B

33. The expression for C3 in Carry Propagation–Look-Ahead Carry generator is

a. G2 + P2G1 + P2P1G0 + P2P1P0C0

b. $G1 + P1G0 + P1P0C0$

c. $G0 + P0C0$

d. $G1 + P1 (G0 + P0C0)$

Answer : A

34. In 2-bit magnitude comparator $A_1A_O = 11$ and $B_1B_O = 01$ then A< B will be

A) 0

B) 1

C) A

D) B

ANSWER: A

35. Which one is a basic comparator?

a) XOR

b) XNOR

c) AND

d) NAND

Answer: a

36. A circuit that compares two numbers and determine their magnitude is called_____

a) Height comparator

b) Size comparator

c) Comparator

d) Magnitude comparator

Answer: d

37. If A = 1010 & B= 0101 then the comparator output is

a) a > b

b) a – b

c) a < b

d) a = b

Answer : a

38. Data stored in ROM is

a. Non-volatile

b. Volatile

c. Secondary

d. Primary

Answer : a

39. EPROM can be erased by

a. Electric pulses
b. UV Light
c. Sound waves
d. Cannot be erased

Answer : b

40. The fundamental building block of a CPU is

a. Memory block
b. Arithmetic and Logic unit block
c. Power Supply module
d. None of the above

Answer : a

41. Total memory capacity of ROM is

a. $2^n$
b. $2^n$-1
c. $2^n$*m
d. $2^n$+m

Answer : c

42. The description of circuit in VHDL refers to register transfers level

a) Structural description
b) Dataflow description
c) Hierarchical Description
d) Behavioral Description

Answer : d

43. Behavioral descriptions use the keyword…….. followed by a list of procedural assignment statements

a) always
b) reg
c) input
d) endmodule

Answer : a

44. The most basic form of behavioral modeling in VHDL is _____

a) IF statements

b) Assignment statements

c) Loop statements

d) WAIT statements

Answer : b

45. Which model in system modelling depicts the dynamic behaviour of the system ?

a) Context Model

b) Behavioral Model

c) Data Model

d) Object Model

Answer : b

46. Which of the following doesn't corresponds to NAND gate?

a) y <= NOT( a AND b)

b) y <= NOT a OR NOT b

c) y <= NOT a AND NOT b

d) WITH ab SELECT

y <= 0 WHEN "11"

1 WHEN OTHERS

Answer : c

47. The inputs in the PLD is given through _____

a) NAND gates

b) OR gates

c) NOR gates

d) AND gates

Answer: d

48. PAL refers to _____

a) Programmable Array Loaded

b) Programmable Logic Array

c) Programmable Array Logic

d) Programmable AND Logic

Answer: c

49. PLA contains _____

a) AND and OR arrays

b) NAND and OR arrays

c) NOT and AND arrays

d) NOR and OR arrays

Answer: a

50. PLA is used to implement _____

a) A complex sequential circuit

b) A simple sequential circuit

c) A complex combinational circuit

d) A simple combinational circuit

Answer: c

51. If a PAL has been programmed once _____

a) Its logic capacity is lost

b) Its outputs are only active HIGH

c) Its outputs are only active LOW

d) It cannot be reprogrammed

Answer: d

52. Simplify the Boolean expression: XY + X(Y+Z) + Y(Y+Z)

A. XY+Z

B. XZ

C. Y+XZ

D. Y

ANSWER: C

53. A switching function f(A,B,C) = (A+B'+C) (A+B'+C') (A'+B'+C) can also be written as

A. ∏(1,4,5)

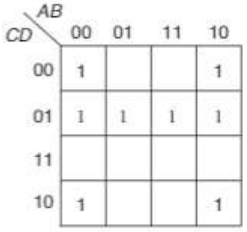
B. ∏(2,4,6)

C. ∏(0,2,4)

D. ∏(3,4,5)

ANSWER: A

54. The minimized expression for the given K-map is



A. B'CD' + B'C'D' +C'D

B. B'D' + C'D

C. A'BCD + AB'CD + ABC' + A'B'C'

D. C'D' + AB'C + A'BCD + AB'C

ANSWER: B

55. The logical expression Y=∑m(0,4,6,7,10,11,14) is equivalent to

A. ∏(0,3,6,7,10,12,15)

B. ∏(1,2,3,5,8,9,12,13,15)

C. ∑(1,2,4,5,8,9,11,13,14)

D. ∑(0,2,4,6,8,10,12,14)

ANSWER: B

56. What is the simplified form of the following Boolean function F= ∑(4,6,8,10,11,12,15) using K-map is __

A. ACD+AB'D'+A'BD'

B. AC'D+A'CD'+AB'D'+A'BD'

C. AC'D'+ACD+AB'D'+A'BD'

D. AC'D+ACD+A'BD'+AB'CD'

ANSWER: C

57. In Boolean algebra XY+XY' +X'Y is equal to

A. X

B. Y

C. XY

D. X+Y

ANSWER: D

58. Simplified form of A + A'B +A'B'C +A'B'C'D is equal to

A. A

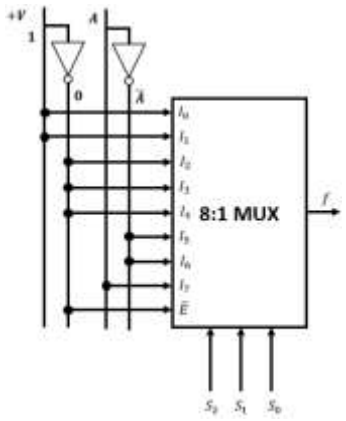
B. A+B

C. A+B+C

D. A+B+C+D

ANSWER: D

59. Which one of the following Boolean function is correct for the given multiplexer circuit?




(a) f = ∑m(0,1,3,4,8,9,15)

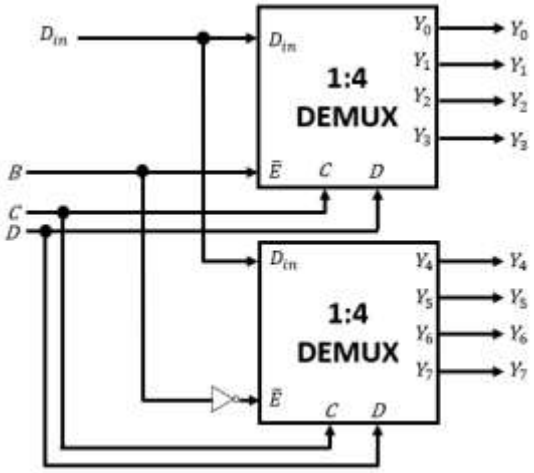
(b) f = ∑m(2,3,4,7,10,11,12,13,14)

(c) f = ΠM(2,3,4,7,10,11,12,13,14)

(d) f = ΠM(2,5,6,7,10,11,12,13,14)

Ans: (c)

60. At which condition, the below demultiplexer circuit output $Y_3$ and $Y_6$ become 1? Verify with output function of $Y_3$ and $Y_6$.




(a) Din = 1, B = 0, C = 1, D = 1 and Din = 1, B = 1, C = 1, D = 1

(b) Din = 1, B = 1, C = 1, D = 1 and Din = 1, B = 0, C = 1, D = 1

(c) Din = 1, B = 0, C = 1, D = 0 and Din = 1, B = 1, C = 1, D = 1

(d) Din = 1, B = 0, C = 1, D = 1 and Din = 1, B = 1, C = 1, D = 0

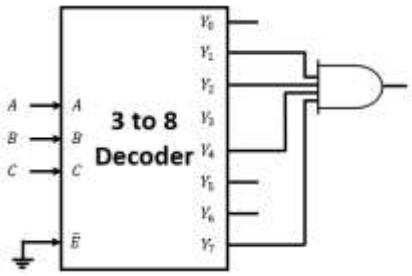
Ans: (d)

61. Which one of the following circuits is correct for the given truth table?

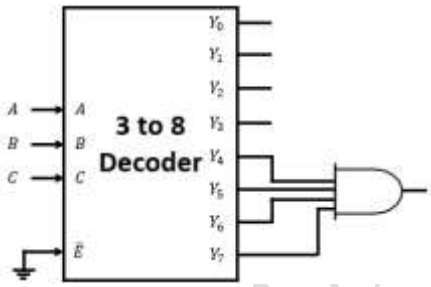
| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |

| | | | |
|---|---|---|---|
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

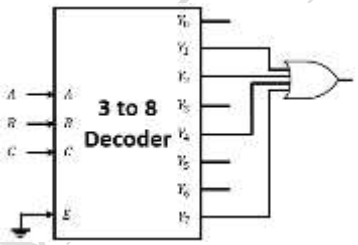
(a)



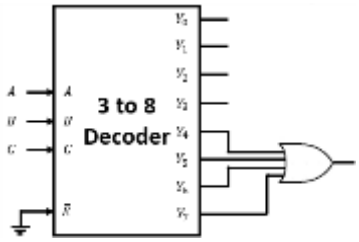

(b)




(c)




(d)




Ans: (c)

62. Which one of the following expressions is correct for hexa to binary encoder?

(a) B3 = I4 + I5 + I6 + I7 + I8 + I9 + I10 + I11

(b) B2 = I2 + I3 + I4 + I5 + I10 + I11 + I12 + I13

(c) B1 = I2 + I3 + I6 + I7 + I10 + I11 + I14 +I15

(d) B0 = I1 + I3 + I5 + I6 + I8 + I10 + I12 + I14

Ans: (c)

63 Designed expression for carry of full adder is

A) AB + AC+ BC

B) AB + AC

C) A' XOR B' XOR c'

D) A XOR B XOR c

ANSWER :A

64. In 4 – bit parallel adder A = 1011 and B = 0011. Find the 4-bit input carry.

A) 0110

B) 0011

C)1010

D)1011

ANSWER: A

65 In two-bit magnitude comparator the logical expression for A > B is

A) $A_1 B_1' + A_0 B_1' B_0' + A_1 A_0 B_O'$

B) $A_1' B_1 + A_0' B_1 B_0' + A_1 A_0' B_O'$

C) $A_1 B_1 + A_0 B_1 B_0 + A_1 A_0 B_O$

D) $A_1' B_1 + A_0' B_1 B_0 + A_1' A'_0 B_O$

ANSWER: A

66 In two-bit magnitude comparator the logical expression for A < B is

A) $A_1 B_1' + A_0 B_1' B_0' + A_1 A_0 B_O'$

B) $A_1' B_1 + A_0' B_1 B_0' + A_1 A_0' B_O'$

C) $A_1 B_1 + A_0 B_1 B_0 + A_1 A_0 B_O$

D) $A_1' B_1 + A_0' B_1 B_0 + A_1' A'_0 B_O$

ANSWER: d

67. What logic circuit is described by the following code?

ARCHITECTURE gate OF my_gate IS

BEGIN

WITH ab SELECT

y<= 0 WHEN "01" OR "10";

1 WHEN OTHERS;

END gate;

a) NAND

b) NOR

c) EXOR

d) EXNOR

Answer : d

**Part – B (2 marks)**

1. What is a half order? Write its truth table
2. What is a full order
3. Design a half subtractor using only basic gates
4. Design a half adder using only basic gates
5. What is the function of a multiplexer select input?
6. How does encoder difference from decoder
7. Describe the application of multiplexer
8. What is the function of a decoder's enable input(s)?
9. How does a priority encoder differ from an ordinary encoder
10. What is mean by magnitude comparator
11. What is demultiplexer? Explain the difference between a DEMUX and MUX
12. Define combinational logic circuit
13. What do you mean by propagation delay?
14. Write a short notes on one bit comparator
15. What will be the maximum number of outputs for a decoder with a 6 bit data word?
16. What is a data selector
17. Difference between decoder and encoder
18. What are the various modelling technique in HDL?
19. What is behavioural modelling?
20. What is data flow modelling?

**Part – C (3 marks)**

1. Implement the following Boolean function with the help of 4:1 Mux.
   f(A,B,C,D) = ΠM(1,2,4,7,11,13,15).
2. Implement the full subtractor with the help of 2:4 decoder.

3. Implementation the full-subtractor using  two half-subtractors.
4. Show how a full order can be converted to a full subtractor with the addition of an inverter circuit.
5. Describe the truth table of a half subtractror and write the Boolean expression corresponding tot eh difference and borrow.
6. Design a 4-bit Carry Propagation–Look-Ahead Carry generator
7. Design a 1- bit magnitude comparator .
8. Design a 8x4 PROM with 3 input and 4 output lines.
9. Explain the data flow level programing of 4-to-1 Multiplexer using VHDL?

```
//4-to-1 Mux: Dataflow description
module mux_4_to_1(S,D,Y);
        input [1:0]S;
        input [3:0]D;
        output Y;
        assign Y = (~S[1]&~S[0]&D[0])|(~S[1]&S[0]&D[1])
        |(S[1]&~S[0]&D[2])|(S[1]&S[0]&D[3]);
endmodule
```

8.Write difference between a PAL & PLA.