SRM Institute of Science and Technology, Ramapuram Campus

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
Degree/Branch: B.Tech / CSE

Year/Sem: II / III

Subject Code:18CSC203J

Subject Name: Computer Organization and Architecture

Question Bank

Unit III

PART-A

Q.No	Question	BLOOMS LEVEL	CLO
1.	The general purpose registers are combined into a block called as _____. **a) Register bank** b) Register Case c) Register file d) None of the above	L1	CLO3
2.	In _____ technology, the implementation of the register file is by using an array of memory locations. **a) VLSI** b) ANSI c) ISA d) ASCI	L1	CLO3
3.	In a three BUS architecture, how many input and output ports are there ? a) 2 output and 2 input **b) 1 output and 2 input** c) 2 output and 1 input d) 1 output and 1 input	L1	CLO3
4.	The main advantage of multiple bus organization over single bus is, a) Reduction in the number of cycles for execution b) Increase in size of the registers **c) Better Connectivity** d) None of these	L1	CLO3
5.	CISC stands for, a) Complete Instruction Sequential Compilation b) Computer Integrated Sequential Compiler **c) Complex Instruction Set Computer** d) Complex Instruction Sequential Compilation	L1	CLO3
6.	. If the instruction Add R1,R2,R3 is executed in a system which is pipelined, then the value of S is (Where S is term of the Basic performance equation) a) 3 **b) ~2** c) ~1 d) 6	L1	CLO3
7.	In multiple BUS organisation _____ is used to select any of the BUSes for input into ALU.	L1	CLO3

	a) MUX b) DE-MUX c) En-CDS d) None of the above		
8.	_____ are the different type/s of generating control signals. a) Micro-programmed b) Hardwired c) Micro-instruction **d) Both a and b**	L1	CLO3
9.	The type of control signal are generated based on, a) contents of the step counter b) Contents of IR c) Contents of condition flags d) All of the above	L1	CLO3
10.	What does the hardwired control generator consist of ? a) Decoder/encoder b) Condition codes c) Control step counter d) All of the above	L1	CLO3
11.	What does the end instruction do ? **a) It ends the generation of a signal** b) It ends the complete generation process c) It starts a new instruction fetch cycle and resets the counter d) It is used to shift the control to the processor	L1	CLO3
12.	What does the RUN signal do ? a) It causes the termination of a signal b) It causes a particular signal to perform its operation **c) It causes a particular signal to end** d) It increments the step counter by one	L1	CLO3
13.	The benefit of using hardwired approach is a) It is cost effective b) It is highly efficient **c) It is very reliable** d) It increases the speed of operation	L1	CLO3
14.	The disadvantage/s of the hardwired approach is a) It is less flexible b) It cannot be used for complex instructions **c) It is costly** d) Both a and b	L1	CLO3
15.	In micro-programmed approach, the signals are generated by _____. **a) Machine instructions** b) System programs c) Utility tools d) None of the above	L1	CLO3
16.	A word whose individual bits represent a control signal is _____. a) Command word **b) Control word** c) Co-ordination word d) Generation word	L1	CLO3
17.	A sequence of control words corresponding to a control sequence is called _____.	L1	CLO3

	a) Micro routine b) Micro function c) Micro procedure d) None of the above		
18.	. Individual control words of the micro routine are called as _____. a) Micro task b) Micro operation **c) Micro instruction** d) Micro command	L1	CLO3
19.	The special memory used to store the micro routines of a computer is _____. a) Control table **b) Control store** c) Control mart d) Control shop	L1	CLO3
20.	To read the control words sequentially _____ is used. a) PC **b) IR** c) UPC d) None of the above	L1	CLO3
21.	_____ have been developed specifically for pipelined systems. a) Utility software **b) Speed up utilities** c) Optimizing compilers d) None of the mentioned	L2	CLO3
22.	The pipelining process is also called as _____. a) Superscalar operation b) Assembly line operation **c) Von neumann cycle** d) None of the mentioned	L2	CLO3
23.	The fetch and execution cycles are interleaved with the help of _____. a) Modification in processor architecture **b) Clock** c) Special unit d) Control unit	L2	CLO3
24.	Each stage in pipelining should be completed within ____ cycle. a) 1 b) 2 c) 3 **d) 4**	L2	CLO3
25.	If a unit completes its task before the allotted time period, then a) It'll perform some other task in the remaining time b) Its time gets reallocated to different task **c) It'll remain idle for the remaining time** d) None of the mentioned	L2	CLO3
26.	To increase the speed of memory access in pipelining, we make use of _____. a) Special memory locations **b) Special purpose registers** c) Cache d) Buffers	L2	CLO3

27.	The periods of time when the unit is idle is called as _____. a) Stalls b) Bubbles c) Hazards **d) Both a and b**	L2	CLO3
28.	The contention for the usage of a hardware device is called as _____. **a) Structural hazard** b) Stalk c) Deadlock d) None of the mentioned	L2	CLO3
29.	Any condition that causes a processor to stall is called as _____. **a) Hazard** b) Page fault c) System error d) None of the above	L2	CLO3
30.	The periods of time when the unit is idle is called as _____. **a) Stalls** b) Bubbles c) Hazards **d) Both a and b**	L2	CLO3
31.	**Various Hazards** i) The contention for the usage of a hardware device is called as _____. **a) Structural hazard** b) Stalk c) Deadlock d) None of the above ii) The situation where in the data of operands are not available is called _____. **a) Data hazard** b) Stock c) Deadlock d) Structural hazard iii) The stalling of the processor due to the unavailability of the instructions is called as ____. **a) Control hazard** b) Structural hazard c) Input hazard d) None of the above iv) The time lost due to branch instruction is often referred to as _____. a) Latency b) Delay **c) Branch penalty** d) None of the above	L3	CLO3
32.	Algorithm used in Concurrency: i) The algorithm followed in most of the systems to perform out of order execution is _____. **a) Tomasulo algorithm** b) Score carding	L3	CLO3

	c) Reader-writer algorithm d) None of the above ii). The problem where process concurrency becomes an issue is called as _____. a) Philosophers problem b) Bakery problem **c) Bankers problem** d) Reader-writer problem		
33.	Bus Structure: i) Suppose that a bus has 16 data lines and requires 4 cycles of 250 nsecs each to transfer data. The bandwidth of this bus would be 2 Megabytes/sec. If the cycle time of the bus was reduced to 125 nsecs and the number of cycles required for transfer stayed the same what would the bandwidth of the bus? (A) 1 Megabyte/sec (B) 4 Megabytes/sec (C) 8 Megabytes/sec **(D) 2 Megabytes/sec** **ii)** The communication between the components in a microcomputer takes place via the address and (A) I/O bus **(B) Data bus** (C) Address bus (D) Control lines	L3	CLO3
34.	**Micro Programmed Control** **i)** A microprogram sequencer **(A) generates the address of next micro instruction to be executed.** (B) generates the control signals to execute a microinstruction. (C) sequentially averages all microinstructions in the control memory. (D) enables the efficient handling of a micro program subroutine. ii) The operation executed on data stored in registers is called (A) Macro-operation **(B) Micro-operation** (C) Bit-operation (D) Byte-operation	L3	CLO3
35.	Hard Wired Control i) Hardwired control unit uses ____to interpret an instruction **a) Special Program** b) Special micro c) fixed logic d) instruction register ii) While designing hardwired control unit factor to be considered a) amount of hardware used b) Speed of operation c) cost of design **d) all of the above**	L3	CLO3

PART-B

1. Define two stage pipelining and four stage pipelining.
2. Define Hazards and its types.
3. State static branch prediction and dynamic branch prediction.
4. What are the advantages of multiple bus organization over a single bus organization?
5. Write short notes on Micro programmed control unit.
6. Define structural, data, and control hazard.
7. Explain about Microinstruction.
8. With examples explain how to fetch a word from memory and to store a word in memory.

PART-C

1. Describe about hardwired control in detail along with neat diagram.
2. Write and Explain the control steps to execute a straight-line instruction and branch instruction
3. Discuss in detail about the hardwired control unit with block diagram. Compare hardwired and micro programmed control unit**.**
4. Explain Micro programmed control unit with neat diagram**.**
5. What is instruction hazard? Explain in detail how to handle the instruction hazards in pipelining with relevant examples.
6. What is Data Hazard? Explain in detail how to handle the data hazards in pipelining with relevant examples.
7. With neat diagram explain Single and Multi Bus Organization of Processor.
8. Explain influence of hazards on Instruction set.