Part A

1. For a 4-bit universal shift register, the selection lines S_0S_1 = 00 represents _____ operation

a. Locked state (No change)

b. Shift-Left

c. Shift-Right

d. Parallel Loading

Ans : Locked state (No change)

2. For a 4-bit universal shift register, the selection lines S_0S_1 = 01 represents _____ operation

a. Locked state (No change)

b. Shift-Left

c. Shift-Right

d. Parallel Loading

Ans : Shift-Left

3. For a 4-bit universal shift register, the selection lines S_0S_1 = 10 represents _____ operation

a. Locked state (No change)

b. Shift-Left

c. Shift-Right

d. Parallel Loading

Ans : Shift- Right

4. For a 4-bit universal shift register, the selection lines S_0S_1 = 11 represents _____ operation

a. Locked state (No change)

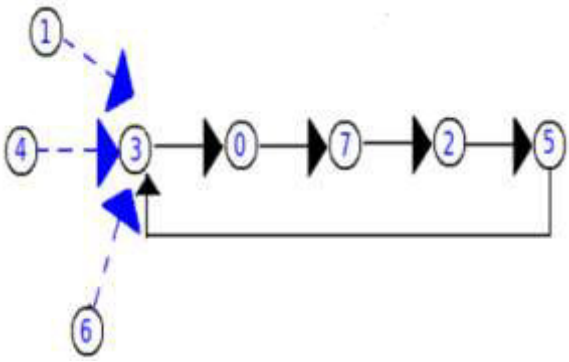
b. Shift-Left

c. Shift-Right

d. Parallel Loading

Ans : Parallel Loading

5. Number of D flipflops required for designing the synchronous counter for the given state diagram is ……



a. 2

b. 3

c. 5

d. 7

Ans: b. 3

6. The propagation delay in synchronous counter is much lesser than that of asynchronous counter due to …….

a. clocking of all flip flops at the same instant

b. increase in number of states

c. absence of connection between output of preceding flip flop and clock of next one

d. absence of mode control operation

Ans: a. clocking of all flip flops at the same instant

7. Ripple counters are also called _____

a) SSI counters

b) Asynchronous counters

c) Synchronous counters

d) VLSI counters

Ans: b) Asynchronous counters

8. In a three-stage counter, using RS flip flops what will be the value of the counter after giving 9 pulses to its input? Assume that the value of counter before giving any pulses is 1.

a) 1

b) 2

c) 9

d) 10

Ans: b) 2

9. A MOD-16 ripple counter is holding the count 1001. What will the count be after 31 clock pulses?

a) 1000

b) 1010

c) 1011

d) 1101

Ans : a) 1000

10. The terminal count of a typical modulus-10 binary counter is _____

a) 0000

b) 1010

c) 1001

d) 1111

Ans: c) 1001

11. **A decimal counter has _____ states.**

a) 5

b) 10

c) 15

d) 20

12. **Three decade counters would have _____**

a) 2 BCD counters

b) 3 BCD counters

c) 4 BCD counters

d) 5 BCD counters

13. The final count of a modulus-11 binary counter is _____.

a) 1000

b) 1100

c) 1010

d) 1011

14. A 4-bit counter has a maximum modulus of _____

a) 3

b) 6

c) 8

d) 16

15. **When two counters are cascaded, the overall MOD number is equal to the _____ of their individual MOD numbers.**

a) product

b) sum

c) log

d) reciprocal

16. **Which of the following is an invalid output state for an 8421 BCD counter?**

a) 1110

b) 0000

c) 0010

d) 1001

17. **The desirable count for a presettable counter is loaded when**

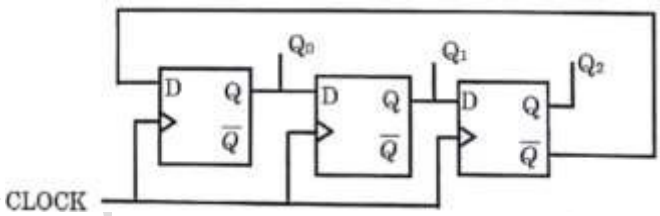
a load = 1 and reset =1

b load = 1 and reset =0

c load = 0 and reset =0

d load = 0 and reset =0 **Ans: b load = 1 and reset =0**

18. **The initial count of the counter is Q0Q1Q2= 010. After 3 clocks the output Q0Q1Q2 will be**



a 101

b 010

c 000

d 111 **Ans: a**

19. **Mod 2 counter and mod 17 counter are cascaded. The modulus of the resultant counter will be**

a mod 34

b mod 9

c mod 17

d mod 2 **Ans: a mod 34**

20. **Among the control signals available in a presettable counter, the least priority is given to**

a clock

b enable

c load

d reset **Ans: a clock**

21. **The final count in a counter designed with 10 T-FFs is**

a 1023

b 1024

c 10

d 1025 **Ans: a 1023**

22. A Seven-segment, common-anode LED display is designed for

a) All cathodes to be wired together

b) One common LED

c) A high signal to turn off each segment

d) Disorientation of segment module

23. Which counter is used for minutes in digital clock?

a) Mod 2 & Decade

b) Mod 12

c) Mod 6 & Decade

d) Mod 5

24 A device which converts BCD to seven segment is called

a) Encoder

b) Decoder

c) Multiplexer

d) Shift register

25. What is the frequency for digital clock circuit

a. 1Hz

b. 50Hz

c. 1KHz

d. 60 Hz

26. The flash type ADC each comparator output is connected to an input of_____

a. priority encoder

b. multiplexer

c. demultiplexer

d. decoder

27. The practical use of binary weighted digital to analog converter is limited to

a. R/2R ladder DAC

b. 4 bit DAC

c. Switched resistor DAC

d. Successive-approximation converter.

28. The resolution of a 6 bit digital to analog converter is

a. 1.56%

b. 15.6%

c. 63%

d. 64%

29. What is the purpose for sample and hold circuit in analog to digital converter?

a. sample and hold the D/A converter staircase waveform during the conversion process

b. stabilize the input analog signal during the conversion process

c. stabilize the comparator's threshold voltage during the conversion process

d. sample and hold the output of the binary counter during the conversion pro

30. Analog to digital conversion includes

(A) quantization

(B) simulation

(C) Data accumulation

(D) summation

31. An 'n' bit analog to digital converter is required to convert analog input in the range (0-5) V to an accuracy of 10 mV. What should be the value of n?

(A) 6

(B) 12

(C) 9

(D) 11

32. An analog voltage in the range of 0-8 V is divided in eight equal intervals for conversion to a 3 bit digital output. The maximum quantization error is

(A) 2 V

(B) 1.32 V

(C) 0.5 V

(D) 1 V

33. A digital volt meter uses a

(A) flash ADC

(B) dual-slope ADC

(C) successive approximation ADC

(D) sigma-delta ADC

34. Which of the following is not a type of ADC?

(A) dual-slope ADC

(B) flash ADC

(C) recessive approximation ADC

(D) sigma-delta ADC

35. The throughput of flash ADC is measured in

(A) distance per second

(B) input voltage per second

(C) samples per second

(D) resolution per second

36 Assume that a 4 bit serial in - parallel out shift register is initially clear. Determine the binary value of the output at 2nd clock pulse for the serial input 1001(first bit – start from right most bit?

a. 1001

b. 0100

c. 0010

d. 0000

Answer: 0100

37 Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first)

a. 1100

b. 0011

c. 0000

d. 1111

Answer: 0000

38 With a 200 kHz clock frequency, eight bits can be serially entered into a shift register in _____

a. 4 μs

b. 40 μs

c. 400 μs

d. 40 ms

Answer: 4 μs

39 Calculate the delay time SISO shift register with 4 stages and 40 kHz clock frequency

a. 0.01 s

b. 0.001 s

c. 0.0001 s

d. 0.00001 s

Ans : 0.0001 s

40 Using four cascaded counters with a total of 16 bits, how many states must be deleted to achieve a modulus of 50,000?

A. 50,000

B. 65,536

C. 25,536

D. 15,536

Answer: D. 15,536

41 A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay (tp(total)) is _____

a) 12 ms

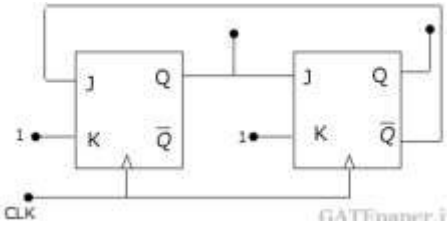
b) 24 ns

c) 48 ns

d) 60 ns

Ans: d) 60 ns

42 Find the modulus of the counter shown in figure



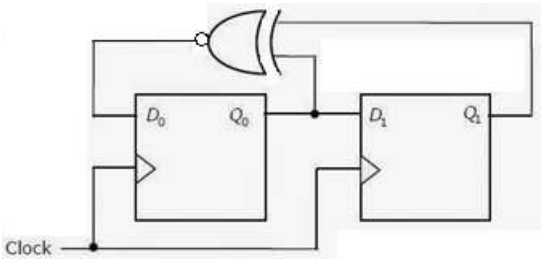
a 1

b 2

c 3

d 4 **Ans: c 3**

43. For the counter shown in figure, the sequence of counter states (Q_0Q_1) are given by (Assume the flipflops are initially reset)



a 10, 01, 00, 10…

b 01, 10, 00, 01…

c 10, 01, 11, 10…

d 01, 10, 11, 01… **ANS: a 10, 01, 00, 10…**

44. BCD input 1000 is fed to a 7-segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are

a) a,b,d

b) a,,b,c

c) a,b,g,c,d

d) a,,b,c,d,e,f,g

Part B (2 Mark)

1. Write the logical expression for the inputs to the D-FF from the state table shown is

Present States		I/p	Next States		O/P
X	Y	C	X'	Y'	
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	0	0
1	1	0	X	X	X
1	1	1	X	X	X

2. A 5-bit binary-weighted DAC has an input voltage at each bit as either 0V or +5V for logic 0 and 1 respectively, Calculate its step size if the feedback resistor is 15Kohm and LSB resistor is 100Kohm.

3. A digital to analog converter with a full-scale output voltage of 3.5 V has a resolution close to 14 mV. Find the bit size.

4. Define shift register

5 what are the different types of shift register

6 What is the difference between serial and parallel transfer?

7 What is the minimum number of flip flop required to implement a modulo 21 synchronous counter?

8 Why are shift register considered to be a memory devices?

9 How are shift left or shift right transfer register built?

10 Explain how a flip flop can store a data bit.

11 Write the different application in flip flop

Part-C (3 Mark)

1. Draw the parallel in serial out circuit diagram.

2. Draw the serial in parallel out circuit diagram and consider the shift register is cleared, assume the input bits are given as '1011' with right most bit as the first bit to enter the shift register. After 2 clock pulses what will be the output bits?

Answer: 1100

3. Write the state transition table for the given synchronous counter for sequence: 0 → 1 → 3 → 4 → 5 → 7 → 0, using T flip-flop

4. Design a modulus 5 asynchronous counter using JK Flipflop.

5. Design a synchronous random counter to count the sequence 2,3,0,1,2… using D – FF.

6. Show the seven segment LED display for which segment illuminated in the input codes of DCBA = 0011.

7. Draw the circuit diagram of R/2R ladder digital to analog converter

8. Write a short note on flash type ADC.

11 The inputs in Asynchronous Fundamental mode sequential circuit are
a.digital
b.pulse
c.alternate signals
d.direct signals

12 The fastest mode of writing and reading data in the shift register is done in
a.Serial In Parallel Out (SIPO)
b.Serial In Serial Out (SISO)
c.Parallel In Serial Out (PISO)
d.Parallel In Parallel Out (PIPO)

13 A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?
a.Tristate
b.End around
c.Universal
d.Conversion

14 A counter circuit is usually constructed of _____
a.A number of latches connected in cascade form
b.A number of NAND gates connected in cascade form
c.A number of flip-flops connected in cascade
d.A number of NOR gates connected in cascade form

15 Modulus Counters are defined based on the ___ counter will sequence through before returning back to its original value
a.number of states
b.number of counts
c.number of iterations
d.number of loops

16 The Common Cathode (CC) in LED 7-segment display connects all
a.Anodes
b.Cathodes
c.Diodes
d. Transistors

17 How can parallel data be taken out of a shift register simultaneously?
a.Use the Q output of the first FF
b.Use the Q output of the last FF
c.Tie all of the Q outputs together
d.Use the Q output of each FF

18 In Synchronous counters, the flip-flops are clocked at the same time by a common
a.signals
b.control line
c. enable
d.clock pulse

19 How many control lines are present in analog to digital converter in addition to reference voltage?
a.Three
b.Two
c.One
d.Four

20 The analog signals are converted to digitals signals with
a.quantizationb.sampling c.decoding d.Both a and b

21 The Shift registers are related to digital
a. Adders
b. Subtractors
c. Comparators
d. Counters

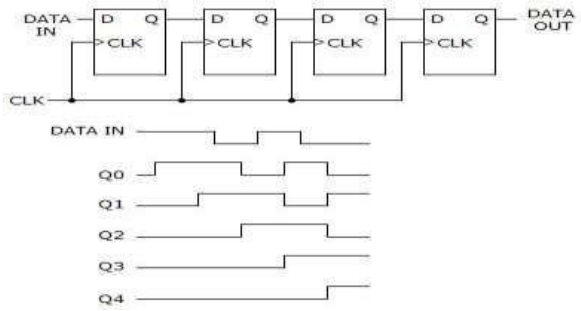
22 The parallel outputs of a counter circuit represent the _____
a.Parallel data word
b.Clock frequency
c.Counter modulus
d.Clock count

23 When two counters are cascaded, the overall MOD number is equal to the _____ of their individual MOD numbers.
a.product
b.sum
c.log
d.reciprocal

24 A BCD counter is a ____.
a.binary counter
b.full-modulus counter
c.decade counter
d.divide-by-10 counter

25 Device which converts BCD to seven segment is called
a.encoder
b.decoder
c.multiplexer
d.demultiplexer

26. The circuit given below fails to produce data output. The individual flip-flops are checked with a logic probe and pulser, and each check OK. What could be causing the problem?



A. The data output line may be grounded.

B. One of the clock input lines may be open.

C. One of the interconnect lines between two stages may have a solder bridge to ground.

D. One of the flip-flops may have a solder bridge between its input and *V*cc.

27. Which statement describes the BEST operation of a negative-edge-triggered D flip-flop?

A. The logic level at the D input is transferred to Q on NGT of CLK

B. The Q output is ALWAYS identical to the CLK input if the D input is HIGH

C. The Q output is ALWAYS identical to the D input when CLK = PGT

D. The Q output is ALWAYS identical to the D input

28. When an inverter is placed between both inputs of an SR flip-flop, then resulting flip-flop is

A. JK flip-flop B. D flip-flop C. SR flip-flop D. Master slave JK flip-flop

29. Assume that a 4 bit serial in - parallel out shift register is initially clear. Determine the binary value of the output at 2nd clock pulse for the serial input 1001(first bit – start from right most bit?

A. 1001 B. 0100 C. 0010 D. 0000

30. With a 200 kHz clock frequency, eight bits can be serially entered into a shift register in _____

A. 4 µs B. 40 µs C. 400 µs D. 40 ms

31. Using four cascaded counters with a total of 16 bits, how many states must be deleted to achieve a modulus of 50,000?

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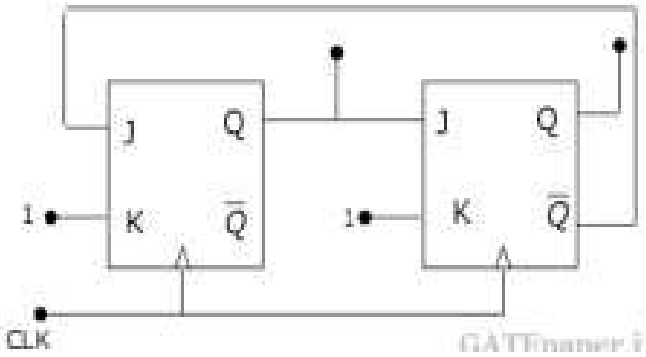
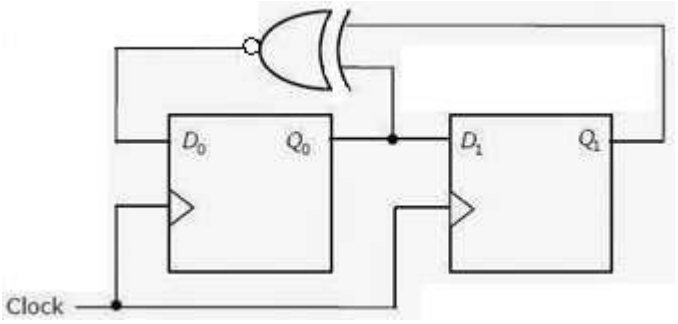
32. Find the modulus of the counter shown in figure



A. 1 B. 2 C. 3 D. 4

33. For the counter shown in figure, the sequence of counter states (Q0Q1) are given by (Assume the flipflops are initially reset)



A. 10, 01, 00, 10… B. 01, 10, 00, 01… C. 10, 01, 11, 10… D. 01, 10, 11, 01…

34. BCD input 1000 is fed to a 7-segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are

A. a,b,d B. a,,b,c C. a,b,g,c,d D. a,,b,c,d,e,f,g

35. A digital to analog converter with a full-scale output voltage of 3.5 V has a resolution close to 14 mV. Find the bit size.

A. 4 B. 8 C. 16 D. 32