DIGITAL ELECTRONICS

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Chapter

1

LOGIC FAMILIES

Chapter Outline

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1.1 INTRODUCTION

Digital logic is concerned with the interconnection among digital components and modules. The best known example of a digital system is the general purpose digital computer. Most of the digital circuits are constructed on a single chip, which are referred to as *integrated circuits* (IC). Integrated circuits contain a large number of interconnected digital circuits within a single small package.

Small scale integration (SSI) and medium scale integration (MSI) devices provide digital functions and large scale integration (LSI) devices provide complete computer modules. It is very important for the logic designer to be familiar with the various digital components encountered in integrated circuit form. It is constructed by basic electronic components such as diodes, transistors, MOSFETs, registers, and capacitors. The complex digital functions can be realized using these basic electronic components in a variety of forms and each form is referred as a *logic family*.

Now-a-days digital integrated circuits are most commonly used in modern digital systems. ICs are popular due to their enormous advantages, as listed below.

- Small in size
- Low cost
- Less power consumption

- High noise margin
- High reliability
- High speed

This chapter includes the study of different logic families, interfacing of logic families, and data sheets of commonly used series 74XX.

1.2 LOGIC FAMILIES

The set of compatible ICs with the same logic levels and same supply voltages have been fabricated to perform the various logic functions known as logic family. Based on the fabrication technology, logic families are classified into two types:

- Bipolar logic family
- Unipolar logic family

Unipolar logic family

In unipolar logic families, unipolar devices are the key element. MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a unipolar device, in which the current flows because of only one type of charge carriers (that is, either electrons or holes). The examples of unipolar families include PMOS, NMOS, and CMOS.

Bipolar logic family

Transistors and diodes are bipolar devices, in which the current flows because of both the charge carriers (electrons and holes). In bipolar logic families, transistors and diodes are used as key elements. On the basis of operations of transistors in ICs, bipolar logic families are further classified as:

- Saturated bipolar logic families
- Unsaturated bipolar logic families

In saturated bipolar logic families, transistors operate in saturation region. The speed of saturated bipolar logic family is low, reasons of which would be discussed in forthcoming topics. Examples of saturated bipolar logic families are:

- Resistor-transistor logic
- Direct coupled transistor logic
- Integrated injection logic
- Diode-transistor logic
- High-threshold logic
- Transistor-transistor logic

In non-saturated bipolar logic families, transistors operate in active region. The speed of non-saturated bipolar logic families is high as compared to saturated logic families. Examples of unsaturated bipolar logic families are:

- Schottky transistor-transistor logic
- Emitter-coupled logic

The transistor is one of the key elements used in logic families. One of the important applications of the transistor is the *switch*.

1.3 TRANSISTOR AS SWITCH

Transistor is one of the basic elements of logic families. It operates as a switch. In switching circuits, transistors operate in cut-off or saturation region. The cut-off condition is referred to as *switch OFF* and saturation is referred to as *switch ON*.

In the cut-off region, both emitter and collector junctions are in reverse-bias condition and only reverse current flows in the transistor, which is negligible.

In the saturation region, both emitter and collector junctions are in forward bias condition. When transistor is operated in the saturation region, voltage across the emitter junction is V_{BEsat} and voltage across emitter and collector terminals is V_{CEsat}. The value of $V_{BEsat} = 0.8$ V for silicon transistor and 0.3 V for germanium transistor. The value of $V_{CEsat} = 0.2$ for silicon transistor and 0.1 V for germanium transistor. The condition to operate the transistor in saturation is that the base current should be greater than the collector current by β, that is, $[I_B > I_C/\beta]$.

The circuit of a transistor working as a switch is shown in Fig. 1.1.

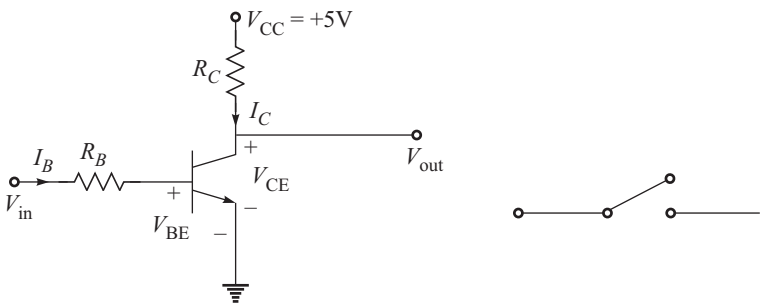


Fig. 1.1 Transistor as a switch

When input V_{in} applied to the transistor is LOW (0 V), the emitter junction is reverse biased, there is no current flowing through the base terminal and the current flowing through the collector terminal is reverse saturation current, which is negligible.

By applying KVL to the output loop,

$$V_{CC} - I_C R_C - V_{out} = 0$$

$$V_{out} = V_{CC} - I_C R_C \tag{1.1}$$

In the cut-off region, collector current $I_C = 0$

$$V_{out} = V_{CC} \tag{1.2}$$

When the transistor is operating in cut-off, the output is equal to V_{CC} and it is referred to as HIGH (logic 1).

When input V_{in} that is applied to the transistor is HIGH (+5 V), the emitter junction is forward biased, current flowing through the base terminal is sufficient and the transistor operates in saturation region. Current flows through the collector terminal and there is a considerable voltage drop across the collector resistor. And output voltage is

$$V_{out} = V_{CEsat} \tag{1.3}$$

When the transistor is operating in saturation, the output is equal to V_{CEsat} and it is referred to as LOW (logic 0). Transistor is either ON or OFF and it is controlled by the input voltage.

The response of a transistor switch for a square wave input is shown in Fig. 1.2.

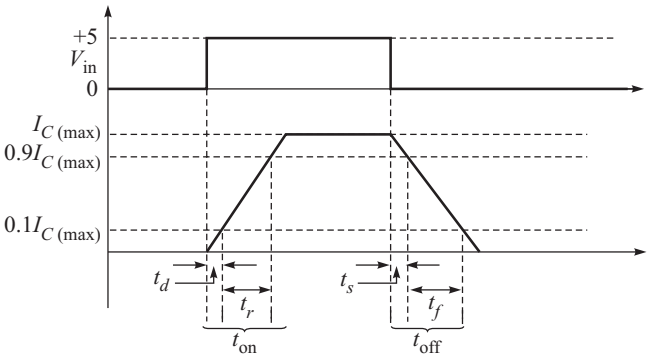


Fig. 1.2 Response of transistor switch for square wave input

When a transistor switches from OFF to ON state, the charge built up requires time to reach the steady-state condition. Similarly when it switches from ON to OFF state, the excess charge stored must be removed which takes some time.

Turn-ON time It is the time required to reach the steady state condition when the input changes from low to high.

$$t_{ON} = t_d + t_r \tag{1.4}$$

where t_d is delay time and t_r is rise time.

Delay time It is the time required for the collector current to rise from 0 to 10 percent of the maximum value of the collector current.

Rise time It is the time required for the collector current to rise from 10 to 90 percent of the maximum value of the collector current.

Turn-OFF time It is the time required to remove the excess charge stored near the junction, when the input changes from high to low.

$$t_{OFF} = t_f + t_s \tag{1.5}$$

where t_f is fall time and t_s is storage time.

Storage time It is the time required to drop the collector current to 90 percent of the maximum value of the collector current when the input changes from high to low.

Fall time It is the time required to drop the collector current from 90 to 10 percent of the maximum value of the collector current.

1.4 CHARACTERISTICS OF DIGITAL ICs

There are various logic families and the selection of a family for a particular application is based on its characteristics. Real time applications demand high speed logic families and hence it is necessary to study the characteristics of digital ICs. Following are the parameters used to compare the performance of digital ICs:

- Speed of operation
- Power dissipation

- Figure of merit
- Fan-out
- Fan-in
- Current and voltage parameters
- Noise Immunity
- Power supply requirements
- Operating temperature

1.4.1 Speed of Operation

The speed of operation of digital ICs should be high. It is specified in terms of *propagation delay time*. It is the average of the propagation delay times from high to low state and low to high state.

$$t_p = \frac{t_{PHL} + t_{PLH}}{2} \tag{1.6}$$

where t_{PHL} is the delay time measured, when output changes from high to low state, and t_{PLH} is the delay time measured, when output changes from low to high state. The input and output voltage waveforms of a logic gate are shown in Fig. 1.3.

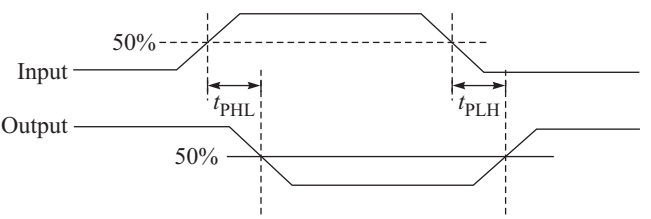


Fig. 1.3 Input and output voltage waveforms of logic gate

The delay times are measured between 50 percent voltage levels of input and output waveforms.

The propagation delay between input and output should be as minimum as possible so that the operating speed of IC remains high.

1.4.2 Power Dissipation

Every electronic circuit requires a certain amount of electric power for its operation. When the power is supplied by an external source, some of it is dissipated in electronic circuits. It is wastage of power across the circuit components and devices. Requirement of power is less, if the dissipation of power is less. Hence power dissipation should be as minimum as possible. Power dissipation of an IC is expressed in terms of milli Watt (mW).

1.4.3 Figure of Merit

The power dissipation of logic families should be minimum to reduce power requirements. But it is important to note that in logic families, if the power dissipation is reduced, the speed of operation gets reduced. Hence the *figure of merit* is a parameter considered for comparison instead of using the speed of operation and

power dissipation. Figure of merit is a product of propagation delay and power dissipation. It is measured in terms of Pico-Joules (ns × mW = pJ).

1.4.4 Current and Voltage Parameters

Current and voltage parameters define the minimum and maximum limit of current and voltage for input and output of a logic family.

V_{IH} *(High level input voltage)* It is the minimum input voltage corresponding to logic 1 state.

V_{IL} *(Low level input voltage)* It is the maximum input voltage corresponding to logic 0 state.

V_{OH} *(High level output voltage)* It is the minimum output voltage corresponding to logic 1 state.

V_{OL} *(Low level output voltage)* It is the maximum output voltage corresponding to logic 0 state.

I_{IH} *(High level input current)* It is the minimum input current corresponding to logic 1 state.

I_{IL} *(Low level input current)* It is the maximum input current corresponding to logic 0 state.

I_{OH} *(High level output current)* It is the minimum output current corresponding to logic 1 state. This current is also referred to as the *source current.*

I_{OL} *(Low level output current)* It is the maximum output current corresponding to logic 0 state. It is also referred to as the *sink current*.

1.4.5 Fan-Out

Fan-out is the capability of a logic gate to drive the maximum number of similar gates. High fan-out is advantageous, because it reduces the need of additional gates to drive more gates. Consider Fig.1.4.

In Fig. 1.4, the driver gate drives all the *N* gates (*N* is fan-out). If more than *N* gates are connected to a load of the driver gate, then the current supply by the driver gate is less than the current required to drive the gates, or the current sink by the driver gate is more than the rating of the driver gate which may damage the gate.

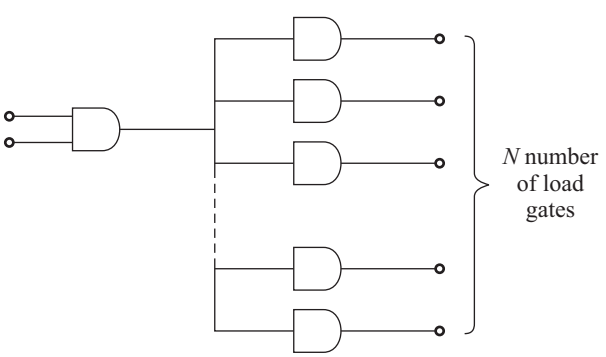


Fig. 1.4 AND gate driving *N* gates

The fan-out of a logic family can be calculated as

$$\text{Fan-out} = \text{minimum of} \left\{ \frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}} \right\} \tag{1.7}$$

1.4.6 Fan-In

Fan-in is the number of inputs to a gate. For a two-inputs gate, fan-in is two; and for a four-inputs gate, fan-in is four.

1.4.7 Noise Immunity

Unwanted signals are known as *noise*. The stray electric and magnetic fields may induce some noise at an input of digital circuit. Because of noise, the input voltage may drop below V_{IH} or may be raise above V_{IL}, which results in undesired operations. The circuit should have the ability to tolerate the noise signal. The noise immunity of digital circuit is defined as the ability of a digital circuit to tolerate the noise signal. A quantitative measure of noise immunity is known as *noise margin*. Logic 1 state noise margin and Logic 0 state noise margin can be calculated as:

$$\text{Logic 1 state noise margin } \Delta 1 = V_{OH} - V_{IH} \tag{1.8}$$

$$\text{Logic 0 state noise margin } \Delta 0 = V_{IL} - V_{OL} \tag{1.9}$$

It is important that for logic families, $V_{OH} > V_{IH}$ and $V_{IL} > V_{OL}$ as shown in Fig. 1.5.

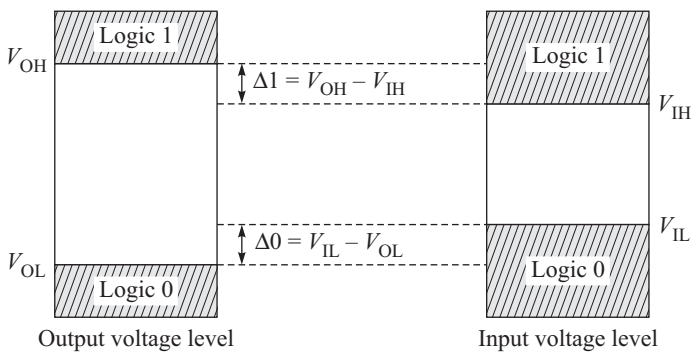


Fig. 1.5 Input and output voltage levels

Let us see how the noise leads to an undesired output. Take the example of a TTL AND gate. A detailed study of TTL AND gate is covered in Section 1.9. The TTL gate has $V_{OH} = 2.4$ V, $V_{OL} = 0.4$ V, $V_{IH} = 2$ V, and $V_{IL} = 0.8$ V. The noise introduced in the signal (V_{noise}) is shown in Fig. 1.6.

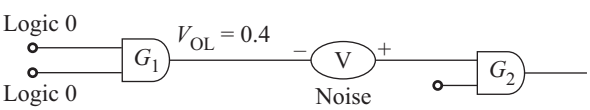


Fig. 1.6 Noise

Let the inputs of gate$_1$ be such that the output of gate$_1$ is in logic 0 state ($V_{OL} = 0.4$ V). This output is given as an input to gate$_2$. Because of the noise present, the actual input given to gate$_2$ is:

$$V_{i2} = V_{OL} + V_{noise} \tag{1.10}$$

$$V_{i2} = 0.4 + V_{noise}$$

$$V_{noise} = V_{i2} - 0.4$$

The maximum low level input of the gate is 0.8 V. When the noise introduced in the signal is greater than (0.8 – 0.4) = 0.4 V, then the input to gate$_2$ will be greater than 0.8 V, which transits to an invalid input level and the output will be unpredictable.

Similarly for high state output of gate$_1$

$$V_{i2} = 2.4 - V_{noise}$$

$$V_{noise} = 2.4 - V_{i2}$$

The minimum high level input of the gate is 2 V. When the noise signal is greater than (2.4 – 2.0) = 0.4 V, the input of gate$_2$ will be less than 2 V, which transits to an invalid input state and the output will be unpredictable.

1.4.8 Power Supply Requirements

Every electronic circuit requires supply voltage to operate. The required supply voltage and power by the IC should be as less as possible.

1.4.9 Operating Temperature

On the basis of operating temperature range, the application of the ICs will be decided. The operating temperature is the range of temperature in which an IC functions properly. It is in order of –55°C to +125°C. The accepted temperature range of an IC is 0 to +70°C for commercial and industrial applications. Selection of a particular logic family for a particular application depends on these parameters. Let us learn each of these logic families.

1.5 RESISTOR-TRANSISTOR LOGIC (RTL)

RTL consists of resistors and transistors. In RTL, transistors operate in cut-off region or saturation region as per the input voltage applied. Figure 1.7 shows the circuit of a two-inputs resistor-transistor logic NOR gate. Here *A* and *B* are the inputs of the gate and *Y* is the output.

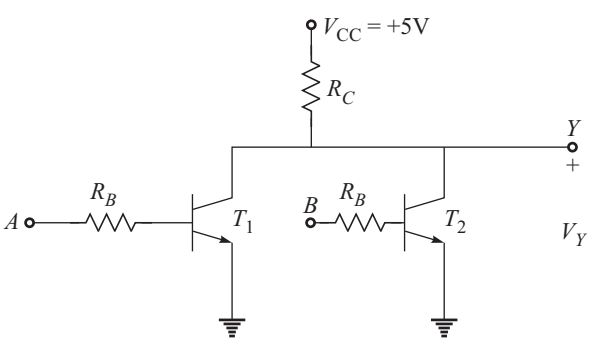


Fig. 1.7 Resistor-transistor logic NOR gate

Operation

- When the transistor operates in saturation region, maximum current flows through resistor R_C. The output voltage $V_Y = V_{CEsat}$ ($V_{CEsat} = 0.2$ V for silicon and 0.1 V for germanium); it is logic 0 level voltage. When the transistor operates in cut-off, no current flows through resistor R_C and the output voltage $V_Y = V_{CC} = +5$ V; it is logic 1 level voltage.
- When both the inputs are in logic 0, transistors T_1 and T_2 operate in cut-off, and the output is $+V_{CC}$, i.e. +5 V (logic 1).
- When any one of the inputs is at logic 1 level, the corresponding transistor operates in saturation, and the output is $V_Y = 0.2$ V (logic 0).
- When both the inputs are at logic 1 level, both the transistors operate in saturation and the output is $V_Y = 0.2$ V (logic 0). The operation of circuit is summarized in Table 1.1(a).

Table 1.1(a) Operation of RTL NOR gate (Fig. 1.7)

V_A	V_B	*Transistor* T_1	*Transistor* T_2	V_Y
Logic 0	Logic 0	Cut-off	Cut-off	Logic 1
Logic 0	Logic 1	Cut-off	Saturation	Logic 0
Logic 1	Logic 0	Saturation	Cut-off	Logic 0
Logic 1	Logic 1	Saturation	Saturation	Logic 0

In terms of 0 and 1, the above table can be written as in Table 1.1(b).

Table 1.1(b) Operation of RTL NOR gate (Fig. 1.7)

V_A	V_B	V_Y
0	0	1
0	1	0
1	0	0
1	1	0

The circuit shown in Fig.1.7 acts as a two-inputs NOR gate and Table 1.1(b) is the truth table of NOR gate.

The RTL suffers from a few drawbacks as listed below:

1. Low noise margin (Typically 0.1 V)
2. Fan-out is poor (Typically 5)
3. Propagation delay is high and the speed of operation is low (Typically 12 ns)
4. High power dissipation (Typically 12 mW)

1.6 DIRECT COUPLED TRANSISTOR LOGIC (DCTL)

In direct coupled transistor logic, the input signal is directly given to the base of the transistor. DCTL is simple than RTL. In DCTL, the transistor operates in saturation or cut-off region. Figure 1.8 shows the circuit of a two-inputs DCTL NOR gate.

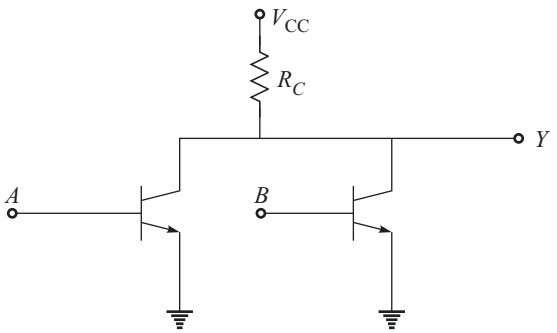


Fig. 1.8 Two-inputs DCTL NOR gate

Operation

The operation of DCTL is same as the operation of RTL. When both the inputs are in logic 0, transistors operate in cut-off, and the output is logic 1. When any one of the inputs or both the inputs are in logic 1, the corresponding transistor or transistors operate in saturation and the output is logic 0.

Although DCTL is simpler than RTL, it is not popular because of the *current hogging problem*. Let us see what the current hogging problem is.

Current hogging problem

Figure 1.9 shows a DCTL gate driving a three-inputs NOR gate.

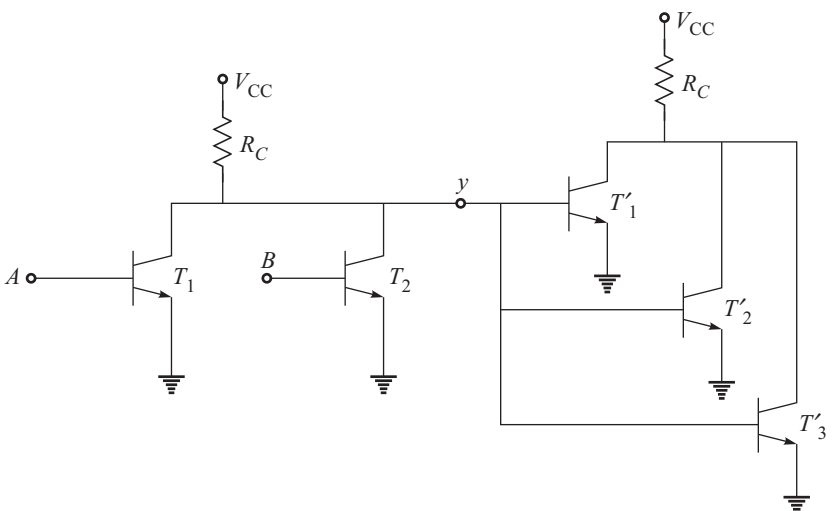


Fig. 1.9 DCTL gate driving the three-inputs NOR gate

Initially the input of transistor T_1 is logic 0, and the input of transistor T_2 is logic 1, T_1 operates in cut-off and T_2 operates in saturation, the output of driving gate is in logic 0 ($V_{CEsat} = 0.2$ V) which drives all the transistors in cut-off. When the input of T_2 changes from logic 1 to logic 0, T_2 operates in cut-off. The output of the driving gate starts to change from 0.2 V to V_{CC}.

Due to manufacturing tolerance, the base to emitter voltage of transistors T_1', T_2' and T_3' are different. Assume V_{BEsat} of transistors T_1', T_2' and T_3' are 0.8 V, 0.79 V and 0.78 V, respectively. When the voltage at the output of driving gate reaches 0.78 V, T_3' goes in saturation and will not allow other transistors to enter in saturation. The whole current flows through the base of T_3' and the transistor may damage. Once T_3' damages, T_2' goes in saturation and will not allow other transistors to enter in saturation. The whole current flows through the base of T_2' and it may damage. Similarly, all the transistors of the driven circuit are damaged. It is known as the *current hogging problem*.

1.7 DIODE-TRANSISTOR LOGIC (DTL)

The circuit of a DTL consists of diodes and transistors. Figure 1.10 shows the circuit of a two-inputs diode-transistor logic NAND gate.

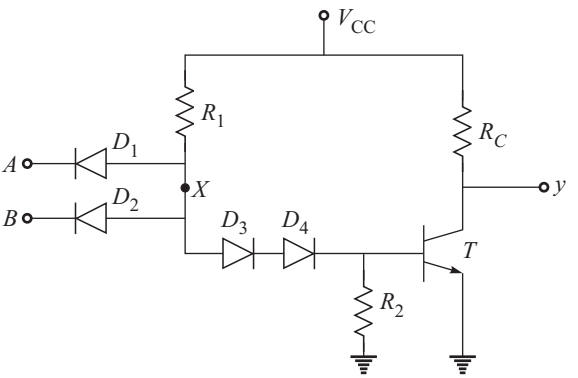


Fig. 1.10 Two-inputs DTL NAND gate

Operation

- When the transistor operates in saturation, the output voltage $V_{(0)} = V_{CEsat} = 0.2$ V; and when it operates in cut-off, the output voltage $V_{(1)} = V_{CC} = +5$ V.
- When both the inputs are in logic 0, $V_{(0)} = V_{CEsat} = 0.2$ V, the input diodes are forward biased, voltage at point x is $V_x = V_{(0)} + V_D = 0.2 + 0.7 = 0.9$ V which is not sufficient to drive the transistor in saturation, because the voltage desired at point x to drive the transistor in saturation should be $V_{BEsat} + V_{D4} + V_{D3} = 0.8 + 0.7 + 0.9 = 2.2$ V. The transistor operates in cut-off and the output voltage is in logic 1 state.
- When any one of the inputs is in logic 1, the corresponding diode is forward biased. Voltage at point x is $V_x = 0.2$ V + 0.7 V = 0.9 V; the transistor operates in cut-off and the output voltage is in logic 1 state.
- When all the inputs are in logic 1 state, the diodes D_1 and D_2 are reverse biased. The resistances R_1 and R_2 are selected such that the transistor operates in saturation and the output voltage is in logic 0 state.

The operation of the circuit is summarized in Table 1.2(a).

Table 1.2(a) Operation of DTL NAND gate (Fig. 1.10)

Inputs		*Diodes*		*Transistor*	*output*
A	***B***	D_1	D_2	***T***	***Y***
Logic 0	Logic 0	Forward biased	Forward biased	Cut-off	Logic 1
Logic 0	Logic 1	Forward biased	Reverse biased	Cut-off	Logic 1
Logic 1	Logic 0	Reverse biased	Forward biased	Cut-off	Logic 1
Logic 1	Logic 1	Reverse biased	Reverse biased	Saturation	Logic 0

In terms of 0 and 1, Table 1.2(a) can be written as in Table 1.2(b).

Table 1.2(b) Operation of DTL NAND gate (Fig. 1.10)

A	***B***	***Y***
0	0	1
0	1	1
1	0	1
1	1	0

The circuit shown in Fig. 1.10 acts as a two-input NAND gate and Table1.2(b) shows the truth table of NAND gate.

Following are the advantages and disadvantages of DTL over RTL.

Advantages

1. Fan-out is high.
2. Power dissipation is 8–12 mW.
3. Noise immunity is good.

Disadvantages

1. More elements are required.
2. Propagation delay is more (typically 30 ns) and hence the speed of operation is less.

1.8 MODIFIED DIODE-TRANSISTOR LOGIC

More fan-out gates are preferred for most of the applications. Fan-out of the gate is a function of source current. The fan-out of a logic gate is increased by increasing the current supply of the gate (source current). When the base current of a transistor is increased, then the source current in the diode-transistor logic increases and this in turn increases the fan-out. Replacement of the diode D_3 in Fig. 1.10 by the transistor T_1 increases the base current of the transistor and the circuit is referred as a modified diode-transistor logic. The modified diode-transistor logic has more fan-out as compared to DTL. The circuit diagram of a modified diode-transistor logic is shown in Fig. 1.11.

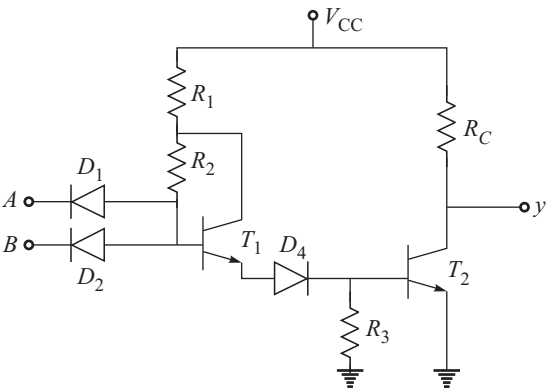


Fig. 1.11 Modified diode-transistor logic

1.9 TRANSISTOR-TRANSISTOR LOGIC (TTL)

Transistor-transistor logic is one of the popular saturated logic families. Transistor is the basic element of this logic family, which operates either in cut-off or saturation region. The first version of TTL is known as the standard TTL.

Standard TTLs are available in various forms:

1. TTL with passive pull-up
2. TTL with totem-pole output
3. TTL with open collector output
4. Tristate TTL

1.9.1 TTL with Passive Pull-Up

Figure 1.12 shows a two-input TTL NAND gate with passive pull-up. Transistor T_1 has two emitter terminals. These terminals act as the inputs of the gate, that is, input *A* and input *B*. The input voltages are logic 0 or logic 1, where logic 0 corresponds to 0.2 V and logic 1 corresponds to +5 V.

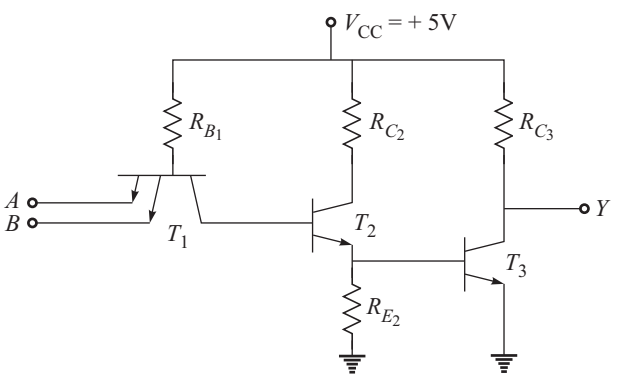


Fig. 1.12 Two-input TTL NAND gate with passive pull-up

Operation

- When both the inputs (A and B) are in logic 0, $V_{(0)} = V_{CEsat} = 0.2$ V, the emitter junctions of transistor T_1 are forward biased and the voltage at the base of transistor T_1 is $V_{B1} = V_{(0)} + V_{BE} = 0.2 + 0.7 = 0.9$ V. The minimum voltage required at the base of T_1, so that T_2 and T_3 start to conduct, is $V_{BEcut\ (in)} + V_{BEcut\ (in)} + 0.7 = 0.5 + 0.5 + 0.7 = 1.7$ V. The required voltage is greater than the voltage available at the base of T_1 and hence T_2 and T_3 are in cut-off and the output voltage is equal to the supply voltage V_{CC} (logic 1 level), output is in logic 1 state.
- When any one of the inputs is at logic 0 level, the corresponding emitter junction of T_1 is forward biased and the voltage at the base of T_1 is $V_{B1} = V_{(0)} + V_{BE} = 0.2 + 0.7 = 0.9$ V. The minimum voltage required at the base of T_1, so that T_2 and T_3 start to conduct, is $V_{BEcut\ (in)} + V_{BEcut\ (in)} + 0.7 = 0.5 + 0.5 + 0.7 = 1.7$ V. The required voltage is greater than the voltage available at the base of T_1 and hence T_2 and T_3 are in cut-off and the output voltage is equal to the supply voltage V_{CC}, output is in logic 1 state.
- When all the inputs are in logic 1 state, the emitter junctions of T_1 are reverse biased and the current supply by the source is sufficient to operate T_2 and T_3 in saturation and the output is in logic 0 state.

The operation of the circuit is summarized in Table 1.3(a).

Table 1.3(a) Operation of TTL NAND gate (Fig. 1.12)

Inputs		*Transistor T_1*		*Transistors T_2 and T_3*	*Output*
A	*B*	*Emitter junction A*	*Emitter junction B*		
Logic 0	Logic 0	Forward biased	Forward biased	Cut-off	Logic 1
Logic 0	Logic 1	Forward biased	Reverse biased	Cut-off	Logic 1
Logic 1	Logic 0	Reverse biased	Forward biased	Cut-off	Logic 1
Logic 1	Logic 1	Reverse biased	Reverse biased	Saturation	Logic 0

In terms of 0 and 1, Table 1.3(a) can be written as follows:

Table 1.3(b) Operation of TTL NAND gate (Fig. 1.12)

V_A	V_B	V_Y
0	0	1
0	1	1
1	0	1
1	1	0

The circuit shown in Fig. 1.12 acts as a two-input NAND gate and its truth table is given in Table 1.3(b).

Passive pull-up

When both inputs are high, T_3 operates in saturation region, $V_0 = V_{CEsat}$ and the capacitor of loaded gate is charged up to V_{CEsat}. When one or more than one inputs change to logic 0, the corresponding emitter junction or junctions of T_1 are forward biased and T_3 goes into cut-off. The capacitor of the loaded gate starts charging towards V_{CC} through the resistor R_{C3} as shown in Fig. 1.13.

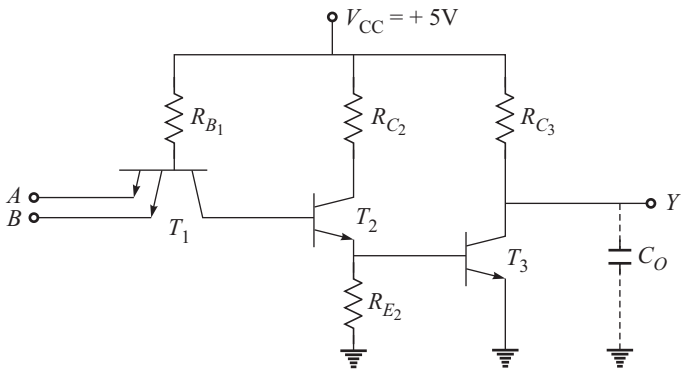


Fig. 1.13 TTL with passive pull-up

The capacitor of the loaded gate is pulled towards V_{CC} through the passive component R_{C_3} and hence the circuit is known as TTL with passive pull-up.

In TTL with passive pull-up, the time constant is $R_{C_3} \times C_O$. The speed of the circuit can be improved by decreasing R_{C_3}, which decreases the time constant. By decreasing the value of R_{C_3}, the power dissipation will go up due to the increased collector current of transistor T_3. This problem of TTL with passive pull-up is overcome in TTL with active pull-up.

1.9.2 TTL with Totem-Pole Output

Figure 1.14 shows the circuit of a two-input TTL NAND gate with totem-pole output. It is possible in TTL to improve the speed of operation by reducing the time constant without increasing power dissipation with the help of active pull-up. TTL with active pull-up is known as TTL with totem-pole output.

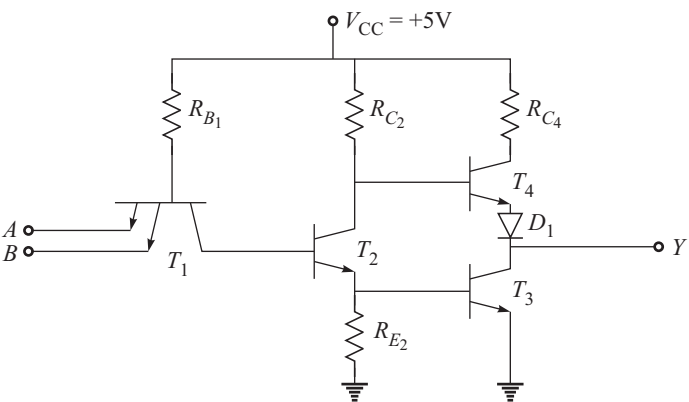


Fig. 1.14 Two-input TTL NAND gate with totem-pole output

Operation

- When both the inputs are in logic 0, $V_{(0)} = V_{CEsat} = 0.2\,V$, emitter junctions of T_1 are forward biased and the voltage at the base of T_1 is $V_{B1} = V_{(0)} + V_{BE} = 0.2 + 0.7 = 0.9\,V$. The minimum voltage required at the base of T_1, so that

T_2 and T_3 start to conduct, is $V_{BEcut\ (in)} + V_{BEcut\ (in)} + 0.7 = 0.5 + 0.5 + 0.7 = 1.7$ V. The required voltage is greater than the voltage available at the base of T_1 and hence T_2 and T_3 are in cut-off and the output voltage is equal to the supply voltage V_{CC} (logic 1 level), output is in logic 1 state. Since T_2 is in cut-off region, the current supply by the source V_{CC} through R_{C_2} is sufficient to operate T_4 in saturation.

- When any one of the inputs is at logic 0 level, the corresponding emitter junction of T_1 is forward biased and the voltage at the base of T_1 is $V_{B1} = V_{(0)} + V_{BE} = 0.2 + 0.7 = 0.9$ V. The minimum voltage required at the base of T_1, so that T_2 and T_3 start to conduct, is $V_{BEcut\ (in)} + V_{BEcut\ (in)} + 0.7 = 0.5 + 0.5 + 0.7 = 1.7$ V. The required voltage is greater than the voltage available at the base of T_1 and hence T_2 and T_3 are in cut-off and the output voltage is equal to the supply voltage V_{CC} (logic 1 level), output is in logic 1 state. Since T_2 is in cut-off region, the current supply by the source V_{CC} through R_{C_2} is sufficient to operate T_4 in saturation.
- When all the inputs are in logic 1 state, the emitter junctions of T_1 are reverse biased and the current supply by the source is sufficient to operate T_2 and T_3 in saturation and the output is logic 0 state. Since T_2 is in saturation region, the voltage at the collector of T_2 is low and T_4 operates in cut-off.

The operation of the circuit is summarized in Table 1.4(a).

Table 1.4(a) Operation of TTL NAND gate (Fig. 1.14)

Inputs		*Transistor T_1*		*Transistors*	*Transistor*	*Output*
A	*B*	*Emitter junction A*	*Emitter junction B*	*T_2 and T_3*	*T_4*	*Y*
Logic 0	Logic 0	Forward biased	Forward biased	Cut-off	Saturation	Logic 1
Logic 0	Logic 1	Forward biased	Reverse biased	Cut-off	Saturation	Logic 1
Logic 1	Logic 0	Reverse biased	Forward biased	Cut-off	Saturation	Logic 1
Logic 1	Logic 1	Reverse biased	Reverse biased	Saturation	Cut-off	Logic 0

In terms of 0 and 1, Table 1.4(a) can be written as in Table 1.4(b).

Table 1.4(b) Operation of TTL NAND gate (Fig. 1.14)

A	*B*	*Y*
0	0	1
0	1	1
1	0	1
1	1	0

The circuit shown in Fig. 1.14 acts as a two-input NAND gate and its truth table is given in Table 1.4(b).

Active pull-up

When both the inputs are high, T_3 operates in saturation region, $V_0 = V_{CEsat}$, and T_4 operates in cut-off. The current provided by the load is sinked by T_3 and the capacitor of the loaded gate is charged up to V_{CEsat}.

When one or more than one input changes to logic 0, the corresponding emitter junction or junctions of T_1 are forward biased. T_3 goes into cut-off and T_4 is in saturation and the diode D_1 is forward biased. The capacitor of the loaded gate starts to charge towards V_{CC} through T_4 and D_1 as shown in Fig. 1.15.

The capacitor of the loaded gate is pulled towards V_{CC} through the active components T_4 and D_1. Hence the circuit is known as TTL with active pull-up.

In totem-pole output, T_4 acts as an emitter follower. The output impedance of emitter follower is low. This means that the output voltage can change quickly from low state to high state.

When the output changes from high to low, T_3 operates in saturation and the capacitor of the loaded gate discharges quickly through T_3.

Due to the current spike problem, wired-AND connection must not be used for totem-pole output circuits, as discussed in the next section.

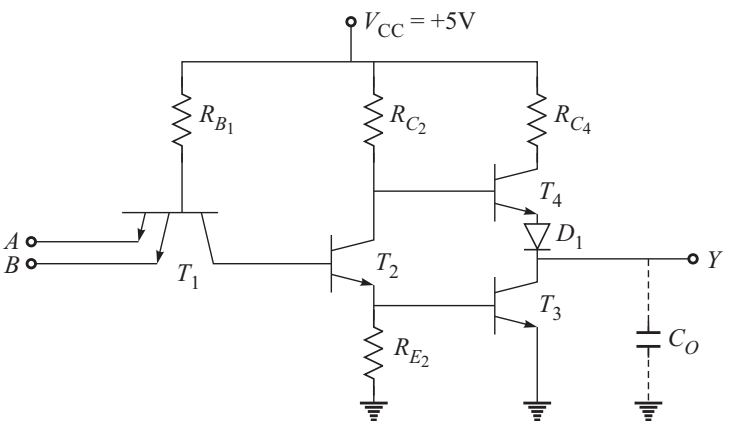


Fig. 1.15 Two-input TTL NAND gate totem-pole output with capacitive load

Function of diode in totem-pole output

In totem-pole output TTL, when T_3 operates in saturation, T_4 must operate in cut-off or vice versa. The diode D_1 is used in the circuit to keep T_4 in cut-off when the output is low. When T_2 and T_3 are in saturation, the voltage available at the base of T_4 is

$$V_{B_4} = V_{BE3sat} + V_{CE2sat} \quad (1.11)$$
$$= 0.8 + 0.2 = 1 \text{ V}$$

In the absence of a diode, the voltage required at the base of T_4 so that it starts to conduct is

$$V_{B_4} = V_0 + V_{\text{BEcut (in)}} \qquad (1.12)$$
$$= 0.2 + 0.5 = 0.7 \text{ V}$$

The voltage available at the base of T_4 is greater than the voltage required and hence both T_3 and T_4 are in saturation. To avoid this situation, D_1 is used in the circuit.

In the presence of a diode, the voltage required at the base of T_4, for the transistor to conduct, is

$$V_{B_4} = V_{(O)} + V_D + V_{\text{BEcut (in)}} \qquad (1.13)$$
$$= 0.2 + 0.7 + 0.5 = 1.4 \text{ V}$$

The voltage available at the base of T_4 is less than the voltage required and hence T_4 is operating in cut-off.

Sink current

It is the current supplied by the load. Figure 1.16 shows a two-input modified TTL NAND gate driving a similar gate.

When both the inputs are in logic 1 state, T_3 operates in saturation and T_4 is in cut-off. The output of the driver gate is logic 0 ($V_O = 0.2$ V), the emitter junction of transistor $T'_1$of the loaded gate becomes forward biased and the current supply by V_{CC} of the loaded gate passes through T_3 of the driver gate. This current is known as the *sink current*.

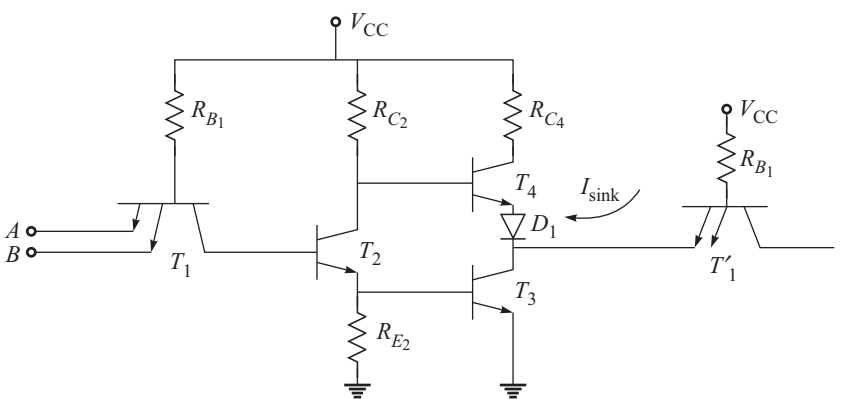


Fig. 1.16 Two-input modified TTL NAND gate driving same gate

Source current

It is the current supplied by the driver gate to the loading gate(s). Figure 1.17 shows a two-input modified TTL NAND gate driving a similar gate.

When both or any one of the inputs is in logic 0 state, T_3 operates in cut-off, and T_4 is in saturation. The source V_{CC} supplies the current to the loading gate through R_{C_4}, T_4 and D_1 as shown in Fig. 1.17. This current is known as the *source current*.

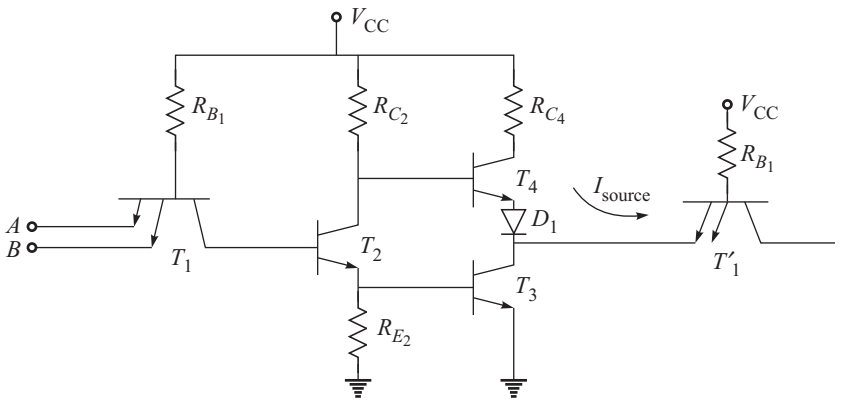


Fig. 1.17 Two-input modified TTL NAND

Clamped Diode

The circuit of a modified TTL with a clamping diode at input is shown in Fig. 1.18.

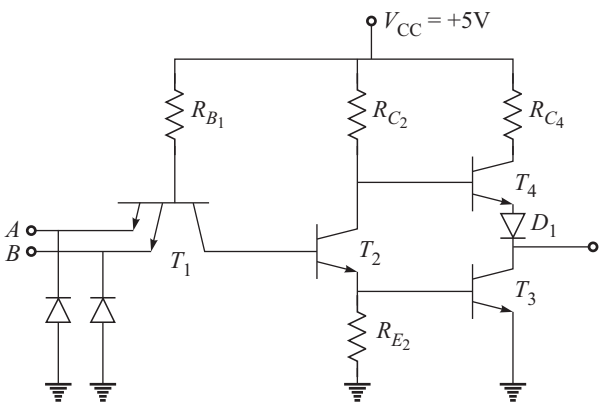


Fig. 1.18 Modified TTL with clamping diode at input

Clamping diodes are commonly used in TTL to suppress the *ringing* caused because of the fast transition found in TTL. At normal input signal, the diodes are reverse biased for high as well as low voltages. When transition occurs, the reactive component associated with the load causes ringing as shown in Fig. 1.19.

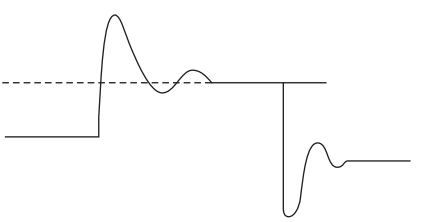


Fig. 1.19 Ringing effect

The rising on the positive side do not create any problem, but it makes the emitter junction reverse biased. Due to rising on the negative side, the emitter junction is more forward biased, the current flow through the emitter is very high, and the

transistor may be damaged. The diode(s) connected at the input is forward biased for negative spike and limits the voltage up to –0.7 V and protects the transistor.

1.9.3 Wired-AND Connection

A wired-AND connection has two or more than two gates connected together. Using a wired-AND connection, the fan-in of the circuit is increased.

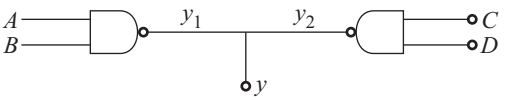


Fig. 1.20 Wired-AND connection

Here the outputs of two NAND gates are connected together.

$$Y = Y_1 \cdot Y_2$$

$$Y_1 = \overline{AB} \text{ and } Y_2 = \overline{CD}$$

Hence $$Y = \overline{AB} \cdot \overline{CD}$$

Using De-Morgan's theorem,

$$Y = \overline{AB + CD} \tag{1.14}$$

Wired-AND connection is not possible in TTL with totem-pole output. The circuit diagram of a wired-AND connection for TTL with totem-pole output is shown in Fig. 1.21.

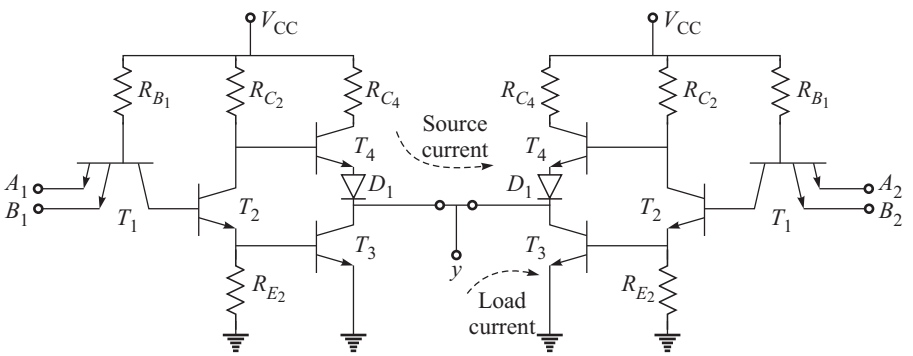


Fig. 1.21 Wired-AND connection for TTL with totem-pole output

When the output of gate$_1$ is high and gate$_2$ is low, then T_3 of gate$_1$ operates in cut-off, T_4 of gate$_1$ operates in saturation, T_3 of gate$_2$ operates in saturation and T_4 of gate$_2$ operates in cut-off. The load current and the current supplied by V_{CC} of gate$_1$ flow through T_3 of gate$_2$ and T_3 can be burnt out. Hence, wired-AND connection must not be used for totem-pole output TTL.

1.9.4 TTL with Open Collector Output

TTL with totem-pole output has a major problem that the two outputs of the two gates cannot be connected together. This problem of TTL with totem-pole output

is overcome in TTL with open collector output. Figure 1.22 shows the circuit of a TTL NAND gate with open collector output.

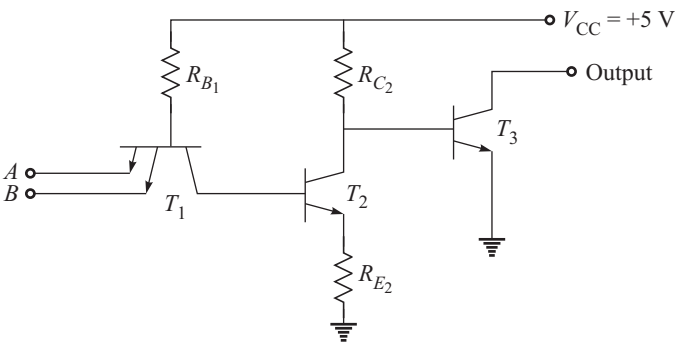


Fig. 1.22 TTL NAND gate with open collector output

The collector terminal of T_3 is available outside the IC where the external resistor is to be connected. The circuit acts as a TTL with passive pull-up and hence the advantages of active pull-up cannot be achieved in the circuit but wired-AND connection is possible.

1.9.5 Unconnected Inputs of TTL

The input circuit of a TTL is shown in Fig. 1.23.

When the input is in logic 0 state, the emitter junction is forward biased and the current flows through the junction. When the input is in logic 1 state, the emitter junction is reversed biased and the current cannot flow through the junction. If any one of the inputs of the TTL gate is open, then the corresponding junction cannot be forward biased, and the current cannot flow. The input acts exactly in the same way, as in case when logic 1 is applied to that input. Therefore in TTL ICs, all unconnected inputs are treated as logical 1s.

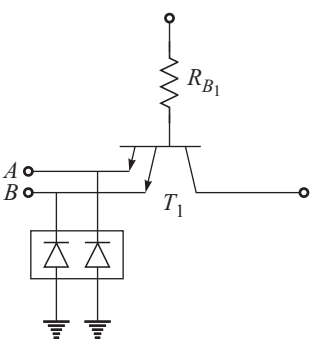


Fig. 1.23 Input circuit of TTL

1.9.6 Tri-state TTL

A normal digital circuit has two output states: Low and High. The output is either in high state or low state. If the output is not in the low state, it is definitely in the high state. The tri-state TTL has three output states: High, Low, and High-impedance.

In TTL with totem-pole output, T_3 is ON when the output is low and T_4 is ON when the output is high. In high-impedance state, both T_3 and T_4 in totem-pole arrangement are turned OFF and as a result, the output is open or floating.

When the output is low, the driver gate sinks the load current as shown in Fig. 1.24(a). When the output is high, the driver gate supplies the current to the

load as shown in Fig. 1.24(b). When the output is in high-impedance state, it acts as open or floating and there is no sink and source current as shown in Fig. 1.24(c).

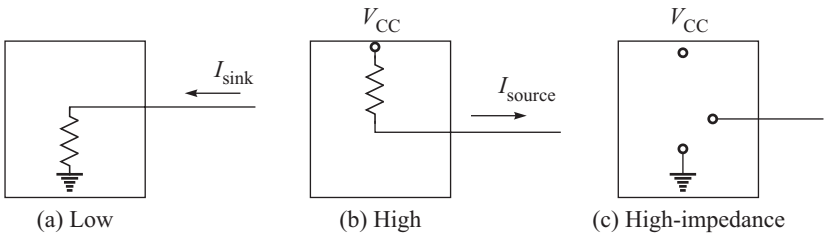


Fig. 1.24 Tri-state logic

Tri-state inverter

The circuit of a tri-state TTL inverter is shown in Fig. 1.25.

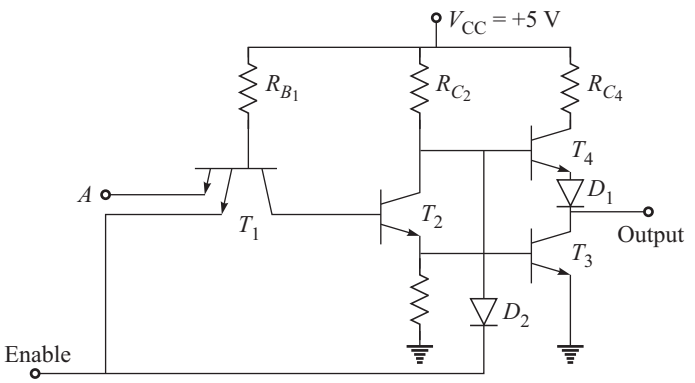
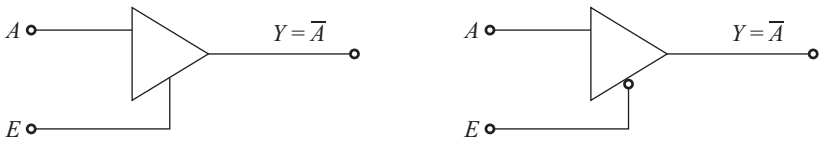


Fig. 1.25 Tri-state TTL inverter

The tri-state TTL inverter has two inputs—normal input A and enable input E.

- When the enable input E is High, the corresponding emitter junction of T_1 is reverse biased and the circuit operates as a normal inverter as explained below.
  - When A is high, the second emitter junction of T_1 is reverse biased. Current supplied by the source flows through the collector terminal of T_1, which forces T_2 and T_3 to be in saturation and the output is low. T_4 operates in cut-off.
  - When A is low, the corresponding emitter junction of T_1 is forward biased, current supplied by the source flows through the emitter terminal of T_1, transistors T_2 and T_3 operate in cut-off and the output is high. T_4 operates in ON state.
- When the enable input E is low, the corresponding emitter junction of T_1 is forward biased. Current supplied by the source flows through the emitter terminal of T_1, transistors T_2 and T_3 operate in cut-off. Because of low enable input, the diode D_2 is forward biased and the current supplied by the source flows through the diode D_2, transistor T_4 is operated in cut-off and thus the output is in high-impedance state.

The logic symbols for the active high and active low enable input inverters are shown in Figs 1.26(a) and (b), respectively.



(a) Active high enable input (b) Active low enable input

Fig. 1.26 Enable input inverter

Application of tri-state logic

Tri-state buffers play an important role in computer systems. In case of 8085 microprocessor, all the buses are in tri-state whenever the 8085 is in reset mode.

Figure 1.27 shows the common bus connected to four output devices, where *A*, *B*, *C* and *D* are the enabled inputs of tri-state buffer. Data present over the bus is given to the device as per the enabled input signal of the tri-state buffer. The enabled signal of the input device is active low.

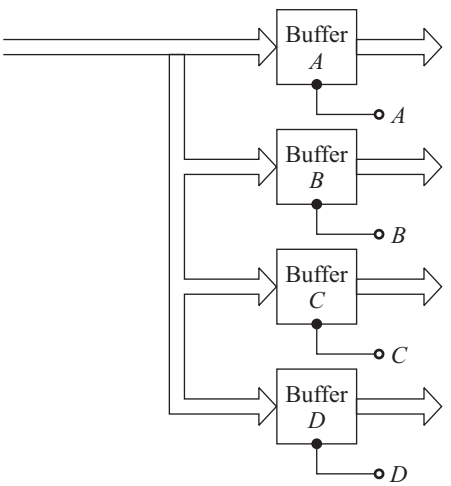


Fig. 1.27 Application of tri-state logic for data bus

When $A = 0, B = 1, C = 1, D = 1$, buffer *A* is enabled and others are disabled, and the data present over the line is given to device 1. When $A = 1, B = 0, C = 1, D = 1$, buffer *B* is enabled and others are disabled, and the data present over the line is given to device 2. When $A = 1, B = 1, C = 0, D = 1$, buffer *C* is enabled and others are disabled, and the data present over the line is given to device 3. When $A = 1, B = 1, C = 1, D = 0$, buffer *D* is enabled and others are disabled, and the data present over the line is given to device 4.

1.10 TTL PARAMETERS

Now let us study the typical values of TTL family parameters.

Speed of operation

The speed of operation of a TTL is specified in terms of propagation delay time. For a standard TTL, the propagation delay time is 18.5 ns.

If $t_{PHL} = 15$ ns and $t_{PLH} = 22$ ns, then $t_p = \dfrac{15 + 22}{2} = 18.5$ ns

Power dissipation

It signifies the wastage of power in a digital circuit. It should be as minimum as possible. For a standard TTL, power dissipation is 19 mW.

Current and voltage parameters

V_{IH} : It is the minimum input voltage to be recognized as logic 1 state.
V_{IL} : It is the maximum input voltage to be recognized as logic 0 state.
V_{OH} : It is the minimum output voltage corresponding to logic 1 state
V_{OL} : It is the maximum output voltage corresponding to logic 0 state.

For a standard TTL family:

$V_{IH} = 2$ V, $V_{OH} = 2.4$ V, $V_{IL} = 0.8$ V, and $V_{OL} = 0.4$ V

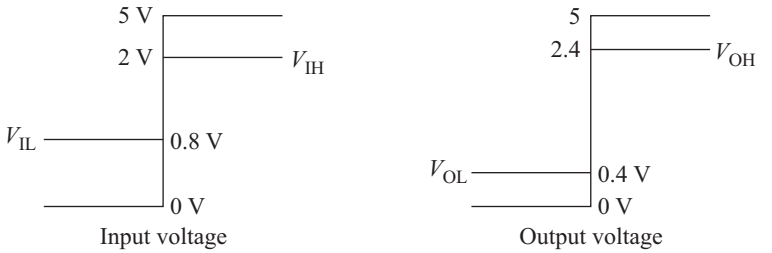


Fig. 1.28 Voltage range for TTL

I_{IH} : It is the minimum input current corresponding to logic 1 state.
I_{IL} : It is the maximum input current corresponding to logic 0 state
I_{OH} : It is the minimum output current corresponding to logic 1 state. It is called the *source current*.
I_{OL} : It is the maximum output current corresponding to logic 0 state. It is called the *sink current*.

For a standard TTL family:

$I_{IH} = 40$ μA, $I_{OH} = -400$ μA, $I_{IL} = 1.6$ mA, and $I_{OL} = 16$ mA

Fan-out

In digital applications, the output of a logic gate is given to one or more than one inputs of other logic gates. Fan-out is nothing but the capacity of the driver gate to drive a number of similar gates.

When the output of the driver gate is low, T_3 sinks current from the forward biased emitter junction of transistor of the load as shown in Fig. 1.29(a). If n similar gates are connected at the output, then the total sink current I_{OL} is n times the input current I_{IL}, where n is the fan-out of TTL.

$$I_{OL} = nI_{IL}$$

$$n = \frac{I_{OL}}{I_{IL}} = \frac{16\text{ mA}}{1.6\text{ mA}} = 10$$

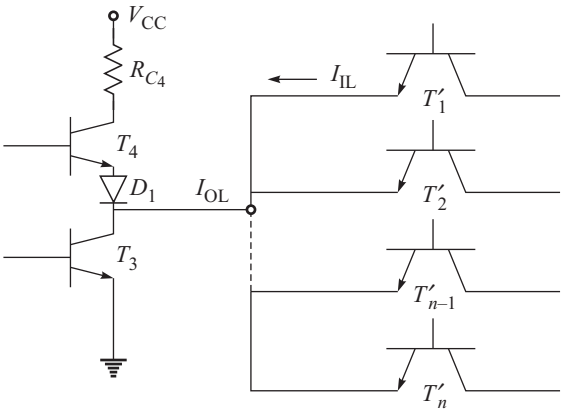


Fig. 1.29(a) TTL sinking the current from *n* gates

When the output of the driver gate is high, T_4 acts as a current source to the load as shown in Fig. 1.29(b). If *n* similar gates are connected at the output, then the total source current must be equal to *n* times the input current I_{IH}, where *n* is the fan-out of TTL.

$$I_{OH} = n\, I_{IH}$$

$$n = \frac{I_{OH}}{I_{IH}} = \frac{400\,\mu\text{A}}{40\,\mu\text{A}} = 10$$

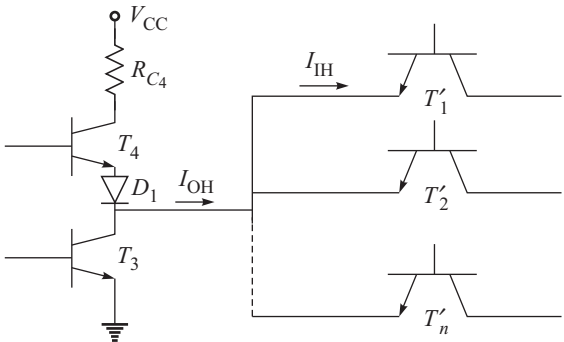


Fig. 1.29(b) TTL supplying the current to *n* gates

$$\text{Fan-out} = \text{minimum of } \left\{\frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}}\right\}$$

Fan-out for a standard TTL = minimum of {10, 10} = 10

Noise Margin

The noise immunity of a digital circuit is its ability to tolerate a noise signal. A quantitative measure of noise immunity is known as the *noise margin*.

Logic 1 level noise margin ($\Delta 1$) = $V_{OH} - V_{IH}$

Logic 0 level noise margin ($\Delta 0$) = $V_{IL} - V_{OL}$

For a standard family,

$V_{IH} = 2\text{ V}$, $V_{OH} = 2.4\text{ V}$, $V_{IL} = 0.8\text{ V}$, $V_{OL} = 0.4\text{ V}$

$(\Delta 1) = 2.4\text{ V} - 2\text{ V} = 0.4\text{ V}$ $(\Delta 0) = 0.8\text{ V} - 0.4\text{ V} = 0.4\text{ V}$

Supply voltage and temperature range

The 74 series and the 54 series are the examples of standard TTL logic families. These series operate on a power supply voltage of +5 V. But, it is found that the 74 series works reliably over the range +4.75 V to +5.25 V and the 54 series operates over the range +4.5 V to +5.5 V.

The 74 series can work reliably over a temperature range of 0°C to 70°C, while the 54 series can work over a temperature range of – 55°C to +125°C.

Summary of standard TTL

Table 1.5 summarizes the typical values of standard TTL parameters.

Table 1.5 Typical values for standard TTL parameters

Characteristics	*74 series*	*54 series*
Supply voltage	4.75 V to 5.25 V	4.5 V to 5.5 V
Temperature range	+0°C to 70°C	– 55°C to 125°C
Voltage levels	$V_{IH} = 2$ V, $V_{OH} = 2.4$ V $V_{IL} = 0.8$ V, $V_{OL} = 0.4$ V	$V_{IH} = 2$ V, $V_{OH} = 2.4$ V $V_{IL} = 0.8$ V, $V_{OL} = 0.4$ V
Current levels	$I_{IH} = 40\ \mu$A, $I_{OH} = -400\ \mu$A $I_{IL} = 1.6$ mA, $I_{OL} = 16$ mA	$I_{IH} = 40\ \mu$A, $I_{OH} = -400\ \mu$A $I_{IL} = 1.6$ mA, $I_{OL} = 16$ mA
Power dissipation	10 mW	10 mW
Propagation delay	10 ns	10 ns
Fan-out	10	10
Noise margin	0.4 V	0.4 V

1.11 COMMONLY USED ICs OF STANDARD TTL

Multiple emitter inputs and totem-pole output TTL circuits are used for different applications with a few exceptions. The 74 series is an example of a standard TTL family. It is available in different packages with different operations. The commonly used ICs of standard TTL are given in Table 1.6.

Table 1.6 Commonly used ICs of standard TTL

IC number	*Description*	*IC number*	*Description*
7400	Quad 2-inputs NAND gates	7411	Triple 3-inputs AND gates
7402	Quad 2-inputs NOR gates	7420	Dual 4-inputs NAND gates
7404	Hex Inverter	7424	Dual 4-inputs AND gates
7408	Quad 2-inputs AND gates	7432	Quad 2-inputs OR gates
7410	Triple 3-inputs NAND gates	7486	Quad 2-inputs EX-OR gates

1.12 IMPROVED TTL SERIES

TTL 54 series/74 series are the most popular and commonly used series of digital ICs. These series have the limitation of speed and power dissipation. These limitations are overcome up to a certain limit in the improved TTL series. The improved TTL series are as follows:

1. 74L series (low power TTL)
2. 74H series (high speed TTL)
3. 74S series (Schottky TTL)
4. 74LS series (low-power Schottky TTL)
5. 74AS series (advanced Schottky TTL)
6. 74ALS series (advanced low power Schottky TTL)
7. 74F series (fast TTL)

1.12.1 Low Power and High Speed TTL

The 74L series were developed to provide low power dissipation. The 74H series were developed to provide high speed. It is seen that the power dissipation goes down by increasing the charging resistance of the gate. Due to an increase in the value of the resistor, the delay is increased and the speed of operation is decreased. The 74L series has 1mW power dissipation and 33 ns propagation delay.

The speed of operation can be increased by reducing the value of the charging resistor. Due to low resistance, the power dissipation is increased. The high speed TTL, 74H series has 6 ns delay and 23 mW power dissipation.

The circuits of 74L series and 74H series are same as the circuit of a standard TTL, but they differ in circuit component values.

1.12.2 Schottky TTL

All the transistors in the circuits of standard TTL, low power TTL, and high speed TTL operate in saturation or cut-off region. When the transistor is in saturation, it stores the charge and the operation causes a storage-time delay during the transistor transition from ON to OFF; and this limits the circuit's switching speed.

In Schottky TTL families, Schottky transistors are used instead of normal transistors. The Schottky transistor is operated in active region or cut-off region, it never goes into saturation and the storage time delay is negligible.

The Schottky transistor is obtained by using a Schottky barrier diode between the base and the collector terminals of the transistor as shown in Fig.1.30(a).

The Schottky diode has a forward biased voltage of 0.25V. Because of this diode connected between the base and the collector terminals of the transistor, the collector junction of the transistor cannot get forward biased and the transistor never goes in saturation; the transistor operates in cut-off or active region. The symbol of Schottky transistor is shown in Fig. 1.30(b).

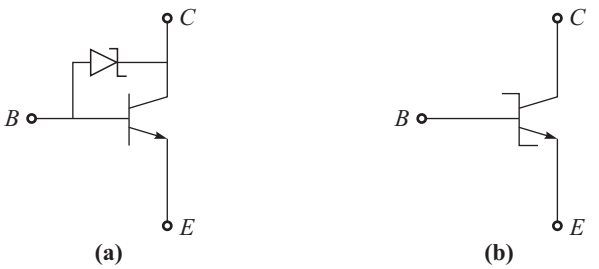


Fig. 1.30 Schottky transistor and Schottky symbol

The 74S series is an example of Schottky TTL. The propagation delay of Schottky TTL is 3 ns only, which is twice as fast as the 74H series. Figure 1.31 shows a basic NAND gate in Schottky TTL series.

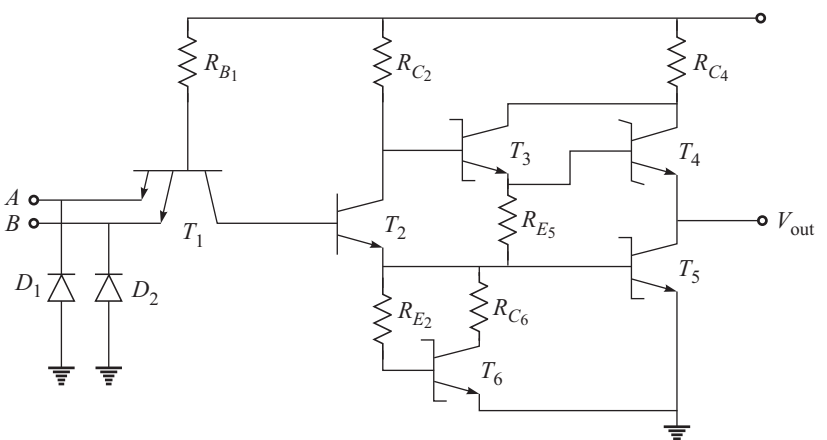


Fig. 1.31 Schottky TTL NAND gate

1.12.3 Low Power Schottky TTL

The 74LS series is a low power Schottky TTL. It uses Schottky transistors. It is similar to 74S, but it has a large value of charging resistor than 74S series. The large resistor values reduce the circuit power requirement but increase the time delay. The 74LS series has 9.5 ns propagation delay and 2 mW power dissipation. The 74AS series is an advanced Schottky TTL. The 74ALS series is an advanced low power Schottky TTL and the 74F series is a fast TTL.

1.13 COMPARISON OF TTL FAMILIES

A comparison of TTL families with respect to their common characteristics is given in Table 1.7.

Table. 1.7 Comparison of TTL families

Character-istics	*74*	*74 LS*	*74 S*	*74 ALS*	*74 AS*	*74 F*
Min. V_{OH}/V_{OL}	2.4/0.4	2.7/0.5	2.7/0.5	2.7/0.5	2.7/0.5	2.7/0.5
Max. V_{IH}/V_{IL}	2/0.8	2/0.8	2/0.8	2/0.8	2/0.8	2/0.8
Min. I_{OH}/I_{OL}	–0.4/16	–0.4/16	–1/20	–0.4/16	–2/20	–1/20
Max. I_{IH}/I_{IL}	40/(–1.6)	20/(–0.4)	50/(–2)	20/(– 0.2)	0.2/(–2)	20/(– 0.6)
T_{pd} (ns)	10	10	3	4	1.5	2.5
P.D. per gate (mW)	10	2	20	1	20	4

1.14 EMITTER COUPLED LOGIC

Emitter coupled logic (ECL) is faster than TTL family. The transistors of an emitter coupled logic are operated in cut-off or active region, it never goes in saturation and therefore the storage time is eliminated. Emitter coupled logic family is an example of unsaturated logic family. Figure 1.32 shows the circuit of an emitter-coupled logic OR/NOR gate.

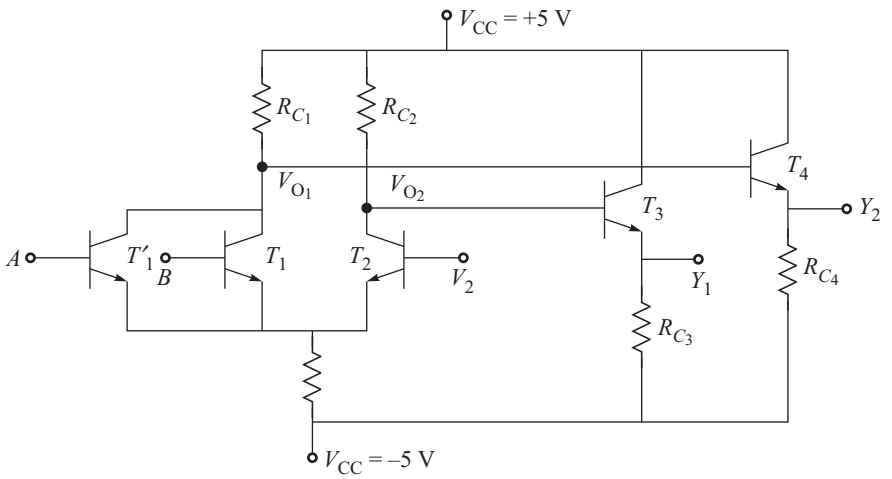


Fig. 1.32 Emitter coupled logic OR/NOR gate

The circuit consists of difference amplifiers and emitter followers. Emitter terminals of the two transistors are connected together and hence it is called as emitter coupled logic.

The emitter followers are used at the output of difference amplifier to shift the DC level. The circuit has two outputs Y_1 and Y_2, which are complementary. Y_1 corresponds to OR logic and Y_2 corresponds to NOR logic.

Operation

The input voltage of T_2 is $V_2 = V_{ref} = -1.15$ V.

- When both the inputs are in logic 0, T_1 and T'_1 operate in cut-off and T_2 operates in active region, voltage V_{O_1} is high, T_3 is ON, and the output at Y_2 is logic 1, voltage V_{O_2} is low, T_4 operates in cut-off and the output at Y_1 is logic 0.
- When any one of the inputs is in logic 1 level, the corresponding transistors T_1 or T'_1 are operated in active region and T_2 operates in cut-off, voltage V_{O_1} is low, T_3 operates in cut-off and Y_2 is logic 0, voltage V_{O_2} is high, T_4 operates in active region and Y_1 is logic 1.
- When both the inputs are in logic 1 state, T_1 and T'_1operate in active region and T_2 operates in cut-off, voltage V_{O_1} is low, T_3 operates in cut-off and Y_2 is logic 0, voltage V_{O_2} is high, T_4 operates in active region and Y_1 is logic 1.

The operation of the circuit is summarized in Table 1.8(a).

Table 1.8(a) Operation of ECL circuit

Inputs		*Transistors*			*Transistors*		*Output*	
A	***B***	T_1	T'_1	T_2	T_3	T_4	Y_1	Y_2
Logic 0	Logic 0	Cut-off	Cut-off	Active	Active	Cut-off	Logic 0	Logic 1
Logic 0	Logic 1	Cut-off	Active	Cut-off	Cut-off	Active	Logic 1	Logic 0
Logic 1	Logic 0	Active	Cut-off	Cut-off	Cut-off	Active	Logic 1	Logic 0
Logic 1	Logic 1	Active	Active	Cut-off	Cut-off	Active	Logic 1	Logic 0

In terms of 0 and 1, Table 1.8(a) can be written as in Table 1.8(b).

Table 1.8(b) Operation of ECL circuit

A	***B***	Y_1	Y_2
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

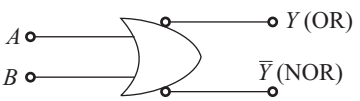


Fig. 1.33 Symbol of OR/NOR gate

The circuit shown in Fig.1.32 acts as a two-input OR/NOR gate and its truth table is given in Table 1.8(b). The symbol of emitter coupled logic OR / NOR gate is shown in Fig.1.33.

Fan-out

Fan-out of logic families is a function of current supply by the source and the input current of individual loaded gates. These are functions of the input and output resistances of the logic family. If the input resistance of a loaded gate is high, then the required current is less. If the output resistance is low, then the supply current is more. For emitter coupled logic, the transistor is used in the emitter follower mode due to which the input resistance is high and the output resistance is low. Thus, current supply by the driving gate is more and the current required to drive the individual gate is less and therefore the fan-out is large.

Wired-OR logic

The ECL circuit has two outputs Y_1 and Y_2. Y_1 is the output of OR logic and Y_2 is the output of NOR logic. ($Y_1 = A + B$, $Y_2 = \overline{Y} = \overline{A + B}$). When the outputs of two or more than two gates are connected, then an additional logic is realized without using any additional hardware. Consider the circuit shown in Fig. 1.34.

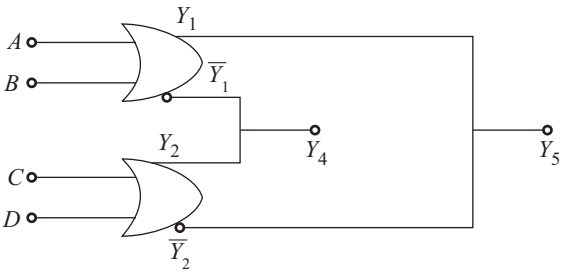


Fig. 1.34 Wired-OR logic

$$Y_4 = \overline{Y_1} + Y_2 = \overline{A \quad B} + C + D$$

$$Y_5 = Y_1 + \overline{Y_2} = A + B + \overline{C + D}$$

Consider another circuit shown in Fig. 1.35.

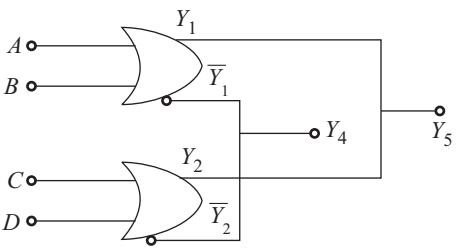


Fig. 1.35 Wired-OR logic

$$Y_4 = \overline{Y_1} + \overline{Y_2} = \overline{A + B} + \overline{C + D}$$

$$Y_5 = Y_1 + Y_2 = A + B + C + D \tag{1.15}$$

Unconnected inputs

If any one of the inputs of the ECL gate is open, then the corresponding transistor operates in cut-off and there is no current flow through the transistor. The same condition occurs when the input is in logic 0 level and hence the unconnected input of ECL is treated as logic 0.

ECL characteristics

Following are the characteristics of an ECL circuit:

1. Less propagation delay time ($t_d = 1$ ns).
2. The logic low-level voltage is –1.7 V and the logic high level voltage is –0.8 V.

3. Poor noise margin.
4. Power dissipation within the range of 40–55 mW.
5. Fan-out is 25.

1.15 INTEGRATED INJECTION LOGIC (I^2L)

The integrated injection logic uses only transistors for the construction of a gate and hence it becomes possible to integrate a large number of gates in a single package. This IC is easier and cheaper to fabricate. The figure of merit of I^2L circuits is quite small (4 PJ).

1.15.1 I^2L Inverter

Figure 1.36 shows a simple inverter circuit. If the input V_1 is at low logic level, transistor T_1 is off and $I_{B_1} = 0$.

The input source acts as a sink for the current supplied by the current source I_1 and the output is at high logic level. If the input is high, the base current $I_{B_1} = I_S + I_1$ and T_1 operates in saturation. The output is at low logic level.

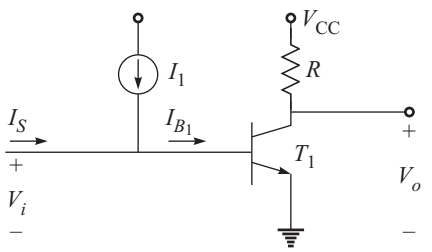


Fig. 1.36 I^2L Inverter with current source

Figure 1.37 shows a simple inverter circuit with transistor T_2 as the constant current source, hence T_2 is in series as a constant current source.

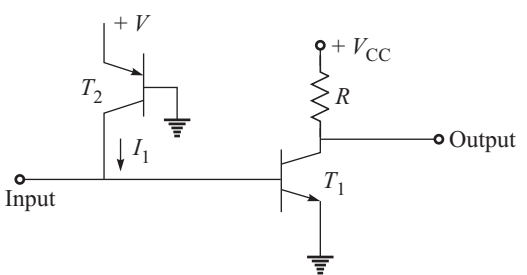


Fig. 1.37 I^2L Inverter with transistor as current source

When the input is low, the source sinks the current and T_1 is off and the output is high. When the input is high, the base current of T_1 is the sum of currents I_1 and the current supplied by the source, T_1 is ON and the output is low.

Figure 1.38 shows the I^2L inverter circuit with two output terminals. Transistor T_1 has two collector terminals. The outputs are connected directly to the inputs of other I^2L gate.

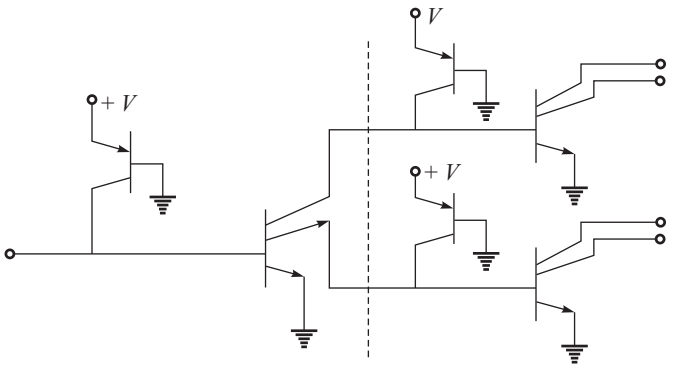


Fig. 1.38 I^2L inverter circuit with two output terminals

1.15.2 I^2L NAND Gate

Figure 1.39 shows the I^2L NAND gate. When inputs A and B are low or any one of the inputs is low, the current provided by T_2 is sinked by the source, T_1 is OFF, and the output is high. When both the inputs are high, the base current of T_1 is the sum of currents provided by the source and T_2, transistor T_1 is ON and the output is low.

Table 1.9 Truth Table of NOR gate

Inputs		*Output*
A	***B***	***Y***
0	0	1
0	1	1
1	1	1
1	1	0

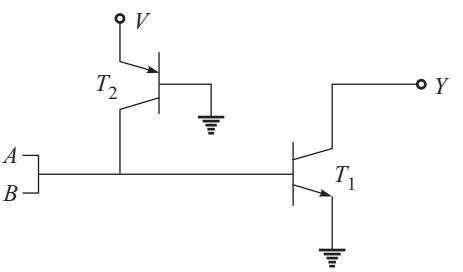


Fig. 1.39 I^2L NAND gate

1.15.3 I^2L NOR Gate

Figure 1.40 shows the I^2L NOR gate. The circuit has two inverters with their outputs connected together. When both or any one of the inputs is high, the output of the corresponding inverter is low and the resulting output is low.

When both inputs are low, the output of both the inverters is high and the result is also high.

Table 1.10 Truth Table of NOR gate

Inputs		*Outputs*		***Y***
A	***B***	Y_1	Y_2	
0	0	1	1	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	0

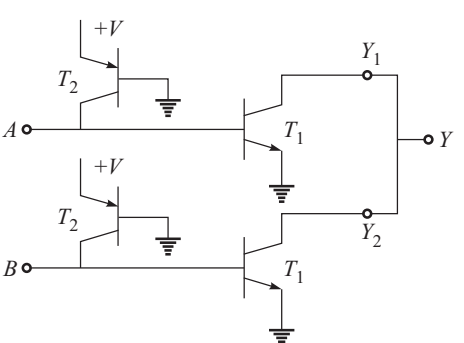


Fig. 1.40 I^2L NOR gate

1.16 MOSFET LOGIC

MOSFETs are very popular due to their low power dissipation and high density of fabrication. The logic families of MOSFETs can be classified into three categories: (i) PMOS, (ii) NMOS, and (iii) CMOS.

PMOS logic is slow as compared to NMOS logic. Hence, it is not used in new designs.

1.17 NMOS

MOSFETs are of two types—*depletion type* and *enhancement type*. NMOS family uses only *n*-channel enhancement MOSFETs.

1.17.1 NMOS Inverter

Figure 1.41 shows the circuit of an NMOS inverter consisting of *n*-channel MOSFETs. When the drain and gate terminals of MOSFETs are short-circuited, then it acts as a resistor.

In Fig. 1.41, MOSFET Q_1 acts as a load resistor and MOSFET Q_2 acts as a switching element. Q_1 is always ON; the load resistance is equal to R_{ON} of the *n*-channel MOSFET. Instead of load resistance, Q_1 is used, which reduces the size of the chip. Q_1 may be of depletion type or enhancement type. But Q_2 is always of enhancement type.

Operation

- When the input signal is high (positive voltage), Q_2 is ON, the current flows through the drain terminal and the output is low.
- When the input signal is low (0 V or negative voltage), Q_2 is OFF, there is no current flow through the circuit and the output is high (V_{DD}).

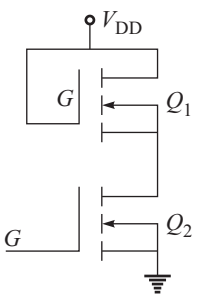


Fig. 1.41 NMOS inverter

The operation of the circuit is summarized in Table 1.11 (a). In terms of 0 and 1, we can write it as in Table 1.11(b). The circuit in Fig. 1.41 acts as a NOT gate and its truth table is given in Table 1.11(b).

Table 1.11 (a) Operation of NMOS inverter

V_{in}	Q_2	V_O
0 V	OFF	V_{DD} = +5 V
+ 5 V	ON	0 V

Table 1.11 (b) Operation of NMOS inverter

V_{in}	V_O
0	1
1	0

1.17.2 NMOS NAND Gate

Similar to NMOS inverter, Q_1 acts as a load resistor that reduces the size of the chip; and here Q_1 is always ON. Q_2 and Q_3 are the switching elements. These two

switching elements are connected in series, which are controlled by the inputs A and B. Q_1 may be of depletion type or enhancement type, but Q_2 and Q_3 are always enhancement MOSFETs.

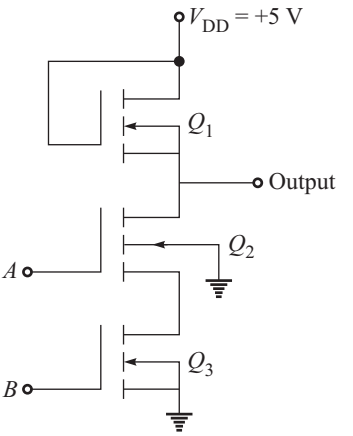


Fig. 1.42 A two-input NAND gate using NMOS

Operation

- When both of the inputs are low, Q_2 and Q_3 are OFF, the current cannot flow through the drain terminal and the output is high (V_{DD}).
- When any one of the inputs is low (0V or negative), then the corresponding MOSFET is OFF. There is no current flow through the circuit and the output is high (V_{DD}).
- When inputs are high (+ve voltage), Q_2 and Q_3 are ON. The current flows through the drain terminal and the output is low.

The operation of the circuit is summarized in Table 1.12(a).

Table 1.12(a) Operation of NMOS NAND gate

A	*B*	Q_2	Q_3	V_o
LOW	LOW	OFF	OFF	HIGH
LOW	HIGH	OFF	ON	HIGH
HIGH	LOW	ON	OFF	HIGH
HIGH	HIGH	ON	ON	LOW

In terms of 0 and 1, Table 1.12(a) can be written as in Table 1.12(b).

Table 1.12(b) Operation of NMOS NAND gate

A	*B*	V_O
0	0	1
0	1	1
1	0	1
1	1	0

The circuit shown in Fig.1.42 acts as a two-input NAND gate and its truth table is given in Table 1.12(b).

1.17.3 NMOS NOR Gate

Figure 1.43 shows a two-input NMOS gate. Q_1 acts as a load resistor. It is always ON. MOSFETs Q_2 and Q_3 are the switching elements. These switching elements are connected in parallel, which are controlled by inputs A and B. Instead of load resistance, Q_1 is used which reduces the size of the chip. Q_1 may be of depletion type or enhancement type, but Q_2 and Q_3 are always enhancement MOSFETs.

Operation

- When both the inputs are low, Q_2 and Q_3 are OFF. The current cannot flow through the drain terminal and the output is high (V_{DD}).
- When any one of the inputs is high (0 V or –ve), then the corresponding MOSFET is ON. The current flows through the circuit and the output is low.
- When inputs are high (+ve voltage), Q_2 and Q_3 are ON. The current flows through the drain terminal and the output is low.

The operation of the circuit is summarized in Table 1.13(a).

Table 1.13(a) NMOS NOR gate

A	*B*	Q_2	Q_3	V_o
LOW	LOW	OFF	OFF	HIGH
LOW	HIGH	OFF	ON	LOW
HIGH	LOW	ON	OFF	LOW
HIGH	HIGH	ON	ON	LOW

In terms of 0 and 1, Table 1.13(a) can be written as in Table 1.13(b).

Table 1.13(b) NMOS NOR gate

A	*B*	V_o
0	0	1
0	1	0
1	0	0
1	1	0

The circuit shown in Fig. 1.43 acts as a two-inputs NAND gate and its truth table is given in Table 1.13(b).

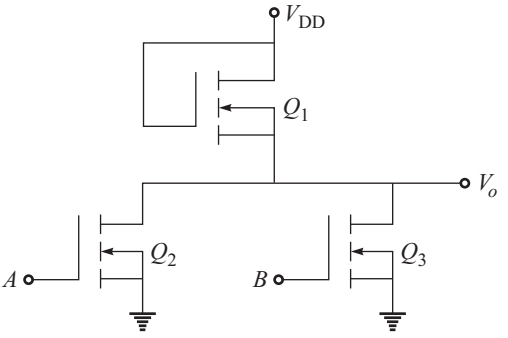


Fig. 1.43 NMOS NOR gate

1.17.4 Fan-out

We have seen that the fan-out of a logic family is the function of its input and output impedance. For high input impedance, the fan-out is large. MOSFET devices have very high input impedance, therefore fan-out is large. Since the number of driving gates is more, the capacitor at the driving gate output considerably reduces the speed of MOSFET gate.

1.17.5 Propagation Delay Time

It is a function of the capacitor of loaded gate and the charging resistor. In case of MOS devices, the large capacitor is present at input and output and the resistor through which the capacitor gets charged or discharged is also high. Hence, the propagation delay is large and the speed of operation is low.

1.17.6 Power Dissipation

It is a function of current supply by the source and resistance of the load. The power supply by the source in MOS logic family is small and hence the power dissipation is low.

1.17.7 Characteristics of NMOS

Table 1.14 summarizes the characteristics of NMOS.

Table 1.14 Characteristics of NMOS

Parameter	*Value*	*Parameter*	*Value*	*Parameter*	*Value*
V_{IH}	2.0 V	I_{OH}	– 400 μA	t_{PHL}	60 ns
V_{IL}	0.8 V	I_{OL}	2 mA	t_{PLH}	45 ns
V_{OH}	2.4 V	Fan-out	30	P.D.	0.1 mW
V_{OL}	0.45 V	Noise margin	1.5 V		

1.18 CMOS

CMOS family uses *n*-channel and *p*-channel MOSFETs. In CMOS, *p*-channel and *n*-channel MOS devices are fabricated on the same chip, which makes its fabrication complicated but it reduces the packaging density, and has small power consumption. Hence, CMOS is ideally suited for battery-operated systems.

1.18.1 CMOS Inverter

Figure 1.44 shows a CMOS logic inverter. For the circuit, the logic levels are 0 V and V_{CC}. It is important to note that the *p*-channel MOSFET is ON, when the input is 0 V and the *n*-channel MOSFET is ON, when the input is V_{CC}. Q_1 is *p*-channel and Q_2 is *n*-channel. When Q_1 is ON, the output voltage is equal to V_{CC} and when Q_2 is ON, the output voltage is equal to 0 V.

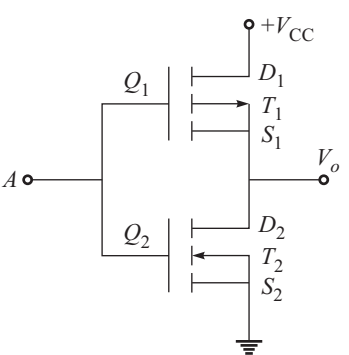


Fig. 1.44 CMOS inverter

Operation

- When the input is low, Q_1 is ON and Q_2 is OFF, output is high.
- When the input is high, Q_1 is OFF and Q_2 is ON, output is low.

Table 1.15 shows the operation of CMOS inverter.

Table 1.15 Operation of CMOS inverter

A	Q_1	Q_2	V_O
0	ON	OFF	1
1	OFF	ON	0

1.18.2 CMOS NAND Gate

Figure 1.45 shows a two-inputs CMOS logic NAND gate. It consists of two *p*-channel and two *n*-channel MOSFETs. *p*-channel MOSFETs are connected in parallel and *n*-channel MOSFETs are connected in series. Here, Q_1 and Q_2 are *p*-channel MOSFETs and Q_3 and Q_4 are *n*-channel MOSFETs.

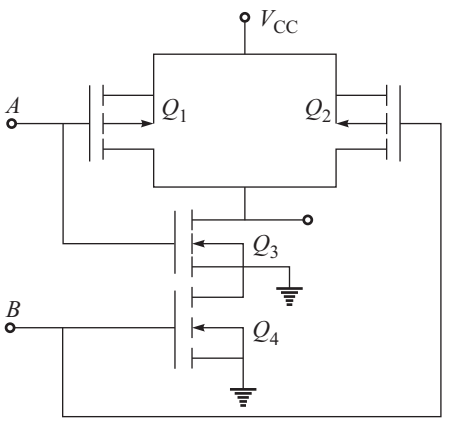


Fig. 1.45 CMOS NAND gate

Operation

- When the inputs are low, Q_1 and Q_2 are ON, Q_3 and Q_4 are OFF, and the output is high (V_{DD}).
- When any one of the inputs is low (0 V or –ve), then the corresponding MOSFET Q_1 or Q_2 is ON, Q_3 or Q_4 is ON, and the output is high.
- When the inputs are high (+ve voltage), Q_1 and Q_2 are OFF, Q_3 and Q_4 are ON, and the output is low.

The operation of the circuit is summarized in Table 1.16.

Table 1.16 Operations of CMOS NAND gate

A	*B*	Q_1	Q_2	Q_3	Q_4	V_O
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

1.18.3 CMOS NOR Gate

Figure 1.46 shows a two-inputs CMOS logic NOR gate. It consists of two *p*-channel and two *n*-channel MOSFETs. *n*-channel MOSFETs are connected in parallel and *p*-channel MOSFETs are connected in series. Here, Q_1 and Q_2 are *p*-channel MOSFETs and Q_3 and Q_4 are *n*-channel MOSFETs. When the input is low, *p*-channel MOSFETs are ON and *n*-channel MOSFETs are OFF. When the input is high, *p*-channel is OFF and *n*-channel is ON.

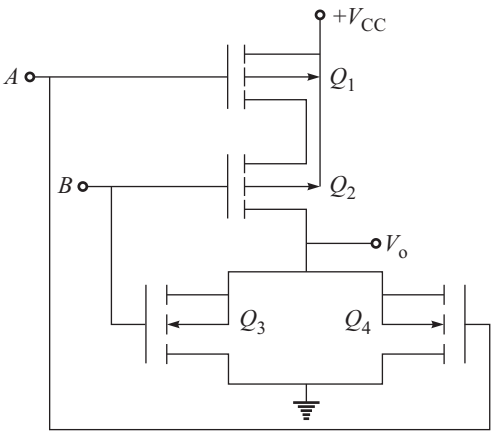


Fig. 1.46 CMOS NOR gate

Operation

- When inputs are low, Q_1 and Q_2 are ON, Q_3 and Q_4 are OFF, and the output is high (V_{DD}).
- When any one of the inputs is low (0 V or –ve), then the corresponding MOSFET Q_1 or Q_2 is ON, Q_3 or Q_4 is ON, and the output is low.
- When inputs are high (+ve voltage), Q_1 and Q_2 are OFF, Q_3 and Q_4 are ON, and the output is low.

Table 1.17 Operations of CMOS NOR gate

A	*B*	Q_1	Q_2	Q_3	Q_4	V_O
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

1.18.4 Characteristics of CMOS

The 54C/74C series is the commonly used CMOS series of ICs. The electrical characteristics of 54C/74C CMOS logic family are given in Table 1.18 for a supply voltage of 5 V.

Table 1.18 Electrical characteristics of 54C/74C CMOS logic family

Parameter	*Value*	*Parameter*	*Value*	*Parameter*	*Value*
V_{IH}	3.5 V	I_{IH}	1 μA	t_{PHL}	60 ns
V_{IL}	1.5 V	I_{IL}	–1 μA	t_{PHL}	45 ns
V_{OH}	4.5 V	I_{OH}	–100 μA	P.D.	10 mW
V_{OL}	0.5 V	I_{OL}	–360 μA		

Operation speed

The speed of a logic family is defined in terms of its propagation delay. The propagation delay,

$$t_p = \frac{t_{PHL} + t_{PLH}}{2}$$

$$= \frac{60 \text{ ns} + 45 \text{ ns}}{2} = 52.5 \text{ ns}$$

Noise margin

It is the capability of a gate to tolerate noise.

Logic 1 level noise margin = $V_{OH} - V_{IH}$

$$\Delta 1 = 4.5 \text{ V} - 3.5 \text{ V} = 1 \text{ V}$$

Logic 0 level noise margin = $V_{IL} - V_{OL}$

$$\Delta 0 = 1.5 \text{ V} - 0.5 \text{ V} = 1 \text{ V}$$

Fan-out

MOS devices have a very high input impedance; therefore, the fan-out is large. Fan-out of a CMOS is 50 for low frequency and less than 50 for high frequency inputs.

Power dissipation

It is a function of current supply by the source. The current drawn from the supply in CMOS logic is less. Hence the power consumption in MOS circuit is less. Power dissipation for CMOS logic family is 1 mW at 1 MHz. It is less than 1 mW for frequencies less than 1 MHz.

Unused inputs

The IC of a logic family may have more than one gate. CMOS inputs have to be connected with a fixed voltage level or to another input. If inputs of unused CMOS gates are open, they are susceptible to noise and static charge that could bias both *p* and *n*-channel MOSFETs in the conductive state and power dissipation is increased.

1.18.5 Buffered and Unbuffered Gates

CMOS circuits are available in two versions, namely (*i*) CMOS with buffered output and (ii) CMOS with unbuffered output.

We have discussed unbuffered outputs of CMOS inverter, CMOS NAND gate, and CMOS NOR gate. To improve the sharpness of the voltage transitions at the output, the buffered version of CMOS circuit is used. Because of the buffer used at

the output, the propagation delay of the gate is increased and it reduces the speed of operation.

1.18.6 Transmission Gates

Figure 1.47 shows the circuit of a transmission gate where Q_1 is PMOS and Q_2 is NMOS. Gates of Q_1 and Q_2 are controlled by the controlled inputs C and $\overline{C}$, respectively.

When $C = 1$ (high), Q_1 and Q_2 are ON or OFF depending upon the input A. When input A is high, then Q_2 is OFF and Q_1 is conducting in the ohmic region; Q_1 behaves as a small resistance connecting the output to the input and output $Y = A =$ high. When input A is low, then Q_1 is OFF and Q_2 is conducting in the ohmic region; Q_2 behaves as a small resistance connecting the output to the input and output $Y = A =$ low.

When $C = 0$ (low), both the MOSFETs are OFF and transmission is not possible.

In short, a transmission gate is a digital controlled CMOS switch. The symbol of transmission gate is shown in Fig. 1.48.

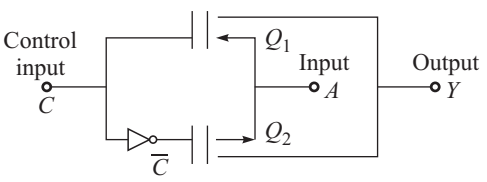


Fig. 1.47 Circuit of transmission gate

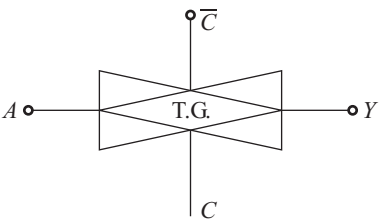


Fig. 1.48 The symbol of transmission gate

1.18.7 Open Drain Outputs

Different outputs are available in CMOS logic family as in the TTL family we had discussed earlier. In CMOS, open drain output is possible by replacing the transistor with a diode. See Fig. 1.49.

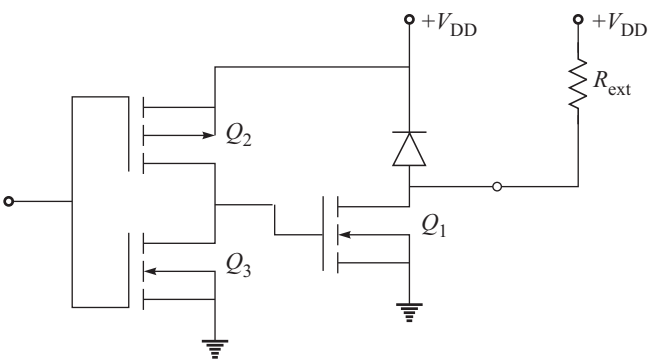


Fig. 1.49 Open drain outputs

The diode D_1 provides protection from electrostatic discharge. As in TTL, an external pull-up resistor is required to take the output. The open drain outputs CMOS supports wired-AND operation also.

1.18.8 High Impedance Outputs

The high impedance output CMOS logic family is similar to the tri-state output in TTL family. Figure 1.50 shows the high impedance output CMOS logic family.

The enable input E is active low input. When E is low, Q_1 will be ON as the input to Q_1 is $(E + I)$, and I (input) is low. Now at the same time, Q_2 is off. Therefore the output is high. When the enable input is low and the input is high, $(E + I)$ and $\overline{E}I$ inputs to Q_1 and Q_2, respectively, are high. So Q_1 will be OFF and Q_2 will be ON.

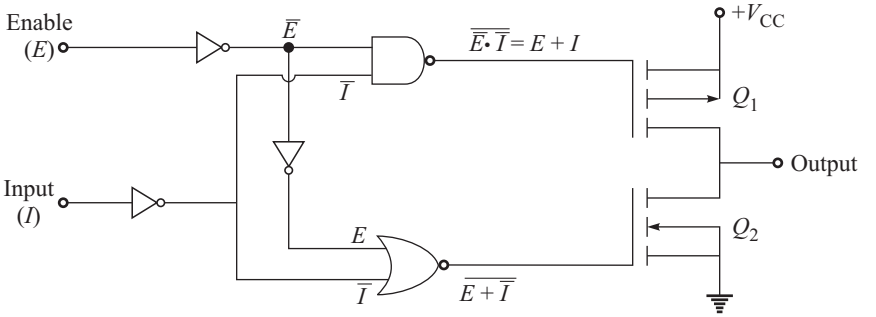


Fig. 1.50 High impedance output CMOS logic family

When the enable input is high, $E + I$ is always high, and $\overline{E}I$ is always low, independent of input high. Due to this, Q_1 and Q_2 are OFF, and the output is in a high impedance state.

1.18.9 Specifications and Standards

The EIA [Electronic Industries Association] has established certain standard specifications for CMOS circuits. In standards to differentiate buffered CMOS, it is identified as B-types and unbuffered are identified as VB types.

Table 1.19 Electrical characteristics
(Supply voltage V_{DD} = 5 V)

Parameter	*Value*
V_{IH}	3.5 V
V_{IL}	1.5 V
V_{OH}	4.5 V
V_{OL}	0.5 V
I_{IH}	1 μA
I_{IL}	–1 μA
I_{OH}	–100 μA
I_{OL}	360 μA
t_{PHL}	60 ns
t_{PLH}	45 ns
Static power dissipation per gate	10 mW

1.19 COMPARISON OF CMOS AND TTL FAMILIES

The CMOS and TTL families are compared and the comparison is given in Table 1.20.

Table 1.20 Comparison of CMOS and TTL families

Parameter	*CMOS*		*TTL*			
	Silicon gateCMOS	*Metal gate CMOS*	*74*	*74L*	*74AS*	*74ALS*
V_{IH}(min)	3.5 V	3.5 V	2.0 V	2.0 V	2.0 V	2.0 V
V_{IL}(max)	1.0 V	1.5 V	0.8 V	0.8 V	0.8 V	0.8 V
V_{OH}(min)	4.9 V	4.95 V	2.4 V	2.7 V	2.7 V	2.7 V
V_{OL}(max)	0.1 V	0.05 V	0.4 V	0.5 V	0.5 V	0.4 V
V_{NH}	1.4 V	1.45 V	0.4 V	0.7 V	0.7 V	0.7 V
V_{NL}	0.9 V	1.45 V	0.4 V	0.3 V	0.3 V	0.4 V
t_{pd}	8 ns	105 ns	10 ns	10 ns	1.5 ns	4 ns
P.D. (per gate)	0.17 mW	0.1 mW	10 mW	2 mW	8.5 mW	1 mW
$I_{pd} \infty$ P.D.	1.4 PJ	10.5 PJ	100 PJ	20 PJ	12.8 PJ	4 PJ

PJ – Pico-Joule, ns – nanosecond, and mW – milliWatts

The fan-out of CMOS is more than TTL. It is typically 50 for CMOS and 10 for TTL. CMOS is more susceptible to noise than TTL.

1.20 INTERFACING CMOS AND TTL DEVICES

Interfacing means connecting two different systems or devices, having different electrical characteristics. In such a case, direct connection is not possible. The circuit used to connect driver and load circuits is called as the *interface circuit*. The interface circuit takes the input from the driver and converts it, so that it is compatible with the requirements of the load.

Following are the important factors to be considered:

- The driver output must satisfy the voltage and current requirements of the load circuit.
- The driver and load circuit may require different power supplies. In such cases, the output of both circuits must swing between their specified voltage ranges.

1.20.1 TTL Driving CMOS

As TTL is driving CMOS, it must meet the current and voltage requirements of the load device. Supply voltage is 5 V.

Table 1.21 Current and voltage requirements of CMOS and TTL

Parameter	*CMOS*		*TTL*		
	4000 B	*74HCT*	*74*	*74L*	*74AS*
I_{IH} (min)	1 μA	1 μA	40 μA	20 μA	200 μA
I_{IL} (max)	1 μA	1 μA	1.6 mA	0.4 mA	2 mA
I_{OH} (min)	0.4 mA	4 mA	0.4 mA	0.4 mA	2 mA
I_{OL} (max)	0.4 mA	4 mA	16 mA	8 mA	20 mA

From Table 1.21, it is clear that the TTL has no problem to drive the CMOS, as the input current requirement of CMOS is very low as compared to the output current capabilities of TTL.

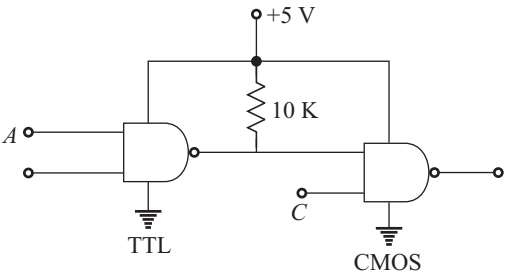


Fig. 1.51 TTL driving CMOS

1.20.2 CMOS Driving TTL

It is necessary to check the CMOS output capacity and the TTL input requirements. Table 1.22 compares the two.

Table 1.22 CMOS output capacity and TTL input requirements

CMOS (4000 B)	TTL
V_{OH} (min) = 4.95 V	V_{IH} (min) = 2.0 V
V_{OL} (max) = 0.05 V	V_{IL} (max) = 0.8 V
I_{OH} (min) = 0.4 mA	I_{IH} (min) = 40 μA
I_{OL} (max) = 0.4 mA	I_{IL} (max) = 1.6 mA

* μA – microampere and mA – milliampere

From the above table, it is proved that the CMOS driving a TTL in the high state do not need any special consideration such as,

V_{OH} (CMOS) > V_{IH} (TTL)

I_{OH} (CMOS) > I_{IH} (TTL)

For the CMOS driving a TTL in low state, see the parameter

V_{OL} (max) CMOS < V_{IL} (max) TTL

This satisfies the requirement in the low state. Now see the current parameter.

I_{OL} (CMOS) must be greater than I_{IL} (max) for TTL.

I_{OL} (CMOS) < I_{IL} (max)

This does not satisfy the condition. In this situation, some buffer circuit is required to be connected between the two. Figure 1.52 shows what it means.

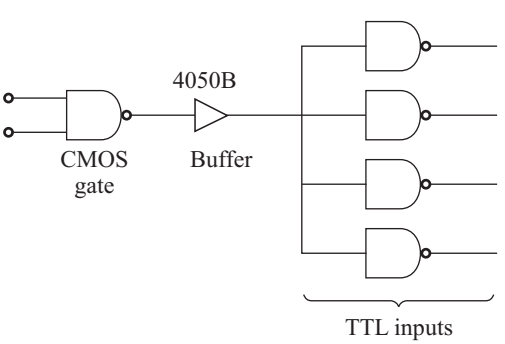


Fig. 1.52 CMOS driving TTL

The above discussion of CMOS and TTL interfacing is only for standard CMOS and standard TTL logic families. For other families, like high speed, low power, it is necessary to compare the output capabilities of driver and the input requirements of load on the same lines as above.

1.21 INTERFACING ECL AND TTL DEVICES

Interfacing means connecting two different systems or devices, having different electrical characteristics. In such a case, direct connection is not possible. The circuit used to connect driver and load circuits is called as the *interface circuit*. The interface circuit takes the input from the driver and converts it, so that it is compatible with the requirements of the load.

1.21.1 TTL Driving ECL

As TTL is driving ECL, it must meet the current and voltage requirements of the load device. A TTL cannot interface directly with an ECL; it requires a translator. The MC10H124 is a TTL to ECL translator. The logic diagram of MC10H124 is shown in Fig. 1.53; it is a 16-pin IC and it uses two power supplies.

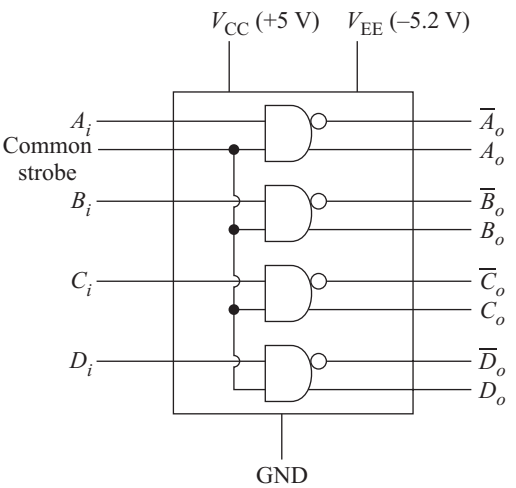


Fig. 1.53 Logic diagram of MC10H124

The logic levels of the translator are:

$$V_{IH} = 2\text{ V}, V_{IL} = 0.8\text{ V}, V_{OH} = -0.98\text{ V and } V_{OL} = -1.63\text{ V}$$

The logic levels of the TTL are: $V_{OH} = 2.4$ V and $V_{OL} = 0.4$ V

The logic levels of the ECL are: $V_{IH} = -1.4$ V and $V_{IH} = -1.2$ V

It is observed that

$$V_{IH}\text{ (Translator)} < V_{OH}\text{ (TTL)}, V_{IL}\text{(Translator)} > V_{OL}\text{ (TTL)}$$

and $$V_{IH}\text{ (ECL)} < V_{OH}\text{ (Translator)}, V_{IL}\text{(ECL)} > V_{OL}\text{ (Translator)}.$$

It shows that the input logic levels of a translator are compatible with the output logic levels of a TTL and the output logic levels of a translator are compatible with the input logic levels of an ECL. Figure 1.54 shows the TTL gate driving an ECL gate.

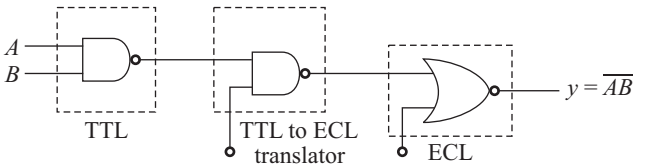


Fig. 1.54 TTL driving ECL

1.21.2 ECL Driving TTL

An ECL cannot interface directly with a TTL; it requires a translator. The MC10H125 is an ECL to TTL translator. The logic diagram of MC10H124 is shown in Fig. 1.55; it is a 16-pin IC and it uses two power supplies.

The logic levels of the translator are:

$V_{IH} = -1.13$ V, $V_{IL} = -1.48$ V,
$V_{OH} = 2.5$ V, and $V_{OL} = 0.5$ V

It shows that the input logic levels of a translator are compatible with the output logic levels of ECL and the output logic levels of a translator are compatible with the input logic levels of a TTL. Figure 1.56 shows the ECL gate driving a TTL gate.

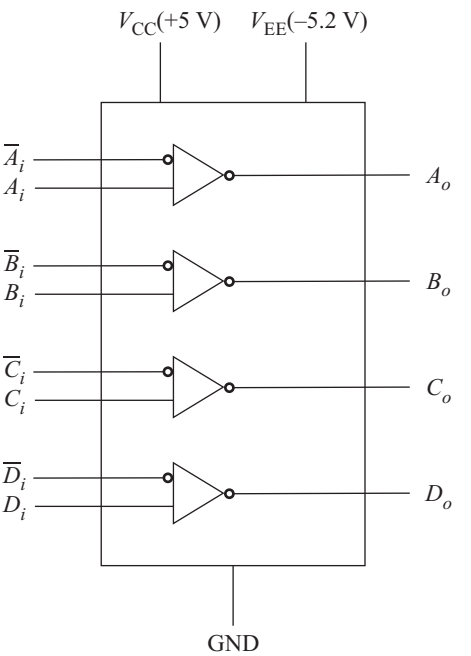
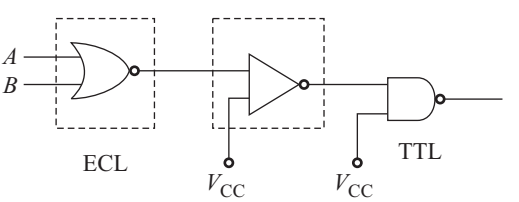


Fig. 1.55 Logic diagram of MC10H125



ECL to TTL translated

Fig. 1.56 ECL driving TTL

SUMMARY

- Modern digital systems use integrated circuits because of the following advantages:
  1. Overall size of digital system gets reduced, because ICs consist of a large number of digital circuits.
  2. The cost of ICs is very low.
  3. Power consumption is less.
  4. They have high noise margin.
  5. They have high reliability.
  6. The operating speed is high.
- The logic families are classified into two types: (a) Bipolar logic families, and (b) Unipolar logic families.
- Bipolar logic families are further classified as: (a) Saturated bipolar logic families, and (b) Unsaturated bipolar logic families.
- The examples of saturated bipolar logic families are: (a) Resistor-transistor logic, (b) Direct coupled transistor logic, (c) Integrated injection logic, (d) Diode-transistor logic, (e) High threshold logic, and (f) Transistor-transistor logic.
- The examples of unsaturated bipolar logic families are: (a) Schottky transistor-transistor logic, and (b) Emitter-coupled logic.
- The examples of unipolar families are: (a) PMOS, (b) NMOS, and (c) CMOS.
- The various parameters of digital ICs used to compare their performance are: (a) Speed of operation, (b) Power dissipation, (c) Figure of merit, (d) Fan-out, (e) Fan-in, (f) Current and voltage parameters, (g) Noise immunity, (h) Power supply requirements, and (i) Operating temperature.
- The RTL family is no more used because of: (a) Low noise margin (typically 0.1 V), (b) Fan-out is poor (typically 5), (c) Propagation delay is high and speed of operation is low (12 ns), and (d) High power dissipation (typically 12 mW).
- The DCTL is simple than RTL, it is not popular because of the current hogging problem.
- A standard TTL can be classified as: (a) TTL with passive pull-up, (b) TTL with totem-pole output (c) TTL with open collector output, and (d) Tri-state TTL.

KEY TERMS AND DEFINITIONS

Integrated circuit Most of the digital circuits are constructed on a single chip, which are referred to as integrated circuits (IC).

Logic family The set of compatible ICs with the same logic levels and same supply voltages, fabricated to perform various logic functions, are known as logic family.

Unipolar logic family The logic family having unipolar devices like MOSFETs as its key element is referred to as unipolar logic family.

Bipolar logic family The logic family with transistors and diodes as its key element is referred to as bipolar logic family.

Resistor-transistor logic (RTL) The logic family that consists of resistors and transistors is called as resistor-transistor logic.

Direct coupled transistor logic (DCTL) The logic family in which the input signal is directly given to the base of the transistor is known as the direct coupled transistor logic.

Diode-transistor logic (DTL) The logic family with diodes and transistors is called as diode-transistor logic.

Transistor-transistor logic (TTL) The saturated logic family consisting transistor as its basic element, which operates either in cut-off or saturation region, is called transistor-transistor logic.

Emitter coupled logic (ECL) The transistors of emitter coupled logic is operated in cut-off or active region, it never goes in saturation and therefore the storage time is eliminated.

Integrated injection logic (I^2L) It uses only transistors for the construction of gate and hence, it becomes possible to integrate a large number of gates in a single package.

MOSFET logic MOSFETs are very popular for logic circuit because of their low power dissipation and high density of fabrication.

CMOS logic CMOS family uses *n*-channel and *p*-channel MOSFETs. In CMOS, *p*-channel and *n*-channel MOS devices are fabricated on the same chip, which makes its fabrication complicated but it reduces the packaging density. It has small power consumption.

EXERCISES

Review Questions

1. With respect to logic gate, explain the following terms: I_{OL}, I_{IL}, I_{OH}, I_{IH}. Specify the values of these parameters for a standard TTL gate. Define fan-out. How do you obtain fan-out from the above four parameters?
2. Explain CMOS inverter gate with a circuit diagram.
3. Explain the totem-pole output configuration for a TTL gate.
4. With the help of a neat diagram, explain the working of a two-inputs CMOS NAND gate. What is the advantage of active load?
5. Define the following parameters of digital IC families and give their typical values for TTL and CMOS families.
   (a) Propagation delay (b) Noise margin
   (c) Fan-out (d) Figure of merit
6. Explain the working of a two-inputs TTL NAND gate with the help of a circuit diagram.
7. Explain the following parameters:
   (a) Propagation delay (b) Fan-out
   (c) Noise margin (d) Power dissipation
8. Write a short note on CMOS logic family.
9. How is propagation delay improved in totem-pole TTL logic?
10. Give typical values of the following parameters for TTL and CMOS logic gates:
    (a) Propagation delay (b) Fan-out
    (c) Noise margin (d) Power dissipation
11. Describe the difference between current sinking and current sourcing in TTL logic.

12. Explain the working of basic TTL NAND gate with a neat diagram. Explain the following three types of output configuration.
    (a) Open collector output (b) Totem-pole output
    (c) Tri-state output
13. Explain the basic ECL OR/NOR gate with a neat circuit diagram. Why does the ECL family have the lowest propagation delay of all logic families?
14. Give typical values of the following parameters for CMOS logic gates:
    (a) Propagation delay (b) Fan-out
15. With a neat circuit diagram, explain the operation of a two-inputs CMOS NOR gate.
16. Explain interfacing of a TTL gate driving CMOS gates and vice versa.
17. Define the following parameters of logic families and give their typical values for a standard TTL gate:
    (a) Propagation delay (b) Fan-out
    (c) Noise margin (d) Figure of merit
18. Explain with a neat circuit diagram the tri-state TTL gate. How can the tri-state circuit outputs be connected together to form a data bus so that each output can be switched onto the bus wire?
19. Draw neat circuit diagrams of:
    (a) Two-inputs TTL NAND gate with totem-pole output
    (b) Two-inputs CMOS NAND gate

Multiple Choice Questions

Select the correct option.

1. Positive logic in a logic circuit is one in which.....
    (a) logic 0 and 1 are represented by negative and positive voltages respectively
    (b) logic 0 voltage level is higher than logic 1 voltage level
    (c) logic 0 voltage level is lower than logic 1 voltage level
    (d) logic 0 and 1 are represented by 0 and positive voltages respectively
2. In standard TTL gates, the totem–pole output stage is primarily used to.....
    (a) increase the noise margin of the gate
    (b) decrease the output switching delay
    (c) facilitate a wired-OR logic connection
    (d) increase the output impedance of the circuit
3. The switching speed of ECL is very high, because.....
    (a) the transistors are switched between cut-off and saturation regions
    (b) the transistors are switched between active and saturation regions
    (c) the transistors are switched between cut-off and active regions
    (d) the transistors may operate in any of the three regions
4. In standard TTL, the totem-pole stage refers to.....
    (a) the multi-emitter input stage
    (b) the phase-splitter
    (c) the output buffer
    (d) the open collector output stage

5. The figure of merit of a logic family is given by.....
   (a) gain-bandwidth product
   (b) product of propagation delay time and power dissipation
   (c) product of fan-out and propagation delay time
   (d) product of noise margin and power dissipation
6. Which of the following uses the least power?
   (a) TTL (b) ECL
   (c) CMOS (d) all use same power
7. Which of the following logics is the fastest?
   (a) TTL (b) ECL
   (c) CMOS (d) LSI
8. In Schottky-clamped TTL, the purpose of Schottky diode is.....
   (a) to increase propagation delay
   (b) to achieve efficient non-saturated switching
   (c) to improve noise margin
   (d) to decrease dissipation

Answers

1. (d)	2. (b)	3. (c)	4. (c)
5. (b)	6. (c)	7. (b)	8. (b)