بسمه تعالی

دانشکده مهندسی برق و کامپیوتر

دانشگاه صنعتی اصفهان

زبان‌های توصیف سخت‌افزار و مدارات – نیمسال دوم ۹۹-۱۳۹۸

تکلیف شماره سه – تحویل یکشنبه ۱۳۹۹/۲/۲۶

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ش.د. : ۹۶۲۹۳۷۳

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* در ابتدا توصیه می‌کنم حتماً از **این لینک** دیدن فرمایید.

در این تکلیف قرار است که مدارهای طراحی شده در تکلیف دوم را با استفاده از نرم افزار ISE سنتز کرده و گزارشی از نتایج سنتز ارائه کنید. برای هر یک از طرح ها از تراشه مشخصات زیر به عنوان هدف سنتز استفاده کنید.

Family	Spartan6
Device	XC6SLX16
Package	CSG324
Speed	-3

برنامه مربوط به هر یک از سوالات تکلیف را با استفاده از یک ماژول وریلاگ و بصورت Top-module تعریف نموده و سپس آن را سنتز کنید. نتایج و مشاهدات خود حاصل از فرایند سنتز را که بصورت گزارش کاملی در بخش Design Summary ارائه شده، بصورت یک گزارش کامل توضیح دهید. این اطلاعات شامل کلیه اطلاعات واحدهای استفاده شده از تراشه مربوطه (اعم از تعداد فلیپ فلاپ ها واحدهای LUT و ...)، اطلاعات Timing و فرکانس کلاک و کلیه مواردی است که در گزارش حاصل از سنتز برنامه شما تولید می‌شود. توجه کنید که برای این تکلیف شما تنها گزارشی به صورت PDF ارسال می کنید. در صورتی که کد طراحی شده توسط شما در تکلیف دوم قابل سنتز نبود می توانید آنرا تغییر دهید. در این صورت در گزارش خود کد جدید را درج کنید.

پس در ادامه صرفاً موارد ذیل برای هر سؤال آورده می‌شود :

1. **اطلاعات واحدهای استفاده شده از تراشه (اعم از تعداد FF , LUT و ....)**
2. **اطلاعات Timing**
3. **فرکانس کلاک**
4. **کد (در صورت تغییر نسبت به تکلیف دوم) به همراه با دلیل اصلاح**
5. **تصاویری از مدار RT بعد از سنتز**

* **P Counter** :

** واحدهای استفاده شده از تراشه :

```
=========================================================================
*                            Design Summary                             *
=========================================================================

Top Level Output File Name         : PCounter.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 11
#      GND                         : 1
#      INV                         : 1
#      LUT2                        : 3
#      LUT6                        : 6
# FlipFlops/Latches                : 7
#      FDCE                        : 7
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 10
#      IBUF                        : 2
#      OBUF                        : 8

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:               7  out of  18224     0%
 Number of Slice LUTs:                   10  out of   9112     0%
    Number used as Logic:                10  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     10
   Number with an unused Flip Flop:       3  out of     10    30%
   Number with an unused LUT:             0  out of     10     0%
   Number of fully used LUT-FF pairs:     7  out of     10    70%
   Number of unique control sets:         2

IO Utilization:
 Number of IOs:                          11
 Number of bonded IOBs:                  11  out of    232     4%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     16     6%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------
```

** اطلاعات Timing :

```
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 7     |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.712ns (Maximum Frequency: 368.745MHz)
   Minimum input arrival time before clock: 3.252ns
   Maximum output required time after clock: 3.820ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 2.712ns (frequency: 368.745MHz)
  Total number of paths / destination ports: 43 / 7
-------------------------------------------------------------------------
Delay:               2.712ns (Levels of Logic = 2)
  Source:            cnt_out_2 (FF)
  Destination:       out (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: cnt_out_2 to out
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDCE:C->Q             7   0.447   1.138  cnt_out_2 (cnt_out_2)
     LUT6:I0->O            2   0.203   0.617  cnt_out[6]_GND_1_o_LessThan_3_o_inv_inv11 (cnt_out[6]_GND_1_o_LessThan_3_o_inv_inv)
     LUT2:I1->O            1   0.205   0.000  Mmux_GND_1_o_cnt_out[6]_MUX_15_o11 (GND_1_o_cnt_out[6]_MUX_15_o)
     FDCE:D                    0.102          out
    ----------------------------------------
    Total                      2.712ns (0.957ns logic, 1.755ns route)
                                       (35.3% logic, 64.7% route)

-------------------------------------------------------------------------
```

** اطلاعات Clock :

```
Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    2.712|         |         |         |
---------------+---------+---------+---------+---------+

================================================================================


Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 7.66 secs

-->

Total memory usage is 4510308 kilobytes
```

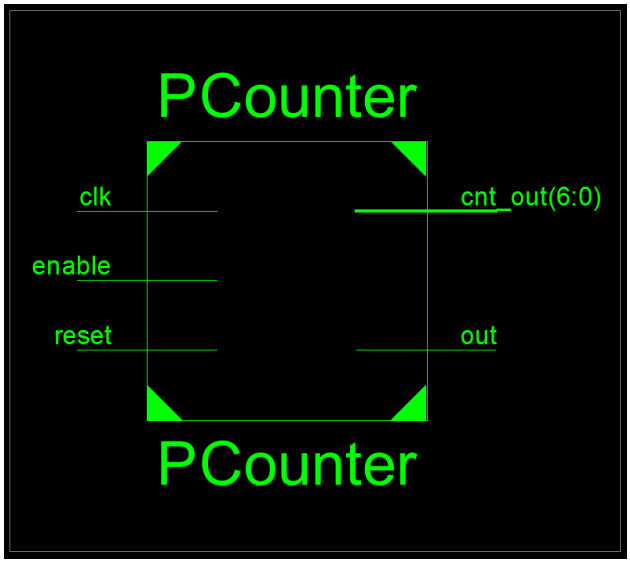
** کد اصلاح شده :

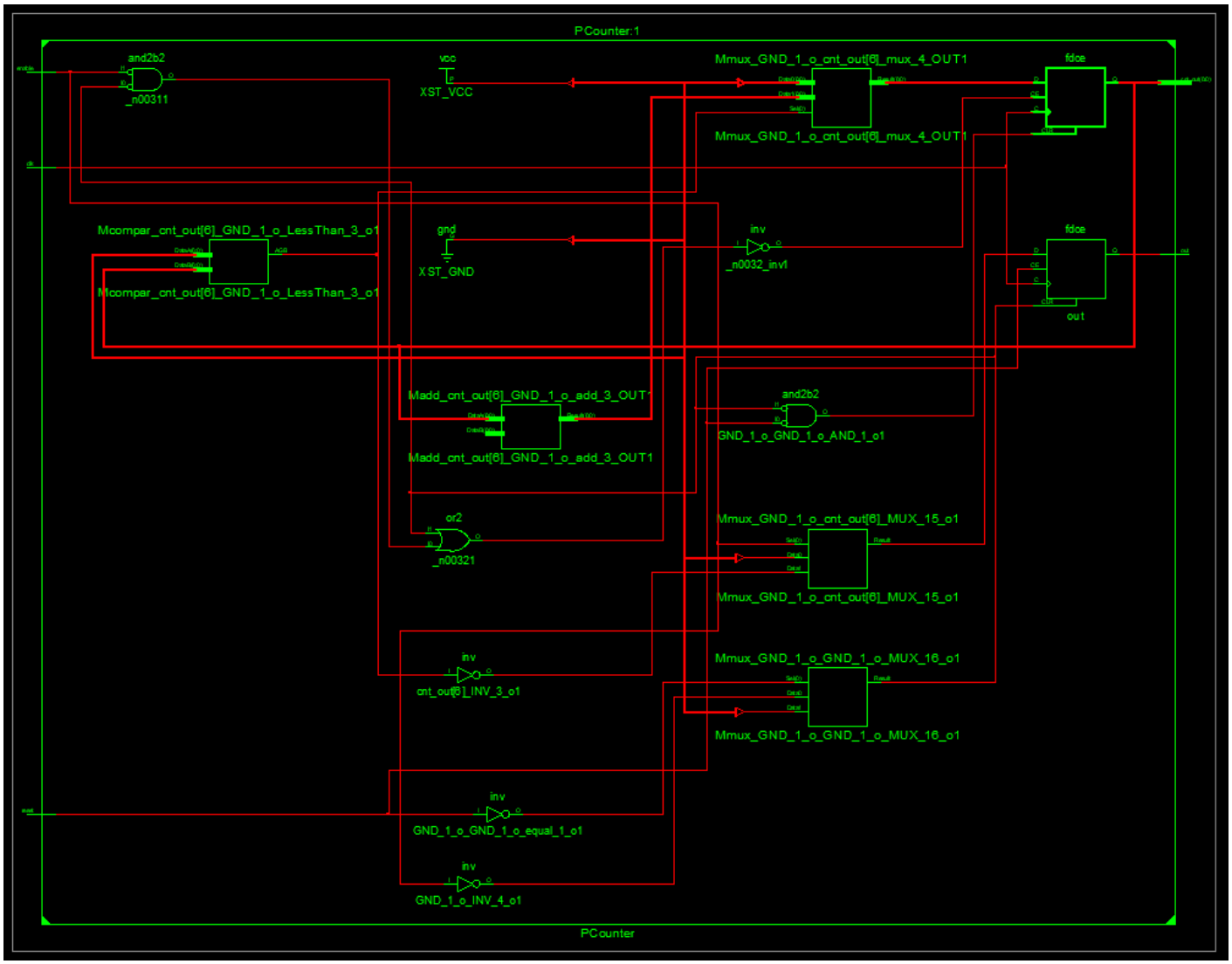
```
`timescale 1ns / 1ps

module PCounter #(parameter MAX_SIZE = 7,parameter [MAX_SIZE-1:0] p = 59) (
        input enable,
        input clk,
        input reset,
        output reg [MAX_SIZE-1:0] cnt_out=0 ,
        output reg out=0
        );

        always @(posedge clk,negedge reset)
        begin : main
                if (reset==0)
                        cnt_out <= 0;
                else
                begin
                        out <= 0;
                        if (enable==1)
                        begin
                                if (cnt_out < p)
                                        cnt_out <= cnt_out + 1;
                                else
                                begin
                                        out <= 1;
                                        cnt_out <= 0;
                                end
                        end
                        else
                                disable main;
                end
        end
endmodule
```

دلیل اصلاح کد

این کد نسبت به کدی که در تکلیف سری دوم آپلود شد ، یک ورودی enable اضافه تر دارد. اضافه کردن این سیگنال ورودی جدید ، به این دلیل است که برای بخش سوم سؤال اول (اضافه کردن سیگنال های stop , start به ماژول) من در کد آپلود شده در تکلیف دوم ، برای هندل کردن این امر ، از Clock Gating استفاده کرده بودم که در جلسه ی حل تمرین روز ۱۶ اردیبهشت متوجه شدم این روش توصیه شده نیست (هرچند که در سنتز کردن و سیمولیشن کد ، اشکالی ایجاد نمی‌کرد !) به همین جهت کد را اصلاح کردم. (به طور خلاصه ، اصلاح کد صرفاً برای بهینه‌تر کردن و درست بودن کد از لحاظ استانداردها است و ربطی به سنتز نشدن آن ندارد)

** تصاویر مدار RT :





* **Day Counter** :

** واحدهای استفاده شده از تراشه :

```
=========================================================================
*                            Design Summary                             *
=========================================================================

Top Level Output File Name         : DayCounter.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 48
#      INV                         : 1
#      LUT2                        : 4
#      LUT3                        : 2
#      LUT4                        : 6
#      LUT5                        : 13
#      LUT6                        : 20
#      MUXF7                       : 2
# FlipFlops/Latches                : 38
#      FDCE                        : 38
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 35
#      IBUF                        : 2
#      OBUF                        : 33

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              38  out of  18224     0%
 Number of Slice LUTs:                   46  out of   9112     0%
    Number used as Logic:                46  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:     46
   Number with an unused Flip Flop:       8  out of     46    17%
   Number with an unused LUT:             0  out of     46     0%
   Number of fully used LUT-FF pairs:    38  out of     46    82%
   Number of unique control sets:        11

IO Utilization:
 Number of IOs:                          36
 Number of bonded IOBs:                  36  out of    232    15%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                1  out of     16     6%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------
```

** اطلاعات Timing :

```
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.


Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
U0/out                             | NONE(U1/cnt_out_5)     | 7     |
clk                                | BUFGP                  | 7     |
U1/out                             | NONE(U2/cnt_out_4)     | 6     |
U2/out                             | NONE(U3/cnt_out_4)     | 6     |
U3/out                             | NONE(U4/cnt_out_3)     | 5     |
U4/out                             | NONE(U5/cnt_out_6)     | 7     |
-----------------------------------+------------------------+-------+
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources.
Please use the buffer_type constraint in order to insert these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.614ns (Maximum Frequency: 382.614MHz)
   Minimum input arrival time before clock: 3.963ns
   Maximum output required time after clock: 3.874ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'U0/out'
  Clock period: 2.414ns (frequency: 414.164MHz)
  Total number of paths / destination ports: 41 / 7
-------------------------------------------------------------------------
Delay:               2.414ns (Levels of Logic = 2)
  Source:            U1/cnt_out_1 (FF)
  Destination:       U1/out (FF)
  Source Clock:      U0/out rising
  Destination Clock: U0/out rising

  Data Path: U1/cnt_out_1 to U1/out
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDCE:C->Q             7   0.447   0.878  U1/cnt_out_1 (U1/cnt_out_1)
     LUT2:I0->O            1   0.203   0.580  U1/Mmux_GND_2_o_cnt_out[5]_MUX_13_o1_SW0 (N2)
     LUT6:I5->O            1   0.205   0.000  U1/Mmux_GND_2_o_cnt_out[5]_MUX_13_o1 (U1/GND_2_o_cnt_out[5]_MUX_13_o)
     FDCE:D                    0.102          U1/out
    ----------------------------------------
    Total                      2.414ns (0.957ns logic, 1.457ns route)
                                       (39.6% logic, 60.4% route)
```

** اطلاعات Clock :

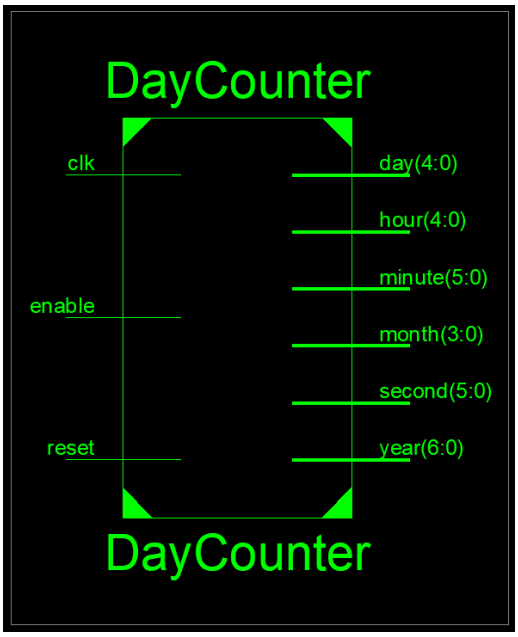
```
Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock U0/out
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
U0/out         |    2.414|         |         |         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock U1/out
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
U1/out         |    1.890|         |         |         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock U2/out
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
U2/out         |    1.890|         |         |         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock U3/out
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
U3/out         |    1.841|         |         |         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock U4/out
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
U4/out         |    2.614|         |         |         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    2.414|         |         |         |
---------------+---------+---------+---------+---------+

=========================================================================


Total REAL time to Xst completion: 5.00 secs
Total CPU time to Xst completion: 5.65 secs

-->

Total memory usage is 4510568 kilobytes
```

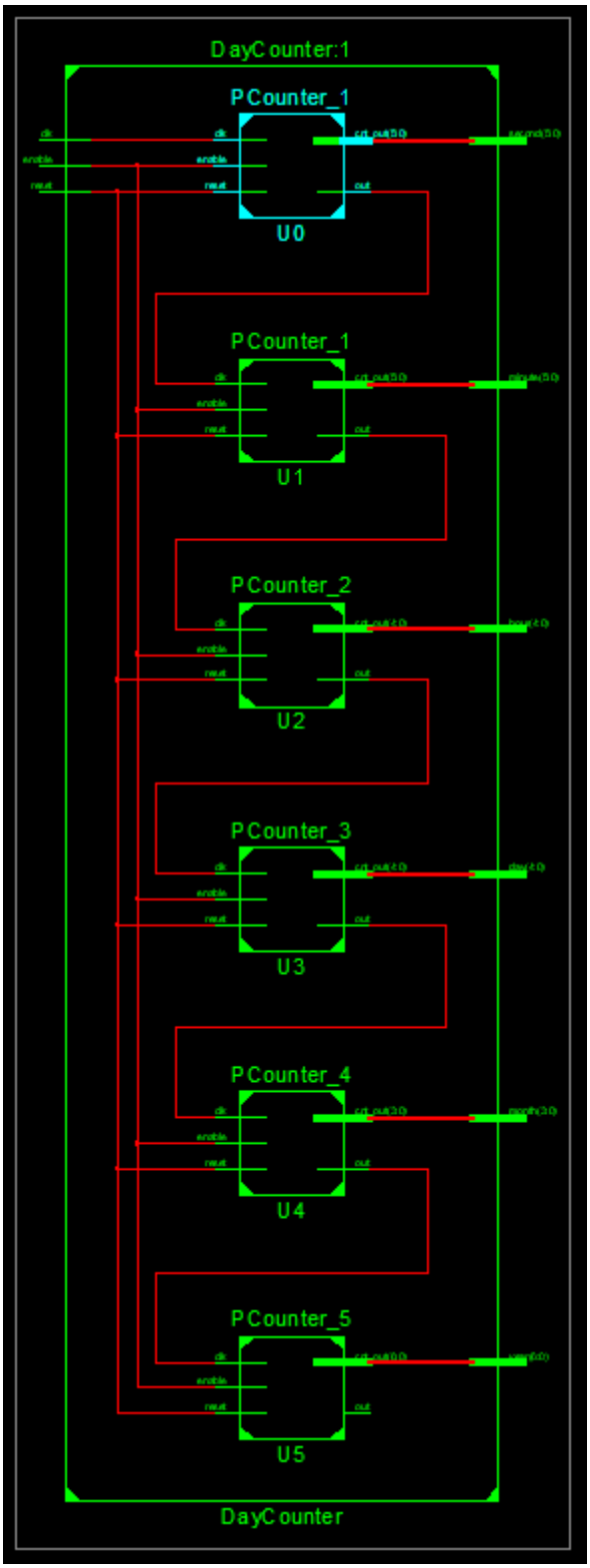
** کد اصلاح شده :

```
`timescale 1ns / 1ps

module DayCounter(
        input enable,
        input clk,
        input reset,
        output [5:0] second,
        output [5:0] minute,
        output [4:0] hour,
        output [4:0] day,
        output [3:0] month,
        output [6:0] year
        );
        // minute and second are maximum 59 => 6 bit
        // hour is maximum 23 and day is maximum 29 => 5 bit
        // month is maximum 11 => 4 bit
        // year is unbounded but e.g. maximum is 99 then it should become a century => 7 bit
        wire year_out,month_out,day_out,hour_out,min_out,sec_out;

        //second
        PCounter #(.MAX_SIZE(6),.p(59)) U0
(.enable(enable),.clk(clk),.cnt_out(second),.out(sec_out),.reset(reset));

        //minute
        PCounter #(.MAX_SIZE(6),.p(59)) U1
(.enable(enable),.clk(sec_out),.cnt_out(minute),.out(min_out),.reset(reset));

        //hour
        PCounter #(.MAX_SIZE(5),.p(23)) U2
(.enable(enable),.clk(min_out),.cnt_out(hour),.out(hour_out),.reset(reset));

        //day
        PCounter #(.MAX_SIZE(5),.p(29)) U3
(.enable(enable),.clk(hour_out),.cnt_out(day),.out(day_out),.reset(reset));

        //month
        PCounter #(.MAX_SIZE(4),.p(11)) U4
(.enable(enable),.clk(day_out),.cnt_out(month),.out(month_out),.reset(reset));

        //year
        PCounter #(.MAX_SIZE(7),.p(99)) U5
(.enable(enable),.clk(month_out),.cnt_out(year),.out(year_out),.reset(reset));

endmodule
```

دلیل اصلاح کد : به دلیل تغییر کد Pcounter ، لازم بود این کد نیز تغییر مختصری کند.

** تصاویر مدار RT :





* **Stopwatch** :

** واحدهای استفاده شده از تراشه :

```
=========================================================================
*                            Design Summary                             *
=========================================================================

Top Level Output File Name         : PCounter.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 11
#      GND                         : 1
#      INV                         : 1
#      LUT2                        : 3
#      LUT6                        : 6
# FlipFlops/Latches                : 7
#      FDCE                        : 7
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 10
#      IBUF                        : 2
#      OBUF                        : 8

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              7  out of  18224     0%
 Number of Slice LUTs:                  10  out of   9112     0%
    Number used as Logic:               10  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    10
   Number with an unused Flip Flop:      3  out of     10    30%
   Number with an unused LUT:            0  out of     10     0%
   Number of fully used LUT-FF pairs:    7  out of     10    70%
   Number of unique control sets:        2

IO Utilization:
 Number of IOs:                         11
 Number of bonded IOBs:                 11  out of    232     4%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     16     6%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------
```

** اطلاعات Timing :

```
==========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 7     |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.712ns (Maximum Frequency: 368.745MHz)
   Minimum input arrival time before clock: 3.252ns
   Maximum output required time after clock: 3.820ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

==========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 2.712ns (frequency: 368.745MHz)
  Total number of paths / destination ports: 43 / 7
--------------------------------------------------------------------------
Delay:               2.712ns (Levels of Logic = 2)
  Source:            cnt_out_2 (FF)
  Destination:       out (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: cnt_out_2 to out
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDCE:C->Q             7   0.447   1.138  cnt_out_2 (cnt_out_2)
     LUT6:I0->O            2   0.203   0.617  cnt_out[6]_GND_1_o_LessThan_3_o_inv_inv11 (cnt_out[6]_GND_1_o_LessThan_3_o_inv_inv)
     LUT2:I1->O            1   0.205   0.000  Mmux_GND_1_o_cnt_out[6]_MUX_15_o11 (GND_1_o_cnt_out[6]_MUX_15_o)
     FDCE:D                    0.102          out
    ----------------------------------------
    Total                      2.712ns (0.957ns logic, 1.755ns route)
                                       (35.3% logic, 64.7% route)
```

** اطلاعات Clock :

```
================================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    2.712|         |         |         |
---------------+---------+---------+---------+---------+

================================================================================


Total REAL time to Xst completion: 6.00 secs
Total CPU time to Xst completion: 5.91 secs

-->

Total memory usage is 4509608 kilobytes
```

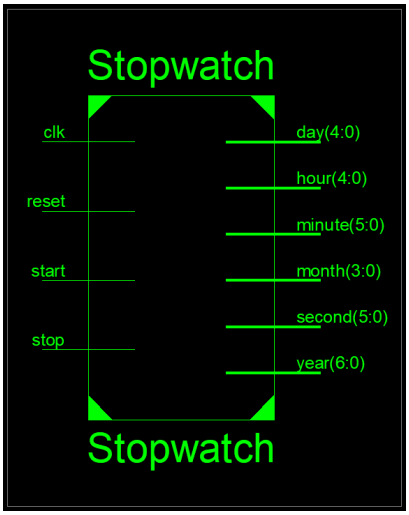
** کد اصلاح شده :

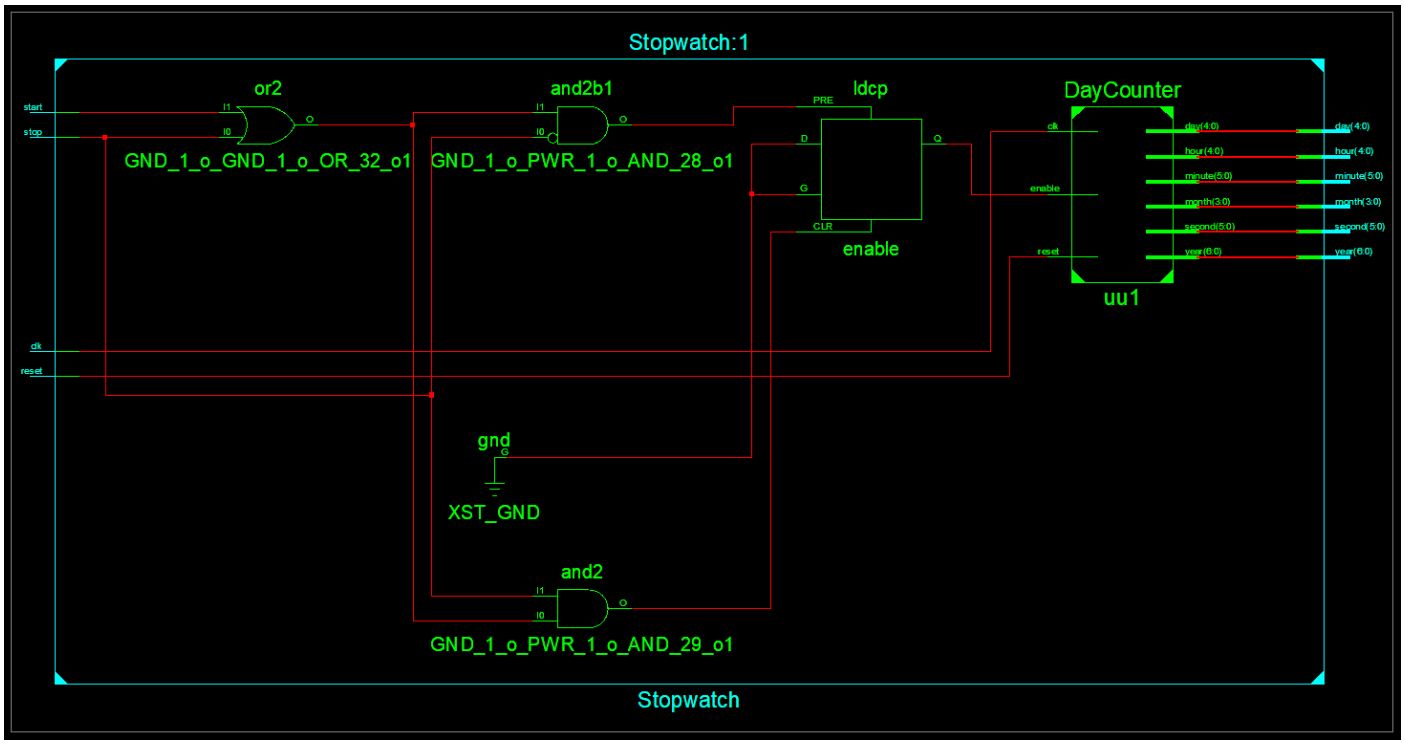
```
`timescale 1ns / 1ps

module Stopwatch(
        input clk,
        input reset,
        input start,
        input stop,
        output [5:0] second,
        output [5:0] minute,
        output [4:0] hour,
        output [4:0] day,
        output[3:0] month,
        output [6:0] year
        );

        reg enable=0;

        DayCounter uu1(
                .enable(enable),
                .clk(clk),
                .reset(reset),
                .second(second),
                .minute(minute),
                .hour(hour),
                .day(day),
                .month(month),
                .year(year)
                );

        always @(posedge start or posedge stop)
        begin

        if(start==1)
                enable <= 1;
        if(stop==1)
                enable <= 0; // stop has a higher priority

        end

endmodule
```

دلیل اصلاح کد :

به دلیل حذف Clock Gating

** تصاویر مدار RT :





* **PWM Generator** :

** واحدهای استفاده شده از تراشه :

```
================================================================================
*                            Design Summary                                    *
================================================================================

Top Level Output File Name         : pwm_generator.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 141
#      GND                         : 1
#      INV                         : 30
#      LUT1                        : 2
#      LUT2                        : 3
#      LUT3                        : 1
#      LUT4                        : 1
#      LUT5                        : 32
#      LUT6                        : 8
#      MUXCY                       : 30
#      VCC                         : 1
#      XORCY                       : 32
# FlipFlops/Latches                : 66
#      FD                          : 2
#      FDE                         : 64
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 19
#      IBUF                        : 18
#      OBUF                        : 1

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              66  out of  18224     0%
 Number of Slice LUTs:                   77  out of   9112     0%
    Number used as Logic:                77  out of   9112     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    109
   Number with an unused Flip Flop:      43  out of    109    39%
   Number with an unused LUT:            32  out of    109    29%
   Number of fully used LUT-FF pairs:    34  out of    109    31%
   Number of unique control sets:         5

IO Utilization:
 Number of IOs:                         20
 Number of bonded IOBs:                 20  out of    232     8%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     16     6%
```

** اطلاعات Timing :

```
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 66    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 3.930ns (Maximum Frequency: 254.430MHz)
   Minimum input arrival time before clock: 3.905ns
   Maximum output required time after clock: 3.597ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 3.930ns (frequency: 254.430MHz)
  Total number of paths / destination ports: 932 / 66
-------------------------------------------------------------------------
Delay:               3.930ns (Levels of Logic = 3)
  Source:            LowCounter_7 (FF)
  Destination:       turn (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: LowCounter_7 to turn
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDE:C->Q              2   0.447   0.981  LowCounter_7 (LowCounter_7)
     LUT6:I0->O            2   0.203   0.981  GND_1_o_GND_1_o_equal_12_o<15>2 (GND_1_o_GND_1_o_equal_12_o<15>1)
     LUT6:I0->O            1   0.203   0.808  _n00571 (_n0057)
     LUT4:I1->O            1   0.205   0.000  turn_rstpot (turn_rstpot)
     FD:D                      0.102          turn
    ----------------------------------------
    Total                      3.930ns (1.160ns logic, 2.770ns route)
                                       (29.5% logic, 70.5% route)
```

** اطلاعات Clock :

```
Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    3.930|         |         |         |
---------------+---------+---------+---------+---------+

================================================================================


Total REAL time to Xst completion: 6.00 secs
Total CPU time to Xst completion: 6.08 secs

-->

Total memory usage is 4509544 kilobytes
```

** کد اصلاح شده :

```
`timescale 1ns / 1ps

module pwm_generator (
	input clk,
	input high_wr,
	input low_wr,
	input [15:0] data_in,
	output reg pwm_out=0
	);

	reg [15:0] Low=0;
	reg [15:0] High=0;
	reg [15:0] HighCounter=0;
	reg [15:0] LowCounter=0;
	reg turn=1'bx;// "turn" decides when pwm_out should be 1 and when 0

	always @(posedge clk)
	begin

	if (high_wr)
	begin
		High <= data_in;
		HighCounter <= data_in;
		turn <= 1;
	end

	if (low_wr)
	begin
		Low <= data_in;
		LowCounter <= data_in;
	end

	if (turn==1)
	begin : up
		pwm_out <= 1;
		if( HighCounter==1 )
		begin
			HighCounter <= High;
			turn <= 0;
			disable up;
		end
		HighCounter <= HighCounter - 1 ;
	end

	if (turn==0)
	begin : down
		pwm_out <= 0;
		if( LowCounter==1 )
		begin
			LowCounter <= Low;
			turn <= 1;
			disable down;
		end
		LowCounter <= LowCounter - 1 ;
	end

	end

endmodule
```

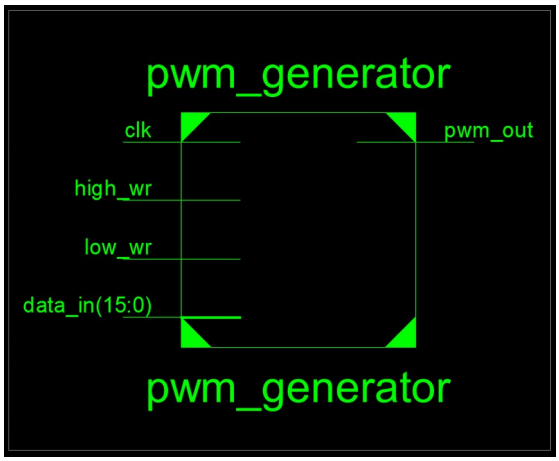
دلیل اصلاح کد :

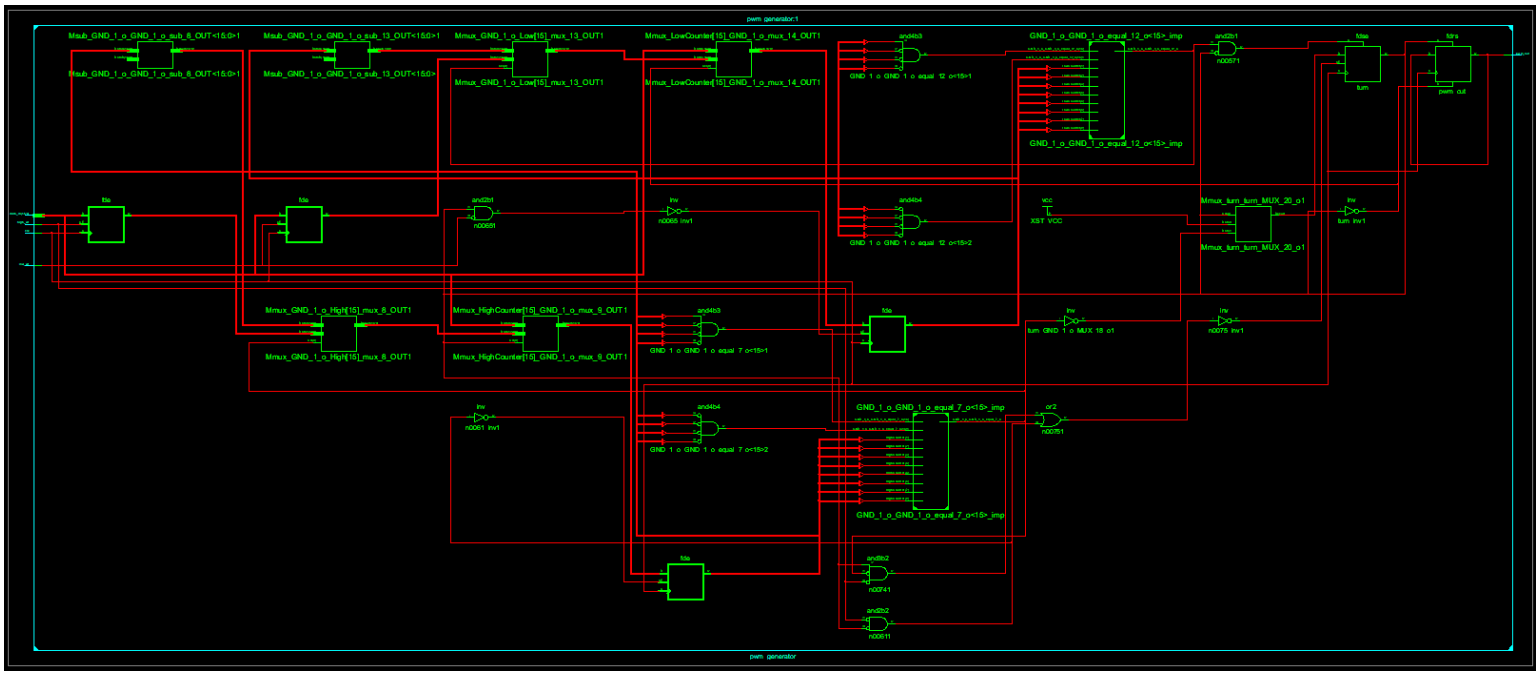
هنگام سنتز کد قبلی (همانی که در تکلیف سری دوم در سامانه آپلود شد) ، اروری مبنی بر

assignment under multiple single edges is not supported for synthesis

دریافت کردم که ظاهراً به دلیل این بود که در چندین بلوک always قصد assign کردن به یک رجیستر خاص را داشتم و در نهایت با گوگل کردن ارور ، متوجه شدم که باید تمام assignment ها به یک رجیستر در یک بلوک always انجام گیرد و در نتیجه تمام سه بلوک always را یکی کردم و بعد از simulation آن از جهت اطمینان از درستی کد جدید ، آن را سنتز کردم و همه چیز اوکی بود .

**** تصاویر مدار RT :**





* **PWM Detector** :

** واحدهای استفاده شده از تراشه :

```
================================================================================
*                            Design Summary                                    *
================================================================================

Top Level Output File Name         : pwm_detector.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 177
#      GND                         : 1
#      INV                         : 4
#      LUT1                        : 30
#      LUT2                        : 3
#      LUT3                        : 16
#      LUT5                        : 34
#      LUT6                        : 14
#      MUXCY                       : 42
#      VCC                         : 1
#      XORCY                       : 32
# FlipFlops/Latches                : 81
#      FD                          : 17
#      FDE                         : 32
#      FDRE                        : 32
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 19
#      IBUF                        : 3
#      OBUFT                       : 16

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              81  out of  18224     0%
 Number of Slice LUTs:                  101  out of   9112     1%
    Number used as Logic:               101  out of   9112     1%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    101
   Number with an unused Flip Flop:      20  out of    101    19%
   Number with an unused LUT:             0  out of    101     0%
   Number of fully used LUT-FF pairs:    81  out of    101    80%
   Number of unique control sets:         5

IO Utilization:
 Number of IOs:                         20
 Number of bonded IOBs:                 20  out of    232     8%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     16     6%
```

** اطلاعات Timing :

```
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 81    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 3.509ns (Maximum Frequency: 284.949MHz)
   Minimum input arrival time before clock: 4.538ns
   Maximum output required time after clock: 4.807ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 3.509ns (frequency: 284.949MHz)
  Total number of paths / destination ports: 1904 / 112
-------------------------------------------------------------------------
Delay:               3.509ns (Levels of Logic = 7)
  Source:            HighCounter_0 (FF)
  Destination:       High_0 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: HighCounter_0 to High_0
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE:C->Q             4   0.447   1.028  HighCounter_0 (HighCounter_0)
     LUT6:I1->O            1   0.203   0.000  Mcompar_High[15]_HighCounter[15]_not_equal_10_o_lut<0> (Mcompar_High[15]_HighCounter[15]_not_equal_10_o_lut<0>)
     MUXCY:S->O            1   0.172   0.000  Mcompar_High[15]_HighCounter[15]_not_equal_10_o_cy<0> (Mcompar_High[15]_HighCounter[15]_not_equal_10_o_cy<0>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_High[15]_HighCounter[15]_not_equal_10_o_cy<1> (Mcompar_High[15]_HighCounter[15]_not_equal_10_o_cy<1>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_High[15]_HighCounter[15]_not_equal_10_o_cy<2> (Mcompar_High[15]_HighCounter[15]_not_equal_10_o_cy<2>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_High[15]_HighCounter[15]_not_equal_10_o_cy<3> (Mcompar_High[15]_HighCounter[15]_not_equal_10_o_cy<3>)
     MUXCY:CI->O           1   0.019   0.000  Mcompar_High[15]_HighCounter[15]_not_equal_10_o_cy<4> (Mcompar_High[15]_HighCounter[15]_not_equal_10_o_cy<4>)
     MUXCY:CI->O          16   0.258   1.004  Mcompar_High[15]_HighCounter[15]_not_equal_10_o_cy<5> (High[15]_HighCounter[15]_not_equal_10_o)
     FDE:CE                    0.322          High_0
    ----------------------------------------
    Total                      3.509ns (1.478ns logic, 2.031ns route)
                               (42.1% logic, 57.9% route)
```

** اطلاعات Clock :

```
Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clk            |    3.509|         |         |         |
---------------+---------+---------+---------+---------+

================================================================================


Total REAL time to Xst completion: 7.00 secs
Total CPU time to Xst completion: 6.12 secs

-->

Total memory usage is 4509480 kilobytes
```

** کد اصلاح شده :

این کد ، بدون اشکال بود و به راحتی نیز سنتز شد .

** تصاویر مدار RT :