



NAND Flash Memory - Fortis Flash

MT29F128G08CBCEB, MT29F256G08CECEB, MT29F512G08CMCEB

Features

- Open NAND Flash Interface (ONFI) 4.0-compliant¹
- JEDEC NAND Flash Interoperability (JESD230C) compliant²
- Multiple-level cell (MLC)
- Organization
 - Page size ×8: 18,592 bytes (16,384 + 2,208 bytes)
 - Block size: MLC: 512 pages, (8192K + 1104K bytes)
 - Plane size: 4 planes × 548 blocks per plane
 - Device size MLC: 128Gb: 2192 blocks; 256Gb: 4384 blocks; 512Gb: 8768 blocks
- NV-DDR2 I/O performance
 - Up to NV-DDR2 timing mode 8
 - Clock rate: 3.75ns (NV-DDR2)
 - Read/write throughput per pin: 533 MT/s
- NV-DDR I/O performance
 - Up to NV-DDR timing mode 5
 - Clock rate: 10ns (NV-DDR)
 - Read/write throughput per pin: 200 MT/s
- Asynchronous I/O performance
 - Up to asynchronous timing mode 5
 - t_{RC}/t_{WC} : 20ns (MIN)
 - Read/write throughput per pin: 50 MT/s
- Array performance
 - SNAP READ operation time: 45 μ s (TYP)³
 - Single-plane READ PAGE operation time: 71 μ s (TYP)³
 - Multi-plane READ PAGE operation time: 75 μ s (TYP)³
 - Effective program page: 750 μ s (TYP)
 - Erase block: 10ms (TYP)
- Operation status byte provides software method for detecting
 - Operation completion
 - Pass/fail condition
 - Write protect status
- Data strobe (DQS) signals provide a hardware method for synchronizing data DQ in the NV-DDR/NV-DDR2 interface
- COPYBACK operations supported within the plane from which data is read

- Advanced command set
 - Read cache sequential
 - Read cache random
 - One-time programmable (OTP) mode
 - Multi-plane commands
 - Multi-LUN operations
 - Read unique ID
 - READ RETRY⁴
 - Copyback
- Command set: ONFI NAND Flash protocol
- First block (block address 00h) is valid when shipped from factory. For minimum required ECC, see Error Management section.
- RESET (FFh) required as first command after power-on
- Quality and reliability⁴
 - Testing methodology: JESD47
 - Data retention: See qualification report - May vary for targeted application
 - Endurance MLC/SLC : 3000/25,000 PROGRAM/ERASE cycles
- Operating voltage range
 - V_{CC} : 2.7–3.6V
 - V_{CCQ} : 1.7–1.95V
- Operating temperature:
 - Industrial: -40°C to +85°C
- Package
 - 132-ball BGA

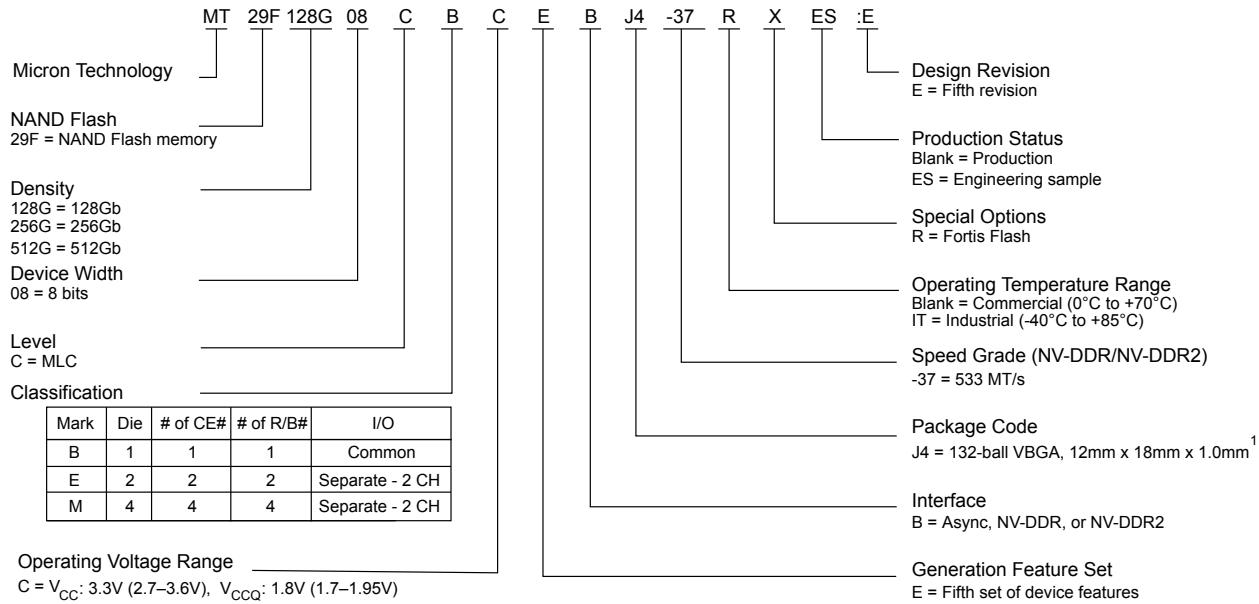
- Notes:
1. The ONFI 4.0 specification is available at www.onfi.org.
 2. The JEDEC specification is available at www.jedec.org/standards-documents.
 3. Contact factory for technical details regarding randomization. Array read times listed are without internal randomization.
 4. READ RETRY operations are required to achieve specified endurance and for general array data integrity.



Part Numbering Information

Micron NAND Flash devices are available in different configurations and densities. Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Numbering



Note: 1. Pb-free package.



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General Description

Micron NAND Flash devices include an asynchronous data interface for I/O operations. These devices use a highly multiplexed 8-bit bus (DQx) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#).

Some versions of this Micron NAND Flash device additionally includes a NV-DDR and/or a NV-DDR2 data interface for high-performance I/O operations. When the NV-DDR interface is active, WE# becomes CLK and RE# becomes W/R#. Data transfers include a bidirectional data strobe (DQS).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). For further details, see Device and Array Organization.

Asynchronous, NV-DDR, NV-DDR2 Signal Descriptions

Table 1: Asynchronous, NV-DDR, and NV-DDR2 Signal Definitions

Signal ¹			Type	Description ²
Asynchronous	NV-DDR	NV-DDR2		
ALE	ALE	ALE	Input	Address latch enable: Loads an address from DQx into the address register.
CE#	CE#	CE#	Input	Chip enable: Enables or disables one or more die (LUNs) in a target.
CLE	CLE	CLE	Input	Command latch enable: Loads a command from DQx into the command register.
DQx	DQx	DQx	I/O	Data inputs/outputs: The bidirectional I/Os transfer address, data, and command information.
–	DQS	DQS, DQS_t	I/O	Data strobe: Provides a synchronous reference for data input and output.
–	–	DQS_c	I/O	Data strobe compliment: Provides a complementary signal to the data strobe signal optionally used in the NV-DDR2 interface for synchronous reference for data input and output.
ENi	ENi	ENi	Input	Enumerate input: Input to a NAND device (if first NAND device on the daisy chain have as NC) from ENo of a previous NAND device to support CE# pin reduction functionality.
ENO	ENO	ENO	Output	Enumerate output: Output from a NAND device to the ENi of the next NAND device in the daisy chain to support CE# pin reduction functionality.



MLC 128Gb to 512Gb Async/Sync NAND Asynchronous, NV-DDR, NV-DDR2 Signal Descriptions

Table 1: Asynchronous, NV-DDR, and NV-DDR2 Signal Definitions (Continued)

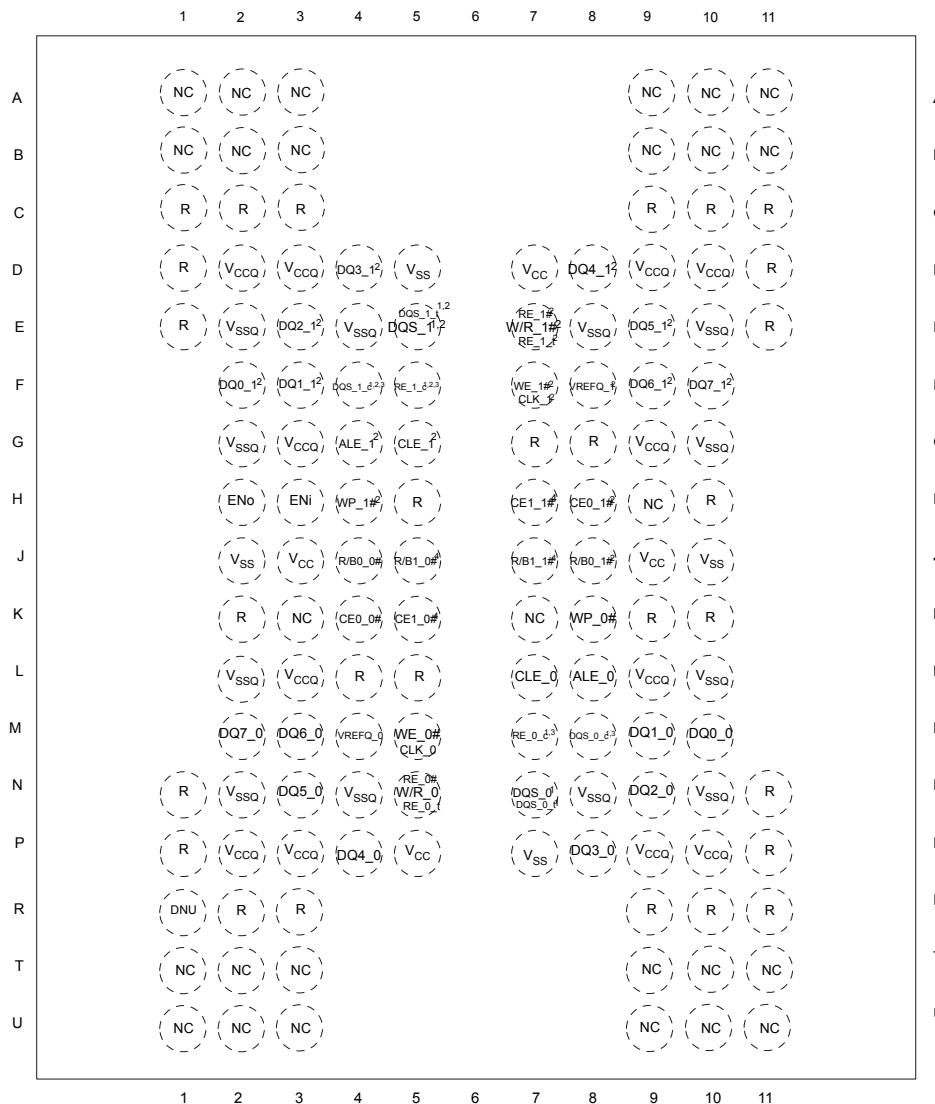
Signal ¹			Type	Description ²
Asynchronous	NV-DDR	NV-DDR2		
RE#	W/R#	RE#, RE_t	Input	Read enable and write/read: RE# transfers serial data from the NAND Flash to the host system when the asynchronous interface is active. When the NV-DDR interface is active, W/R# controls the direction of DQx and DQS.
-	-	RE_c	Input	Read enable complement: Provides a complementary signal to the read enable signal optionally used in the NV-DDR2 interface for synchronous reference for data output.
WE#	CLK	WE#	Input	Write enable and clock: WE# transfers commands, addresses when the asynchronous and NV-DDR2 interfaces are active, and serial data from the host system to the NAND Flash when the asynchronous interface is active. When the NV-DDR interface is active, CLK latches command and address cycles.
WP#	WP#	WP#	Input	Write protect: Enables or disables array PROGRAM and ERASE operations.
R/B#	R/B#	R/B#	Output	Ready/busy: An open-drain, active-low output that requires an external pull-up resistor. This signal indicates target array activity.
V _{CC}	V _{CC}	V _{CC}	Supply	V_{CC}: Core power supply
V _{CCQ}	V _{CCQ}	V _{CCQ}	Supply	V_{CCQ}: I/O power supply
V _{SS}	V _{SS}	V _{SS}	Supply	V_{SS}: Core ground connection
V _{SSQ}	V _{SSQ}	V _{SSQ}	Supply	V_{SSQ}: I/O ground connection
-	-	V _{REFQ}	Supply	V_{REFQ}: Reference voltage used with NV-DDR2 interface
NC	NC	NC	-	No connect: NCs are not internally connected. They can be driven or left unconnected.
DNU	DNU	DNU	-	Do not use: DNUs must be left unconnected.
RFU	RFU	RFU	-	Reserved for future use: RFUs must be left unconnected.

- Notes:
1. See Device and Array Organization for detailed signal connections.
 2. See sections Bus Operation - Asynchronous Interface, Bus Operation - NV-DDR Interface, and Bus Operations - NV-DDR2 Interface for detailed Asynchronous, NV-DDR, and NV-DDR2 interface signal descriptions.



Signal Assignments

Figure 2: 132-Ball BGA (Ball-Down, Top View)

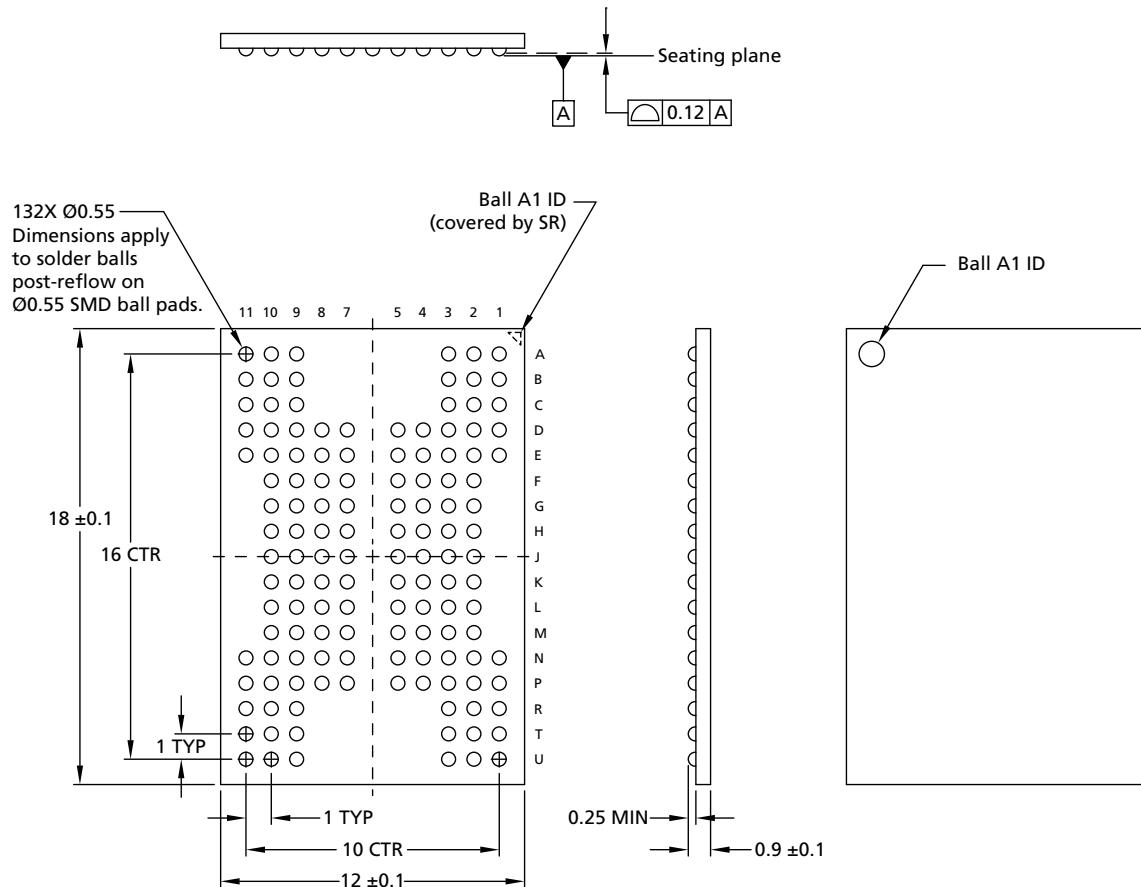


- Notes:
1. N/A: This signal is tri-stated when the asynchronous interface is active.
 2. These signals are available on dual and quad die packages. They are NC for other configurations.
 3. These signals are available when differential signaling is enabled.
 4. These signals are available on quad LUN four CE# stacked packages. They are NC for other configurations.



Package Dimensions

Figure 3: 132-Ball VBGA – 12mm x 18mm x 1.0mm (Package Code: J4)



Notes:

1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).



Architecture

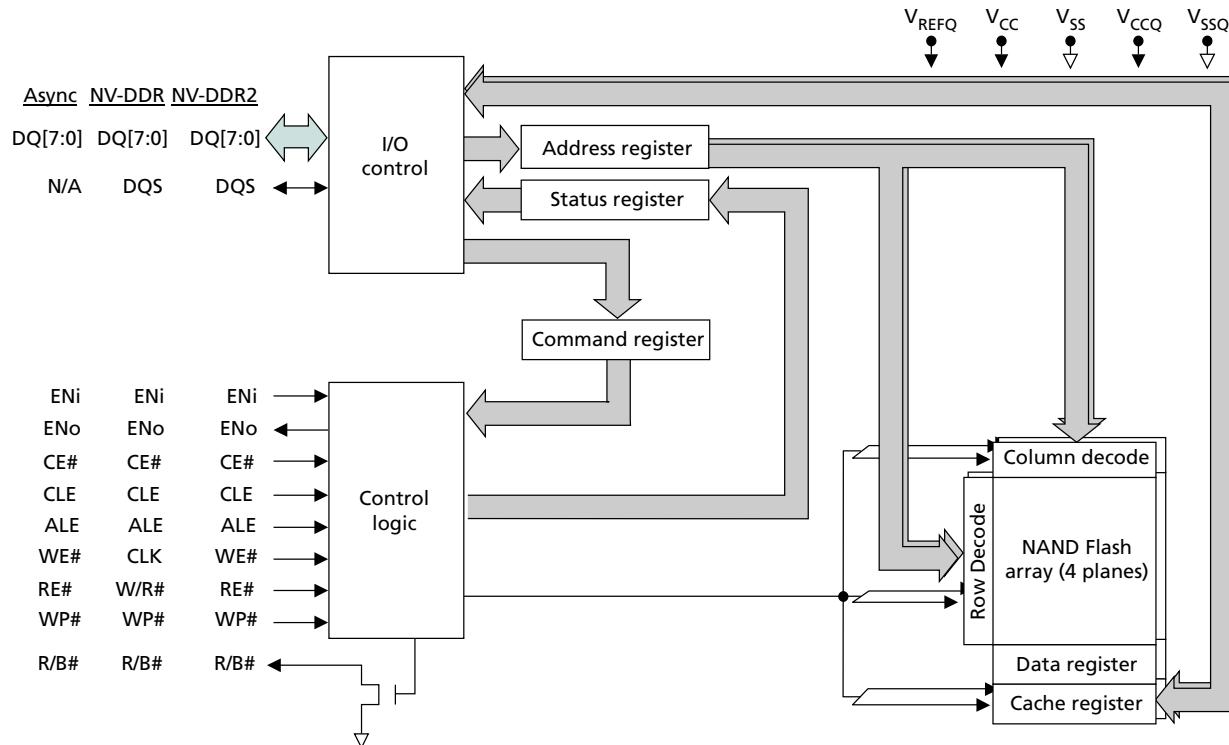
These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address, or to a column decoder to select a column address.

Data is transferred to or from the NAND Flash memory array, byte by byte, through a data register and a cache register.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput.

The status register reports the status of die (LUN) operations.

Figure 4: NAND Flash Die (LUN) Functional Block Diagram



- Notes:
1. N/A: This signal is tri-stated when the asynchronous interface is active.
 2. Some devices do not include the NV-DDR or NV-DDR2 interface.
 3. Some devices do not include the **V_{REFQ}** signal.



Device and Array Organization

Figure 5: Device Organization for Single-Die Package

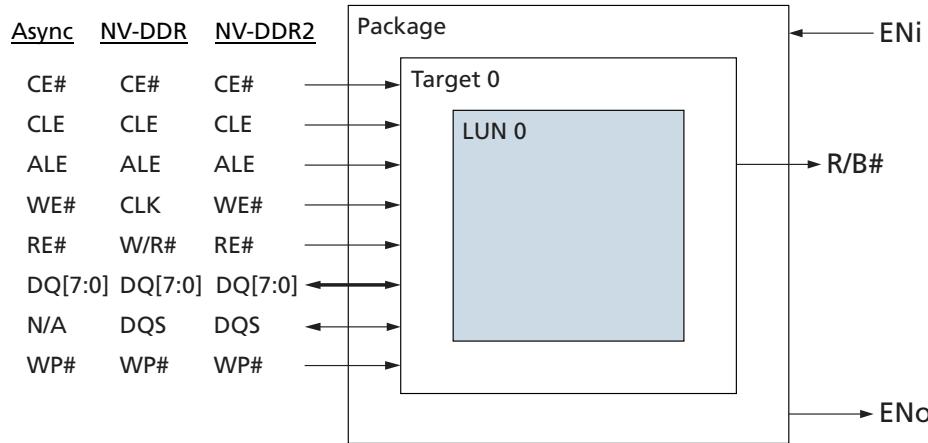


Figure 6: Device Organization for Two-Die Package (132-ball BGA)

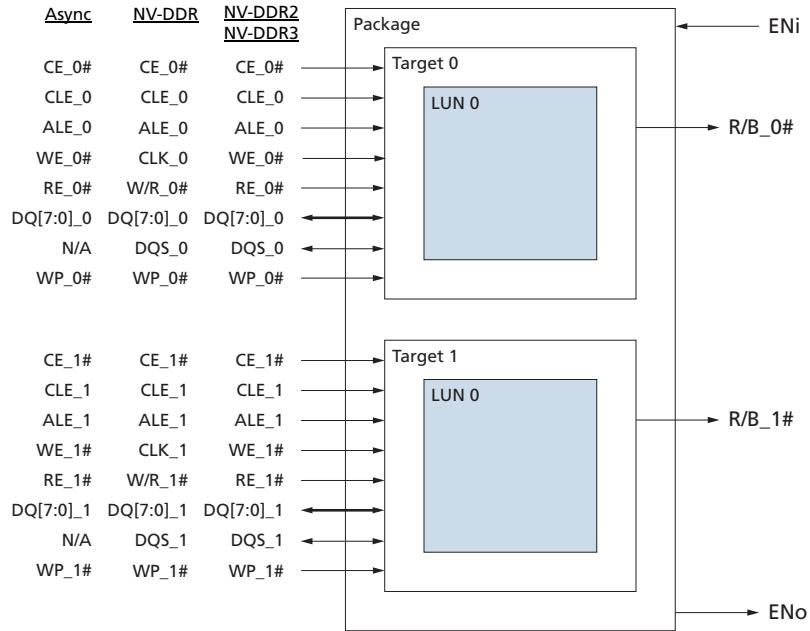


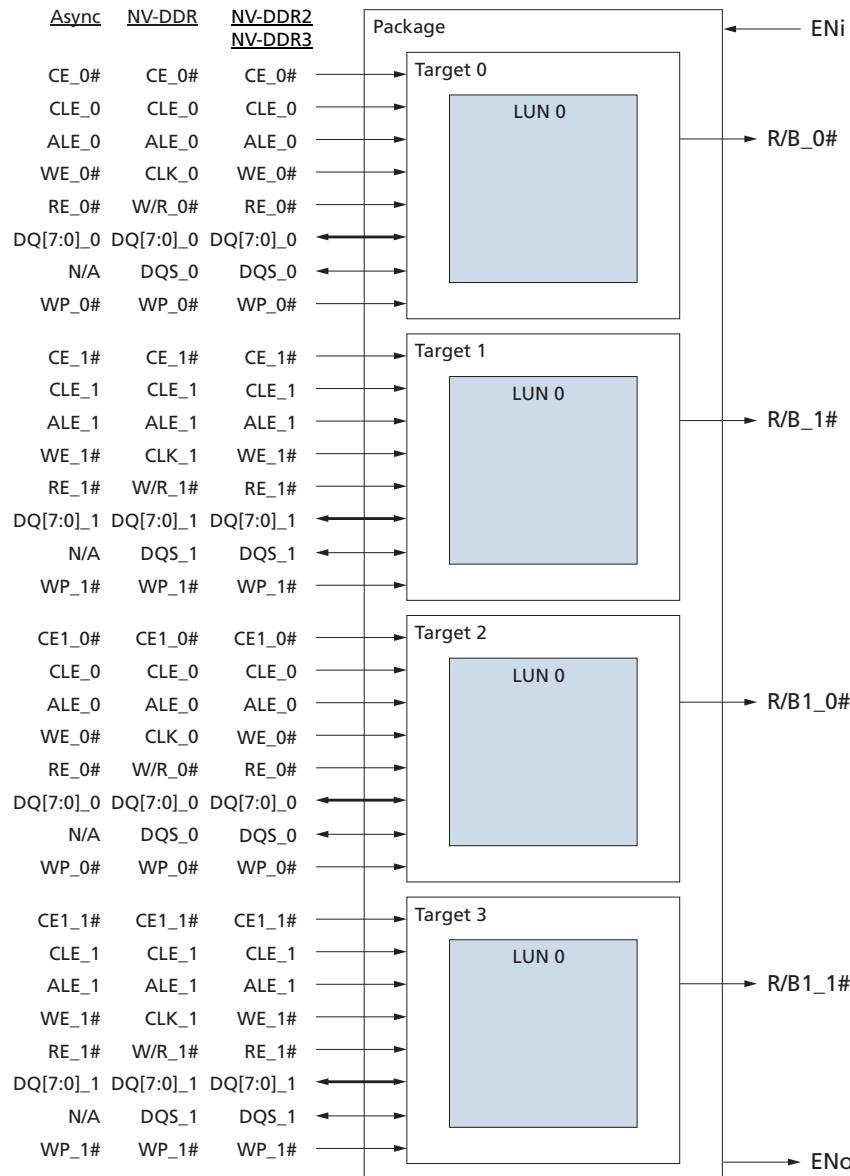
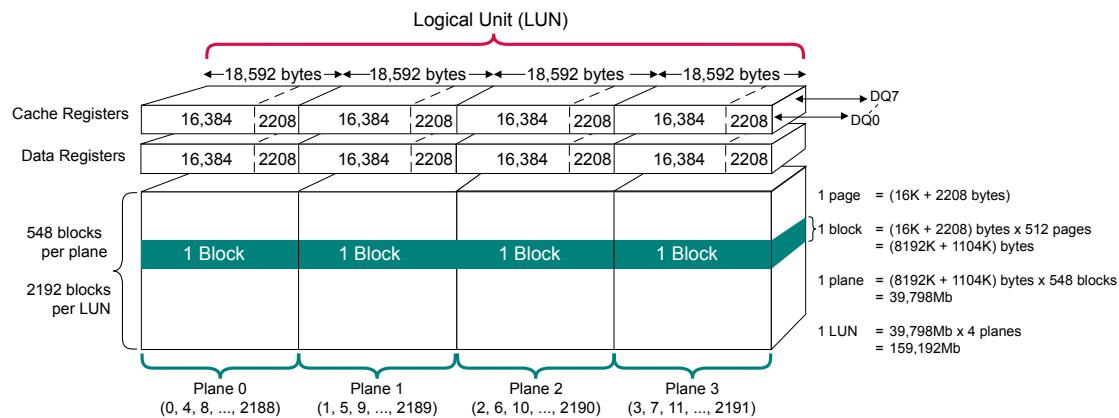
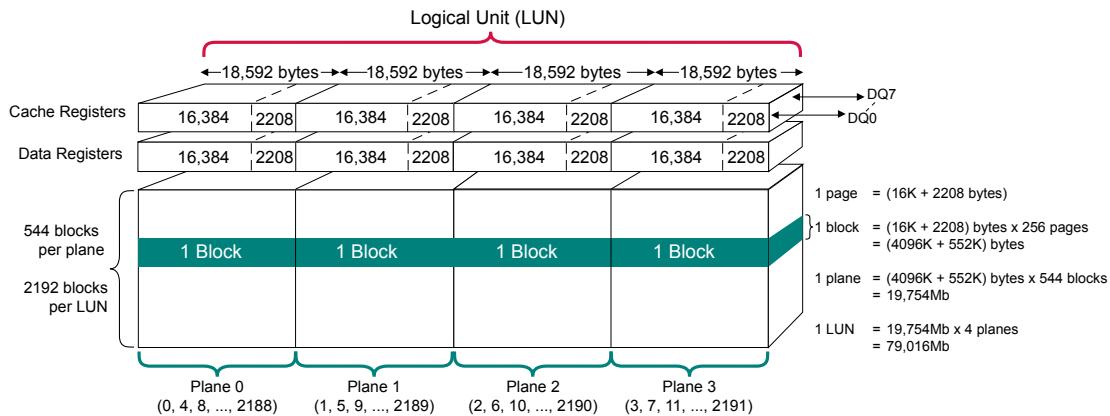

Figure 7: Device Organization for Four-Die Package with four CE# (132-ball BGA)



Figure 8: Array Organization per Logical Unit (LUN) – MLC Mode


**Table 2: Array Addressing for Logical Unit (LUN) – MLC Mode**

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0 ²
Second	LOW	CA14 ³	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10 ⁴	BA9 ⁴	BA8
Fifth	LOW	LOW	LA0 ^{5, 6}	BA20	BA19	BA18	BA17	BA16

- Notes:
1. CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.
 2. When using the NV-DDR/NV-DDR2 interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
 3. Column addresses 18,592 (48A0h) through 32,767 (7FFFh) are invalid and out of bounds; these addresses cannot be addressed because they do not exist in the device.
 4. BA[10:9] are the plane-select bits:
 Plane 0: BA[10:9] = 00
 Plane 1: BA[10:9] = 01
 Plane 2: BA[10:9] = 10
 Plane 3: BA[10:9] = 11
 5. LA0 is the LUN-select bit. It is present only when two LUNs are shared on the target; otherwise, it should be held LOW.
 LUN 0: LA0 = 0
 LUN 1: LA0 = 1
 6. For single LUN targets block addresses, 2192 through 4095 are invalid and out of bounds; these addresses cannot be addressed because they do not exist in the device. For dual LUN targets, block addresses 2192 through 4095 and 6288 through 8191 are invalid and out of bounds; these addresses cannot be addressed because they do not exist in the device.

**Figure 9: Array Organization per Logical Unit (LUN) – SLC Mode****Table 3: Array Addressing for Logical Unit (LUN) in SLC Mode – Non-Squashed Addressing**

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0 ²
Second	LOW	CA14 ³	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA14	BA13	BA12	BA11	BA10	BA9 ⁴	BA8 ⁴	LOW
Fifth	LOW	LOW	LA0 ^{5, 6}	BA19	BA18	BA17	BA16	BA15

- Notes:
1. CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.
 2. When using the NV-DDR/NV-DDR2 interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
 3. Column addresses 18,592 (48A0h) through 32,767 (7FFFh) are invalid and out of bounds; these addresses cannot be addressed because they do not exist in the device.
 4. BA[10:9] are the plane-select bits:
 Plane 0: BA[10:9] = 00
 Plane 1: BA[10:9] = 01
 Plane 2: BA[10:9] = 10
 Plane 3: BA[10:9] = 11
 5. LA0 is the LUN-select bit. It is present only when two LUNs are shared on the target; otherwise, it should be held LOW.
 LUN 0: LA0 = 0
 LUN 1: LA0 = 1
 6. For single LUN targets, block addresses 2192 through 4095 are invalid and out of bounds; these addresses cannot be addressed because they do not exist in the device. For dual LUN targets, block addresses 2192 through 4095 and 6288 through 8191 are invalid and out of bounds; these addresses cannot be addressed because they do not exist in the device.



Bus Operation – Asynchronous Interface

The asynchronous interface is active when the NAND Flash device powers on. The I/O bus, DQ[7:0], is multiplexed sharing data I/O, addresses, and commands. The DQS signal, if present, is tri-stated when the asynchronous interface is active.

Asynchronous interface bus modes are summarized below.

Table 4: Asynchronous Interface Mode Selection

Mode	CE#	CLE	ALE	WE#	RE#	DQS	DQx	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V _{CCQ} ²	2
Bus idle	L	X	X	H	H	X	X	X	
Command input	L	H	L		H	X	input	H	
Address input	L	L	H		H	X	input	H	
Data input	L	L	L		H	X	input	H	
Data output	L	L	L	H		X	output	X	
Write protect	X	X	X	X	X	X	X	L	

- Notes:
1. DQS is tri-stated when the asynchronous interface is active.
 2. WP# should be biased to CMOS LOW or HIGH for standby.
 3. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

Asynchronous Enable/Standy

A chip enable (CE#) signal is used to enable or disable a target. When CE# is driven LOW, all of the signals for that target are enabled. With CE# LOW, the target can accept commands, addresses, and data I/O. There may be more than one target in a NAND Flash package. Each target is controlled by its own chip enable; the first target (Target 0) is controlled by CE#; the second target (if present) is controlled by CE2#, and so forth.

A target is disabled when CE# is driven HIGH, even when the target is busy. When disabled, all of the target's signals are disabled except CE#, WP#, and R/B#. This functionality is also known as CE# "Don't Care." While the target is disabled, other devices can utilize the disabled NAND signals that are shared with the NAND Flash.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations. Standby helps reduce power consumption.

Asynchronous Bus Idle

A target's bus is idle when CE# is LOW, WE# is HIGH, and RE# is HIGH.

During bus idle, all of the signals are enabled except DQS, which is not used when the asynchronous interface is active. No commands, addresses, and data are latched into the target; no data is output.



Asynchronous Pausing Data Input/Output

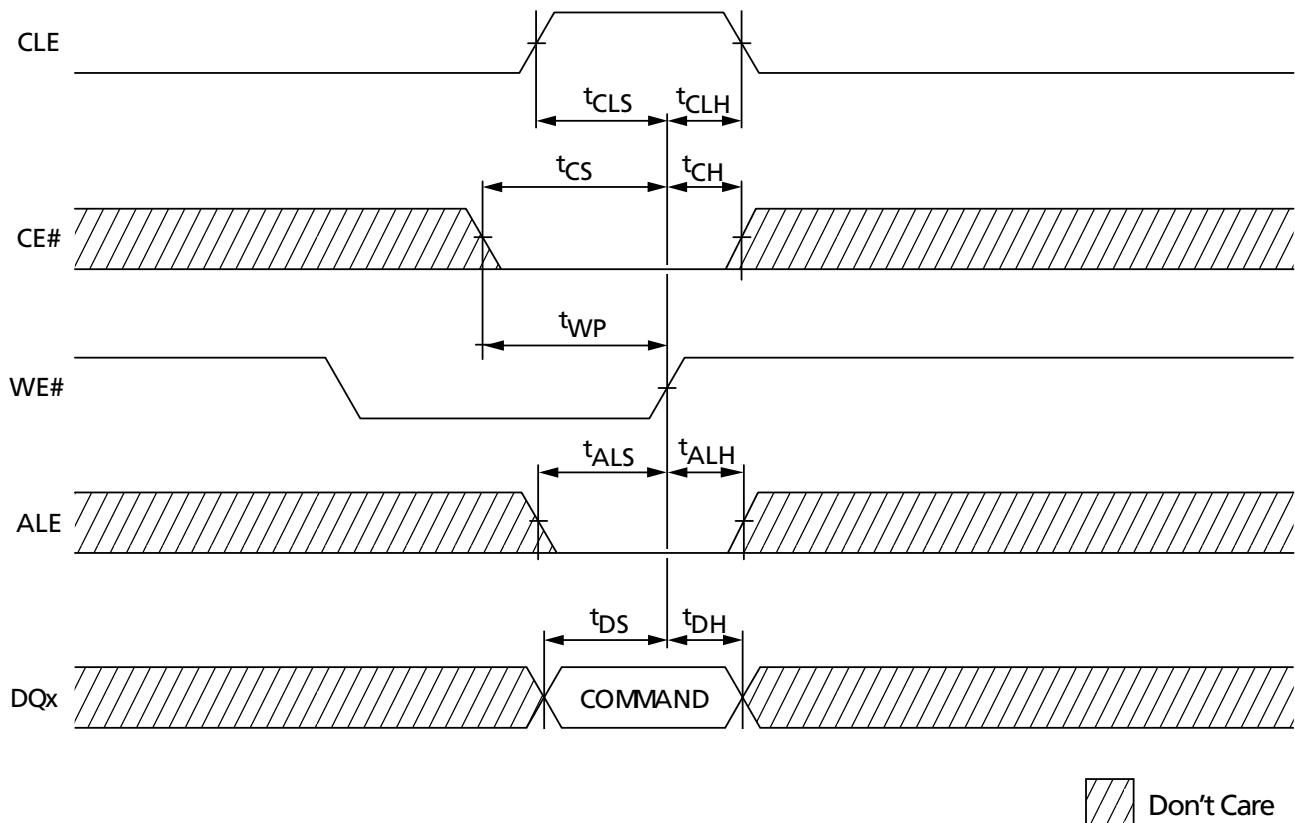
Pausing data input or data output is done by keeping WE# or RE# HIGH, respectively.

Asynchronous Commands

An asynchronous command is written from DQ[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, including READ STATUS (70h), READ STATUS ENHANCED (78h), and FIXED ADDRESS READ STATUS ENHANCED (71h) are accepted by die (LUNs) even when they are busy.

Figure 10: Asynchronous Command Latch Cycle



Asynchronous Addresses

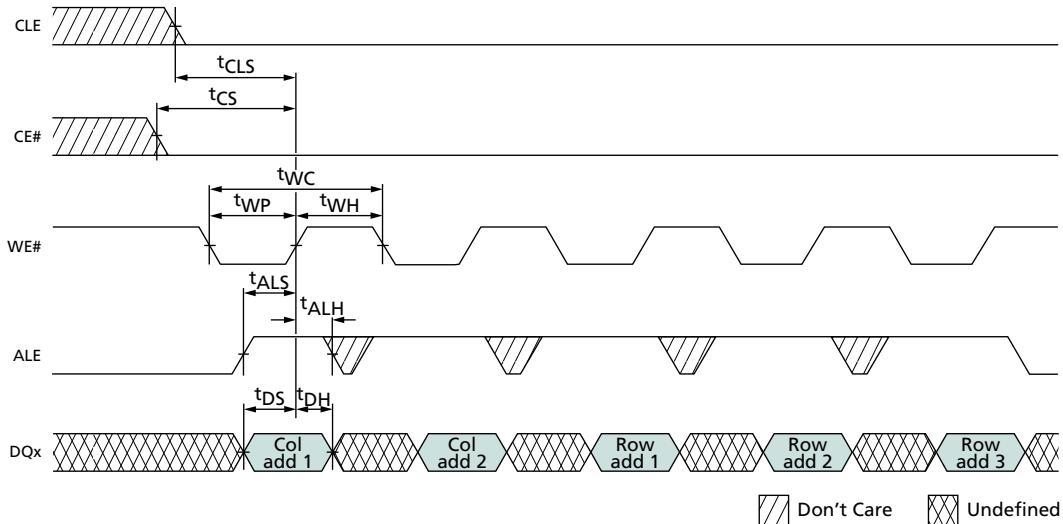
An asynchronous address is written from DQ[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits that are not part of the address space must be LOW (see Device and Array Organization). The number of cycles required for each command varies. Refer to the command descriptions to determine addressing requirements (see Command Definitions).



Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses are accepted by die (LUNs) even when they are busy; for example, address cycles that follow the READ STATUS ENHANCED (78h) command.

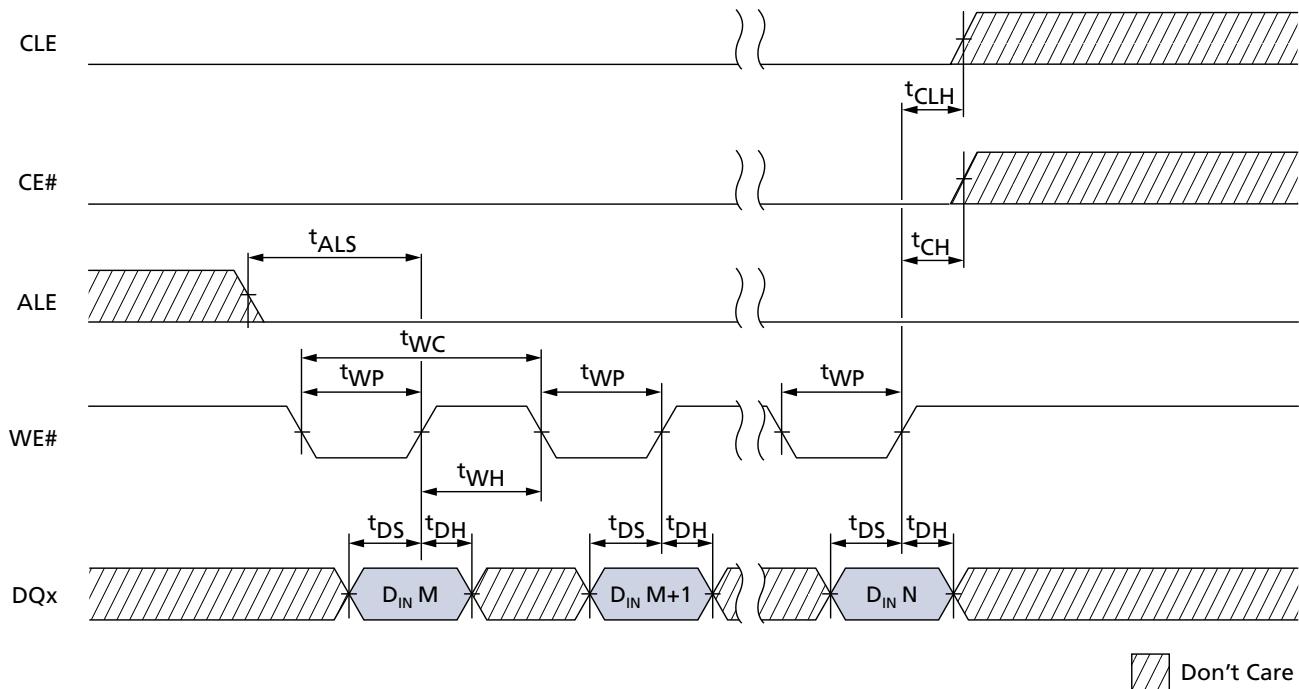
Figure 11: Asynchronous Address Latch Cycle



Asynchronous Data Input

Data is written from DQ[7:0] to the cache register of the selected die (LUN) on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is LOW, and RE# is HIGH.

Data input is ignored by die (LUNs) that are not selected or are busy (RDY = 0).

**Figure 12: Asynchronous Data Input Cycles**

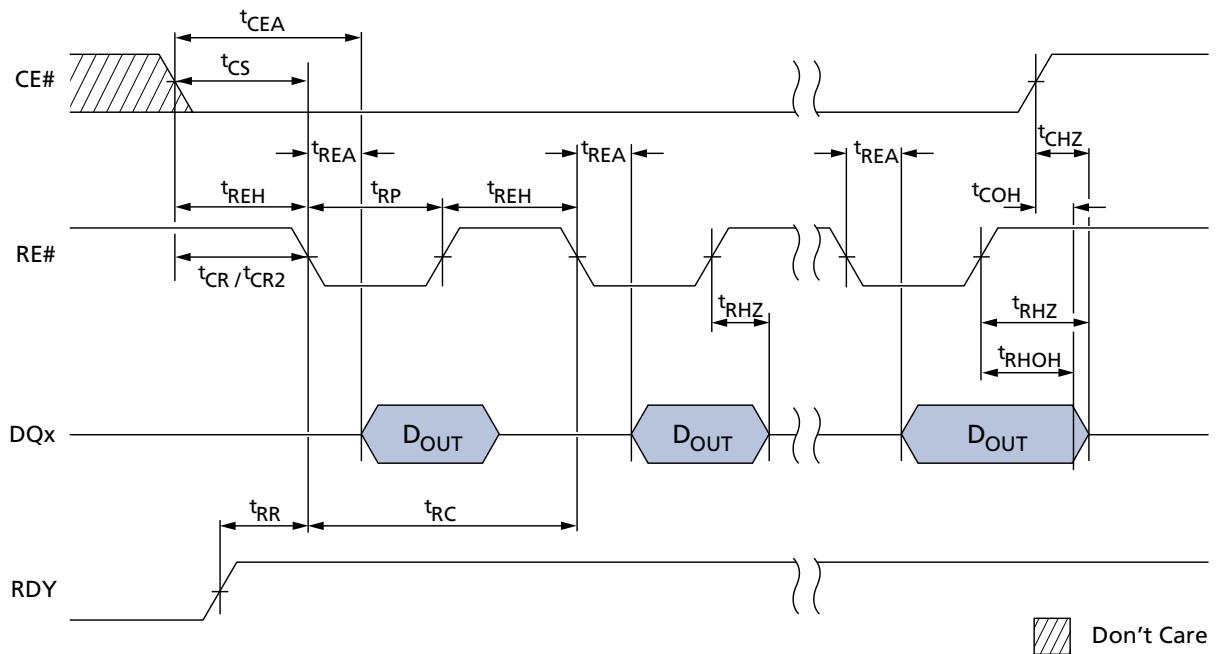
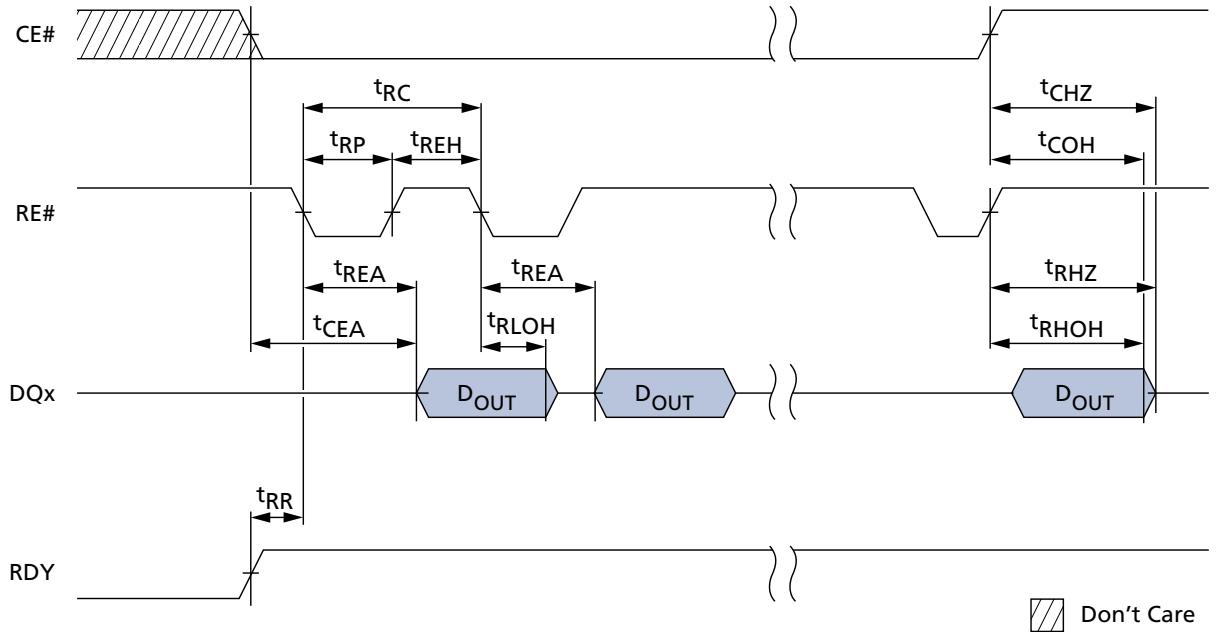
Asynchronous Data Output

Data can be output from a die (LUN) if it is in a ready state. Data output is supported following a READ operation from the NAND Flash array. Data is output from the cache register of the selected die (LUN) to DQ[7:0] on the falling edge of RE# when CE# is LOW, ALE is LOW, CLE is LOW, and WE# is HIGH.

If the host controller is using a t_{RC} of 30ns or greater, the host can latch the data on the rising edge of RE# (see Figure 13 for proper timing). If the host controller is using a t_{RC} of less than 30ns, the host can latch the data on the next falling edge of RE# (see Figure 14 (page 27) for extended data output (EDO) timing).

Using the READ STATUS ENHANCED (78h) or the FIXED ADDRESS READ STATUS ENHANCED (71h) command prevents data contention following an interleaved die (multi-LUN) operation. After issuing the READ STATUS ENHANCED (78h) command, to enable data output, issue the READ MODE (00h) command.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by first issuing the READ STATUS (70h), READ STATUS ENHANCED (78h), or FIXED ADDRESS READ STATUS ENHANCED (71h) command.

**Figure 13: Asynchronous Data Output Cycles****Figure 14: Asynchronous Data Output Cycles (EDO Mode)**

Write Protect

The write protect (WP#) signal enables or disables PROGRAM and ERASE operations to a target. When WP# is LOW, PROGRAM and ERASE operations are disabled. When WP# is HIGH, PROGRAM and ERASE operations are enabled.



It is recommended that the host drive WP# LOW during power-on until V_{CC} and V_{CCQ} are stable to prevent inadvertent PROGRAM and ERASE operations (see Device Initialization (page 44) for additional details).

WP# must be transitioned only when the target is not busy and prior to beginning a command sequence. After a command sequence is complete and the target is ready, WP# can be transitioned. After WP# is transitioned, the host must wait t_{WW} before issuing a new command.

The WP# signal is always an active input, even when CE# is HIGH. This signal should not be multiplexed with other signals.

Ready/Busy#

The ready/busy# (R/B#) signal provides a hardware method of indicating whether a target is ready or busy. A target is busy when one or more of its die (LUNs) are busy (RDY = 0). A target is ready when all of its die (LUNs) are ready (RDY = 1). Because each die (LUN) contains a status register, it is possible to determine the independent status of each die (LUN) by polling its status register instead of using the R/B# signal (see Status Operations (page 105) for details regarding die (LUN) status).

This signal requires a pull-up resistor, R_P, for proper operation. R/B# is HIGH when the target is ready, and transitions LOW when the target is busy. The signal's open-drain driver enables multiple R/B# outputs to be OR-tied. Typically, R/B# is connected to an interrupt pin on the system controller (see Figure 15 (page 29)).

It is not permitted to drive or have the NAND R/B# signal HIGH while the NAND V_{CCQ} voltage is below V_{CCQ,min}.

The combination of R_P and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for R_P depends on the system timing requirements. Large values of R_P cause R/B# to be delayed significantly. Between the 10- to 90-percent points on the R/B# waveform, the rise time is approximately two time constants (TC).

$$TC = R \times C$$

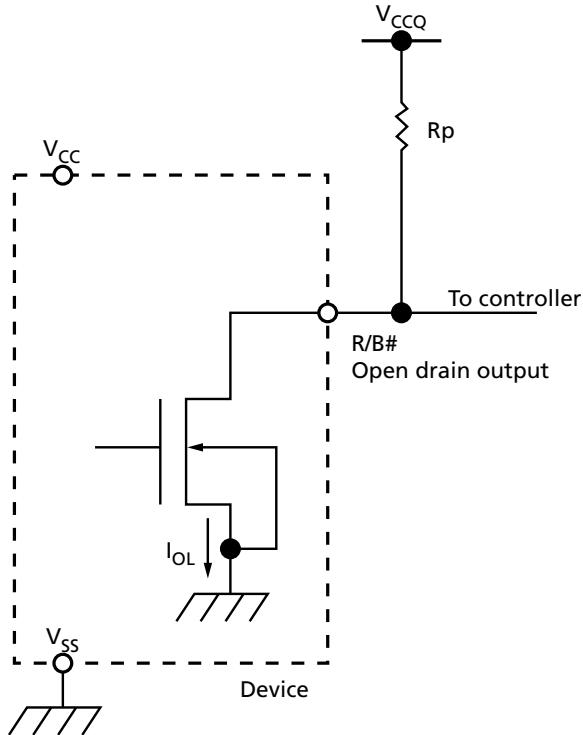
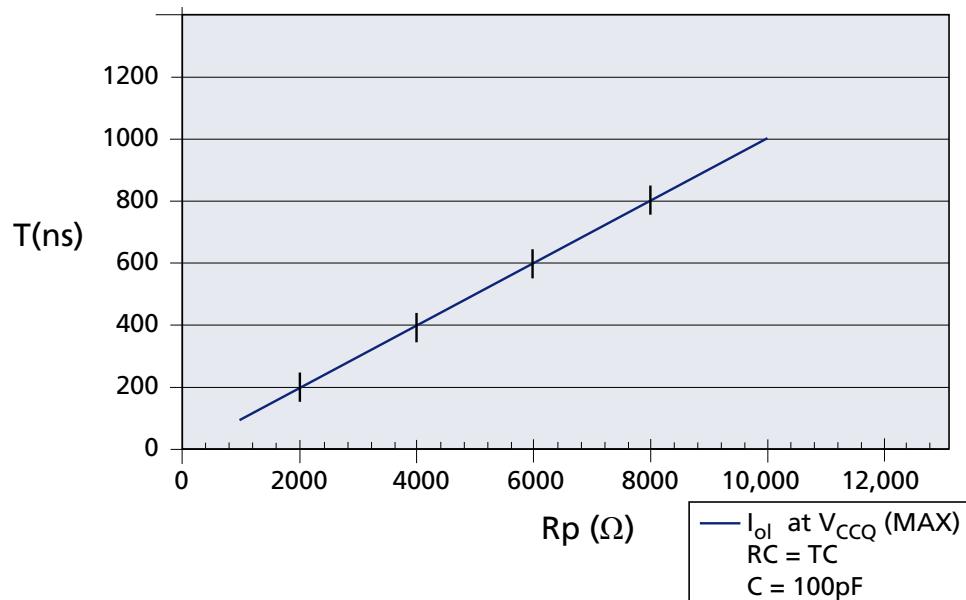
Where R = R_P (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# signal and the total load capacitance. Approximate R_P values using a circuit load of 100pF are provided in Figure 16 (page 29).

The minimum value for R_P is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CCQ}.

$$R_P = \frac{V_{CCQ}(\text{MAX}) - V_{OL}(\text{MAX})}{I_{OL} + \sum I_{IL}}$$

Where $\sum I_{IL}$ is the sum of the input currents of all devices tied to the R/B# pin.

**Figure 15: READ/BUSY# Open Drain****Figure 16: TC vs R_p** 



Bus Operation – NV-DDR Interface

The NAND Flash command protocol for both the asynchronous and NV-DDR interfaces is identical. However, there are some differences between the asynchronous and NV-DDR interfaces when issuing command, address, and data I/O cycles using the NAND Flash signals.

When the NV-DDR interface is activated on a target (see Activating Interfaces), the target is capable of high-speed NV-DDR data transfers. Existing signals are redefined for high-speed NV-DDR I/O. The WE# signal becomes CLK. DQS is enabled. The RE# signal becomes W/R#. CLK provides a clock reference to the NAND Flash device.

DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

The direction of DQS and DQ[7:0] is controlled by the W/R# signal. When the W/R# signal is latched HIGH, the controller is driving the DQ bus and DQS. When the W/R# is latched LOW, the NAND Flash is driving the DQ bus and DQS.

Transition from the NV-DDR interface to the NV-DDR2 interface is not permitted.

The NV-DDR interface bus modes are summarized below.

Table 5: NV-DDR Interface Mode Selection

Mode	CE#	CLE	ALE	CLK	W/R#	DQS	DQ[7:0]	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V _{CCQ}	1, 2
Bus idle	L	L	L		H	X	X	X	
Bus driving	L	L	L		L	output	output	X	
Command input	L	H	L		H	X	input	H	3
Address input	L	L	H		H	X	input	H	3
Data input	L	H	H		H		input	H	4
Data output	L	H	H		L	See Note 5	output	X	5
Write protect	X	X	X	X	X	X	X	L	
Undefined	L	L	H		L	output	output	X	
Undefined	L	H	L		L	output	output	X	

- Notes:
1. CLK can be stopped when the target is disabled, even when R/B# is LOW.
 2. WP# should be biased to CMOS LOW or HIGH for standby.
 3. Commands and addresses are latched on the rising edge of CLK.
 4. During data input to the device, DQS is the “clock” that latches the data in the cache register.



5. During data output from the NAND Flash device, DQS is an output generated from CLK after t_{DQSCK} delay.
6. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL} .

NV-DDR Enable/Standy

In addition to the description found in Asynchronous Enable/Standy, the following requirements also apply when the NV-DDR interface is active.

Before enabling a target, CLK must be running and ALE and CLE must be LOW. When CE# is driven LOW, all of the signals for the selected target are enabled. The target is not enabled until t_{CS} completes; the target's bus is then idle.

Prior to disabling a target, the target's bus must be idle. A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#. After the target is disabled, CLK can be stopped.

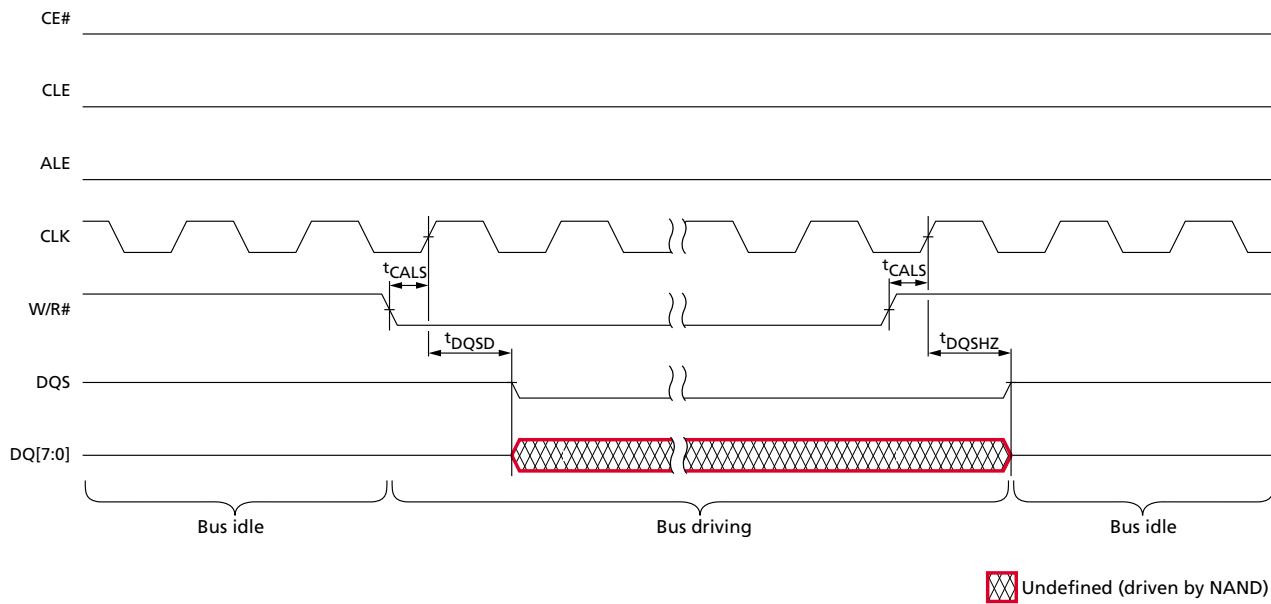
A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations.

NV-DDR Bus Idle/Driving

A target's bus is idle or driving when CLK is running, CE# is LOW, ALE is LOW, and CLE is LOW.

The bus is idle when W/R# transitions HIGH and is latched by CLK. During the bus idle mode, all signals are enabled; DQS and DQ[7:0] are inputs. No commands, addresses, or data are latched into the target; no data is output. When entering the bus idle mode, the host must wait a minimum of t_{CAD} before changing the bus mode. In the bus idle mode, the only valid bus modes supported are: bus driving, command, address, and NV-DDR data input.

The bus is driving when W/R# transitions LOW and is latched by CLK. During the bus driving mode, all signals are enabled; DQS is LOW and DQ[7:0] is driven LOW or HIGH, but no valid data is output. Following the bus driving mode, the only valid bus modes supported are bus idle and NV-DDR data output.

**Figure 17: NV-DDR Bus Idle/Driving Behavior**

Undefined (driven by NAND)

Note: 1. Only the selected die (LUN) drives DQS and DQ[7:0]. During an interleaved die (multi-LUN) operation, the host must use the READ STATUS ENHANCED (78h) to prevent data output contention.

NV-DDR Pausing Data Input/Output

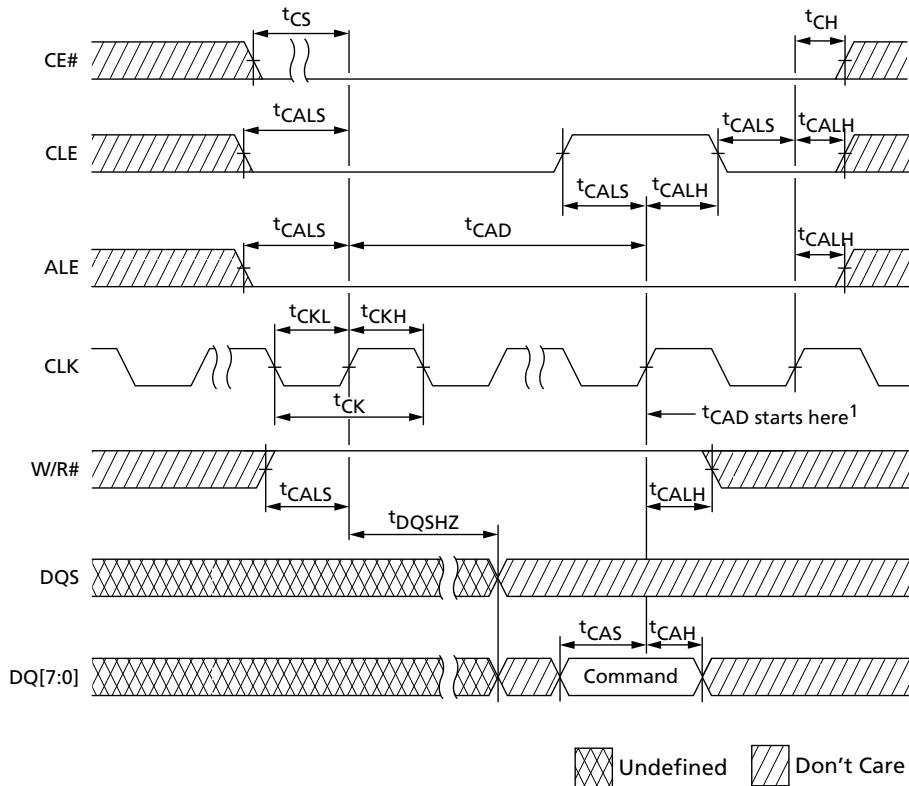
Pausing data input or data output is done by setting ALE and CLE to LOW. The host may continue data transfer by setting ALE and CLE to HIGH after the applicable t_{CAD} time has passed.

NV-DDR Commands

A command is written from DQ[7:0] to the command register on the rising edge of CLK when CE# is LOW, ALE is LOW, CLE is HIGH, and W/R# is HIGH.

After a command is latched—and prior to issuing the next command, address, or data I/O—the bus must go to bus idle mode on the next rising edge of CLK, except when the clock period, t_{CK} , is greater than t_{CAD} .

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, such as READ STATUS (70h) and READ STATUS ENHANCED (78h) are accepted by die (LUNs) even when they are busy.

**Figure 18: NV-DDR Command Cycle**

Note: 1. When CE# remains LOW, t_{CAD} begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

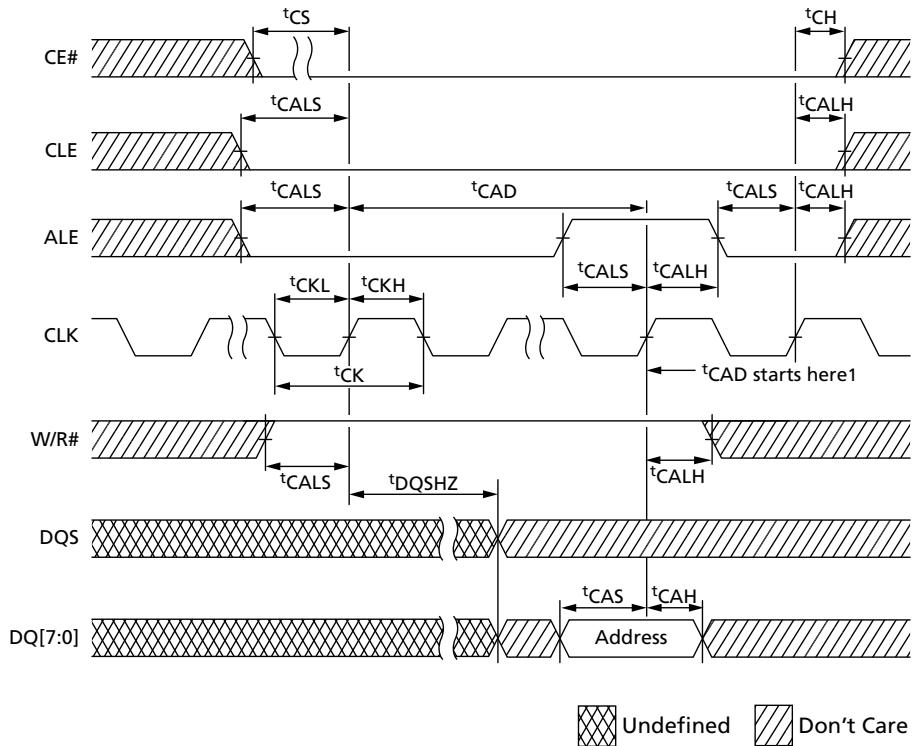
NV-DDR Addresses

A NV-DDR address is written from DQ[7:0] to the address register on the rising edge of CLK when CE# is LOW, ALE is HIGH, CLE is LOW, and W/R# is HIGH.

After an address is latched—and prior to issuing the next command, address, or data I/O—the bus must go to bus idle mode on the next rising edge of CLK, except when the clock period, t_{CK} , is greater than t_{CAD} .

Bits not part of the address space must be LOW (see Device and Array Organization). The number of address cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses such as address cycles that follow the READ STATUS ENHANCED (78h) command, are accepted by die (LUNs) even when they are busy.

**Figure 19: NV-DDR Address Cycle**

Note: 1. When CE# remains LOW, t_{CAD} begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

NV-DDR DDR Data Input

To enter the NV-DDR data input mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- W/R# is HIGH
- t_{CAD} is met
- DQS is LOW
- ALE and CLE are HIGH on the rising edge of CLK

Upon entering the NV-DDR data input mode after t_{DQSS} , data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when CLK is running and the DQS to CLK skew meets t_{DSH} and t_{DSS} , CE# is LOW, W/R# is HIGH, and ALE and CLE are HIGH on the rising edge of CLK.

To exit NV-DDR data input mode, the following conditions must be met:

- CLK is running and the DQS to CLK skew meets t_{DSH} and t_{DSS}
- CE# is LOW
- W/R# is HIGH
- ALE and CLE are latched LOW on the rising edge of CLK

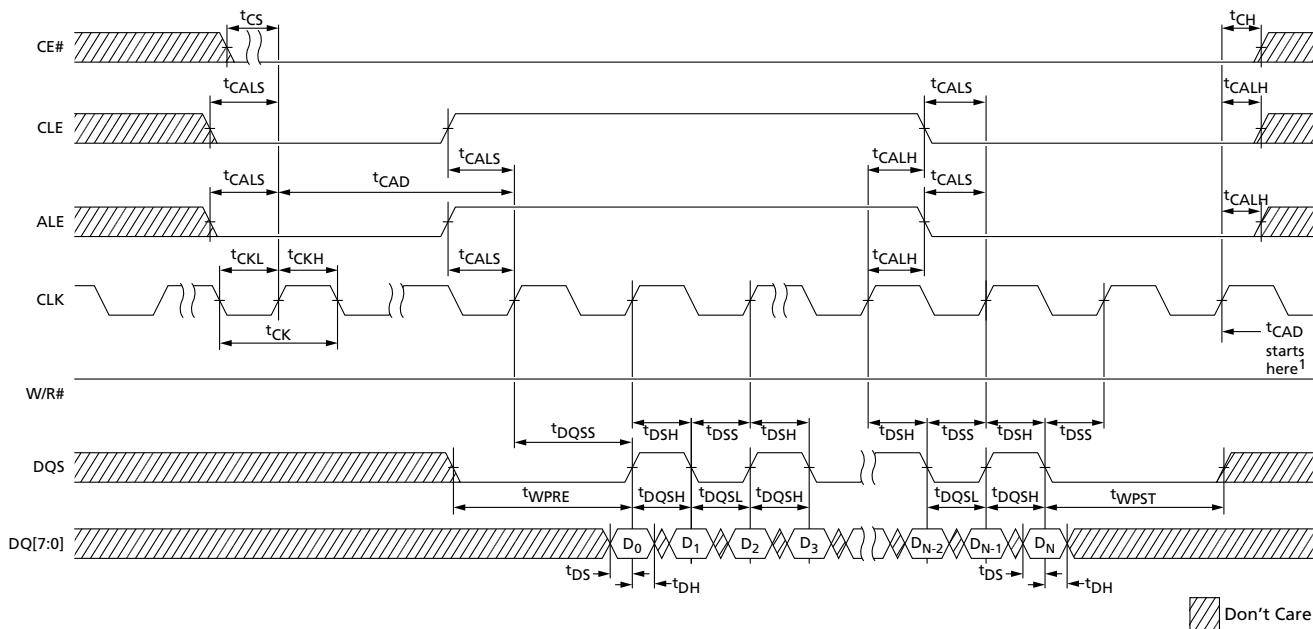


- The final two data bytes of the data input sequence are written to DQ[7:0] to the cache register on the rising and falling edges of DQS after the last cycle in the data input sequence in which ALE and CLE are latched HIGH.
- DQS is held LOW for t_{WPST} (after the final falling edge of DQS)

Following t_{WPST} , the bus enters bus idle mode and t_{CAD} begins on the next rising edge of CLK. After t_{CAD} starts, the host can disable the target if desired.

Data input is ignored by die (LUNs) that are not selected or are busy.

Figure 20: NV-DDR Data Input Cycles



- Notes:
- When CE# remains LOW, t_{CAD} begins at the first rising edge of the clock after t_{WPST} completes.
 - t_{DSH} (MIN) generally occurs during t_{DQSS} (MIN).
 - t_{DSS} (MIN) generally occurs during t_{DQSS} (MAX).

NV-DDR Data Output

Data can be output from a die (LUN) if it is ready. Data output is supported following a READ operation from the NAND Flash array.

To enter the NV-DDR data output mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- The host has released the DQ[7:0] bus and DQS
- W/R# is latched LOW on the rising edge of CLK to enable the selected die (LUN) to take ownership of the DQ[7:0] bus and DQS within t_{WRCK}
- t_{CAD} is met
- ALE and CLE are HIGH on the rising edge of CLK



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Upon entering the NV-DDR data output mode, DQS will toggle HIGH and LOW with a delay of t_{DQSCK} from the respective rising and falling edges of CLK. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than t_{AC} .

NV-DDR data output mode continues as long as CLK is running, CE# is LOW, W/R# is LOW, and ALE and CLE are HIGH on the rising edge of CLK.

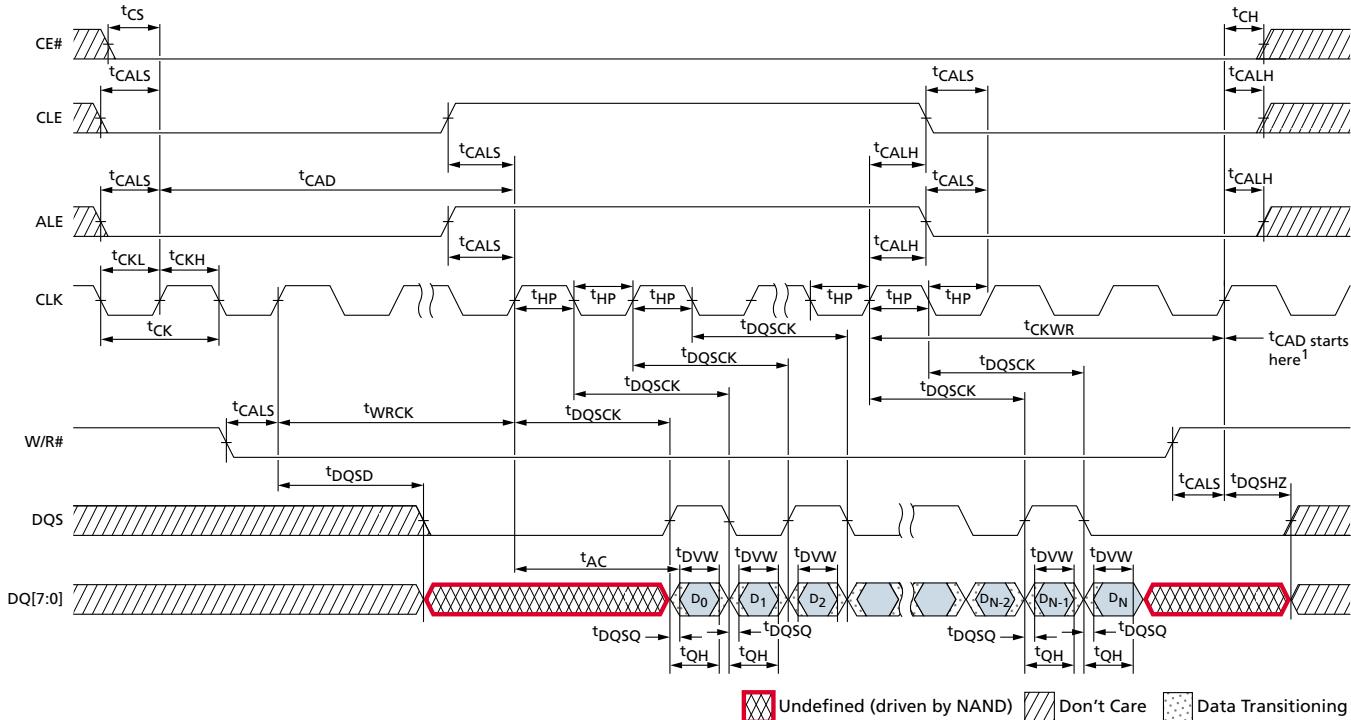
To exit NV-DDR data output mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- W/R# is LOW
- ALE and CLE are latched LOW on the rising edge of CLK

The final two data bytes are output on DQ[7:0] on the final rising and falling edges of DQS. The final rising and falling edges of DQS occur t_{DQSCK} after the last cycle in the data output sequence in which ALE and CLE are latched HIGH. After t_{CKWR} , the bus enters bus idle mode and t_{CAD} begins on the next rising edge of CLK. Once t_{CAD} starts the host can disable the target if desired.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

Figure 21: NV-DDR Data Output Cycles



- Notes:
1. When CE# remains LOW, t_{CAD} begins at the rising edge of the clock after t_{CKWR} for subsequent command or data output cycle(s).
 2. See Figure 18 (page 33) for details of W/R# behavior.



3. t_{AC} is the DQ output window relative to CLK and is the long-term component of DQ skew.
4. For W/R# transitioning HIGH, DQ[7:0] and DQS go to tri-state.
5. For W/R# transitioning LOW, DQ[7:0] drives current state and DQS goes LOW.
6. After final data output, DQ[7:0] is driven until W/R# goes HIGH, but is not valid.

Write Protect

See Write Protect under Bus Operations – Asynchronous Interface.

Ready/Busy#

See Ready/Busy# under Bus Operations – Asynchronous Interface.

Bus Operation – NV-DDR2 Interface

When the NV-DDR2 interface is activated on a target (see Activating Interfaces), the target is capable of high-speed DDR data transfers. and the DQS signal is enabled. DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

For operations in NV-DDR2 mode, the NV-DDR2 interface must be selected (see Activating the NV-DDR2 Interface). The capabilities that NV-DDR2 operations offers beyond NV-DDR operations include:

- Supported only at 1.8VV_{CCQ}
- Support for speeds beyond 200 MT/s
- Support for differential signaling for the RE# and/or DQS signals (RE_c, DQS_c)
- Support for WARMUP cycles
- Support for V_{REFQ}

Use of differential signaling and external V_{REFQ} is optional for interface speeds 200 MT/s or slower. Differential signaling and external V_{REFQ} are optional for NV-DDR2 interface speeds faster than 200 MT/s but required to guarantee specified AC timings. If a host does not use differential signaling and external V_{REFQ} at speeds faster than 200 MT/s, specified AC timings are not guaranteed. If not using the differential signaling, statements about those signal types can be ignored.

Transition from the NV-DDR2 interface to the NV-DDR interface is not permitted.

The NV-DDR2 interface bus modes are summarized below:

Table 6: NV-DDR2 Interface Mode Selection

Mode	CE#	CLE	ALE	RE# (RE_t)	DQS (DQS_t)	DQ[7:0]¹	WE#	WP#	Notes
Standby	H	X	X	X	X	X	X	0V/V _{CCQ}	1, 2
Idle	L	L	L	H	H	X	H	X	3
Command input	L	H	L	H	X	input		H	
Address input	L	L	H	H	X	input		H	

**Table 6: NV-DDR2 Interface Mode Selection (Continued)**

Mode	CE#	CLE	ALE	RE# (RE_t)	DQS (DQS_t)	DQ[7:0]¹	WE#	WP#	Notes
Data input	L	L	L	H		input	H	H	2
Data output	L	L	L			output	H	X	2
Write protect	X	X	X	X	X	X	X	L	

- Notes:
1. The current state of the device is data input, data output, or neither based on the commands issued.
 2. There are two data input/output cycles from the rising edge of DQS/RE# to the next rising edge of DQS/RE#.
 3. WE# is set HIGH during the Idle state.
 4. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

Differential Signaling

An enabler for higher speed operation is differential signaling for the RE# and DQS signals. A complementary RE# and complementary DQS signal may be optionally used to create differential signal pairs (RE_t/RE_c and DQS_t/DQS_c). When using differential signaling, RE# is referred to as RE_t and DQS is referred to as DQS_t, for example, the "true" versions of the signals. Differential signaling may be used to improve signal integrity through enhanced noise immunity. Differential signaling shall only be enabled for use when the NV-DDR2 data interface is selected.

A device may support differential RE# and/or differential DQS signaling. The support for differential RE# and/or DQS is reported in the parameter page. Complementary RE# (for example, RE_c) and complementary DQS (for example, DQS_c) signals are individually configured/enabled. By default, differential signaling is disabled. The host may configure the device to use differential signaling using the NV-DDR2 configuration feature address.

Differential signaling is not enabled by default. It is recommended that if differential signaling is used by a host system that it is enabled at the same time as the interface utilizing the differential signaling is enabled.

To begin using differential signaling, the host shall issue a SET FEATURES (EFh) command to the timing mode feature address that sets the data Interface from asynchronous to NV-DDR2 operation. Then issue a SET FEATURES (EFh) command to the NV-DDR2 configuration feature address to activate differential RE# and/or differential DQS signaling. The differential signaling is then enabled after CE# is brought HIGH.

To change from differential signaling to single-ended signaling, the host shall configure the device using the NV-DDR2 configuration feature address to disable differential signaling. The differential signaling is disabled after CE# is brought HIGH.

A RESET (FFh) command will disable differential signaling. The SYNCHRONOUS RESET (FCh) and RESET LUN (FAh) commands have no effect on differential signaling.



WARMUP Cycles

In order to support higher speed operation, WARMUP cycles for data output and data input may be provided. WARMUP cycles shall only be enabled for use when the NV-DDR2 data interface is selected.

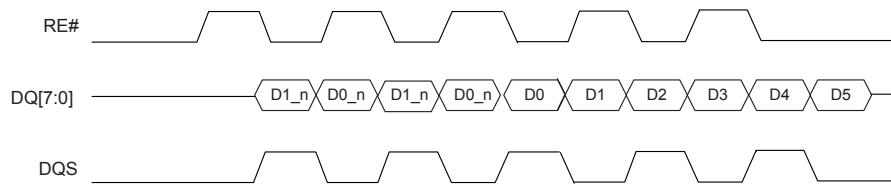
WARMUP cycles for data output provides extra RE# and corresponding DQS transitions at the beginning of a data output burst. These extra RE#/DQS transitions do not have any data associated with them. The number of extra cycles is configured via the NV-DDR2 configuration feature address.

WARMUP cycles for data input provides extra DQS transitions at the beginning of a data input burst. These extra DQS transitions do not have any data associated with them. The number of extra cycles is configured via the NV-DDR2 configuration feature address. The number of cycles specified includes a full data input cycle (both rising and falling edge for DQS).

WARMUP cycles are optional for both data output and data input, and if used, do not need to be configured to the same value. WARMUP cycles apply to all commands.

WARMUP cycles are initiated at the start of each data burst when WARMUP cycles are enabled for that data transfer type. If the host pauses and then resumes a data transfer without exiting and re-entering the data burst, then the host shall not issue additional WARMUP cycles. Exiting and re-entering the data burst shall be performed by bringing ALE, CLE, or CE# HIGH without latching with WE#. In the case of not re-issuing WARMUP cycles, the host should take care to avoid signal integrity issues due to pausing the data transfer and resuming without WARMUP cycles.

Figure 22: WARMUP Cycles for Data Output (2 WARMUP Cycles)



NV-DDR2 Standby

Prior to disabling a target, the target's bus must be idle. A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations.

NV-DDR2 Idle

A target's bus is idle when CE# is LOW, ALE is LOW, CLE is LOW, RE# is HIGH, and DQS is HIGH and no internal LUN operations are ongoing or data being inputted or outputted from the target. DQS is a "Don't Care" during Idle states.

During the bus idle mode, all signals are enabled. No commands, addresses, or data are latched into the target; no data is output.



NV-DDR2 Pausing Data Input/Output

Pausing data input or data output may be done by placing the bus in an Idle state. The pausing of data output may also be done by pausing RE# and holding the signal(s) static HIGH or LOW until the data burst is resumed. The pausing of data input may also be done by pausing DQS and holding the signal(s) static HIGH or LOW until the data burst is resumed. WE# shall be held HIGH during data input and output burst pause time. The host will be required to exit the data burst if it wishes to re-issue WARMUP cycles when re-starting. If the host wishes to end the data burst, after exiting the data burst, a new command is issued.

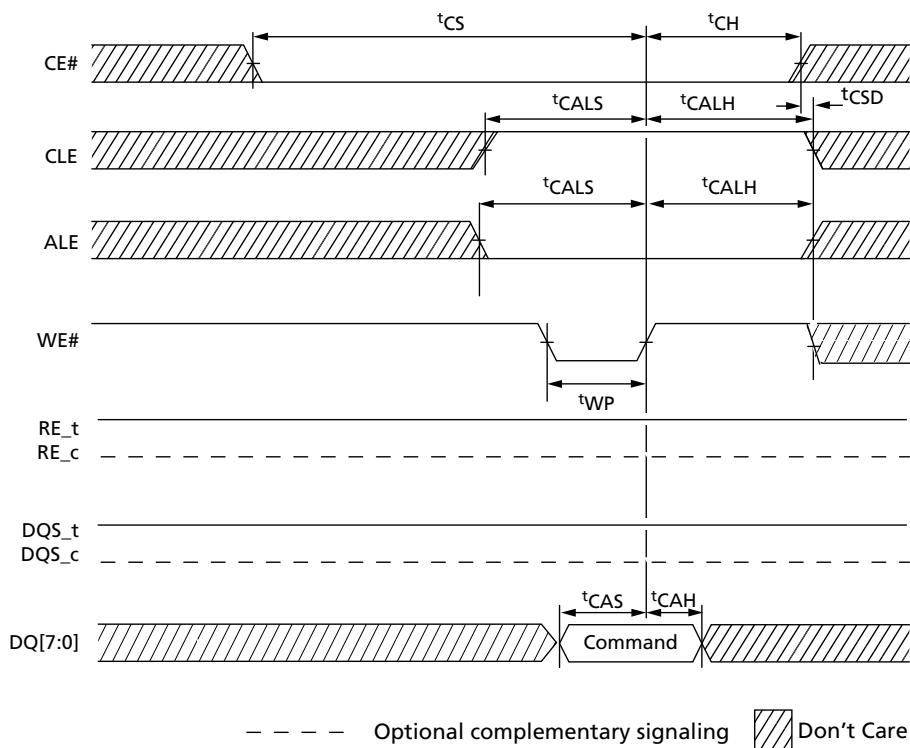
During the bus idle mode, all signals are enabled. No commands, addresses, or data are latched into the target; no data is output.

NV-DDR2 Commands

A command is written from DQ[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, such as READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs), even when they are busy.

Figure 23: NV-DDR2 Command Cycle



Note: 1. DQS is "Don't Care" during active command cycle (CLE is HIGH).



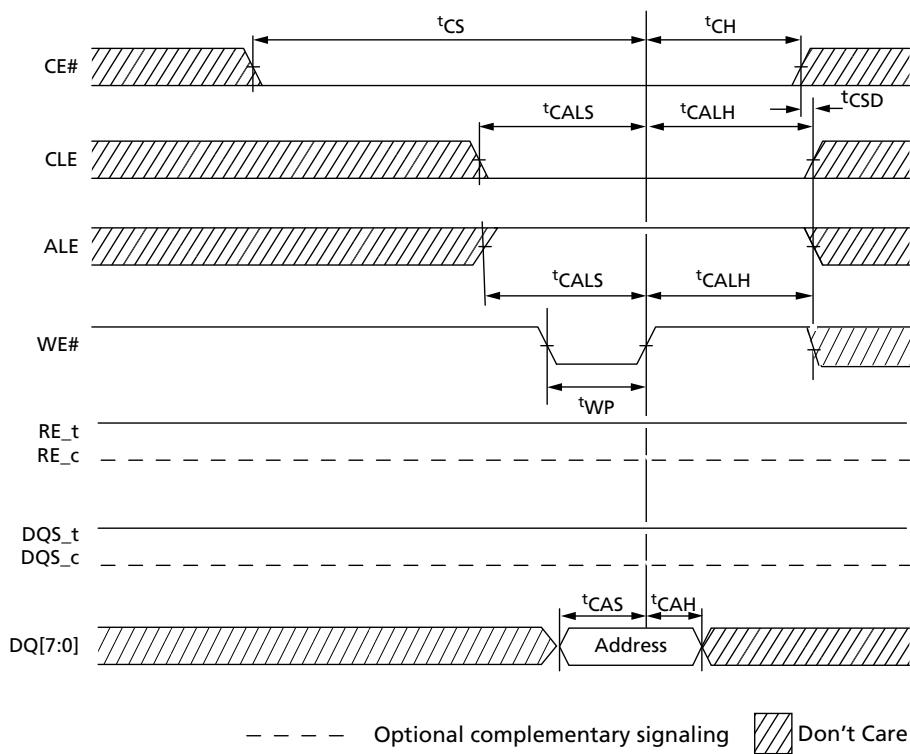
NV-DDR2 Addresses

A NV-DDR2 address is written from DQ[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits not part of the address space must be LOW (see Device and Array Organization). The number of address cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses such as address cycles that follow the READ STATUS ENHANCED (78h) command, are accepted by die (LUNs), even when they are busy.

Figure 24: NV-DDR2 Addresses Cycle



Note: 1. DQS is "Don't Care" during active address cycle (ALE is HIGH).

NV-DDR2 Data Input

To enter the NV-DDR2 data input mode, the following conditions must be met:

- CE# is LOW
- ALE and CLE are LOW
- RE# is HIGH
- tWPRE is met
- DQS is LOW

Upon entering the NV-DDR2 data input mode after tWPRE, data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when CE# is LOW, RE# is HIGH, and ALE and CLE are LOW.



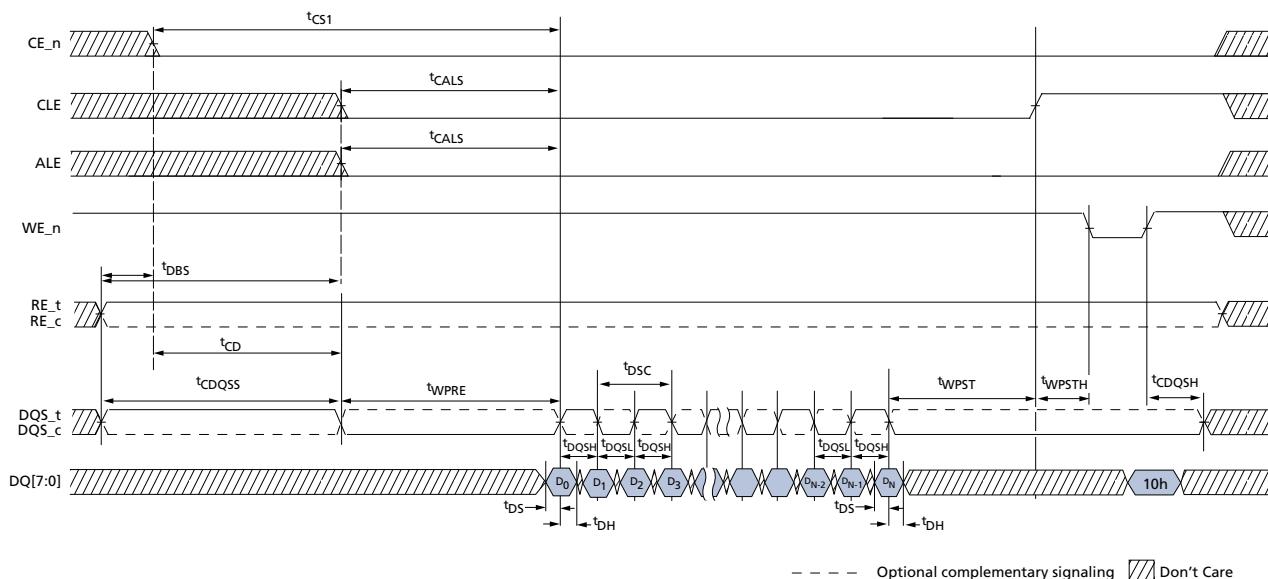
To exit NV-DDR2 data input mode, the following conditions must be met:

- CE# is LOW
- ALE and CLE are LOW
- RE# is HIGH
- The final two data bytes of the data input sequence are written to DQ[7:0] to the cache register on the rising and falling edges of DQS after the last cycle in the data input sequence
- DQS is held LOW for t_{WPST} (after the final falling edge of DQS)

Following t_{WPST} , CE#, CLE, or ALE should be brought HIGH to exit the data burst.

Data input is ignored by die (LUNs) that are not selected or are busy.

Figure 25: NV-DDR2 Data Input Cycles



NV-DDR2 Data Output

Data can be output from a die (LUN) if it is ready. Data output is supported following a READ operation from the NAND Flash array.

To enter the NV-DDR2 data output mode, the following conditions must be met:

- CE# is LOW
- The host has released the DQ[7:0] bus and DQS
- ALE and CLE are LOW
- t_{RPRE} is met

Upon entering the NV-DDR2 data output mode, DQS will toggle HIGH and LOW with a delay of t_{DQSRE} from the respective rising and falling edges of RE#. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than t_{AC} .

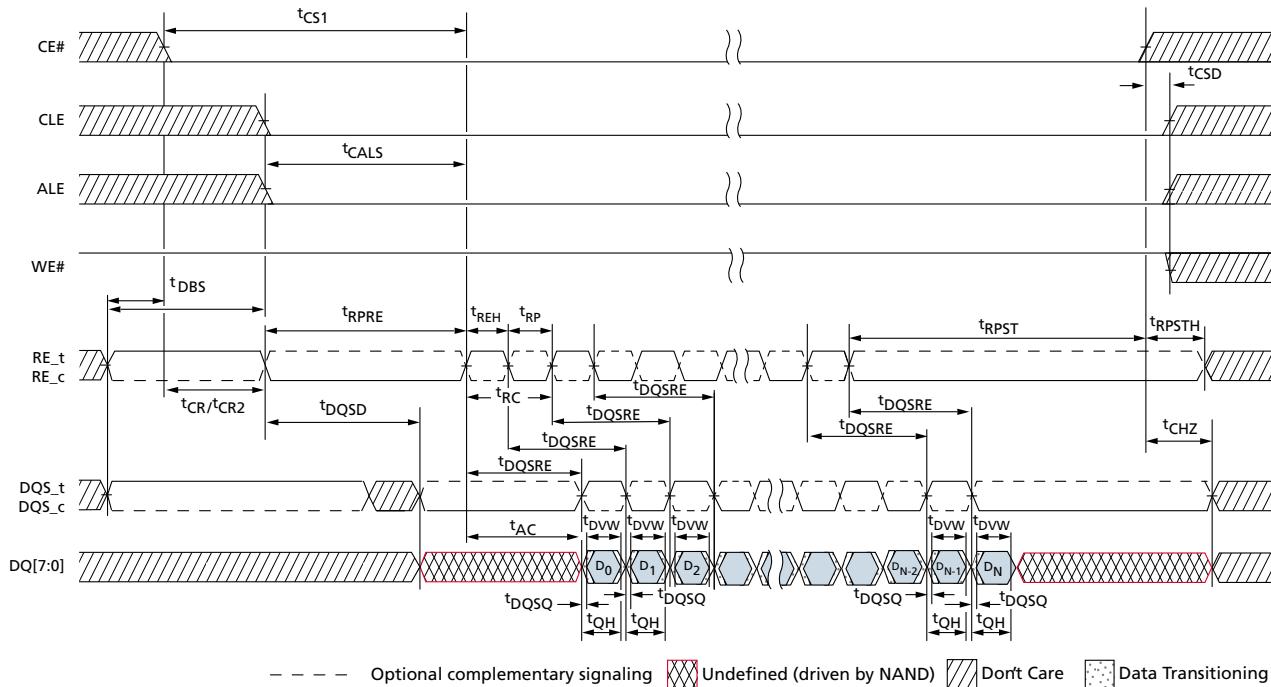
The final two data bytes are output on DQ[7:0] on the final rising and falling edges of DQS. The final rising and falling edges of DQS occur t_{DQSRE} after the last cycle in the



data output sequence. The host must hold RE# for t_{RPST} after the last RE# falling edge for data output.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

Figure 26: NV-DDR2 Data Output Cycles



Write Protect

See Write Protect under Bus Operations – Asynchronous Interface.

Ready/Busy#

See Ready/Busy# under Bus Operations – Asynchronous Interface.



Device Initialization

Some NAND Flash devices do not support V_{CCQ}. For these devices all references to V_{CCQ} are replaced with V_{CC}.

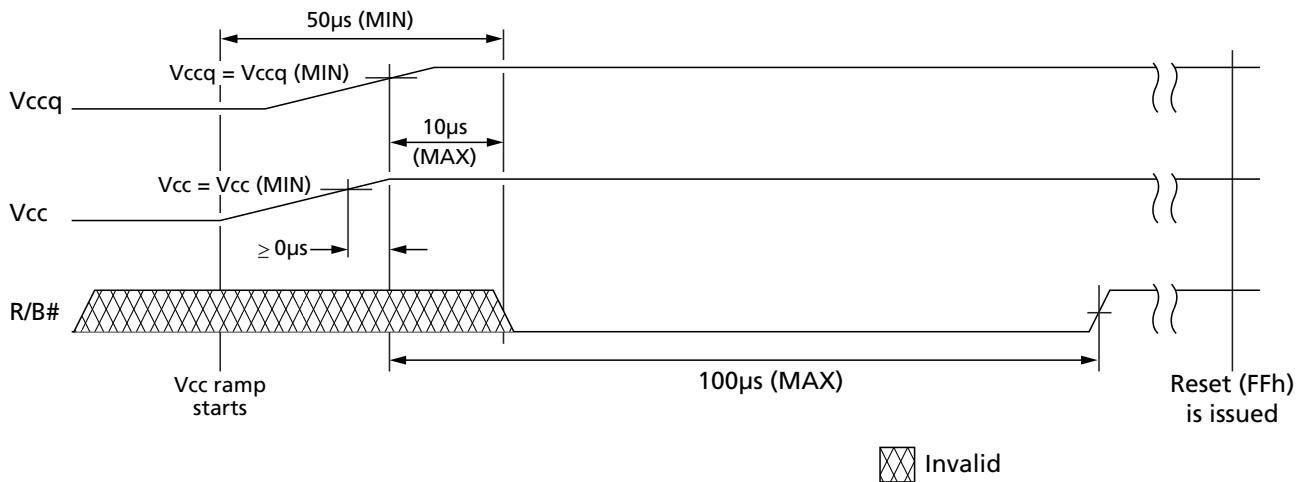
Micron NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored. (The WP# signal supports additional hardware protection during power transitions.) When ramping V_{CC} and V_{CCQ}, use the following procedure to initialize the device:

1. Ramp V_{CC}.
2. Ramp V_{CCQ}. V_{CCQ} may ramp before, simultaneously, or after V_{CC}.
3. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target (see Figure 27). The R/B# signal becomes valid when 50µs has elapsed since the beginning the V_{CC} ramp, and 10µs has elapsed since V_{CCQ} reaches V_{CCQ,min} and V_{CC} reaches V_{CC,min}.
4. If not monitoring R/B#, the host must wait at least 100µs after V_{CCQ} reaches V_{CCQ,min} and V_{CC} reaches V_{CC,min}. If monitoring R/B#, the host must wait until R/B# is HIGH.
5. If V_{CCQ} is in the 1.8V operational range, then the asynchronous interface is active by default for each target. Each LUN draws less than an average of I_{ST} measured over intervals of 1ms until the RESET (FFh) command is issued.
6. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for ^tPOR after a RESET command is issued. LUN0 of each target is selected by default after power-on. The RESET busy time can be monitored by polling R/B# or FIXED ADDRESS READ STATUS ENHANCED (71h) command must be used to check initialization status of each LUN on the target. The host must not issue an additional RESET (FFh) command during ^tPOR.
7. The device is now initialized and ready for normal operation.

At power-down, V_{CCQ} may go LOW, either before, simultaneously, or after V_{CC} going LOW.

When V_{CCQ} = 0V, the host must keep RE_t/RE_c, DQS_t/DQS_c signals LOW. RE_t/RE_c, DQS_t/DQS_c signals maybe ramped with V_{CCQ} during power-up but not exceed V_{CCQ}. When V_{CCQ} = 0V, the host must keep DQ[7:0] signals LOW or they can be left High-Z. DQ[7:0] signals maybe ramped with V_{CCQ} during power up but not exceed V_{CCQ}.

It is not permitted to drive or have the NAND R/B# signal HIGH while the NAND V_{CCQ} voltage is below V_{CCQ,min}. R/B# signals maybe ramped with V_{CCQ} during power up but not exceed V_{CCQ}.

**Figure 27: R/B# Power-On Behavior**

Note: 1. Disregard V_{CCQ} for devices that use only V_{CC} .

To initialize a discovered target, the following steps shall be taken. The initialization process should be followed for each connected CE# signal, including performing the READ PARAMETER PAGE (ECh) command for each target. Each chip enable corresponds to a unique target with its own independent properties that the host shall observe and subsequently use.

The host should issue the READ PARAMETER PAGE (ECh) command. This command returns information that includes the capabilities, features, and operating parameters of the device. When the information is read from the device, the host shall check the CRC to ensure that the data was received correctly and without error prior to taking action on that data.

If the CRC of the first parameter page read is not valid, the host should read redundant parameter page copies. The host can determine whether a redundant parameter page is present or not by checking if the first four bytes contain at least two bytes of the parameter page signature. If the parameter page signature is present, then the host should read the entirety of that redundant parameter page. The host should then check the CRC of that redundant parameter page. If the CRC is correct, the host may take action based on the contents of that redundant parameter page. If the CRC is incorrect, then the host should attempt to read the next redundant parameter page by the same procedure.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. The host may use bit-wise majority or other ECC techniques to recover the contents of the parameter page from the parameter page copies present. When the host determines that a parameter page signature is not present, then all parameter pages have been read.

After successfully retrieving the parameter page, the host has all information necessary to successfully communicate with that target. If the host has not previously mapped defective block information for this target, the host should next map out all defective blocks in the target. The host may then proceed to utilize the target, including ERASE and PROGRAM operations.



Electronic Mirroring

Electronically mirrored DQ[7:0] pinout is available in order to assist in optimizing printed circuit board (PCB) layout by assisting two-sided (clamshell) designs in reducing the complexity and the number of signal routing layers between the top and bottom side of the PCB. This ability for electronic mirrored DQ[7:0] pinout also assists in reducing the vertical profile of a two-sided system. Only the DQ[7:0] signals have the ability to be changed by electronic mirrored functionality, all other NAND signals remain static.

See Figure 28 (page 46) and Figure 29 (page 46) as examples of how packages in the default non-mirrored DQ[7:0] pinout and the mirrored DQ[7:0] pinout could be used in a two-sided PCB system.

Figure 28: Example PCB Layout of a Two-Sided System without Electronic Mirroring of DQ[7:0]

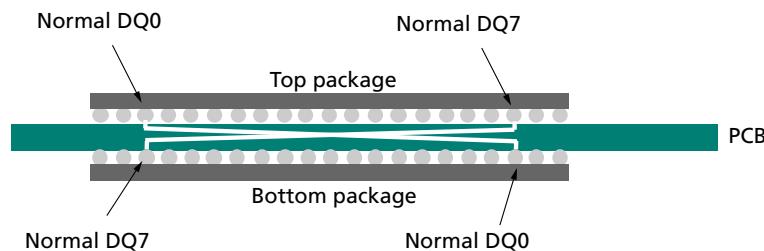
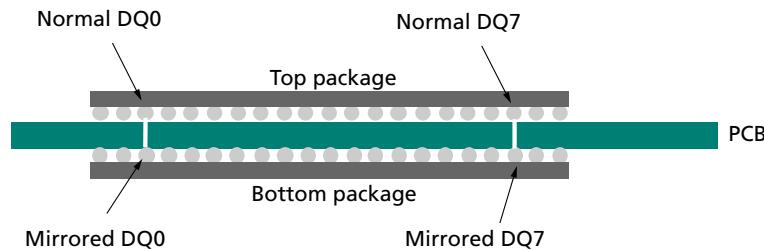


Figure 29: Example PCB Layout of a Two-Sided System with Electronic Mirroring of DQ[7:0]



The mirror and non-mirrored packages are physically the same with same internal bond connections, but based on how first issued command after device initialization is decoded, the LUNs internally are electrically configured to be non-mirrored or mirrored.

If using the mirrored DQ[7:0] pinout configuration, the READ STATUS (70h) command must be issued in order to properly configure the device DQ[7:0] signals as mirrored or non-mirrored mode after device initialization. This READ STATUS (70h) command appears as "0Eh" on the DQ[7:0] bus of the NAND device in the mirrored position; "0Eh" is not a valid command and is recognized by the NAND device as a 70h command which is the indication to the NAND target (CE#) to configure itself into mirrored DQ[7:0] mode. The READ STATUS (70h) command needs to be issued only once per target (CE#) or volume after device initialization for a device in the mirrored position; the device in the mirrored position will remain in the mirrored DQ[7:0] mode until device power-down.

If the READ STATUS (70h) command is issued prior to first RESET (FFh) and CE# pin reduction is enabled, then sequential initialization is enabled. If the READ STATUS



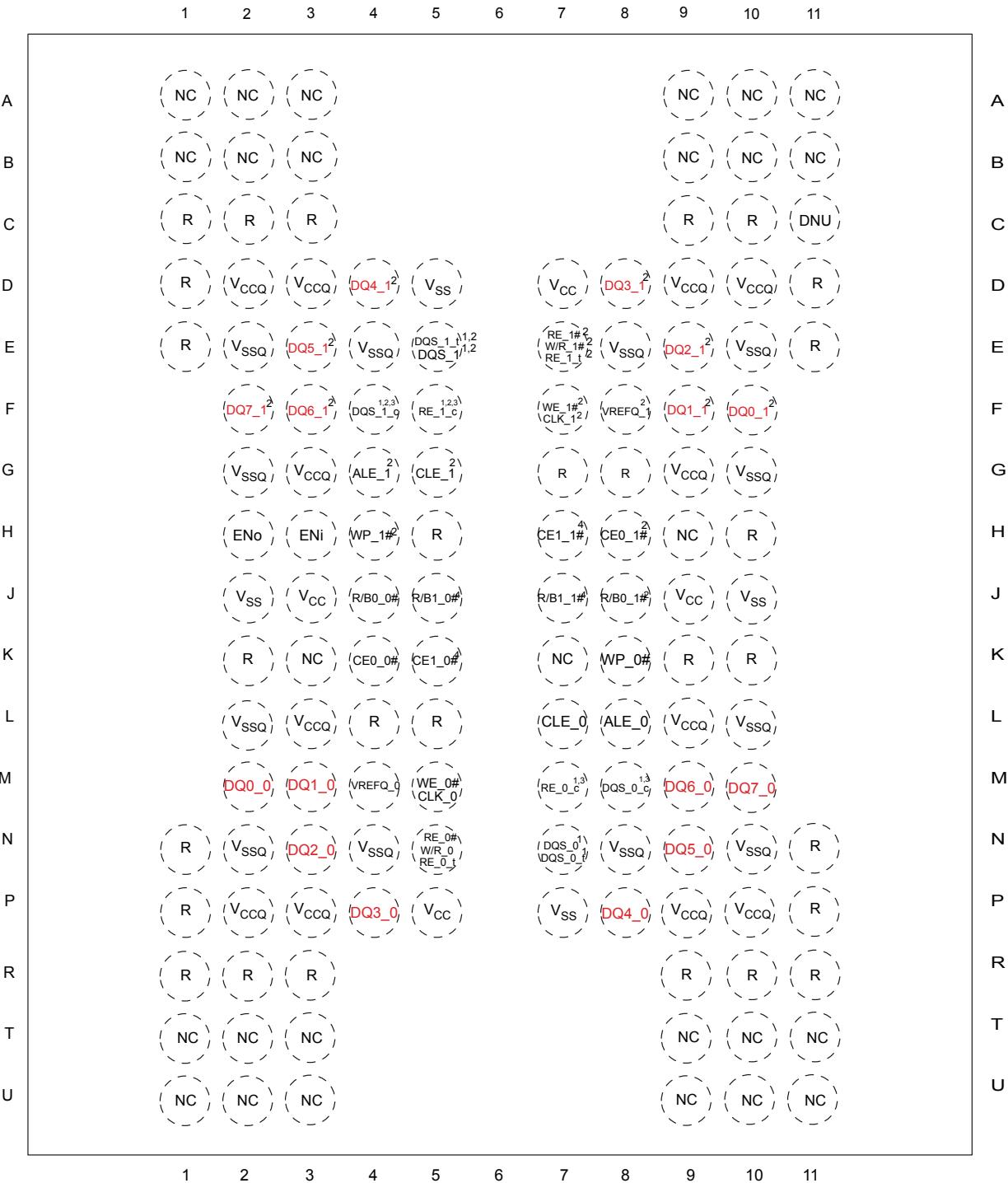
MLC 128Gb to 512Gb Async/Sync NAND Electronic Mirroring

(70h) command is issued after the first RESET (FFh) and CE# pin reduction is enabled, then parallel initialization is enabled.

Only the 132-ball and/or 152-ball BGA packages offer electronic mirroring operations. The 272-ball BGA package will not support electronic mirroring due to the limitation of DQ[7:0] signal assignment ordering.

See Figure 30 (page 48) as an example of how a package in the mirrored DQ[7:0] pinout changes signal assignments for the DQ[7:0] signals.

A HARD RESET (FDh) command will not change a device from the mirrored pinout configuration to the non-mirrored pinout configuration.


Figure 30: Example of 132-Ball BGA Package in Mirrored DQ[7:0] Pinout


Note: 1. Note the DQ[7:0] signals highlighted in red for the mirrored pinout configuration in comparison to the default non-mirrored pinout configuration. See the Signal Assignments section for the default non-mirrored pinout configuration for this package.



Activating Interfaces

After performing the steps under Device Initialization, the asynchronous interface is active for all targets on the device when the device powers on within the 1.8VV_{CCQ} operational range.

Each target's interface is independent of other targets, so the host is responsible for changing the interface for each target.

If the host and NAND Flash device, through error, are no longer using the same interface when within the 1.8VV_{CCQ} operational range, then steps under Activating the Asynchronous Interface are performed to re-synchronize the interfaces.

Activating the Asynchronous Interface

To activate the asynchronous NAND interface, once the synchronous interface is active, the following steps are repeated for each target:

1. The host pulls CE# HIGH, disables its input to CLK, and enables its asynchronous interface.
2. The host pulls CE# LOW and issues the RESET (FFh) command, using an asynchronous command cycle.
3. R/B# goes LOW for t_{RST} .
4. After t_{ITC} , and during t_{RST} , the device enters the asynchronous NAND interface. READ STATUS (70h) and READ STATUS ENHANCED (78h) are the only commands that can be issued.
5. After t_{RST} , R/B# goes HIGH. Timing mode feature address (01h), subfeature parameter P1 is set to 00h, indicating that the asynchronous NAND interface is active and that the device is set to timing mode 0.

For further details, see Reset Operations.

Activating the NV-DDR Interface

To activate the NV-DDR NAND Flash interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the Timing mode feature address.
3. Write P1 with 1Xh, where "X" is the timing mode used in the NV-DDR interface (see Configuration Operations).
4. Write P2-P4 as 00h-00h-00h.
5. R/B# goes LOW for t_{ITC} . The host should pull CE# HIGH. During t_{ITC} , the host should not issue any type of command, including status commands, to the NAND Flash device.
6. After t_{ITC} , R/B# goes HIGH and the synchronous interface is enabled. Before pulling CE# LOW, the host should enable the clock.

Activating the NV-DDR2 Interface

Transitions from NV-DDR directly to NV-DDR2 (or vice versa) is not supported. In this case, the host should transition to the asynchronous interface and then select the desired synchronous interface

Prior to selecting the NV-DDR2 interface, it is recommended that settings for the NV-DDR2 interface be configured. Specifically:



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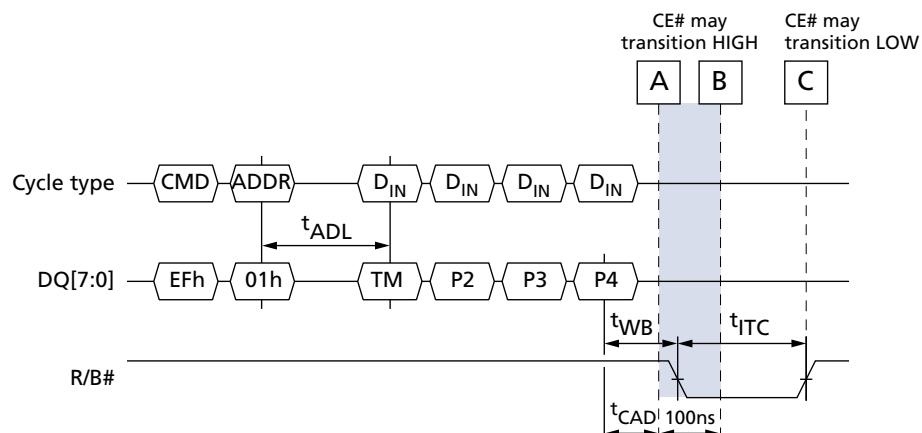
- SET FEATURES (EFh) command should be used to configure the NV-DDR2 Configuration feature address.

These actions should be completed prior to selecting the NV-DDR2 interface. If these settings are modified when the NV-DDR2 interface is already selected, the host should take care to ensure appropriate settings are applied in a manner that avoids signal integrity issues.

To activate the NV-DDR2 NAND Flash interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the Timing mode feature address.
3. Write P1 with 2Xh, where "X" is the timing mode used in the NV-DDR2 interface (see Configuration Operations).
4. Write P2–P4 as 00h-00h-00h.
5. R/B# goes LOW for t_{ITC} . The host should pull CE# HIGH. During t_{ITC} , the host should not issue any type of command, including status commands, to the NAND Flash device.
6. After t_{ITC} , R/B# goes HIGH and the NV-DDR2 interface is enabled.

Figure 31: Activating Interfaces



Note: 1. TM = Timing mode.



CE# Pin Reduction and Volume Addressing

In higher density capacity implementations there may be a significant number of CE# pins required for a host to support where there are many NAND packages with two to four CE# pins per package. The CE# pin reduction mechanism enables a single CE# pin from the host to be shared by multiple NAND targets, thus enabling a significant reduction in the number of CE# pins required by the host system. The CE# pin reduction mechanism may be utilized with any data interface (asynchronous, NV-DDR, NV-DDR2).

In the CE# pin reduction mechanism, each NAND package is appointed a volume address during the initialization sequence. After initialization is complete, the host may address a particular volume (NAND target) by using the VOLUME SELECT (E1h) command. See VOLUME SELECT (E1h) for more details.

ENi and ENo pins are added to each NAND package and a daisy chain is created between NAND packages. The first NAND package in the chain has the ENi pin as not connected. All other NAND packages have their ENi pin connected to the previous package's ENo pin in a daisy chain configuration.

At power-on, the ENo pins are driven LOW by the NAND device. ENo shall be High-Z when all CE# signals on the NAND package are HIGH. When a NAND target has had a volume address appointed with the SET FEATURES (EFh) command, then the ENo pin shall be pulled HIGH by the NAND target when the corresponding CE# is LOW. This enables the next NAND target on a subsequent package in the daisy chain to accept commands because the ENi pin pulls HIGH when ENo is no longer pulling LOW. After a volume address has been appointed to a volume (i.e., NAND target), that volume shall become deselected and ignores the ENi pin until the next power cycle.

The state of ENi determines whether the NAND package is able to accept commands. If the ENi pin is HIGH and CE# is LOW for the NAND target, then the NAND target shall accept commands. If the ENi pin is LOW or CE# is HIGH for the NAND Target, then the NAND Target shall not accept commands.

To be selected to process a command, the VOLUME SELECT command shall be issued to the host target using the volume address that was previously appointed for a particular NAND target. After the CE# signal is pulled HIGH for tCEH time, all LUNs on a volume revert to their previous states.

A HARD RESET (FDh) command will not undo CE# Pin Reduction or any previously set Volume addressing assignments that were performed prior to the HARD RESET (FDh) command.



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Figure 32: CE# Pin Reduction Topology with Single Channel

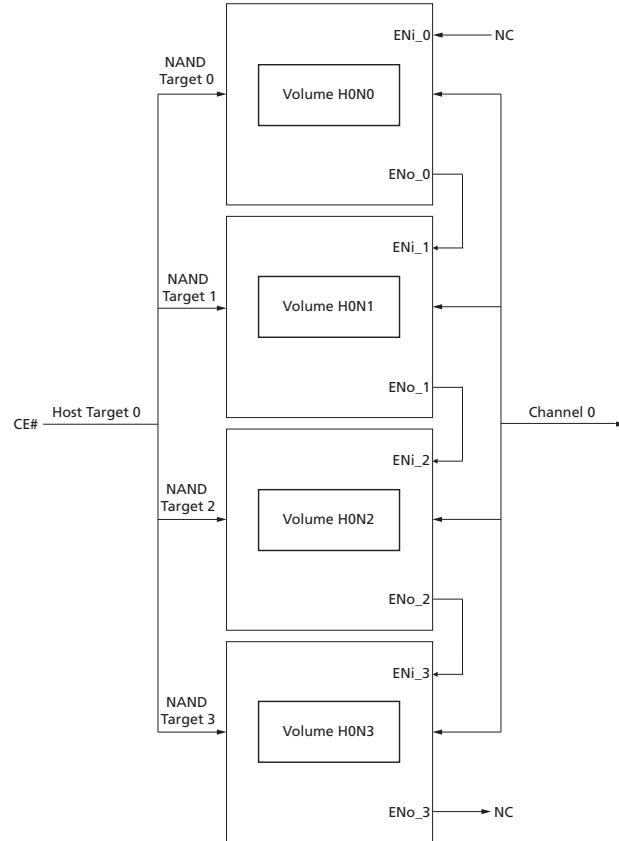
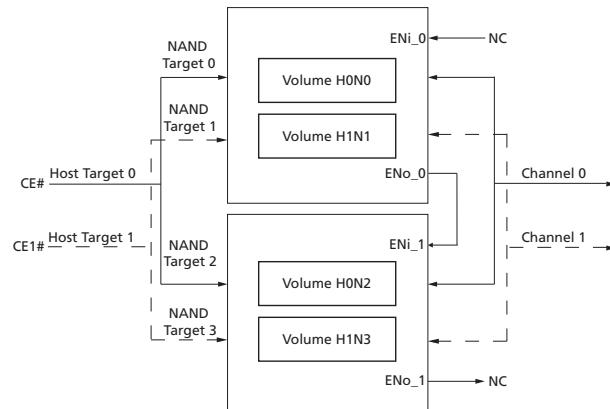


Figure 33: CE# Pin Reduction and Volume Addressing Topology with Dual Channel





Initialization Sequence

The host may issue a RESET (FFh) to all targets in parallel on the selected host target, or the host may sequentially issue RESET (FFh) to each target. The methodology chosen depends on host requirements for maximum current draw. To reset all targets in parallel, the host issues a RESET (FFh) as the first command issued to the NAND device(s). To reset targets sequentially, the host issues a READ STATUS (70h) command as the first command issued to all NAND targets on the selected host target.

During initialization when addressing a newly selected NAND target with an initial command, the host shall wait for the ENo signal to be propagated to the ENi of the subsequent target. Before addressing a new target, the host shall wait ($t_{ENo} + t_{ENi}$) and should also include signal propagation time.

In cases where there are multiple NAND targets within a package (multiple CE#), those NAND targets share the same ENo signal, and the host shall not stagger SET FEATURES (EFh) commands that appoint the volume addresses. If the SET FEATURES (EFh) commands are not issued simultaneously, then the host shall wait until volume appointment for previous NAND target(s) is complete before issuing the next SET FEATURES (EFh) command to appoint the volume address for the next NAND target that shares the ENo within a package.

After issuing the SET FEATURE (EFh) command to appoint the volume address, the host shall not issue another command to any NAND target on the associated host target (including status commands) until after the t_{FEAT} time has elapsed. This is to ensure that the proper NAND target responds to the next command, allowing for the proper ENo/ENi signal levels to be reflected.

The initialization sequence when utilizing the CE# reduction functionality is as follows:

1. The host powers on the NAND device(s).
2. The host pulls CE# LOW.
3. If resetting all NAND targets in parallel, then the host issues the RESET (FFh) command. This command is accepted by all NAND targets connected to the CE# (host target).
4. If resetting each NAND target sequentially, then:
 - a. The host issues the READ STATUS (70h) command to check for ready status. Issuing the READ STATUS (70h) command prior to any other command indicates sequential RESET (FFh) of each NAND target. The host then issues the RESET (FFh) command, which is only accepted by NAND devices with ENi set HIGH.
 5. The host issues a READ STATUS (70h) command and waits for the device to be ready (RDY = 1; ARDY = 1).
 6. The host configures the NAND target via commands necessary to perform that function (READ PARAMETER PAGE (ECh) command, SET FEATURES (EFh) command, etc).
 7. The host issues SET FEATURES (EFh) command to the volume configuration feature address to appoint the volume address for the NAND target. The volume address specified shall be unique amongst all NAND targets. After the SET FEATURE (EFh) command completes, ENo is set to one and the volume is deselected until a VOLUME SELECT (E1h) command is issued that selects the volume. The host shall not issue another command to a NAND target connected to the associated host target until after t_{FEAT} time has elapsed.



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8. For each NAND target connected to a host target, steps 4–7 are repeated for sequential initialization, and steps 5–7 are repeated for parallel initialization.
9. When no further NAND targets are found connected to the host target, then repeat steps 2–8 for the next host target (i.e., host CE# pin).
10. To complete the initialization process, a VOLUME SELECT (E1h) command is issued to select the next volume that is going to execute a command.

After volume addresses have been appointed to all NAND targets, the host may complete any additional initialization tasks and then proceed with normal operation. Prior to issuing a command to a volume, the VOLUME SELECT (E1h) command shall be issued.

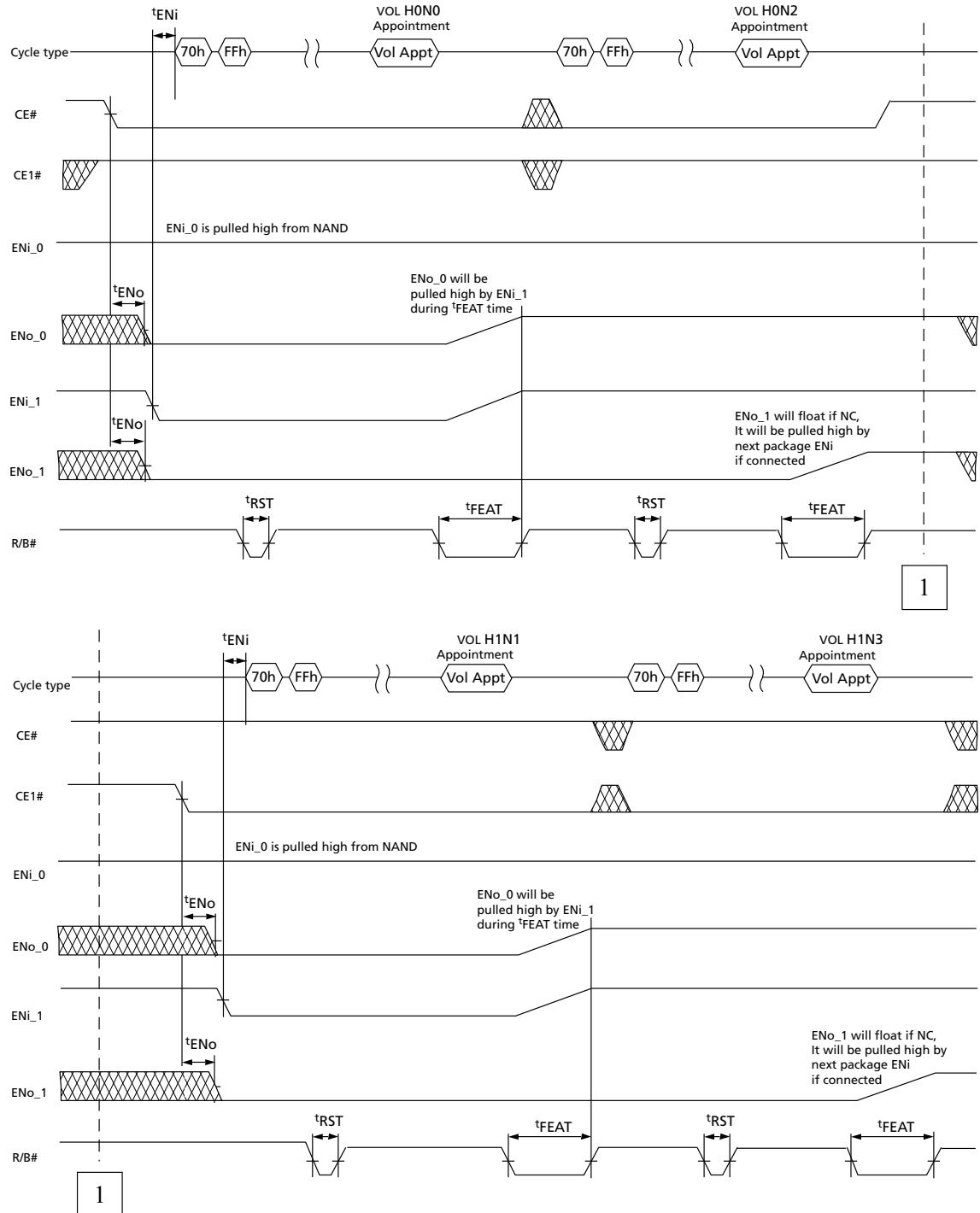
The host CE# signal shall be kept LOW for steps 2–7. If the host CE# signal that is LOW for steps 2–7 is brought HIGH anytime after step 7 but before the initialization process is complete, then 'CS for Asynchronous timing mode 0 shall be used.

Figure 34 (page 55) is an example of sequential reset initialization for the CE# pin reduction topology of Figure 33 (page 52).



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Figure 34: Example of Sequential Reset Initialization



Volume Appointment Without CE# Pin Reduction

If CE# pin reduction is not used (for example, if ENi and ENo are not connected) and the host desires to have the terminator on a package that does not share a CE# with the



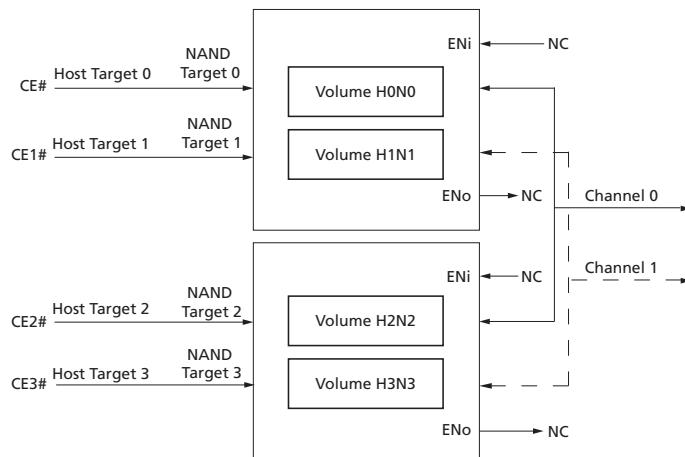
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selected NAND target, then each package that shares the CE# must have a volume appointed at initialization using the SET FEATURE (EFh) command using the volume configuration feature.

Each CE# must have a unique volume address appointed. Once all NAND targets have volume addresses appointed, the appointed volume addresses may be used for termination selection. Volume addressing is not required for operation due to discrete CE# signals; however, the VOLUME SELECT (E1h) command is required for terminator selection when using non-target termination schemes.

During operation, the CE# signal for the selected Volume and for any NAND targets assigned as a terminator for the selected volume need to be brought LOW. When CE# is brought LOW for an unselected volume, all LUNs that are not assigned as terminators for the selected volume are deselected.

Figure 35: Volume Addressing Without CE# Pin Reduction Topology with Dual Channel



Appointing Volume Addresses

To appoint a volume address, the SET FEATURE command is issued with a feature address of volume configuration. The volume address is not retained across power cycles; thus, if volume addressing is going to be used it needs to be appointed after each power-on prior to use of the NAND device(s). The volume address is retained when HARD RESET (FDh) command is issued.

Selecting a Volume

After volume addresses have been appointed, every NAND target (and associated LUN) is selected when the associated CE# is pulled LOW. After CE# is held LOW for at least 100ns, the host issues a VOLUME SELECT (E1h) command to indicate the volume (NAND target) that shall execute the next command issued.

Multiple Volume Operation Restrictions

Volumes are independent entities. A multiple volume operation is when two or more Volumes are simultaneously processing commands. Before issuing a command to an unselected volume, CE# shall be pulled HIGH for a minimum of tCEH, and the VOLUME SELECT (E1h) command shall then be issued to select the volume to issue a com-



mand to next. While commands (including multi-LUN operations) are being performed on the selected volume, a VOLUME SELECT (E1h) command is not required.

Issuing the same command to multiple volumes at the same time is not supported.

For a LUN level command (e.g., READ, PROGRAM), the host may select a different volume during a data input or data output operation and then resume the data transfer operation at a later time for a LUN level command. When re-selecting a Volume and associated LUN to complete the data input or data output operation, the following actions are required:

- Data input: The host shall wait t_{CCS} and then issue a CHANGE ROW ADDRESS (85h) command prior to resuming data input.
- Data output: The host shall issue a CHANGE READ COLUMN ENHANCED (06h-E0h) or RANDOM DATA OUT (00h-05h-E0h) command prior to resuming data output.

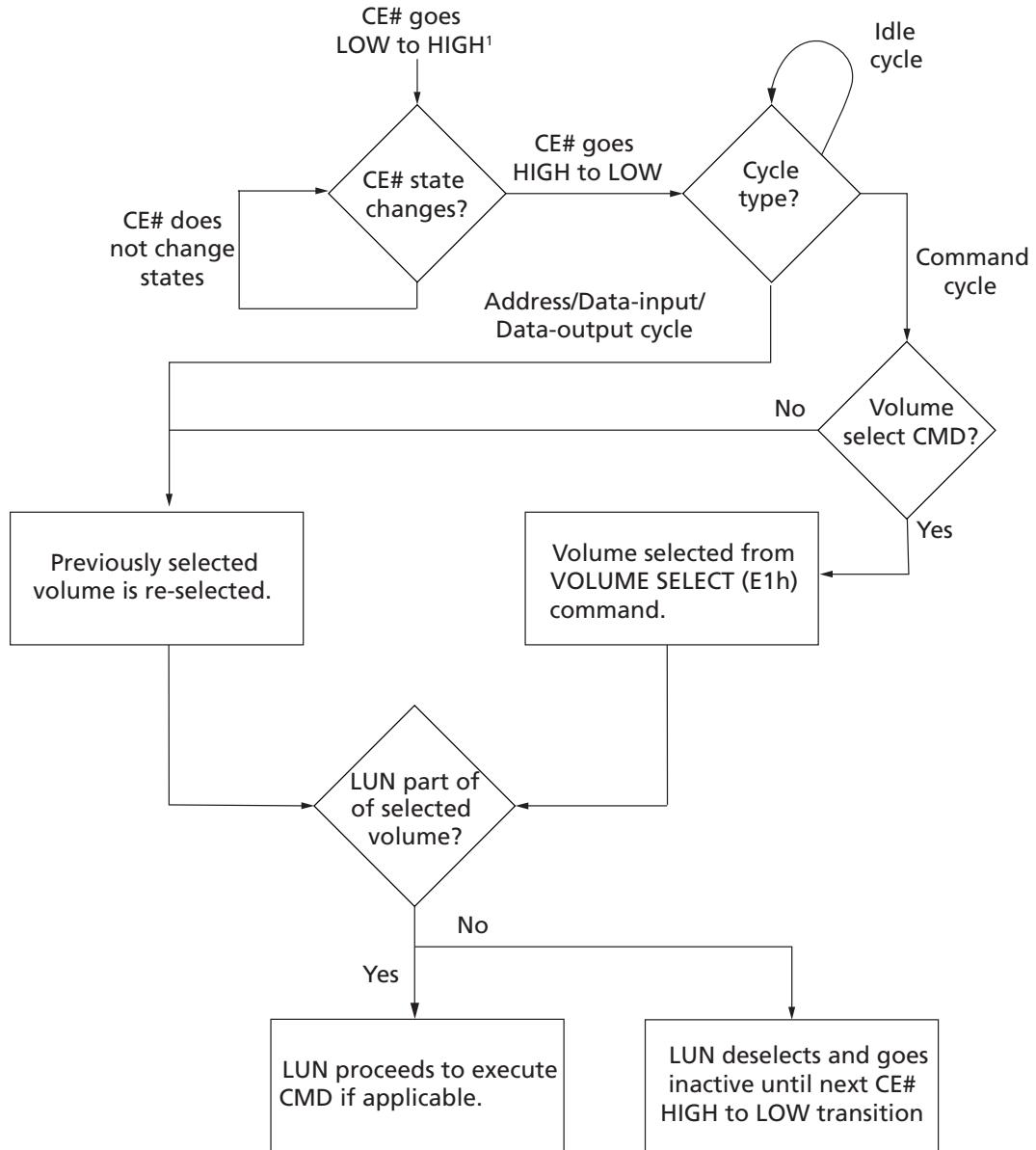
For a target level command (GET FEATURES (EEh), SET FEATURES (EFh)), the host shall complete all data input or data output operations associated with that command prior to selecting a new volume.

A VOLUME SELECT command shall not be issued during the following atomic portions of the COPYBACK, READ, PROGRAM, and ERASE operations:

- READ operations:
 - READ PAGE (00h-30h)
 - COPYBACK READ (00h-35h)
 - READ PAGE MULTI-PLANE (00h-32h)
 - READ PAGE CACHE RANDOM (00h-31h)
- PROGRAM operations, note: The VOLUME SELECT (E1h) command may be issued prior to the 10h or 11h command if the next command to this volume is CHANGE ROW ADDRESS (85h). After Volume Select command is issued to resume data input, the host shall wait t_{CCS} before issuing Change Row Address command:
 - PROGRAM PAGE (80h-10h)
 - PROGRAM PAGE MULTI-PLANE (80h/81h-11h)
 - COPYBACK PROGRAM (85h-10h)
 - COPYBACK PROGRAM MULTI-PLANE (85h-11h)
- ERASE operations:
 - ERASE BLOCK (60h-D0h)
 - ERASE BLOCK MULTI-PLANE (60h-D1h or 60h-60h-D0h)

Volume Reversion

When using volume addressing, the LUNs shall support Volume reversion. Specifically, if CE# is transitioned from HIGH to LOW and a Volume Select is not the first command, then the LUN shall revert to the previously Selected, Sniff, and Deselected states based on the last specified volume address.

**Figure 36: Volume Reversion behavioral flow**

Note: 1. This state is entered asynchronously when CE# transitions from LOW to HIGH.



Command Definitions

Table 7: Command Set

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Number of Valid Address Cycles #2	Command Cycle #3	Valid While Selected LUN is Busy ¹	Valid While Other LUNs are Busy ²	Notes
Reset Operations									
RESET	FFh	0	–	–	–	–	Yes	Yes	
HARD RESET	FDh	0	–	–	–	–		Yes	
SYNCHRO- NOUS RESET	FCh	0	–	–	–	–	Yes	Yes	
RESET LUN	FAh	3	–	–	–	–	Yes	Yes	
Identification Operations									
READ ID	90h	1	–	–	–	–			3
READ PARAMETER PAGE	ECh	1	–	–	–	–			
READ UNIQUE ID	EDh	1	–	–	–	–			
Configuration Operations									
VOLUME SELECT	E1h	1	–	–	–	–			
GET FEATURES	EEh	1	–	–	–	–			3
SET FEATURES	EFh	1	4	–	–	–			4
GET FEATURES by LUN	D4h	2	–	–	–	–		Yes	3
SET FEATURES by LUN	D5h	2	4	–	–	–		Yes	4
SLC MODE ENABLE	DAh	0	–	–	–	–		Yes	
SLC MODE DISABLE	DFh	0	–	–	–	–		Yes	
Status Operations									
READ STATUS	70h	0	–	–	–	–	Yes		
FIXED ADDRESS READ STATUS ENHANCED	71h	1	–	–	–	–	Yes	Yes	
READ STATUS ENHANCED	78h	3	–	–	–	–	Yes	Yes	

**Table 7: Command Set (Continued)**

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Number of Valid Address Cycles #2	Command Cycle #3	Valid While Selected LUN is Busy¹	Valid While Other LUNs are Busy²	Notes
Column Address Operations									
CHANGE READ COLUMN	05h	2	–	E0h	–	–		Yes	
CHANGE READ COLUMN ENHANCED (ONFI)	06h	5	–	E0h	–	–		Yes	
CHANGE READ COLUMN ENHANCED (JEDEC)	00h	5	–	05h	2	E0h		Yes	
CHANGE WRITE COLUMN	85h	2	Optional	–	–	–		Yes	
CHANGE ROW ADDRESS	85h	5	Optional	11h (Optional)	–	–		Yes	5
Read Operations									
READ MODE	00h	0	–	–	–	–		Yes	
READ PAGE	00h	5	–	30h	–	–		Yes	6
READ PAGE MULTI-PLANE	00h	5	–	32h	–	–		Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	–	–	–	–		Yes	7
READ PAGE CACHE RANDOM	00h	5	–	31h	–	–		Yes	6, 7
READ PAGE CACHE LAST	3Fh	0	–	–	–	–		Yes	7
Program Operations									
PROGRAM PAGE	80h	5	Yes	10h	–	–		Yes	
PROGRAM PAGE MULTI-PLANE	80h or 81h	5	Yes	11h	–	–		Yes	

**Table 7: Command Set (Continued)**

Command	Command Cycle #1	Number of Valid Address Cycles	Data Input Cycles	Command Cycle #2	Number of Valid Address Cycles #2	Command Cycle #3	Valid While Selected LUN is Busy¹	Valid While Other LUNs are Busy²	Notes
PROGRAM SUSPEND	84h	5	–	–	–	–	Yes	Yes	
PROGRAM RESUME	13h	5	–	–	–	–		Yes	
Erase Operations									
ERASE BLOCK	60h	3	–	D0h	–	–		Yes	
ERASE BLOCK MULTI-PLANE (ONFI)	60h	3	–	D1h	–	–		Yes	
ERASE BLOCK MULTI-PLANE (JEDEC)	60h	3	–	60h	3	D0h		Yes	
ERASE SUSPEND	61h	3	–	–	–	–	Yes	Yes	
ERASE RESUME	D2h	–	–	–	–	–		Yes	
Copyback Operations									
COPYBACK READ	00h	5	–	35h	–	–		Yes	6
COPYBACK PROGRAM	85h	5	Optional	10h	–	–		Yes	
COPYBACK PROGRAM MULTI-PLANE	85h	5	Optional	11h	–	–		Yes	

- Notes:
1. Busy means RDY = 0.
 2. These commands can be used for interleaved die (multi-LUN) operations.
 3. The READ ID (90h), GET FEATURES (EEh), and GET FEATUERS by LUN (D4h) commands output identical data on rising and falling DQS edges.
 4. The SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands requires data transition prior to the rising edge of CLK, with identical data for the rising and falling edges.
 5. Command cycle #2 of 11h is conditional. See CHANGE ROW ADDRESS (85h) for more details.
 6. This command can be preceded by READ PAGE MULTI-PLANE (00h-32h) command to accommodate a maximum simultaneous multi-plane array operation.
 7. Issuing a READ PAGE CACHE-series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE-series command; otherwise, it is prohibited.



Reset Operations

RESET (FFh)

The RESET (FFh) command is used to put a target into a known condition and to abort command sequences in progress. This command is accepted by all die (LUNs), even when they are busy.

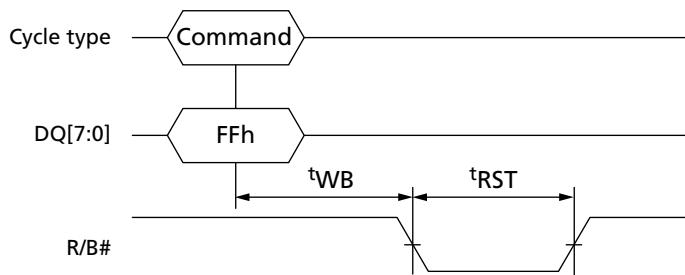
When FFh is written to the command register, the target goes busy for t_{RST} . During t_{RST} , the selected target (CE#) discontinues all array operations on all die (LUNs). All pending single- and multi-plane operations are cancelled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more die (LUNs), the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are valid.

RESET (FFh) must be issued as the first command to each target following power-up (see Device Initialization). Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET. To determine when each LUN on the target is ready, use FIXED ADDRESS READ STATUS ENHANCED (71h).

If the RESET (FFh) command is issued when the synchronous interface is enabled (NV-DDR/NV-DDR2), the target's interface is changed to the asynchronous interface and the timing mode is set to 0. The RESET (FFh) command can be issued asynchronously when the synchronous (NV-DDR) interface is active, meaning that CLK does not need to be continuously running when CE# is transitioned LOW and FFh is latched on the rising edge of CLK. After this command is latched, the host should not issue any commands during t_{ITC} . After t_{ITC} , and during or after t_{RST} , the host can poll each LUN's status register.

If the RESET (FFh) command is issued when the asynchronous interface is active, the target's asynchronous timing mode remains unchanged. During or after t_{RST} , the host can poll each LUN's status register.

Figure 37: RESET (FFh) Operation



SYNCHRONOUS RESET (FCh)

When the synchronous interface is active, the SYNCHRONOUS RESET (FCh) command is used to put a target into a known condition and to abort command sequences in progress. This command is accepted by all die (LUNs), even when they are BUSY.

When FCh is written to the command register, the target goes busy for t_{RST} . During t_{RST} , the selected target (CE#) discontinues all array operations on all die (LUNs). All pending single- and multi-plane operations are cancelled. If this command is issued



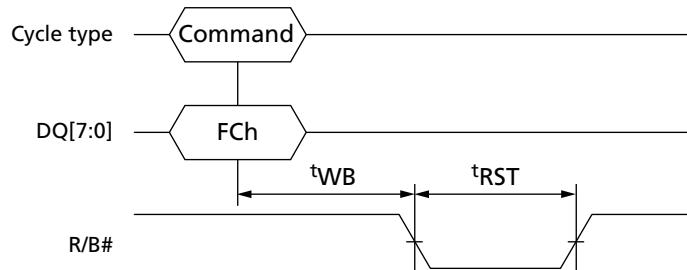
MLC 128Gb to 512Gb Async/Sync NAND Reset Operations

while a PROGRAM or ERASE operation is occurring on one or more die (LUNs), the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are valid and the synchronous interface remains active.

During or after t_{RST} , the host can poll each LUN's status register.

SYNCHRONOUS RESET is only accepted while the synchronous interface (NV-DDR/NV-DDR2) is active. Its use is prohibited when the asynchronous interface is active.

Figure 38: SYNCHRONOUS RESET (FCh) Operation





RESET LUN (FAh)

The RESET LUN (FAh) command is used to put a particular LUN on a target into a known condition and to abort command sequences in progress. This command is accepted by only the LUN addressed by the RESET LUN (FAh) command, even when that LUN is busy.

When FAh is written to the command register, the addressed LUN goes busy for t_{RST} . During t_{RST} , the selected LUN discontinues all array operations. All pending single- and multi-plane operations are canceled. If this command is issued while a PROGRAM or ERASE operation is occurring on the addressed LUN, the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are valid.

If the RESET LUN (FAh) command is issued when the synchronous (NV-DDR/NV-DDR2) interface is enabled, the target's interface remains in synchronous mode.

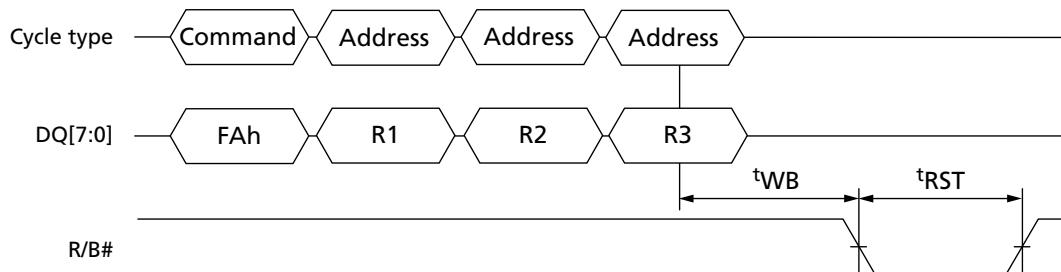
If the RESET LUN (FAh) command is issued when the asynchronous interface is enabled, the target's interface remains in asynchronous mode.

During or after t_{RST} , the host can poll each LUN's status register.

The RESET LUN (FAh) command is prohibited when not in the default array operation mode.

The RESET LUN (FAh) command can only be issued to a target (CE#) after the RESET (FFh) command has been issued as the first command to a target following power-up.

Figure 39: RESET LUN (FAh) Operation



HARD RESET (FDh)

The HARD RESET (FDh) command is used to put a particular die (LUN) on a target into a known condition similar to that of a power-on initialized state. The HARD RESET (FDh) command is accepted by only the LUN previously selected by a READ STATUS ENHANCED (78h) command. The host is required to issue a READ STATUS ENHANCED (78h) command prior to issuing the HARD RESET (FDh) command, there should be no other NAND commands after the READ STATUS ENHANCED (78h) command and before the HARD RESET (FDh) command issued by the host. The HARD RESET (FDh) command is only permitted to be issued when the selected LUN is not in a busy state (RDY = 1, ARDY = 1).

HARD RESET (FDh) performs a initialization to the die (LUN) similar to the initialization performed during the first RESET (FFh) command at device power-on. All target LUN parameters and configurations shall be initialized to default values. The target LUN is chosen by the host issuing a READ STATUS ENHANCED (78h) command prior



to issuing the HARD RESET (FDh) command. The HARD RESET (FDh) operation is completed within t_{POR} . After t_{POR} , the data register and cache register contents of the previously selected LUN that carried out the HARD RESET (FDh) operation are invalid.

In shared CE# configuration, only the selected LUN shall perform the HARD RESET (FDh) command. The host is required to issue the READ STATUS ENHANCED (78h) command prior to issuing the HARD RESET (FDh) command to select LUN to perform the HARD RESET (FDh) operation.

If in the NV-DDR or NV-DDR2 interface, issuing a HARD RESET (FDh) command will revert the NAND interface back to asynchronous mode and the timing mode is set to 0.

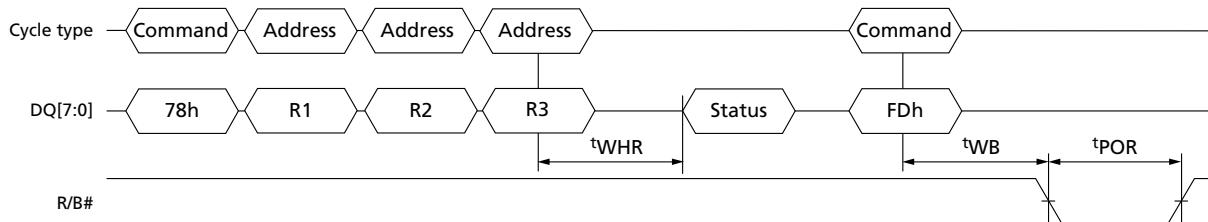
If the HARD RESET (FDh) command is issued when the asynchronous interface is enabled, the target's interface remains in asynchronous mode and timing mode is set to 0.

During or after t_{POR} , the host can poll each LUN's status register. A status command is only valid 5 μ s after HARD RESET (FDh) is issued, incorrect status may result if status command is issued within 5 μ s of HARD RESET (FDh) command.

The HARD RESET (FDh) command is prohibited when not in the default array operation mode.

The HARD RESET (FDh) command can only be issued to a target (CE#) after the RESET (FFh) command has been issued as the first command to a target following power-up. A HARD RESET (FDh) command will not change a device from the mirrored pinout configuration to the non-mirrored pinout configuration or change CE# pin reduction. A HARD RESET (FDh) command will change all feature addresses back to their default values for the target LUN with the exception of previously assigned volume configuration (feature address 58h).

Figure 40: HARD RESET (FDh) Operation



Identification Operations

READ ID (90h)

The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

When the 90h command is followed by a 00h address cycle, the target returns a 5-byte identifier code that includes the manufacturer ID, device configuration, and part-specific information.



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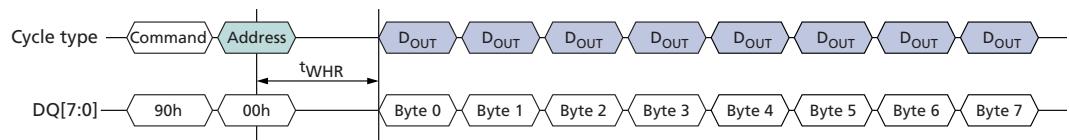
When the 90h command is followed by a 20h address cycle, the target returns the 6-byte ONFI identifier code.

When the 90h command is followed by a 40h address cycle, the target returns the 5-byte JEDEC identifier code.

After the 90h and address cycle are written to the target, the host enables data output mode to read the identifier information. When the asynchronous interface is active, one data byte is output per RE# toggle. When the NV-DDR interface is active, one data byte is output per rising edge of DQS when ALE and CLE are HIGH; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS. When the NV-DDR2 interface is active, one data byte is output per rising edge of DQS when ALE and CLE are LOW; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS.

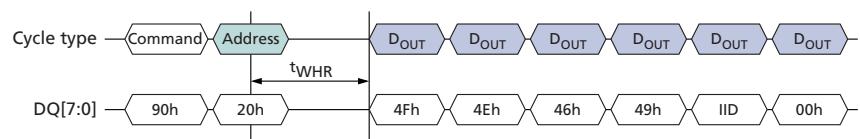
If host issues READ ID (90h) command during a program data load sequence, first the data load sequence must be closed and internal pipeline flushed with an 11h command prior to issuing the command.

Figure 41: READ ID (90h) with 00h Address Operation



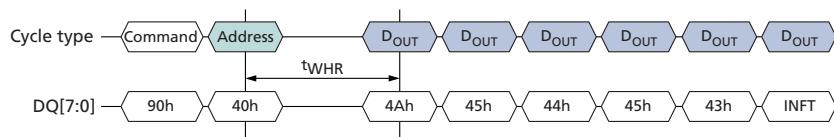
Note: 1. See the READ ID Parameter tables for byte definitions.

Figure 42: READ ID (90h) with 20h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.

Figure 43: READ ID (90h) with 40h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.



READ ID Parameter Tables

Table 8: Read ID Parameters for Address 00h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
MT29F128G08CBCEB	2Ch	84h	44h	34h	AAh	00h	00h	00h
MT29F256G08CECEB	2Ch	84h	44h	34h	AAh	00h	00h	00h
MT29F512G08CMCEB	2Ch	84h	44h	34h	AAh	00h	00h	00h

Note: 1. h = hexadecimal.

Table 9: Read ID Parameters for Address 20h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
MT29F128G08CBCEB	4Fh	4Eh	46h	49h	00h
MT29F256G08CECEB	4Fh	4Eh	46h	49h	00h
MT29F256G08CECEB	4Fh	4Eh	46h	49h	00h

Note: 1. h = hexadecimal.

Table 10: Read ID Parameters for Address 40h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
Asynchronous or synchronous	4Ah	45h	44h	45h	43h	05h

Note: 1. h = hexadecimal.



READ PARAMETER PAGE (ECh)

The READ PARAMETER PAGE (ECh) command is used to read the ONFI or JEDEC parameter page programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When the ECh command is followed by an 00h or 40h address cycle, the target goes busy for t^R . If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. Use of the READ STATUS ENHANCED (78h) command is prohibited while the target is busy and during data output.

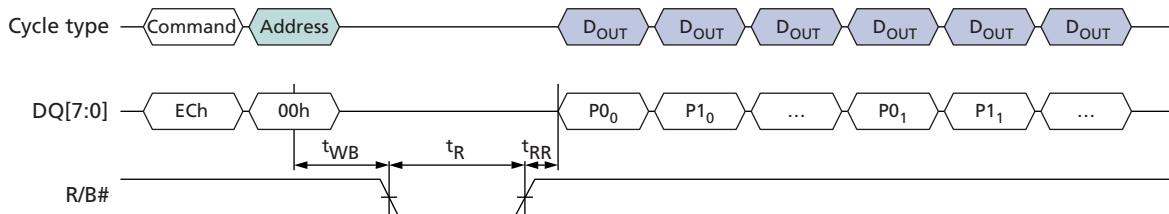
After t^R completes, the host enables data output mode to read the parameter page. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, one data byte is output for each rising or falling edge of DQS.

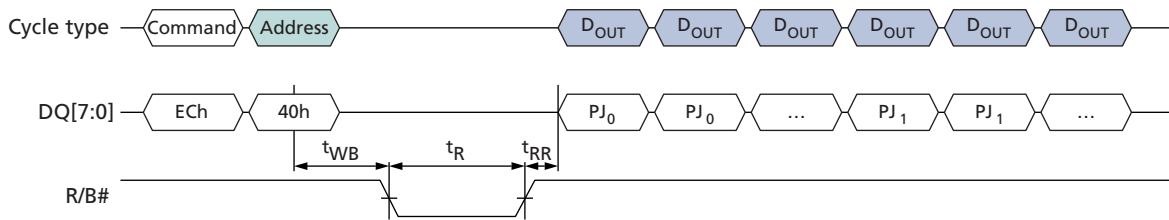
A minimum of three copies of the parameter page are stored in the device. Each parameter page is 256 bytes. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the location of data output. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h or 00h-05h-E0h) command is prohibited.

The READ PARAMETER PAGE (ECh) output data can be used by the host to configure its internal settings to properly use the NAND Flash device. Parameter page data is static per part, however the value can be changed through the product cycle of NAND Flash. The host should interpret the data and configure itself accordingly.

The host should continue reading redundant parameter pages until the host is able to accurately reconstruct the parameter page contents. Parameter pages returned by the target may have invalid CRC values; however, bit-wise majority may be used to recover the contents of the parameter page. The host may use bit-wise majority or other techniques to recover the contents of the parameter page from the parameter page copies present.

Figure 44: READ PARAMETER (ECh) with 00h Address Operation for ONFI



**Figure 45: READ PARAMETER (ECh) with 40h Address Operation for JEDEC**

Parameter Page Data Structure Tables

Table 11: ONFI Parameter Page Data Structure

Byte	Description	Device	Values
Revision information and features block			
0–3	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	-	4Fh, 4Eh, 46h, 49h
4–5	Revision number Bit[15:10]: Reserved (0) Bit 9: 1 = Supports ONFI version 4.0 Bit 8: 1 = Supports ONFI version 3.2 Bit 7: 1 = Supports ONFI version 3.1 Bit 6: 1 = Supports ONFI version 3.0 Bit 5: 1 = Supports ONFI version 2.3 Bit 4: 1 = Supports ONFI version 2.2 Bit 3: 1 = Supports ONFI version 2.1 Bit 2: 1 = Supports ONFI version 2.0 Bit 1: 1 = Supports ONFI version 1.0 Bit 0: Reserved (0)	-	FEh, 03h

**Table 11: ONFI Parameter Page Data Structure (Continued)**

Byte	Description	Device	Values
6–7	Features supported Bit15: supports Package Electrical Specification Bit 14: 1 = Supports ZQ calibration Bit 13: 1 = Supports NV-DDR3 Bit 12: 1 = Supports external V _{PP} Bit 11: 1 = Supports volume addressing Bit 10: 1 = Supports NV-DDR2 interface Bit 9: 0 = Reserved Bit 8: 1 = Supports program page register clear enhancement Bit 7: 1 = Supports extended parameter page Bit 6: 1 = Supports interleaved (multi-plane) read operations Bit 5: 1 = Supports NV-DDR interface Bit 4: 1 = Supports odd-to-even page copyback Bit 3: 1 = Supports interleaved (multi-plane) program and erase operations Bit 2: 1 = Supports non-sequential page programming Bit 1: 1 = Supports multiple LUN operations Bit 0: 1 = Supports 16-bit data bus width	-	F8h, 0Dh
8–9	Optional commands supported Bit[15:14]: Reserved (0) Bit 13: 1 = Supports ZQ calibration (long and short) Bit 12: 1 = Supports GET/SET FEATURES by LUN Bit 11: 1 = Supports ODT CONFIGURE Bit 10: 1 = Supports VOLUME SELECT Bit 9: 1 = Supports RESET LUN Bit 8: 1 = Supports small data move Bit 7: 1 = Supports CHANGE ROW ADDRESS Bit 6: 1 = Supports CHANGE READ COLUMN ENHANCED Bit 5: 1 = Supports READ UNIQUE ID Bit 4: 1 = Supports COPYBACK Bit 3: 1 = Supports READ STATUS ENHANCED Bit 2: 1 = Supports GET FEATURES and SET FEATURES Bit 1: 1 = Supports READ CACHE commands Bit 0: 1 = Supports PROGRAM PAGE CACHE	-	FEh, 17h
10	ONFI-JEDEC JTG primary advanced command support Bit[7:4]: Reserved (0) Bit 3: 1 = Supports ERASE BLOCK MULTI-PLANE Bit 2: 1 = Supports COPYBACK PROGRAM MULTI-PLANE Bit 1: 1 = Supports PROGRAM PAGE MULTI-PLANE Bit 0: 1 = Supports CHANGE READ COLUMN	-	0Fh
11	Reserved (0)	-	All 00h
12–13	Extended parameter page length	-	03h, 00h
14	Number of parameter pages	-	3Dh
15–31	Reserved (0)	-	All 00h
Manufacturer information block			

**Table 11: ONFI Parameter Page Data Structure (Continued)**

Byte	Description	Device	Values
32–43	Device manufacturer (12 ASCII characters) Micron	-	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44–63	Device model (20 ASCII characters)	MT29F128G08CBCEB	4Dh, 54h, 32h, 39h, 46h, 31h, 32h, 38h, 47h, 30h, 38h, 43h, 42h, 43h, 45h, 42h, 4Ah, 34h, 20h, 20h
		MT29F256G08CECEB	4Dh, 54h, 32h, 39h, 46h, 32h, 35h, 36h, 47h, 30h, 38h, 43h, 45h, 43h, 45h, 42h, 4Ah, 34h, 20h, 20h
		MT29F512G08CMCEB	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 43h, 4Dh, 43h, 45h, 42h, 4Ah, 34h, 20h, 20h
64	JEDEC manufacturer ID	-	2Ch
65–66	Date code	-	00h, 00h
67–79	Reserved (0)	-	All 00h
Memory organization block			
80–83	Number of data bytes per page	-	00h, 40h, 00h, 00h
84–85	Number of spare bytes per page	-	A0h, 08h
86–89	Number of data bytes per partial page	-	00h, 04h, 00h, 00h
90–91	Number of spare bytes per partial page	-	8Ah, 00h
92–95	Number of pages per block	-	00h, 02h, 00h, 00h
96–99	Number of blocks per LUN	-	90h, 08h, 00h, 00h
100	Number of LUNs per chip enable	-	01h
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	-	23h
102	Number of bits per cell	-	02h
103–104	Bad blocks maximum per LUN	-	60h, 00h
105–106	Block endurance	-	03h, 03h
107	Guaranteed valid blocks at beginning of target	-	01h
108–109	Block endurance for guaranteed valid blocks	-	00h, 00h
110	Number of programs per page	-	01h
111	Reserved (0)	-	00h
112	Number of bits ECC correctability	-	FFh

**Table 11: ONFI Parameter Page Data Structure (Continued)**

Byte	Description	Device	Values
113	Number of interleaved address bits Bit[7:4]: Reserved (0) Bit[3:0]: Number of interleaved address bits	-	02h
114	Interleaved operation attributes Bit[7:6]: Reserved (0) Bit 5: Reserved Bit 4: 1 = Supports read cache Bit 3: Address restrictions for cache operations Bit 2: 1 = Supports program cache Bit 1: 1 = No block address restrictions Bit 0: Overlapped/concurrent interleaving support	-	1Ah
115–127	Reserved (0)	-	All 00h
Electrical parameters block			
128	I/O pin capacitance per chip enable	-	00h
129–130	Asynchronous timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = Supports timing mode 5 Bit 4: 1 = Supports timing mode 4 Bit 3: 1 = Supports timing mode 3 Bit 2: 1 = Supports timing mode 2 Bit 1: 1 = Supports timing mode 1 Bit 0: 1 = Supports timing mode 0, shall be 1	-	3Fh, 00h
131–132	Reserved (0)	-	All 00h
133–134	^t PROG MAX program page time (μs)	-	B8h, 0Bh
135–136	^t BERS MAX block erase time (μs)	-	30h, 75h
137–138	^t R MAX page read time (μs)	-	4Eh, 00h
139–140	^t CCS MIN change column setup time (ns)	-	90h, 01h
141	NV-DDR timing mode support Bit[7:6]: Reserved (0) Bit 5: 1 = Supports timing mode 5 Bit 4: 1 = Supports timing mode 4 Bit 3: 1 = Supports timing mode 3 Bit 2: 1 = Supports timing mode 2 Bit 1: 1 = Supports timing mode 1 Bit 0: 1 = Supports timing mode 0	-	3Fh

**Table 11: ONFI Parameter Page Data Structure (Continued)**

Byte	Description	Device	Values
142	NV-DDR2 timing mode support Bit 7: 1 = Supports timing mode 7 Bit 6: 1 = Supports timing mode 6 Bit 5: 1 = Supports timing mode 5 Bit 4: 1 = Supports timing mode 4 Bit 3: 1 = Supports timing mode 3 Bit 2: 1 = Supports timing mode 2 Bit 1: 1 = Supports timing mode 1 Bit 0: 1 = Supports timing mode 0	-	FFh
143	NV-DDR/NV-DDR2 features Bit[7:4]: Reserved (0) Bit 3: 0 = Device does not require V _{PP} enablement sequence Bit 2: 1 = Devices support CLK stopped for data input Bit 1: 1 = Typical capacitance values present Bit 0: 0 = Use t _{CAD} MIN value	-	02h
144–145	CLK input pin capacitance, typical	MT29F128G08CBCEB MT29F256G08CECEB MT29F512G08CMCEB	23h, 00h 23h, 00h 1Eh, 00h
146–147	I/O pin capacitance, typical	MT29F128G08CBCEB MT29F256G08CECEB MT29F512G08CMCEB	10h, 00h 10h, 00h 10h, 00h
148–149	Input capacitance, typical	MT29F128G08CBCEB MT29F256G08CECEB MT29F512G08CMCEB	23h, 00h 23h, 00h 1Dh, 00h
150	Input pin capacitance, maximum	MT29F128G08CBCEB MT29F256G08CECEB MT29F512G08CMCEB	05h 05h 04h
151	Driver strength support Bit[7:3]: Reserved (0) Bit 2: 1 = Supports 18 ohm drive strength Bit 1: 1 = Supports 25 ohm drive strength Bit 0: 1 = Supports driver strength settings	-	03h
152–153	t _R MAX interleaved (multi-plane) page read time (μs)	-	50h, 00h
154–155	t _{ADL} program page register clear enhancement value (ns)	-	96h, 00h
156–157	Reserved (0)	-	All 00h
158	NV-DDR2/3 features Bit[7:6]: Reserved (0) Bit 5: 0 = External V _{REFQ} not required for ≥200 MT/s Bit 4: 1 = Supports differential signaling for DQS Bit 3: 1 = Supports differential signaling for RE# Bit 2: 1 = Supports ODT value of 30 ohms Bit 1: 1 = Supports matrix termination ODT Bit 0: 1 = Supports self-termination ODT	-	18h

**Table 11: ONFI Parameter Page Data Structure (Continued)**

Byte	Description	Device	Values
159	NV-DDR2/3 WARMUP cycles Bit[7:4]: Data input WARMUP cycles support Bit[3:0]: Data output WARMUP cycles support	-	44h
160–161	NV-DDR3 timing mode support Bit [15:8]: Reserved (0) Bit 7: 1 = Supports timing mode 10 Bit 6: 1 = Supports timing mode 9 Bit 5: 1 = Supports timing mode 8 Bit 4: 1 = Supports timing mode 7 Bit 3: 1 = Supports timing mode 6 Bit 2: 1 = Supports timing mode 5 Bit 1: 1 = Supports timing mode 4 Bit 0: 1 = Supports timing mode 0 to 3	-	00h, 00h
162	NV-DDR2 timing mode support Bit[7:3]: Reserved (0) Bit 2: 1 = Supports NV-DDR2 timing mode 10 Bit 1: 1 = Supports NV-DDR2 timing mode 9 Bit 0: 1 = Supports NV-DDR2 timing mode 8	-	01h
163	Reserved (0)	-	All 00h
Vendor block			
164–165	Vendor-specific revision number	-	02h, 00h
166	TWO-PLANE PAGE READ support Bit[7:1]: Reserved (0) Bit 0: 1 = Support for TWO-PLANE PAGE READ	-	01h
167	Read cache support Bit[7:1]: Reserved (0) Bit 0: 0 = No support Micron-specific READ CACHE function	-	00h
168	READ UNIQUE ID support Bit[7:1]: Reserved (0) Bit 0: 0 = No support Micron-specific READ UNIQUE ID	-	00h
169	Programmable DQ output impedance support Bit[7:1]: Reserved (0) Bit 0: 0 = No support for programmable DQ output impedance by B8h command	-	00h
170	Number of programmable DQ output impedance settings Bit[7:3]: Reserved (0) Bit [2:0] = Number of programmable DQ output impedance settings	-	03h
171	Programmable DQ output impedance feature address Bit[7:0] = Programmable DQ output impedance feature address	-	10h
172	Programmable R/B# pull-down strength support Bit[7:1]: Reserved (0) Bit 0: 1 = Support programmable R/B# pull-down strength	-	01h

**Table 11: ONFI Parameter Page Data Structure (Continued)**

Byte	Description	Device	Values
173	Programmable R/B# pull-down strength feature address Bit[7:0] = Feature address used with programmable R/B# pull-down strength	-	81h
174	Number of programmable R/B# pull-down strength settings Bit[7:3]: Reserved (0) Bit[2:0] = Number of programmable R/B# pull-down strength settings	-	04h
175	OTP mode support Bit[7:2]: Reserved (0) Bit 1: 1 = Supports GET/SET FEATURES command set Bit 0: 0 = No support A5h/A0h/AFh OTP command set	-	02h
176	OTP page start Bit[7:0] = Page where OTP page space begins	-	04h
177	OTP DATA PROTECT address Bit[7:0] = Page address to use when issuing OTP DATA PROTECT command	-	01h
178	Number of OTP pages Bit[15:5]: Reserved (0) Bit[4:0] = Number of OTP pages	-	1Bh
179	OTP Feature Address	-	90h
180	Read retry Options Bit[7:4]: Reserved (0) Bit[3:0] = Number of read retry options supported	-	10h
181–184	Read retry options available. A value of "1" in a bit position shows that read retry option is available for use. A value of "0" in a bit position shows that read retry option is not available for use. For example, the binary value of '37h, 00h, 00h, 00h' would represent that read retry options 0, 1, 2, 4, and 5 are available which would correspond to read retry input option selections of 00h, 01h, 02h, 04h, and 05h. It furthermore would show that read retry options 3, 6, and 7 to 32 which would correspond to read retry input option selections 03h, 06h, 07h to 20h, are not available.	-	FFh, FFh, 00h, 00h
185–249	Reserved (0)	-	All 00h
250–252	Designator bytes 1 to 3 (ASCII characters) Byte 250 = Designator byte 1, "R" Byte 251 = Designator byte 2 Byte 252 = Designator byte 3	-	52h, 00h, 00h
253	Parameter page revision	-	02h
254–255	Integrity CRC	MT29F128G08CBCEB	01h, 8Ah
		MT29F256G08CECEB	E7h, 20h
		MT29F512G08CMCEB	24h, 18h
Redundant parameter pages			

**Table 11: ONFI Parameter Page Data Structure (Continued)**

Byte	Description	Device	Values
256–511	Value of bytes 0–255	-	See bytes 0–255
512–767	Value of bytes 0–255	-	See bytes 0–255
...	...	-	...
15,104– 15,359	Value of bytes 0–255	-	See bytes 0–255
15,360– 15,615	Value of bytes 0–255	-	See bytes 0–255
Extended parameter pages			
15,616– 15,617	Extended parameter page Integrity CRC	-	5Eh, 94h
15,618– 15,621	Extended parameter page signature Byte 0: 45h, "E" Byte 1: 50h, "P" Byte 2: 50h, "P" Byte 3: 53h, "S"	-	45h, 50h, 50h, 53h
15,622– 15,631	Reserved (0)	-	All 00h
15,632	Section 0 type	-	02h
15,633	Section 0 length	-	01h
15,634– 15,647	Reserved (0)	-	All 00h
15,648	Number of bits ECC correctability	-	48h
15,649	ECC codeword size	-	0Ah
15,650– 15,651	Bad blocks maximum per LUN	-	60h, 00h
15,652– 15,653	Block endurance	-	03h, 03h
15,654– 15,663	Reserved (0)	-	All 00h
Redundant extended parameter pages			
15,664– 15,711	Value of bytes 15,616–15,663	-	See bytes 15,616– 15,663
15,712– 15,759	Value of bytes 15,616–15,663	-	See bytes 15,616– 15,663
...	...	-	...
18,448– 18,495	Value of bytes 15,616–15,663	-	See bytes 15,616– 15,663
18,496– 18,543	Value of bytes 15,616–15,663	-	See bytes 15,616– 15,663
18,544 to end of page	Reserved (FFh)	-	All FFh

**Table 12: JEDEC Parameter Page Definition**

Byte	Description	Device	Values
Revision information and features block			
0–3	Parameter page signature Byte 0: 4Ah, "J" Byte 1: 45h, "E" Byte 2: 53h, "S" Byte 3: 44h, "D"	-	4Ah, 45h, 53h, 44h
4–5	Revision number Bit[15:3]: Reserved (0) Bit 2: 1 = Supports JEDEC version 1.0 and standard revision 1.0 Bit 1: 1 = Supports vendor specific parameter page Bit 0: Reserved (0)	-	06h, 00h
6–7	Features supported Bit[15:9]: Reserved (0) Bit 8: 1 = Supports program page register clear enhancement Bit 7: 1 = Supports external V _{PP} Bit 6: 1 = Supports toggle mode DDR Bit 5: 1 = Supports synchronous DDR Bit 4: 1 = Supports MULTI-PLANE READ operations Bit 3: 1 = Supports MULTI-PLANE PROGRAM and ERASE operations Bit 2: 1 = Supports non-sequential page programming Bit 1: 1 = Supports multiple LUN operations Bit 0: 1 = Supports 16-bit data bus width	-	38h, 01h
8–10	Features supported Bit[23:11]: Reserved (0) Bit 10: 1 = Supports synchronous reset Bit 9: 1 = Supports reset LUN (Primary) Bit 8: 1 = Supports small data move Bit 7: 1 = Supports multi-plane copyback program (Primary) Bit 6: 1 = Supports random data out (Primary) Bit 5: 1 = Supports read Unique ID Bit 4: 1 = Supports copyback Bit 3: 1 = Supports read status enhanced (Primary) Bit 2: 1 = Supports get features and set features Bit 1: 1 = Supports READ CACHE commands Bit 0: 1 = Supports PAGE CACHE PROGRAM command	-	FEh, 07h, 00h
11–12	Secondary commands supported - Bit[15:8]: Reserved (0) Bit 7: 1 = supports secondary read status enhanced Bit 6: 1 = Supports secondary multi-plane block erase Bit 5: 1 = Supports secondary multi-plane copyback program Bit 4: 1 = Supports secondary multi-plane program Bit 3: 1 = Supports secondary random data out Bit 2: 1 = Supports secondary multi-plane copyback read Bit 1: 1 = Supports secondary multi-plane read cache random Bit 0: 1 = Supports secondary multi-plane read	-	58h, 00h

**Table 12: JEDEC Parameter Page Definition (Continued)**

Byte	Description	Device	Values
13	Number of parameter pages	-	24h
14–31	Reserved (0)	-	All 00h
Manufacturer information block			
32–43	Device manufacturer (12 ASCII characters) Micron	-	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44–63	Device model (20 ASCII characters)	MT29F128G08CBCEB	4Dh, 54h, 32h, 39h, 46h, 31h, 32h, 38h, 47h, 30h, 38h, 43h, 42h, 43h, 45h, 42h, 4Ah, 34h, 20h, 20h
		MT29F256G08CECEB	4Dh, 54h, 32h, 39h, 46h, 32h, 35h, 36h, 47h, 30h, 38h, 43h, 45h, 43h, 45h, 42h, 4Ah, 34h, 20h, 20h
		MT29F512G08CMCEB	4Dh, 54h, 32h, 39h, 46h, 35h, 31h, 32h, 47h, 30h, 38h, 43h, 4Dh, 43h, 45h, 42h, 4Ah, 34h, 20h, 20h
64–69	JEDEC manufacturer ID	-	2Ch, 00h, 00h, 00h, 00h, 00h
70–71	Reserved (0)	-	All 00h
72–79	Reserved (0)	-	All 00h
Memory organization block			
80–83	Number of data bytes per page	-	00h, 40h, 00h, 00h
84–85	Number of spare bytes per page	-	A0h, 08h
86–89	Number of data bytes per partial page	-	00h, 04h, 00h, 00h
90–91	Number of spare bytes per partial page	-	8Ah, 00h
92–95	Number of pages per block	-	00h, 02h, 00h, 00h
96–99	Number of blocks per LUN	-	90, 08h, 00h, 00h
100	Number of LUNs per chip enable	-	01h
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	-	23h
102	Number of bits per cell	-	02h
103	Number of programs per page	-	01h
104	Multi-plane operation addressing Bit[7:4]: Reserved (0) Bit[3:0]: Number of plane address bits	-	02h

**Table 12: JEDEC Parameter Page Definition (Continued)**

Byte	Description	Device	Values
105	Multi-plane operation attributes Bit[7:3]: Reserved (0) Bit 2: 1 = READ CACHE operations supported Bit 1: 1 = PROGRAM CACHE operations supported Bit 0: 1 = Address restrictions for cache operations	-	05h
106-143	Reserved (0)	-	All 00h
Electrical parameters block			
144-145	Asynchronous SDR speed grade support Bit[15:6]: Reserved (0) Bit 5: 1 = Supports timing mode 5 Bit 4: 1 = Supports timing mode 4 Bit 3: 1 = Supports timing mode 3 Bit 2: 1 = Supports timing mode 2 Bit 1: 1 = Supports timing mode 1 Bit 0: 1 = Supports timing mode 0, shall be 1	-	3Fh, 00h
146-147	Synchronous DDR2 speed grade support Bit[15:8]: Reserved (0) Bit 7: 1 = Supports timing mode 7 Bit 6: 1 = Supports timing mode 6 Bit 5: 1 = Supports timing mode 5 Bit 4: 1 = Supports timing mode 4 Bit 3: 1 = Supports timing mode 3 Bit 2: 1 = Supports timing mode 2 Bit 1: 1 = Supports timing mode 1 Bit 0: 1 = Supports timing mode 0, shall be 1	-	FFh, 00h
148-149	Synchronous DDR speed grade support Bit[15:6]: Reserved (0) Bit 5: 1 = Supports timing mode 5 Bit 4: 1 = Supports timing mode 4 Bit 3: 1 = Supports timing mode 3 Bit 2: 1 = Supports timing mode 2 Bit 1: 1 = Supports timing mode 1 Bit 0: 1 = Supports timing mode 0, shall be 1	-	3Fh, 00h
150	Asynchronous SDR features Bit[7:0]: Reserved (0)	-	00h
151	Reserved (0)	-	00h
152	Synchronous DDR features Bit[7:2]: Reserved (0) Bit 1: 1 = Devices leave CLK running for data input Bit 0: 0 = use tCAD MIN value	-	00h
153-154	t ^{PROG} MAX program page time (μs)	-	B8h, 0Bh
155-156	t ^{BERS} MAX block erase time (μs)	-	30h, 75h
157-158	t ^R MAX page read time (μs)	-	4Eh, 00h
159-160	t ^R MAX multi-plane page read time (μs)	-	50h, 00h

**Table 12: JEDEC Parameter Page Definition (Continued)**

Byte	Description	Device	Values
161–162	^t CCS MIN change column setup time (ns)	-	90h, 01h
163–164	I/O pin capacitance, typical	MT29F128G08CBCEB	10h, 00h
		MT29F256G08CECEB	10h, 00h
		MT29F512G08CMCEB	10h, 00h
165–166	Input capacitance, typical	MT29F128G08CBCEB	23h, 00h
		MT29F256G08CECEB	23h, 00h
		MT29F512G08CMCEB	1Dh, 00h
167–168	CLK input pin capacitance, typical	MT29F128G08CBCEB	23h, 00h
		MT29F256G08CECEB	23h, 00h
		MT29F512G08CMCEB	1Eh, 00h
169	Driver strength support Bit[7:3]: Reserved (0) Bit 2: 1 = Supports 18 ohm drive strength Bit 1: 1 = Supports 25 ohm drive strength Bit 0: 1 = Supports driver strength settings	-	03h
170–171	^t ADL program page register clear enhancement value (ns)	-	96h, 00h
172–207	Reserved (0)	-	00h
ECC and endurance block			
208	Guaranteed valid blocks at beginning of target	-	01h
209–210	Block endurance for guaranteed valid blocks	-	00h, 00h
211	Number of bits ECC correctability	-	48h
212	ECC codeword size	-	0Ah
213–214	Bad blocks maximum per LUN	-	60h, 00h
215–216	Block endurance	-	03h, 03h
217–218	Reserved (0)	-	All 00h
219–271	Reserved (0)	-	All 00h
Reserved			
272–419	Reserved (0)	-	All 00h
Vendor specific block			
420–421	Vendor-specific revision number	-	02h, 00h
422	Read retry Options Bit[7:4]: Reserved (0) Bit[3:0] = Number of read retry options supported	-	10h

**Table 12: JEDEC Parameter Page Definition (Continued)**

Byte	Description	Device	Values
423–426	Read retry options available. A value of "1" in a bit position shows that read retry option is available for use. A value of "0" in a bit position shows that read retry option is not available for use. For example, the binary value of '37h, 00h, 00h, 00h' would represent that read retry options 0, 1, 2, 4, and 5 are available which would correspond to read retry input option selections of 00h, 01h, 02h, 04h, and 05h. It furthermore would show that read retry options 3, 6, and 7 to 32 which would correspond to read retry input option selections 03h, 06h, 07h to 20h, are not available.	-	FFh, FFh, 00h, 00h
427–429	Designator Bytes 1 to 3 (ASCII characters) Byte 250 = Designator Byte 1, "R" Byte 251 = Designator Byte 2 Byte 252 = Designator Byte 3	-	52h, 00h, 00h
430–509	Reserved (0)	-	All 00h
CRC for Parameter Page			
510–511	Integrity CRC	MT29F128G08CBCEB	A7h, 26h
		MT29F256G08CECEB	90h, 46h
		MT29F512G08CMCEB	A5h, 43h
Redundant JEDEC Parameter Pages			
512–1023	See byte values 0–511	-	See bytes 0–511
1024–1535	See byte values 0–511	-	See bytes 0–511
...	...	-	...
17,408–17,919	See byte values 0–511	-	See bytes 0–511
17,920–18,431	See byte values 0–511	-	See bytes 0–511
18,432 to end of page	Reserved (FFh)	-	All FFh

Note: 1. h = hexadecimal.

READ UNIQUE ID (EDh)

The READ UNIQUE ID (EDh) command is used to read a unique identifier programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.



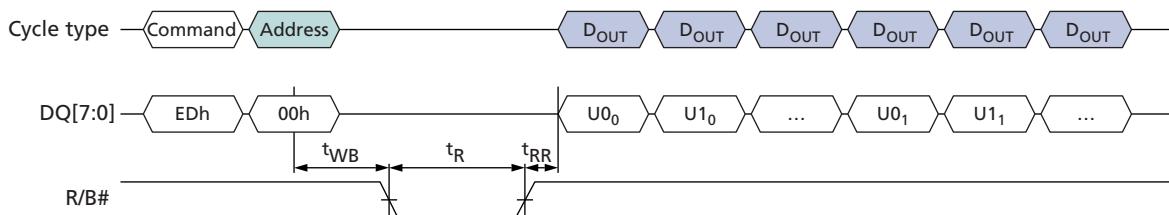
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When the EDh command is followed by a 00h address cycle, the target goes busy for t^R . If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

After t^R completes, the host enables data output mode to read the unique ID. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, two data bytes are output, one byte for each rising or falling edge of DQS.

Sixteen copies of the unique ID data are stored in the device. Each copy is 32 bytes. The first 16 bytes of a 32-byte copy are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. In the event that a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the data output location. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h) command is prohibited.

Figure 46: READ UNIQUE ID (EDh) Operation





Configuration Operations

The SET FEATURES (EFh) and GET FEATURES (EEh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which subfeature parameters will be read or modified. Each feature address (in the 00h to FFh range) is defined in Table 13. The SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command writes subfeature parameters (P1-P4) to the specified feature address. The GET FEATURES (EEh) or GET FEATURES by LUN (D4h) command reads the subfeature parameters (P1-P4) at the specified feature address.

Unless otherwise specified, the values of the feature addresses do not change when RESET (FAh, FFh, FCh) is issued by the host. A HARD RESET (FDh) command will reset all feature addresses to their default values for the target LUN. A HARD RESET (FDh) command will not undo any previously set electronic mirroring, CE# pin reduction, or volume addressing assignments that were performed prior to the HARD RESET (FDh) command.

Table 13: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h	NV-DDR2 configuration
03h–0Fh	Reserved
10h	Programmable output drive strength
11h–57h	Reserved
58h	Volume configuration
59h–7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable R/B# pull-down strength
82h–88h	Reserved
89h	Read retry
8Ah–8Fh	Reserved
90h	Array operation mode
91h	SLC MODE operation
92h–E5h	Reserved
E6h	Sleep mode
E7h	Temperature sensor
E8h–F4h	Reserved
F5h	Snap read/Express read
F6h	Sleep lite
F7h–FFh	Reserved



SET FEATURES (EFh)

The SET FEATURES (EFh) command writes the subfeature parameters (P1-P4) to the specified feature address to enable or disable target-specific features. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

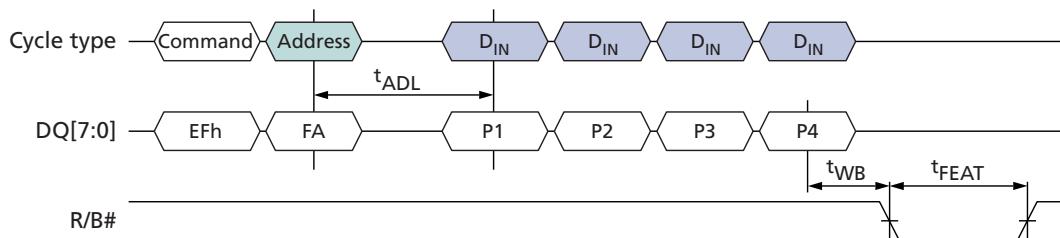
The SET FEATURES (EFh) command is followed by a valid feature address as specified in Table 13. The host waits for t_{ADL} before the subfeature parameters are input. When the asynchronous interface is active, one subfeature parameter is latched per rising edge of WE#. When the NV-DDR, or NV-DDR2 interface is active, one subfeature parameter is latched per rising edge of DQS_t. The data on the falling edge of DQS_t should be identical to the subfeature parameter input on the previous rising edge of DQS_t. The device is not required to wait for the repeated data byte before beginning internal actions.

After all four subfeature parameters are input, the target goes busy for t_{FEAT} , unless otherwise specified. The READ STATUS (70h) command can be used to monitor for command completion.

FEATURE ADDRESS 01h (Timing mode) operation is unique. If SET FEATURES is used to modify the interface type, the target will be busy for t_{ITC} . See Activating Interfaces for details.

If host issues SET FEATURES (EFh) command during a program data load sequence, first the data load sequence must be closed and internal pipeline flushed with an 11h command prior to issuing the command.

Figure 47: SET FEATURES (EFh) Operation



GET FEATURES (EEh)

The GET FEATURES (EEh) command reads the subfeature parameters (P1-P4) from the specified feature address. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

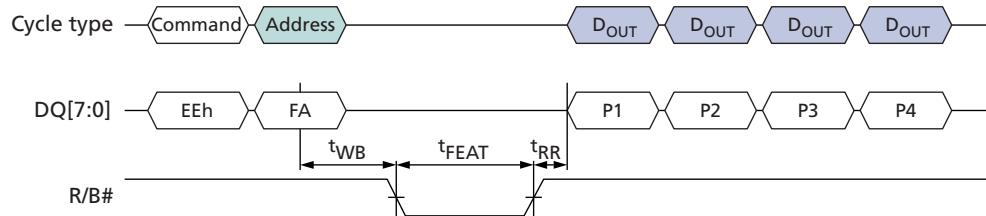
When the GET FEATURES (EEh) command is followed by a feature address, the target goes busy for t_{FEAT} , unless otherwise specified. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. During and prior to data output, use of the READ STATUS ENHANCED (78h) command is prohibited.



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After t_{FEAT} completes, the host enables data output mode to read the subfeature parameters. When the asynchronous interface is active, one data byte is output per RE# toggle. When the NV-DDR or NV-DDR2 interface is active, one subfeature parameter is output per DQS_t toggle on rising or falling edge of DQS_t.

Figure 48: GET FEATURES (EEh) Operation



GET/SET FEATURES by LUN (D4h/D5h)

The original GET FEATURES (EEh) and SET FEATURES (EFh) commands were target (CE#) based operations that did not take into account LUN addressing. By that, setting a feature address or getting a value for a feature address for a given target (CE#) applied to all LUNs on that target (CE#). GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) commands have the ability to also select a LUN address gives added flexibility to set the same feature address to different values for each LUN on a target (CE#) for more complex and versatile system solutions.

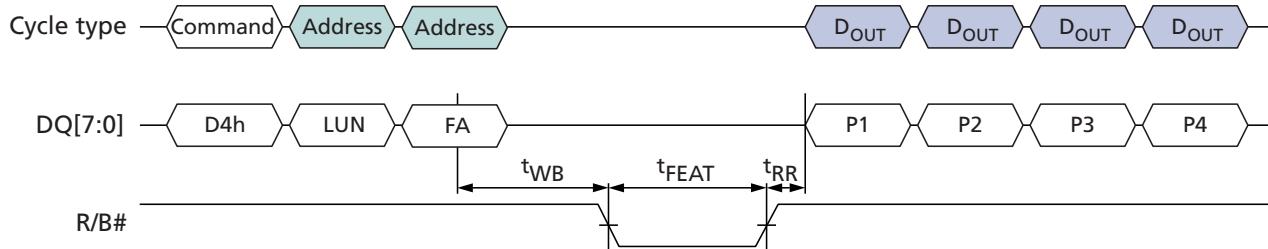
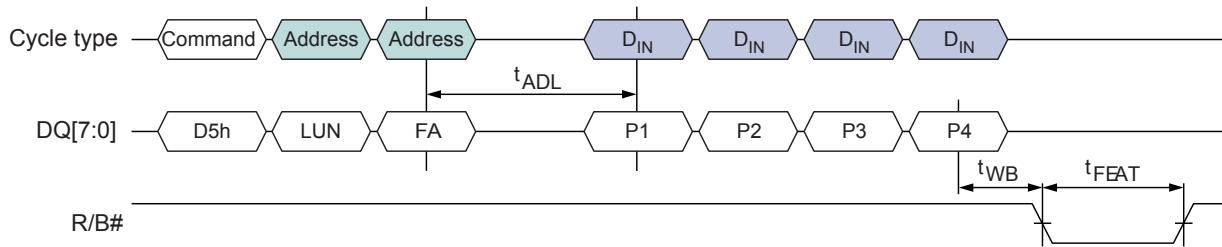
GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) operations work in the same manner as the non-LUN versions of those commands that did not take LUN addressing into account. The GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) commands both have an added LUN address cycle that is before the address cycle of the feature address which denotes the LUN to select for the operation. See Table 14 (page 85) for the decode of the LUN address cycle.

If host issues SET FEATURES by LUN (D5h) command during a program data load sequence, first the data load sequence must be closed and internal pipeline flushed with an 11h command prior to issuing the command.

Table 14: GET/SET FEATURES by LUN Operation LUN Address Cycle Decoding

Description	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
LUN											
LUN selection	LUN0								0	0b	
	LUN1								1	1b	
Reserved	-	-	-	-	-	-	-	-	-	-	

GET FEATURES by LUN (D4h) and SET FEATURES by LUN (D5h) can be issued to any addressable LUN that is not busy (RDY = 1, ARDY = 1). Target LUN status can be determined by using the READ STATUS ENHANCED (78h) command. When doing multiple LUN operations, refer to the Interleaved Die (Multi-LUN) Operation section for details on proper operations.

**Figure 49: GET FEATURES by LUN (D4h) Operation****Figure 50: SET FEATURES by LUN (D5h) Operation****Table 15: Feature Address 01h: Timing Mode**

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Timing mode	Mode 0 (default)					0	0	0	0	x0h	1, 2
	Mode 1					0	0	0	1	x1h	
	Mode 2					0	0	1	0	x2h	
	Mode 3					0	0	1	1	x3h	
	Mode 4					0	1	0	0	x4h	
	Mode 5					0	1	0	1	x5h	
	Mode 6					0	1	1	0	x6h	
	Mode 7					0	1	1	1	x7h	
	Mode 8					1	0	0	0	x8h	
	Mode 9					1	0	0	1	x9h	
	Mode 10					1	0	1	0	xAh	
	Reserved					1	x	x	x	Bh-Fh	
Data interface	Asynchronous (default)			0	0					0xh	1
	NV-DDR			0	1					1xh	
	NV-DDR2			1	0					2xh	
	Reserved			1	1					3xh	

**Table 15: Feature Address 01h: Timing Mode (Continued)**

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Program clear	PROGRAM command clears all cache registers on a target (default)		0							0b	
	PROGRAM command clears only the cache register of the selected plane of addressed LUN on a target		1							1b	
Reserved		0								0b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

- Notes:
1. Asynchronous timing mode 0 is the default, power-on value when the NAND device is powered-on with V_{CCQ} in the 1.8V operational range.
 2. If the NV-DDR or NV-DDR2 interface is active, a RESET (FFh) command will change the timing mode and data interface bits of FEATURE ADDRESS 01h to their default values. If the asynchronous interface is active, a RESET (FFh) command will not change the values of the timing mode or data interface bits to their default values. Transition from the NV-DDR interface to the NV-DDR2 interface or vice versa is not permitted.

**Table 16: Feature Address 02h: NV-DDR2 Configuration**

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Voltage reference (VEN)	External V _{REFQ} is disabled and internal voltage is used as reference for DQ signals (default)								0	0b	1
	External V _{REFQ} is enabled and used as reference for DQ signals								1	1b	2
Complementary DQS (CMPD)	DQS_c signal disabled (default)							0		0b	
	DQS_c signal enabled							1		1b	2
Complementary RE# (CMPR)	RE_c signal disabled (default)					0				0b	
	RE_c signal enabled					1				1b	2
Reserved	—					0				0b	
P2											
Warmup RE_t/RE_c and DQS cycles for data output	0 cycles (default)					0	0	0	0	0h	3
	1 WARMUP cycle					0	0	0	1	1h	2
	2 WARMUP cycles					0	0	1	0	2h	2
	4 WARMUP cycles					0	0	1	1	3h	2
	4 WARMUP cycles					0	1	0	0	4h	2
	Reserved					0	1	0	1	5h	
						0	1	1	0	6h	
						0	1	1	1	7h	
						1	X	X	X	8h–Fh	



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Table 16: Feature Address 02h: NV-DDR2 Configuration (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Warmup DQS cycles for data input	0 cycles (default)	0	0	0	0					0h	4
	1 WARMUP cycle	0	0	0	1					1h	2
	2 WARMUP cycles	0	0	1	0					2h	2
	4 WARMUP cycles	0	0	1	1					3h	2
	4 WARMUP cycles	0	1	0	0					4h	2
	Reserved	0	1	0	1					5h	
		0	1	1	0					6h	
		0	1	1	1					7h	
		1	X	X	X					8h–Fh	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

- Notes:
- If set to one, then external V_{REFQ} is used as a reference for the input and I/O signals. If cleared to zero, then internal V_{REFQ} is used as a reference for the input and I/O signals. This setting applies to input and I/O signals, including DQ[7:0], DQS_t, DQS_c, RE_t, RE_c, WE#, ALE, and CLE. CE# and WP# are CMOS signals and always use internal V_{REFQ} .
 - If the NV-DDR2 interface is active, a RESET (FFh) command will change the bit values FEATURE ADDRESS 02h to their default values, but SYNCHRONOUS RESET (FCh) and RESET LUN (FAh) will not.
 - Number of WARMUP cycles for DQS and RE_t/RE_c and DQS_t/DQS_c for data output. The number of initial "dummy" RE_t/RE_c cycles at the start of data output operations. There are corresponding "dummy" DQS_t/DQS_c cycles to the "dummy" RE_t/RE_c cycles that the host shall ignore during data output.
 - This field indicates the number of WARMUP cycles of DQS that are provided for data input. These are the number of initial "dummy" DQS_t/DQS_c cycles at the start of data input operations.

Table 17: Feature Address 58h: Volume Configuration

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Volume address	Field used to assign a value for a given volume address					X	X	X	X		1

**Table 17: Feature Address 58h: Volume Configuration (Continued)**

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Reserved	-	0	0	0	0					0h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. After the volume address is appointed, the ENo pin for that volume is set to one, the ENi pin for that volume is ignored until the next power cycle, and the volume is deselected until a VOLUME SELECT (E1h) command is issued that selects the associated volume. The host shall only set this feature once per power cycle for each volume. The address specified is then used in VOLUME SELECT (E1h) command for accessing this NAND target. This setting is retained across RESET (FAh, FCh, FFh) commands. A HARD RESET (FDh) command will not undo any previously set volume addressing assignments that were performed prior to the HARD RESET (FDh) command.

Table 18: Feature Addresses 10h and 80h: Programmable Output Drive Strength

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Output drive strength	Not supported								0	0	00h
	25 ohms								0	1	01h
	35 ohms (default)								1	0	02h
	50 ohms								1	1	03h
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. See Output Drive Impedance for details.

**Table 19: Feature Address 81h: Programmable R/B# Pull-Down Strength**

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
R/B# pull-down strength	Full (default)							0	0	00h	1
	Three-quarter							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

Table 20: Feature Addresses 89h: Read Retry

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Read Retry	Disable (default)					0	0	0	0	00h	
	Option 1					0	0	0	1	01h	
	Option 2					0	0	1	0	02h	
	Option 3					0	0	1	1	03h	
	Option 4					0	1	0	0	04h	
	Option 5					0	1	0	1	05h	
	Option 6					0	1	1	0	06h	
	Option 7					0	1	1	1	07h	
	Option 8					1	0	0	0	08h	2
	Option 9					1	0	0	1	09h	
	Option 10					1	0	1	0	0Ah	
	Option 11					1	0	1	1	0Bh	
	Option 12					1	1	0	0	0Ch	
	Option 13					1	1	0	1	0Dh	
	Option 14					1	1	1	0	0Eh	
	Option 15					1	1	1	1	0Fh	

**Table 20: Feature Addresses 89h: Read Retry (Continued)**

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Reserved		0	0	0	0					00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:

1. See Read Retry Operation for details.
2. tR will be longer with selected option. See Electrical Specifications – Array Characteristics section for details.

Table 21: Feature Address 90h: Array Operation Mode

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Array operation mode	Normal (default)								0	00h	
	OTP block								1	01h	1
Reserved		0	0	0	0	0	0	0		00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:

1. See One-Time Programmable (OTP) Operations for details.
2. A RESET (FFh) command will cause the bits of the array operation mode to change to their default values. If in NV-DDR/NV-DDR2 mode, a SYNCHRONOUS RESET (FCh) command will cause the bits of the array operation mode to change to their default values. The HARD RESET (FDh) command is prohibited when not in the default array operation mode.

**Table 22: Feature Address E6h: Sleep Mode**

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Sleep mode	Sleep mode disabled (default)								0	0b	
	Sleep mode enabled								1	1b	
Reserved	-	-	-	-	-	-	-	-			
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Sleep mode is a power state in which the LUNs power consumption is minimal. The trade off for this functionality is longer wake up duration from the sleep state.

The die (LUN) will retain its entire configuration (including set feature settings, RV level values, and so forth.) during sleep mode, but does not retain the contents of the cache or data registers.

Sleep mode is enabled by issuing a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to FEATURE ADDRESS E6h. After the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command is issued, the target (CE#) or target LUN will enter sleep mode upon bringing CE# HIGH.

During sleep mode, upon asserting CE# LOW, the LUN will exit the mode and change state to normal mode. The transition period between sleep mode and normal mode shall be less than t_{SLP} . After the transition, the LUN will move to normal ready mode and be ready to receive commands.

For a configuration of more than one LUN sharing the same CE# (or volume address), if SET FEATURES (EFh) command is used to enter sleep mode, the shared LUNs shall jointly enter/exit to/from sleep mode. All LUNs on a target (CE#) shall monitor in parallel the SET FEATURES (EFh) or SET FEATURE by LUN (D5h) command to enter the mode. As CE# is shared, upon asserting the signal, all LUNs on a target shall exit from sleep mode.

It is not required to have all targets (CE#s) of a NAND device enabled for sleep mode. A host can have as little as LUN enabled for sleep mode. When used with volume addressing, sleep mode can only be enabled on a single volume at a time.

Once sleep mode is entered, the host is required to keep the NAND device in sleep mode for a minimum time of 1μs before exiting sleep mode.

The host shall not issue any commands with exception of RESET (FFh, FAh, FCh, FDh) between issuing the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command



to enable sleep mode (FEATURE ADDRESS E6h) and bringing CE# HIGH to enter sleep mode.

If a RESET (FFh, FAh, FCh, FDh) command is issued to the target (CE#) or LUN after a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to enable sleep mode is issued, but before CE# goes HIGH, the target (CE#) or LUN will not enter sleep mode upon CE# HIGH. In other words, the setting for sleep mode is not retained across RESET (FFh, FAh, FCh, FDh) operations.

When exiting sleep mode, CE# shall be asserted LOW for a minimum of t_{CE_SLP} .

When exiting sleep mode, the host is required to wait t_{SLP} before issuing any commands (including RESET) to the device. During t_{SLP} period the device may draw significantly more current than I_{SB} even when CE# is HIGH.

Table 23: Sleep Mode Parameters

Parameter	Min	Max	Units
t_{SLP}	–	50	μs
t_{CE_SLP}	–	1.5	μs
CE# LOW exiting sleep	200	–	ns
I_{SB_SLEEP}	–	75	μA
I_{SBQ_SLEEP}	–	50	μA

Sleep mode entry/exit required method:

1. Issue a SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to FEATURE ADDRESS E6h with subfeature P1 = 1h to enable sleep mode entry.
2. CE# is brought HIGH after sleep mode entry and the NAND target (CE#) enters sleep mode.
3. CE# is brought LOW to exit sleep mode. Sleep mode entry is cleared (for example, DQ0 of subfeature P1 of FEATURE ADDRESS E6h is automatically cleared).
4. During the t_{SLP} time allowed for the NAND target to return to normal mode from sleep mode, no commands (including RESET) are allowed to the target.
5. To re-enter sleep mode the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to FEATURE ADDRESS E6h with subfeature P1 = 1h to enable sleep mode entry must be issued again.

**Table 24: Feature Address E7h: Temperature Sensor Readout**

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Temperature sensor readout	-37°C example output		0	0	0	0	0	0	0	00h	1, 2
	-35.8°C example output		0	0	0	0	0	0	1	01h	
	-	X	X	X	X	X	X	X	-		
	89°C example output		1	1	0	1	0	0	1	69h	
	90.2°C example output		1	1	0	1	0	1	0	6Ah	
	Reserved	-	-	-	-	-	-	-	-	6Bh-7Fh	
Reserved		0								0b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

- Notes:
1. Each bit is roughly 1.2°C. For example, an output of 55h is roughly 65°C.
 2. Device reading out temperature beyond specified operational temperature ranges for a given device is not meant to signify support of those temperatures.

Only a GET FEATURES (EEh) or GET FEATURES by LUN (D4h) commands are permitted to FEATURE ADDRESS E7h, SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands are not supported to FEATURE ADDRESS E7h. The temperature sensor shall return the current temperature value no more than tTEMP after the host controller issues the GET FEATURES (EEh) or GET FEATURES by LUN (D4h) command to FEATURE ADDRESS E7h. GET FEATURES (EEh) and GET FEATURES by LUN (D4h) commands are not supported to FEATURE ADDRESS E7h when the target (CE#) or target LUN is in any busy state.

If there is only 1 LUN per CE# of a NAND device, then either the GET FEATURES (EEh) or GET FEATURES by LUN (D4h) command can be used to access the temperature sensor readout (FEATURE ADDRESS E7h). If there is more than one LUN per CE#, then the GET FEATURES by LUN (D4h) command shall be used to access the temperature sensor readout (FEATURE ADDRESS E7h), not the GET FEATURES (EEh) command, to avoid possible data contention.

**Table 25: Temperature Sensor Readout Parameter**

Parameter	Symbol	Min	Max	Units
Busy time for GET FEATURES operation for temperature sensor readout	t_{TEMP}	–	120	μs

Table 26: Feature Address F5h: Snap Read/Express Read

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Snap read/Express read enable	Reserved								0	0b	
	Snap read/Express read disable (default)						0	0		00b	
	Express read enable						0	1		01b	
	Snap read enable						1	1		11b	
	Reserved	0	0	0	0	0				00000b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

FEATURE ADDRESS F5h: Snap read/Express read controls two different feature configurations. The snap read feature provides fastest possible read of a partial page. The express read feature allows the host to begin clocking out data before the read command has fully completed, also allowing for faster t_R for READ operations with internal NAND randomizer disabled. A snap read includes express read functionality.

Note that snap read cannot be used in conjunction with the NAND internal data randomizer. If performing a snap read from a page that has been programmed with the NAND internal randomizer enabled, indeterminate data will be output.

The snap read feature allows for a fixed 8KB+ section of a page to be read, providing fastest possible t_R times.

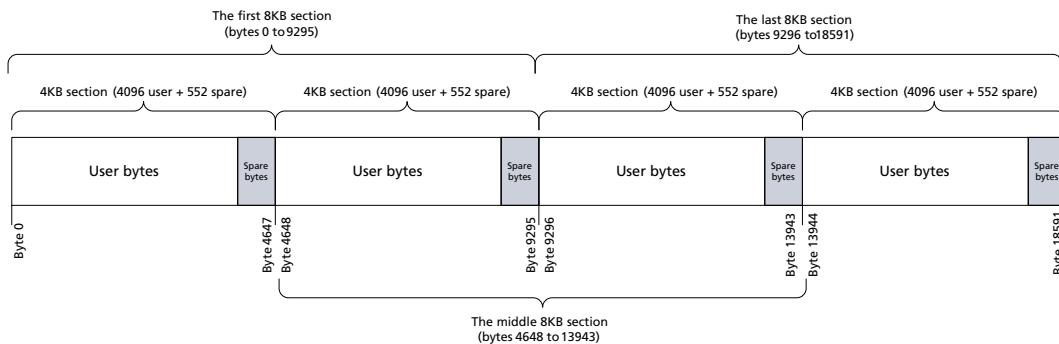
When the snap read feature is enabled, all READ operations will occur within a fixed 8K + section of a page. The page has 3 fixed 8KB+ logical sections: bytes 0–9295, bytes 4648–13943, and bytes 9296–18591 (each section contains 2×4 KB sections plus $2 \times \frac{1}{4}$ of the spare area bytes). When any read command is issued, the byte address specified by the command will determine which section of the page to be read. It is not necessary to address the first byte in a particular section during a READ operation. Addressing any



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byte within the first 4KB+ section (bytes 0–4647) will activate the first 8KB+ section (bytes 0–9295); Addressing any byte within the second 4KB+ section (bytes 4648–9295) will activate the middle 8KB+ section (bytes 4648–13943); Addressing any byte within the third or fourth 4KB+ sections (bytes 9296–13843 or bytes 13944–18591) will activate the last 8KB+ section (bytes 9296–bytes 18591). When using the NV-DDR2 interface, CA0 is forced to 0 internally, so start byte address is always an even byte. Data will be invalid for byte addresses not included in the selected 8KB+ section of the page.

Figure 51: Example of Fixed 8kB+ Length Sections



Snap read is only performed if READ PAGE (00h-30h) or COPYBACK READ (00h-35h) is issued to the device. If READ PAGE CACHE RANDOM (00h-31h), READ PAGE CACHE SEQUENTIAL (31h), READ PAGE CACHE LAST (3Fh), READ PAGE MULTI-PLANE (00h-32h), or FEATURE ADDRESS 89h: Read retry options selected that has a longer t_R time are issued to the device, the snap read is not executed and the commands issued are executed.

Snap read is not supported if reading from a page where not all shared pages have been programmed (for example, not in full MLC "4" state). In this case, undetermined data will result.

Snap read is supported in erase suspend or program suspend state.

Snap read should not be used to check for bad blocks when building a bad block table.

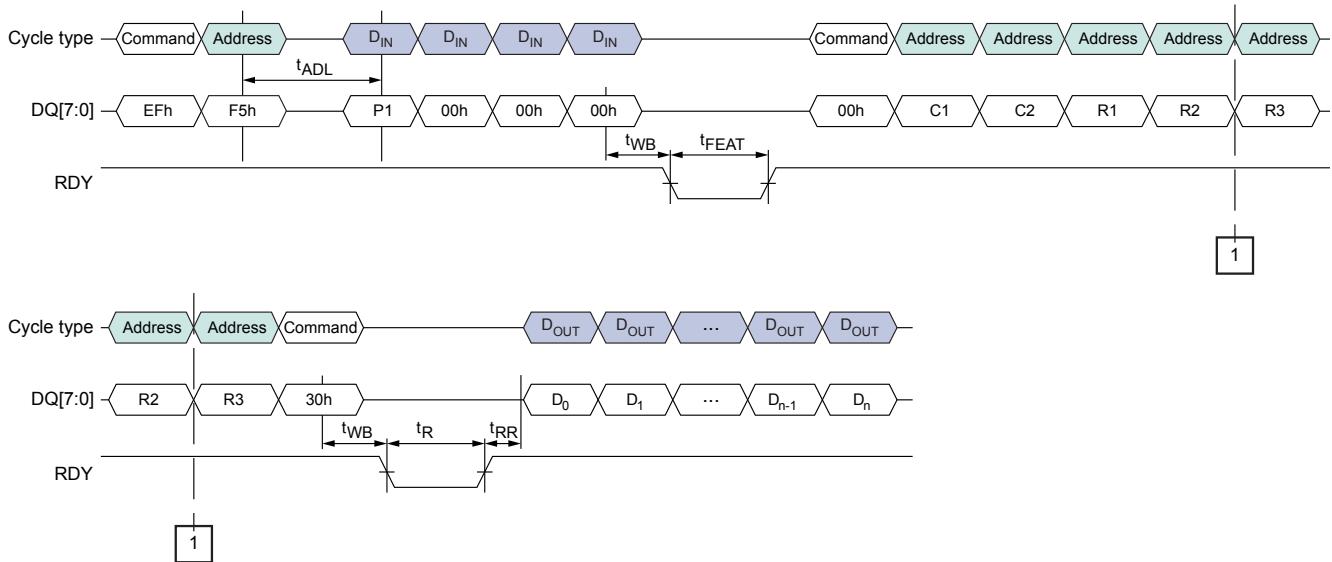
Snap read is only supported in the case of SINGLE-PLANE READ operations.

READ UNIQUE ID (EDh), READ OTP PAGE, and READ PARAMETER PAGE (ECh) commands are issued to the device the snap read is not executed and the commands are executed.

Snap read incorporates the express read feature, so any express read requirements must also be met for snap read.



Figure 52: Example of Snap Read Sequence



Note: 1. Byte address of data byte D₀ is defined by the byte addressed by C1 and C2.

The express read feature allows the host to begin clocking data out of the part once the data in the data register becomes valid. This will happen before the entire read algorithm is completed, thus reducing the apparent 'R time for READ operations with internal NAND randomizer disabled. Before any additional array commands can be issued the entire read algorithm must be completed. Express read is not optimized to provide 'R savings with WL flag status read enabled.

When the express read feature is enabled the host must monitor the status register using either READ STATUS (70h) or READ STATUS ENHANCED (78h) commands. Status register bit 6 ('RDY') will provide a method for the host to determine when data can begin being clocked out of the device. Status register bit 5 ('ARDY') will remain LOW until the entire read algorithm has been completed. The host must not issue any additional array operations until status register bit 5 is ready. In addition to READ STATUS (70h/78h) and RESET (FFh/FCh/FAh) commands, the host is allowed to issue the CHANGE READ COLUMN (05h-E0h), CHANGE READ COLUMN ENHANCED (06h- E0h/00h-05h-E0h), READ PAGE CACHE SEQUENTIAL (31h), READ PAGE CACHE RANDOM (00h-31h), READ PAGE CACHE LAST (3Fh), READ PAGE MULTI-PLANE (00h-32h), PAGE READ (00h-30h), and READ MODE (00h) commands when status register bit 5 ('ARDY') is LOW and status register bit 6 ('RDY') is HIGH during express read.

Express read may be enabled for any read command, but in some cases express read will not be executed and no 'R improvement witnessed. If express read is enabled during READ PAGE CACHE RANDOM (00h-31h), READ PAGE CACHE SEQUENTIAL (31h), READ PAGE CACHE LAST (3Fh), or FEATURE ADDRESS 89h: READ RETRY options selected that has a longer 'R time, Express read will not be executed and no 'R improvement witnessed.



Figure 53: Example of Express Read Sequence

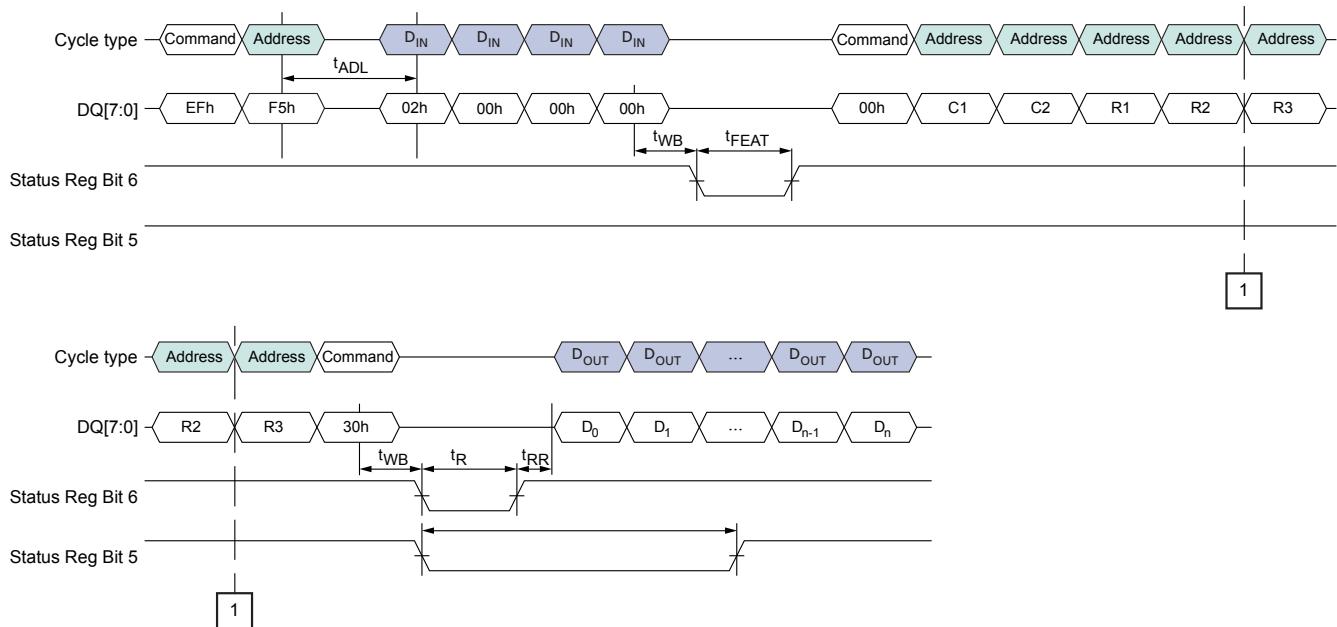


Table 27: Feature Address F6h: Sleep Lite

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Sleep light configuration	Sleep lite disable (default)							0	0	00b	
	Sleep lite enable							0	1	01b	
	Sleep lite - target level enable							1	1	11b	
	Reserved	-	-	-	-	-	-				
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

The sleep lite feature allows the host to place unselected LUNs on an active target (CE#) into a low power state to reduce overall I_{CC} where the current consumption by any LUN in sleep lite will be I_{SB} and I_{SBQ}. This feature only applies to NAND targets where more



than one LUN exists per CE#. Once a LUN has been placed in sleep lite mode it is unable to accept any host commands.

The sleep lite feature will allow for any number of LUNs within a selected target to be placed in a low power state through the use of the SET FEATURES by LUN (D5h) command. When multiple LUNs within a target are to remain active the host will need to issue a SET FEATURES by LUN (D5h) command to each LUN that is to be put into sleep lite mode. In the event that the host only wants a single LUN to be active (all other LUNs to be placed into sleep lite mode) two different methods exist. The host could issue SET FEATURES by LUN (D5h) commands to each LUN on the target as suggested in the method 1 example. An alternative solution would be for the host to use a target level SET FEATURES (EFh) command with the sleep lite - target level enable (P1 = 11b) option as suggested in the method 2 example.

Method 1 for a 2 LUN per CE# Configuration Example:

1. Issue SET FEATURE by LUN (D5h) command to LUN0 to enable sleep lite (P1 = 01b)
2. LUN0 is in sleep lite mode. LUN1 remains active.

Method 2 for a 2 LUN per CE# Configuration Example:

1. LUN1 is selected (could be done using READ STATUS ENHANCED (78h) command or other means)
2. Issue SET FEATURE (EFh) command to enable sleep lite - target level (P1 = 11b)
3. LUN0 enters sleep lite mode. LUN1 remains active.

Because LUNs in sleep lite mode cannot accept host commands the only method for exiting sleep lite mode is by toggling CE#.

Since LUNs in sleep lite cannot accept commands, if GET FEATURE by LUN (D4h) command is issued to a LUN in sleep lite there will be no response. If a GET FEATURE (EEh) command is issued to a target, the target response will only be from the LUNs that are not in sleep lite and the GET FEATURES (EEh) returned data will specify not in sleep lite (P0 = 00h), hence there is no way to check if any of the LUNs on the target are in sleep lite.

SLC Operations

This NAND Flash device supports SLC Operations, within defined limitations. SLC Operations allow the NAND array blocks in this MLC (2 bit per cell) device to operate in a SLC (1 bit per cell) mode.

Configuration using SET FEATURES

The host can enable SLC Mode of operations through the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) commands. The number of bits per cell configuration is available in Feature Address 91h. When using SET FEATURES (EFh) or SET FEATURES by LUN (D5h) commands to enable/disable SLC Mode operations, use of SLC MODE ENABLE (DAh) and SLC MODE DISABLE (DFh) commands to enable/disable SLC Mode operations is prohibited.

**Table 28: Feature Address 91h: SLC Mode Enable**

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Bits per cell	1							0	0	00h	1
	Reserved							0	1	01h	
	2 (default)							1	0	02h	
	Reserved							1	1	03h	
Reserved	-	0	0	0	0	0					
P2											
Required	Required	0	0	0	0	0	0	0	1	01h	2
P3											
Reserved	-	0	0	0	0	0	0	0	0	00h	
P4											
Reserved	-	0	0	0	0	0	0	0	0	00h	

Notes:

1. The default option is 2 bits per cell (P1[DQ7:DQ0] = 02h).
2. P2 Subfeature is required to have a non-zero data entry (P2[DQ7:DQ0] = 01h).

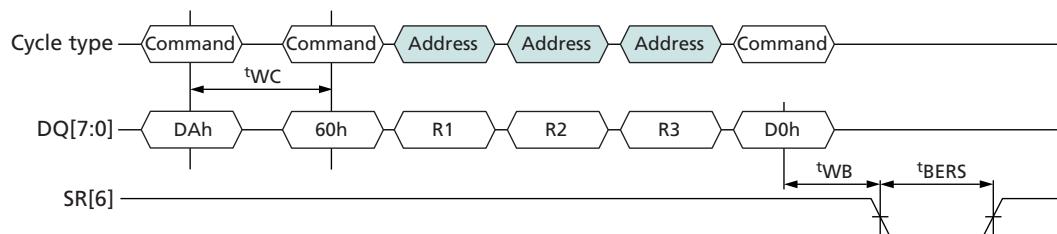
Configuration using Commands (DAh, DFh)

An alternative method to enable SLC Mode operations is through the use of the SLC MODE ENABLE (DAh) and SLC MODE DISABLE (DFh) commands. When using SLC MODE ENABLE (DAh) and SLC MODE DISABLE (DFh) commands to enable/disable SLC Mode operations, use of SET FEATURES (EFh) or SET FEATURES by LUN (D5h) commands to enable/disable SLC Mode operations is prohibited.

The SLC MODE ENABLE (DAh) command is issued prior to issuing an array operation command. All LUNs on the Target that were not busy when the SLC MODE Enable command was issued will enter and will remain in SLC Mode of operation until the SLC MODE DISABLE (DFh) command is issued. If not busy all LUNs on the Target will revert to the default mode of operation (for example, MLC) when the SLC MODE DISABLE (DFh) command is issued.

After an SLC MODE ENABLE (DAh) command is issued, a RESET (FFh/FCh/FAh) command will not cause the device to revert to its default mode of operation. However, a HARD RESET (FDh) command will cause the device to revert to its default mode of operation.

Figure 54: Block Erase Operation with SLC MODE ENABLE (DAh) Command Example





SLC/MLC Mode Operations

When in SLC mode, within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (for example, 0, 1, 2, 3, ...). Programming pages out of order within a block is prohibited.

The device itself does not maintain any tracking of which blocks have been designated as either default mode operational blocks or SLC blocks. Therefore, the host controller must keep track of which blocks have been used in SLC mode. Furthermore, the host must be aware of what mode the device is currently operating in.

Any block that is being changed from its default mode of operation must be "initialized" with an erase command in the SLC mode. After completion of the erase command, the host can then issue program operations in SLC mode to the previously erased NAND block. To properly "initialize" a block for SLC MODE, the host must first ensure that the block has at least 50% of the pages programmed (either in default mode or in SLC mode) before issuing the first SLC MODE erase. This includes "initialization" if the block is put into the SLC MODE immediately upon first cycle. Micron initializes all blocks with a default mode erase as the last manufacturing step, so the SLC block must be properly "initialized". Any time the device is used in the default mode prior to SLC MODE, the user must ensure that at least 50% of the pages are programmed before the first SLC MODE erase.

Once a NAND block is used in an array operation (PROGRAM/ERASE) in SLC mode, it is not permitted to use that NAND block in the default mode from that point forward. All future array operations on that block must be performed in SLC mode. If a NAND block is used in an array operation (PROGRAM/ERASE) in default mode, it may be changed to be an SLC block if the change occurs within the first 300 PROGRAM/ERASE cycles of that block's use. It is the responsibility of the controller to keep track of how many cycles have occurred.

It is imperative that the device is in the corresponding mode that a given block has been designated as. This applies to all PROGRAM, ERASE, and READ sequences. Mixing pages of different modes within a block is prohibited.

Programming a page in a block which was programmed in SLC mode while in default mode, or vice versa, will result in the data corruption.

The host must ensure that it does not mix MLC and SLC modes during any single operation. For example, the host cannot cache pages from blocks in SLC and the default mode in the same Random Read Cache (00h-31h) operation. The host has to wait until an operation on a block in the default mode is complete before starting an operation on a block in SLC mode and vice versa.

When performing multi-plane operations, all the blocks which are being accessed must be in the same mode (for example, SLC or default mode).

If the host controller uses a structured data pattern to program a page or pages of a NAND block when in SLC mode, then the NAND host is required to appropriately randomize the data and program the entire page length (for example, all columns) even if beyond the user data.



VOLUME SELECT (E1h)

The VOLUME SELECT function is used to select a particular volume based on the address specified. VOLUME SELECT (E1h) command is required to be used when CE# pin reduction is used.

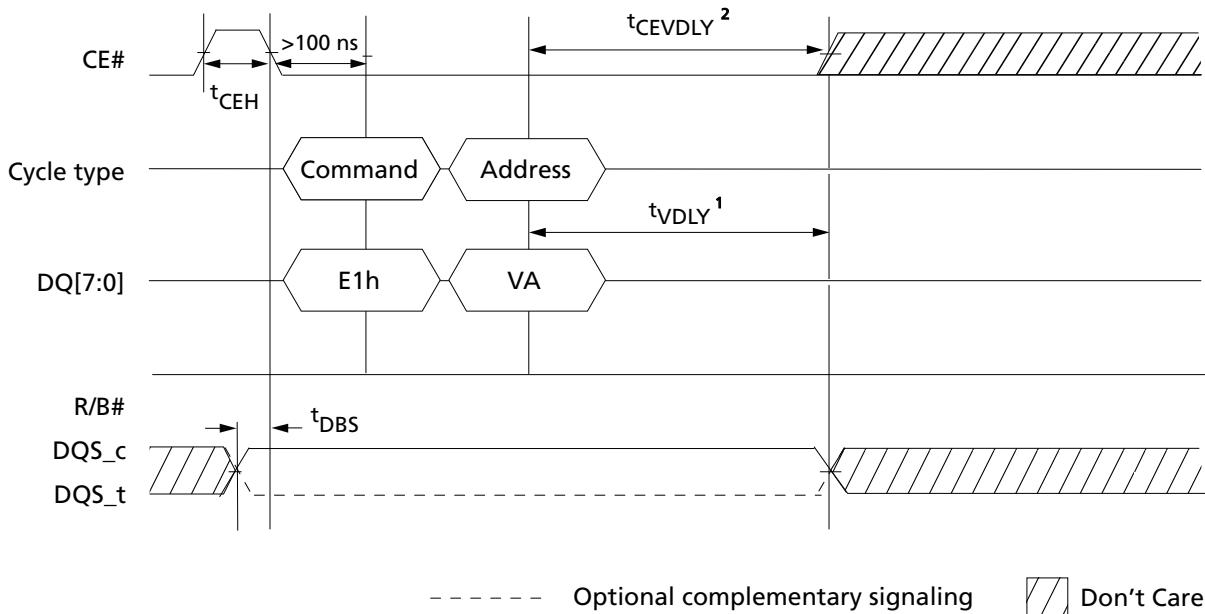
This command is accepted by all targets that share a particular CE# pin. The command may be executed with any LUN on the volume in any state. The VOLUME SELECT (E1h) command may only be issued as the first command after CE# is pulled LOW; CE# shall have remained HIGH for t_{CEH} and CE# LOW for at least 100ns prior to the command in order for the VOLUME SELECT (E1h) command to be properly received by all NAND targets connected to the host target. The DQS (DQS_t) signal shall remain HIGH for the entire VOLUME SELECT command sequence.

If volumes that share a host target are configured to use different data interfaces, then the host shall issue the VOLUME SELECT (E1h) command using the asynchronous data interface.

When the VOLUME SELECT (E1h) command is issued, all NAND targets that have a volume address that does not match the address specified shall be deselected to save power (equivalent behavior to CE# pulled HIGH).

If the volume address specified does not correspond to any appointed volume address, then all NAND targets shall be deselected until a subsequent VOLUME SELECT (E1h) command is issued. If the VOLUME SELECT (E1h) command is not the first command issued after CE# is pulled LOW, then the NAND targets revert to their previous states.

The volume address is retained across RESET (FAh, FCh, FFh) commands. A HARD RESET (FDh) command will not undo any previously set volume addressing assignments that were performed prior to the HARD RESET (FDh) command. After HARD RESET (FDh) command is issued the NAND targets do not revert to their previous states and a VOLUME SELECT command (E1h) is required to select the desired volume.

**Figure 55: VOLUME SELECT (E1h) Operation**

- Notes:
1. The host shall not issue new commands to any LUN on any volume until after t_{VDLY} . This delay is required to ensure the appropriate volume is selected for the next command issued. During a data input operation, VOLUME SELECT command may be issued prior to the 10h, 11h, or 15h command if the next command to the volume in data input mode is change row address. In this case, the host shall wait t_{CCS} before issuing the CHANGE ROW ADDRESS command.
 2. The host shall not bring CE# high on any volume until after t_{CEVLDY} . This delay is required to ensure the appropriate volume is selected based on the previously issued VOLUME SELECT command.

Table 29: Volume Address

	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Volume Address											
VA						Volume address					
Reserved		0	0	0	0					-	



Status Operations

Each die (LUN) provides its status independently of other die (LUNs) on the same target through its 8-bit status register.

After the READ STATUS (70h) or READ STATUS ENHANCED (78h) command is issued, status register output is enabled. The contents of the status register are returned on DQ[7:0] for each data output request.

When the asynchronous or NV-DDR2 interfaces are active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and RE# are LOW; it is not necessary to toggle RE# to see the status register update.

When the NV-DDR interface is active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and W/R# are LOW and ALE and CLE are HIGH. DQS also toggles (with 'DQSCK delay) while ALE and CLE are captured HIGH. If status register output is enabled and CE# and W/R# are LOW and ALE and CLE are also captured LOW, changes in the status register are still seen asynchronously on DQ[7:0] but DQS does not toggle.

While monitoring the status register to determine when a data transfer from the Flash array to the data register ('R) is complete, the host must issue the READ MODE (00h) command to disable the status register and enable data output (see Read operations section - READ MODE (00h)).

The READ STATUS (70h) command returns the status of the most recently selected die (LUN). To prevent data contention during or following an interleaved die (multi-LUN) operation, the host must enable only one die (LUN) for status output by using the READ STATUS ENHANCED (78h) command (see Interleaved Die (Multi-LUN) Operations).

Table 30: Status Register Definition

SR Bit	Definition	Independent per Plane ¹	Description
7	WP#	2	Write protect: 0 = Protected 1 = Not protected In the normal array mode, this bit indicates the value of the WP# signal. In OTP mode this bit is set to 0 if a PROGRAM OTP PAGE operation is attempted and the OTP area is protected.
6	RDY	–	Ready/Busy I/O: 0 = Busy 1 = Ready This bit indicates that the selected die (LUN) is not available to accept new commands, address, or data I/O cycles with the exception of RESET LUN (FAh), SYNCHRONOUS RESET (FCh), RESET (FFh), READ STATUS (70h), READ STATUS ENHANCED (78h), and FIXED ADDRESS READ STATUS ENHANCED (71h). This bit applies only to the selected die (LUN).

**Table 30: Status Register Definition (Continued)**

SR Bit	Definition	Independent per Plane¹	Description
5	ARDY	–	<p>Ready/Busy array: 0 = Busy 1 = Ready</p> <p>This bit goes LOW (busy) when an array operation is occurring on any plane of the selected die (LUN). It goes HIGH when all array operations on the selected die (LUN) finish. This bit applies only to the selected die (LUN).</p>
4	–	–	Reserved (0)
3	–	–	Reserved (0)
2	SUSPEND	–	<p>Erase and program suspend: Used in conjunction with FAIL of the status register (SR[0])</p> <p>SUSPEND = 0, FAIL = 0: ERASE or PROGRAM operation completed with successful status.</p> <p>SUSPEND = 0, FAIL = 1: ERASE or PROGRAM operation completed with fail status.</p> <p>SUSPEND = 1, FAIL = X: ERASE or PROGRAM operation successful suspended FAILC is valid in suspend state (SUSPEND = 1) and provides fail status for previous program immediately completed prior to suspended PROGRAM operation.</p> <p>FAIL is invalid in suspend state (SUSPEND = 1)</p> <p>FAILC is invalid for operations performed after suspend is issued or for the resumed array operation from suspend state.</p>
1	FAILC	Yes	<p>Pass/Fail (N-1): 0 = Pass 1 = Fail</p> <p>This bit is set if the previous PROGRAM operation on the selected die (LUN) failed. This bit is valid only when RDY (SR bit 6) is 1. The valid operations for this bit are PROGRAM-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 85h-10h).</p> <p>This bit is not valid following an ERASE-series or READ-series operation.</p> <p>This bit is not an indicator for the status of ERASE- or READ-series operations and is not updated even if the previous operation was a program command. This bit retains the status of the previous valid PROGRAM operation when the most recent PROGRAM operation is complete. For example, if an ERASE or READ operation is complete and the previous operation was a PROGRAM operation the FAILC bit will not provide pass/fail status information for the previous PROGRAM operation. The FAILC bit will only provide pass/fail status information if the most recently finished operation was a PROGRAM operation.</p>

**Table 30: Status Register Definition (Continued)**

SR Bit	Definition	Independent per Plane ¹	Description
0	FAIL	Yes	<p>Pass/Fail (N): 0 = Pass 1 = Fail</p> <p>This bit is set if the most recently finished operation on the selected die (LUN) failed. This bit is valid only when ARDY (SR bit 5) is 1. It applies to PROGRAM-, ERASE-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 60h-D0h, 85h-10h). This bit is not valid following a READ-series operation.</p>

- Notes:
1. After a multi-plane operation begins, the FAILC and FAIL bits are ORed together for the active planes when the READ STATUS (70h) command or FIXED ADDRESS READ STATUS ENHANCED (71h) command are issued. After the READ STATUS ENHANCED (78h) command is issued, the FAILC and FAIL bits reflect the status of the plane selected.
 2. In addition to WP# status, SR[7] also provides LOCK Status (SR[7] = 0) to indicate the host issued a command that was blocked from execution by the NAND. The LOCK Status is cleared upon the host issuing the next valid array operation command. The LOCK Status is Plane independent. If the user issues READ STATUS ENHANCED (78h) or FIXED ADDRESS READ STATUS ENHANCED (71h) to a non-active plane (planes not enabled by user are deemed non-active), then LOCK status (SR[7]) will be invalid.

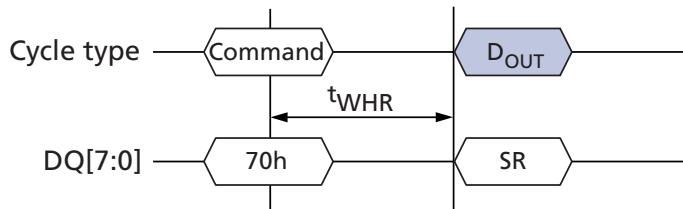
READ STATUS (70h)

The READ STATUS (70h) command returns the status of the last-selected die (LUN) on a target. This command is accepted by the last-selected die (LUN) even when it is busy (RDY = 0).

If there is only one die (LUN) per target, the READ STATUS (70h) command can be used to return status following any NAND command.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select the die (LUN) that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as two or more die (LUNs) could respond until the next operation is issued. The READ STATUS (70h) command can be used following all single die (LUN) operations.

If following a multi-plane operation, regardless of the number of LUNs per target, the READ STATUS (70h) command indicates an error occurred (FAIL = 1), use the READ STATUS ENHANCED (78h) command—once for each plane—to determine which plane operation failed.

Figure 56: READ STATUS (70h) Operation



READ STATUS ENHANCED (78h)

The READ STATUS ENHANCED (78h) command returns the status of the addressed die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0).

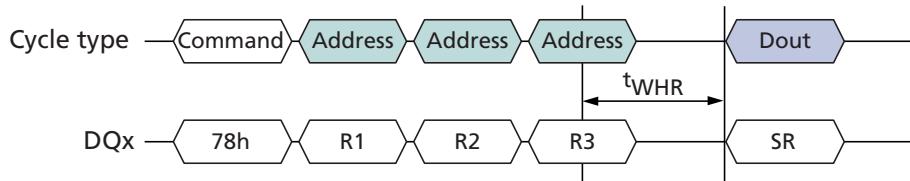
Writing 78h to the command register, followed by three row address cycles containing the page, block, and LUN addresses, puts the selected die (LUN) into read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

The selected LUN's status is returned when the host requests data output. The RDY and ARDY bits of the status register are shared for all of the planes of the selected die (LUN). The FAILC and FAIL bits are specific to the plane specified in the row address.

The READ STATUS ENHANCED (78h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command after the die (LUN) is ready (see CHANGE READ COLUMN ENHANCED (06h-E0h)).

Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET (FFh) command and when OTP mode is enabled. It is also prohibited following some of the other RESET, IDENTIFICATION, and CONFIGURATION operations. See individual operations for specific details.

Figure 57: READ STATUS ENHANCED (78h) Operation



FIXED ADDRESS READ STATUS ENHANCED (71h)

The FIXED ADDRESS READ STATUS ENHANCED (71h) command returns the status of the addressed die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0). The FIXED ADDRESS READ STATUS ENHANCED (71h) command can be used instead of READ STATUS ENHANCED (78h) command, but address cycle bit locations are fixed and do not change based on NAND architecture, number of bits per cell, or any mode selections.

Use of the FIXED ADDRESS READ STATUS ENHANCED (71h) command is allowed during the power-on RESET (FFh) command (during tPOR) and when OTP mode is enabled. It is also allowed following some of the other RESET, IDENTIFICATION, and CONFIGURATION operations that READ STATUS ENHANCED (78h) is prohibited.

Writing 71h to the command register, followed by one row address cycle containing the hardcoded LUN selections, puts the selected die (LUN) into read status mode. The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.



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The status output for FIXED ADDRESS READ STATUS ENHANCED (71h) command is identical to the status output for READ STATUS ENHANCED (78h) command. The selected LUN's status is returned when the host requests data output. The RDY, ARDY, FAILC, and FAIL bits of the status register are shared for all of the planes of the selected die (LUN).

The FIXED ADDRESS READ STATUS ENHANCED (71h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command after the die (LUN) is ready (see CHANGE READ COLUMN ENHANCED (06h-E0h)).

Figure 58: FIXED ADDRESS READ STATUS ENHANCED (71h) Operation

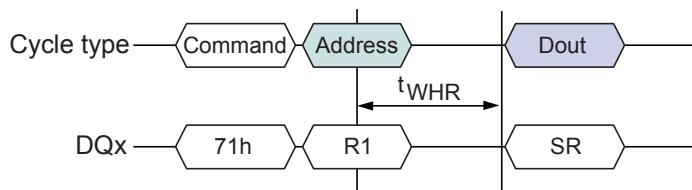


Table 31: R1 Address Cycle Decoding for FIXED ADDRESS READ STATUS ENHANCED (71h) Operation

Description	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
R1											
Bit LA0 (DQ0) for LUN selection	LUN0								0	0b	
	LUN1								1	1b	
Reserved	Don't Care	-	-	-	-	-	-	-			1

Note: 1. Must be "0".

Column Address Operations

The column address operations affect how data is input to and output from the cache registers within the selected die (LUNs). These features provide host flexibility for managing data, especially when the host internal buffer is smaller than the number of data bytes or words in the cache register.

When the asynchronous interface is active, column address operations can address any byte in the selected cache register.

When the synchronous interface is active, column address operations are aligned to word boundaries (CA0 is forced to 0), because as data is transferred on DQ[7:0] in two-byte units.

CHANGE READ COLUMN (05h-E0h)

The CHANGE READ COLUMN (05h-E0h) command changes the column address of the selected cache register and enables data output from the last selected die (LUN). This



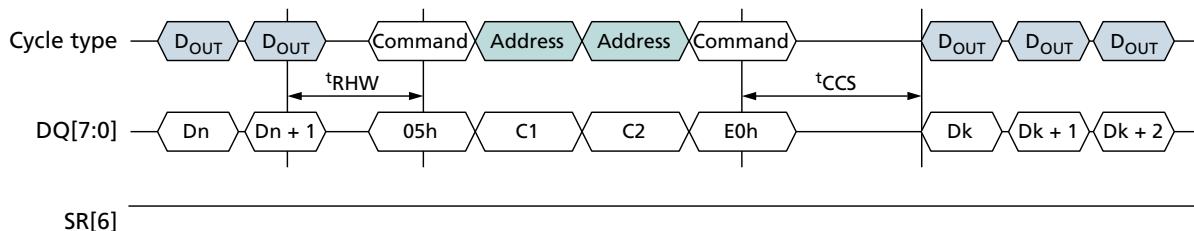
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command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE READ operations (RDY = 1; ARDY = 0).

Writing 05h to the command register, followed by two column address cycles containing the column address, followed by the E0h command, puts the selected die (LUN) into data output mode. After the E0h command cycle is issued, the host must wait at least t_{CCS} before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be issued prior to issuing the CHANGE READ COLUMN (05h-E0h). In this situation, using the CHANGE READ COLUMN (05h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

Figure 59: CHANGE READ COLUMN (05h-E0h) Operation



CHANGE READ COLUMN ENHANCED (06h-E0h)

The CHANGE READ COLUMN ENHANCED (06h-E0h) command enables data output on the addressed die's (LUN's) cache register at the specified column address. This command is accepted by a die (LUN) when it is ready (RDY = 1; ARDY = 1).

Writing 06h to the command register, followed by two column address cycles and three row address cycles, followed by E0h, enables data output mode on the address LUN's cache register at the specified column address. Only the column, plane and LUN addresses are valid; the page and block addresses are ignored. After the E0h command cycle is issued, the host must wait at least t_{CCS} before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

Following a MULTI-PLANE READ PAGE operation, the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select the cache register to be enabled for data output. After data output is complete on the selected plane, the command can be issued again to begin data output on another plane.

In devices with more than one die (LUN) per target, after all of the die (LUNs) on the target are ready (RDY = 1), the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used following an interleaved die (multi-LUN) READ operation. Die (LUNs) that are not addressed are deselected to avoid bus contention.

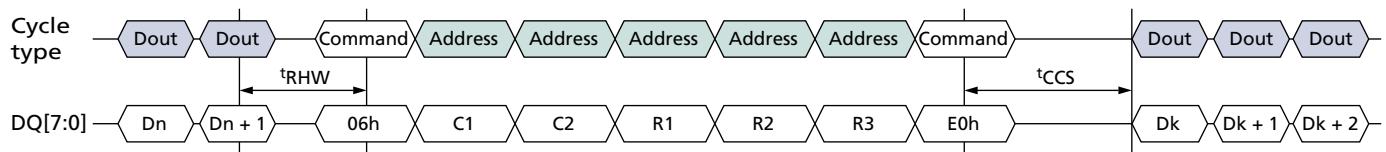
In devices with more than one die (LUN) per target, during interleaved die (multi-LUN) operations where more than one or more die (LUNs) are busy (RDY = 1; ARDY = 0 or RDY = 0; ARDY = 0), the READ STATUS ENHANCED (78h) command must be issued to the die (LUN) to be selected prior to issuing the CHANGE READ COLUMN ENHANCED



(06h-E0h). In this situation, using the CHANGE READ COLUMN ENHANCED (06h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

If there is a need to update the column address without selecting a new cache register or LUN, the CHANGE READ COLUMN (05h-E0h) command can be used instead.

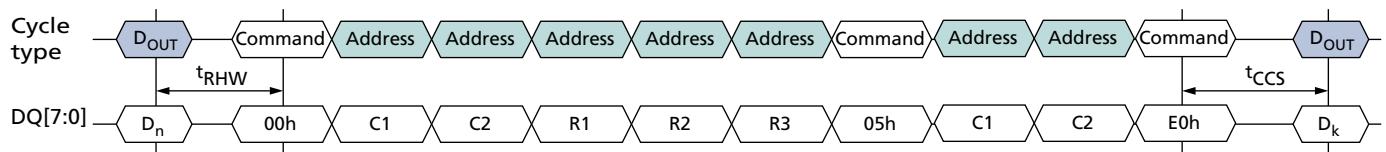
Figure 60: CHANGE READ COLUMN ENHANCED (06h-E0h) Operation



CHANGE READ COLUMN ENHANCED (00h-05h-E0h) Operation

This operation behaves the same as the CHANGE READ COLUMN ENHANCED (06h-E0h) command.

Figure 61: CHANGE READ COLUMN ENHANCED (00h-05h-E0h) Operation



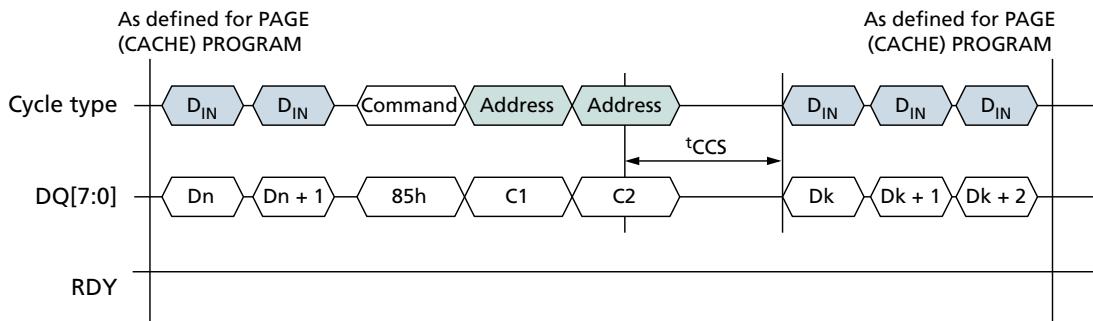
CHANGE WRITE COLUMN (85h)

The CHANGE WRITE COLUMN (85h) command changes the column address of the selected cache register and enables data input on the last-selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1).

Writing 85h to the command register, followed by two column address cycles containing the column address, puts the selected die (LUN) into data input mode. After the second address cycle is issued, the host must wait at least t_{CCS} before inputting data. The selected die (LUN) stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE WRITE COLUMN (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h).

In devices that have more than one die (LUN) per target, the CHANGE WRITE COLUMN (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

**Figure 62: CHANGE WRITE COLUMN (85h) Operation**

CHANGE ROW ADDRESS (85h)

The CHANGE ROW ADDRESS (85h) command changes the row address (block and page) where the cache register contents will be programmed in the NAND Flash array. It also changes the column address of the selected cache register and enables data input on the specified die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1).

Write 85h to the command register. Then write two column address cycles and three row address cycles. This updates the page and block destination of the selected plane for the addressed LUN and puts the cache register into data input mode. After the fifth address cycle is issued the host must wait at least t_{CCS} before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE ROW ADDRESS (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h). When used with these commands, the LUN address and plane select bits are required to be identical to the LUN address and plane select bits originally specified.

The CHANGE ROW ADDRESS (85h) command enables the host to modify the original page and block address for the data in the cache register to a new page and block address.

In devices that have more than one die (LUN) per target, the CHANGE ROW ADDRESS (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

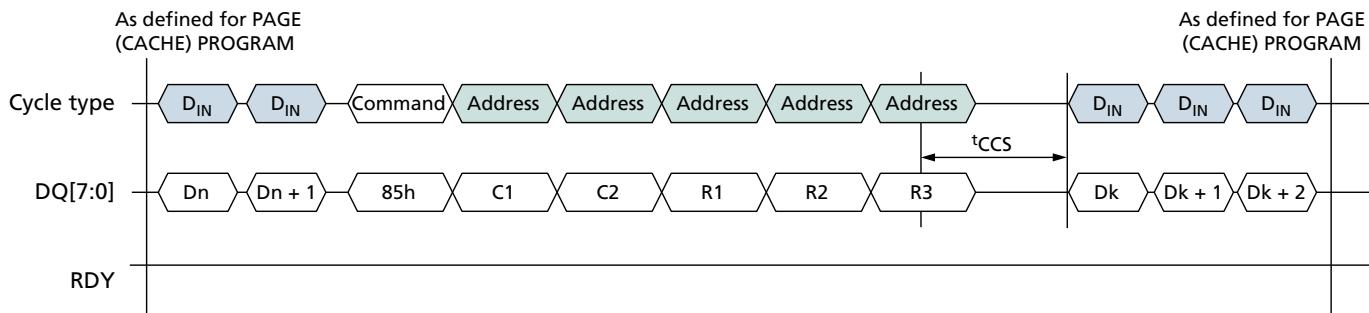
The CHANGE ROW ADDRESS (85h) command can be used with the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) commands to read and modify cache register contents in small sections prior to programming cache register contents to the NAND Flash array. This capability can reduce the amount of buffer memory used in the host controller.

To modify the cache register contents in small sections, first issue a PAGE READ (00h-30h) or COPYBACK READ (00h-35h) operation. When data output is enabled, the host can output a portion of the cache register contents. To modify the cache register



contents, issue the 85h command, the column and row addresses, and input the new data. The host can re-enable data output by issuing the 11h command, waiting t_{DBSY} , and then issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command. It is possible to toggle between data output and data input multiple times. After the final CHANGE ROW ADDRESS (85h) operation is complete, issue the 10h command to program the cache register to the NAND Flash array.

Figure 63: CHANGE ROW ADDRESS (85h) Operation



Read Operations

Read operations are used to copy data from the NAND Flash array of one or more of the planes to their respective cache registers and to enable data output from the cache registers to the host through the DQ bus.

Read Operations

The READ PAGE (00h-30h) command, when issued by itself, reads one page from the NAND Flash array to its cache register and enables data output for that cache register.

During data output the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h) and CHANGE ROW ADDRESS (85h).

Read Cache Operations

To increase data throughput, the READ PAGE CACHE-series (31h, 00h-31h) commands can be used to output data from the cache register while concurrently copying a page from the NAND Flash array to the data register.

To begin a read page cache sequence, begin by reading a page from the NAND Flash array to its corresponding cache register using the READ PAGE (00h-30h) command.

R/B# goes LOW during t_R and the selected die (LUN) is busy ($RDY = 0$, $ARDY = 0$). After t_R (R/B# is HIGH and $RDY = 1$, $ARDY = 1$), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h)—copies the next sequential page from the NAND Flash array to the data register
- READ PAGE CACHE RANDOM (00h-31h)—copies the page specified in this command from the NAND Flash array (any plane) to its corresponding data register

After the READ PAGE CACHE-series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and $RDY = 0$ and $ARDY = 0$ on the die (LUN) for t_{RCBSY} while the next page begins copying data from the array to the data register. After t_{RCBSY} ,



R/B# goes HIGH and the die's (LUN's) status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache register becomes available and the page requested in the READ PAGE CACHE operation is transferred to the data register. At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output by the die (LUN).

After outputting the desired number of bytes from the cache register, either an additional READ PAGE CACHE-series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for t_{RCBSY} while the data register is copied into the cache register. After t_{RCBSY} , R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache register is available and that the die (LUN) is ready. Data can then be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, t_{RCBSY} , when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h, 71h) and RESET (FFh, FCh, FAh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status operations (70h, 78h, 71h), READ MODE (00h), READ PAGE CACHE-series (31h, 00h-31h), CHANGE READ COLUMN (05h-E0h), and RESET (FFh, FCh, FAh).

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with a READ PAGE CACHE LAST (3Fh) command.

Multi-Plane Read Operations

MULTI-PLANE READ PAGE operations improve data throughput by copying data from more than one plane simultaneously to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the READ PAGE (00h-30h) command.

When the die (LUN) is ready, the CHANGE READ COLUMN ENHANCED (06h-E0h) command determines which plane outputs data. During data output, the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h) and CHANGE ROW ADDRESS (85h). See Multi-Plane Operations for details.

Multi-Plane Read Cache Operations

MULTI-PLANE READ CACHE operations can be used to output data from more than one cache register while concurrently copying one or more pages from the NAND Flash array to the data register. This is done by prepending READ PAGE MULTI-PLANE (00h-32h) commands in front of the READ PAGE CACHE RANDOM (00h-31h) command.

To begin a multi-plane read page cache sequence, begin by issuing a MULTI-PLANE READ PAGE operation using the READ PAGE MULTI-PLANE (00h-32h) and READ PAGE (00h-30h) commands. R/B# goes LOW during t_R and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After t_R (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:



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- READ PAGE CACHE SEQUENTIAL (31h)—copies the next sequential page from the previously addressed planes from the NAND Flash array to the data registers.
- READ PAGE MULTI-PLANE (00h-32h) commands, if desired, followed by the READ PAGE CACHE RANDOM (00h-31h) command—copies the pages specified from the NAND Flash array to the corresponding data registers.

After the READ PAGE CACHE-series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^tRCBSY while the next pages begin copying data from the array to the data registers. After ^tRCBSY, R/B# goes HIGH and the LUN's status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache registers become available and the pages requested in the READ PAGE CACHE operation are transferred to the data registers. Issue the CHANGE READ COLUMN ENHANCED (06h-E0h) command to determine which cache register will output data. After data is output, the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output.

After outputting data from the cache registers, either an additional MULTI-PLANE READ CACHE-series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for ^tRCBSY while the data registers are copied into the cache registers. After ^tRCBSY, R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache registers are available and that the die (LUN) is ready. Issue the CHANGE READ COLUMN ENHANCED (06h-E0h) command to determine which cache register will output data. After data is output, the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^tRCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h, 71h) and RESET (FFh, FCh, FAh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status operations (70h, 78h, 71h), READ MODE (00h), MULTI-PLANE READ CACHE-series (31h, 00h-32h, 00h-31h), CHANGE READ COLUMN (05h-E0h, 06h-E0h), and RESET (FFh, FCh, FAh).

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with a READ PAGE CACHE LAST (3Fh) command.

See Multi-Plane Operations for additional multi-plane addressing requirements.

READ MODE (00h)

The READ MODE (00h) command disables status output and enables data output for the last-selected die (LUN) and cache register after a READ operation (00h-30h, 00h-35h) has been monitored with a status operation (70h, 78h, 71h). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 3Fh, 00h-31h) operations (RDY = 1 and ARDY = 0).



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In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to issuing the READ MODE (00h) command. This prevents bus contention.

READ PAGE (00h-30h)

The READ PAGE (00h–30h) command copies a page from the NAND Flash array to its respective cache register and enables data output. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To read a page from the NAND Flash array, write the 00h command to the command register, the write five address cycles to the address registers, and conclude with the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for t_R as data is transferred.

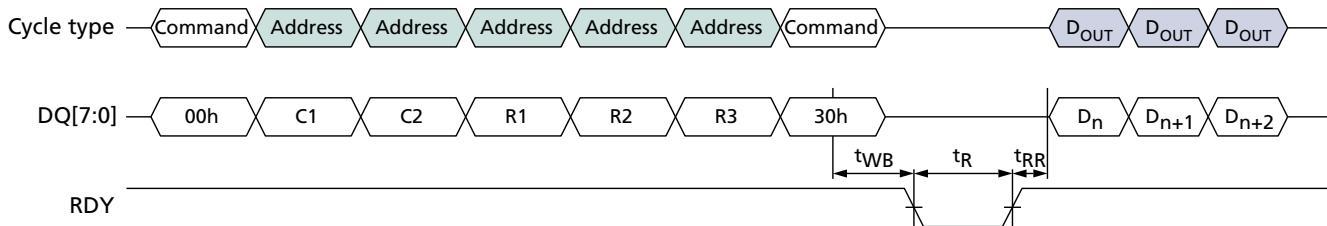
To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h, 71h) can be used. If the status operations are used to monitor the LUN's status, when the die (LUN) is ready (RDY = 1, ARDY = 1), the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, output begins at the column address specified.

During data output the CHANGE READ COLUMN (05h-E0h) command can be issued.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to the issue of the READ MODE (00h) command. This prevents bus contention.

The READ PAGE (00h-30h) command is used as the final command of a MULTI-PLANE READ operation. It is preceded by one or more READ PAGE MULTI-PLANE (00h-32h) commands. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the least significant plane addressed, regardless of input order. When the host requests data output, output begins at the column address last specified in the READ PAGE (00h-30h) command. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to enable data output in the other cache registers. See Multi-Plane Operations for additional multi-plane addressing requirements.

Figure 64: READ PAGE (00h-30h) Operation





READ PAGE CACHE SEQUENTIAL (31h)

The READ PAGE CACHE SEQUENTIAL (31h) command reads the next sequential page within a block into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

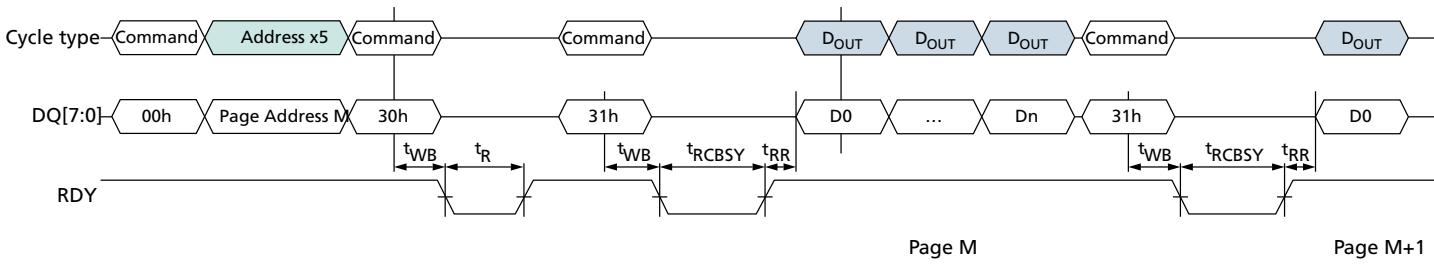
To issue this command, write 31h to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for tRCBSY. After tRCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

The READ PAGE CACHE SEQUENTIAL (31h) command can be used to cross block boundaries. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a block is read into the data register, the next page read will be the next logical block in the plane which the 31h command was issued. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a plane is read into the data register, the NAND device will keep outputting the data from the last page of the plane. The last page of the plane is not re-read from the NAND array. Data is kept in the cache register and read from there. Do not issue the READ PAGE CACHE SEQUENTIAL (31h) to cross die (LUN) boundaries. Instead, issue the READ PAGE CACHE LAST (3Fh) command.

If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after a MULTI-PLANE READ PAGE operation (00h-32h, 00h-30h), the next sequential pages are read into the data registers while the previous pages can be output from the cache registers. During multi-plane sequential cache read mode, if the READ PAGE CACHE SEQUENTIAL (31h) command is issued after reading the last page in the last block in one plane and a last page in a random block in the other plane, the circuit increments the block address and page address for only the plane that has not reached the end of its plane addressing. After the die (LUN) is ready (RDY = 1, ARDY = 0), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with a READ PAGE CACHE LAST (3Fh) command.

Figure 65: READ PAGE CACHE SEQUENTIAL (31h) Operation



**READ PAGE CACHE RANDOM (00h-31h)**

The READ PAGE CACHE RANDOM (00h-31h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

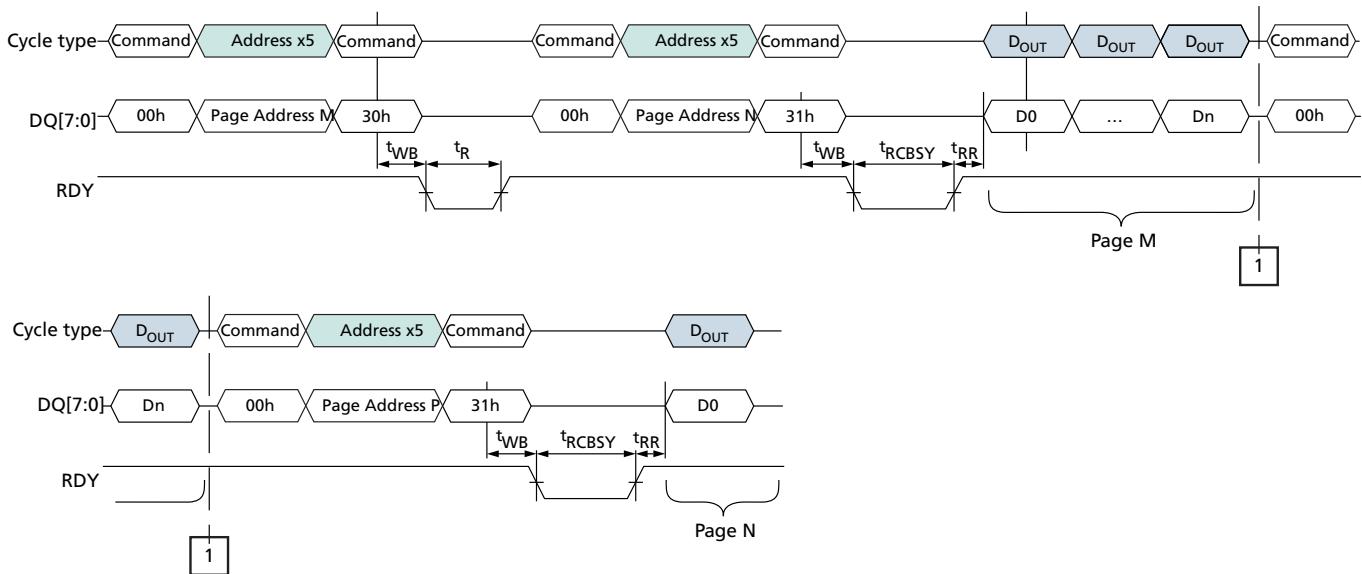
To issue this command, write 00h to the command register, then write five address cycles to the address register, and conclude by writing 31h to the command register. The column address in the address specified is ignored. The die (LUN) address must match the same die (LUN) address as the previous READ PAGE (00h-30h) command or, if applicable, the previous READ PAGE CACHE RANDOM (00h-31h) command. There is no restriction on the plane address.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^tRCBSY. After ^tRCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

If a MULTI-PLANE CACHE RANDOM (00h-32h, 00h-31h) command is issued after a MULTI-PLANE READ PAGE operation (00h-32h, 00h-30h), then the addressed pages are read into the data registers while the previous pages can be output from the cache registers. After the die (LUN) is ready (RDY = 1, ARDY = 0), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with a READ PAGE CACHE LAST (3Fh) command.

**Figure 66: READ PAGE CACHE RANDOM (00h-31h) Operation**

READ PAGE CACHE LAST (3Fh)

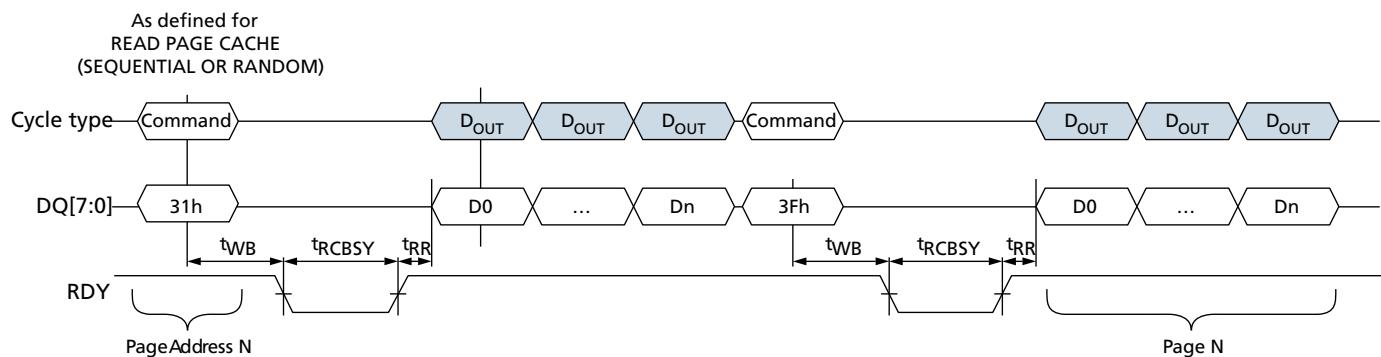
The READ PAGE CACHE LAST (3Fh) command ends the read page cache sequence and copies a page from the data register to the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue the READ PAGE CACHE LAST (3Fh) command, write 3Fh to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for t_{RCBSY}. After t_{RCBSY}, R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one LUN per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

If the READ PAGE CACHE LAST (3Fh) command is issued after a MULTI-PLANE READ PAGE CACHE operation (31h; 00h-32h, 00h-30h), the die (LUN) goes busy until the pages are copied from the data registers to the cache registers. After the die (LUN) is ready (RDY = 1, ARDY = 1), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with a READ PAGE CACHE LAST (3Fh) command.

**Figure 67: READ PAGE CACHE LAST (3Fh) Operation**

READ PAGE MULTI-PLANE (00h-32h)

The READ PAGE MULTI-PLANE (00h-32h) command queues a plane to transfer data from the NAND flash array to its cache register. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for data transfer. The READ PAGE (00h-30h) command is issued to select the final plane and to begin the READ operation for all previously queued planes. All queued planes will transfer data from the NAND Flash array to their cache registers.

To issue the READ PAGE MULTI-PLANE (00h-32h) command, write 00h to the command register, then write five address cycles to the address register, and conclude by writing 32h to the command register. The column address in the address specified is ignored.

After this command is issued, R/B# goes LOW and the die (LUN) is busy ($RDY = 0$, $ARDY = 0$) for t_{DBSY} . After t_{DBSY} , R/B# goes HIGH and the die (LUN) is ready ($RDY = 1$, $ARDY = 1$). At this point, the die (LUN) and block are queued for data transfer from the array to the cache register for the addressed plane. During t_{DBSY} , the only valid commands are status operations (70h, 78h, 71h) and RESET (FFh, FCh, FAh). Following t_{DBSY} , to continue the MULTI-PLANE READ operation, the only valid commands are status operations (70h, 78h, 71h), READ PAGE MULTI-PLANE (00h-32h), READ PAGE (00h-30h), and READ PAGE CACHE RANDOM (00h-31h).

Additional READ PAGE MULTI-PLANE (00h-32h) commands can be issued to queue additional planes for data transfer.

If the READ PAGE (00h-30h) command is used as the final command of a MULTI-PLANE READ operation, data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready ($RDY = 1$, $ARDY = 1$), data output is enabled for the cache register linked to the least significant plane addressed, regardless of input order. When the host requests data output, it begins at the column address specified in the READ PAGE (00h-30h) command. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

If the READ PAGE CACHE SEQUENTIAL (31h) is used as the final command of a MULTI-PLANE READ CACHE operation, data is copied from the previously READ operation from each plane to each cache register and then data is transferred from the NAND



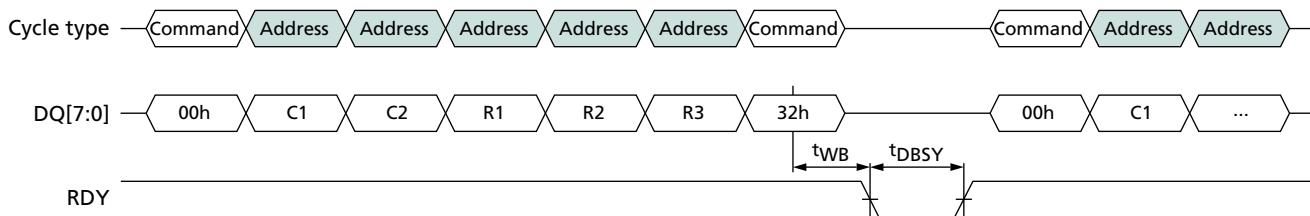
Flash array for all previously addressed planes to their respective data registers. When the die (LUN) is ready (RDY = 1, ARDY = 0), data output is enabled. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to determine which cache register outputs data first. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

If the READ PAGE CACHE RANDOM (00h-31h) command is used as the final command of a MULTI-PLANE READ CACHE operation, data is copied from the previously READ operation from the data register to the cache register and then data is transferred from the NAND Flash array for all of the addressed planes to their respective data registers. When the die (LUN) is ready (RDY = 1, ARDY = 0), data output is enabled. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to determine which cache register outputs data first. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

SET FEATURES operations are not supported within a cache read sequence that has not been closed out with a READ PAGE CACHE LAST (3Fh) command.

See Multi-Plane Operations for additional multi-plane addressing requirements.

Figure 68: READ PAGE MULTI-PLANE (00h-32h) Operation



Read Retry Operations

READ RETRY operations are used as an additional method to recover from bit errors beyond the ECC correction threshold.

Read Retry Operations

The READ RETRY operations are a coordination of READ operations and SET FEATURES (EFh) or SET FEATURES by LUN (D5h) with feature address 89h, selecting different internal read settings in attempt to recover data that is beyond the ECC correction threshold. Using the READ RETRY operations with any array READ operation commands is allowed. See Configuration Operations and Feature Address 89h: Read Retry for details.

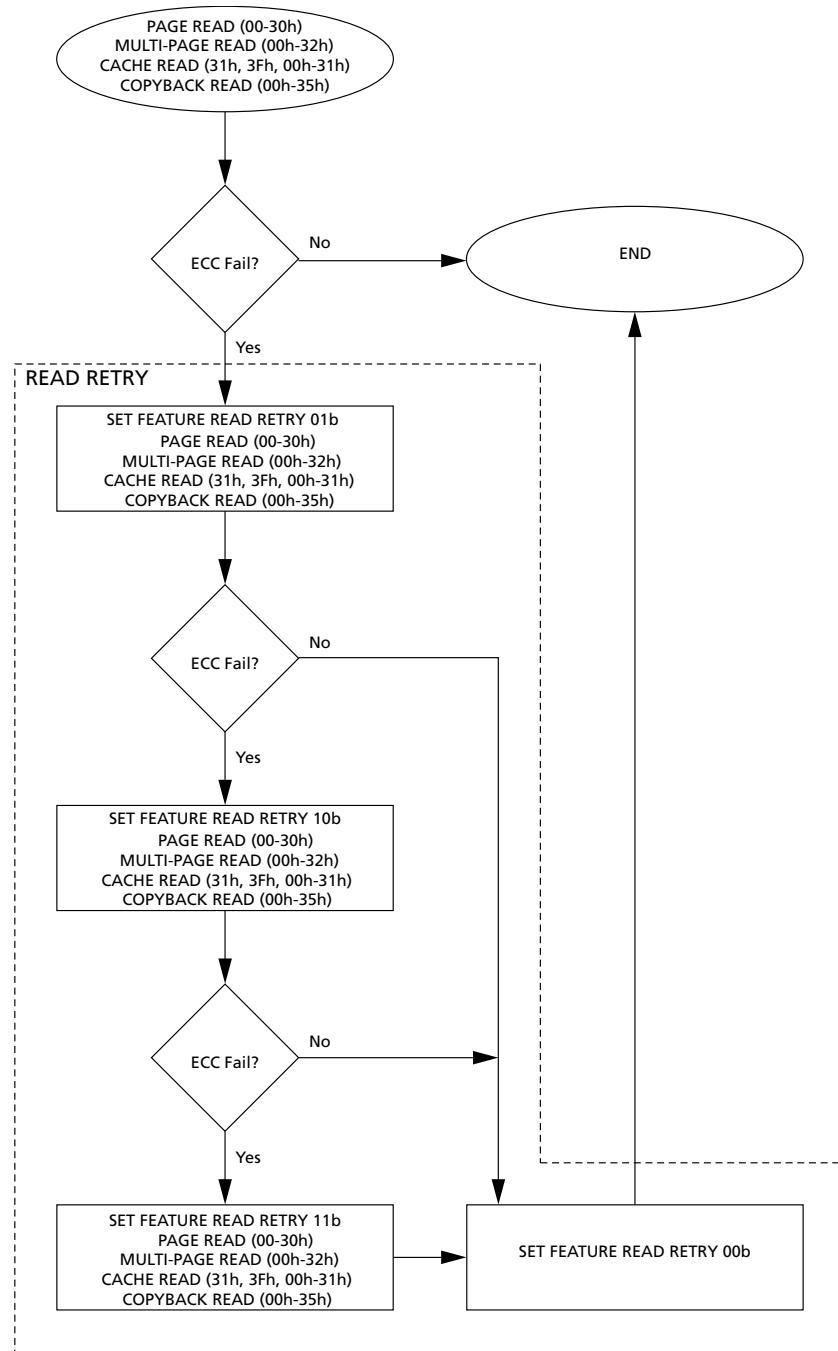
If reading a page has failed for bit errors beyond the ECC correction threshold, the host issues the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command to feature address 89h with P1 subfeature set to a read retry option, as defined in that feature address. A new NAND array READ operation can now be performed. If the read still fails for bit errors beyond the ECC correction threshold, issue the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command with the read retry (89h) feature address to select the next consecutive read retry option and repeat READ RETRY operations until the



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data is correctable or the last option has been attempted. If the re-read is now correctable within the ECC threshold limits, the next read retry option should be set to its default value before the next NAND array READ operation. See Figure 69 (page 123) for flow diagram of READ RETRY operations.

When the user writes to the read retry feature address, all subsequent reads use the internal NAND settings associated with that value until either the read retry feature address is rewritten or the device is powered-down. This feature should not be used with the following commands: READ PARAMETER PAGE (ECh), READ UNIQUE ID (EDh), READ OTP PAGE (00h-30h).

**Figure 69: Read Retry Flow Chart**

Note: 1. There may be more read retry options than are shown in the figure for this NAND device. See Configuration Operations and Read Retry (89h) feature address for details.



Program Operations - Single Pass Programming

Program operations are used to move data from the cache or data registers to the NAND array of one or more planes. During a PROGRAM operation the contents of the cache and/or data registers are modified by the internal control logic. The MLC single pass programming sequence requires both lower and upper associated shared pages be entered before data is programmed into the array. Lower page data must be entered before the upper page data. After data has been entered to a lower page address, the program confirm command (10h) will trigger the LUN to move the data from the cache register into internal page buffer latches, ^tPBSY. After data has been entered to an upper page address, the confirm command (10h) will trigger the LUN to begin the PROGRAM operation.

Within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (for example, 0, 1, 2, 3, ...). Programming pages out of order within a block is prohibited.

The PROGRAM PAGE (80h-10h) command is used to enter the lower page address and data into the cache register. After the 10h command is entered the LUN will go busy (RDY = 0, ARDY = 0) for ^tPBSY while data is transferred from the cache register into the page buffer latches. A second PROGRAM PAGE (80h-10h) operation is used to enter the upper page address and data into the cache register. After the 10h command is entered the LUN will go busy (RDY = 0, ARDY = 0) for ^tPROG while data is written to the array. If RESET (FFh, FCh, FAh) is issued anytime during the program sequence prior to ^tPROG time (including ^tPBSY time), the program sequence is aborted and must be re-started from the beginning. Data in the page registers is valid.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the READ STATUS (70h, 78h) operations may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit.

It is the responsibility of the host to ensure that the lower page and upper page address are associated shared pages (see Shared Pages section). No internal address checks are performed by the LUN. In the event that the lower page and upper page addresses are not associated shared pages, the data will be programmed to the lower and upper pages specified by the upper page address, and the lower page data will not be valid.

After lower page data has been entered via PROGRAM PAGE (80h-10h) command, if a second PROGRAM PAGE (80h-10h) command is issued with a lower page address to the same plane, the data entered into the first lower page address will be overwritten. A subsequent (80h-10h) command sequence with upper page address and data will still be required to trigger the start of the program algorithm.

Use of READ PAGE (00h-30h) and READ PAGE MULTI-PLANE (00h-32h) commands are allowed to be performed in between lower page and upper page data entry to other pages and/or LUNs. ERASE operations using ERASE BLOCK (60h-D0h) commands are also allowed in between lower page and upper page data entry as long as the ERASE operation does not occur in the same plane and same LUN as the SINGLE PASS PROGRAMMING operation.

While in a single pass programming sequence, all Cache read operations (00h-31h, 31h, 3Fh) are prohibited between lower page and upper page data entry. READ RETRY operations that invoke a longer ^tR time (see Configuration Operations section, feature address 89h: read retry for details) are also prohibited between lower page and upper page



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data entry. Programming operations to other blocks on the same die (LUN) are prohibited between lower page and upper page data entry

PROGRAM SUSPEND (84h) AND PROGRAM RESUME (13h) operations are supported within a single pass programming sequence. See Program Suspend (84h) and Program Resume (13h) for description of the use of suspend and resume operations.

Pages that are mapped without a shared page require only a single PROGRAM PAGE (80h-10h) operation. See the Shared Pages section for details.

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can also be used with single pass programming. Special care must be taken to ensure the command sequence follows the correct order when multi-plane programming operations are being used. Because the LUN is triggered to move data from the cache register into the internal page buffer latches only after the confirm command (10h) associated with data loaded to a lower page address, data must first be loaded into the lower page of each plane before upper page data can be loaded. Multi-Plane operations follow all of the same restrictions as single-plane operations.

The following are examples of program command sequences using the single pass programming sequence.

Example command sequence for PROGRAM PAGE (80h-10h) with single pass programming for one plane:

1. Issue PROGRAM PAGE (80h-10h) with lower page data
2. Wait ^tPBSY
3. Issue PROGRAM PAGE (80h-10h) with upper page data
4. Wait ^tPROG

Example command sequence for PROGRAM PAGE MULTI-PLANE (80h-11h) with single pass programming for two planes:

1. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 lower page data
2. Issue PROGRAM PAGE (80h-10h) with Plane 1 lower page data
3. Wait ^tPBSY
4. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 upper page data
5. Issue PROGRAM PAGE (80h-10h) with Plane 1 upper page data
6. Wait ^tPROG

Example command sequence for COPYBACK PROGRAM (85h-10h) with single pass programming for one plane:

1. Issue COPYBACK READ (00h-35h). It is possible for the COPYBACK READ (00h-35h) command to address a different block or page type from the subsequent 85h command, however both the 00h-35h and 85h commands must address the same plane.
2. Read data out and identify errors
3. Issue CHANGE WRITE COLUMN (85h) + 5 address cycles (addressed to a lower page) to address of first error and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.
4. Wait ^tPBSY
5. Issue COPYBACK READ (00h-35h) to another address
6. Read data out and identify errors
7. Issue CHANGE WRITE COLUMN (85h) + 5 address cycles (addressed to an upper page) to address of first error and enter corrected data. Repeat error correction by



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issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.

8. Wait t_{PROG}

Example command sequence for MULTI-PLANE PROGRAM with READ PAGE Interrupt with single pass programming with two planes:

1. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 lower page data
2. Issue PROGRAM PAGE (80h-10h) with Plane 1 lower page data
3. Wait t_{PBSY}
4. Issue PROGRAM PAGE MULTI-PLANE (80h-11h) with Plane 0 upper page data
5. Issue PROGRAM PAGE (80h-10h) with Plane 1 upper page data
6. After t_{PROG} has started but has not yet finished, Issue PROGRAM SUSPEND (84h) with 5 cycle address
7. Wait t_{PSPD}
8. Issue READ PAGE MULTI-PLANE (00h-32h) to Plane 0
9. Issue READ PAGE (00h-30h) to Plane 1
10. Wait t_R
11. Read out data from Plane 0 and Plane 1
12. Issue PROGRAM RESUME (13h) with 5 cycle address
13. Wait t_{PROG}



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Figure 70: PROGRAM PAGE (80h-10h) Operation with Single Pass Programming

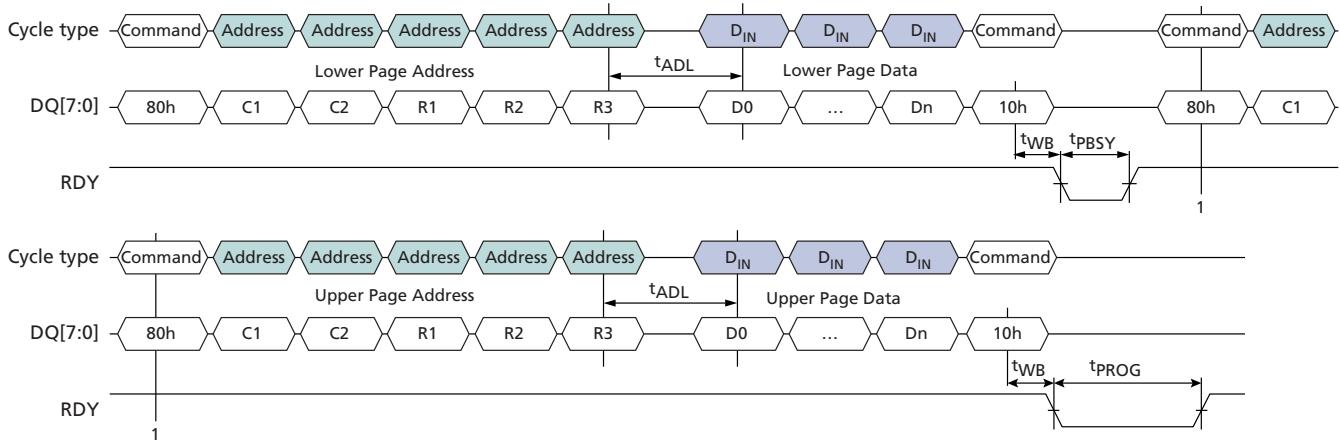
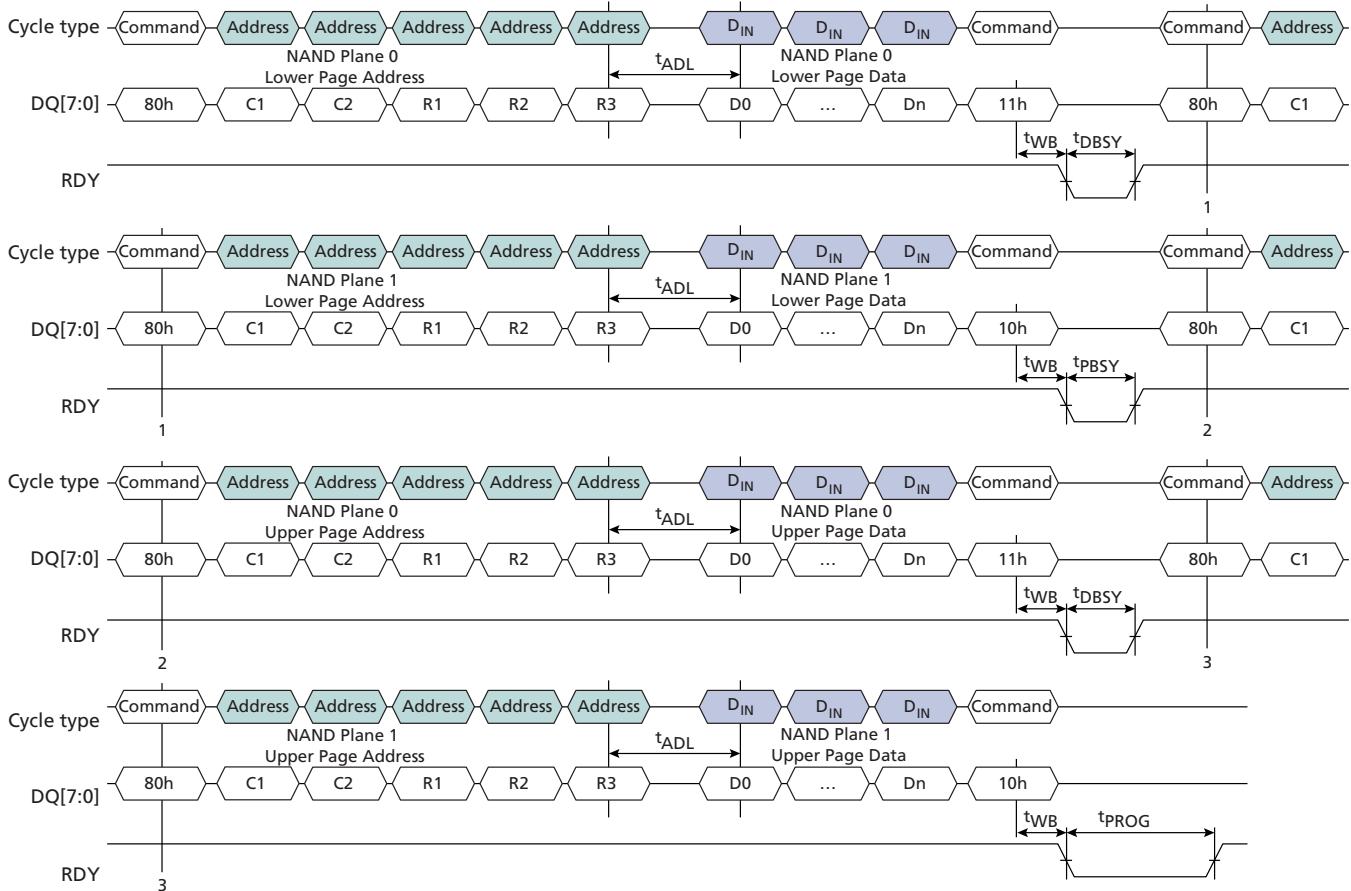


Figure 71: PROGRAM PAGE MULTI-PLANE (80h-11h) Operation with Single Pass Programming



Program Operations



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The PROGRAM PAGE (80h-10h) command, when not preceded by the PROGRAM PAGE MULTI-PLANE (80h-11h) command, programs one page from the cache register to the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that the operation has completed successfully.

Multi-Plane Program Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve PROGRAM operation system performance by enabling multiple pages to be moved from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE (80h-10h) command. See Multi-Plane Operations for details.

PROGRAM PAGE (80h-10h)

The PROGRAM PAGE (80h-10h) command enables the host to input data to a cache register, and move the data from the cache register to the specified block and page address in the array of the selected die (LUN). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To input a page to the cache register and move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write five address cycles containing the column address and row address of the lower page address. Data input cycles follow for the lower page address. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for 'PBSY as the lower page data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1).

After the lower page data is committed, write another 80h to the command register. Then write five address cycles containing the column address and row address of the upper page address. Data input cycles follow for the upper page address. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for 'PROG as both the lower page data and upper page data is programmed.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1).

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

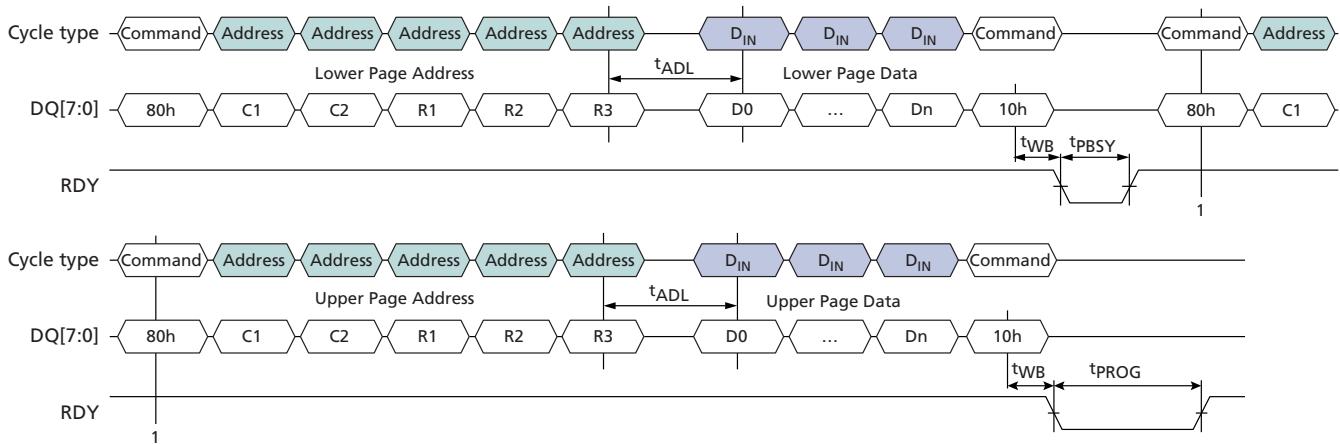
When the last PROGRAM PAGE (80h-10h) command is used as the final command of a MULTI-PLANE PROGRAM operation, it is preceded by one or more PROGRAM PAGE



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MULTI-PLANE (80h-11h) commands, data is transferred from the cache registers for all of the addressed planes to the NAND array. The host should check the status of the operation by using the status operations (70h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.

Figure 72: PROGRAM PAGE (80h-10h) Operation



PROGRAM PAGE MULTI-PLANE (80h-11h)

The PROGRAM PAGE MULTI-PLANE (80h-11h) command enables the host to input data to the addressed plane's cache register and queue the cache register to ultimately be moved to the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the PROGRAM operation for all previously queued planes, issue the PROGRAM PAGE (80h-10h) command. All of the queued planes will move the data to the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1).

To input a page to the cache register and queue it to be moved to the NAND Flash array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by an 11h command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Write five address cycles containing the column address and row address for a lower page; data input cycles follow for the lower page. Serial data is input beginning at the column address specified. At any time during the data input cycle, the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands can be issued. When data input is complete, write 11h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for tDBSY.

To determine the progress of tDBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used.

When the LUN's status shows that it is ready (RDY = 1) and the lower page data is committed for the first NAND plane enter, write another 80h to the command register and then write five address cycles containing the column address and row address of the lower page address of another NAND plane. Data input cycles follow for the lower page address of the NAND plane. Serial data is input beginning at the column address speci-



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fied. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 11h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for t_{DBSY} .

Additional PROGRAM PAGE MULTI-PLANE (80h-11h) commands can be issued to queue additional planes of lower page addresses for data transfer in this manner.

When the last address of lower page plane data is desired to be issued, instead of issuing the PROGRAM PAGE MULTI-PLANE (80h-11h) the PROGRAM PAGE (80h-10h) shall be issued. The selected LUN will go busy (RDY = 0, ARDY = 0) for t_{PBSY} .

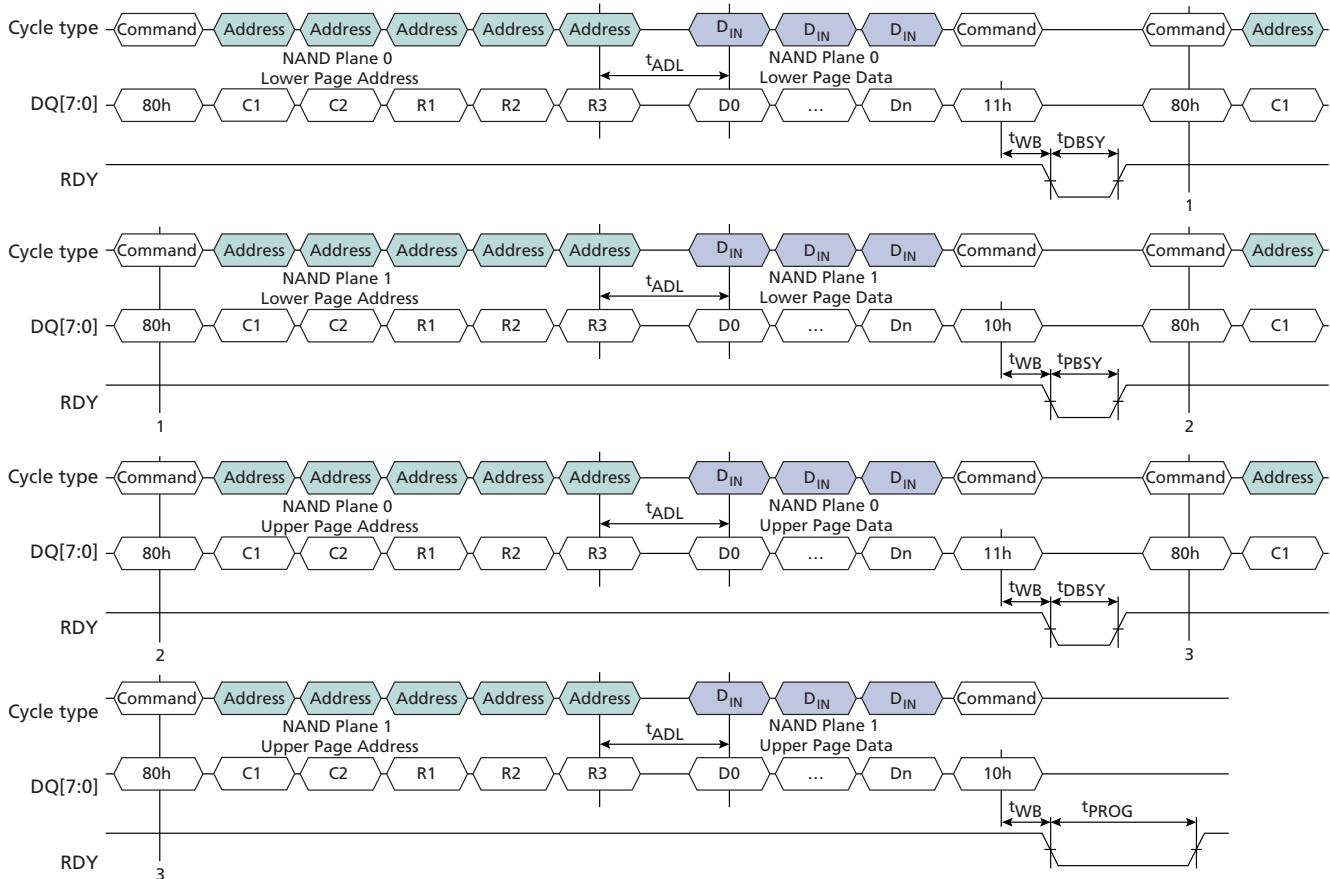
When the LUN's status shows that it is ready (RDY = 1) the same sequence that was used for inputting the lower page addresses for the previous inputted number of planes is repeated for the upper page addresses to complete the multi-plane programming sequence. When the final PROGRAM PAGE (80h-10h) command is issued with the last upper page address, data is transferred from the cache registers to the NAND Flash array for all of the addressed planes during t_{PROG} . When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit for each of the planes to verify that programming completed successfully.

For the PROGRAM PAGE MULTI-PLANE (80h-11h) and PROGRAM PAGE (80h-10h) commands, see Multi-Plane Operations for multi-plane addressing requirements.



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Figure 73: PROGRAM PAGE MULTI-PLANE (80h-11h) Operation



For JEDEC compliance the PROGRAM PAGE MULTI-PLANE (81h-11h) command is also supported. This would also include the last command 81h-10h to conclude a PROGRAM PAGE MULTI-PLANE sequence.

PROGRAM SUSPEND (84h) and PROGRAM RESUME (13h)

The PROGRAM SUSPEND (84h) command is used to pause a program in execution for the LUN specified (RDY = 0, ARDY = 0 or RDY = 1, ARDY = 0). If a PROGRAM SUSPEND (84h) command is issued when RDY (SR[6]) is set to one or zero and ARDY (SR[5]) is set to one or zero and the LUN is not performing a PROGRAM operation then the PROGRAM SUSPEND (84h) command should be ignored (for example, R/B# stays HIGH). If a multi-plane program is executing, the PROGRAM operation for all multi-plane addresses is paused and the LUN shall make forward progress for the PROGRAM operation prior to suspending the operation.

The SUSPEND (SR[2]) bit of the status register is valid for this command after ARDY transitions from zero to one and until the next array operation transition of RDY to zero or RESET (FFh, FCh, FAh, FDh) is issued. The FAIL (SR[0]) bit of the status register is valid for this command after ARDY transitions from zero to one until the next transition of ARDY to zero. SUSPEND shall be set to one if a program was suspended successfully, in



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this case FAIL (SR[0]) shall be cleared to zero. SR[2] shall be cleared to zero if the program was completed, in this case SR[0] reflects whether the program was successful.

Table 32: PROGRAM SUSPEND (84h) Status Details

Description	SR[2]	SR[1]	SR[0]
PROGRAM completed with successful status	0	Previous program fail status	0
PROGRAM completed with fail status	0	Previous program fail status	1
PROGRAM suspended	1	X (invalid)	X (invalid)

To suspend an ongoing PROGRAM operation to a LUN, issue 84h command, then write five address cycles containing the row address (LUN, block and page address) and column addresses. Only the LUN address is required for program suspend; the block, page, and column addresses are ignored. The selected LUN status will be reflected in the status bits FAIL (SR[0]) and SUSPEND (SR[2]) in the status register after the status bit RDY is set to one. The selected LUN which the PROGRAM operation was suspended on will respond within ^tPSPD.

If issuing a program command while an ERASE operation on the same LUN is suspended, the PROGRAM operation is not allowed to be suspended.

To resume a suspended PROGRAM operation to a LUN, issue 13h command, then write five address cycles containing the row address matching the LUN in the suspended state; the block, page, and column addresses are ignored. The suspended PROGRAM operation will then resume and finish within ^tPROG.

While a program is suspended, if the host issues a RESET (FFh, FCh, FAh, FDh) command for the affected LUN, then the program that was suspended is canceled and status is cleared. With the exception of erase and program commands, all commands are allowed during suspended state (some with limitations listed in subsequent paragraphs). SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands are permitted during program suspend.

CACHE READ operations and read retry options that have a longer ^tR time are not permitted to be issued to a LUN that is in the program suspend state. Commands READ UNIQUE ID (EDh), READ OTP PAGE, and READ PARAMETER PAGE (ECh) are not allowed when the LUN is in a program suspend state.

While a program is suspended on a LUN, if host issues a PROGRAM (80h/81h-10h, 85h-10h) based command (regardless of the address) to the suspended LUN, the program command is not accepted by the LUN (R/B# goes LOW for ^tPSPDN) the LOCK status (SR[7] = 0) is set and the program that was suspended keeps its suspend state and can still be resumed. If a program based command is issued to a different LUN on the shared target then the program is performed on the selected page and the program that was suspended keeps its suspend state.

While a program is suspended, if host issues a read (00h-30h, 00h-31h, 00h-35h, 31h, 3Fh) based command to the page address (or any shared page) of the suspended program the read will be performed with data output being undefined and the program that was suspended keeps its suspend state. If host issues read command to block or LUN address other than the suspended page address then the read is performed and the program that was suspended keeps its suspend state.



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If the host issues a PROGRAM SUSPEND (84h) while there is no PROGRAM operation ongoing (including the case of the LUN already being in a program suspend state with SR[2]=1) the command should be ignored (for example, R/B# stays HIGH). If the host issues a PROGRAM RESUME (13h) while there is no PROGRAM operation ongoing or no program suspended, the NAND will respond with a t_{PSPDN} busy time.

PROGRAM SUSPEND operations are only supported in the default mode of operation (for example, not in the OTP mode of operation).

Figure 74: PROGRAM SUSPEND (84h) Operation

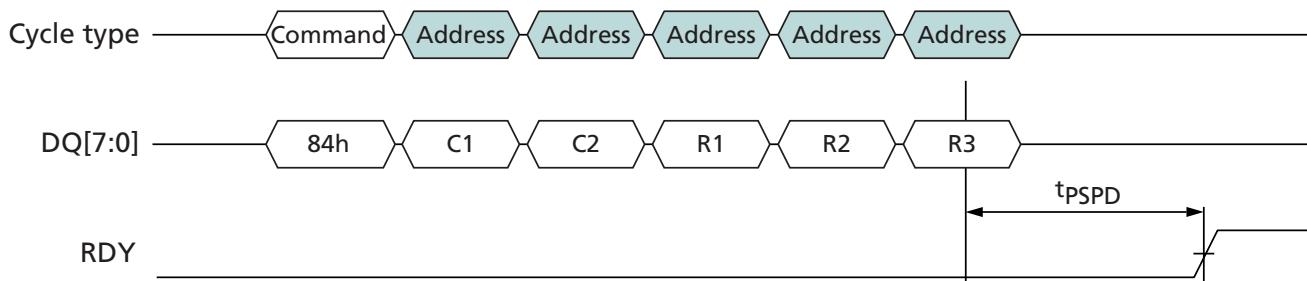
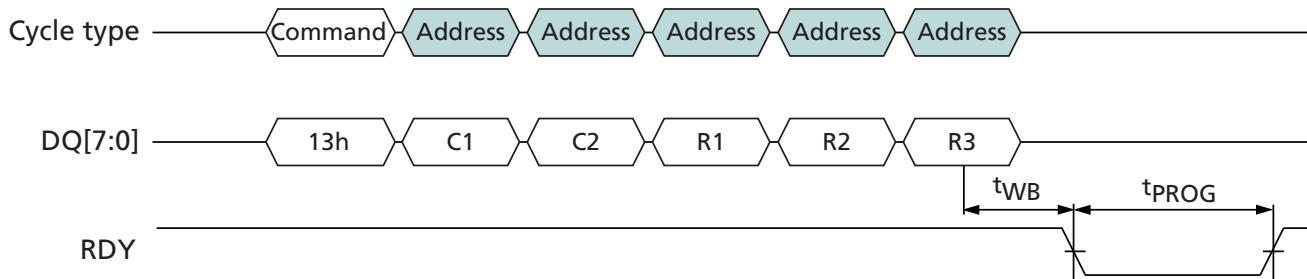


Figure 75: PROGRAM RESUME (13h) Operation





Erase Operations

ERASE operations are used to clear the contents of a block in the NAND Flash array to prepare its pages for PROGRAM operations.

Erase Operations

The ERASE BLOCK (60h-D0h) command, when not preceded by the ERASE BLOCK MULTI-PLANE (60h-D1h) command, erases one block in the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

MULTI-PLANE ERASE Operations

The ERASE BLOCK MULTI-PLANE (60h-D1h) command can be used to further system performance of ERASE operations by allowing more than one block to be erased in the NAND array. This is done by prepending one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands in front of the ERASE BLOCK (60h-D0h) command. See Multi-Plane Operations for details.

ERASE BLOCK (60h-D0h)

The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

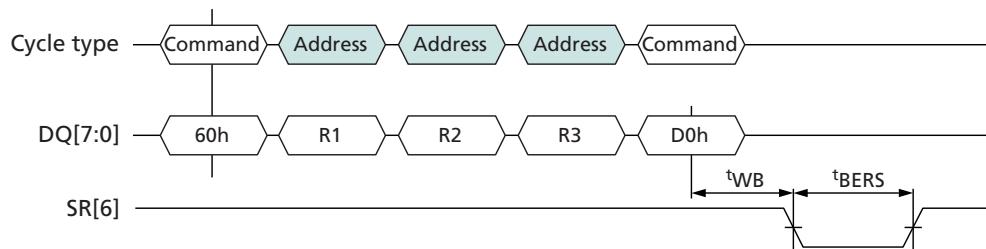
To erase a block, write 60h to the command register. Then write three address cycles containing the row address; the page address is ignored. Conclude by writing D0h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for t_{BERS} while the block is erased.

To determine the progress of an ERASE operation, the host can monitor the target's R/B# signal, or alternatively, the STATUS operations (70h, 78h) can be used. When the die (LUN) is ready (RDY = 1, ARDY = 1) the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The ERASE BLOCK (60h-D0h) command is used as the final command of a MULTI-PLANE ERASE operation. It is preceded by one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands. All of blocks in the addressed planes are erased. The host should check the status of the operation by using the STATUS operations (70h, 78h). See Multi-Plane Operations for multi-plane addressing requirements.

Figure 76: ERASE BLOCK (60h-D0h) Operation





ERASE BLOCK MULTI-PLANE (60h-D1h)

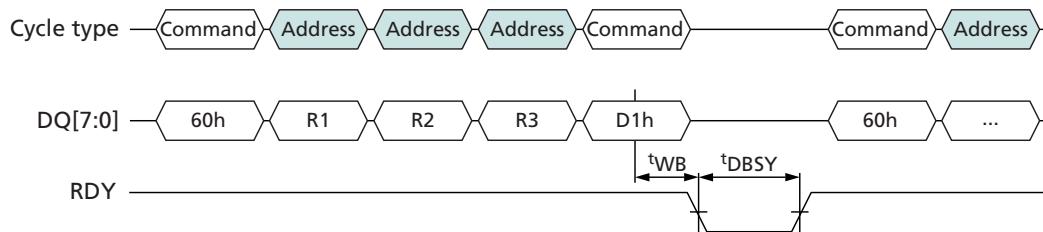
The ERASE BLOCK MULTI-PLANE (60h-D1h) command queues a block in the specified plane to be erased in the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for a block to be erased. To specify the final block to be erased and to begin the ERASE operation for all previously queued planes, issue the ERASE BLOCK (60h-D0h) command. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To queue a block to be erased, write 60h to the command register, then write three address cycles containing the row address; the page address is ignored. Conclude by writing D1h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for tDBSY.

To determine the progress of tDBSY, the host can monitor the target's R/B# signal, or alternatively, the STATUS operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1, ARDY = 1), additional ERASE BLOCK MULTI-PLANE (60h-D1h) commands can be issued to queue additional planes for erase. Alternatively, the ERASE BLOCK (60h-D0h) command can be issued to erase all of the queued blocks.

For multi-plane addressing requirements for the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Multi-Plane Operations.

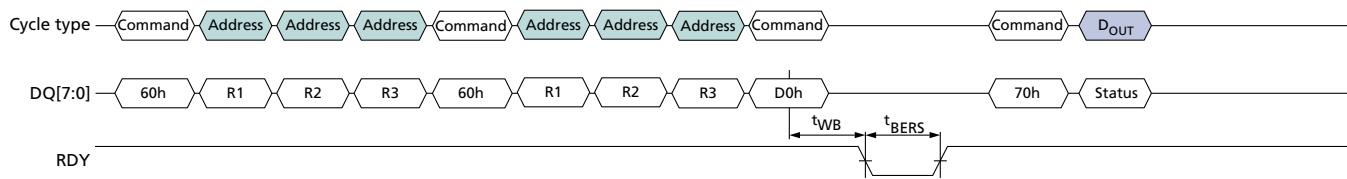
Figure 77: ERASE BLOCK MULTI-PLANE (60h-D1h) Operation



ERASE BLOCK MULTI-PLANE (60h-60h-D0h)

This operation behaves the same as the ERASE BLOCK MULTI-PLANE (60h-D1h) command followed by a ERASE BLOCK (60h-D0h) command.

Figure 78: ERASE BLOCK MULTI-PLANE (60h-60h-D0h) Operation



ERASE SUSPEND (61h) and ERASE RESUME (D2h)

The ERASE SUSPEND (61h) command is used to pause an erase in execution for the LUN specified (RDY = 0, ARDY = 0). If ERASE SUSPEND (61h) is issued when ARDY = 1 or 0 and LUN is not performing an ERASE operation then the ERASE SUSPEND (61h) command should be ignored (for example, tESPD = 0). If an interleaved erase is executing



(ERASE operations on more than one LUN on a target), the erase for the addressed LUN with the ERASE SUSPEND (61h) command is paused. The LUN shall make forward progress for the erase prior to suspending (for example, complete an erase pulse) provided the delay from the ERASE RESUME (D2h) to the subsequent ERASE SUSPEND (61h) command is longer than t_{RSESPD} . Issuing an ERASE SUSPEND (61h) command after an ERASE RESUME (D2h) with a delay shorter than t_{RSESPD} is allowed, but there may not be forward progress in the suspended ERASE operation. An ERASE operation is not allowed to be suspended more than 20 times and only 10 of the suspends per ERASE operation cannot make forward progress (for example, issued with shorter delay than t_{RSESPD}).

FAIL (SR[0]) and SUSPEND (SR[2]) of the status register are valid for this command after RDY transitions from zero to one until the next array operation transition of RDY to zero. SR[2] shall be set to one if an erase was suspended successfully, in this case SR[0] and SR[1] will be invalid. SR[2] shall be cleared to zero if the erase was completed, in this case SR[0] reflects whether the erase was successful.

To suspend an ongoing ERASE operation to a LUN, write 61h to the command register, then write three address cycles containing the row address; the page address is ignored. The selected LUN status will be reflected in the status bits FAIL (SR[0]) and SUSPEND (SR[2]) in the status register after the status bit RDY (SR[6]) is set to one.

Table 33: ERASE SUSPEND (61h) Status Details

Description	SR[2]	SR[1]	SR[0]
ERASE completed with successful status	0	X (invalid)	0
ERASE completed with fail status	0	X (invalid)	1
ERASE suspended	1	X (invalid)	X (invalid)

For multi-plane addressing requirements for the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Multi-Plane Operations.

To resume a suspended ERASE operation, issue the ERASE RESUME (D2h) or ERASE BLOCK (60h-D0h) command to the target (CE#)/LUN which has had an erase operation suspended. The suspended erase operation will then resume and finish within t_{BERS} . In the case of Multi-LUN ERASE operations that have been suspended, the ERASE RESUME (D2h) command will cause all LUNs on a target (CE#) to resume any suspended ERASE operations. However, if issuing ERASE BLOCK (60h-D0h) command to that target (CE#) instead, only the addressed LUN will resume its suspended ERASE operation.

While an erase is suspended, if the host issues a RESET (FFh, FCh, FAh) command for the affected LUN then the erase that was suspended is canceled and status is cleared. All commands are accepted during suspended state (some with limitations listed in subsequent paragraphs).

While an erase is suspended, if host issues a ERASE BLOCK (60h-D0h) command to the suspended block the suspended erase will be resumed (not restarted) and the erase that was suspended is canceled and status is cleared. If block erase is issued to different block address than suspended block then the erase is performed on the selected block and the erase that was suspended is canceled and status is cleared. If an erase is issued to a different LUN on the shared target then the erase is performed on the selected block and the erase that was suspended keeps its suspend state.

**Table 34: ERASE SUSPEND (61h) Behavior for ERASE Operations**

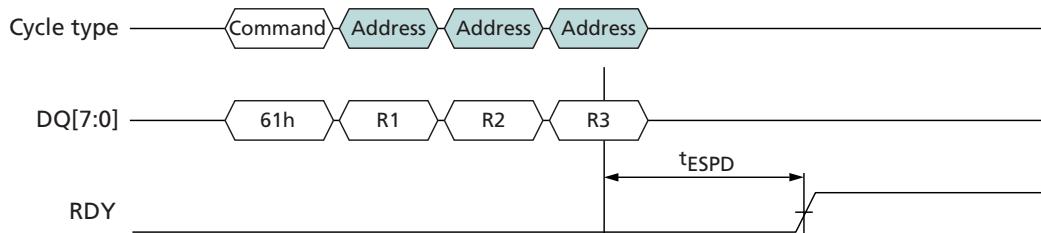
Description	Command Issued	Next State
Block A ERASE operation suspended	ERASE BLOCK to block A	Resume ERASE operation to block A
	ERASE BLOCK to block B	Start normal erase to block B and suspend to block A is canceled
	ERASE BLOCK MULTI-PLANE to block A and B	Start normal erase to block A and B
ERASE BLOCK MULTI-PLANE to block A and B suspended	ERASE BLOCK to block A	Resume ERASE operation to block A and B
	ERASE BLOCK to block B	Resume ERASE operation to block A and B
	ERASE BLOCK MULTI-PLANE to block A and B	Resume ERASE operation to block A and B
	ERASE BLOCK MULTI-PLANE to block A and D	Start normal erase to block A and D. Suspend to block B is canceled
	ERASE BLOCK MULTI-PLANE to block C and B	Start normal erase to block C and B. Suspend to block A is canceled

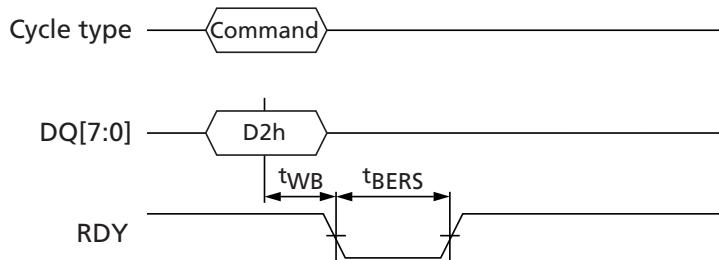
While an erase is suspended, if host issues a program command to the suspended block or in the case of multi-plane program, if at least one of the blocks addressed has a suspended erase, the program is aborted with short busy time (t_{ESPDN}) and the lock status (SR[7] = 0) is set. In this case, the erase that was suspended keeps its suspend state and can still be resumed. If host issues a program command to a block or LUN address other than the suspended block, also in case of a MULTI-PLANE PROGRAM operation, as long as the suspended block is not one of the addressed blocks, then the program is performed and the erase that was suspended keeps its suspend state.

While an erase is suspended, if host issues a read command to the suspended block the read will be performed (undefined data read out) and the erase that was suspended keeps its suspend state. If host issues read command to block or LUN address other than the suspended block then the read is performed and the erase that was suspended keeps its suspend state.

If the host issues an ERASE SUSPEND (61h) command while there is no ERASE operation ongoing the command should be ignored (for example, $t_{ESPD} = 0$). If the host issues an ERASE RESUME (D2h) command while there is no ERASE operation ongoing or no erase suspended, the NAND will respond with a t_{ESPDN} busy time. If the host issues an ERASE SUSPEND (61h) to a LUN already in erase suspend state, the command will be ignored and the erase that was suspended will stay in the erase suspend state.

It is recommended for forward progress to occur on a ERASE SUSPEND (61h) operation, the host should not issue ERASE SUSPEND (61h) command within t_{RSESPD} of a previous ERASE RESUME (D2h) command.

Figure 79: ERASE SUSPEND (61h) Operation

**Figure 80: ERASE RESUME (D2h) Operation**

Copyback Operations

COPYBACK operations make it possible to transfer data within a plane from one page to another using the cache register. This is particularly useful for block management and wear leveling.

The COPYBACK operation is a two-step process consisting of a COPYBACK READ (00h-35h) and a COPYBACK PROGRAM (85h-10h) command. To move data from one page to another on the same plane, first issue the COPYBACK READ (00h-35h) command. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host can transfer the data to a new page by issuing the COPYBACK PROGRAM (85h-10h) command. When the die (LUN) is again ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

To prevent bit errors from accumulating over multiple COPYBACK operations, it is recommended that the host read the data out of the cache register after the COPYBACK READ (00h-35h) completes prior to issuing the COPYBACK PROGRAM (85h-10h) command. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address. The host should check the data for ECC errors and correct them. When the COPYBACK PROGRAM (85h-10h) command is issued, any corrected data can be input. The CHANGE ROW ADDRESS (85h) command can be used to change the column address.

It is not possible to use the COPYBACK operation to move data from one plane to another or from one die (LUN) to another. Instead, use a READ PAGE (00h-30h) or COPYBACK READ (00h-35h) command to read the data out of the NAND, and then use a PROGRAM PAGE (80h-10h) command with data input to program the data to a new plane or die (LUN).

Between the COPYBACK READ (00h-35h) and COPYBACK PROGRAM (85h-10h) commands, the following commands are supported: STATUS operations (70h, 78h), and column address operations (05h-E0h, 06h-E0h, 85h). RESET operations (FFh, FCh) can be issued after COPYBACK READ (00h-35h), but the contents of the cache registers on the target are not valid.

Read Retry option 8-15 and Auto Read Calibration shall not be used in conjunction with COPYBACK READ (00h-35h) or COPYBACK PROGRAM (85h-10h) operations.

In devices which have more than one die (LUN) per target, once the COPYBACK READ (00h-35h) is issued, interleaved die (multi-LUN) operations are prohibited until after the COPYBACK PROGRAM (85h-10h) command is issued.

Multi-Plane Copyback Operations



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MULTI-PLANE COPYBACK READ operations improve read data throughput by copying data simultaneously from more than one plane to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the COPYBACK READ (00h-35h) command.

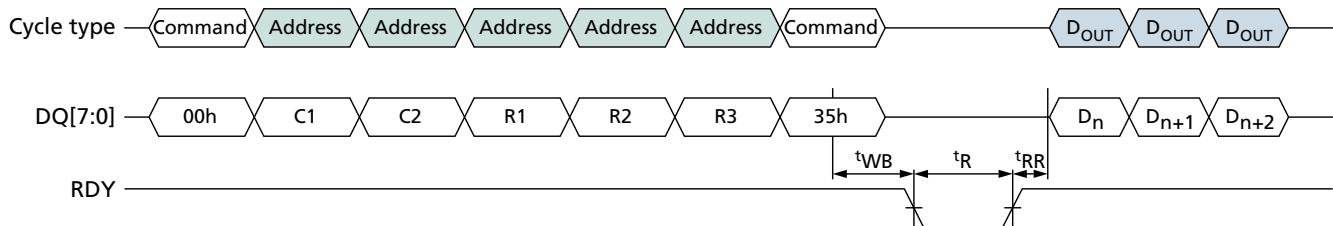
The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command can be used to further system performance of COPYBACK PROGRAM operations by enabling movement of multiple pages from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more COPYBACK PROGRAM (85h-11h) commands in front of the COPYBACK PROGRAM (85h-10h) command. See Multi-Plane Operations for details.

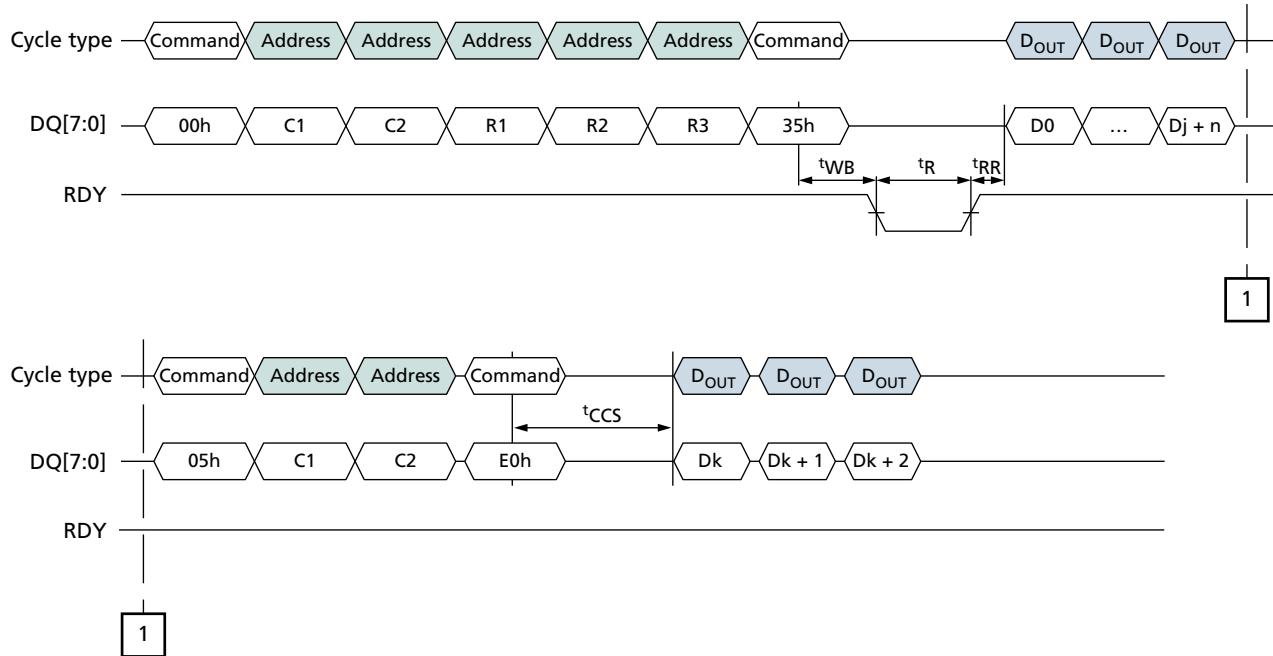
COPYBACK READ (00h-35h)

The COPYBACK READ (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except that 35h is written to the command register instead of 30h. See Read Operations - READ PAGE (00h-30h) sections for further details.

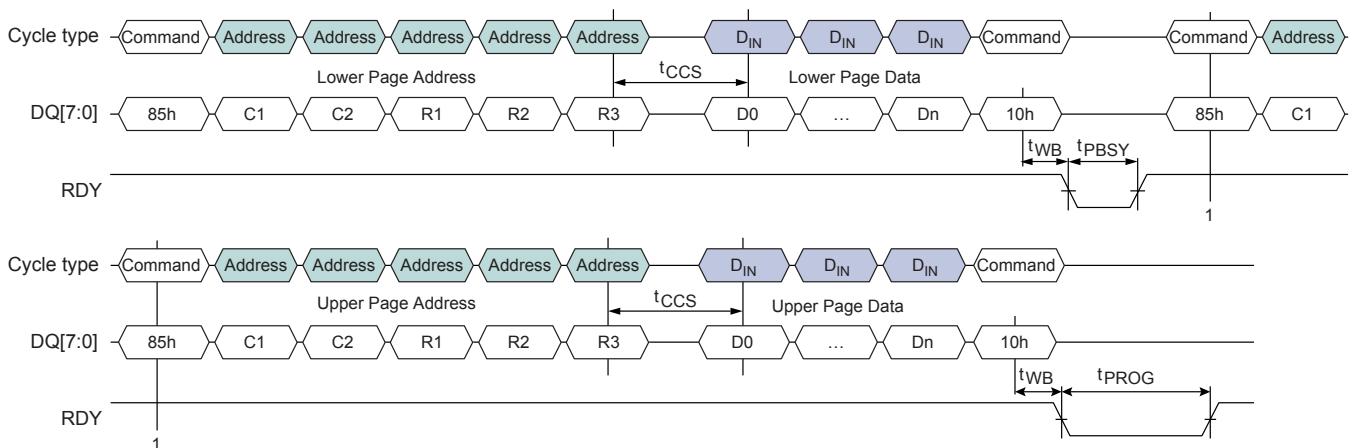
Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the COPYBACK PROGRAM (85h-10h) command to prevent the propagation of data errors.

Figure 81: COPYBACK READ (00h-35h) Operation



**Figure 82: COPYBACK READ (00h-35h) with CHANGE READ COLUMN (05h-E0h) Operation****COPYBACK PROGRAM (85h-10h)**

The COPYBACK PROGRAM (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register, cache register contents are not cleared. See PROGRAM PAGE (80h-10h) for further details.

Figure 83: COPYBACK PROGRAM (85h-10h) Operation – Single-Pass

Example command sequence for COPYBACK PROGRAM with Single Pass Programming Enabled:

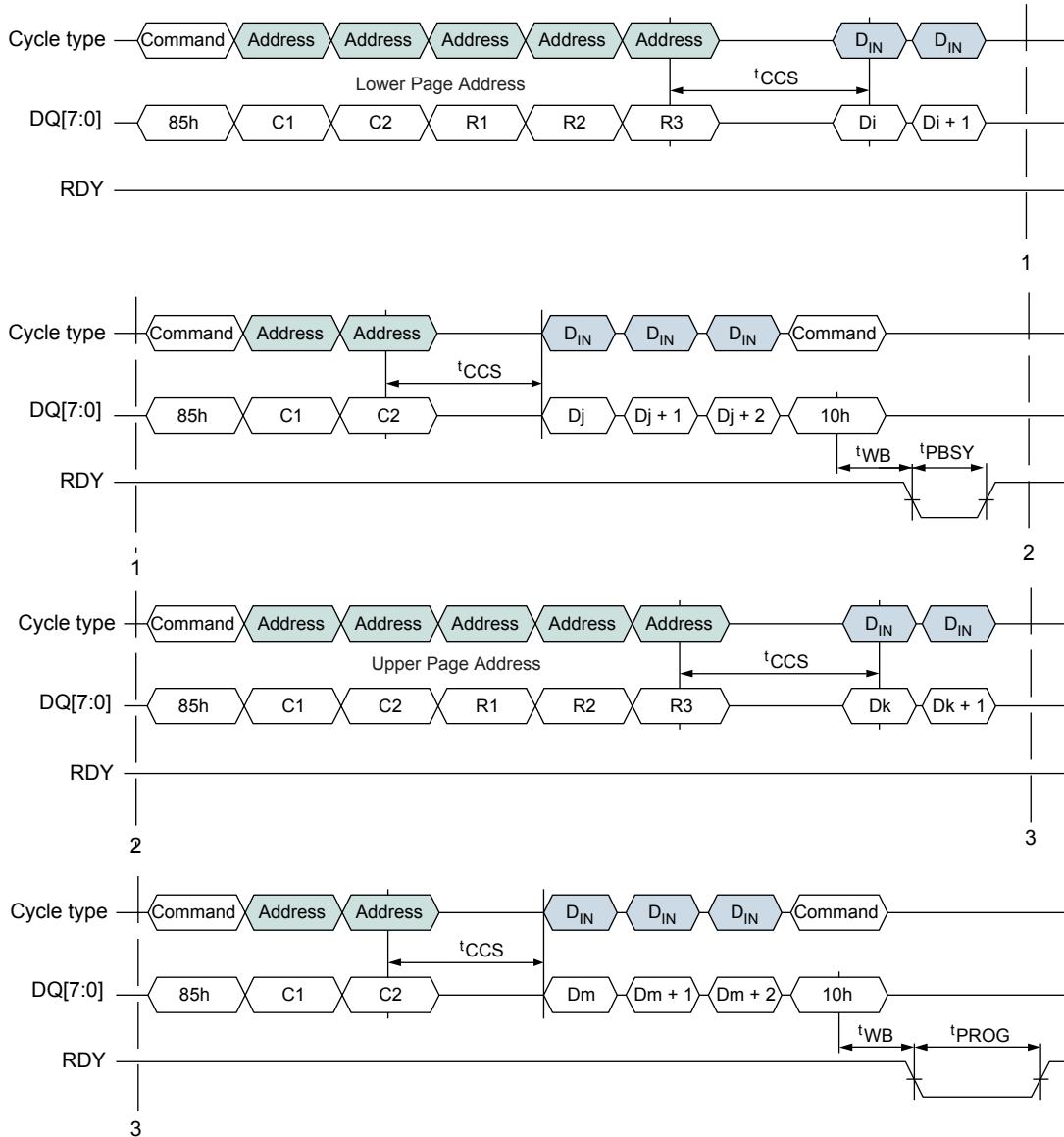


MLC 128Gb to 512Gb Async/Sync NAND Copyback Operations

1. Issue COPYBACK READ (00h-35h) (It is possible for the COPYBACK READ (00h-35h) command to address a different block or page type from the subsequent 85h command, however both the 00h-35h and 85h commands must address the same plane.)
2. Read data out and identify errors (optional)
3. Issue CHANGE WRITE COLUMN (85h) + 5 address cycles (addressed to a lower page) to address of first error and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.
4. Wait ^tPBSY
5. Issue COPYBACK READ (00h-35h) to another address
6. Read data out and identify errors (optional)
7. Issue CHANGE WRITE COLUMN (85h) + 5 address cycles (addressed to an upper page) to address of first error and enter corrected data. Repeat error correction by issuing CHANGE WRITE COLUMN (85h) + 2 column address cycles until all errors are corrected, then issue 10h command.
8. Wait ^tPROG



Figure 84: COPYBACK PROGRAM (85h-10h) with CHANGE WRITE COLUMN (85h) Operation – Single-Pass



COPYBACK READ MULTI-PLANE (00h-32h)

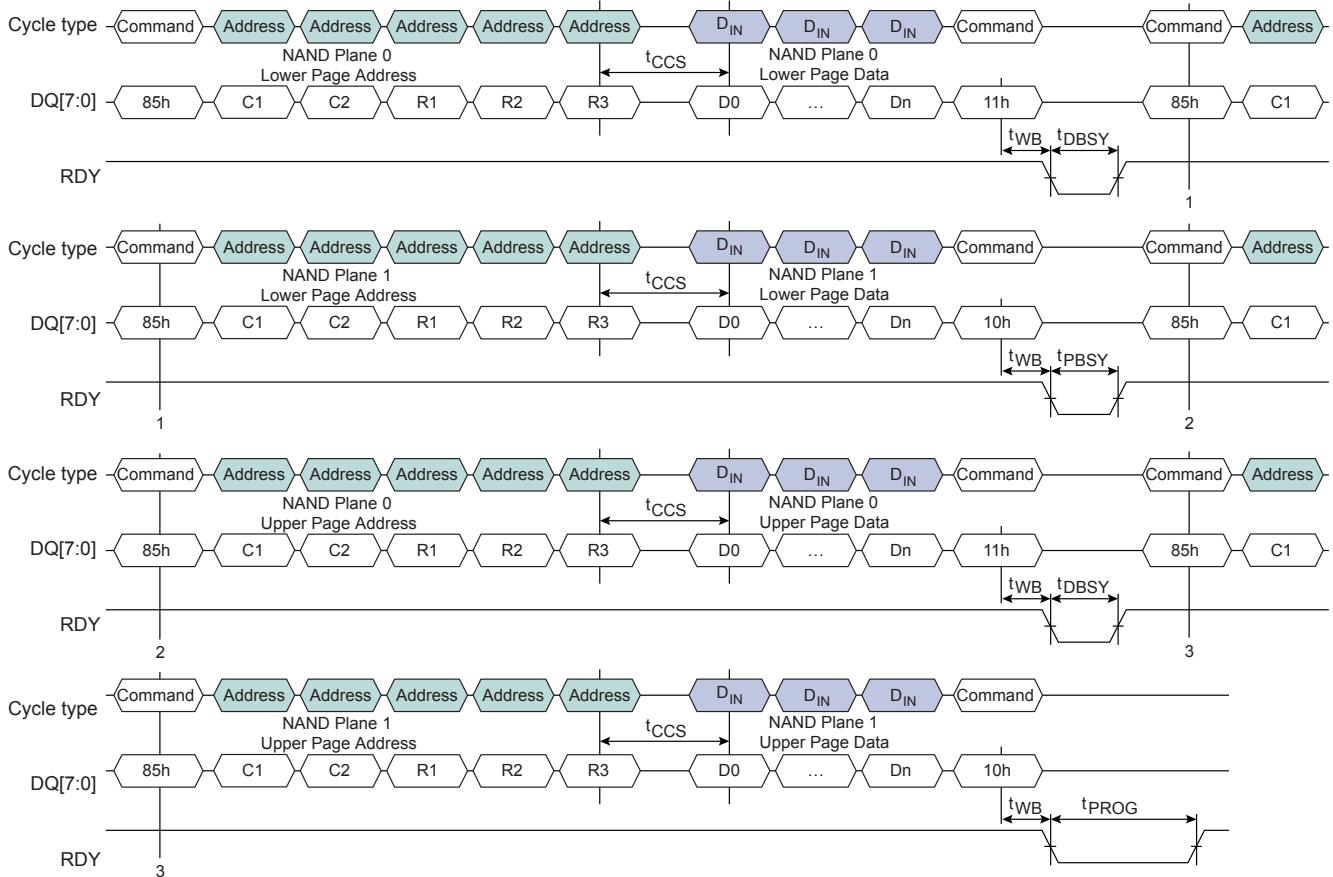
The COPYBACK READ MULTI-PLANE (00h-32h) command is functionally identical to the READ PAGE MULTI-PLANE (00h-32h) command, except that the 35h command is written as the final command. The complete command sequence for the COPYBACK READ PAGE MULTI-PLANE is 00h-32h-00h-35h. See Read Operation - READ PAGE MULTI-PLANE (00h-32h) section for further details.



COPYBACK PROGRAM MULTI-PLANE (85h-11h)

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command is functionally identical to the PROGRAM PAGE MULTI-PLANE (80h-11h) command, except that when 85h is written to the command register, cache register contents are not cleared. See PROGRAM PAGE MULTI-PLANE (80h-11h) for further details.

Figure 85: COPYBACK PROGRAM MULTI-PLANE (85h-11h) Operation – Single-Pass





One-Time Programmable Operations

This Micron NAND Flash device offers a protected, one-time programmable (OTP) NAND Flash memory area. Each target has a OTP area with a range of OTP pages (see Table 35 (page 145)); the entire range is guaranteed to be good. Customers can use the OTP area in any way they desire; typical uses include programming serial numbers or other data for permanent storage.

The OTP area leaves the factory in an erased state (all bits are 1). Programming an OTP page changes bits that are 1 to 0, but cannot change bits that are 0 to 1. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area prevents further programming of the pages in the OTP area.

Enabling the OTP Operation Mode

The OTP area is accessible while the OTP operation mode is enabled. To enable OTP operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 01h to P1, followed by three cycles of 00h to P2 through P4.

When the target is in OTP operation mode, all subsequent PAGE READ (00h-30h) and PROGRAM PAGE (80h-10h) commands are applied to the OTP area.

ERASE commands are not valid while the target is in OTP operation mode.

Programming OTP Pages

Each page in the OTP area is programmed using the PROGRAM OTP PAGE (80h-10h) command. Each page can be programmed more than once, in sections, up to the maximum number allowed (see NOP in Table 35 (page 145)). The pages in the OTP area must be programmed in ascending order.

If the host issues a PAGE PROGRAM (80h-10h) command to an address beyond the maximum page-address range, the target will be busy for ¹OBSY and the WP# status register bit will be 0, meaning that the page is write-protected.

Protecting the OTP Area

To protect the OTP area, issue the OTP PROTECT (80h-10h) command to the OTP Protect Page. When the OTP area is protected it cannot be programmed further. It is not possible to unprotect the OTP area after it has been protected.

Reading OTP Pages

To read pages in the OTP area, whether the OTP area is protected or not, issue the PAGE READ (00h-30h) command.

If the host issues the PAGE READ (00h-30h) command to an address beyond the maximum page-address range, the data output will not be valid. To determine whether the target is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command. Use of the READ STATUS ENHANCED (78h) command is prohibited while the OTP operation is in progress.

Returning to Normal Array Operation Mode

To exit OTP operation mode and return to normal array operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 00h to P1 through P4.

If the RESET (FFh) command is issued while in OTP operation mode, the target will exit OTP operation mode and enter normal operating mode. If the synchronous interface is active, the target will exit OTP operation and enable the asynchronous interface.



If the SYNCHRONOUS RESET (FCh) command is issued while in the OTP operation mode, the target will exit OTP operation mode and the synchronous interface remains active.

Table 35: OTP Area Details

Description	Value
Number of OTP pages	27
OTP protect page address	01h
OTP start page address	04h
Number of partial page programs (NOP) to each OTP page	2

PROGRAM OTP PAGE (80h-10h)

The PROGRAM OTP PAGE (80h-10h) command is used to write data to the pages within the OTP area. To program data in the OTP area, the target must be in OTP operation mode.

To use the PROGRAM OTP PAGE (80h-10h) command, issue the 80h command. Issue five address cycles including the column address, the page address within the OTP page range, and a block address of 0. Next, write the data to the cache register using data input cycles. After data input is complete, issue the 10h command.

R/B# goes LOW for the duration of the array programming time, t_{PROG} . The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. The RDY bit of the status register will reflect the state of R/B#. Use of the READ STATUS ENHANCED (78h) command is prohibited.

When the target is ready, read the FAIL bit of the status register to determine whether the operation passed or failed (see Status Operations).

The PROGRAM OTP PAGE (80h-10h) command also accepts the CHANGEWRITE COLUMN (85h) command during data input.

If a PROGRAM PAGE command is issued to the OTP area after the area has been protected, then R/B# goes LOW for t_{OBSY} . After t_{OBSY} , the status register is set to 60h.

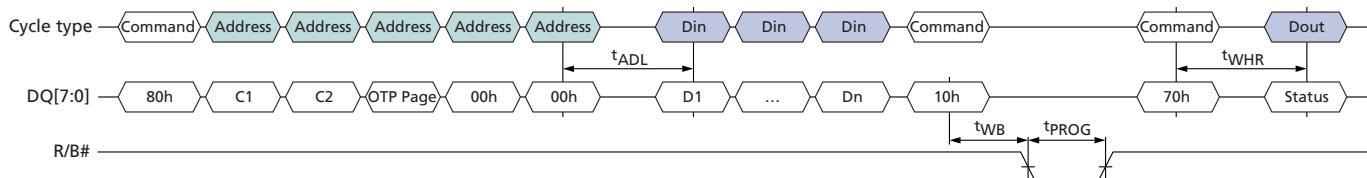
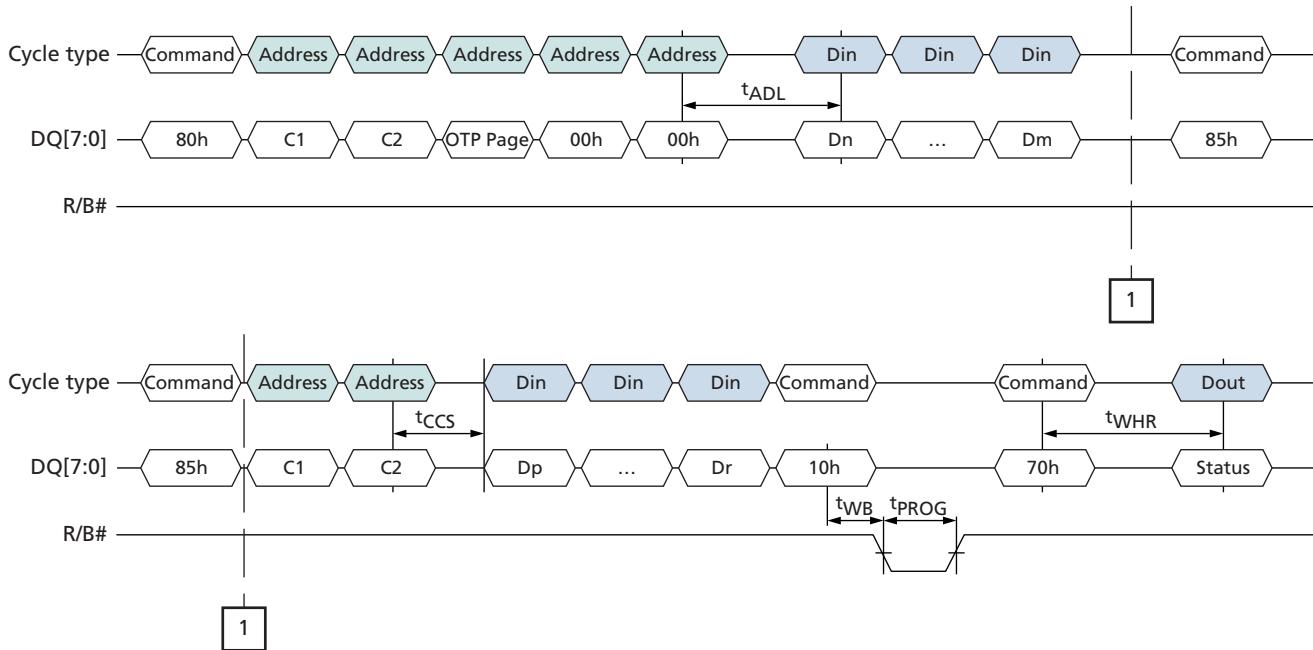
Figure 86: PROGRAM OTP PAGE (80h-10h) Operation



Figure 87: PROGRAM OTP PAGE (80h-10h) with CHANGE WRITE COLUMN (85h) Operation


PROTECT OTP AREA (80h-10h)

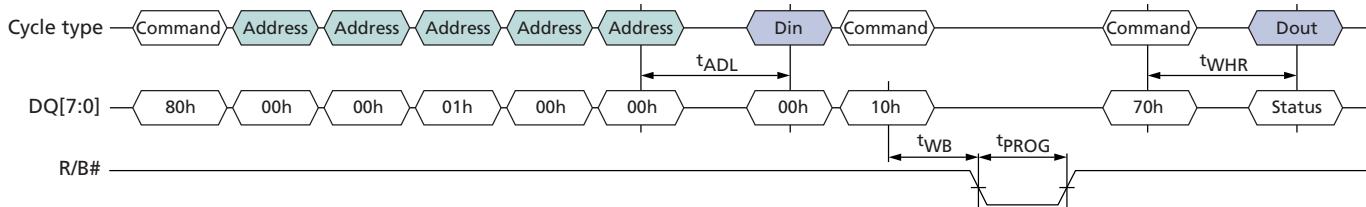
The PROTECT OTP AREA (80h-10h) command is used to prevent further programming of the pages in the OTP area. To protect the OTP area, the target must be in OTP operation mode.

To protect all data in the OTP area, issue the 80h command. Issue five address cycles including the column address, OTP protect page address and block address; the column and block addresses are fixed to 0. Next, write 00h data for the first byte location and issue the 10h command.

R/B# goes LOW for the duration of the array programming time, t_{PROG} . The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. The RDY bit of the status register will reflect the state of R/B#. Use of the READ STATUS ENHANCED (78h) command is prohibited.

When the target is ready, read the FAIL bit of the status register to determine if the operation passed or failed (see Status Operations).

If the PROTECT OTP AREA (80h-10h) command is issued after the OTP area has already been protected, R/B# goes LOW for t_{OBSY} . After t_{OBSY} , the status register is set to 60h.

**Figure 88: PROTECT OTP AREA (80h-10h) Operation**

Note: 1. OTP data is protected following a status confirmation.

READ OTP PAGE (00h-30h)

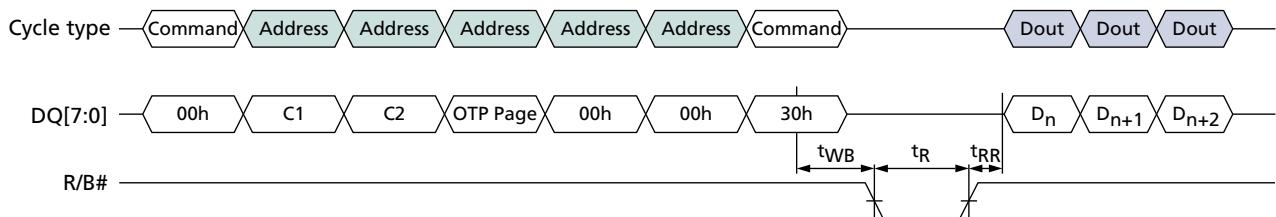
The READ OTP PAGE (00h-30h) command is used to read data from the pages in the OTP area. To read data in the OTP area, the target must be in OTP operation mode.

To use the READ OTP PAGE (00h-30h) command, issue the 00h command. Issue five address cycles including the column address, the page address within the OTP page range, and a block address of 0. Next, issue the 30h command. The selected die (LUN) will go busy ($RDY = 0$, $ARDY = 0$) for t_R as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal, or alternatively the READ STATUS (70h) command can be used. If the status operations are used to monitor the die's (LUN's) status, when the die (LUN) is ready ($RDY = 1$, $ARDY = 1$) the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, it begins at the column address specified.

Additional pages within the OTP area can be read by repeating the READ OTP PAGE (00h-30h) command.

The READ OTP PAGE (00h-30h) command is compatible with the CHANGE READ COLUMN (05h-E0h) command. Use of the READ STATUS ENHANCED (78h) and CHANGE READ COLUMN ENHANCED (06h-E0h) commands are prohibited.

Figure 89: READ OTP PAGE (00h-30h) Operation



Multi-Plane Operations

Each NAND Flash logical unit (LUN) is divided into multiple physical planes. Each plane contains a cache register and a data register independent of the other planes. The planes are addressed via the low-order block address bits. Specific details are provided in Device and Array Organization.

Multi-plane operations make better use of the NAND Flash arrays on these physical planes by performing concurrent READ, PROGRAM, or ERASE operations on multiple planes, significantly improving system performance. Multi-plane operations must be of the same type across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

When issuing MULTI-PLANE PROGRAM operation, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL=1 and/or FAILC =1), use the READ STATUS ENHANCED (78h) command—time for each plane—to determine which plane operation failed.

When issuing MULTI-PLANE ERASE operations, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL=1), use the READ STATUS ENHANCED (78h) command—time for each plane—to determine which plane operation failed.

Multi-Plane Addressing

Multi-plane commands require an address per operational plane. For a given multi-plane operation, these addresses are subject to the following requirements.

For two plane configuration:

- The LUN address bit(s) must be identical for all of the issued addresses.
- The plane select bits, BA[10:9], must be different for each issued address.
- The page address bits, PA[8:0] for MLC and PA[7:0] for SLC, must be identical for each issued address.

The READ STATUS (70h) command should be used following MULTI-PLANE PROGRAM PAGE and ERASE BLOCK operations on a single die (LUN).

Interleaved Die (Multi-LUN) Operations

In devices that have more than one die (LUN) per target, it is possible to improve performance by interleaving operations between the die (LUNs). An interleaved die (multi-LUN) operation is one that individual die (LUNs) involved may be in any combination of busy or ready status during operations.

Interleaved die (multi-LUN) operations are prohibited following RESET (FFh, FCh), identification (90h, ECh, EDh), and configuration (EEh, EFh) operations until ARDY =1 for all of the die (LUNs) on the target.

During an interleaved die (multi-LUN) operation, there are two methods to determine operation completion. The R/B# signal indicates when all of the die (LUNs) have finished their operations. R/B# remains LOW while any die (LUN) is busy. When R/B# goes HIGH, all of the die (LUNs) are idle and the operations are complete. Alternatively, the READ STATUS ENHANCED (78h) command can report the status of each die (LUN) individually.



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Use the READ STATUS ENHANCED (78h) command to monitor status for the addressed die (LUN). When multi-plane commands are used with interleaved die (multi-LUN) operations, the multi-plane commands must also meet the requirements, see Multi-Plane Operations for details. After the READ STATUS ENHANCED (78h) command has been issued, the READ STATUS (70h) command may be issued for the previously addressed die (LUN).

See Command Definitions for the list of commands that can be issued while other die (LUNs) are busy.

During an interleaved die (multi-LUN) operation that involves a PROGRAM-series (80h-10h, 80h-11h) operation and a READ operation, the PROGRAM-series operation must be issued before the READ-series operation. The data from the READ-series operation must be output to the host before the next PROGRAM-series operation is issued. This is because the 80h command clears the cache register contents of all cache registers on all planes.

During a interleaved die (multi-LUN) operation that involves PROGRAM-series (80h-10h, 80h-11h) operations between multiple die (LUNs) on the same target, after data is inputted to the first die (LUN) addressed in that interleaved die (multi-LUN) sequence, before addressing the next die (LUN) with a PROGRAM-series (80h-10h, 80h-11h) operation a program confirm command (via 80h-10h) must be issued to begin the array programming of the previous die (LUN). If this is not done by the host prior to addressing the next die (LUN), data in all the cache registers of the previously die (LUNs) will be cleared by the PROGRAM-series (80h-10h, 80h-11h) operation to the next die (LUN) in the interleaved die (multi-LUN) sequence. Utilizing the Program Clear functionality in feature address 01h can be utilized to avoid a PROGRAM-series (80h-10h, 80h-11h) operation from clearing the contents of non-addressed NAND planes.

When issuing combinations of commands to multiple die (LUNs) (e.g. Reads to one die (LUN) and Programs to another die (LUN)) or Reads to one die (LUN) and Reads to another die (LUN)), the host shall issue the READ STATUS ENHANCED (78h) command before reading data from any LUN. This ensures that only the LUN selected by the READ STATUS ENHANCED (78h) command responds to a data output cycle after being put into data output mode, and thus avoiding bus contention. After the READ STATUS ENHANCED (78h) command is issued to the selected die (LUN) a CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command shall be issued prior to any data output from the selected die (LUN).



Error Management

Each NAND Flash die (LUN) is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the die (LUNs) could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per die (LUN) will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices could contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error-correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the first spare area location and the bad-block mark.

System software should check the first spare area location on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks could be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. It is not permitted to issue any PROGRAM or ERASE operation to any identified factory bad block or any block that has reported a fail status via the NAND status register after a PROGRAM or ERASE operation. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Always check status after a PROGRAM or ERASE operation.
- Under typical conditions, use the minimum required ECC (see table below)
- Use bad-block management and wear-leveling algorithms.

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Table 36: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	2096
Total available blocks per LUN	2192
First spare area location	Byte 16,384
Bad-block mark ¹	00h

**Table 36: Error Management Details (Continued)**

Description	Requirement
Minimum required ECC	MLC: 72-bit ECC per 1162 bytes of data SLC: 72-bit ECC per 1162 bytes of data

Note: 1. Reading for the factory bad block mark in the first spare byte location of page 0 in each NAND block may only be done in the default MLC mode with randomizer enabled.

Shared Pages

In MLC NAND Flash devices, each memory cell contains two bits of data. These bits are distributed across two NAND pages. Pages within a NAND block that share the same NAND memory cells are referred to as shared pages. If any PROGRAM operation is interrupted (for example, power loss or reset), data in previously programmed shared pages can also be corrupted.

The least significant numbered shared page must be programmed before the most significant numbered page of that pair can be programmed.

Table 37: Shared Pages

| Shared Pages |
|--------------|--------------|--------------|--------------|--------------|
| 0 | - | 1 | - | 2 |
| 4 | - | 5 | - | 6 |
| 8 | - | 9 | - | 10 |
| 12 | - | 13 | - | 14 |
| 16 | 17 | 18 | 19 | 20 |
| 24 | 25 | 26 | 27 | 28 |
| 32 | 33 | 34 | 35 | 36 |
| 40 | 41 | 42 | 43 | 44 |
| 48 | 49 | 50 | 51 | 52 |
| 56 | 57 | 58 | 59 | 60 |
| 64 | 65 | 66 | 67 | 68 |
| 72 | 73 | 74 | 75 | 76 |
| 80 | 81 | 82 | 83 | 84 |
| 88 | 89 | 90 | 91 | 92 |
| 96 | 97 | 98 | 99 | 100 |
| 104 | 105 | 106 | 107 | 108 |
| 112 | 113 | 114 | 115 | 116 |
| 120 | 121 | 122 | 123 | 124 |
| 128 | 129 | 130 | 131 | 132 |
| 136 | 137 | 138 | 139 | 140 |
| 144 | 145 | 146 | 147 | 148 |
| 152 | 153 | 154 | 155 | 156 |
| | | | | 157 |
| | | | | 158 |
| | | | | 159 |

**Table 37: Shared Pages (Continued)**

Shared Pages		Shared Pages		Shared Pages		Shared Pages	
160	161	162	163	164	165	166	167
168	169	170	171	172	173	174	175
176	177	178	179	180	181	182	183
184	185	186	187	188	189	190	191
192	193	194	195	196	197	198	199
200	201	202	203	204	205	206	207
208	209	210	211	212	213	214	215
216	217	218	219	220	221	222	223
224	225	226	227	228	229	230	231
232	233	234	235	236	237	238	239
240	241	242	243	244	245	246	247
248	249	250	251	252	253	254	255
256	257	258	259	260	261	262	263
264	265	266	267	268	269	270	271
272	273	274	275	276	277	278	279
280	281	282	283	284	285	286	287
288	289	290	291	292	293	294	295
296	297	298	299	300	301	302	303
304	305	306	307	308	309	310	311
312	313	314	315	316	317	318	319
320	321	322	323	324	325	326	327
328	329	330	331	332	333	334	335
336	337	338	339	340	341	342	343
344	345	346	347	348	349	350	351
352	353	354	355	356	357	358	359
360	361	362	363	364	365	366	367
368	369	370	371	372	373	374	375
376	377	378	379	380	381	382	383
384	385	386	387	388	389	390	391
392	393	394	395	396	397	398	399
400	401	402	403	404	405	406	407
408	409	410	411	412	413	414	415
416	417	418	419	420	421	422	423
424	425	426	427	428	429	430	431
432	433	434	435	436	437	438	439
440	441	442	443	444	445	446	447
448	449	450	451	452	453	454	455
456	457	458	459	460	461	462	463

**Table 37: Shared Pages (Continued)**

Shared Pages		Shared Pages		Shared Pages		Shared Pages	
464	465	466	467	468	469	470	471
472	473	474	475	476	477	478	479
480	481	482	483	484	485	486	487
488	489	490	491	492	493	494	495
496	–	497	–	498	–	499	–
500	–	501	–	502	–	503	–
504	–	505	–	506	–	507	–
508	–	509	–	510	–	511	–

Output Drive Impedance

Because NAND Flash is designed for use in systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. The three supported settings for the output drivers for the asynchronous, NV-DDR, and NV-DDR2 interfaces are: 25 ohms, 35 ohms, and 50 ohms.

The 35 ohm output drive strength setting is the power-on default value in the asynchronous, NV-DDR, and NV-DDR2 interfaces. The host can select a different drive strength setting using the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command.

The output impedance range from minimum-to-maximum covers process, voltage, and temperature variations. Devices are not guaranteed to be at the nominal line.

Table 38: Output Drive Strength Conditions ($V_{CCQ} = 1.7\text{--}1.95V$)

Range	Process	Voltage	Temperature
Minimum	Fast-Fast	1.95V	T_{OPER} (MIN)
Nominal	Typical-Typical	1.8V	+25°C
Maximum	Slow-Slow	1.7V	T_{OPER} (MAX)

Table 39: Output Drive Strength Impedance Values ($V_{CCQ} = 1.7\text{--}1.95V$)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
25 ohms	Rpd	$V_{CCQ} \times 0.2$	11.4	25.0	44.0	Ohms
		$V_{CCQ} \times 0.5$	15.0	25.0	44.0	Ohms
		$V_{CCQ} \times 0.8$	15.0	25.0	61.0	Ohms
	Rpu	$V_{CCQ} \times 0.2$	15.0	25.0	61.0	Ohms
		$V_{CCQ} \times 0.5$	15.0	25.0	44.0	Ohms
		$V_{CCQ} \times 0.8$	11.4	25.0	44.0	Ohms

**Table 39: Output Drive Strength Impedance Values ($V_{CCQ} = 1.7\text{--}1.95V$) (Continued)**

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
35 ohms	Rpd	$V_{CCQ} \times 0.2$	16.0	35.0	61.0	Ohms
		$V_{CCQ} \times 0.5$	21.0	35.0	61.0	Ohms
		$V_{CCQ} \times 0.8$	21.0	35.0	85.3	Ohms
	Rpu	$V_{CCQ} \times 0.2$	21.0	35.0	85.3	Ohms
		$V_{CCQ} \times 0.5$	21.0	35.0	61.0	Ohms
		$V_{CCQ} \times 0.8$	16.0	35.0	61.0	Ohms
50 ohms	Rpd	$V_{CCQ} \times 0.2$	24.0	50.0	87.0	Ohms
		$V_{CCQ} \times 0.5$	30.0	50.0	87.0	Ohms
		$V_{CCQ} \times 0.8$	30.0	50.0	122.0	Ohms
	Rpu	$V_{CCQ} \times 0.2$	30.0	50.0	122.0	Ohms
		$V_{CCQ} \times 0.5$	30.0	50.0	87.0	Ohms
		$V_{CCQ} \times 0.8$	24.0	50.0	87.0	Ohms

Table 40: Pull-Up and Pull-Down Output Impedance Mismatch for Asynchronous, NV-DDR, and NV-DDR2

Drive Strength	Minimum	Maximum	Unit	Notes
25 ohms	0	4.4	Ohms	1, 2
35 ohms	0	6.2	Ohms	1, 2
50 ohms	0	8.8	Ohms	1, 2

Notes:

1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2. Test conditions: $V_{CCQ} = V_{CCQ,min}$, $V_{OUT} = V_{CCQ} \times 0.5$, T_{OPER} .

AC Overshoot/Undershoot Specifications

The supported AC overshoot and undershoot area depends on the timing mode selected by the host. NAND devices may have different maximum amplitude requirements for overshoot and undershoot than the host controller. If the host controller has more stringent requirements, termination, or other means of reducing overshoot or undershoot may be required beyond the NAND requirements.

Table 41: Asynchronous Overshoot/Undershoot Parameters

Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	1	V

**Table 41: Asynchronous Overshoot/Undershoot Parameters (Continued)**

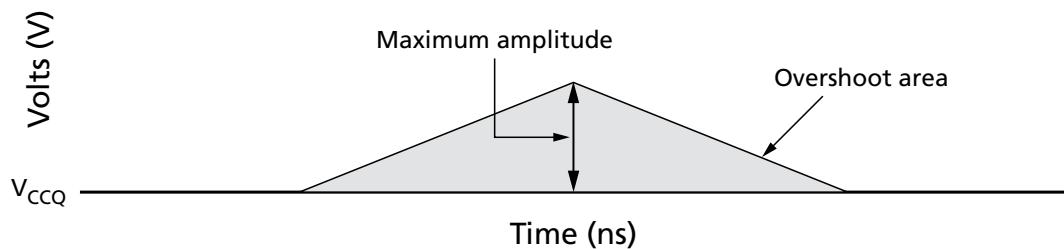
Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum overshoot area above V _{CCQ}	3	3	3	3	3	3	V-ns
Maximum undershoot area below V _{SSQ}	3	3	3	3	3	3	V-ns

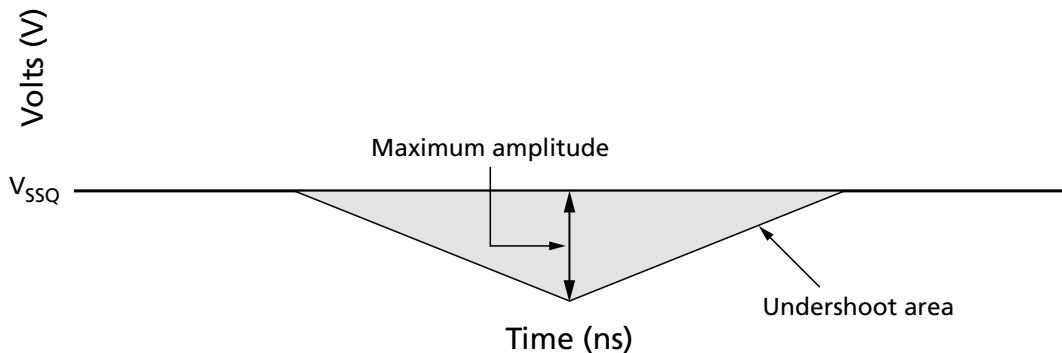
Table 42: NV-DDR Overshoot/Undershoot Parameters

Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	1	V
Maximum overshoot area above V _{CCQ}	3	3	3	2.25	1.8	1.5	V-ns
Maximum undershoot area below V _{SSQ}	3	3	3	2.25	1.8	1.5	V-ns

Table 43: NV-DDR2 Overshoot/Undershoot Parameters

Parameter	Signals	Timing Mode									Unit
		0	1	2	3	4	5	6	7	8	
Maximum peak amplitude provided for overshoot area	-	1	1	1	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	-	1	1	1	1	1	1	1	1	1	V
Maximum overshoot area above V _{CCQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	3	
Maximum undershoot area below V _{SSQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	3	

Figure 90: Overshoot

**Figure 91: Undershoot**

Input Slew Rate

Though all AC timing parameters are tested with a nominal input slew rate of 1 V/ns, it is possible to run the device at a slower slew rate. The input slew rates shown below are sampled, and not 100% tested. When using slew rates slower than the minimum values, timing must be derated by the host.

Table 44: Test Conditions for Input Slew Rate

Parameter	Value
Rising edge for setups	$V_{IL(DC)}$ to $V_{IH(AC)}$ for NV-DDR
	The last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IH(AC)min}$ for NV-DDR2
Falling edge for setups	$V_{IH(DC)}$ to $V_{IL(AC)}$ for NV-DDR
	The last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IL(AC)max}$ for NV-DDR2
Rising edge for holds	$V_{IL(DC)}$ to $V_{IH(AC)}$ for NV-DDR
	The first crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REFQ(DC)}$ for NV-DDR2
Falling edge for holds	$V_{IH(DC)}$ to $V_{IL(AC)}$ for NV-DDR
	The first crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REFQ(DC)}$ for NV-DDR2
Temperature range	T_{OPER}

The minimum and maximum input slew rate requirements that the device shall comply with below for NV-DDR operations. If the input slew rate falls below the minimum value, then derating shall be applied.

Table 45: NV-DDR Maximum and Minimum Input Slew Rate

Description	Timing Modes 0–5	Unit
Input slew rate (MIN)	0.5	V/ns
Input slew rate (MAX)	4.5	V/ns

**Table 46: Input Slew Rate Derating for NV-DDR ($V_{CCQ} = 1.7\text{--}1.95V$)**

Command/ Address and DQ Slew Rate V/ns	$\Delta t_{DS}, \Delta t_{DH}$ Derating (ps)																Unit	
	$V_{IH(AC)}/V_{IL(AC)} = V_{REF} \pm 540mV, V_{IH(DC)}/V_{IL(DC)} = V_{REF} \pm 360mV$																	
	CLK/DQS Slew Rate																	
	1 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns		0.3 V/ns			
t_{DS}		t_{DH}		t_{DS}		t_{DH}		t_{DS}		t_{DH}		t_{DS}		t_{DH}		t_{DS}		t_{DH}
1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	ps
0.9	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	ps
0.8	—	—	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	ps
0.7	—	—	—	—	0	0	0	0	0	—	—	—	—	—	—	—	—	ps
0.6	—	—	—	—	—	—	0	0	0	0	0	0	—	—	—	—	—	ps
0.5	—	—	—	—	—	—	—	—	—	0	0	0	0	180	180	—	—	ps
0.4	—	—	—	—	—	—	—	—	—	—	—	180	180	360	360	660	660	ps
0.3	—	—	—	—	—	—	—	—	—	—	—	—	660	660	920	920	920	ps

The minimum and maximum input slew rate requirements that the device shall comply with below for NV-DDR2 operations. If the input slew rate falls below the minimum value, then derating shall be applied.

Table 47: NV-DDR2 Maximum and Minimum Input Slew Rate

Description	Single Ended	Differential	Unit
Input slew rate (MIN)	1.0	2.0	V/ns
Input slew rate (MAX)	4.5	9.0	V/ns

For DQ signals when used for input, the total data setup time (t_{DS}) and data hold time (t_{DH}) required is calculated by adding a derating value to the t_{DS} and t_{DH} values indicated for the timing mode. To calculate the total data setup time, t_{DS} is incremented by the appropriate Δ set derating value. To calculate the total data hold time, t_{DH} is incremented by the appropriate Δ hold derating value. Table 48 (page 159) provides the derating values when single-ended DQS is used. Table 49 (page 159) provides the derating values when differential DQS (DQS_t/DQS_c) is used.

The setup nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IH(AC)min}$. The setup nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IL(AC)max}$. If the actual signal is always earlier than the nominal slew rate line between the shaded "V_{REFQ(DC)} to AC region", then the derating value uses the nominal slew rate shown in Figure 92 (page 160). If the actual signal is later than the nominal slew rate line anywhere between shaded "V_{REFQ(DC)} to AC region", then the derating value uses the slew rate of a tangent line to the actual signal from the AC level to the DC level shown in Figure 93 (page 160).

The hold nominal slew rate for a rising signal is defined as the slew rate between the first crossing of $V_{IL(DC)max}$ and the first crossing of $V_{REFQ(DC)}$. The hold nominal slew rate for a falling signal is defined as the slew rate between the first crossing of $V_{IH(DC)min}$ and the first crossing of $V_{REFQ(DC)}$. If the actual signal is always later than the nominal slew

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rate line between shaded "DC to $V_{REFQ(DC)}$ region", then the derating value uses the nominal slew rate shown in Figure 94 (page 161). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded "DC to $V_{REFQ(DC)}$ region", then the derating value uses the slew rate of a tangent line to the actual signal from the DC level to the $V_{REFQ(DC)}$ level shown in Figure 95 (page 161).

If the tangent line is used for derating, the setup and hold values shall be derated from where the tangent line crosses $V_{REFQ(DC)}$, not the actual signal (refer to Figure 93 (page 160) and Figure 95 (page 161)).

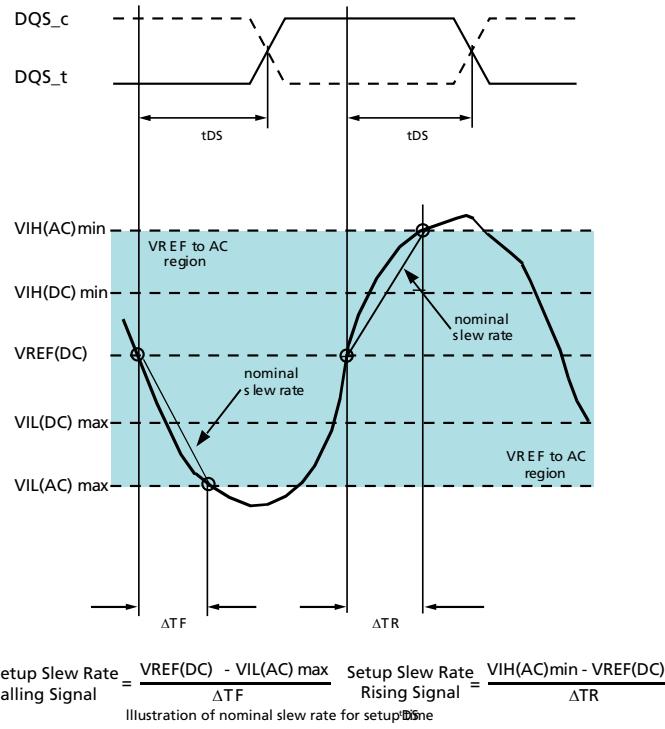
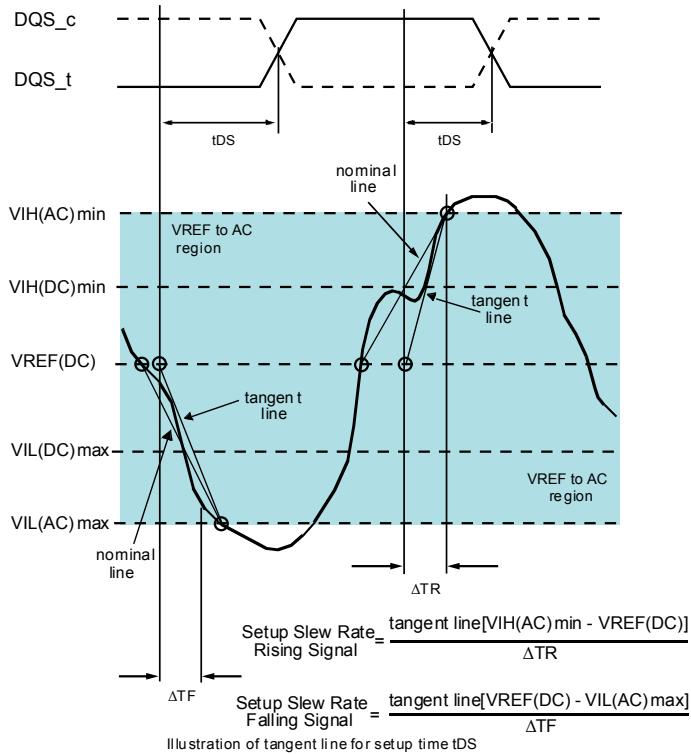
For slew rates not explicitly listed in Table 48 (page 159) and Table 49 (page 159), the derating values should be obtained by linear interpolation. These values are typically not subject to production test; the values are verified by design and characterization.

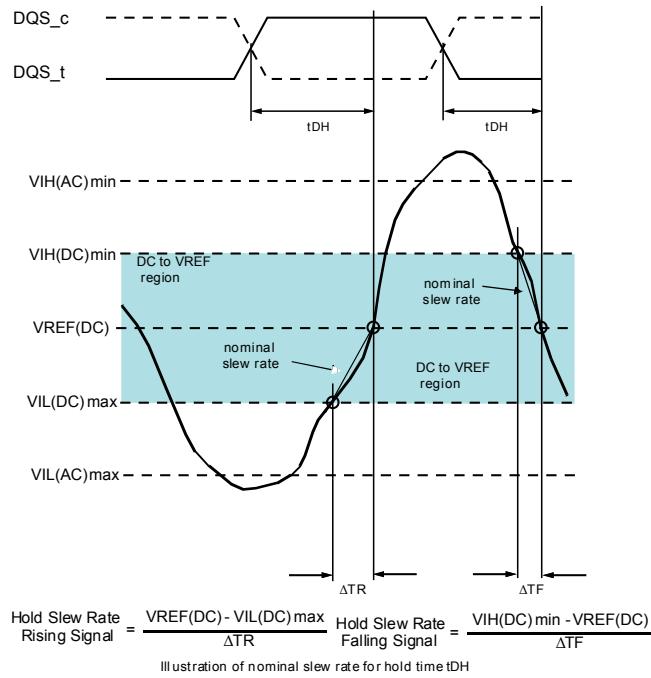
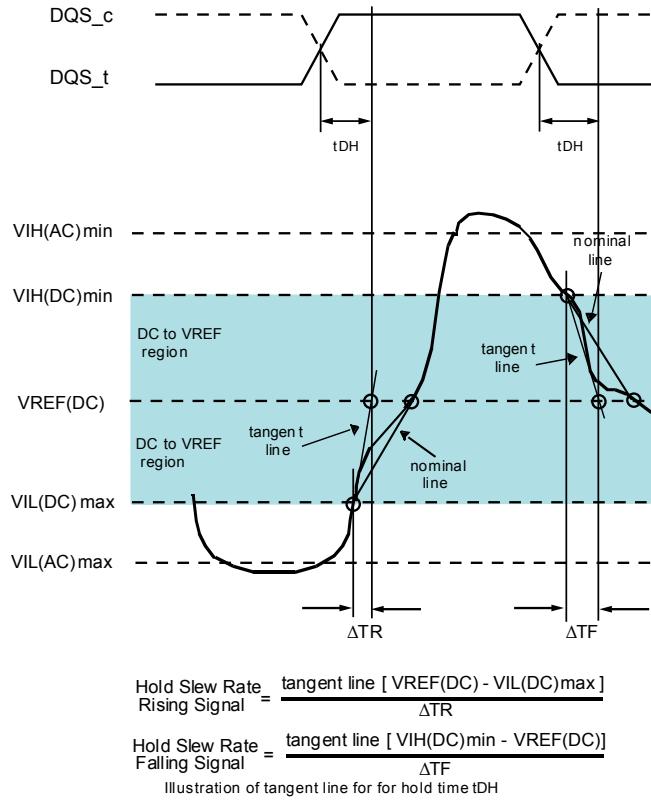

**MLC 128Gb to 512Gb Async/Sync NAND
Input Slew Rate**
Table 48: Input Slew Rate Derating for NV-DDR2 Single-Ended ($V_{CCQ} = 1.7\text{--}1.95V$)

DQ Slew Rate V/ns	$\Delta t_{DS}, \Delta t_{DH}$ Derating (ps) $V_{IH(AC)}/V_{IL(AC)} = V_{REF} \pm 250mV, V_{IH(DC)}/V_{IL(DC)} = V_{REF} \pm 125mV$																		Unit	
	ΔDQS Slew Rate																			
	2 V/ns		1.5 V/ns		1 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns			
t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}			
2	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	ps	
1.5	0	0	0	0	0	0	14	0	—	—	—	—	—	—	—	—	—	—	ps	
1	0	0	0	0	0	0	14	0	31	0	—	—	—	—	—	—	—	—	ps	
0.9	—	—	14	0	14	0	28	0	45	0	67	0	—	—	—	—	—	—	ps	
0.8	—	—	—	—	31	0	45	0	63	0	85	0	115	0	—	—	—	—	ps	
0.7	—	—	—	—	—	—	67	0	85	0	107	0	137	0	179	0	—	—	ps	
0.6	—	—	—	—	—	—	—	—	115	0	137	0	167	0	208	0	271	0	ps	
0.5	—	—	—	—	—	—	—	—	—	179	0	208	0	250	0	313	0	418	0	ps
0.4	—	—	—	—	—	—	—	—	—	—	271	0	313	0	375	0	480	0	ps	
0.3	—	—	—	—	—	—	—	—	—	—	—	—	—	418	0	480	0	594	0	ps

Table 49: Input Slew Rate Derating for NV-DDR2 Differential ($V_{CCQ} = 1.7\text{--}1.95V$)

DQ Slew Rate V/ns	$\Delta t_{DS}, \Delta t_{DH}$ Derating (ps) $V_{IH(AC)}/V_{IL(AC)} = V_{REF} \pm 250mV, V_{IH(DC)}/V_{IL(DC)} = V_{REF} \pm 125mV$																		Unit	
	DQS_t/DQS_c Slew Rate																			
	2 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1 V/ns		0.8 V/ns		0.6 V/ns					
t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}	t _{DS}	t _{DH}			
2	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ps	
1.5	0	0	7	7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ps	
1	0	0	7	7	16	16	—	—	—	—	—	—	—	—	—	—	—	—	ps	
0.9	14	14	21	21	30	30	41	41	—	—	—	—	—	—	—	—	—	—	ps	
0.8	31	31	38	38	47	47	58	58	73	73	—	—	—	—	—	—	—	—	ps	
0.7	—	—	61	61	69	69	80	80	90	90	116	116	—	—	—	—	—	—	ps	
0.6	—	—	—	—	99	99	100	100	100	100	100	100	100	100	100	100	100	—	ps	
0.5	—	—	—	—	—	150	150	150	150	150	150	150	150	150	150	150	150	150	ps	
0.4	—	—	—	—	—	—	—	—	200	200	200	200	200	200	200	200	200	200	ps	
0.3	—	—	—	—	—	—	—	—	—	225	225	225	225	225	225	225	225	225	ps	

**Figure 92: Nominal Slew Rate for Data Setup Time (t_{DS}), NV-DDR2 only****Figure 93: Tangent Line for Data Setup Time (t_{DS}), NV-DDR2 only**

**Figure 94: Nominal Slew Rate for Data Hold Time (tDH), NV-DDR2 only****Figure 95: Tangent Line for Data Hold Time (tDH), NV-DDR2 only**



Output Slew Rate

The output slew rate is tested using the following setup with only one die per DQ channel.

Table 50: Test Conditions for Output Slew Rate

Parameter	Asynchronous/ NV-DDR Interface ¹	NV-DDR2 Single-Ended ¹	NV-DDR2 Differential ¹
$V_{OL(DC)}$	$0.4 \times V_{CCQ}$	–	–
$V_{OH(DC)}$	$0.6 \times V_{CCQ}$	–	–
$V_{OL(AC)}^2$	$0.3 \times V_{CCQ}$	$V_{TT} - (V_{CCQ} \times 0.10)$	–
$V_{OH(AC)}^2$	$0.7 \times V_{CCQ}$	$V_{TT} + (V_{CCQ} \times 0.10)$	–
$V_{OLdiff(AC)}$	–	–	$-0.2 \times V_{CCQ}$
$V_{OHdiff(AC)}$	–	–	$0.2 \times V_{CCQ}$
Rising edge (t_{RISE})	$V_{OL(DC)}$ to $V_{OH(AC)}$	$V_{OL(AC)}$ to $V_{OH(AC)}$	–
Falling edge (t_{FALL})	$V_{OH(DC)}$ to $V_{OL(AC)}$	$V_{OH(AC)}$ to $V_{OL(AC)}$	–
Differential rising edge ($t_{RISE-diff}$)	–	–	$V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$
Differential falling edge ($t_{FALL-diff}$)	–	–	$V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$
Output slew rate rising edge	$[V_{OH(AC)} - V_{OL(DC)}]/t_{RISE}$	$[V_{OH(AC)} - V_{OL(AC)}]/t_{RISE}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]/t_{RISE-diff}$
Output slew rate falling edge	$[V_{OH(DC)} - V_{OL(AC)}]/t_{FALL}$	$[V_{OH(AC)} - V_{OL(AC)}]/t_{FALL}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]/t_{FALL-diff}$
Output reference load	$5pf$ to V_{SS}		
Temperature range	T_{OPER}	T_{OPER}	T_{OPER}

- Notes:
1. $1.8V V_{CCQ}$ is required for asynchronous, NV-DDR, and NV-DDR2 operations.
 2. V_{TT} is $0.5 \times V_{CCQ}$.

Table 51: Output Slew Rate for Single-Ended Asynchronous, NV-DDR, or NV-DDR2 ($V_{CCQ} = 1.7\text{--}1.95V$)

Output Drive Strength	Min	Max	Unit
25 ohms	0.85	5	V/ns
35 ohms	0.75	4	V/ns
50 ohms	0.6	4	V/ns

Table 52: Output Slew Rate for Differential NV-DDR2 ($V_{CCQ} = 1.7\text{--}1.95$)

Output Drive Strength	Min	Max	Unit
25 ohms	1.7	10.0	V/ns
35 ohms	1.5	8.0	V/ns
50 ohms	1.2	8.0	V/ns

**Table 53: Output Slew Rate Matching Ratio for NV-DDR2**

Drive Strength	Minimum	Maximum
Output slew rate matching ratio (pull-up to pull-down)	0.7	1.4

Notes:

1. The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, then divide the rising slew rate by the falling slew rate. If the falling edge is faster than the rising edge, then divide the falling slew rate by the rising slew rate.
2. The output slew rate mismatch is verified by design and characterization; it may not be subject to production testing.

Slew rates are measured under normal SSO conditions, with half of the DQ signals per data byte driving high and half of the DQ signals per data byte driving low. The output slew rate is measured per individual DQ signal.

Power Cycle and Ramp Requirements

Upon power-down the NAND device requires a maximum voltage and minimum time that the host must hold V_{CC} and V_{CCQ} below the voltage prior to power-on.

Table 54: Power Cycle Requirements

Parameter	Value	Unit
Maximum V_{CC}/V_{CCQ}	100	mV
Minimum time below maximum voltage	100	ns

The NAND device will successfully power-up over the range of V_{CC}/V_{CCQ} slew rates for the following range:

Power supply voltage = 3.3V/35ms : 0.094 mV/ μ s to 100 mV/ μ s

Power supply voltage = 1.8V/25ms: 0.072 mV/ μ s to 100 mV/ μ s



Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 55: Absolute Maximum DC Ratings by Device

Parameter	Symbol	Min ¹	Max ¹	Unit
Voltage input	V _{IN}	-0.45	2.4	V
V _{CC} supply voltage	V _{CC}	-0.6	4.6	V
V _{CCQ} supply voltage	V _{CCQ}	-0.45	2.4	V
V _{PP} supply voltage	V _{PP}	-0.6	16	V
V _{REFQ} supply voltage	V _{REFQ}	-0.45	2.4	V
Storage temperature	T _{STG}	-65	+150	°C

Note: 1. Voltage on any pin relative to V_{SS}.

Table 56: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating temperature ¹	T _{OPER}	-40	–	+85	°C
V _{CC} supply voltage ²	V _{CC}	2.7	3.3	3.6	V
V _{CCQ} supply voltage (1.8V) ²	V _{CCQ}	1.7	1.8	1.95	V
V _{REFQ} supply voltage	V _{REFQ}	0.49 x V _{CCQ}	0.5 x V _{CCQ}	0.51 x V _{CCQ}	V
V _{SS} ground voltage	V _{SS}	0	0	0	V

Notes: 1. Operating temperature (T_{OPER}) is the case surface temperature on the center/top of the NAND.
 2. AC Noise on the supply voltages shall not exceed +/- 3% (10kHz to 800MHz). AC and DC noise together shall stay within the Min-Max range specified in this table.

Table 57: Valid Blocks per LUN

Parameter	Symbol	Min	Max	Unit	Notes
Valid block number	NVB	2096	2192	Blocks	1

Note: 1. Invalid blocks are blocks that contain one or more bad bits beyond ECC. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid from the factory.



Package Electrical Specification and Pad Capacitance

The capacitance delta values in Table 58 (page 165) measure the pin-to-pin capacitance for all LUNs within a package, including across data buses if the package has the same number of LUNs per x8 data bus (i.e. package channel). The capacitance delta values are not measured across data buses if the package has a different number of LUNs per x8 data bus.

For Table 59 (page 165) Z_{IO} applies to DQ[7:0], DQS_t, DQS_c, RE_t and RE_c. $Td_{IO\ RE}$ applies to RE_t and RE_c. Td_{IO} and $Td_{IO\ Mismatch}$ applies to DQ[7:0], DQS_t and DQS_c. Mismatch and Delta values are required to be met across same data bus on given package (i.e. package channel), but not required across all channels on a given package. All other pins only need meet requirements described in Table 58 (page 165). The DQ[7:0], DQS_t, DQS_c, RE_t and RE_c pins only need to meet the requirements in Table 59 (page 165).

For each signal group defined below for Table 58 (page 165), a typical capacitance value is defined and reported for each NAND Target within a package. The signal groups include all signal group pins in a single package even if the pins belong to separate I/O channels unless the package has a different number of LUNs per x8 data bus. If the package has a different number of LUNs per x8 data bus then the signal group pins are separated per each x8 data bus.

- Signal groups for Table 58 (page 165):
 - CLK: CLK (NV-DDR only)
 - Inputs: ALE, CLE, WE#
 - Other: CE#, WP#

Table 58: Input Capacitance: 132-Ball BGA Package

Description	Symbol	Single Die/Dual Die Package			Quad Die Package			Unit	Notes
		Min	Typ	Max	Min	Typ	Max		
Input capacitance (CLK/WE#)	C_{CK}	2.5	3.5	4.5	4.4	5.9	7.4	pF	3
Input capacitance (ALE, CLE)	C_{IN}	2.5	3.5	4.5	4.2	5.7	7.2	pF	3
Input capacitance (CE#, WP#)	C_{OTHER}	–	–	4.5	–	–	7.0	pF	
Delta input capacitance	DC_{IN}	–	–	1.4	–	–	1.7	pF	

Notes:

1. Verified in device characterization; not 100% tested.
2. Test conditions: $T_A = 25^\circ\text{C}$, $f = 100\text{ MHz}$, $V_{IN} = 0\text{V}$.
3. Values for C_{CK} , C_{IN} and C_{IO} (TYP) are estimates.

Table 59: Package Electrical Specifications

Description	Symbol	<= 400MT/s			533MT/s			Unit	Notes
		Min	Typ	Max	Min	Typ	Max		
Input/Output Z_{PKG}	Z_{IO}	35	–	90	35	–	90	Ohms	1

**Table 59: Package Electrical Specifications (Continued)**

Description	Symbol	<= 400MT/s			533MT/s			Unit	Notes
		Min	Typ	Max	Min	Typ	Max		
Delta Z _{PKG} for DQS_t and DQS_c	DZ _{IO} DQS	–	–	10	–	–	10	Ohms	2
Input/Output Package delay	Td _{IO}	–	–	160	–	–	160	ps	1
RE# Package delay	Td _{IO RE}	–	–	160	–	–	160	ps	
Input/Output Package delay mismatch	Td _{IO Mismatch}	–	–	50	–	–	40	ps	6
Delta package delay for DQS_t and DQS_c	DZd _{IO} DQS	–	–	10	–	–	10	ps	
Delta Z _{PKG} for RE_t and RE_c	DZ _{IO RE}	–	–	10	–	–	10	Ohms	
Delta package delay for RE_t and RE_c	DC _{IO}	–	–	10	–	–	10	ps	

- Notes:
1. Z_{IO} applies to DQ[7:0], DQS_t, DQS_c, RE_t and RE_c.
 2. Td_{IO} applies to DQ[7:0], DQS_t, and DQS_c.
 3. Test conditions: T_{OPER} = 25°C, f = 100 MHz, V_{IN} = 0V.
 4. Verified in device characterization; not 100% tested. The package parasitic (L & C) are validated using package only samples. The capacitance is measured with V_{CC}, V_{CCQ}, V_{SS}, V_{SSQ} shorted with all other signal pins floating. The inductance is measured with V_{CC}, V_{CCQ}, V_{SS}, and V_{SSQ} shorted and all other signal pins shorted at the die side (not pin).
 5. Package only impedance (Z_{PKG}) is calculated based on the L_{PKG} and C_{PKG} total for a given pin where: Z_{PKG} (total per pin) = SQRT(L_{PKG}/C_{PKG}).
 6. Mismatch for Td_{IO} (Td_{IO Mismatch}) is calculated based on L_{PKG} and C_{PKG} total for a given pin where: Td_{PKG}(total per pin) = SQRT(L_{PKG} * C_{PKG}).
 7. Package only delay (T_{PKG}) is calculated based on L_{PKG} and C_{PKG} total for a given pin where: Td_{PKG}(total per pin) = SQRT(L_{PKG}*C_{PKG}).
 8. Delta for DQS is Absolute value of Z_{IO}(DQS_t - Z_{IO}(DQS_c)) for impedance (Z) or absolute value of Td_{IO}(DQS_t) - Td_{IO}(DQS_c) for delay (Td).
 9. Delta for RE is Absolute value of Z_{IO}(RE_t - Z_{IO}(RE_c)) for impedance (Z) or absolute value of Td_{IO}(RE_t) - Td_{IO}(RE_c) for delay (Td).

Table 60: LUN Pad Specifications

Description	Symbol	<= 400MT/s			533MT/s			Unit	Notes
		Min	Typ	Max	Min	Typ	Max		
Input/Output Pad capacitance	C_Pad _{IO}	–	–	1.65	–	–	1.65	pF	1
Delta Input/Output Pad capacitance for DQS_t and DQS_c	D_C_Pad _{IO} DQS	0	–	0.2	0	–	0.2	pF	4
Delta Input/Output Pad capacitance for RE_t and RE_c	D_C_Pad _{IO} RE	0	–	0.2	0	–	0.2	pF	5

- Notes:
1. LUN Pad capacitances apply to DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c. All other LUN pads only need to meet ONFI legacy capacitance requirements.



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2. Verified in device characterization; not 100% tested. These parameters are not subject to a production test. They are verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with V_{CC} , V_{CCQ} , V_{SS} , and V_{SSQ} applied and all other pins floating (except the pin under test).
3. These parameters apply to monolithic LUN, obtained by de-embedding the package L & C parasitics.
4. Delta for DQS is Absolute value of $C_{PAD_{IO}}(DQS_t) - C_{PAD_{IO}}(DQS_c)$.
5. Delta for RE is Absolute value of $C_{PAD_{IO}}(RE_t) - C_{PAD_{IO}}(RE_c)$.



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – DC Characteristics and Operating Conditions (Asynchronous)

Electrical Specifications – DC Characteristics and Operating Conditions (Asynchronous)

Table 61: DC Characteristics and Operating Conditions (Asynchronous Interface)

Parameter	Conditions	Symbol	Min ¹	Single-Plane Typ ¹	Two-Plane Typ ¹	Four-Plane Typ ¹	Max ¹	Unit
Array read current (active)	–	I _{CC1_A}	–	30	38	51	75	mA
	–	I _{CCQ1_A}	–	2	2	2	5	
Array program current (active)	–	I _{CC2_A}	–	32	38	51	75	mA
	–	I _{CCQ2_A}	–	2.5	2.5	2.5	8	
Erase current (active)	–	I _{CC3_A}	–	24	29	38	75	mA
		I _{CCQ3_A}	–	2	2	2	5	
I/O burst read current	t _{RC} = t _{RC} (MIN); I _{OUT} = 0mA	I _{CC4R_A}	–	8	8	8	10	mA
		I _{CCQ4R_A}	–	5	5	5	7	
I/O burst write current	t _{WC} = t _{WC} (MIN)	I _{CC4w_A}	–	8	8	8	12	mA
		I _{CCQ4w_A}	–	6	6	6	12	
Bus idle current	–	I _{CC5_A}	–	5	5	5	7	mA
		I _{CCQ5_A}	–	5	5	5	7	mA
Current during first RESET command after power-on	–	I _{CC6}	–	33	33	33	49	mA
Power-up peak current (V _{CC})	–	I _{CC_Peak_Up}	–	–	–	–	20	mA
Power-down peak current(V _{CC})	–	I _{CC_Peak_Down}	–	–	–	–	20	mA
Power-up peak current (V _{CCQ})	–	I _{CCQ_Peak_Up}	–	–	–	–	10	mA
Power-down peak current (V _{CCQ})	–	I _{CCQ_Peak_Down}	–	–	–	–	15	mA
Standby current – V _{CC}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SB}	–	15	15	15	75	µA
Standby current – V _{CCQ}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SBQ}	–	5	5	5	50	µA
Staggered power-up current	t _{RISE} = 1ms; C _{LINE} = 0.1µF	I _{ST}	–	–	–	–	10	mA

- Notes:
1. All values are per die (LUN) unless otherwise specified.
 2. During I_{SBQ} testing, DQS_t/DQS_c, RE_t/RE_c, and DQ[7:0] are floating.
 3. For the I_{CC_Peak} and I_{CCQ_Peak} currents the entire duration of the operation should be considered when calculating the maximum average current of the worst case 1µs subset of the operation.



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – DC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Electrical Specifications – DC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 62: DC Characteristics and Operating Conditions (NV-DDR Interface) 1.8V V_{CCQ}

Parameter	Conditions	Symbol	Min ¹	Single-Plane Typ ¹	Two-Plane Typ ¹	Four-Plane Typ ¹	Max ¹	Unit
Array read current (active)	CE# = V _{IL} ; tCK = tCK (MIN) or tRC = tRC (MIN) – I _{CC1_S} –	I _{CC1_S}	–	31	39	54	75	mA
		I _{CCQ1_S}	–	2				
Array program current (active)	tCK = tCK (MIN) or tDSC = tDSC (MIN) tCK = tCK (MIN) or tDSC = tDSC (MIN)	I _{CC2_S}	–	32	37	49	75	mA
		I _{CCQ2_S}	–	2.5				
Erase current (active)	tCK = tCK (MIN)	I _{CC3_S}	–	25	35	39	75	mA
		I _{CCQ3_S}	–	2				
I/O burst read current	tCK = tCK (MIN) or tRC = tRC (MIN); I _{OUT} = 0mA	I _{CC4R_S}	–	6				mA
		I _{CCQ4R_S}	–	25				
I/O burst write current	tCK = tCK (MIN) or tDSC = tDSC (MIN)	I _{CC4W_S}	–	7				mA
		I _{CCQ4W_S}	–	13				
Bus idle current	tCK = tCK (MIN) in NV-DDR	I _{CC5_S}	–	5				mA
		I _{CCQ5_S}	–	5				
Power-up peak current (V _{CC})	–	I _{CC_Peak_Up}	–	–				mA
Power-up peak current (V _{CCQ})	–	I _{CCQ_Peak_Up}	–	–				mA
Power-down peak current (V _{CC})	–	I _{CC_Peak_Down}	–	–				mA
Power-down peak current (V _{CCQ})	–	I _{CCQ_Peak_Down}	–	–				mA
Standby current – V _{CC}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SB}	–	15				μA
Standby Current – V _{CCQ}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SBQ}	–	5				μA

- Notes:
1. All values are per die (LUN) unless otherwise specified.
 2. During I_{SBQ} testing, DQS_t/DQS_c, RE_t/RE_c, and DQ[7:0] are floating.
 3. I_{CCQ1} only occurs for the first 20μs of a read command and I_{CCQ2} last 20μs of a program command.
 4. For the I_{CC_Peak} and I_{CCQ_Peak} currents the entire duration of the operation should be considered when calculating the maximum average current of the worst case 1μs subset of the operation.



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – DC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 63: DC Characteristics and Operating Conditions (NV-DDR2 Interface) 1.8V V_{CCQ}

Parameter	Conditions	Symbol	Min¹	Single-Plane Typ¹	Two-Plane Typ¹	Four-Plane Typ¹	Max¹	Unit
Array read current (active)	CE# = V _L ; t _{CK} = t _{CK} (MIN) or t _{RC} = t _{RC} (MIN)	I _{CC1_S}	–	31	39	53	75	mA
		I _{CCQ1_S}	–	2			5	
Array program current (active)	t _{CK} = t _{CK} (MIN) or t _{DSC} = t _{DSC} (MIN)	I _{CC2_S}	–	32	37	49	75	mA
		I _{CCQ2_S}	–	2.5			8	
Erase current (active)	t _{CK} = t _{CK} (MIN)	I _{CC3_S}	–	24	35	38	75	mA
		I _{CCQ3_S}	–	2			5	
I/O burst read current	t _{CK} = t _{CK} (MIN) or t _{RC} = t _{RC} (MIN); I _{OUT} = 0mA	I _{CC4R_S}	–	8 ³			12 ³	mA
				12 ⁴			14 ⁴	
				15 ⁵			18 ⁵	
		I _{CCQ4R_S}	–	23 ³			31 ³	mA
				43 ⁴			50 ⁴	
				56 ⁵			81 ⁵	
I/O burst write current	t _{CK} = t _{CK} (MIN) or t _{DSC} = t _{DSC} (MIN)	I _{CC4W_S}	–	6 ³			9 ³	mA
				10 ⁴			16 ⁴	
				12 ⁵			21 ⁵	
		I _{CCQ4W_S}	–	14 ³			16 ³	mA
				21 ⁴			32 ⁴	
				26 ⁵			43 ⁵	
Bus idle current	t _{CK} = t _{CK} (MIN) in NV-DDR	I _{CC5_S}	–	5			7	mA
		I _{CCQ5_S}	–	5			7	mA
Power-up peak current (V _{CC})	–	I _{CC_Peak_Up}	–	–			20	mA
Power-up peak current (V _{CCQ})	–	I _{CCQ_Peak_Up}	–	–			10	mA
Power-down peak current (V _{CC})	–	I _{CC_Peak_Down}	–	–			20	mA
Power-down peak current (V _{CCQ})	–	I _{CCQ_Peak_Down}	–	–			15	mA
Standby current – V _{CC}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SB}	–	15			75	µA
Standby current – V _{CCQ}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SBQ}	–	5			50	µA

- Notes:
1. All values are per die (LUN) unless otherwise specified.
 2. During I_{SBQ} testing, DQS_t/DQS_c, RE_t/RE_c, and DQ[7:0] are floating.
 3. For speeds up to 200 MT/s.
 4. For speeds greater than 200 MT/s up to 400 MT/s.
 5. For speeds greater than 400 MT/s.



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6. I_{CCQ1} only occurs for the first 20 μ s of a read command and I_{CCQ2} last 20 μ s of a program command.
7. For the I_{CC_Peak} and I_{CCQ_Peak} currents the entire duration of the operation should be considered when calculating the maximum average current of the worst case 1 μ s subset of the operation.



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Electrical Specifications – DC Characteristics and Operating Conditions (V_{CCQ})

Table 64: Asynchronous/NV-DDR DC Characteristics and Operating Conditions (1.8V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	CE#, DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#), WP#	$V_{IH(AC)}$	$0.8 \times V_{CCQ}$	–	See note	V	1
AC input low voltage		$V_{IL(AC)}$	See note	–	$0.2 \times V_{CCQ}$	V	
DC input high voltage	DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#)	$V_{IH(DC)}$	$0.7 \times V_{CCQ}$	–	$V_{CCQ} + 0.3$	V	
DC input low voltage		$V_{IL(DC)}$	-0.3	–	$0.3 \times V_{CCQ}$	V	
Input leakage current	Any input $V_{IN} = 0V$ to V_{CCQ}	I_{LI}	–	–	± 10	μA	2
Output leakage current	DQ are disabled; $V_{OUT} = V_{CCQ}$	I_{LO_pd}	–	0.3	1	μA	4
	DQ are disabled; $V_{OUT} = 0V$	I_{LO_pu}	–	0.9	5	μA	
Output low current (R/B#)	$V_{OL} = 0.2V$	I_{OL} (R/B#)	3	4	–	mA	3

- Notes:
1. See AC Overshoot/Undershoot Specifications AC Overshoot and Undershoot requirements.
 2. All leakage currents are per die (LUN). For example, two die (LUNs) have a maximum leakage current of $\pm 20\mu A$ and four die (LUNs) have a maximum leakage current of $\pm 40\mu A$.
 3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See Feature Address 81h: Programmable R/B# Pull-Down Strength table in Configuration Operations section for additional details.
 4. Absolute leakage value per I/O per NAND die (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

Table 65: NV-DDR2 DC Characteristics and Operating Conditions for Single-Ended Signals (1.8V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	$V_{IH(AC)}$	$V_{REFQ} + 0.250$	–	See note	V	4
AC input low voltage		$V_{IL(AC)}$	See note	–	$V_{REFQ} - 0.250$	V	
AC input high voltage	CE#, WP#	$V_{IH(AC)}$	$0.8 \times V_{CCQ}$	–	See note	V	4
AC input low voltage		$V_{IL(AC)}$	See note	–	$0.2 \times V_{CCQ}$	V	
DC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	$V_{IH(DC)}$	$V_{REFQ} + 0.125$	–	$V_{CCQ} + 0.3$	V	2
DC input low voltage		$V_{IL(DC)}$	-0.3	–	$V_{REFQ} - 0.125$	V	
DC input high voltage	CE#, WP#	$V_{IH(DC)}$	$0.7 \times V_{CCQ}$	–	$V_{CCQ} + 0.3$	V	
DC input low voltage		$V_{IL(DC)}$	-0.3	–	$0.3 \times V_{CCQ}$	V	
Input leakage current	Any input $V_{IN} = 0V$ to V_{CCQ}	I_{LI}	–	–	± 10	μA	1
Output leakage current	DQ are disabled; $V_{OUT} = V_{CCQ}$	I_{LO_pd}	–	0.3	1	μA	5
	DQ are disabled; $V_{OUT} = 0V$	I_{LO_pu}	–	0.9	5	μA	
Output low current (R/B#)	$V_{OL} = 0.2V$	I_{OL} (R/B#)	3	4	–	mA	3



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Table 65: NV-DDR2 DC Characteristics and Operating Conditions for Single-Ended Signals (1.8V V_{CCQ}) (Continued)

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
V_{REFQ} leakage current	$V_{REFQ} = V_{CCQ}/2$ (all other pins not under test = 0V)	I_{VREFQ}	–	–	± 5	μA	

- Notes:
1. All leakage currents are per die (LUN). For example, two die (LUNs) have a maximum leakage current of $\pm 20\mu A$ and four die (LUNs) have a maximum leakage current of $\pm 40\mu A$.
 2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)max}$, $V_{IL(DC)min}$] for single-ended signals as well as the limitations for overshoot and undershoot.
 3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See Feature Address 81h: Programmable R/B# Pull-Down Strength table in Configuration Operations section for additional details.
 4. See AC Overshoot/Ubershoot Specifications AC Overshoot and Undershoot requirements.
 5. Absolute leakage value per I/O per NAND die (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

Table 66: NV-DDR2 DC Characteristics and Operating Conditions for Differential Signals (1.8V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
Differential AC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	$V_{IHdiff(AC)}$	$2 \times [V_{IH(AC)} - V_{REF}]$	–	See note	V	2
Differential AC input low voltage		$V_{ILdiff(AC)}$	See note	–	$2 \times [V_{REF} - V_{IL(AC)}]$	V	2
Differential DC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	$V_{IHdiff(DC)}$	$2 \times [V_{IH(DC)} - V_{REF}]$	–	See note	V	2
Differential DC input low voltage		$V_{ILdiff(DC)}$	See note	–	$2 \times [V_{REF} - V_{IL(DC)}]$	V	2
Input leakage current	Any input $V_{IN} = 0V$ to V_{CCQ}	I_{LI}	–	–	± 10	μA	1
Output leakage current	DQ are disabled; $V_{OUT} = V_{CCQ}$	I_{LO_pd}	–	0.3	1	μA	4
	DQ are disabled; $V_{OUT} = 0V$	I_{LO_pu}	–	0.9	5	μA	
Output low current (R/B#)	$V_{OL} = 0.2V$	I_{OL} (R/B#)	3	4	–	mA	3
V_{REFQ} leakage current	$V_{REFQ} = V_{CCQ}/2$ (all other pins not under test = 0V)	I_{VREFQ}	–	–	± 5	μA	

- Notes:
1. All leakage currents are per die (LUN). For example, two die (LUNs) have a maximum leakage current of $\pm 20\mu A$ and four die (LUNs) have a maximum leakage current of $\pm 40\mu A$.
 2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)max}$, $V_{IL(DC)min}$] for single-ended signals as well as the limitations for overshoot and undershoot.
 3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See Feature Address 81h: Programmable R/B# Pull-Down Strength table in Configuration Operations section for additional details.
 4. Absolute leakage value per I/O per NAND die (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

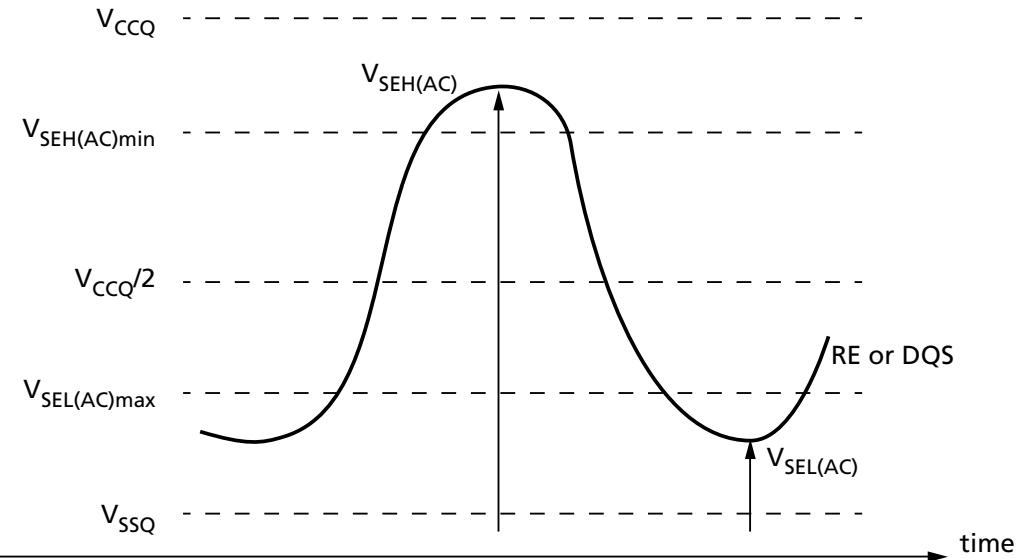


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Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (RE_t, RE_c, DQS_t, or DQS_c) shall comply with requirements for single-ended signals. RE_t and RE_c shall meet $V_{SEH(AC)\min}/V_{SEL(AC)\max}$ in every half-cycle. DQS_t and DQS_c shall meet $V_{SEH(AC)\min}/V_{SEL(AC)\max}$ in every half-cycle preceding and following a valid transition.

Figure 96: Single-Ended requirements for Differential Signals



While control (for example, ALE, CLE) and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to $V_{CCQ}/2$; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL(AC)}$ Max, $V_{SEH(AC)}$ Min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 67: Single-Ended Levels for RE_t, RE_c, DQS_t, DQS_c for NV-DDR2 (1.8V V_{CCQ})

Parameter	Symbol	Min	Max	Unit	Notes
Single-ended high level	$V_{SEH(AC)}$	$V_{CCQ}/2 + 0.250$	See note	V	1
Single-ended low level	$V_{SEL(AC)}$	See note	$V_{CCQ}/2 - 0.250$	V	1

Note: 1. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)\max}$, $V_{IL(DC)\min}$] for single-ended signals as well as the limitations for overshoot and undershoot.

Table 68: Differential AC Input/Output Parameters

Parameter	Symbol	Min	Max	Unit	Notes
AC differential input cross-point voltage relative to $V_{CCQ}/2$: NV-DDR2 interface	$V_{IX(AC)}$	$0.5 \times V_{CCQ} - 0.175$	$0.5 \times V_{CCQ} + 0.175$	V	1



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – DC Characteristics and Operating Conditions (V_{CCQ})

Table 68: Differential AC Input/Output Parameters (Continued)

Parameter	Symbol	Min	Max	Unit	Notes
AC differential output cross-point voltage	$V_{OX(AC)}$	$0.5 \times V_{CCQ} - 0.2$	$0.5 \times V_{CCQ} + 0.2$	V	2, 3, 4

Notes:

1. The typical value of $V_{IX(AC)}$ is expected to be $0.5 \times V_{CCQ}$ of the transmitting device. $V_{IX(AC)}$ is expected to track variations in V_{CCQ} . $V_{IX(AC)}$ indicates the voltage at which differential input signals shall cross.
2. The typical value of $V_{OX(AC)}$ is expected to be $0.5 \times V_{CCQ}$ of the transmitting device. $V_{OX(AC)}$ is expected to track variations in V_{CCQ} . $V_{OX(AC)}$ indicates the voltage at which differential input signals shall cross.
3. $V_{OX(AC)}$ is measured with $\frac{1}{2}$ DQ signals per data byte driving logic HIGH and $\frac{1}{2}$ DQ signals per data byte driving logic LOW.
4. $V_{OX(AC)}$ is verified by design and characterization; it may not be subject to production testing.



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (Asynchronous)

Electrical Specifications – AC Characteristics and Operating Conditions (Asynchronous)

Table 69: AC Characteristics: Asynchronous Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max												
Clock period		100		50		35		30		25		20		ns	
Frequency		≈10		≈20		≈28		≈33		≈40		≈50		MHz	
ALE to data start	^t ADL	150	–	150	–	150	–	150	–	150	–	150	–	ns	1
ALE hold time	^t ALH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
ALE setup time	^t ALS	50	–	25	–	15	–	10	–	10	–	10	–	ns	
ALE to RE# delay	^t AR	25	–	10	–	10	–	10	–	10	–	10	–	ns	
CE# access time	^t CEA	–	100	–	45	–	30	–	25	–	25	–	25	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	^t CEH	20	–	20	–	20	–	20	–	20	–	20	–	ns	
CE# hold time	^t CH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
Delay before CE# HIGH for any volume after a volume is selected	^t CEVDLY	50	–	50	–	50	–	50	–	50	–	50	–	ns	
CE# HIGH to output High-Z	^t CHZ	–	100	–	50	–	50	–	50	–	30	–	30	ns	2
CLE hold time	^t CLH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
CLE to RE# delay	^t CLR	20	–	10	–	10	–	10	–	10	–	10	–	ns	
CLE setup time	^t CLS	50	–	25	–	15	–	10	–	10	–	10	–	ns	
CE# HIGH to output hold	^t COH	0	–	15	–	15	–	15	–	15	–	15	–	ns	
CE# setup time	^t CS	70	–	35	–	25	–	25	–	20	–	15	–	ns	
CE# to RE# LOW or RE_t/RE_c	^t CR	10	–	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW after CE# has been HIGH for >1μs	^t CR2	100	–	100	–	100	–	100	–	100	–	100	–	ns	
	^t CR2 (Read ID)	150	–	150	–	150	–	150	–	150	–	150	–	ns	5
CE# setup time for data input after CE# has been HIGH for >1μs	^t CS3	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Data hold time	^t DH	20	–	10	–	5	–	5	–	5	–	5	–	ns	
Data setup time	^t DS	40	–	20	–	15	–	10	–	10	–	7	–	ns	
ENi LOW until any issued command is ignored	^t ENi	–	15	–	15	–	15	–	15	–	15	–	15	ns	



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (Asynchronous)

Table 69: AC Characteristics: Asynchronous Command, Address, and Data (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max												
CE# LOW until ENo LOW	t_{ENo}	–	50	–	50	–	50	–	50	–	50	–	50	ns	
Output High-Z to RE# LOW	t_{IR}	10	–	0	–	0	–	0	–	0	–	0	–	ns	
RE# cycle time	t_{RC}	100	–	50	–	35	–	30	–	25	–	20	–	ns	
RE# access time	t_{REA}	–	40	–	30	–	25	–	20	–	20	–	16	ns	3
RE# HIGH hold time	t_{REH}	30	–	15	–	15	–	10	–	10	–	7	–	ns	3
RE# HIGH to output hold	t_{RHOH}	0	–	15	–	15	–	15	–	15	–	15	–	ns	3
RE# HIGH to WE# LOW	t_{RHW}	200	–	100	–	100	–	100	–	100	–	100	–	ns	
RE# HIGH to output High-Z	t_{RHZ}	–	200	–	100	–	100	–	100	–	100	–	100	ns	2, 3
RE# LOW to output hold	t_{RLOH}	0	–	0	–	0	–	0	–	5	–	5	–	ns	3
RE# pulse width	t_{RP}	50	–	25	–	17	–	15	–	12	–	10	–	ns	
Ready to RE# LOW	t_{RR}	40	–	20	–	20	–	20	–	20	–	20	–	ns	
WE# HIGH to R/B# LOW	t_{WB}	–	200	–	100	–	100	–	100	–	100	–	100	ns	4
WE# cycle time	t_{WC}	100	–	45	–	35	–	30	–	25	–	20	–	ns	
WE# HIGH hold time	t_{WH}	30	–	15	–	15	–	10	–	10	–	7	–	ns	
WE# HIGH to RE# LOW	t_{WHR}	120	–	80	–	80	–	60	–	60	–	60	–	ns	
WE# pulse width	t_{WP}	50	–	25	–	17	–	15	–	12	–	10	–	ns	
WP# transition to WE# LOW	t_{WW}	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a volume is selected	t_{VDLY}	50	–	50	–	50	–	50	–	50	–	50	–	ns	

- Notes:
- Timing for t_{ADL} begins in the address cycle, on the final rising edge of WE# and ends with the first rising edge of WE# for data input. t_{ADL} SPEC for SET FEATURES operations is 70ns.
 - Data transition is measured $\pm 200\text{mV}$ from steady-steady voltage with load. This parameter is sampled and not 100 percent tested.
 - AC characteristics may need to be relaxed if output drive strength is not set to at least nominal.
 - Any command (including read status commands) cannot be issued during t_{WB} , even if R/B# or RDY is ready.
 - t_{CR2} (MIN) is 150ns for read ID sequence only. For all other command sequences t_{CR2} (MIN) requirement is 100ns.



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 70: AC Characteristics: NV-DDR Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		50		30		20		15		12		10		ns	
Frequency		≈20		≈33		≈50		≈67		≈83		≈100		MHz	
Access window of DQ[7:0] from CLK	^t AC	3	20	3	20	3	20	3	20	3	20	3	20	ns	
ALE to data loading time	^t ADL	150	–	150	–	150	–	150	–	150	–	150	–	ns	6
Command, address data delay	^t CAD	25	–	25	–	25	–	25	–	25	–	25	–	ns	1
DQ hold – command, address	^t CAH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
ALE, CLE, W/R# hold	^t CALH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
ALE, CLE, W/R# setup	^t CALS	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
DQ setup – command, address	^t CAS	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	^t CEH	20	–	20	–	20	–	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any volume after a volume is selected	^t CEVDLY	50	–	50	–	50	–	50	–	50	–	50	–	ns	
CE# hold	^t CH	10	–	5	–	4	–	3	–	2.5	–	2	–	ns	
Average CLK cycle time	^t CK (AVG)	50	100	30	50	20	30	15	20	12	15	10	12	ns	2
Absolute CLK cycle time, from rising edge to rising edge	^t CK (ABS)	$\begin{aligned} t_{CK \text{ (ABS)}} \text{ MIN} &= t_{CK \text{ (AVG)}} + t_{JIT \text{ (per)}} \text{ MIN} \\ t_{CK \text{ (ABS)}} \text{ MAX} &= t_{CK \text{ (AVG)}} + t_{JIT \text{ (per)}} \text{ MAX} \end{aligned}$												ns	
CLK cycle HIGH	^t CKH (ABS)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^t CK	3
CLK cycle LOW	^t CKL (ABS)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^t CK	3



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 70: AC Characteristics: NV-DDR Command, Address, and Data (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Data output end to W/R# HIGH	t_{CKWR}	$t_{CKWR} (\text{MIN}) = \text{RoundUp}[(t_{DQSCK} (\text{MAX}) + t_{CK})/t_{CK}]$												t_{CK}	
CE# setup time for data input and data output after CE# has been HIGH for $>1\mu\text{s}$	t_{CS3}	75	–	75	–	75	–	75	–	75	–	75	–	ns	
CE# setup	t_{CS}	35	–	25	–	15	–	15	–	15	–	15	–	ns	
Data In hold	t_{DH}	5	–	2.5	–	1.7	–	1.3	–	1.1	–	0.9	–	ns	
Access window of DQS from CLK	t_{DQSCK}	–	20	–	20	–	20	–	20	–	20	–	20	ns	
DQS, DQ[7:0] driven by NAND	t_{DQSD}	–	18	–	18	–	18	–	18	–	18	–	18	ns	
DQS, DQ[7:0] to tri-state	t_{DQSHZ}	–	20	–	20	–	20	–	20	–	20	–	20	ns	4
DQS input high pulse width	t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
DQS input low pulse width	t_{DQLS}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
DQS-DQ skew	t_{DQSQ}	–	5	–	2.5	–	1.7	–	1.3	–	1.0	–	0.85	ns	
Data input	t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
Data In setup	t_{DS}	5	–	3	–	2	–	1.5	–	1.1	–	0.9	–	ns	
DQS falling edge from CLK rising – hold	t_{DSH}	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	t_{CK}	
DQS falling to CLK rising – set-up	t_{DSS}	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	t_{CK}	
Data valid window	t_{DVW}	$t_{DVW} = t_{QH} - t_{DQSQ}$												ns	
ENi LOW until any issued command is ignored	t_{ENi}	–	15	–	15	–	15	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	t_{ENO}	–	50	–	50	–	50	–	50	–	50	–	50	ns	
Half clock period	t_{HP}	$t_{HP} = \text{MIN}(t_{CKH}, t_{CKL})$												ns	



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 70: AC Characteristics: NV-DDR Command, Address, and Data (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
The deviation of a given t_{CK} (ABS) from a t_{CK} (AVG)	t_{JIT} (per)	-0.7	0.7	-0.7	0.7	-0.7	0.7	-0.6	0.6	-0.6	0.6	-0.5	0.5	ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	t_{QH}	$t_{QH} = t_{HP} - t_{QHS}$												ns	
Data hold skew factor	t_{QHS}	-	6	-	3	-	2	-	1.5	-	1.2	-	1	ns	
Data output to command, address, or data input	t_{RHW}	100	-	100	-	100	-	100	-	100	-	100	-	ns	
Ready to data output	t_{RR}	20	-	20	-	20	-	20	-	20	-	20	-	ns	
CLK HIGH to R/B# LOW	t_{WB}	-	100	-	100	-	100	-	100	-	100	-	100	ns	7
Command cycle to data output	t_{WHR}	80	-	80	-	80	-	80	-	80	-	80	-	ns	7
DQS write preamble	t_{WPRE}	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	t_{CK}	
DQS write post-preamble	t_{WPST}	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	t_{CK}	
W/R# LOW to data output cycle	t_{WRCK}	20	-	20	-	20	-	20	-	20	-	20	-	ns	
WP# transition to command cycle	t_{WW}	100	-	100	-	100	-	100	-	100	-	100	-	ns	
Delay before next command after a volume is selected	t_{VDLY}	50	-	50	-	50	-	50	-	50	-	50	-	ns	

- Notes:
1. Delay is from start of command to next command, address, or data cycle; start of address to next command, address, or data cycle; and end of data to start of next command, address, or data cycle.
 2. t_{CK} (AVG) is the average clock period over any consecutive 200-cycle window.
 3. t_{CKH} (ABS) and t_{CKL} (ABS) include static offset and duty cycle jitter.
 4. t_{DQSHZ} begins when W/R# is latched HIGH by CLK. This parameter is not referenced to a specific voltage level; it specifies when the device outputs are no longer driving.
 5. If RESET (FFh) is issued when the target is idle, the target goes busy for a maximum of 5 μ s.



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6. t_{ADL} SPEC for SET FEATURES operations is 70ns.
7. Any command (including read status commands) cannot be issued during t_{WB} , even if R/B# or RDY is ready.

Table 71: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0–4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max										
Clock period		30		25		15		12		10		ns	
Frequency		≈33		≈40		≈66		≈83		≈100		MHz	
Command and Address													
Access window of DQ[7:0] from RE# LOW or RE_t/RE_c	t_{AC}	3	25	3	25	3	25	3	25	3	25	ns	
ALE to data loading time	t_{ADL}	150	–	150	–	150	–	150	–	150	–	ns	13
ALE to RE# LOW or RE_t/RE_c	t_{AR}	10	–	10	–	10	–	10	–	10	–	ns	
DQ hold – command, address	t_{CAH}	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE hold	t_{CALH}	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE setup	t_{CALS}	15	–	15	–	15	–	15	–	15	–	ns	
DQ setup – command, address	t_{CAS}	5	–	5	–	5	–	5	–	5	–	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	t_{CEH}	20	–	20	–	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any volume after a volume is selected	t_{CEVDLY}	50	–	50	–	50	–	50	–	50	–	ns	
CE# hold	t_{CH}	5	–	5	–	5	–	5	–	5	–	ns	
CE# HIGH to output High-Z	t_{CHZ}	–	30	–	30	–	30	–	30	–	30	ns	1
CLE HIGH to output High-Z	t_{CLHZ}	–	30	–	30	–	30	–	30	–	30	ns	1
CLE to RE# LOW or RE_t/RE_c	t_{CLR}	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c	t_{CR}	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c if CE# has been HIGH for >1μs	t_{CR2}	100	–	100	–	100	–	100	–	100	–	ns	
	t_{CR2} (Read ID)	150	–	150	–	150	–	150	–	150	–	ns	14



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 71: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0–4 (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CE# setup	t_{CS}	20	–	20	–	20	–	20	–	20	–	ns	
CE# setup for data output	t_{CS1}	30	–	30	–	30	–	30	–	30	–	ns	
CE# setup time to DQS (DQS_t) low after CE# has been HIGH for >1μs	t_{CD}	100	–	100	–	100	–	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	t_{CSD}	10	–	10	–	10	–	10	–	10	–	ns	
ENi LOW until any issued command is ignored	t_{ENi}	–	15	–	15	–	15	–	15	–	15	ns	
CE_# LOW until ENo LOW	t_{ENo}	–	50	–	50	–	50	–	50	–	50	ns	
Ready to data output	t_{RR}	20	–	20	–	20	–	20	–	20	–	ns	
WE# HIGH to R/B# LOW	t_{WB}	–	100	–	100	–	100	–	100	–	100	ns	15
WE# cycle time	t_{WC}	25	–	25	–	25	–	25	–	25	–	ns	
WE# pulse width	t_{WH}	11	–	11	–	11	–	11	–	11	–	ns	
Command cycle to data output	t_{WHR}	80	–	80	–	80	–	80	–	80	–	ns	
WE# pulse width	t_{WP}	11	–	11	–	11	–	11	–	11	–	ns	
WP# transition to command cycle	t_{WW}	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a volume is selected	t_{VDLY}	50	–	50	–	50	–	50	–	50	–	ns	
Jitter													
The deviation of a given t_{DQS} (ABS)/ t_{DSC} (ABS) from a t_{DQS} (AVG)/ t_{DSC} (AVG)	t_{JITper} (DQS)	–2.4	2.4	–2.0	2.0	–1.2	1.2	–1.0	1.0	–0.8	0.8	ns	3, 5, 7
The deviation of a given t_{RC} (ABS)/ t_{DSC} (ABS) from a t_{RC} (AVG)/ t_{DSC} (AVG)	t_{JITper} (RE#)	–1.8	1.8	–1.5	1.5	–0.9	0.9	–0.75	0.75	–0.6	0.6	ns	3, 5, 7



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 71: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0–4 (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Cycle to cycle jitter for DQS	t_{JITcc} (DQS)	-	4.8	-	4.0	-	2.4	-	2.0	-	1.6	ns	3, 6
Cycle to cycle jitter for RE#	t_{JITcc} (RE#)	-	3.6	-	3.0	-	1.8	-	1.5	-	1.2	ns	3, 6
Data Input													
DQS setup time for data input start	t_{CDQSS}	30	-	30	-	30	-	30	-	30	-	ns	
DQS hold time for data input burst end	t_{CDQSH}	100	-	100	-	100	-	100	-	100	-	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH set-up to ALE, CLE and CE# LOW during data burst	t_{DBS}	5	-	5	-	5	-	5	-	5	-	ns	
Data In hold	t_{DH}	4.0	-	3.3	-	2.0	-	1.1	-	0.7	-	ns	10
Data In setup	t_{DS}	4.0	-	3.3	-	2.0	-	1.1	-	0.7	-	ns	10
DQ input pulse width	t_{DIPW}	0.31	-	0.31	-	0.31	-	0.31	-	0.31	-	$t_{DSC(AVG)}$	12
DQS input high pulse width	t_{DQSH}	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	$t_{DSC(AVG)}$	
DQS input low pulse width	t_{DQLS}	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	$t_{DSC(AVG)}$	
Average DQS cycle time	$t_{DSC(AVG)}$ or t_{DSC}	30	-	25	-	15	-	12	-	10	-	ns	2
Absolute DQS cycle time, from rising edge to rising edge	$t_{DSC(ABS)}$	$t_{DSC(ABS)} \text{ MIN} = t_{DSC(AVG)} + t_{JITper(DQS)} \text{ MIN}$ $t_{DSC(ABS)} \text{ MAX} = t_{DSC(AVG)} + t_{JITper(DQS)} \text{ MAX}$										ns	
ENi LOW until any issued command is ignored	t_{ENi}	-	15	-	15	-	15	-	15	-	15	ns	
CE# LOW until ENo LOW	t_{ENO}	-	50	-	50	-	50	-	50	-	50	ns	
DQS write preamble	t_{WPRE}	15	-	15	-	15	-	15	-	15	-	ns	
DQS write post-preamble	t_{WPST}	6.5	-	6.5	-	6.5	-	6.5	-	6.5	-	ns	
DQS write post-preamble hold time	t_{WPSTH}	15	-	15	-	15	-	15	-	15	-	ns	



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 71: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0–4 (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Data Output													
Access window of DQ[7:0] from CLK	t_{AC}	3	25	3	25	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH set-up to ALE, CLE and CE# LOW during data burst	t_{DBS}	5	–	5	–	5	–	5	–	5	–	ns	
DQS-DQ skew	t_{DQSQ}	–	2.5	–	2.0	–	1.4	–	1.0	–	0.8	ns	
Access window of DQS from RE# or RE_t/RE_c	t_{DQSRE}	3	25	3	25	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	t_{DQSD}	6	18	6	18	6	18	6	18	6	18	ns	
Data valid window	t_{DVW}	$t_{DVW} = t_{QH} - t_{DQSQ}$										ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	t_{QH}	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	t_{RC} (AVG)	9, 11
DQS (DQS_t/ DQS_c) output HIGH time	t_{QSH}	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	t_{RC} (AVG)	9, 11
DQS (DQS_t/ DQS_c) output LOW time	t_{QSL}	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	t_{RC} (AVG)	9, 11
Average RE# cycle time	t_{RC} (AVG) or t_{RC}	30	–	25	–	15	–	12	–	10	–	ns	2
Absolute RE# cycle time	t_{RC} (ABS)	t_{RC} (ABS) MIN = t_{RC} (AVG) + $t_{JITper(Re)}$ MIN t_{RC} (ABS) MAX = t_{RC} (AVG) + $t_{JITper(Re)}$ MAX										ns	
Average RE# HIGH hold time	t_{REH} (AVG)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{RC} (AVG)	4
Absolute RE# HIGH hold time	t_{REH} (ABS)	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	t_{RC} (AVG)	
Data output to command, address, or data input	t_{RHW}	100	–	100	–	100	–	100	–	100	–	ns	
Average RE# pulse width	t_{RP} (AVG)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{RC} (AVG)	4



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 71: AC Characteristics: NV-DDR2 Command, Address, and Data for modes 0–4 (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Absolute RE# pulse width	^t RP (ABS)	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	^t RC (AVG)	
Read preamble	^t RPRE	15	–	15	–	15	–	15	–	15	–	ns	
Read postamble	^t RPST	^t RPST (MIN) = ^t DQSRE + 0.5 × ^t RC ^t RPST (MAX): –										ns	
Read postamble hold time	^t RPSTH	15	–	15	–	15	–	15	–	15	–	ns	

- Notes:
1. ^tCHZ and ^tCLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.
 2. The parameters ^tRC (AVG) and ^tDSC (AVG) are the average over any 200 consecutive periods and ^tRC (AVG)/^tDSC (AVG) MIN are the smallest rates allowed, with the exception of a deviation due to ^tJIT (per).
 3. Input jitter is allowed provided it does not exceed values specified.
 4. ^tREH (AVG) and ^tRP (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
 5. The period jitter ^tJIT (per) is the maximum deviation in the ^tRC or ^tDSC period from the average or nominal ^tRC or ^tDSC period. It is allowed in either the positive or negative direction.
 6. The cycle-to-cycle jitter ^tJITcc is the amount the clock period can deviate from one cycle to the next.
 7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed ^tJITper. As long as the absolute minimum half period ^tRP (ABS), ^tREH (ABS), ^tDQSH, or ^tDQL is not less than 43 percent of the average cycle.
 8. All timing parameter values assume differential signaling for RE# and DQS is used.
 9. When the device is operated with input clock jitter, ^tQSL, ^tQSH, and ^tQH need to be derated by the actual ^tJITper in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
 10. The ^tDS and ^tDH times listed are based on an input slew rate greater than or equal to 1 V/ns for single-ended signal, and based on an input slew rate greater than or equal to 2 V/ns for differential signal. If the input slew rate is less than 1 V/ns for single-ended signal, or less than 2 V/ns for differential signal, then the derating methodology shall be used.
 11. When the device is operated with input RE (RE_t/RE_c) jitter, ^tQSL, ^tQSH, and ^tQH need to be derated by the actual input duty cycle jitter beyond $0.45 \times ^tRC (AVG)$ but not exceeding $0.43 \times ^tRC (AVG)$. Output deratings are relative to the device input RE pulse that generated the DQS pulse.
 12. The parameter ^tDIPW is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
 13. ^tADL SPEC for SET FEATURES operations is 70ns.
 14. ^tCR2 (MIN) is 150ns for read ID sequence only. For all other command sequences ^tCR2 (MIN) requirement is 100ns.
 15. Any command (including read status commands) cannot be issued during ^tWB, even if R/B# or RDY is ready.



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 72: AC Characteristics: NV-DDR2Command, Address, and Data for Timing Modes 5–7

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock period		7.5		6		5		ns	
Frequency		≈133		≈166		≈200		MHz	
Command and Address									
Access window of DQ[7:0] from RE# LOW or RE_t/RE_c	^t AC	3	25	3	25	3	25	ns	
ALE to data loading time	^t ADL	150	–	150	–	150	–	ns	13
ALE to RE# LOW or RE_t/RE_c	^t AR	10	–	10	–	10	–	ns	
DQ hold – command, address	^t CAH	5	–	5	–	5	–	ns	
ALE, CLE hold	^t CALH	5	–	5	–	5	–	ns	
ALE, CLE setup	^t CALS	15	–	15	–	15	–	ns	
DQ setup – command, address	^t CAS	5	–	5	–	5	–	ns	
CE# HIGH hold time	^t CEH	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any volume after a volume is selected	^t CEVDLY	50	–	50	–	50	–	ns	
CE# hold	^t CH	5	–	5	–	5	–	ns	
CE# HIGH to output High-Z	^t CHZ	–	30	–	30	–	30	ns	1
CLE HIGH to output High-Z	^t CLHZ	–	30	–	30	–	30	ns	1
CLE to RE# LOW or RE_t/RE_c	^t CLR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c	^t CR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c if CE# has been HIGH for >1μs	^t CR2	100	–	100	–	100	–	ns	
CE# setup	^t CR2 (Read ID)	150	–	150	–	150	–	ns	14
CE# setup	^t CS	20	–	20	–	20	–	ns	
CE# setup for data output	^t CS1	30	–	30	–	30	–	ns	
CE# setup time to DQS (DQS_t) low after CE# has been HIGH for >1μs	^t CD	100	–	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	^t CSD	10	–	10	–	10	–	ns	



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 72: AC Characteristics: NV-DDR2Command, Address, and Data for Timing Modes 5–7 (Continued)

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
EN# LOW until any issued command is ignored	t_{ENi}	–	15	–	15	–	15	ns	
CE# LOW until EN# LOW	t_{ENO}	–	50	–	50	–	50	ns	
Ready to data output	t_{RR}	20	–	20	–	20	–	ns	
WE# HIGH to R/B# LOW	t_{WB}	–	100	–	100	–	100	ns	15
WE# cycle time	t_{WC}	25	–	25	–	25	–	ns	
WE# pulse width	t_{WH}	11	–	11	–	11	–	ns	
Command cycle to data output	t_{WHR}	80	–	80	–	80	–	ns	
WE# pulse width	t_{WP}	11	–	11	–	11	–	ns	
WP# transition to command cycle	t_{WW}	100	–	100	–	100	–	ns	
Delay before next command after a volume is selected	t_{VDLY}	50	–	50	–	50	–	ns	
Jitter									
The deviation of a given t_{DQS} (ABS)/ t_{DSC} (ABS) from a t_{DQS} (AVG)/ t_{DSC} (AVG)	t_{JITper} (DQS)	–0.6	0.6	–0.48	0.48	–0.40	0.40	ns	3, 5, 7
The deviation of a given t_{RC} (ABS)/ t_{DSC} (ABS) from a t_{RC} (AVG)/ t_{DSC} (AVG)	t_{JITper} (RE#)	–0.45	0.45	–0.36	0.36	–0.30	0.30	ns	3, 5, 7
Cycle to cycle jitter for DQS	t_{JITcc} (DQS)	1.2	–	0.96	–	0.80	–	ns	3, 6
Cycle to cycle jitter for RE#	t_{JITcc} (RE#)	0.9	–	0.72	–	0.60	–	ns	3, 6
Data Input									
DQS setup time for data input start	t_{CDQSS}	30	–	30	–	30	–	ns	
DQS hold time for data input burst end	t_{CDQSH}	100	–	100	–	100	–	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	t_{DBS}	5	–	5	–	5	–	ns	
Data In hold	t_{DH}	0.6	–	0.55	–	0.40	–	ns	10



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 72: AC Characteristics: NV-DDR2Command, Address, and Data for Timing Modes 5–7 (Continued)

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data In setup	t_{DS}	0.6	–	0.55	–	0.40	–	ns	10
DQ input pulse width	t_{DIPW}	0.31	–	0.31	–	0.31	–	$t_{DSC(AV)}$ G)	12
DQS input high pulse width	t_{DQSH}	0.43	–	0.43	–	0.43	–	t_{DSC} (AVG)	
DQS input low pulse width	t_{DQLS}	0.43	–	0.43	–	0.43	–	t_{DSC} (AVG)	
Average DQS cycle time	t_{DSC} (AVG) or t_{DSC}	7.5	–	6	–	5	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	t_{DSC} (ABS)	t_{DSC} (ABS) MIN = t_{DSC} (AVG) + $t_{JITper(DQS)}$ MIN t_{DSC} (ABS) MAX = t_{DSC} (AVG) + $t_{JITper(DQS)}$ MAX							
ENi LOW until any issued command is ignored	t_{ENi}	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	t_{ENO}	–	50	–	50	–	50	ns	
DQS write preamble	t_{WPRE}	15	–	15	–	15	–	ns	
DQS write postamble	t_{WPST}	6.5	–	6.5	–	6.5	–	ns	
DQS write postamble hold time	t_{WPSTH}	15	–	15	–	15	–	ns	
Data Output									
Access window of DQ[7:0] from CLK	t_{AC}	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	t_{DBS}	5	–	5	–	5	–	ns	
DQS-DQ skew	t_{DQSQ}	–	0.6	–	0.5	–	0.4	ns	
Access window of DQS from RE# or RE_t/RE_c	t_{DQSRE}	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	t_{DQSD}	6	18	6	18	6	18	ns	
Data valid window	t_{DVW}	$t_{DVW} = t_{QH} - t_{DQSQ}$						ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	t_{QH}	0.37	–	0.37	–	0.37	–	t_{RC} (AVG)	9, 11
DQS (DQS_t/DQS_c) output HIGH time	t_{QSH}	0.37	–	0.37	–	0.37	–	t_{RC} (AVG)	9, 11



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 72: AC Characteristics: NV-DDR2Command, Address, and Data for Timing Modes 5–7 (Continued)

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
DQS (DQS_t/DQS_c) output LOW time	t_{QSL}	0.37	–	0.37	–	0.37	–	t_{RC} (AVG)	9, 11
Average RE# cycle time	t_{RC} (AVG) or t_{RC}	7.5	–	6	–	5	–	ns	2
Absolute RE# cycle time	t_{RC} (ABS)	t_{RC} (ABS) MIN = t_{RC} (AVG) + $t_{JITper(Re\#)}$ MIN t_{RC} (ABS) MAX = t_{RC} (AVG) + $t_{JITper(Re\#)}$ MAX						ns	
Average RE# HIGH hold time	t_{REH} (AVG)	0.45	0.55	0.45	0.55	0.45	0.55	t_{RC} (AVG)	4
Absolute RE# HIGH hold time	t_{REH} (ABS)	0.43	–	0.43	–	0.43	–	t_{RC} (AVG)	
Data output to command, address, or data input	t_{RHW}	100	–	100	–	100	–	ns	
Average RE# pulse width	t_{RP} (AVG)	0.45	0.55	0.45	0.55	0.45	0.55	t_{RC} (AVG)	4
Absolute RE# pulse width	t_{RP} (ABS)	0.43	–	0.43	–	0.43	–	t_{RC} (AVG)	
Read preamble	t_{RPRE}	15	–	15	–	15	–	ns	
Read postamble	t_{RPST}	t_{RPST} (MIN) = t_{DQSRE} + 0.5 × t_{RC} t_{RPST} (MAX): –						ns	
Read postamble hold time	t_{RPSTH}	15	–	15	–	15	–	ns	

- Notes:
1. t_{CHZ} and t_{CLHZ} are not referenced to a specific voltage level, but specify when the device output is no longer driving.
 2. The parameters t_{RC} (AVG) and t_{DSC} (AVG) are the average over any 200 consecutive periods and t_{RC} (AVG)/ t_{DSC} (AVG) MIN are the smallest rates allowed, with the exception of a deviation due to t_{JIT} (per).
 3. Input jitter is allowed provided it does not exceed values specified.
 4. t_{REH} (AVG) and t_{RP} (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
 5. The period jitter t_{JIT} (per) is the maximum deviation in the t_{RC} or t_{DSC} period from the average or nominal t_{RC} or t_{DSC} period. It is allowed in either the positive or negative direction.
 6. The cycle-to-cycle jitter t_{JITcc} is the amount the clock period can deviate from one cycle to the next.
 7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed t_{JITper} . As long as the absolute minimum half period t_{RP} (ABS), t_{REH} (ABS), t_{DQSH} , or t_{DQL} is not less than 43 percent of the average cycle.
 8. All timing parameter values assume differential signaling for RE# and DQS is used.
 9. When the device is operated with input clock jitter, t_{QSL} , t_{QSH} , and t_{QH} need to be derated by the actual t_{JITper} in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).



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10. The t_{DS} and t_{DH} times listed are based on an input slew rate greater than or equal to 1 V/ns for single-ended signal, and based on an input slew rate greater than or equal to 2 V/ns for differential signal. If the input slew rate is less than 1 V/ns for single-ended signal, or less than 2 V/ns for differential signal, then the derating methodology shall be used.
11. When the device is operated with input RE (RE_t/RE_c) jitter, t_{QSL} , t_{QSH} , and t_{QH} need to be derated by the actual input duty cycle jitter beyond $0.45 \times t_{RC}(\text{AVG})$ but not exceeding $0.43 \times t_{RC}(\text{AVG})$. Output deratings are relative to the device input RE pulse that generated the DQS pulse.
12. The parameter t_{DIPW} is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(\text{DC})}$ and the consecutive crossing of $V_{REFQ(\text{DC})}$.
13. t_{ADL} SPEC for SET FEATURES operations is 70ns.
14. $t_{CR2}(\text{MIN})$ is 150ns for Read ID sequence only. For all other command sequences $t_{CR2}(\text{MIN})$ requirement is 100ns.
15. Any command (including read status commands) cannot be issued during t_{WB} , even if R/B# or RDY is ready.

Table 73: AC Characteristics: NV-DDR2 Command, Address, and Data for Timing Modes 8–9

Parameter	Symbol	Mode 8		Mode 9		Unit	Notes
		Min	Max	Min	Max		
Clock period		3.75		3		ns	
Frequency		≈ 266		≈ 333		MHz	
Command and Address							
Access window of DQ[7:0] from RE# LOW or RE_t/RE_c	t_{AC}	3	25	3	25	ns	
ALE to data loading time	t_{ADL}	150	–	150	–	ns	1
ALE to RE# LOW or RE_t/RE_c	t_{AR}	10	–	10	–	ns	
DQ hold – command, address	t_{CAH}	5	–	5	–	ns	
ALE, CLE hold	t_{CALH}	5	–	5	–	ns	
ALE, CLE setup	t_{CALS}	15	–	15	–	ns	
DQ setup – command, address	t_{CAS}	5	–	5	–	ns	
CE# HIGH hold time	t_{CEH}	20	–	20	–	ns	
Delay before CE# HIGH for any volume after a volume is selected	t_{CEVDLY}	50	–	50	–	ns	
CE# hold	t_{CH}	5	–	5	–	ns	
CE# HIGH to output High-Z	t_{CHZ}	–	30	–	30	ns	2
CLE HIGH to output High-Z	t_{CLHZ}	–	30	–	30	ns	2
CLE to RE# LOW or RE_t/RE_c	t_{CLR}	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c	t_{CR}	10	–	10	–	ns	



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 73: AC Characteristics: NV-DDR2 Command, Address, and Data for Timing Modes 8–9 (Continued)

Parameter	Symbol	Mode 8		Mode 9		Unit	Notes
		Min	Max	Min	Max		
CE# to RE# LOW or RE_t/ RE_c if CE# has been HIGH for >1μs	tCR2	100	–	100	–	ns	
	tCR2 (Read ID)	150	–	150	–	ns	15
CE# setup	tCS	20	–	20	–	ns	
CE# setup for data output	tCS1	30	–	30	–	ns	
CE# setup time to DQS (DQS_t) low after CE# has been HIGH for >1μs	tCD	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	tCSD	10	–	10	–	ns	
ENi LOW until any issued command is ignored	tENi	–	15	–	15	ns	
CE_# LOW until ENo LOW	tENO	–	50	–	50	ns	
Ready to data output	tRR	20	–	20	–	ns	
WE# HIGH to R/B# LOW	tWB	–	100	–	100	ns	17
WE# cycle time	tWC	25	–	25	–	ns	
WE# pulse width	tWH	11	–	11	–	ns	
Command cycle to data output	tWHR	80	–	80	–	ns	
WE# pulse width	tWP	11	–	11	–	ns	
WP# transition to command cycle	tWW	100	–	100	–	ns	
Delay before next com- mand after a volume is se- lected	tVDLY	50	–	50	–	ns	
Jitter							
The deviation of a given tDQS (ABS)/tDSC (ABS) from a tDQS (AVG)/tDSC (AVG)	tJITper (DQS)	–0.30	0.30	–0.24	0.24	ns	4, 6, 8
The deviation of a given tRC (ABS)/tDSC (ABS) from a tRC (AVG)/tDSC (AVG)	tJITper (RE#)	–0.225	0.225	–0.18	0.18	ns	4, 6, 8
Cycle to cycle jitter for DQS	tJITcc (DQS)	0.6	–	0.48	–	ns	4, 7
Cycle to cycle jitter for RE#	tJITcc (RE#)	0.45	–	0.36	–	ns	4, 7
Data Input							
DQS setup time for data in- put start	tCDQSS	30	–	30	–	ns	
DQS hold time for data in- put burst end	tCDQSH	100	–	100	–	ns	



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 73: AC Characteristics: NV-DDR2 Command, Address, and Data for Timing Modes 8–9 (Continued)

Parameter	Symbol	Mode 8		Mode 9		Unit	Notes
		Min	Max	Min	Max		
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	tDBS	5	–	5	–	ns	
Data In hold	tDH	0.30	–	0.24	–	ns	11
Data In setup	tDS	0.30	–	0.24	–	ns	11
DQ input pulse width	tDIPW	0.31	–	0.31	–	tDSC(AVG)	13
DQS input high pulse width	tDQSH	0.43	–	0.43	–	tDSC (AVG)	
DQS input low pulse width	tDQL	0.43	–	0.43	–	tDSC (AVG)	
Average DQS cycle time	tDSC (AVG) or tDSC	3.75	–	3	–	ns	3
Absolute DQS cycle time, from rising edge to rising edge	tDSC (ABS)	tDSC (ABS) MIN = tDSC (AVG) + tJITper(DQS) MIN		tDSC (ABS) MAX = tDSC (AVG) + tJITper(DQS) MAX		ns	
ENi LOW until any issued command is ignored	tENi	–	15	–	15	ns	
CE# LOW until ENo LOW	tENO	–	50	–	50	ns	
DQS write preamble	tWPRE	15	–	15	–	ns	
DQS write postamble	tWPST	6.5	–	6.5	–	ns	
DQS write postamble hold time	tWPSTH	15	–	15	–	ns	
Data Output							
Access window of DQ[7:0] from CLK	tAC	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	tDBS	5	–	5	–	ns	
DQS-DQ skew	tDQSQ	–	0.350	–	0.30	ns	
Access window of DQS from RE# or RE_t/RE_c	tDQSRE	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	tDQSD	6	18	6	18	ns	
Data valid window	tDVW	tDVW = tQH - tDQSQ				ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	tQH	0.37	–	0.37	–	tRC (AVG)	10, 12
DQS (DQS_t/DQS_c) output HIGH time	tQSH	0.37	–	0.37	–	tRC (AVG)	10, 12



MLC 128Gb to 512Gb Async/Sync NAND Electrical Specifications – AC Characteristics and Operating Conditions (NV-DDR, NV-DDR2)

Table 73: AC Characteristics: NV-DDR2 Command, Address, and Data for Timing Modes 8–9 (Continued)

Parameter	Symbol	Mode 8		Mode 9		Unit	Notes
		Min	Max	Min	Max		
DQS (DQS_t/DQS_c) output LOW time	tQSL	0.37	–	0.37	–	tRC (AVG)	10, 12
Average RE# cycle time	tRC (AVG) or tRC	3.75	–	3	–	ns	3
Absolute RE# cycle time	tRC (ABS)	tRC (ABS) MIN = tRC (AVG) + tJITper(RE#) MIN tRC (ABS) MAX = tRC (AVG) + tJITper(RE#) MAX				ns	
Average RE# HIGH hold time	tREH (AVG)	0.45	0.55	0.45	0.55	tRC (AVG)	5
Absolute RE# HIGH hold time	tREH (ABS)	0.43	–	0.43	–	tRC (AVG)	
Data output to command, address, or data input	tRHW	100	–	100	–	ns	
Average RE# pulse width	tRP (AVG)	0.45	0.55	0.45	0.55	tRC (AVG)	5
Absolute RE# pulse width	tRP (ABS)	0.43	–	0.43	–	tRC (AVG)	
Read preamble	tRPRE	15	–	15	–	ns	
Read postamble	tRPST	tDQSRE + 0.5 × tRC	–	tDQSRE + 0.5 × tRC	–	ns	
Read postamble hold time	tRPSTH	15	–	15	–	ns	

- Notes:
1. t_{ADL} for SET FEATURES operations is 100ns.
 2. t_{CHZ} and t_{CLHZ} are not referenced to a specific voltage level, but specify when the device output is no longer driving.
 3. The parameters t_{RC} (AVG) and t_{DSC} (AVG) are the average over any 200 consecutive periods and t_{RC} (AVG)/ t_{DSC} (AVG) MIN are the smallest rates allowed, with the exception of a deviation due to t_{JIT} (per).
 4. Input jitter is allowed provided it does not exceed values specified.
 5. t_{REH} (AVG) and t_{RP} (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
 6. The period jitter t_{JIT} (per) is the maximum deviation in the t_{RC} or t_{DSC} period from the average or nominal t_{RC} or t_{DSC} period. It is allowed in either the positive or negative direction.
 7. The cycle-to-cycle jitter t_{JITcc} is the amount the clock period can deviate from one cycle to the next.
 8. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed t_{JITper} . As long as the absolute minimum half period t_{RP} (ABS), t_{REH} (ABS), t_{DQSH} , or t_{DQSL} is not less than 43 percent of the average cycle.
 9. All timing parameter values assume differential signaling for RE# and DQS is used.
 10. When the device is operated with input clock jitter, t_{QSL} , t_{QSH} , and t_{QH} need to be derated by the actual t_{JITper} in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
 11. The t_{DS} and t_{DH} times listed are based on an input slew rate greater than or equal to 1 V/ns for single-ended signal, and based on an input slew rate greater than or equal to 2 V/ns for differential signal. If the input slew rate is less than 1 V/ns for single-ended sig-



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nal, or less than 2 V/ns for differential signal, then the derating methodology shall be used.

12. When the device is operated with input RE (RE_t/RE_c) jitter, t_{QSL} , t_{QSH} , and t_{QH} need to be derated by the actual input duty cycle jitter beyond $0.45 \times t_{RC}(\text{AVG})$ but not exceeding $0.43 \times t_{RC}(\text{AVG})$. Output deratings are relative to the device input RE pulse that generated the DQS pulse.
13. The parameter t_{DIPW} is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(\text{DC})}$ and the consecutive crossing of $V_{REFQ(\text{DC})}$.
14. t_{ADL} SPEC for SET FEATURES operations is 70ns.
15. $t_{CR2}(\text{MIN})$ is 150ns for Read ID sequence only. For all other command sequences $t_{CR2}(\text{MIN})$ requirement is 100ns.
16. Parameters t_{DQSQ} and t_{QH} are used to calculate overall t_{DVW} ($t_{DVW} = t_{QH} - t_{DQSQ}$). Since data eye training to optimize strobe placement is expected at high I/O speeds (≥ 533 MT/s), t_{DQSQ} and t_{QH} may borrow time from each other without changing t_{DVW} . For example, if there exists X ps of margin on t_{DQSQ} , then t_{QH} can be provided with an additional X ps without changing the value of t_{DVW} . When timing margin is borrowed from t_{DQSQ} to provide additional timing for t_{QH} , the same amount of timing margin can be used for additional timing for t_{QSL} or t_{QSH} .
17. Any command (including read status commands) cannot be issued during t_{WB} , even if R/B# or RDY is ready.



Electrical Specifications – Array Characteristics

Table 74: MLC Array Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	–	1	Cycles	1
ERASE BLOCK operation time	t_{BERS}	10	30	ms	7
Change column setup time to data in/out or next command	t_{CCS}	–	400	ns	
Dummy busy time	t_{DBSY}	0.5	1	μs	
ERASE SUSPEND operation time	t_{ESPD}	–	300	μs	
Busy time when ERASE SUSPEND is issued when LUN is already in the suspend state or ERASE RESUME is issued when no erase is suspended or ongoing	t_{ESPDN}	–	18	μs	
Busy time for SET FEATURES and GET FEATURES operations	t_{FEAT}	–	1	μs	
Busy time for interface change	t_{ITC}	–	1	μs	2
LAST PAGE PROGRAM operation time	t_{LPROG}	–	–	μs	3
Busy time for OTP DATA PROGRAM operation if OTP is protected	t_{OBSY}	–	100	μs	
Power-on reset time	t_{POR}	–	3	ms	
PROGRAM PAGE operation time (single-pass programming - per page)	t_{PROG_eff}	750	1500	μs	
PROGRAM PAGE operation time (Single-pass programming_avg)	t_{PROG}	1500	3000	μs	6
Page buffer transfer busy time	t_{PBSY}	12	34	μs	8
PROGRAM SUSPEND operation time	t_{PSPD}	–	150	μs	
Busy time when PROGRAM SUSPEND is issued when LUN is already in suspend state or PROGRAM RESUME is issued when no program is suspended or ongoing	t_{PSPDN}	–	18	μs	
Internal randomization time	t_{RAND}	35	50	μs	8
MULTI PLANE READ PAGE operation time	t_R	75	80	μs	5, 8
SINGLE PLANE READ PAGE operation time	t_{R_SP}	71	78	μs	5, 8
Cache read busy time	t_{RCBSY}	26	75	μs	5, 8
MULTI-PLANE EXPRESS READ operation time	t_{RER}	59	71	μs	8
SINGLE PLANE EXPRESS READ operation time	t_{RER_SP}	57	69	μs	8
SNAP READ operation time	t_{RSNAP}	45	55	μs	8
Device reset time (read/program/erase)	t_{RST}	–	15/30/500	μs	4
Busy time for GET FEATURES operation for temperature sensor readout	t_{TEMP}	–	120	μs	

- Notes:
1. The pages in the OTP Block have an NOP of 2.
 2. t_{ITC} (MAX) is the busy time when the interface changes from Asynchronous to NV-DDR/NV-DDR2 using the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command or NV-DDR/NV-DDR2 to asynchronous using the RESET (FFh) command. During the t_{ITC} time, any command, including READ STATUS (70h) and READ STATUS ENHANCED (78h), is prohibited.



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3. $t_{LPROG} = t_{PROG}$ (last page) + t_{PROG} (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page).
4. If RESET command is issued when the target is READY, the target goes busy for a maximum of 5 μ s.
5. For read retry options 8 to 15, t_R and t_{RCBSY} (MAX) may be up to 180 μ s.
6. In the case of a PROGRAM operation that exceeds t_{PROG} (MAX), that specific NAND block may be retired by the host system.
7. In the case of an ERASE operation that exceeds t_{BERS} (MAX), that specific NAND block may be retired by the host system.
8. With randomizer enabled, the total time for a given parameter will be the value of that parameter + t_{RAND} .

Any parameters not referenced in the Table 75 (page 196) should be referenced in the Table 74 (page 195)

Table 75: SLC Array Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	–	2	Cycles	
ERASE BLOCK operation time	t_{BERS}	10	30	ms	4
LAST PAGE PROGRAM operation time	t_{LPROG}	–	–	μ s	1
PROGRAM PAGE operation time	t_{PROG}	360	600	μ s	3
MULTI PLANE READ PAGE operation time	t_R	52	60	μ s	2
SINGLE PLANE READ PAGE operation time	t_{R_SP}	51	60	μ s	2
Cache read busy time	t_{RCBSY}	14	60	μ s	2
MULTI-PLANE EXPRESS READ operation time	t_{RER}	–	60	μ s	
SINGLE PLANE EXPRESS READ operation time	t_{RER_SP}	–	60	μ s	
SNAP READ operation time	t_{RSNAP}	34	38	μ s	

- Notes:
1. $t_{LPROG} = t_{PROG}$ (last page) + t_{PROG} (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page).
 2. For read retry options 8 to 15, t_R and t_{RCBSY} (MAX) may be up to 180 μ s.
 3. In the case of a PROGRAM operation that exceeds t_{PROG} (MAX), that specific NAND block may be retired by the host system.
 4. In the case of a ERASE operation that exceeds t_{BERS} (MAX), that specific NAND block may be retired by the host system.



Asynchronous Interface Timing Diagrams

Figure 97: RESET Operation

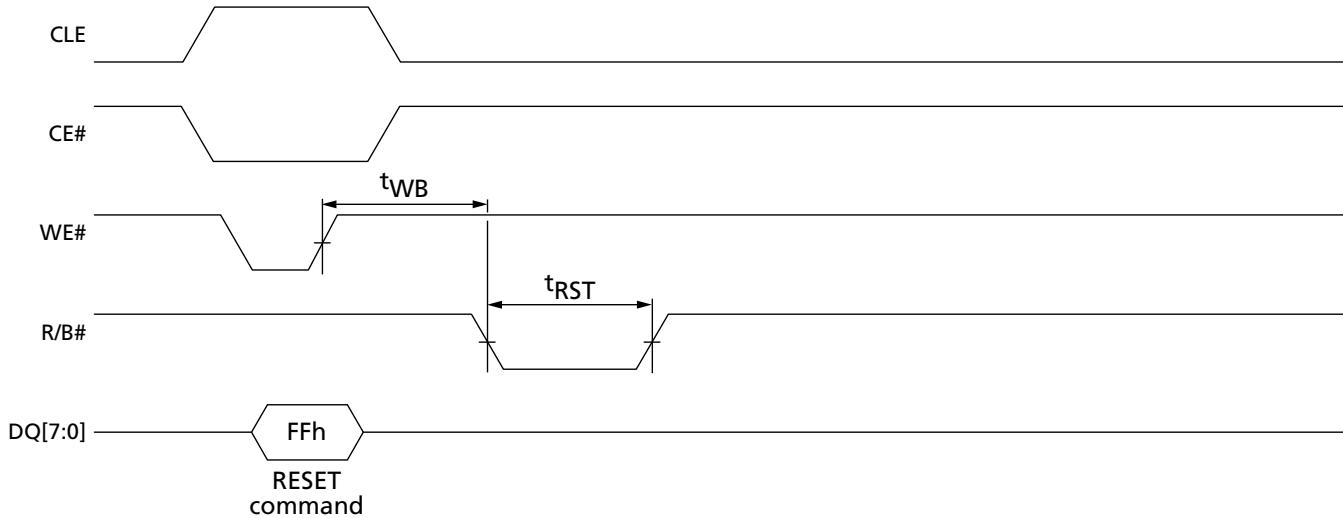
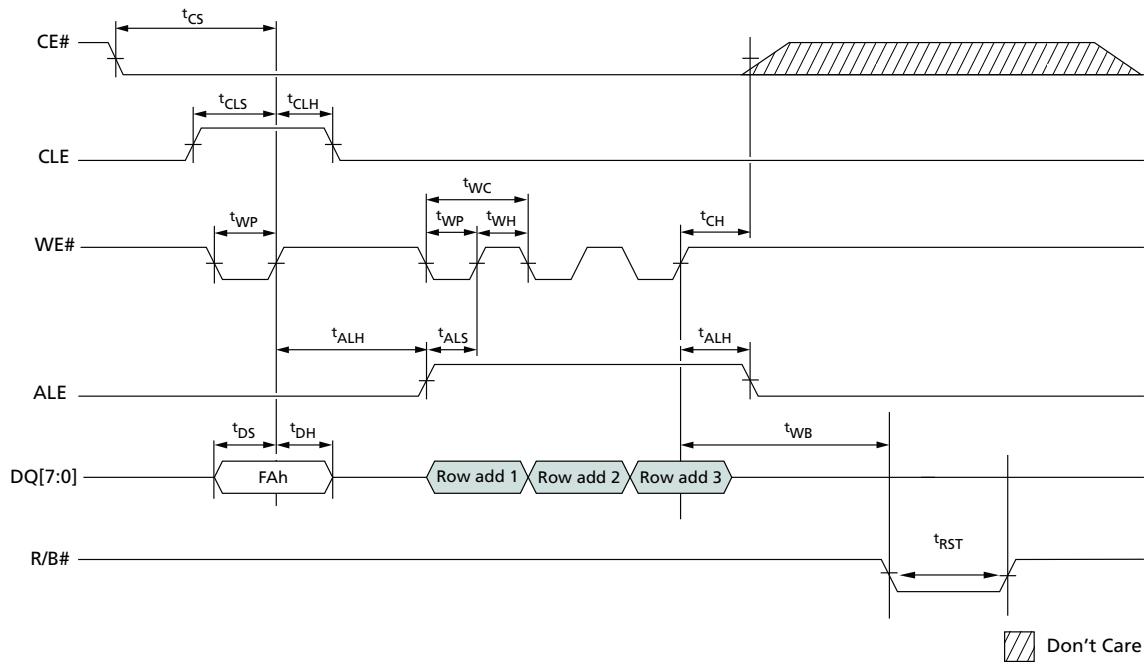
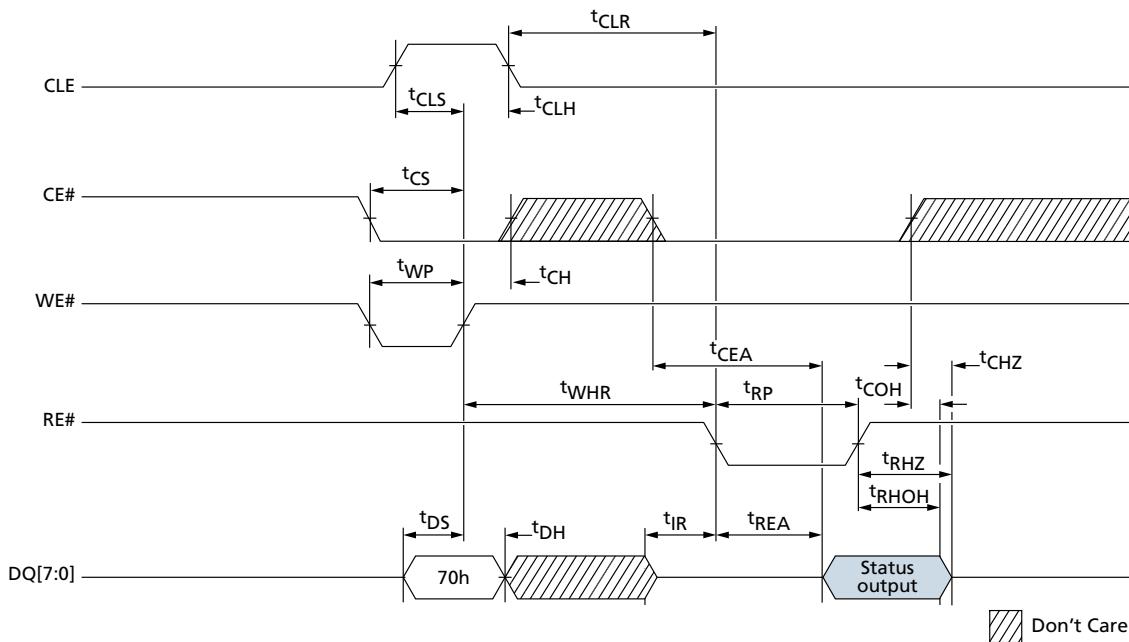
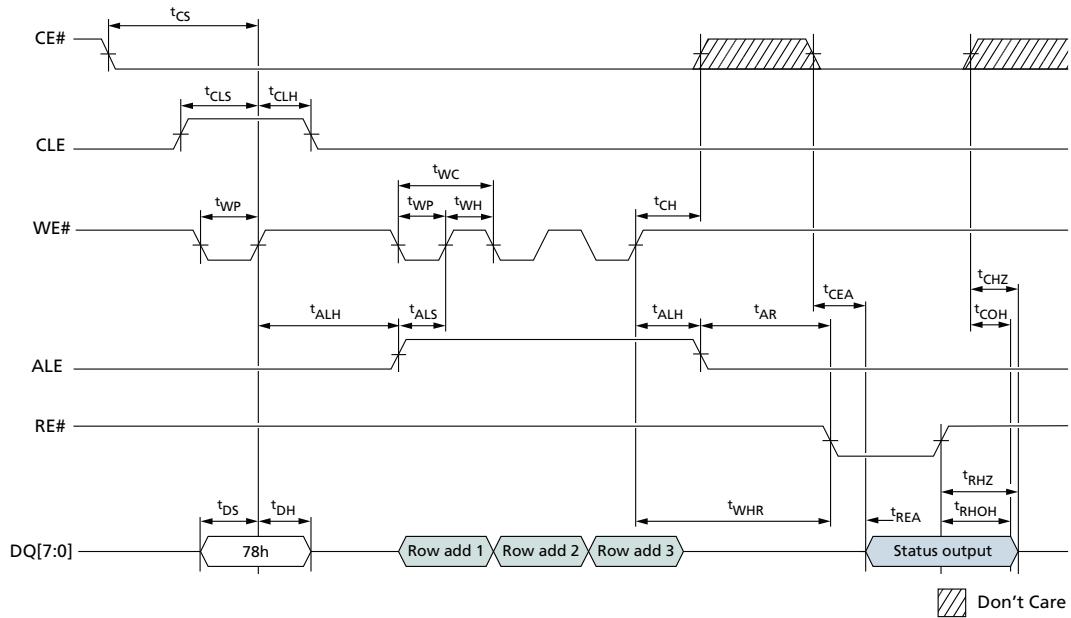
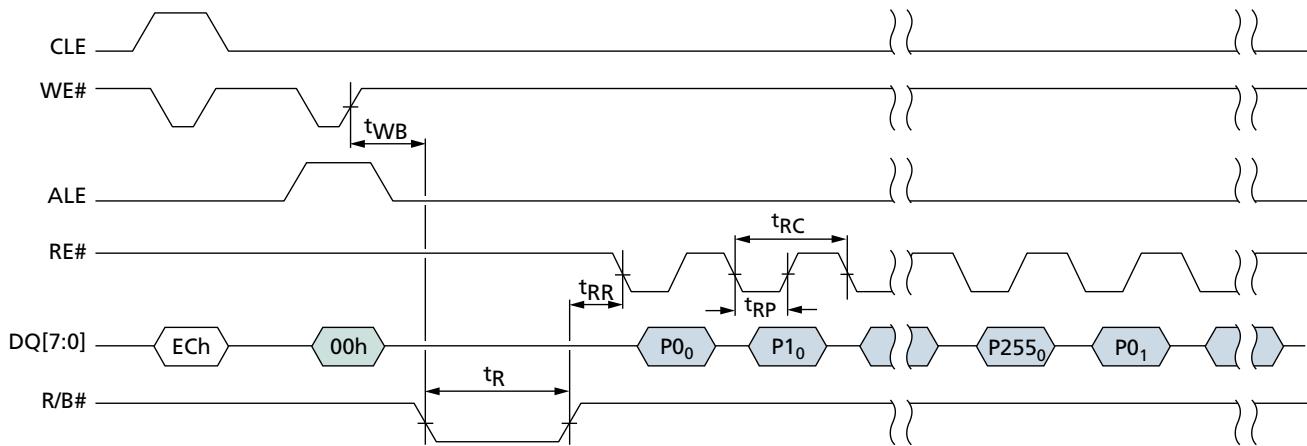
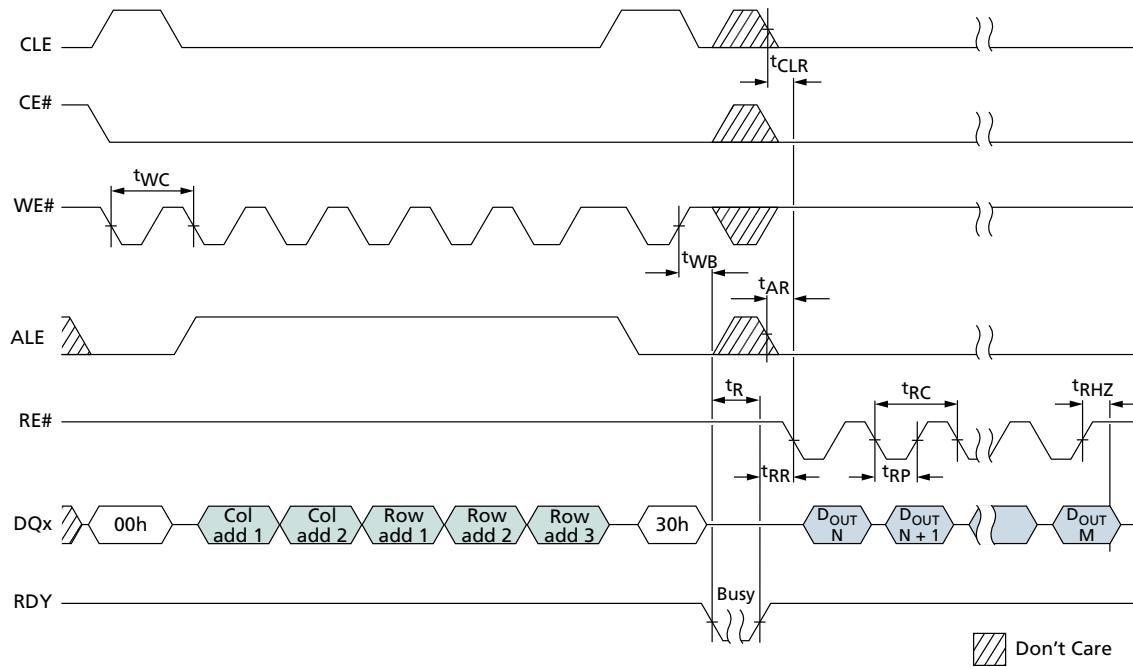
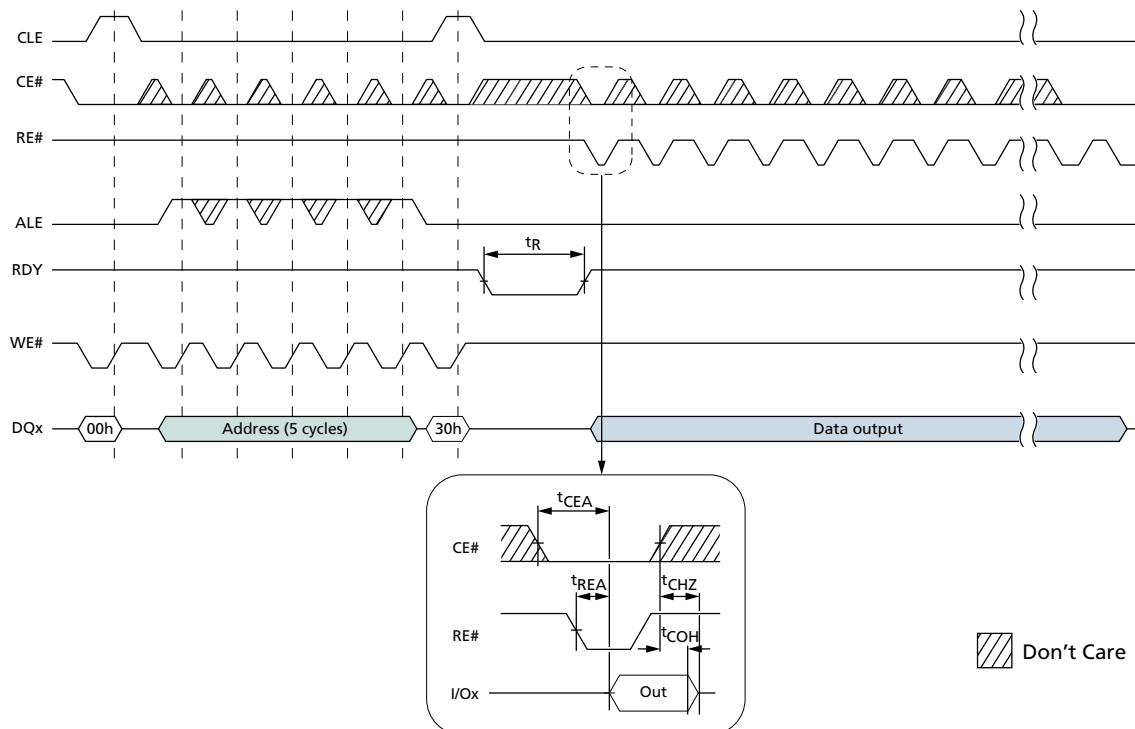
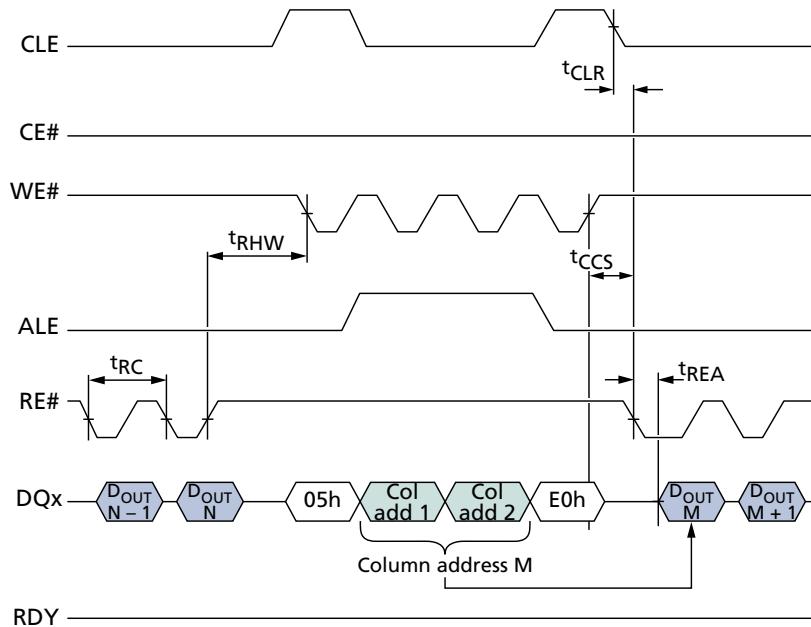


Figure 98: RESET LUN Operation



**Figure 99: READ STATUS Cycle****Figure 100: READ STATUS ENHANCED Cycle**

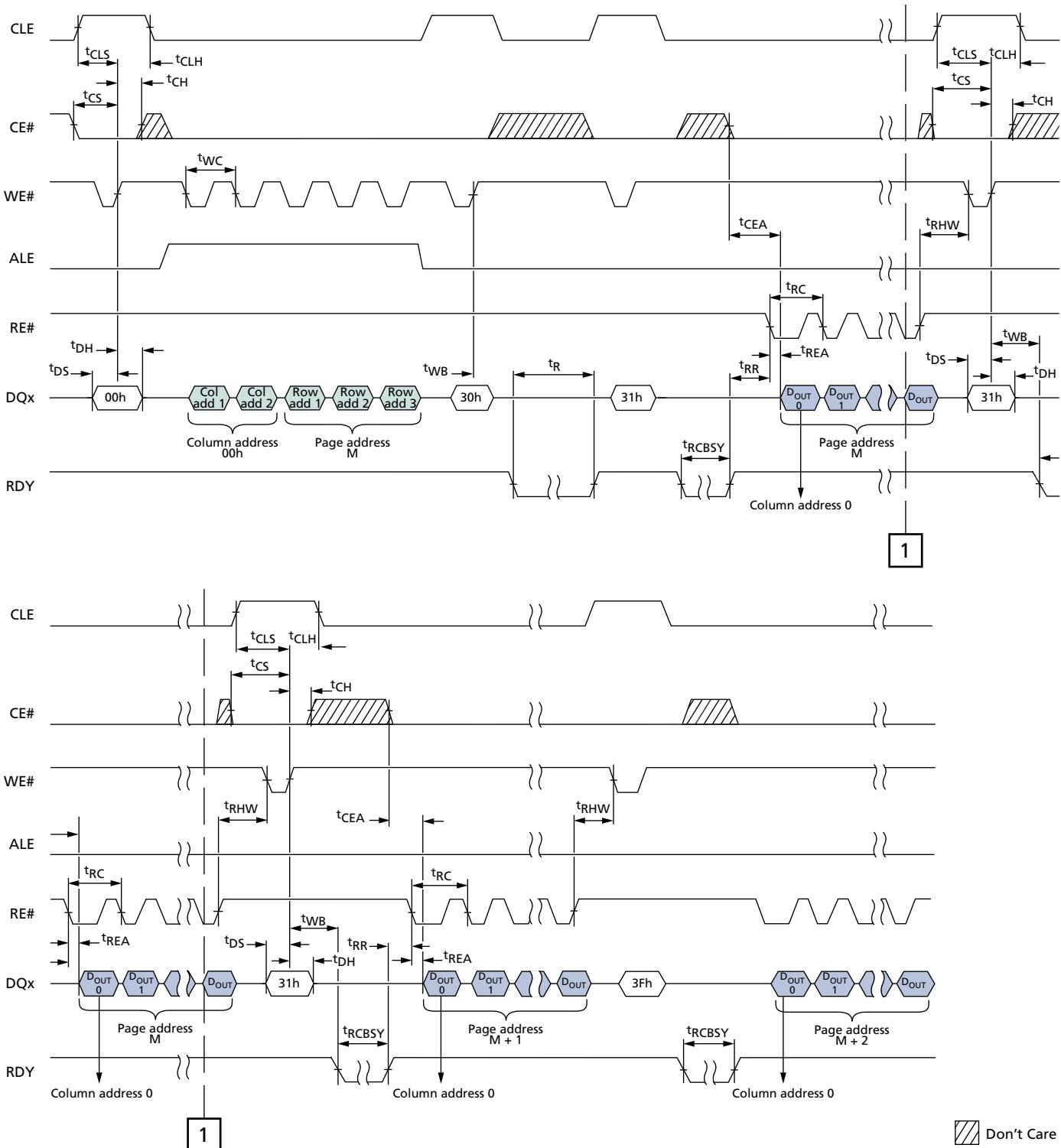
**Figure 101: READ PARAMETER PAGE****Figure 102: READ PAGE**

**Figure 103: READ PAGE Operation with CE# "Don't Care"****Figure 104: CHANGE READ COLUMN**



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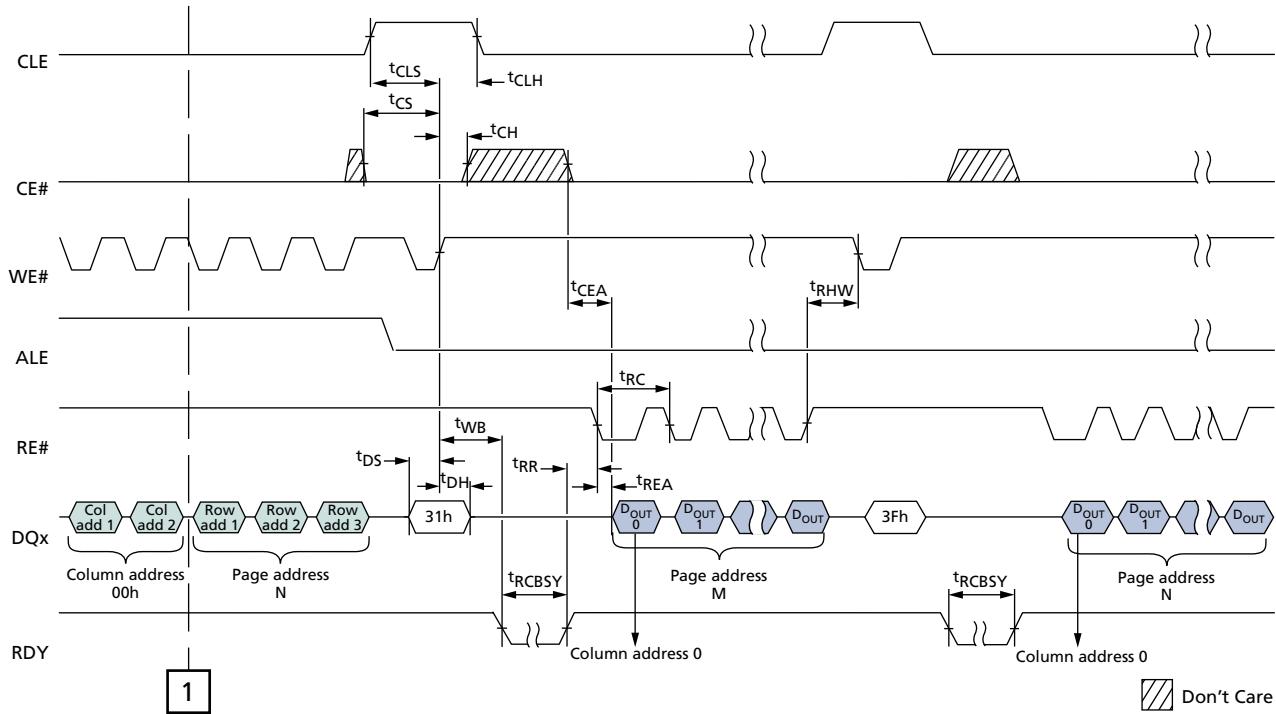
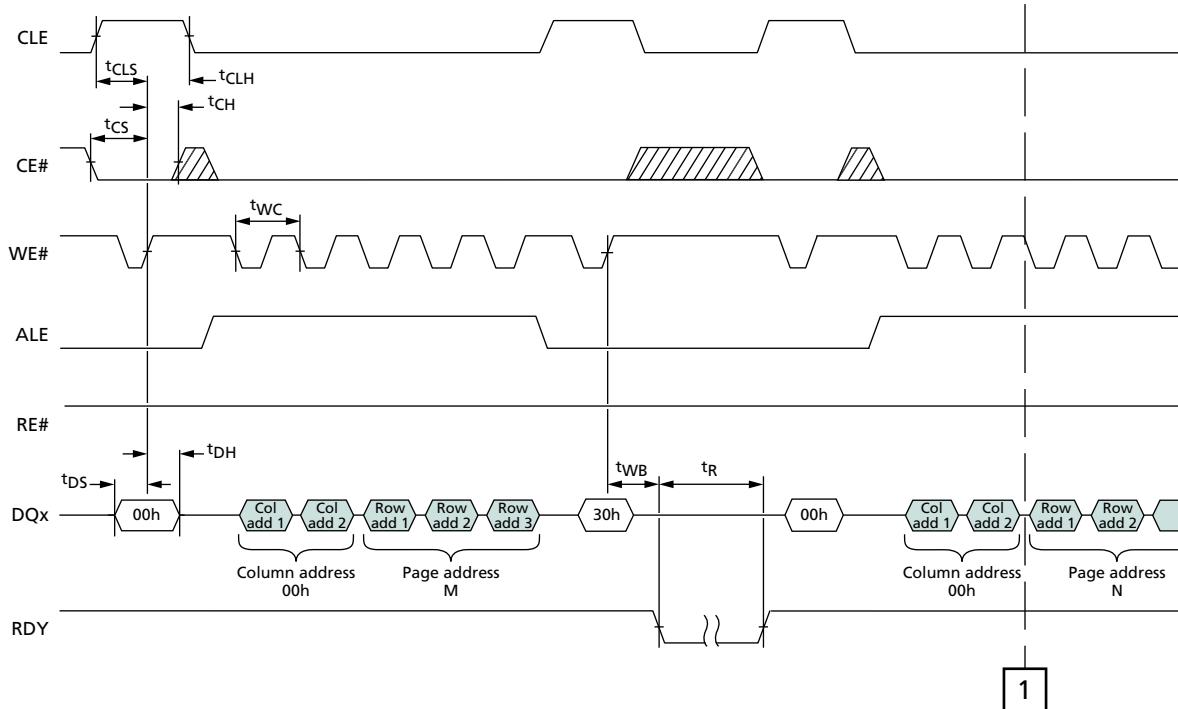
Figure 105: READ PAGE CACHE SEQUENTIAL

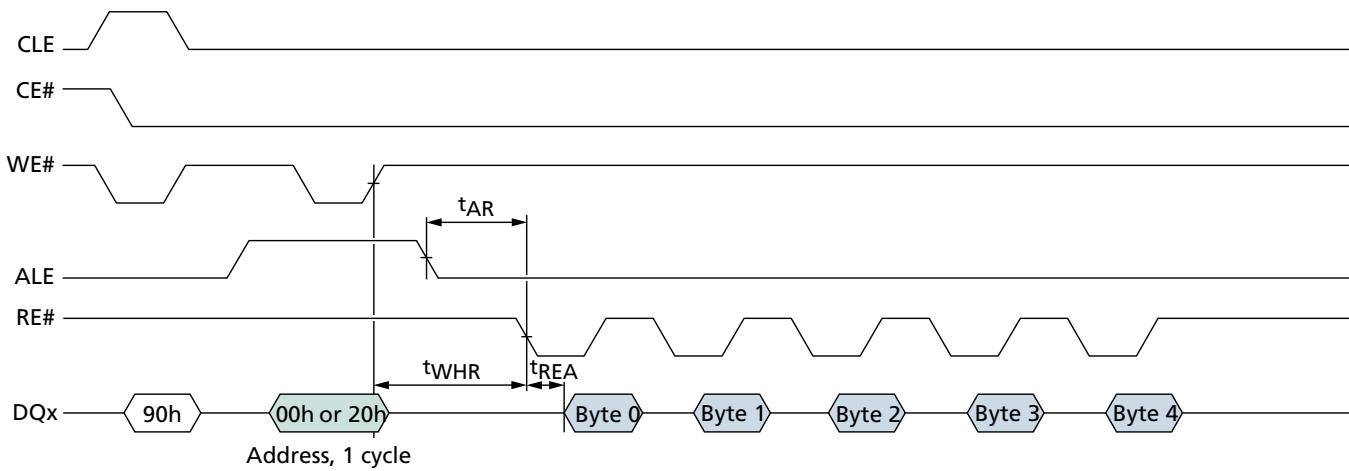
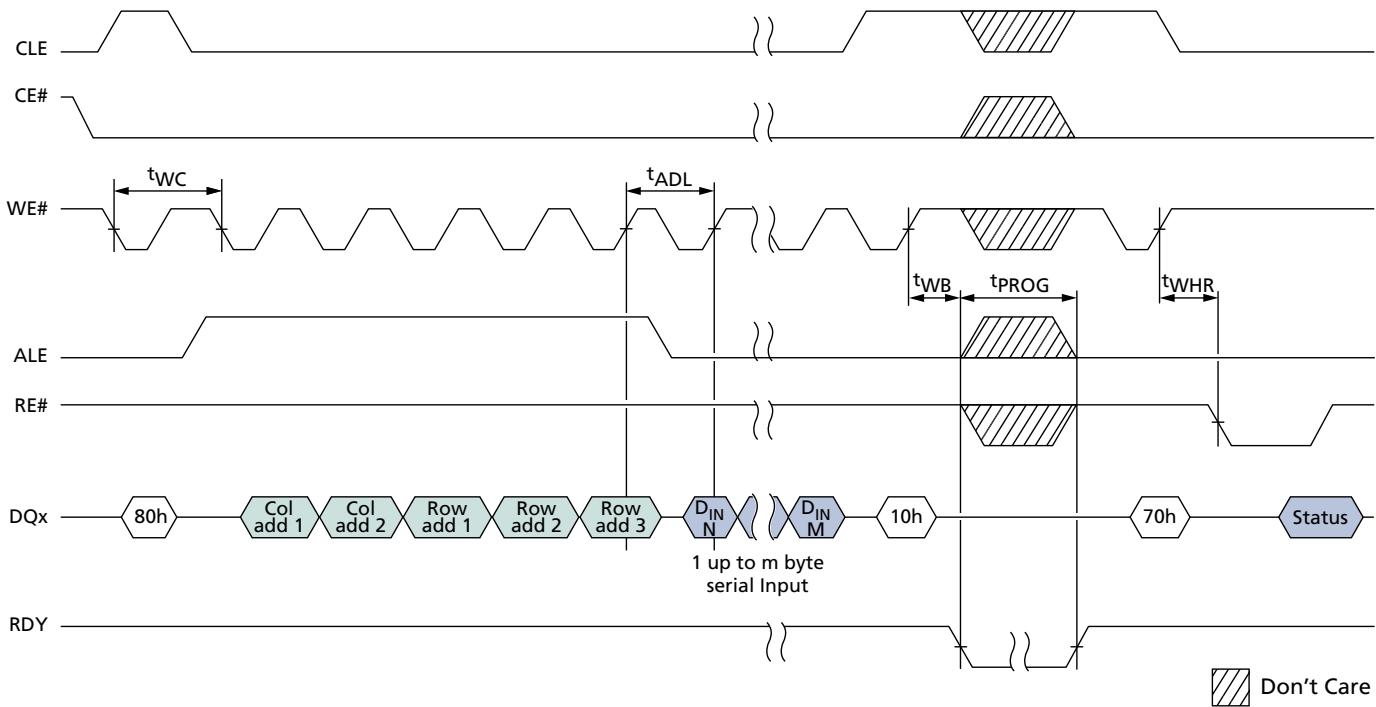




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Figure 106: READ PAGE CACHE RANDOM



**Figure 107: READ ID Operation****Figure 108: PROGRAM PAGE Operation**



MLC 128Gb to 512Gb Async/Sync NAND Asynchronous Interface Timing Diagrams

Figure 109: PROGRAM PAGE Operation with CE# “Don’t Care”

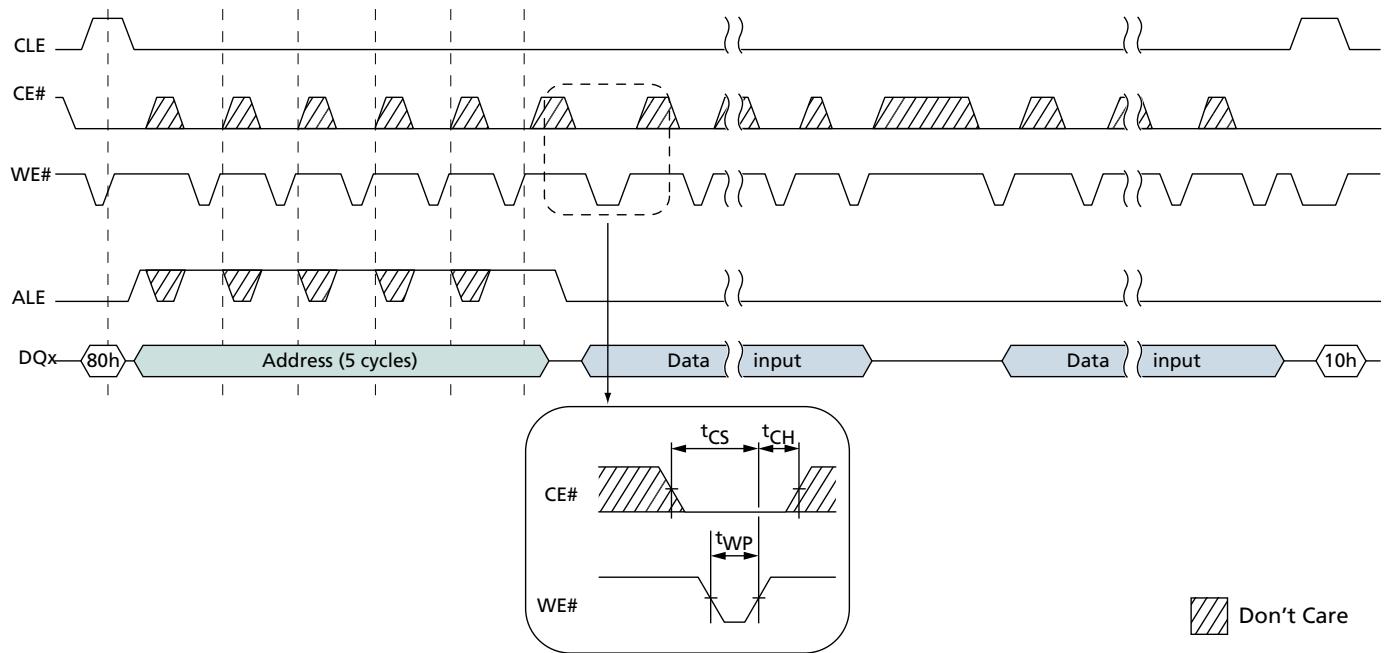
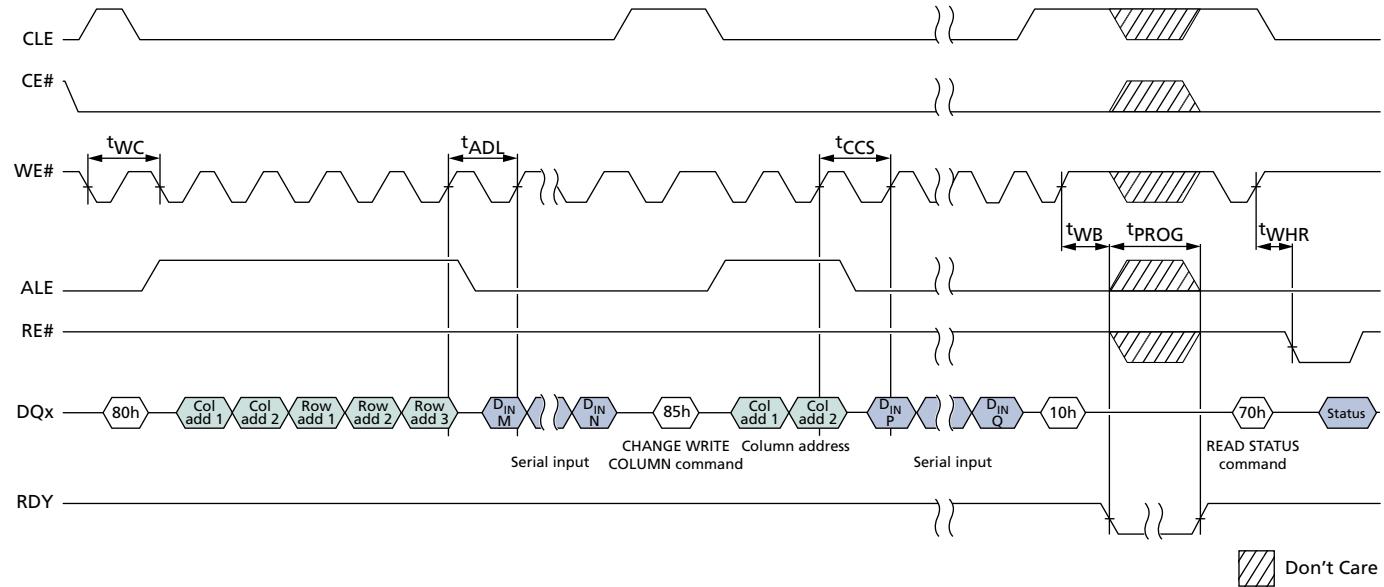
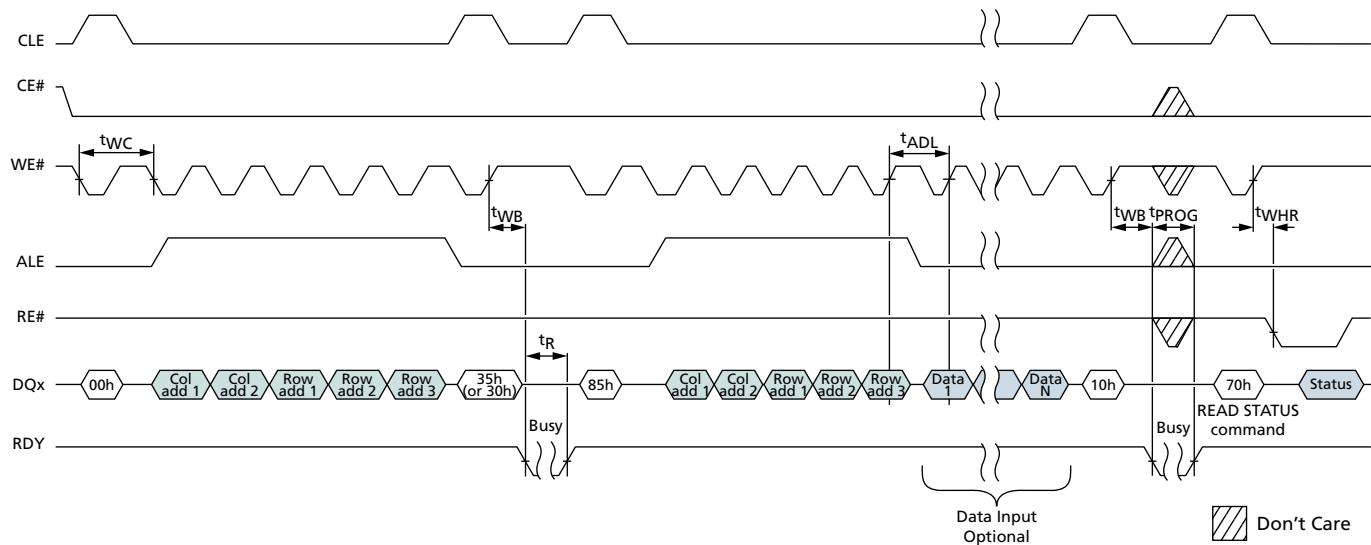
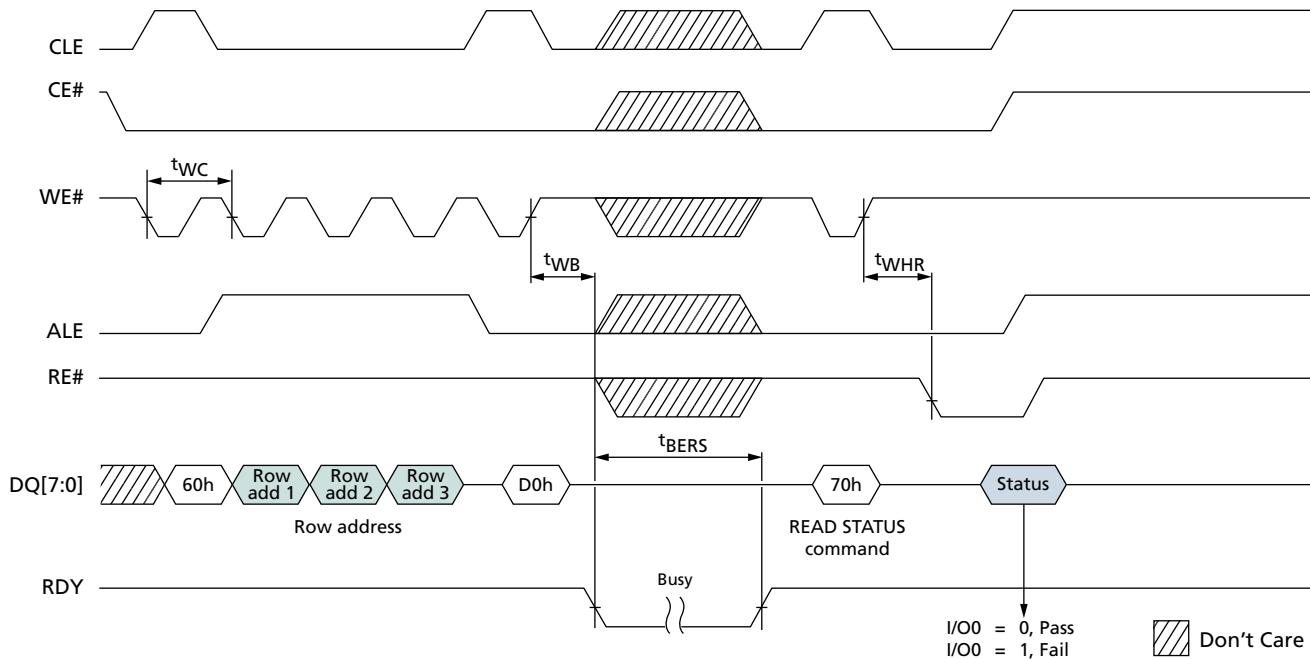


Figure 110: PROGRAM PAGE Operation with CHANGE WRITE COLUMN





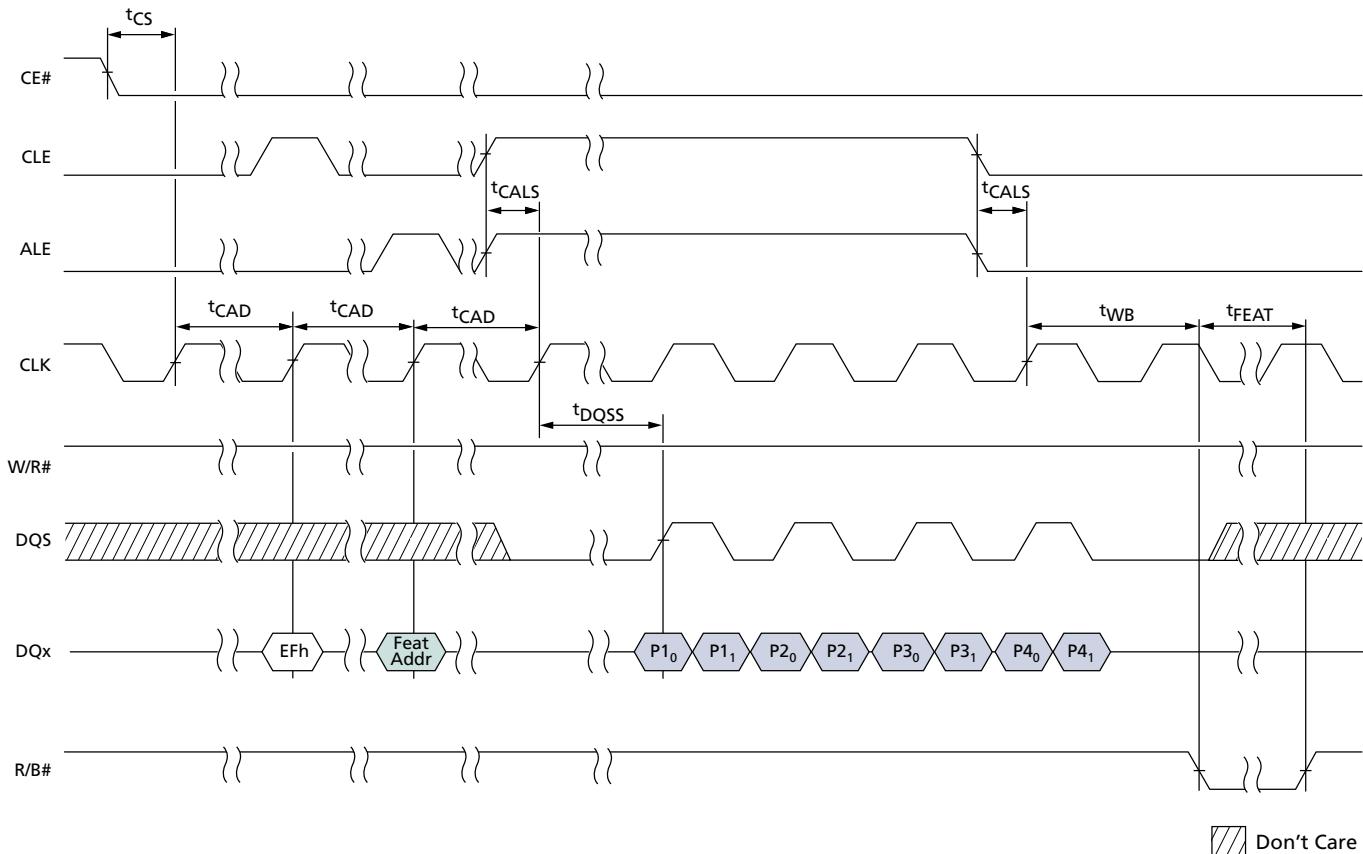
MLC 128Gb to 512Gb Async/Sync NAND Asynchronous Interface Timing Diagrams

Figure 111: COPYBACK**Figure 112: ERASE BLOCK Operation**

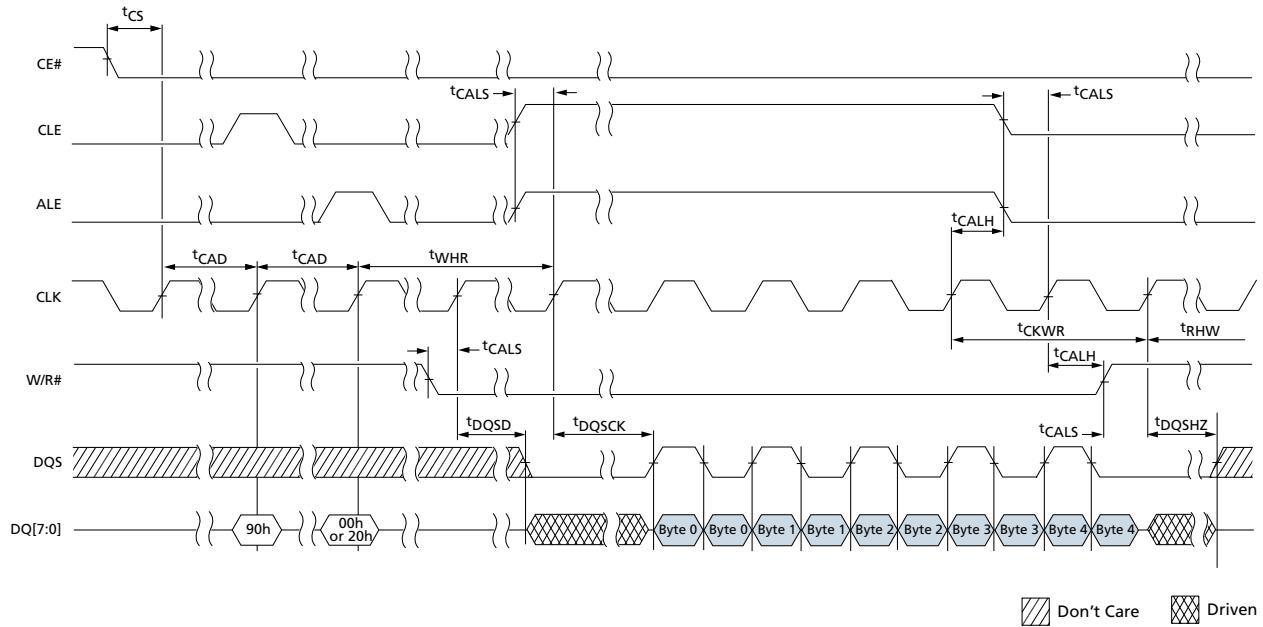
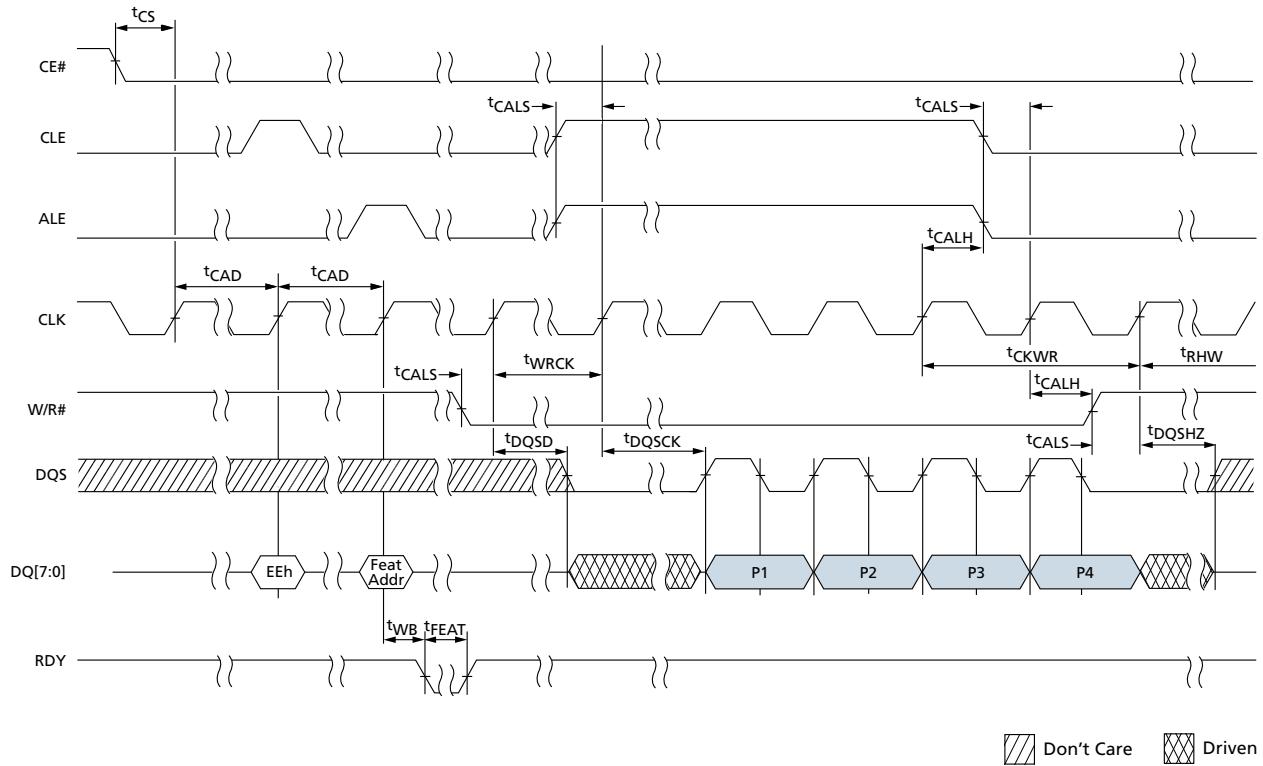


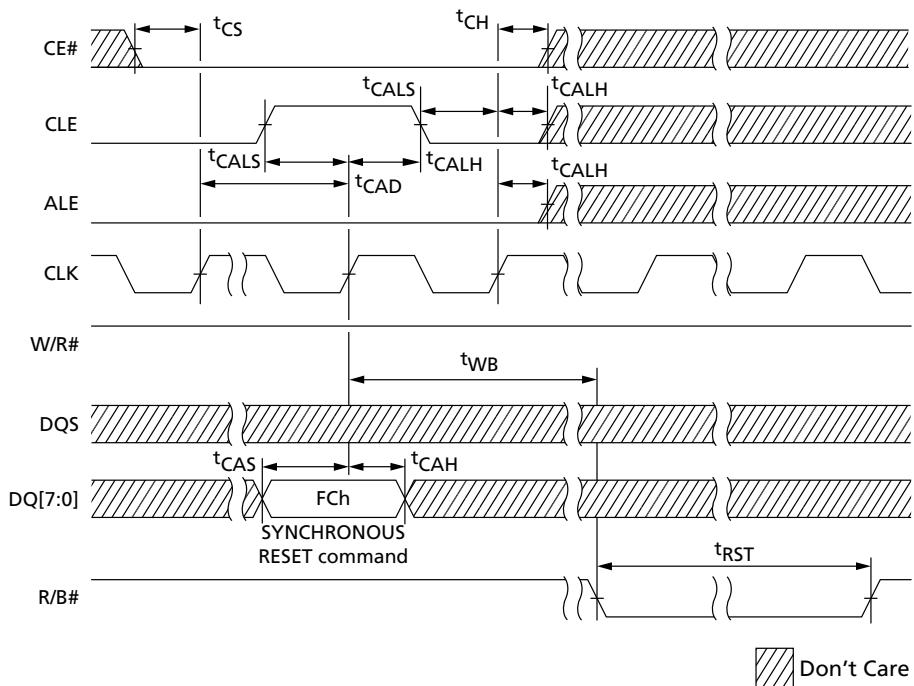
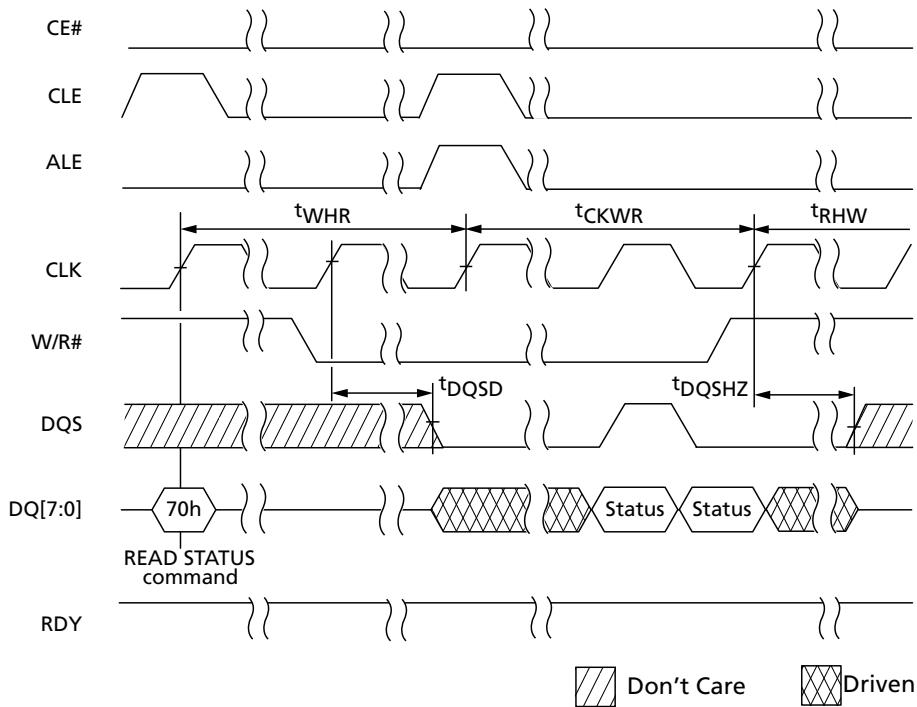
NV-DDR Interface Timing Diagrams

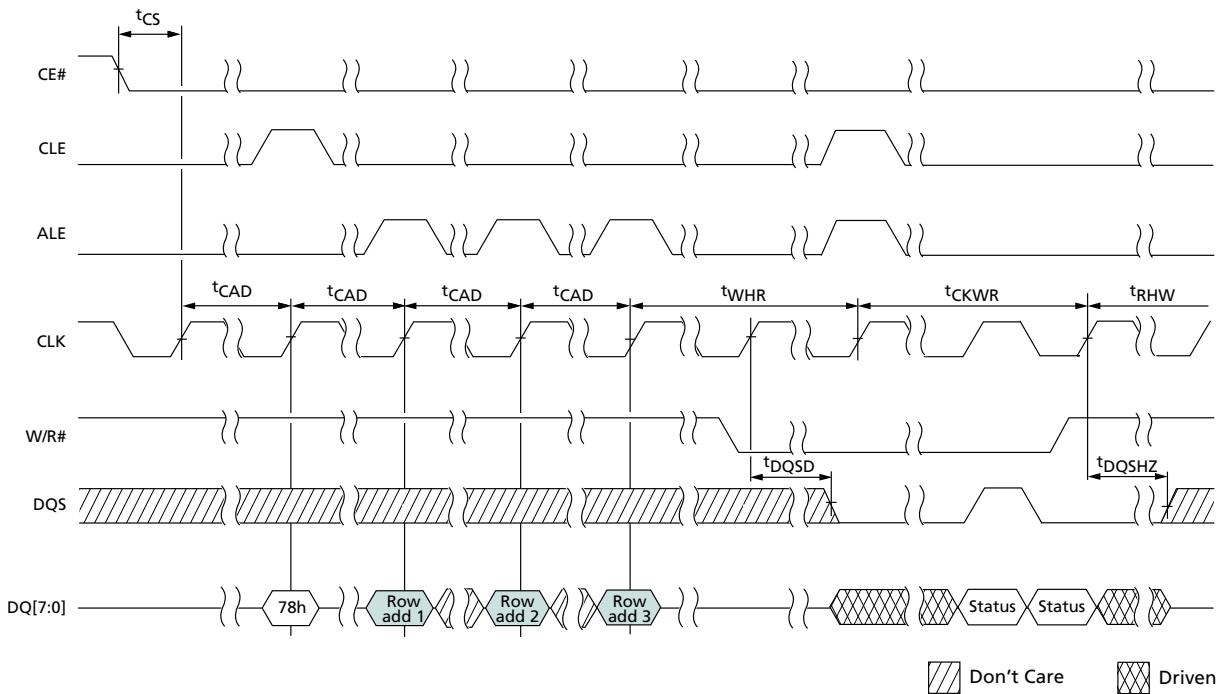
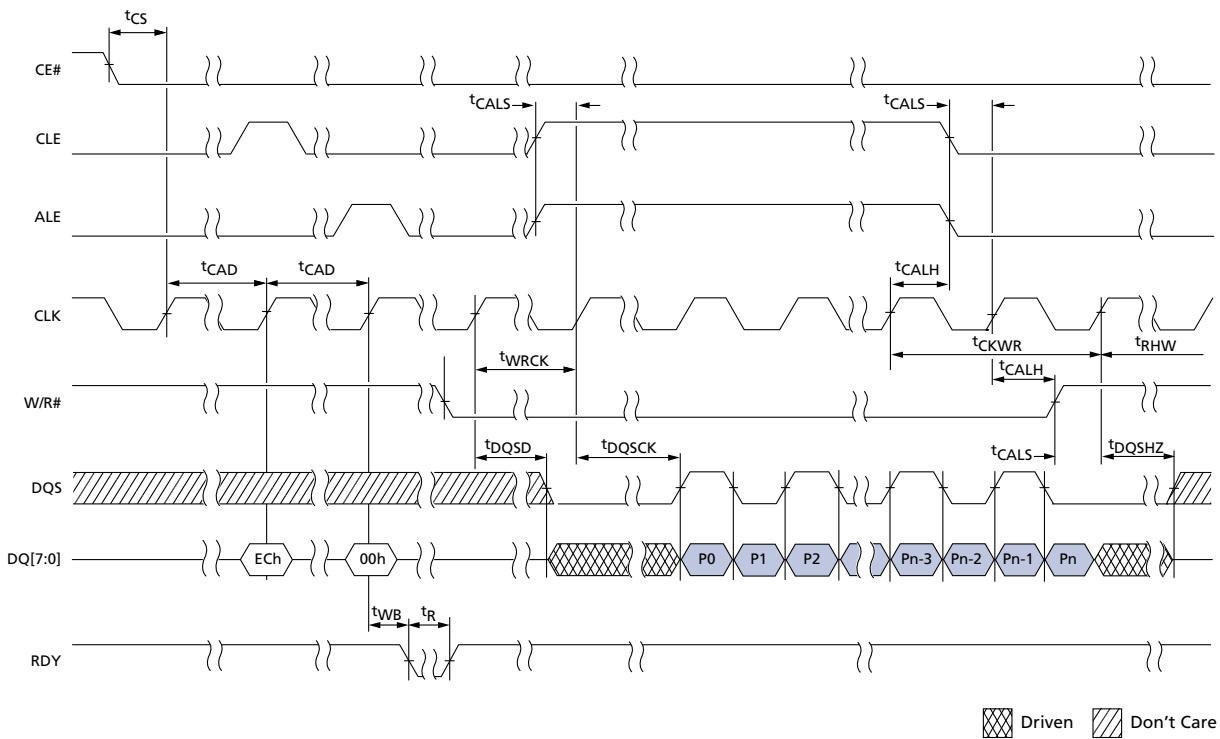
Figure 113: SET FEATURES Operation

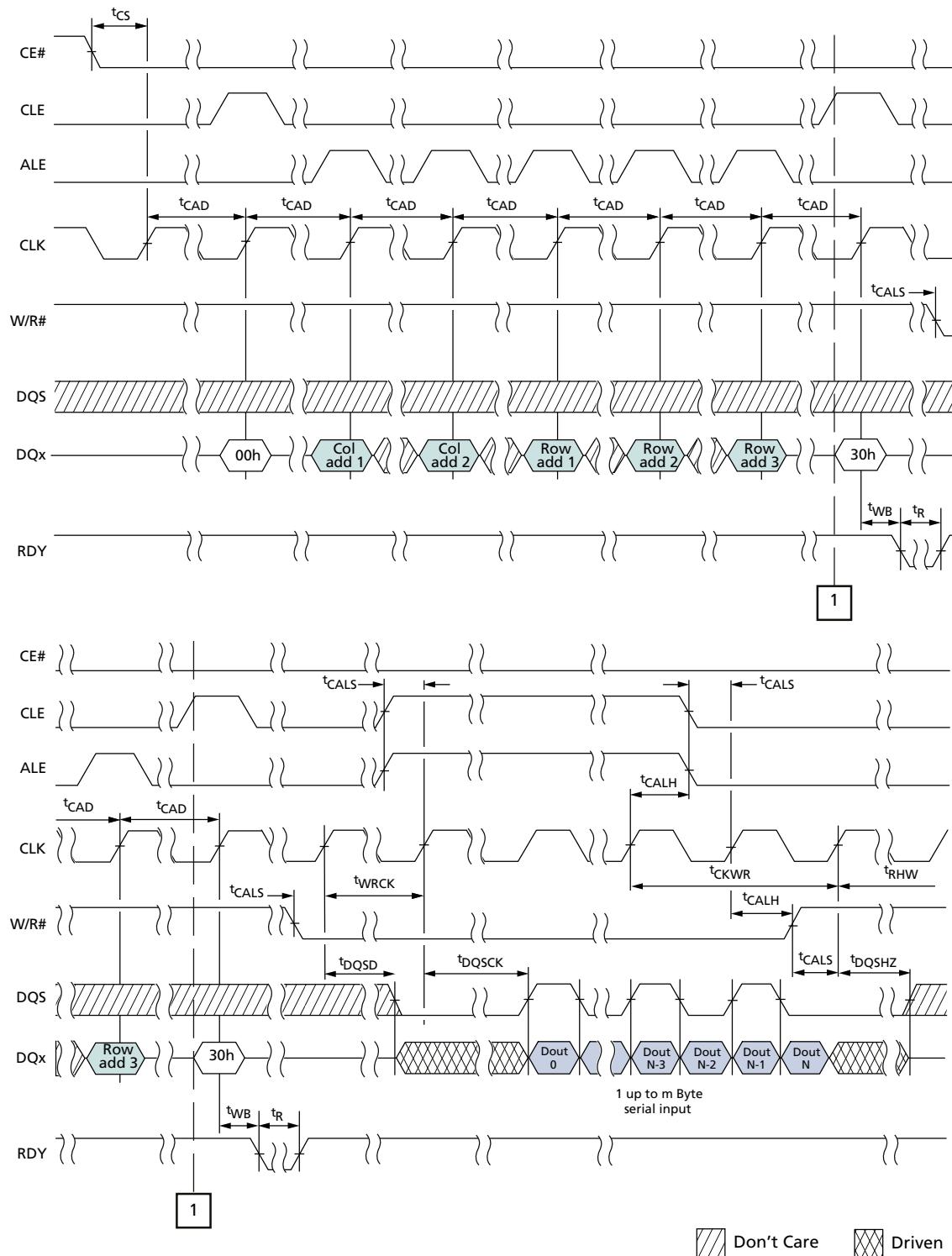


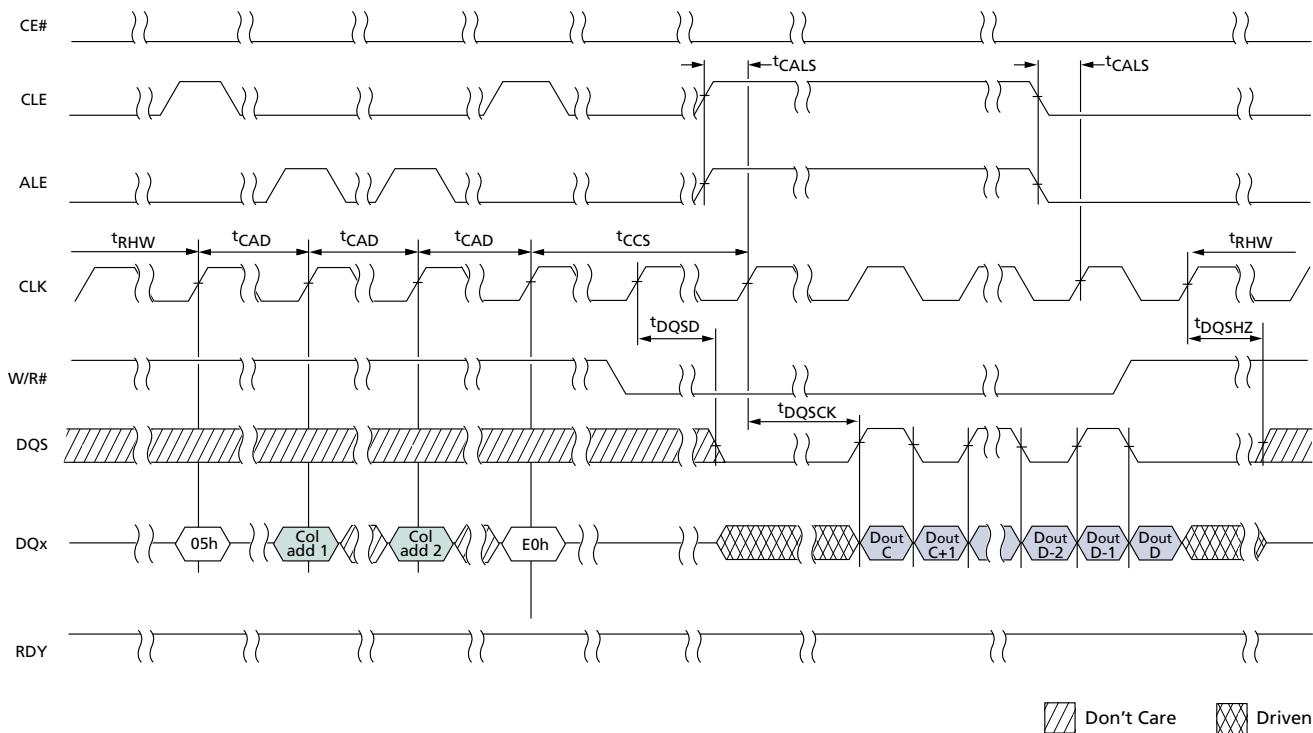
- Notes:
1. When CE# remains LOW, t_{CAD} begins at the rising edge of the clock from which the last data byte is input for the subsequent command or data input cycle(s).
 2. t_{DSH} (MIN) generally occurs during t_{DQSS} (MIN).
 3. t_{DSS} (MIN) generally occurs during t_{DQSS} (MAX).
 4. The cycle that t_{CAD} is measured from may be an idle cycle (as shown), another command cycle, an address cycle, or a data cycle. The idle cycle is shown in this diagram for simplicity.

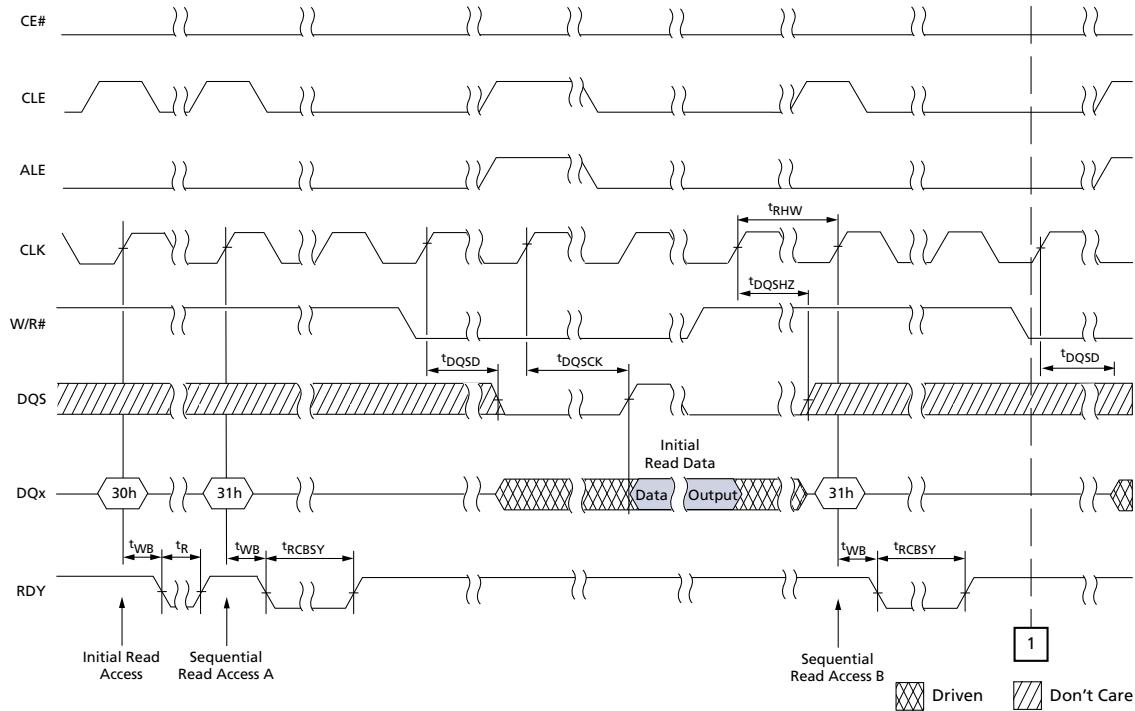
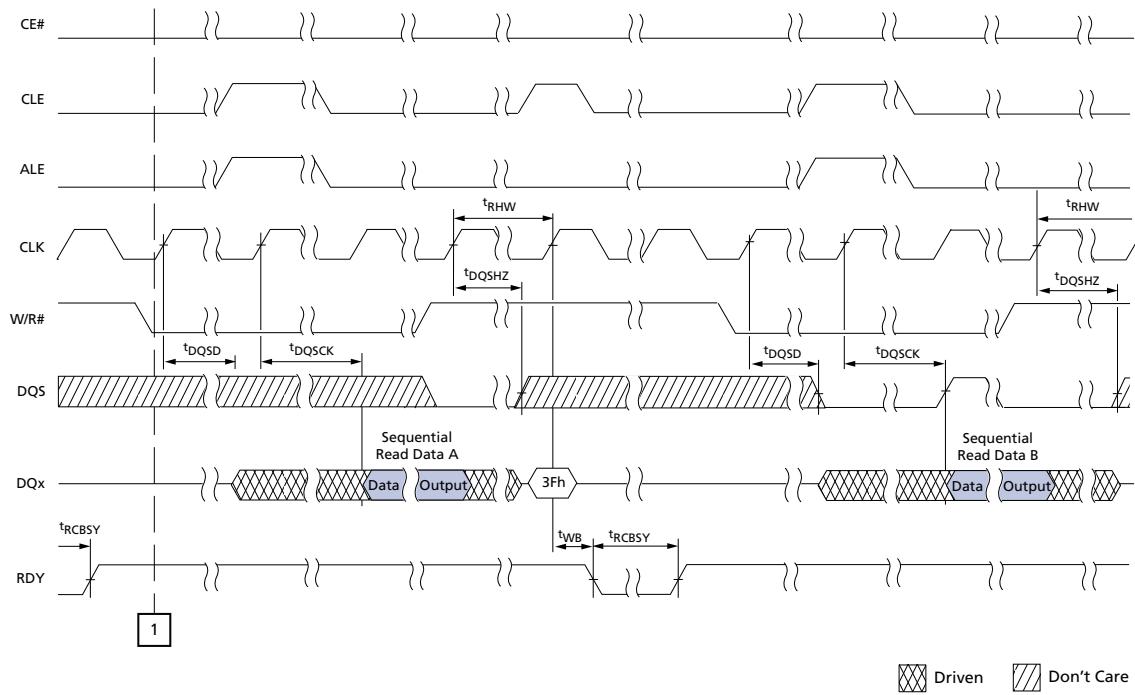
**Figure 114: READ ID Operation****Figure 115: GET FEATURES Operation**

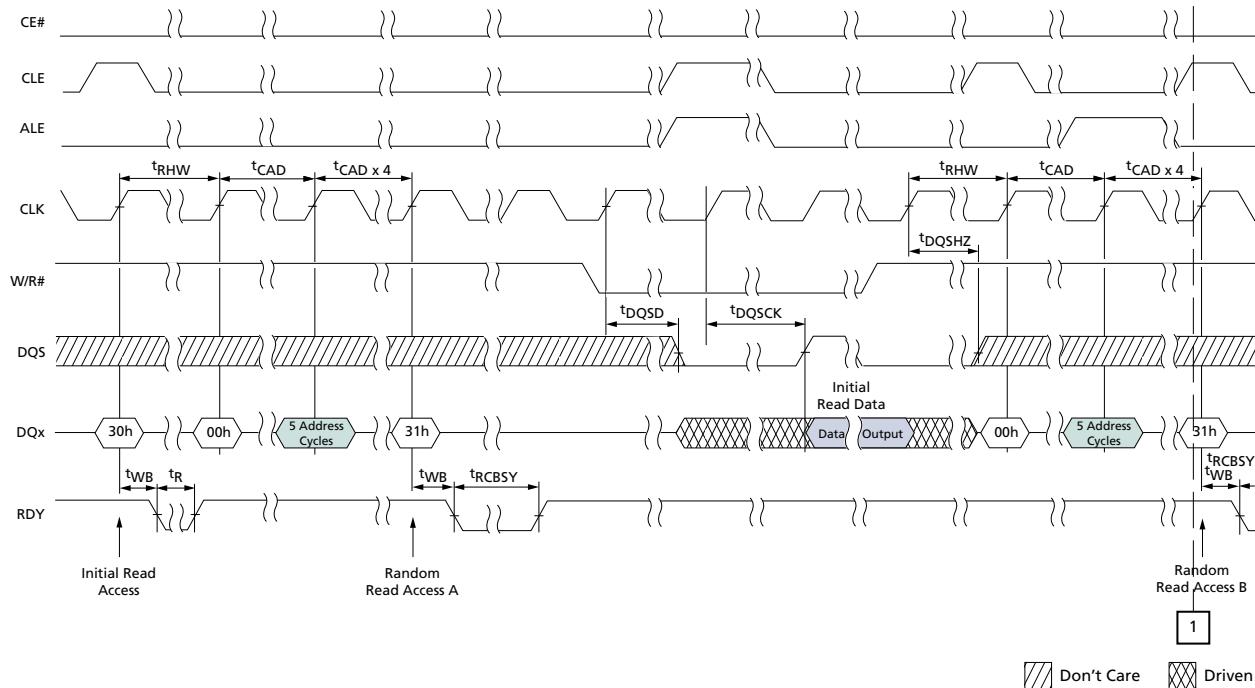
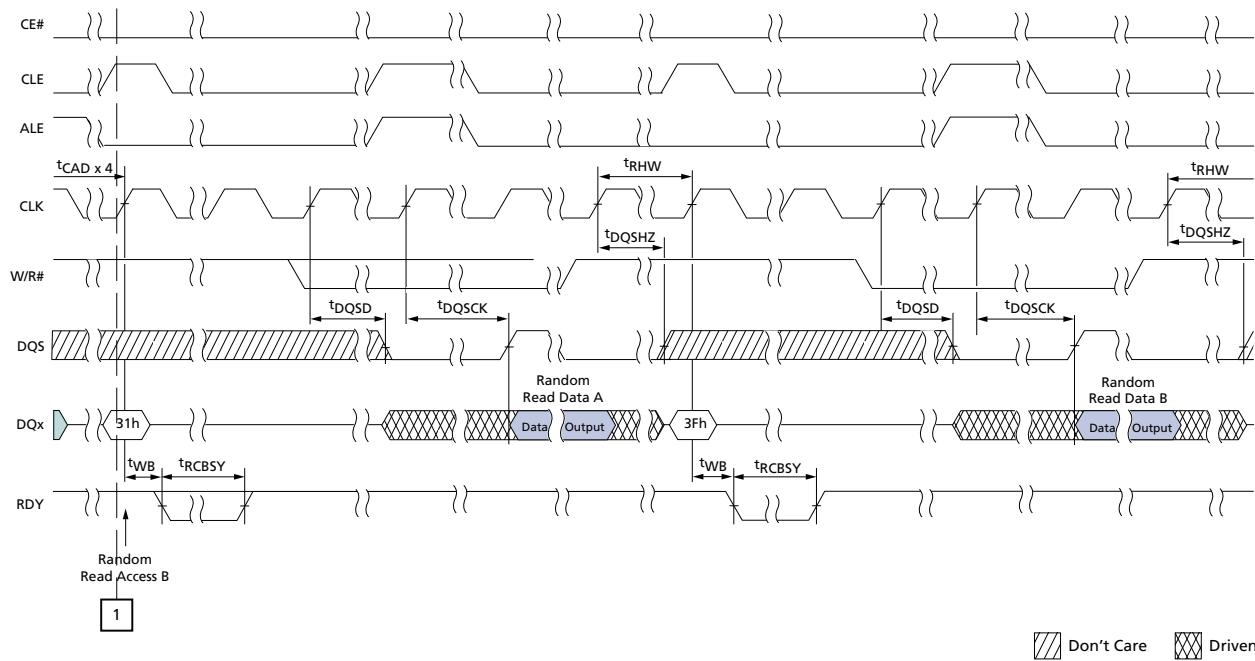
**Figure 116: RESET (FCh) Operation****Figure 117: READ STATUS Cycle**

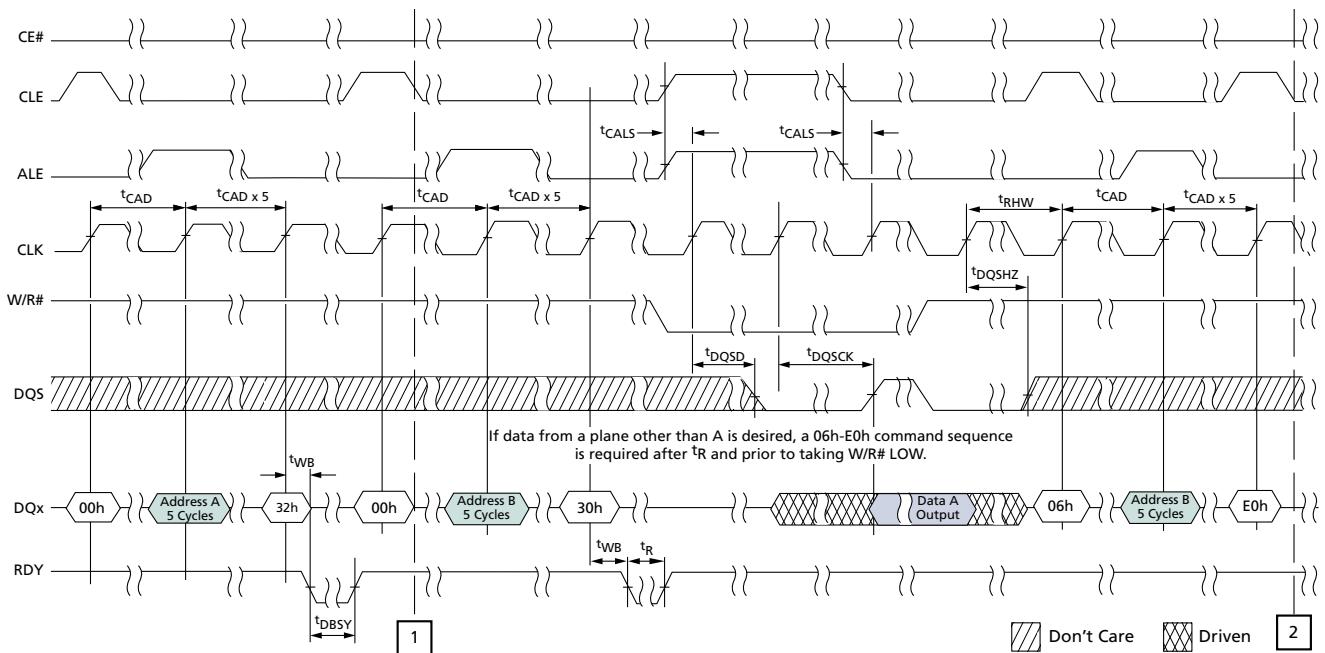
**Figure 118: READ STATUS ENHANCED Operation****Figure 119: READ PARAMETER PAGE Operation**

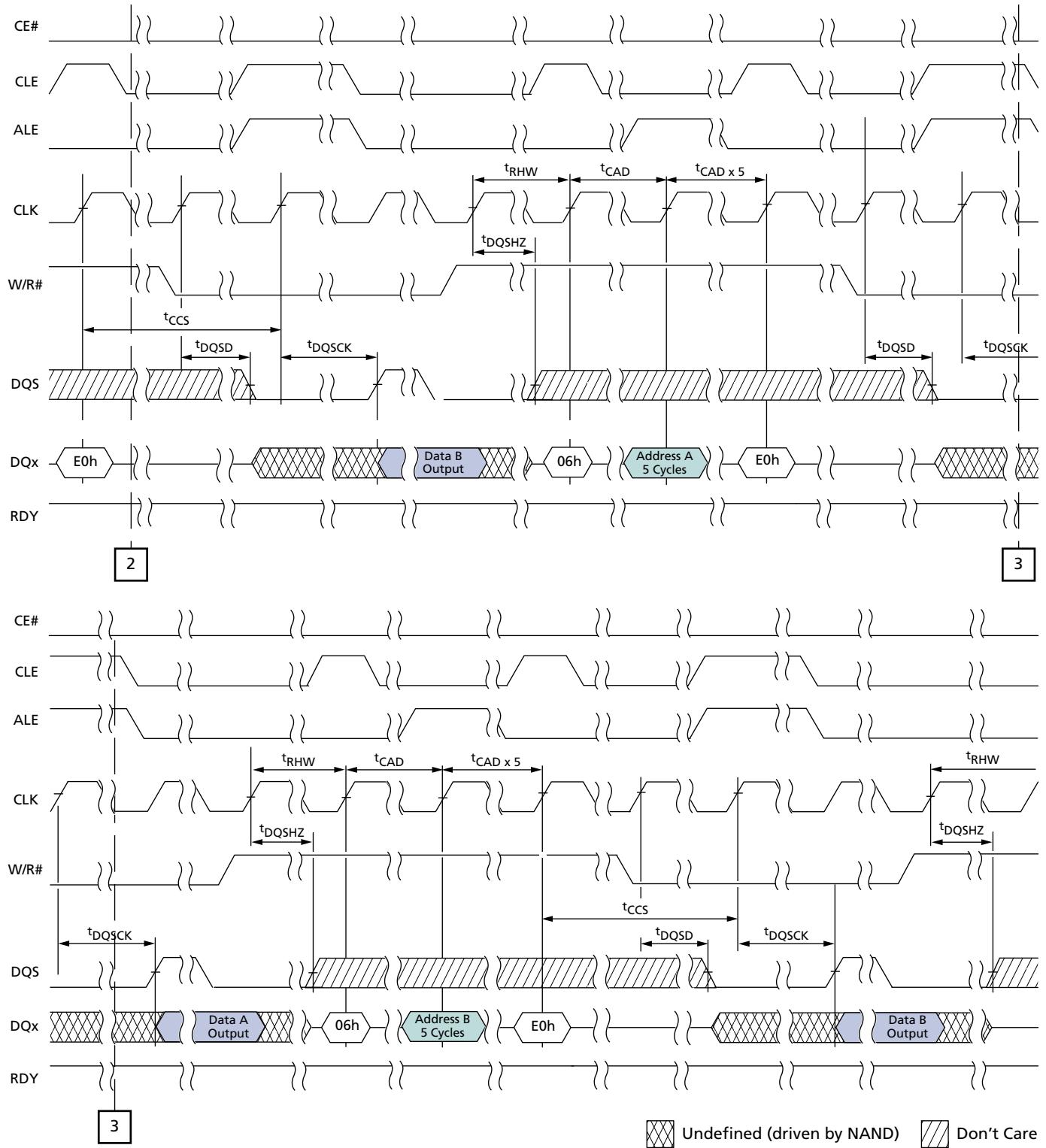
**Figure 120: READ PAGE Operation**

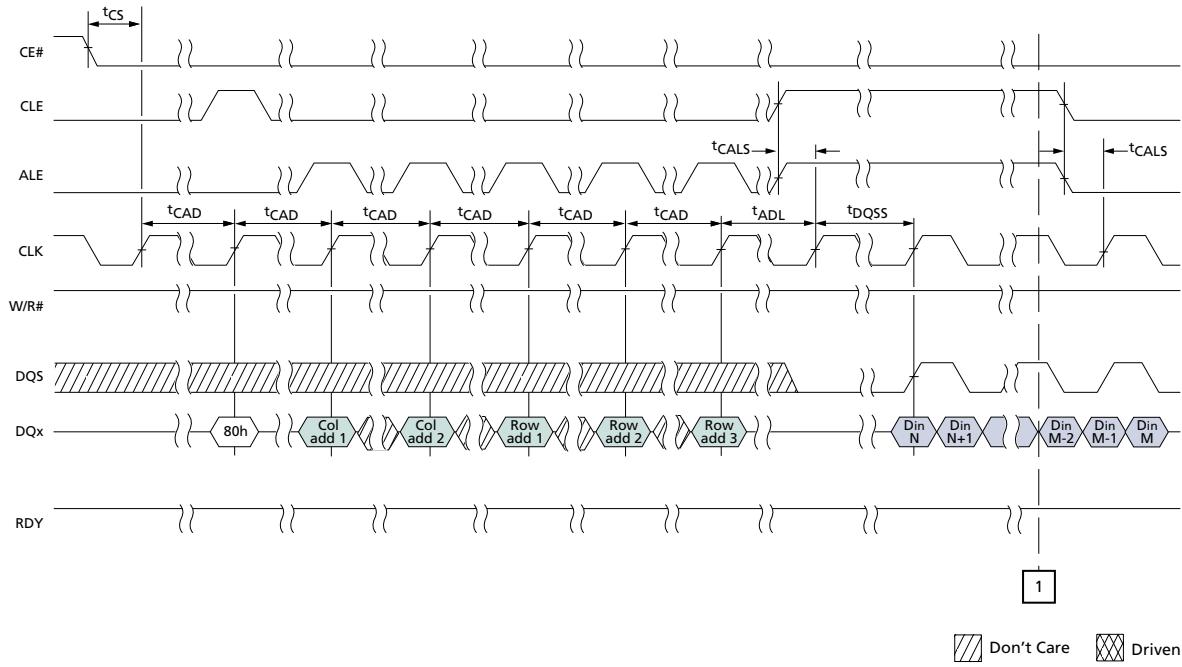

**MLC 128Gb to 512Gb Async/Sync NAND
NV-DDR Interface Timing Diagrams**
Figure 121: CHANGE READ COLUMN

**Figure 122: READ PAGE CACHE SEQUENTIAL (1 of 2)****Figure 123: READ PAGE CACHE SEQUENTIAL (2 of 2)**

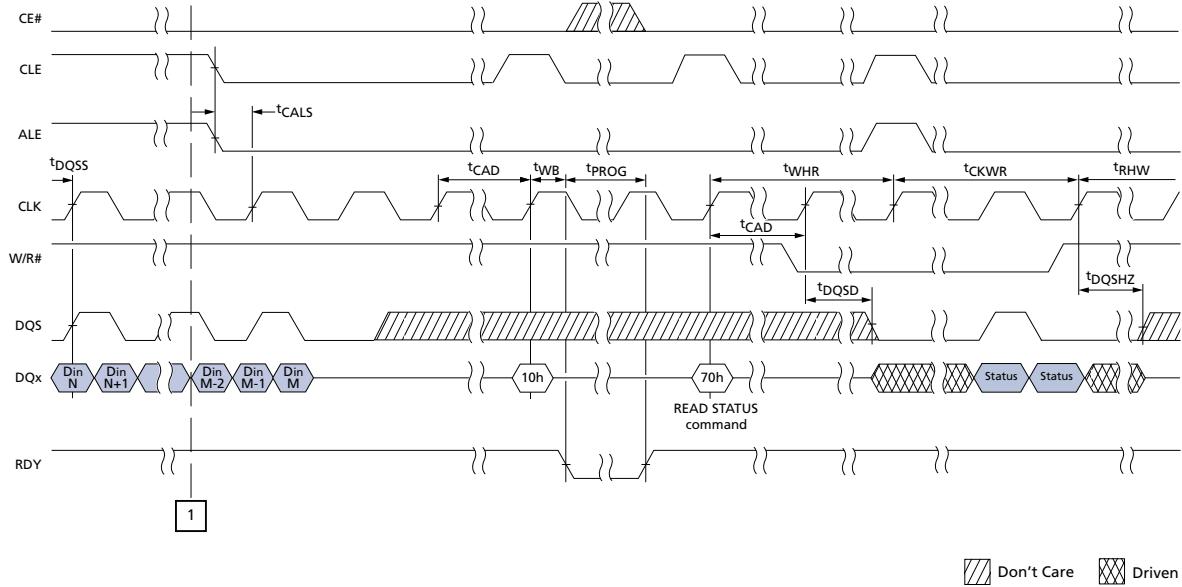
**Figure 124: READ PAGE CACHE RANDOM (1 of 2)****Figure 125: READ PAGE CACHE RANDOM (2 of 2)**

**Figure 126: Multi-Plane Read Page (1 of 2)**

**Figure 127: Multi-Plane Read Page (2 of 2)**

**Figure 128: PROGRAM PAGE Operation (1 of 2)**

Note: 1. Programming timing figures do not represent single-pass programming format - to be updated.

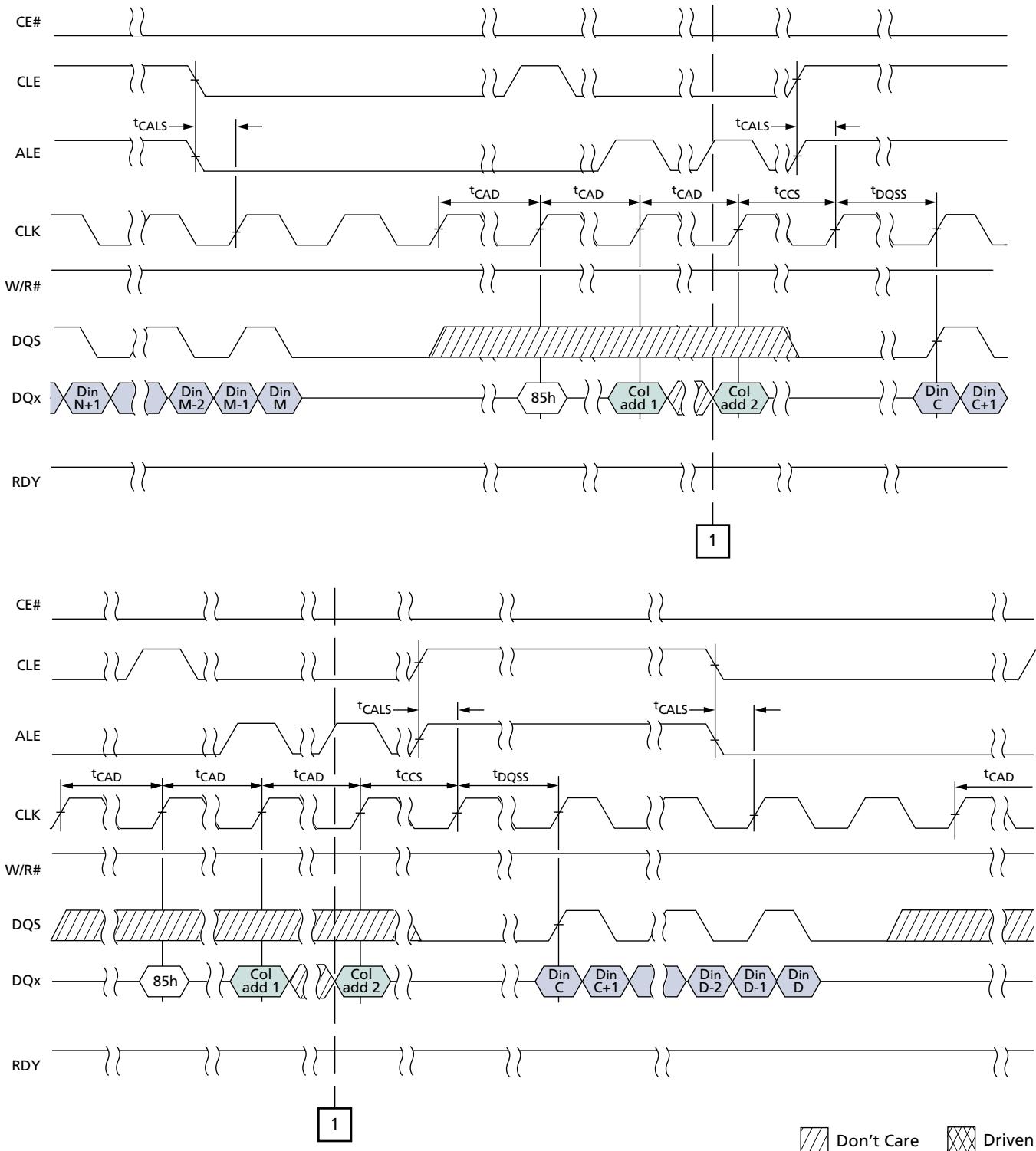
Figure 129: PROGRAM PAGE Operation (2 of 2)

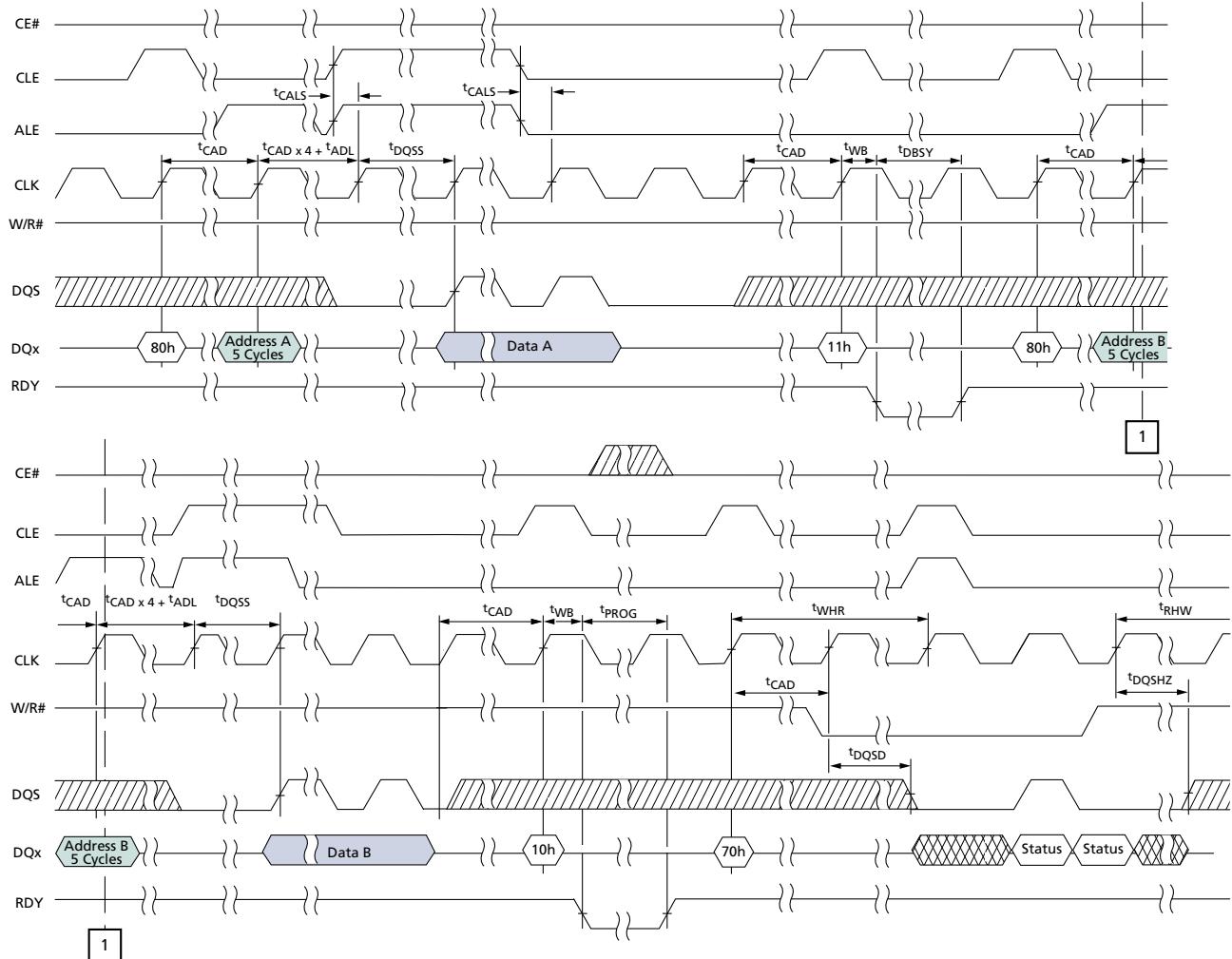
Note: 1. Programming timing figures do not represent single-pass programming format - to be updated.



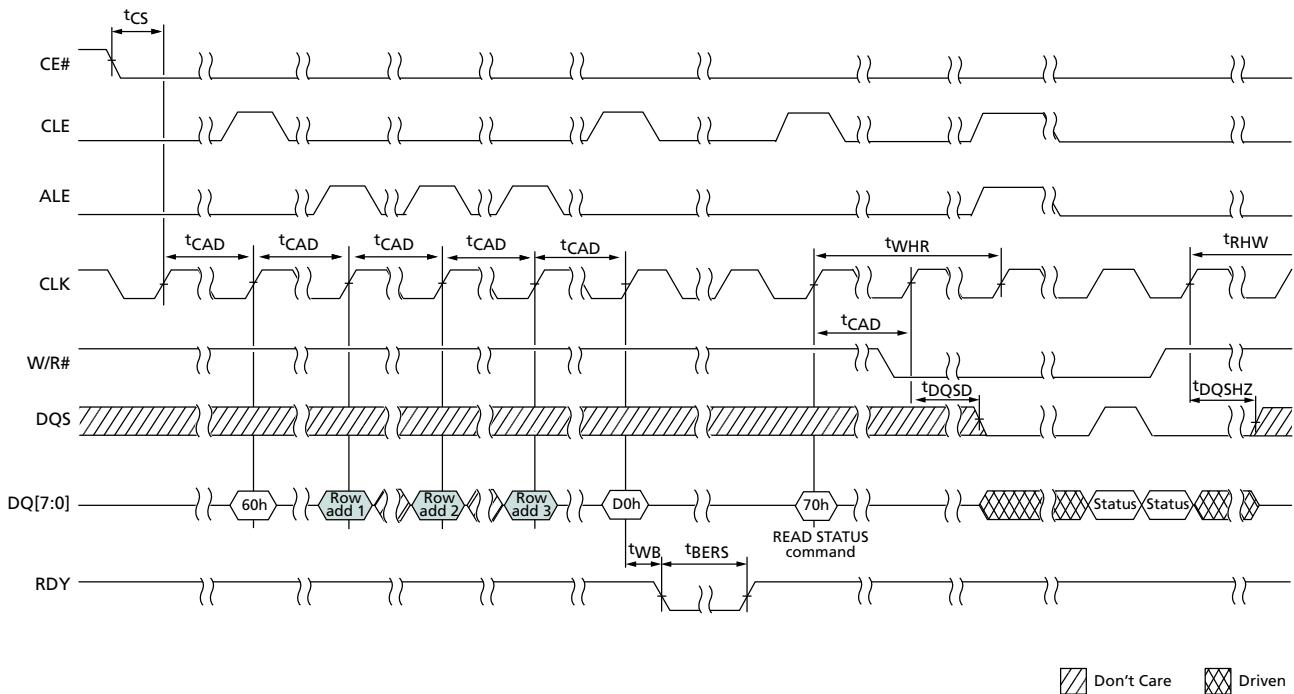
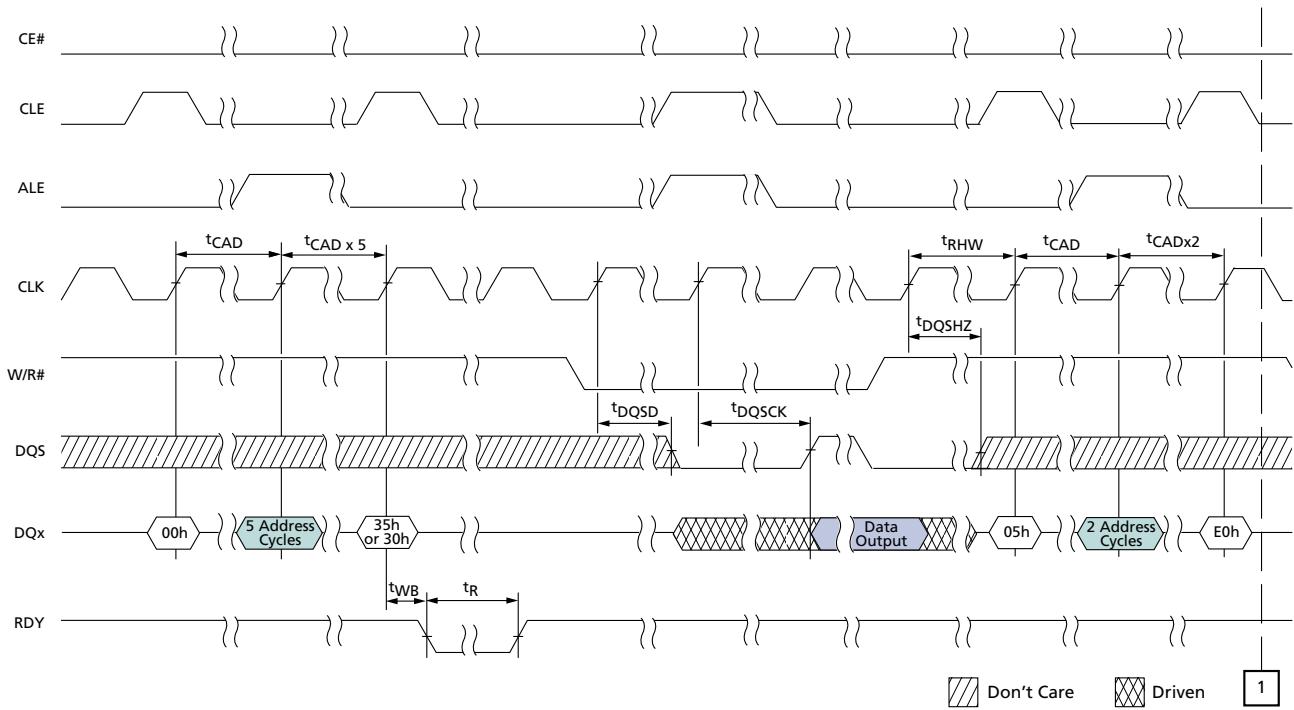
MLC 128Gb to 512Gb Async/Sync NAND NV-DDR Interface Timing Diagrams

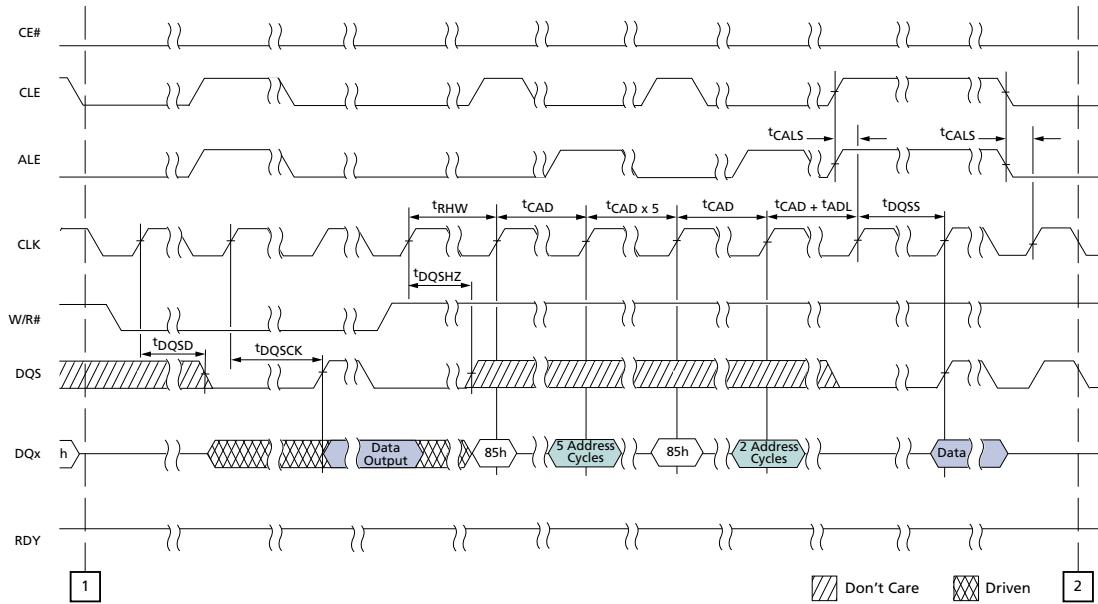
Figure 130: CHANGE WRITE COLUMN



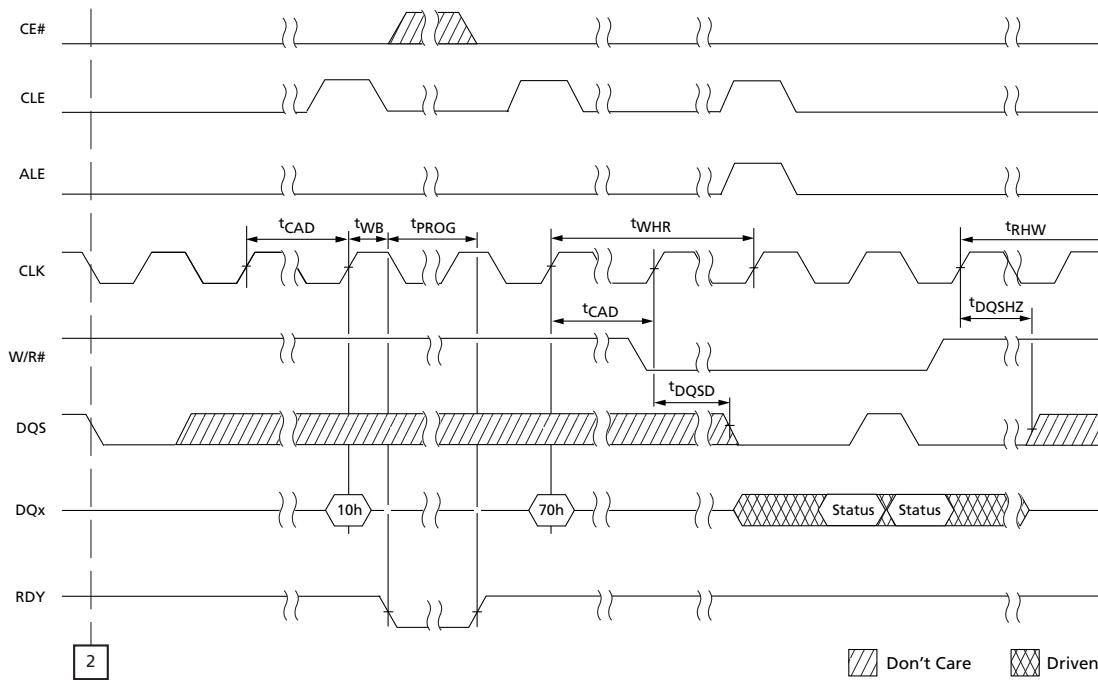
**Figure 131: Multi-Plane Program Page**

Note: 1. Programming timing figures do not represent single-pass programming format - to be updated.

**Figure 132: ERASE BLOCK****Figure 133: COPYBACK (1 of 3)**

**Figure 134: COPYBACK (2 of 3)**

Note: 1. Programming timing figures do not represent single-pass programming format - to be updated.

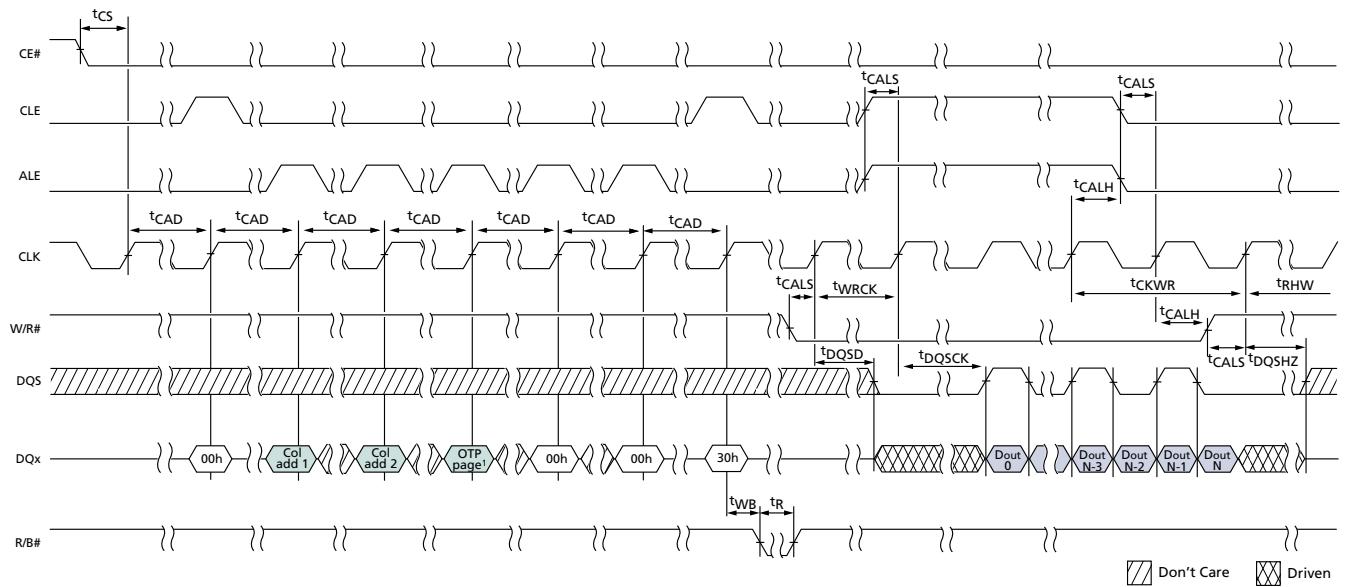
Figure 135: COPYBACK (3 of 3)

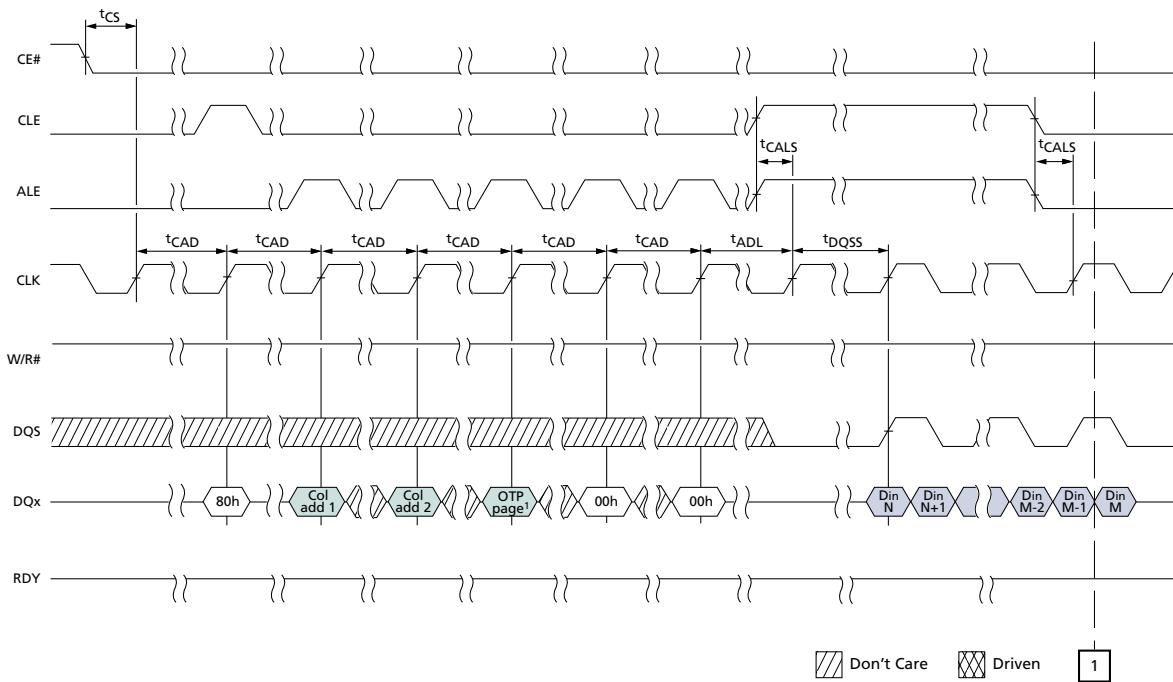
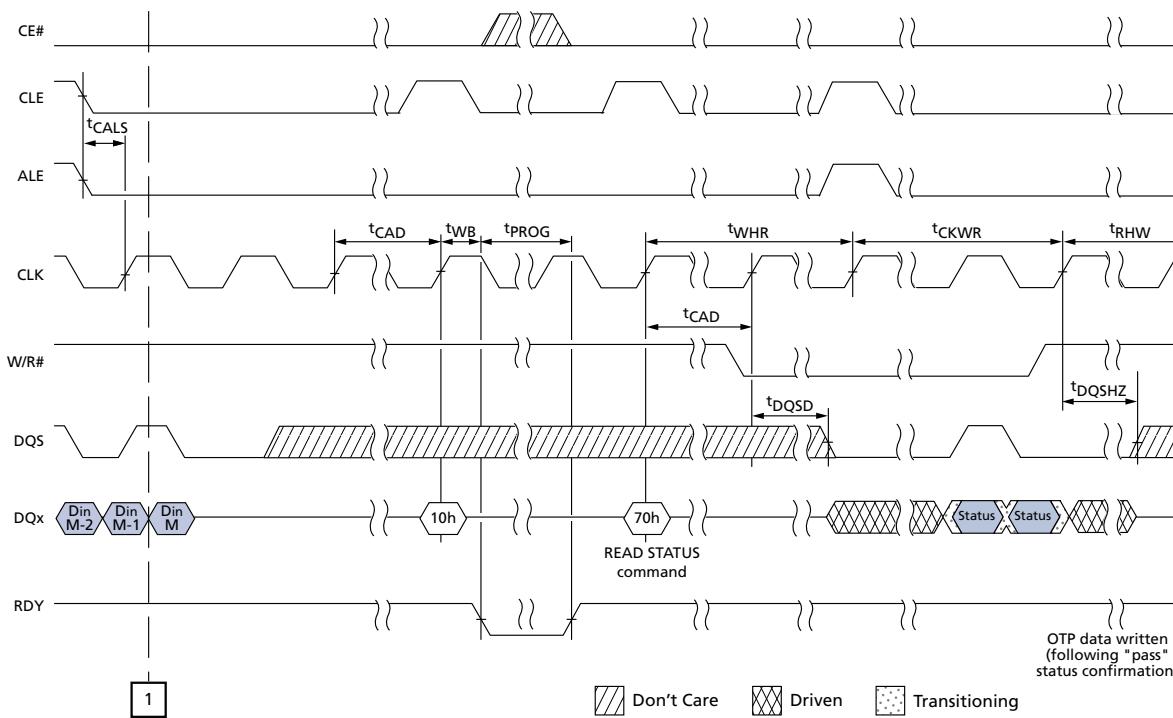
Note: 1. Programming timing figures do not represent single-pass programming format - to be updated.

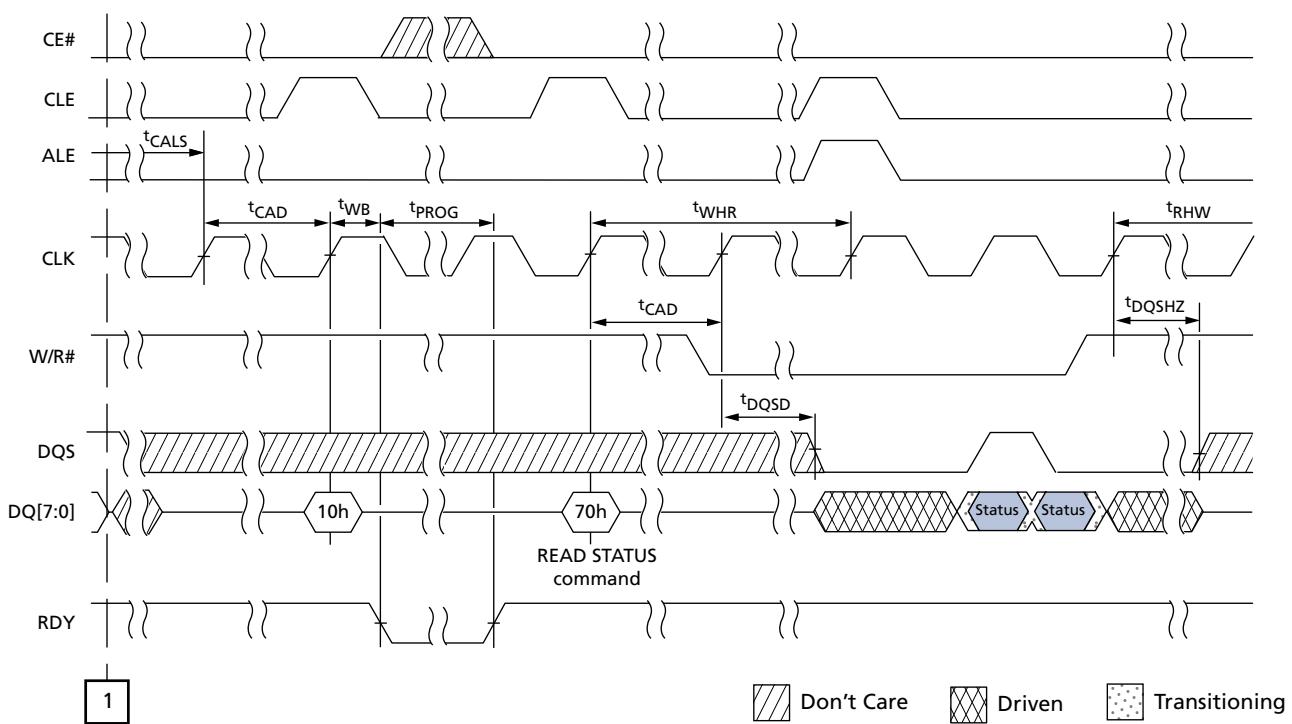
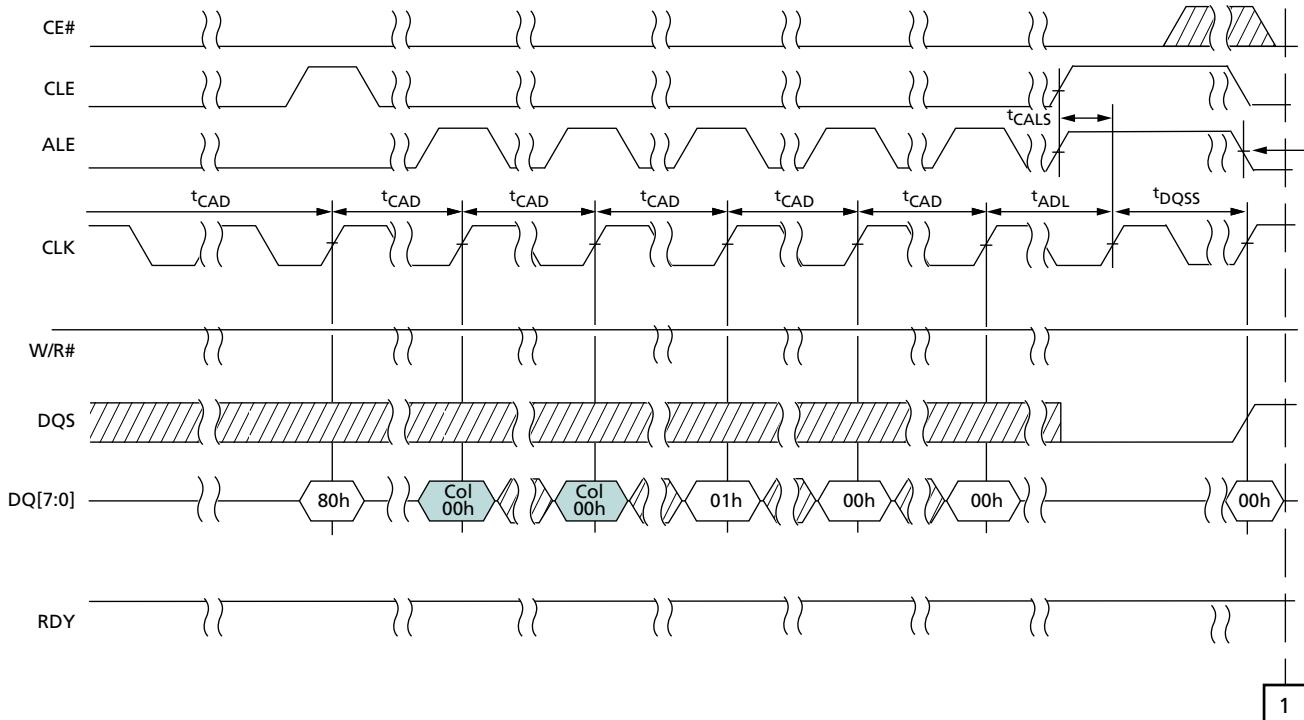


MLC 128Gb to 512Gb Async/Sync NAND NV-DDR Interface Timing Diagrams

Figure 136: READ OTP PAGE



**Figure 137: PROGRAM OTP PAGE (1 of 2)****Figure 138: PROGRAM OTP PAGE (2 of 2)**

**Figure 139: PROTECT OTP AREA**



NV-DDR2 Interface Timing Diagrams

Figure 140: SET FEATURES Operation

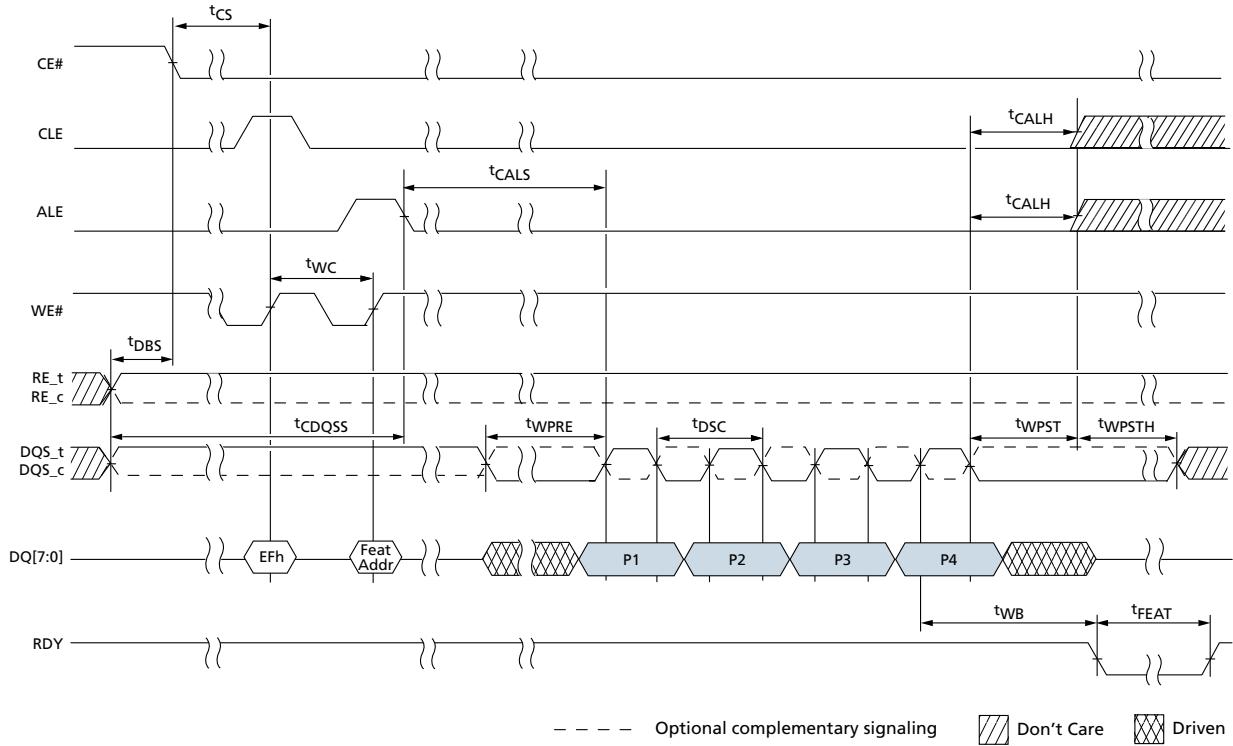
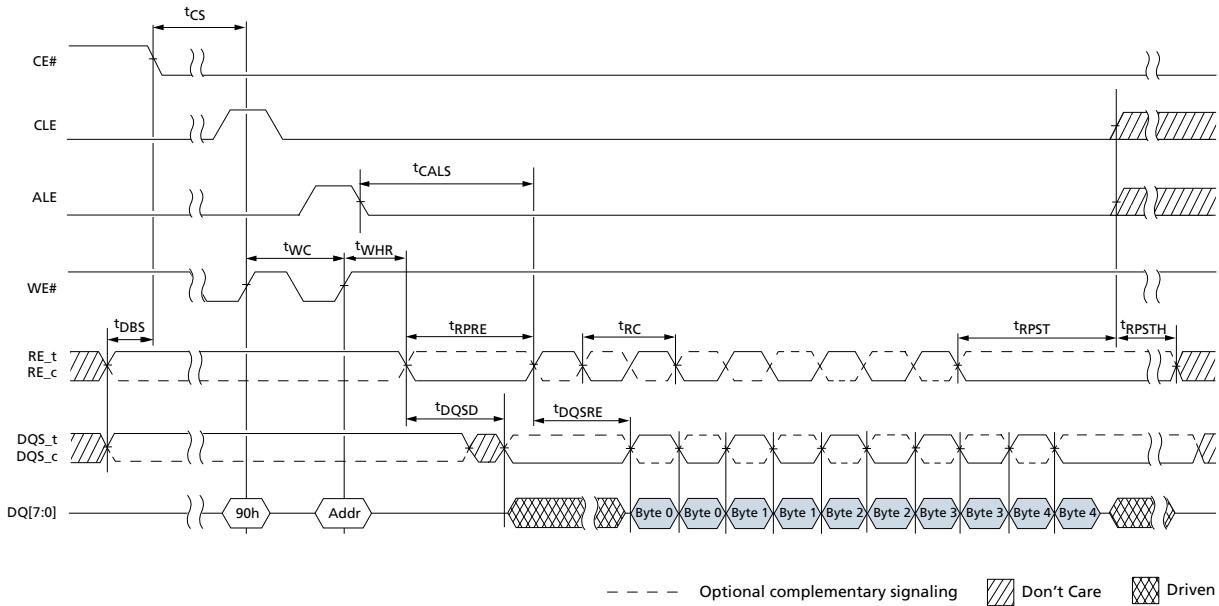


Figure 141: READ ID Operation



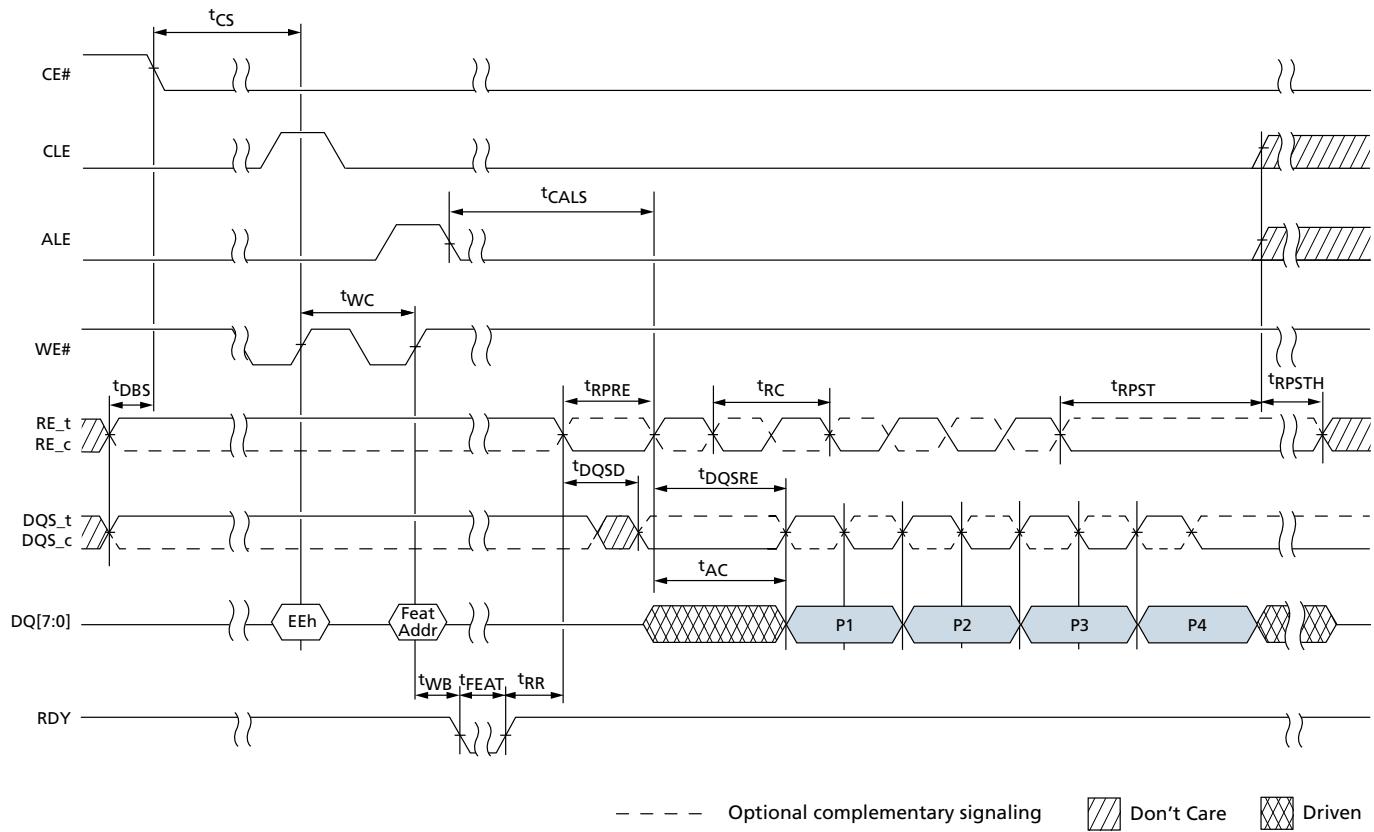
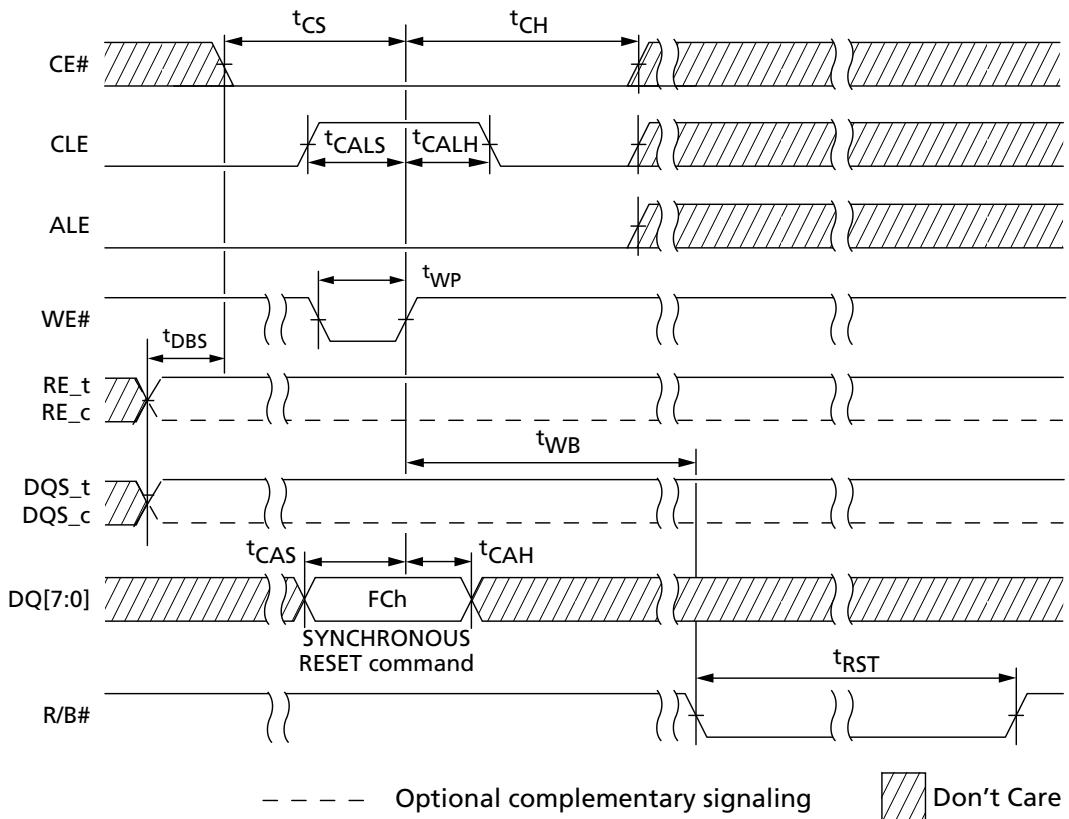
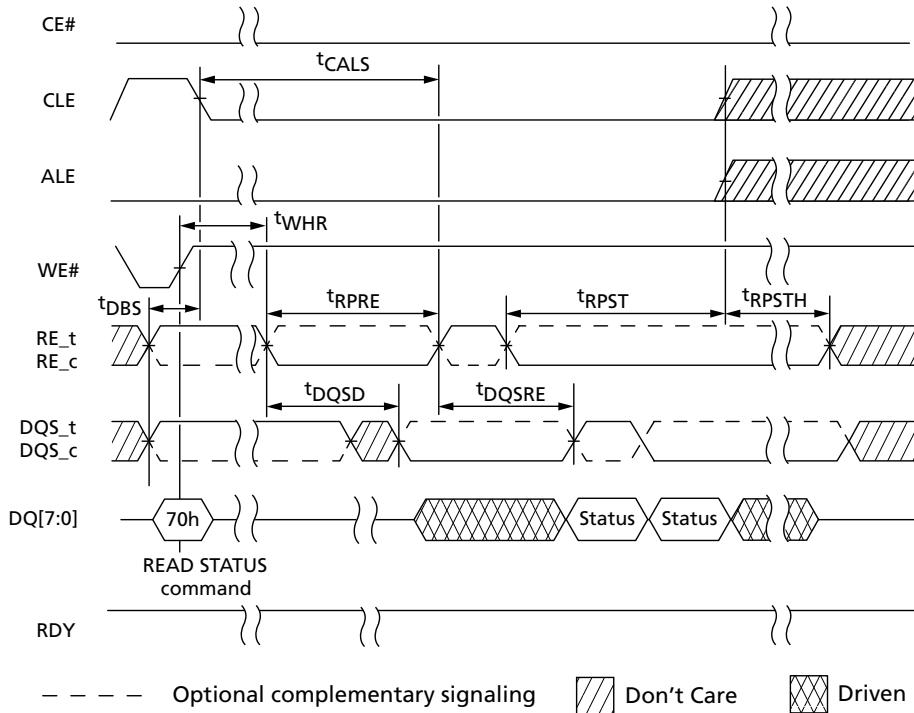
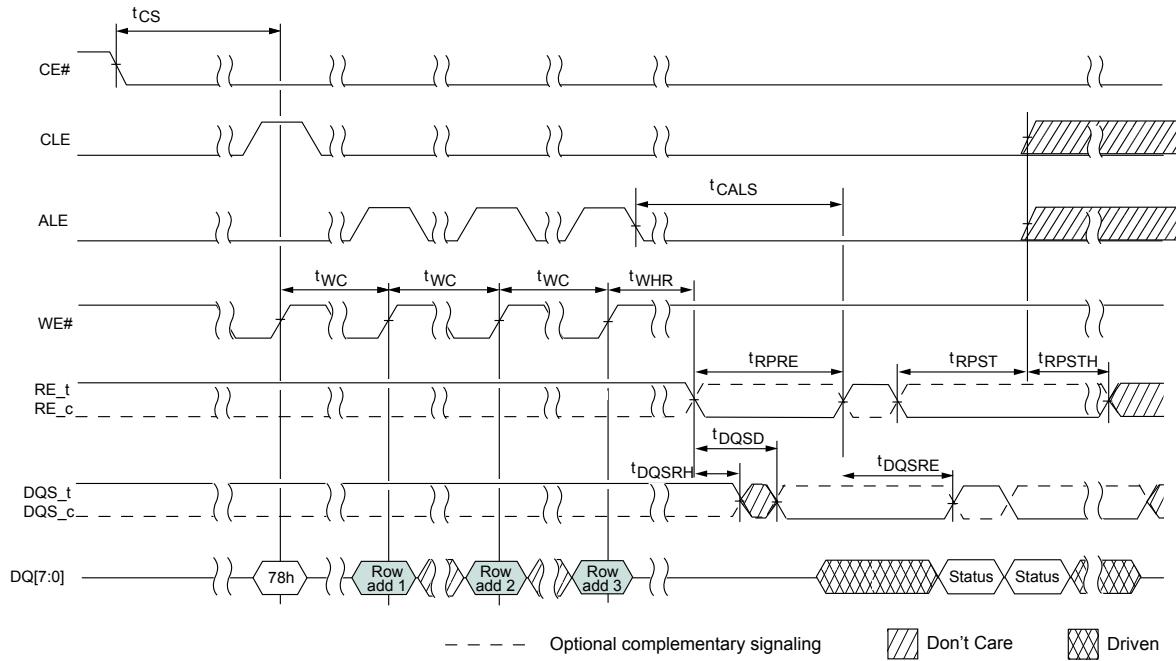
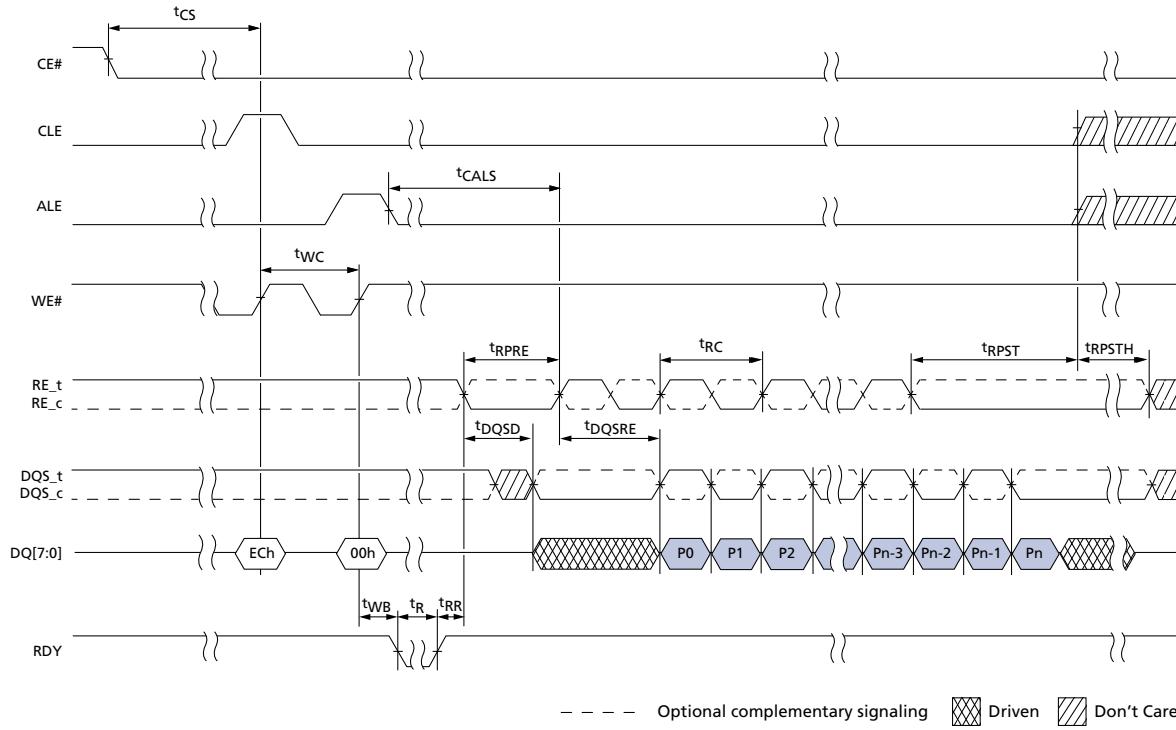
**Figure 142: GET FEATURES Operation**

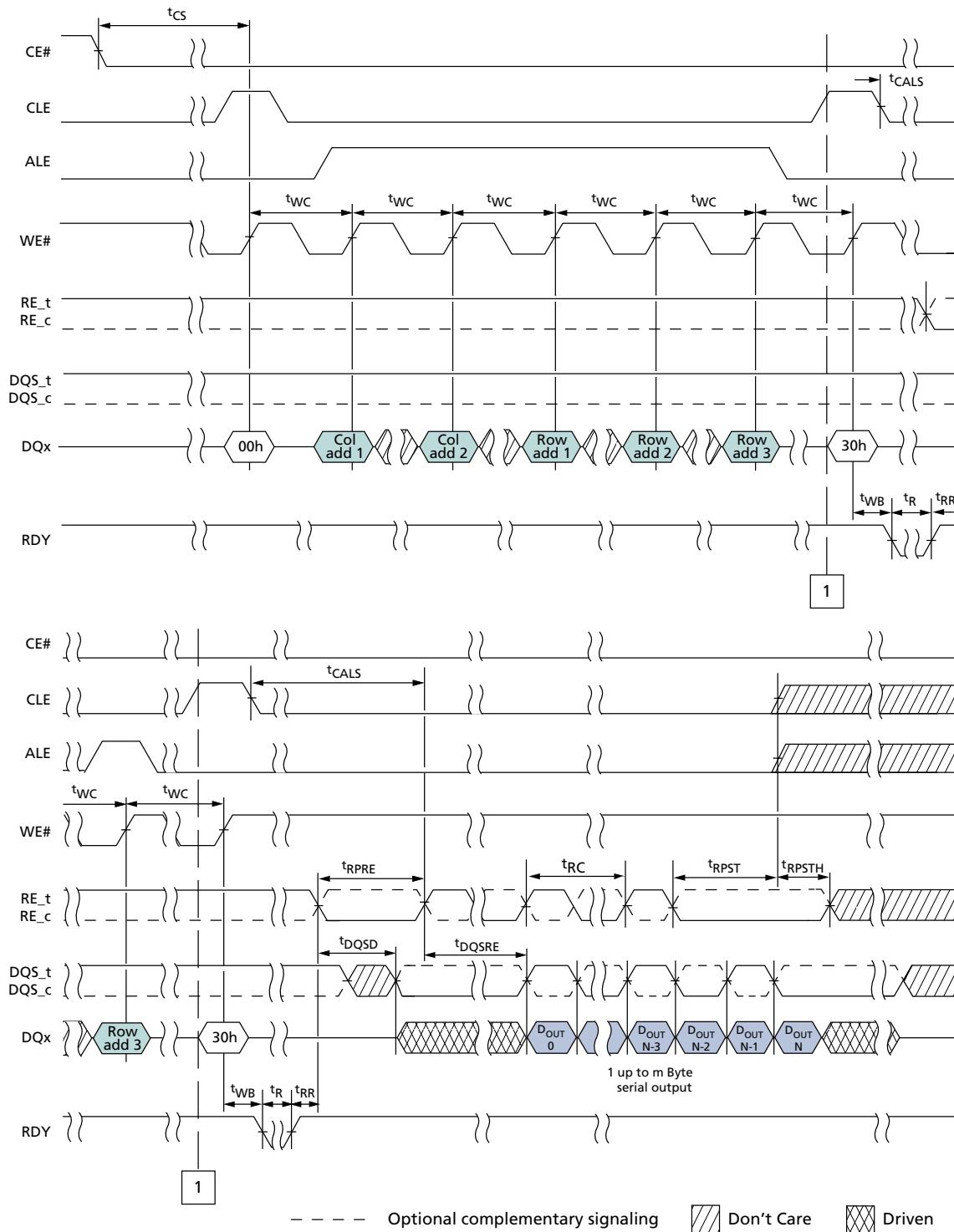


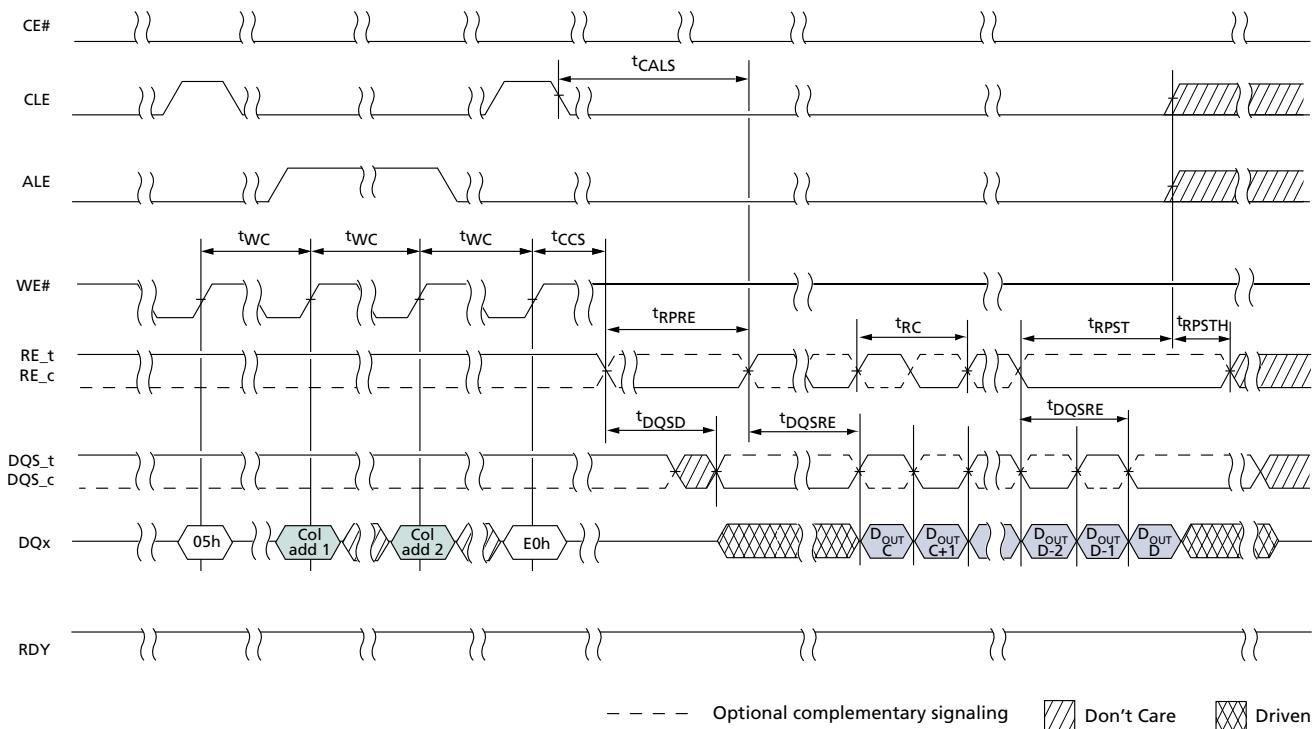
Figure 143: RESET (FCh) Operation

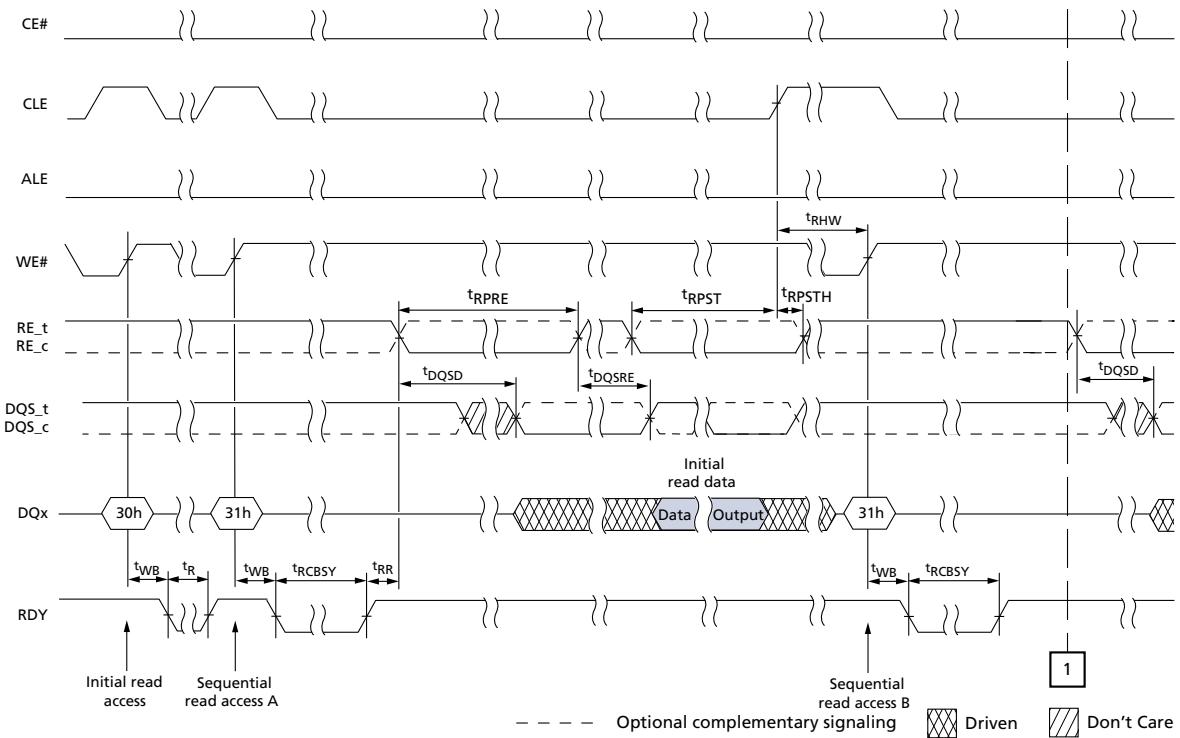
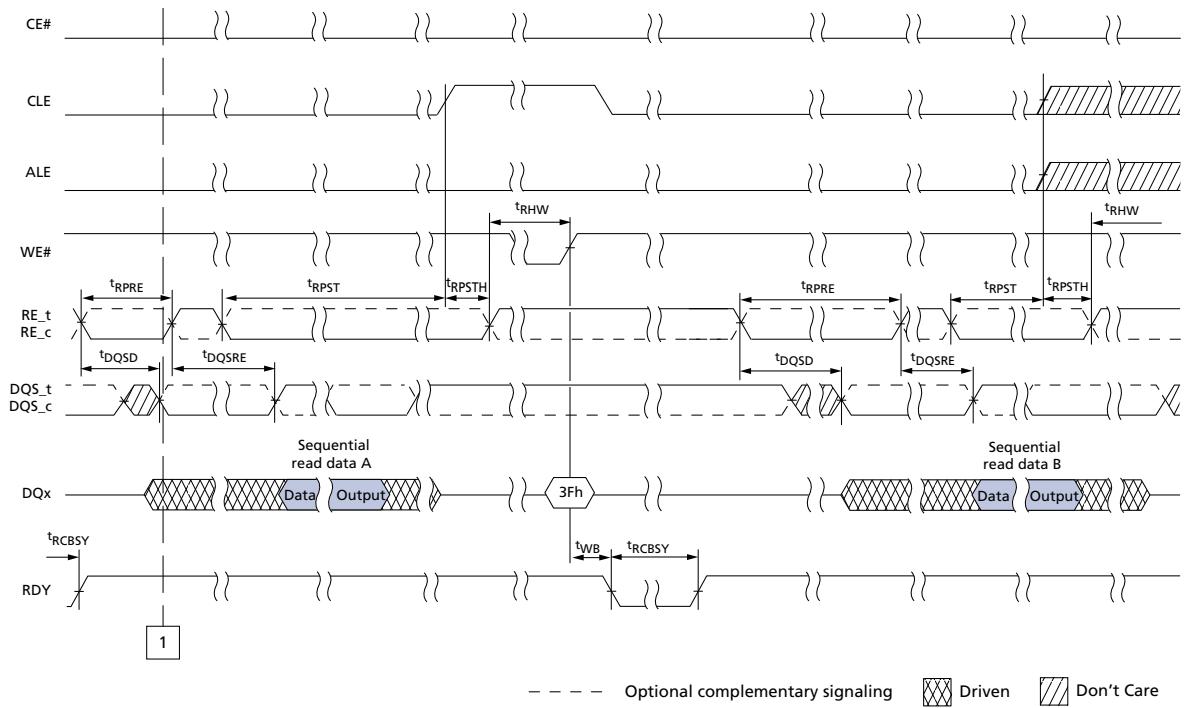


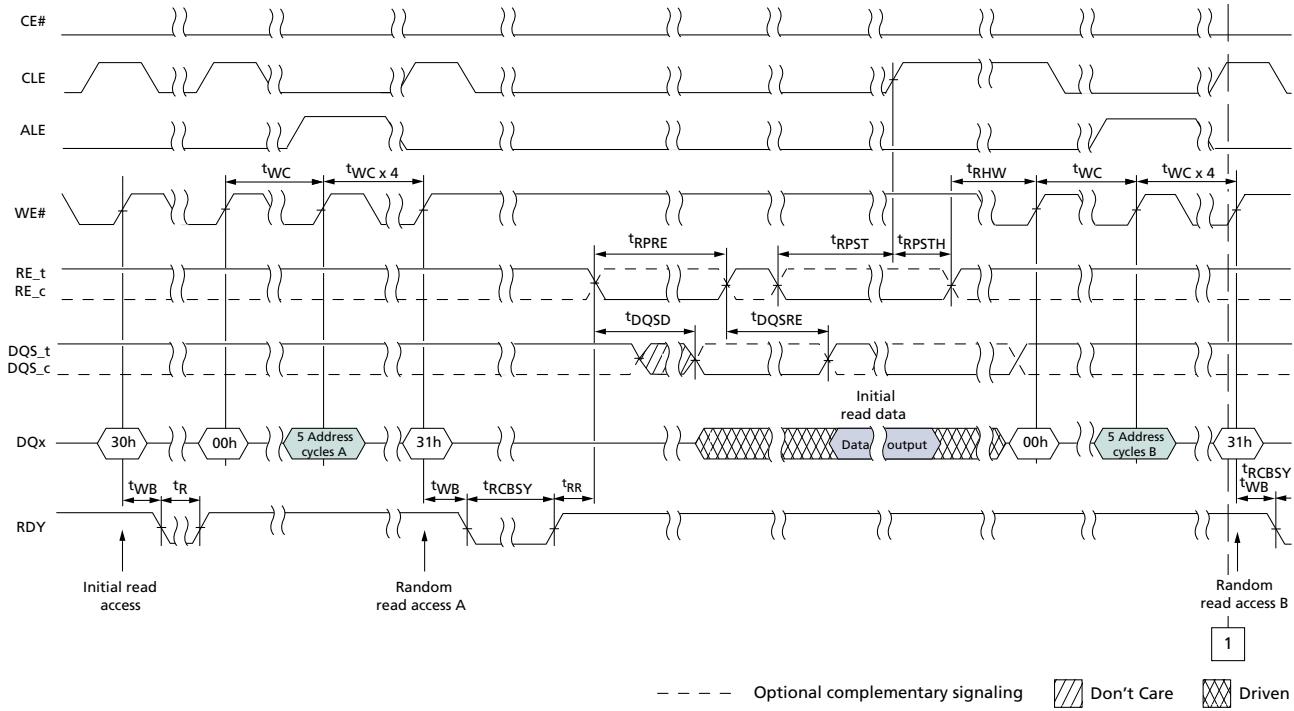
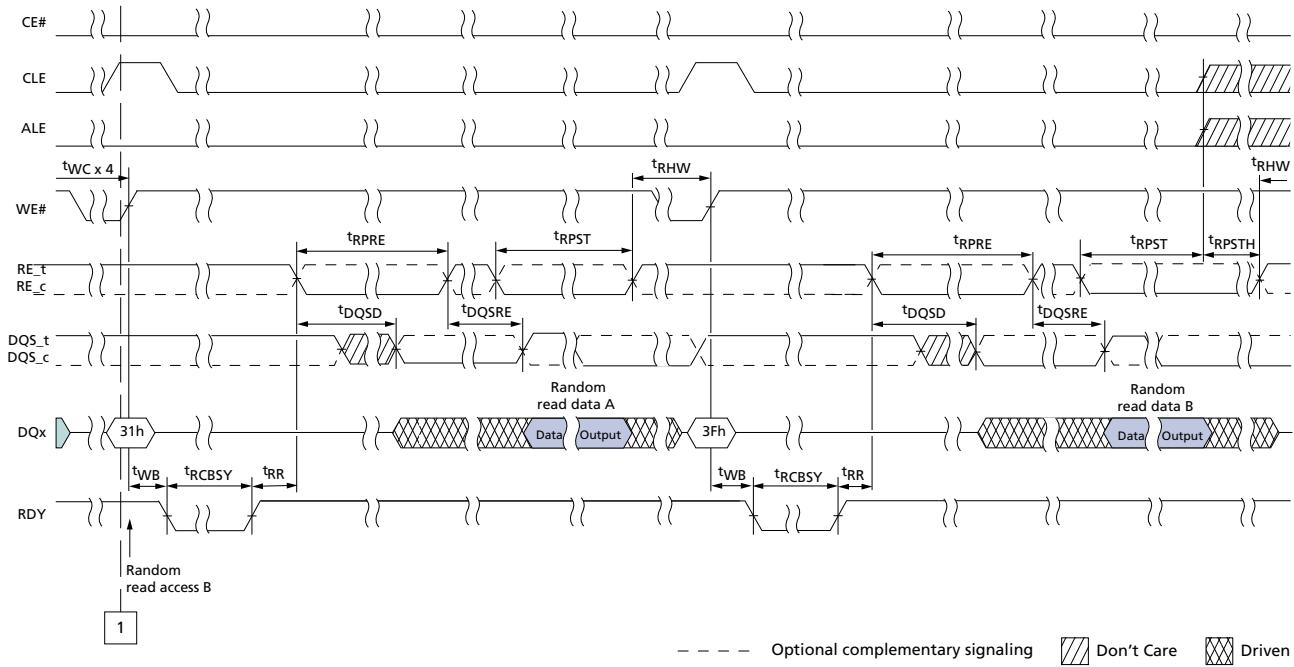
**Figure 144: READ STATUS Cycle**

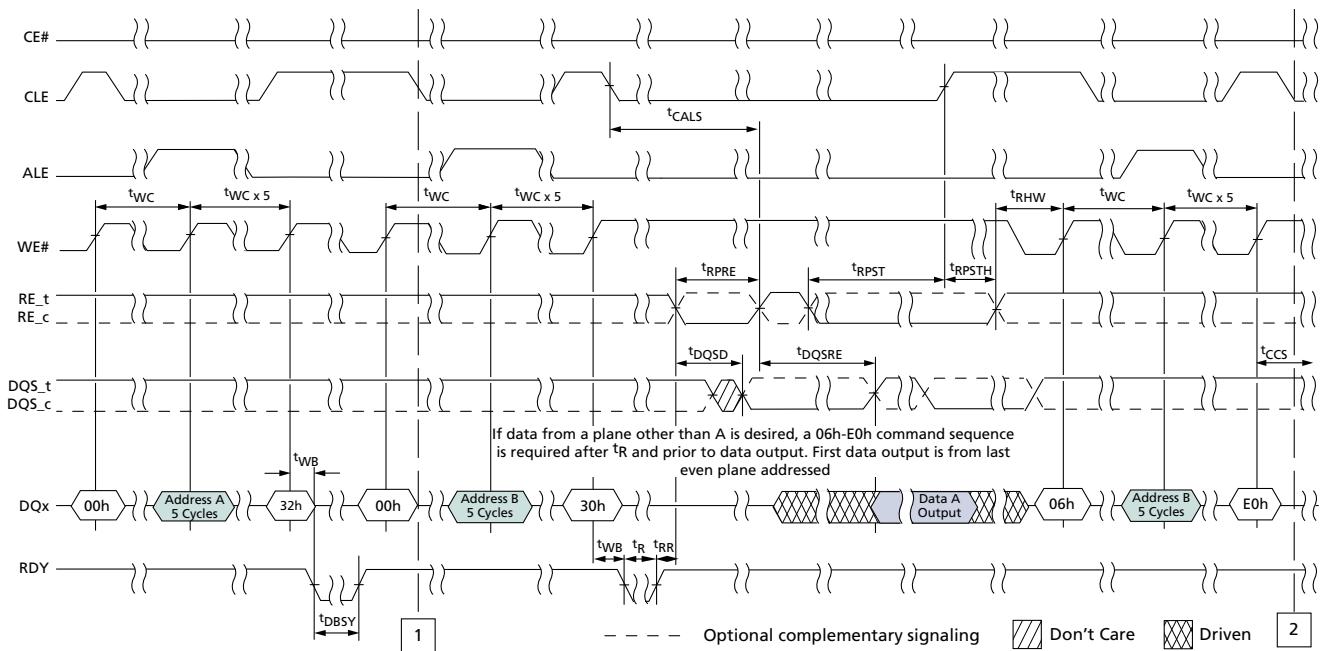
**Figure 145: READ STATUS ENHANCED Operation****Figure 146: READ PARAMETER PAGE Operation**

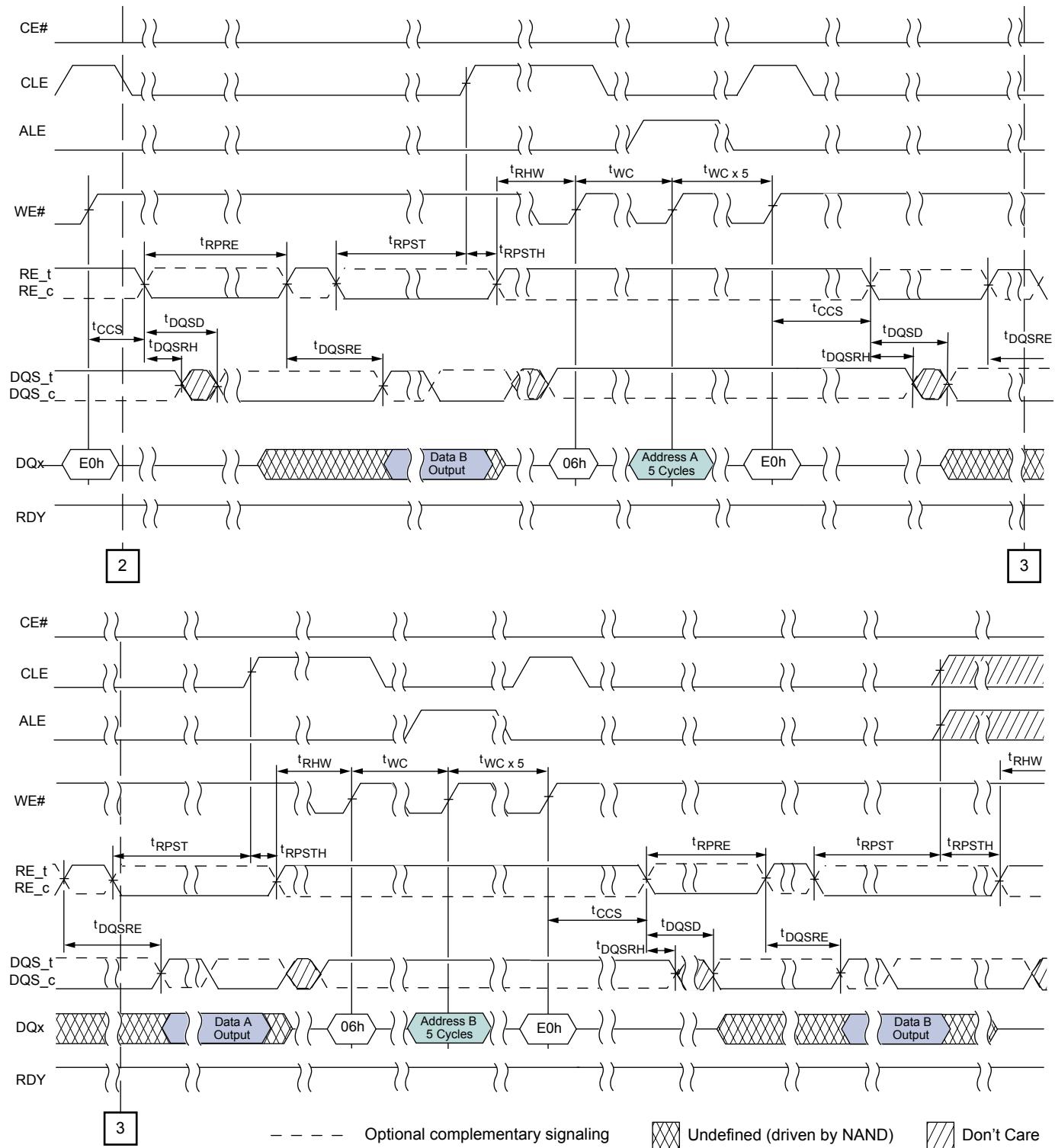
**Figure 147: READ PAGE Operation**

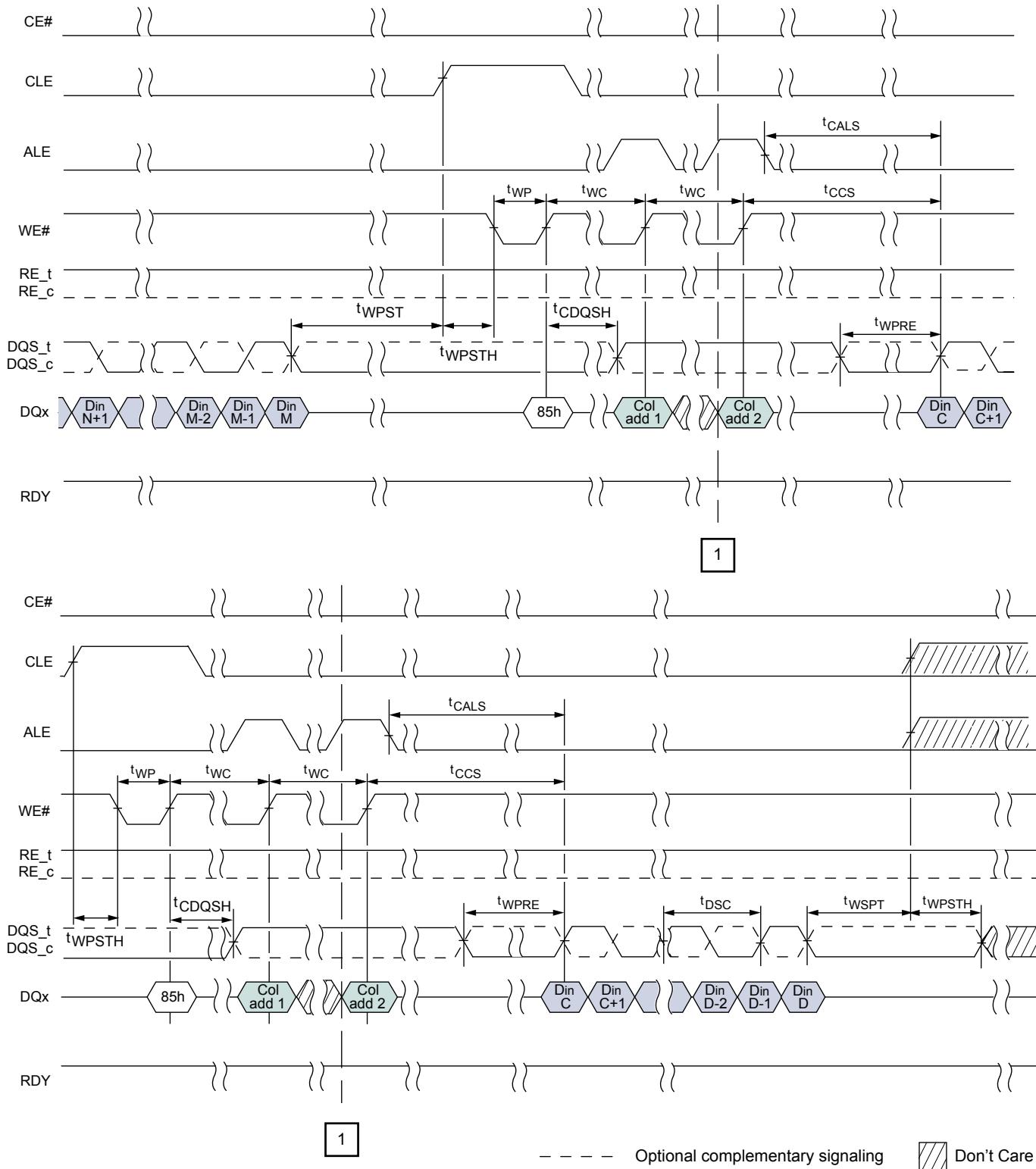
**Figure 148: CHANGE READ COLUMN**

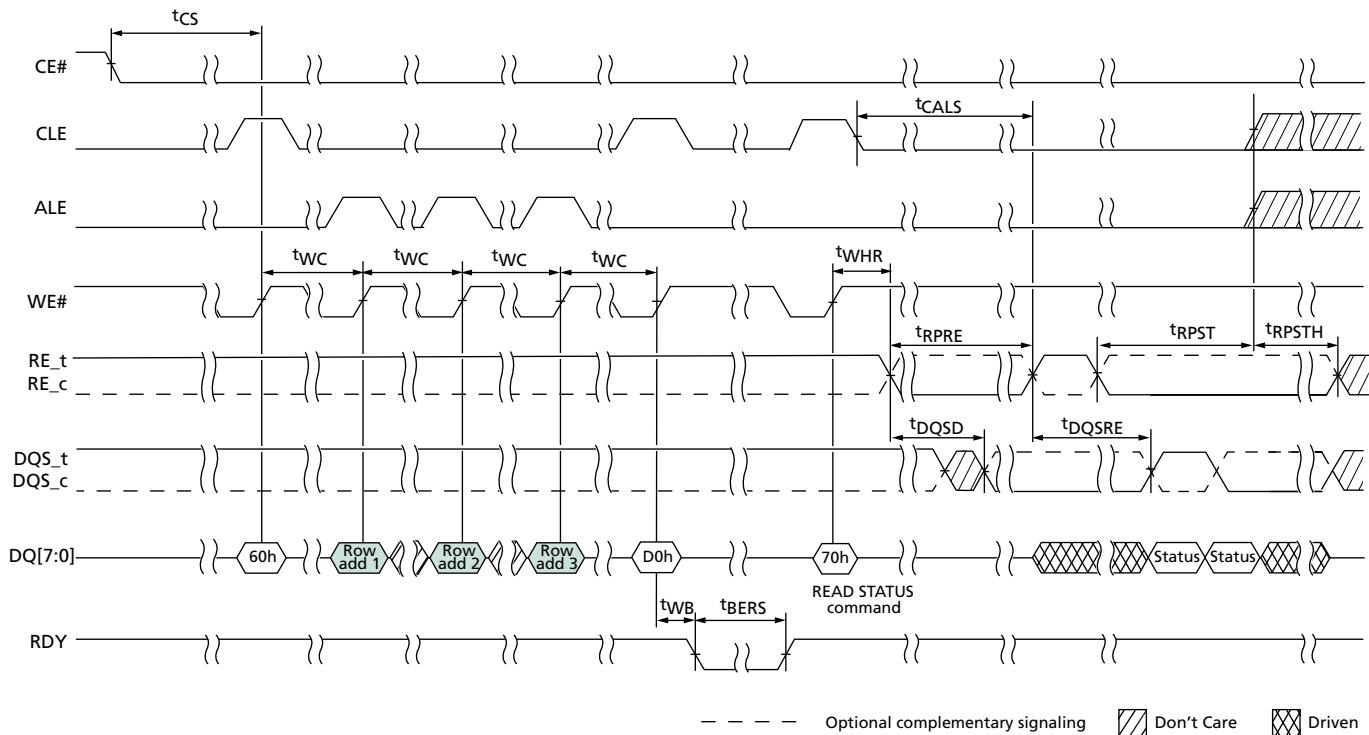
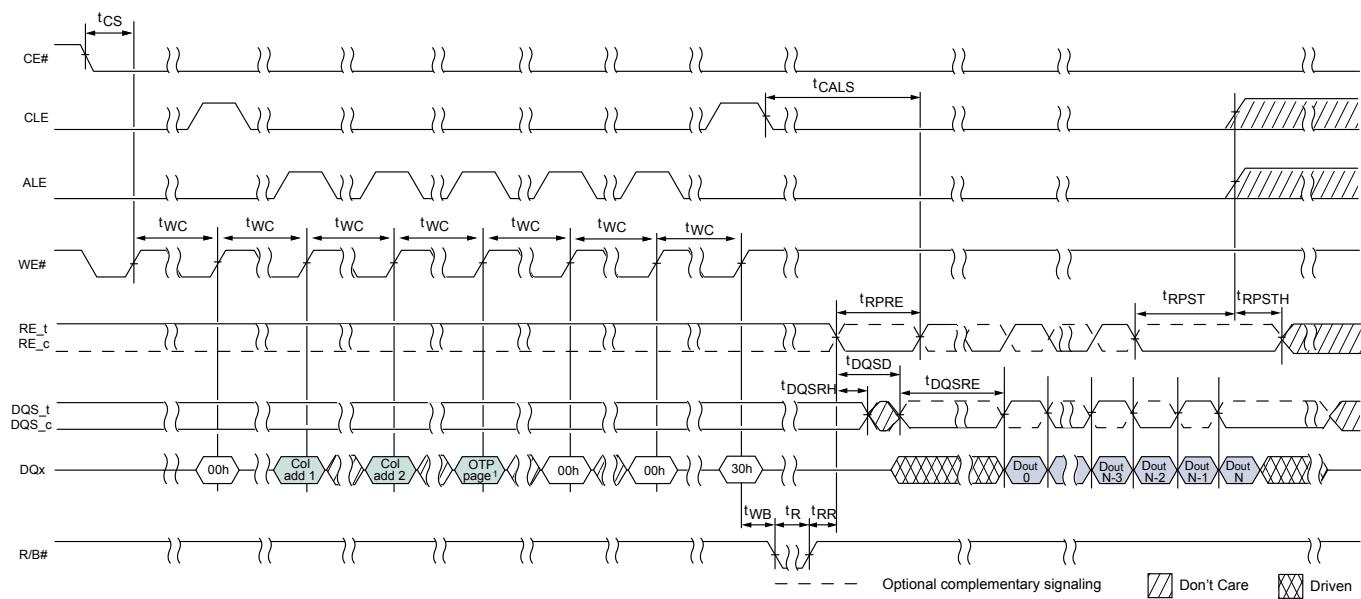
**Figure 149: READ PAGE CACHE SEQUENTIAL (1 of 2)****Figure 150: READ PAGE CACHE SEQUENTIAL (2 of 2)**

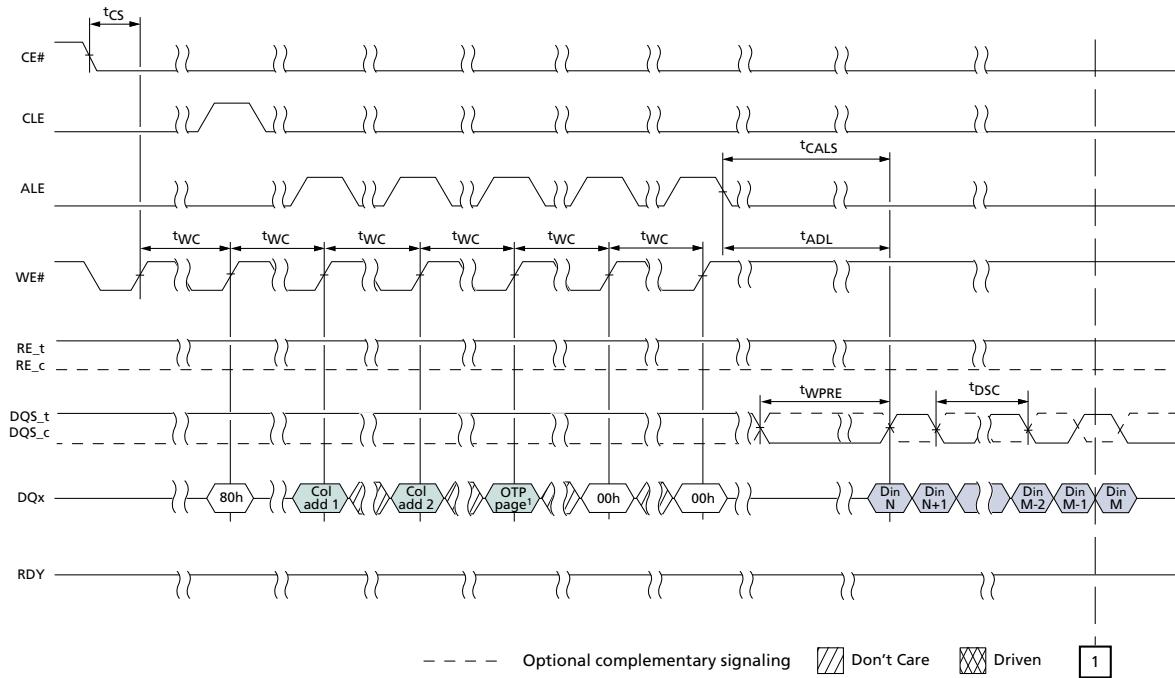
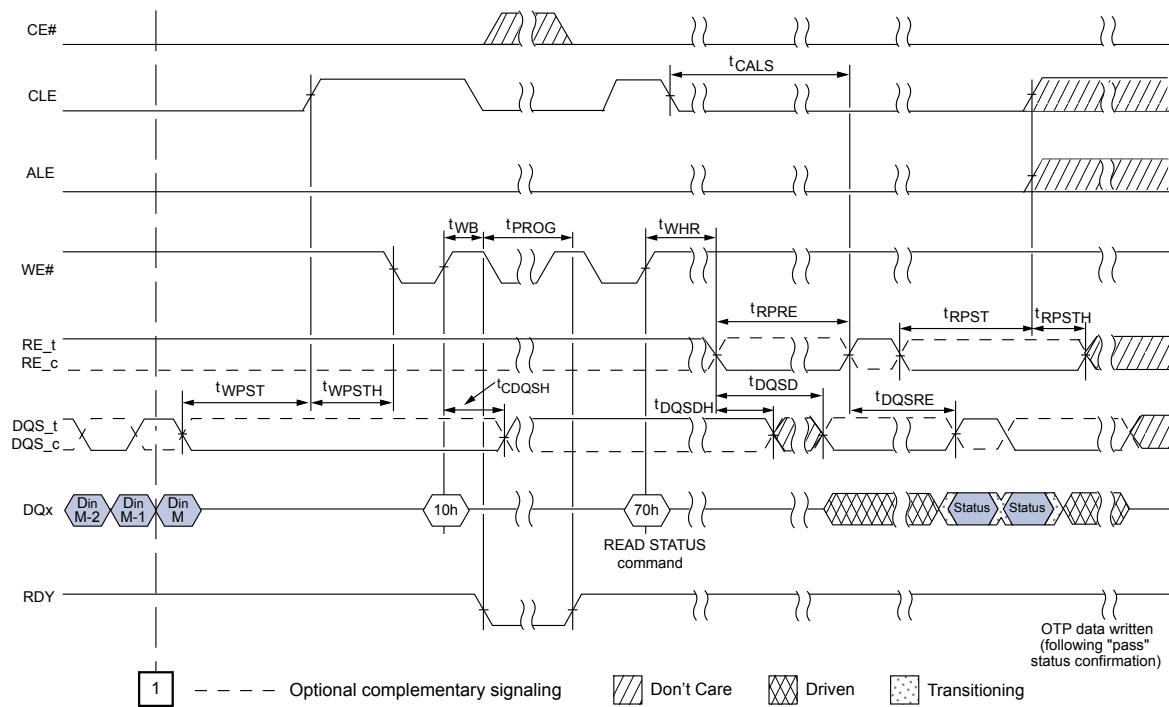
**Figure 151: READ PAGE CACHE RANDOM (1 of 2)****Figure 152: READ PAGE CACHE RANDOM (2 of 2)**

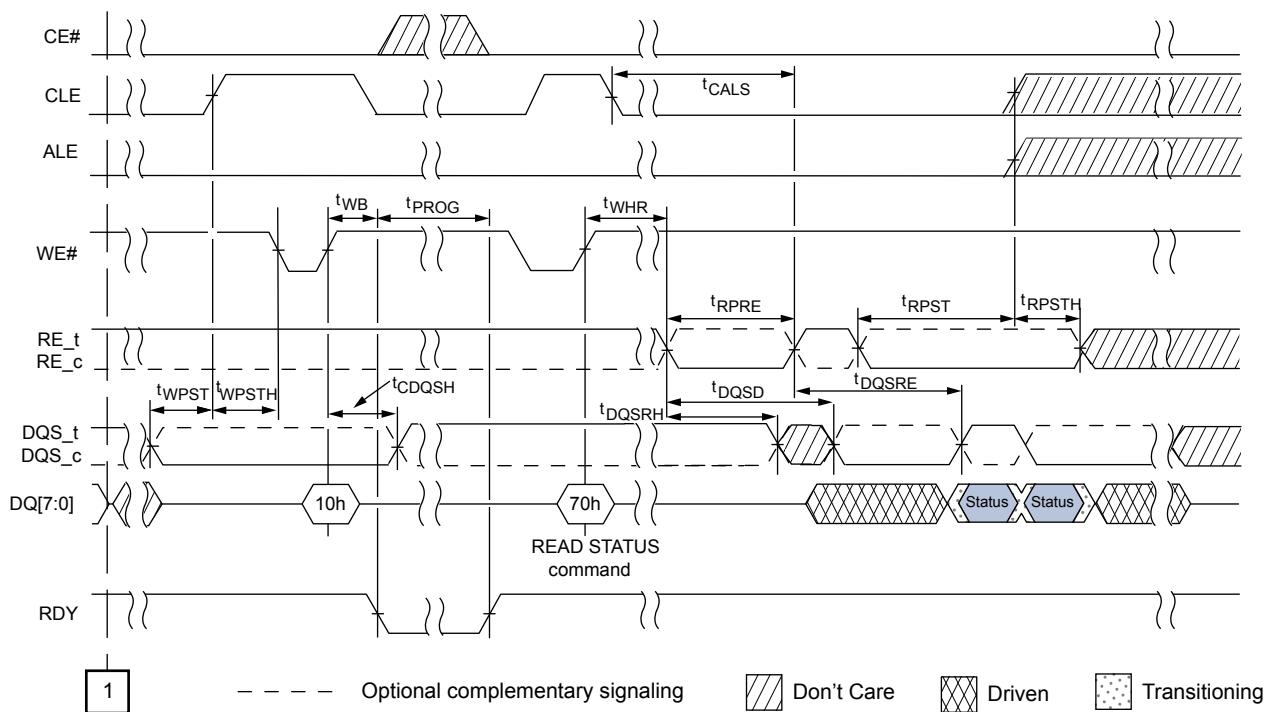
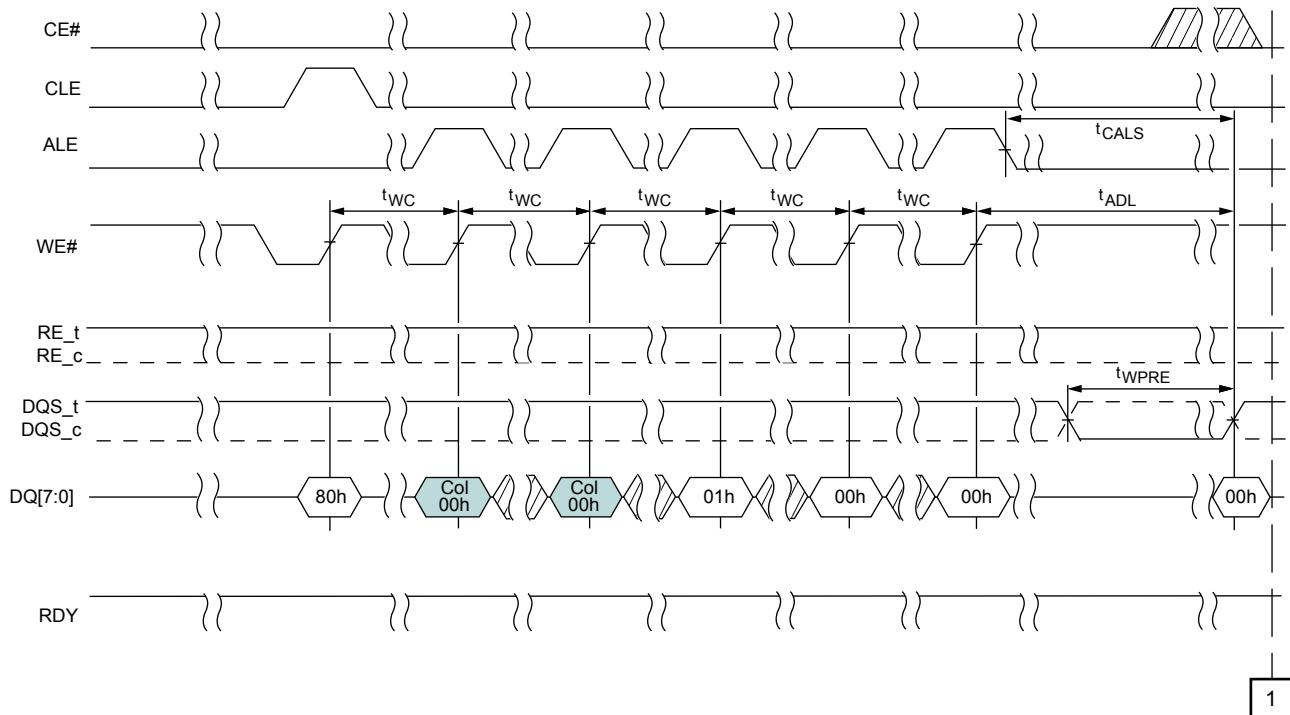
**Figure 153: Multi-Plane Read Page (1 of 2)**

**Figure 154: Multi-Plane Read Page (2 of 2)**

**Figure 155: CHANGE WRITE COLUMN**

**Figure 156: ERASE BLOCK****Figure 157: READ OTP PAGE**

**Figure 158: PROGRAM OTP PAGE (1 of 2)****Figure 159: PROGRAM OTP PAGE (2 of 2)**

**Figure 160: PROTECT OTP AREA**



Revision History

Rev. A - 12/17

- Initial release

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