ICM-20618 Datasheet
Revision 1.0

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1 Document Information

1.1 Revision History

Revision Date	Revision	Description
12/02/2015	1.0	Initial Release

1.2 Purpose and Scope

This document is a preliminary product specification, providing a description, specifications, and design related information on the ICM-20618 MotionTracking device.

Specifications are subject to change without notice. Final specifications will be updated based upon characterization of production silicon. For references to register map and descriptions of individual registers, please refer to the ICM-20618 Register Map and Register Descriptions document.

1.3 Product Overview

The ICM-20618 is a MotionTracking device that combines a 3-axis gyroscope, 3-axis accelerometer, and a Digital Motion Processor™ (DMP) all in a small 3x3x0.75mm QFN package. The device supports the following features:

- FIFO of size 512 bytes (FIFO size will vary depending on DMP feature-set)
- Runtime Calibration

ICM-20618 devices, with their 6-axis integration, on-chip DMP, and run-time calibration firmware, enable manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope has a programmable full-scale range of ±250, ±500, ±1000, and ±2000 degrees/sec. The accelerometer has a user-programmable accelerometer full-scale range of ±2*g*, ±4*g*, ±8*g*, and ±16*g*. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other key features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I^2C and SPI serial interfaces, a VDD operating range of 1.71 to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

Communication with all registers of the device is performed using I^2C at up to 100kHz (standard-mode) or up to 400kHz (fast-mode), or SPI at up to 2MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 3x3x0.75mm (24-pin QFN), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 10,000*g* shock reliability.

2 Features

2.1 Gyroscope Features

The triple-axis MEMS gyroscope in the ICM-20618 includes the following features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±250, ±500, ±1000, and ±2000°/sec and integrated 16-bit ADCs
- User-selectable ODR; User-selectable low pass filters
- Self-test

2.2 Accelerometer Features

The triple-axis MEMS accelerometer in ICM-20618 includes the following features:

- Digital-output X-, Y-, and Z-axis accelerometer with a programmable full scale range of ±2*g*, ±4*g*, ±8*g* and ±16*g* and integrated 16-bit ADCs
- User-selectable ODR; User-selectable low pass filters
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 DMP Features

The DMP in ICM-20618 includes the following capabilities:

- Offloads computation of motion processing algorithms from the host processor. The DMP can be used to minimize power, simplify timing, simplify the software architecture, and save valuable MIPS on the host processor for use in applications.
- The DMP enables ultra-low power run-time and background calibration of the accelerometer, gyroscope, and compass, maintaining optimal performance of the sensor data for both physical and virtual sensors generated through sensor fusion. This enables the best user experience for all sensor enabled applications for the lifetime of the device.
- DMP features simplify the software architecture resulting in a more robust overall solution.
- DMP features are OS, Platform, and Architecture independent, supporting virtually any AP, MCU, or other embedded architecture.

2.4 Additional Features

The ICM-20618 includes the following additional features:

- I^2C at up to 100kHz (standard-mode) or up to 400kHz (fast-mode) or SPI at up to 2MHz for communication with registers
- Auxiliary master I^2C bus for reading data from external sensors (e.g. magnetometer)
- Digital-output temperature sensor
- 10,000 *g* shock tolerant
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 Electrical Characteristics

3.1 Gyroscope Specifications

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Note: All specifications apply to Standard (Duty-Cycled) Mode and Low-Noise Mode, unless noted otherwise

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	GYRO_FS_SEL=0		±250		º/s	1
	GYRO_FS_SEL=1		±500		º/s	1
	GYRO_FS_SEL=2		±1000		º/s	1
	GYRO_FS_SEL=3		±2000		º/s	1
Gyroscope ADC Word Length			16		bits	1
Sensitivity Scale Factor	GYRO_FS_SEL=0		131		LSB/(º/s)	1
	GYRO_FS_SEL=1		65.5		LSB/(º/s)	1
	GYRO_FS_SEL=2		32.8		LSB/(º/s)	1
	GYRO_FS_SEL=3		16.4		LSB/(º/s)	1
Sensitivity Scale Factor Tolerance	25°C	-3		+3	%	2
Sensitivity Scale Factor Variation Over Temperature	-40°C to +85°C		±4		%	2
Nonlinearity	Best fit straight line; 25°C		±0.2		%	2, 3
Cross-Axis Sensitivity			±2		%	2, 3
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C	-20		+20	º/s	2
ZRO Variation Over Temperature	-40°C to +85°C	-0.24		+0.24	º/s/°C	2
GYROSCOPE NOISE PERFORMANCE (GYRO_FS_SEL=0)						
Total RMS Noise	GYRO_DLPFCFG=2 (Noise Bandwidth = 154Hz) Calculated from Noise Spectral Density		0.25		º/s-rms	2, 3
Noise Spectral Density	Based on Noise Bandwidth = 10Hz		0.02		º/s/√Hz	2
GYROSCOPE MECHANICAL FREQUENCIES		25	27	29	kHz	2
LOW PASS FILTER RESPONSE	Programmable Range	5.7		197	Hz	1, 3
GYROSCOPE START-UP TIME	From Full-Chip Sleep mode		35		ms	2, 3
OUTPUT DATA RATE	Low power (duty-cycled)	4.4		562.5	Hz	1
	Programmable, Normal (Filtered) mode GYRO_FCHOICE=1; GYRO_DLPFCFG=x	4.4		1.125k	Hz	
	GYRO_FCHOICE=0; GYRO_DLPFCFG=x			9k	Hz	

Table 1 Gyroscope Specifications

Notes:

1. Guaranteed by design
2. Derived from validation or characterization of parts, not guaranteed in production
3. Low-noise mode specification

3.2 Accelerometer Specifications

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Note: All specifications apply to Standard (Duty-Cycled) Mode and Low-Noise Mode, unless noted otherwise

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY						
Full-Scale Range	ACCEL_FS=0		±2		*g*	1
	ACCEL_FS=1		±4		*g*	1
	ACCEL_FS=2		±8		*g*	1
	ACCEL_FS=3		±16		*g*	1
ADC Word Length	Output in two's complement format		16		bits	1
Sensitivity Scale Factor	ACCEL_FS=0		16,384		LSB/*g*	1
	ACCEL_FS=1		8,192		LSB/*g*	1
	ACCEL_FS=2		4,096		LSB/*g*	1
	ACCEL_FS=3		2,048		LSB/*g*	1
Initial Tolerance	Component-level	-3.25		3.25	%	2
Sensitivity Change vs. Temperature	-40°C to +85°C ACCEL_FS=0 Component-level		±3		%	2
Nonlinearity	Best Fit Straight Line		±0.5		%	2, 3
Cross-Axis Sensitivity			±2		%	2, 3
ZERO-G OUTPUT						
Initial Tolerance	Component-level, X and Y axes		±80		m*g*	2
	Component-level, Z axis		±100		m*g*	2
	Board-level, X and Y axes		±120		m*g*	2
	Board-level, Z axis		±180		m*g*	2
Zero-G Level Change vs. Temperature	-40°C to +85°C, X and Y axes		±0.64		m*g*/°C	2
	-40°C to +85°C, Z axis		±2		m*g*/°C	2
ACCELEROMETER NOISE PERFORMANCE						
Total RMS Noise	ACCEL_DLPFCFG=2 (Noise Bandwidth = 136Hz) Calculated from Noise Spectral Density		3.5		m*g*-rms	2, 3
Noise Spectral Density	Based on Noise Bandwidth = 10Hz		300		µ*g*/√Hz	2
LOW PASS FILTER RESPONSE	Programmable Range	5.7		246	Hz	1, 3
INTELLIGENCE FUNCTION INCREMENT			32		m*g*/LSB	
ACCELEROMETER STARTUP TIME	From Sleep mode			0.75	ms	2, 3
	From Cold Start, 1ms V_{DD} ramp			30	ms	2, 3
OUTPUT DATA RATE	Low power (duty-cycled)	0.27		563	Hz	1
	Low noise (active) ACCEL_FCHOICE=1; ACCEL_DLPFCFG=x	4.5		1.125k	Hz	1
	ACCEL_FCHOICE=0; ACCEL_DLPFCFG=x			4.5k	Hz	1

Table 2 Accelerometer Specifications

Notes:

1. Guaranteed by design
2. Derived from validation or characterization of parts, not guaranteed in production
3. Low-noise mode specification

3.3 Electrical Specifications

4.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	Units	Notes
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.6	V	1
VDDIO		1.71	1.8	3.6	V	1
SUPPLY CURRENTS						
Gyroscope Only (DMP & Accelerometer disabled)	102.3Hz update rate, 1x averaging filter		1.29		mA	2, 3
Accelerometer Only (DMP & Gyroscope disabled)	102.3Hz update rate, 1x averaging filter		252		µA	2, 3
Gyroscope + Accelerometer (DMP disabled)	102.3Hz update rate, 1x averaging filter		1.33		mA	2, 3
Full-Chip Sleep Mode			8		µA	2
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 3 D.C. Electrical Characteristics

Notes:

1. Guaranteed by design
2. Derived from validation or characterization of parts, not guaranteed in production
3. The 102.3Hz ODR value shown here is an example, please see the Register Map for the full list of ODRs supported and corresponding current values

4.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameter	Conditions	MIN	TYP	MAX	Units	NOTES
SUPPLIES						
Supply Ramp Time	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.1		100	ms	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
Sensitivity	Untrimmed		333.87		LSB/°C	
Room Temp Offset	21°C		0		LSB	
Power-On RESET						
Supply Ramp Time (T_{RAMP})	Valid power-on RESET	0.01	20	100	ms	1
Start-up time for register read/write	From power-up		11	100	ms	1
I²C ADDRESS	AD0 = 0 AD0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, AD0, SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1MΩ;			0.1*VDDIO	V	
$V_{OL.INT1}$, INT Low-Level Output Voltage	OPEN=1, 0.3mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	LATCH_INT_EN=0		50		µs	
I2C I/O (SCL, SDA)						
V_{IL}, LOW Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL}=0.4V V_{OL}=0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		250	ns	
AUXILLIARY I/O (AUX_CL, AUX_DA)						
V_{IL}, LOW-Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7* VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1* VDDIO		V	
V_{OL1}, LOW-Level Output Voltage	VDDIO > 2V; 1mA sink current	0		0.4	V	

Parameter	Conditions	MIN	TYP	MAX	Units	NOTES
V_{OL3}, LOW-Level Output Voltage	VDDIO < 2V; 1mA sink current	0		0.2* VDDIO	V	
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V V_{OL} = 0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pF	20+0.1C_b		250	ns	
INTERNAL CLOCK SOURCE						
Clock Frequency Initial Tolerance	Accelerometer Only Mode	-2		+2	%	1
	Gyroscope or 6-Axis Mode WITHOUT Timebase Correction	-9		+9	%	1
	Gyroscope or 6-Axis Mode WITH Timebase Correction	-1		+1		
Frequency Variation over Temperature	Accelerometer Only Mode	-10		+10	%	1
	Gyroscope or 6-Axis Mode		±1		%	1

Table 4 A.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

4.3 Other Electrical Specifications

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	Units	Notes
SERIAL INTERFACE						
SPI Operating Frequency, All Registers Read/Write	Low Speed Characterization		100 ±10%		kHz	
	High Speed Characterization		2 ±10%		MHz	
I^2C Operating Frequency	All registers, Fast-mode			400	kHz	
	All registers, Standard-mode			100	kHz	

Table 5 Other Electrical Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

3.4 I2C Timing Characterization

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency				400	kHz	
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	
t_{LOW}, SCL Low Period		1.3			µs	
t_{HIGH}, SCL High Period		0.6			µs	
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400pF	20+0.1C_b		300	ns	
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	
C_b, Capacitive Load for each Bus Line			< 400		pF	
$t_{VD.DAT}$, Data Valid Time				0.9	µs	
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	

Table 6 I²C Timing Characteristics

Notes:

1. Timing Characteristics apply to both Primary and Auxiliary I2C Bus
2. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

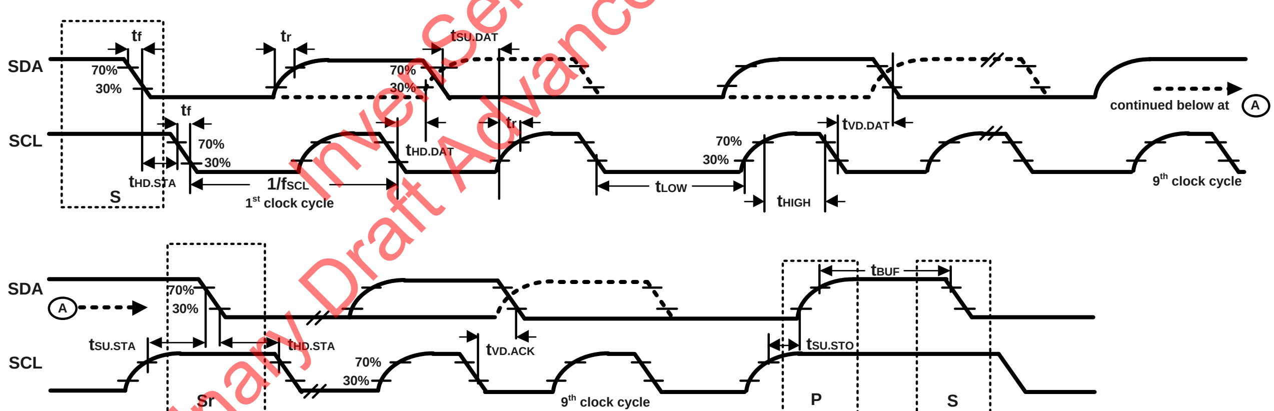


Figure 1 I2C Bus Timing Diagram

3.5 SPI Timing Characterization

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
SPI TIMING						
f_{SCLK}, SCLK Clock Frequency				2	MHz	1
t_{LOW}, SCLK Low Period		224			ns	1
t_{HIGH}, SCLK High Period		224			ns	1
$t_{SU.CS}$, CS Setup Time		8			ns	1
$t_{HD.CS}$, CS Hold Time		500			ns	1
$t_{SU.SDI}$, SDI Setup Time		5			ns	1
$t_{HD.SDI}$, SDI Hold Time		7			ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20pF			59	ns	1
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20pF	6			ns	1
$t_{DIS.SDO}$, SDO Output Disable Time				50	ns	1

Table 7 SPI Timing Characteristics

Notes:

3. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

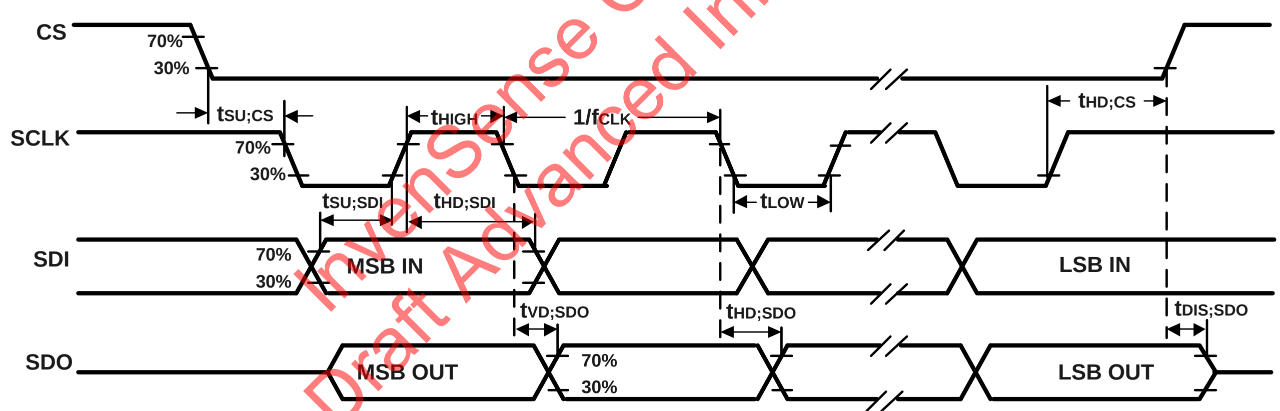


Figure 2 SPI Bus Timing Diagram

3.6 Absolute Maximum Ratings

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage, VDD	-0.5V to +4V
Supply Voltage, VDDIO	-0.5V to +4V
REGOUT	-0.5V to 2V
Input Voltage Level (AUX_DA, AD0, FSYNC, INT, SCL, SDA)	-0.5V to VDD + 0.5V
Acceleration (Any Axis, unpowered)	10,000g for 0.2ms
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2kV (HBM); 200V (MM)
Latch-up	JEDEC Class II (2),125°C ±100mA

Table 8 Absolute Maximum Ratings

4 Applications Information

4.1 Pin Out Diagram and Signal Description

Pin Number	Pin Name	Pin Description
7	AUX_CL	I^2C Master serial clock, for connecting to external sensors
8	VDDIO	Digital I/O supply voltage
9	AD0 / SDO	I^2C Slave Address LSB (AD0); SPI serial data output (SDO)
10	REGOUT	Regulator filter capacitor connection
11	FSYNC	Frame synchronization digital input. Connect to GND if unused.
12	INT	Interrupt digital output (totem pole or open-drain)
13	VDD	Power supply voltage
18	GND	Power supply ground
19	RESV	Reserved. Do not connect.
20	RESV	Reserved. Connect to GND.
21	AUX_DA	I^2C master serial data, for connecting to external sensors
22	nCS	Chip select (SPI mode only)
23	SCL / SCLK	I^2C serial clock (SCL); SPI serial clock (SCLK)
24	SDA / SDI	I^2C serial data (SDA); SPI serial data input (SDI)
1 – 6, 14 - 17	NC	No Connect pins. Do not connect.

Table 9 Signal Descriptions

Note: Power up with SCL/SCLK and nCS pins held low is not a supported use case. In case this power up approach is used, software reset is required using the PWR_MGMT_1 register, prior to initialization.

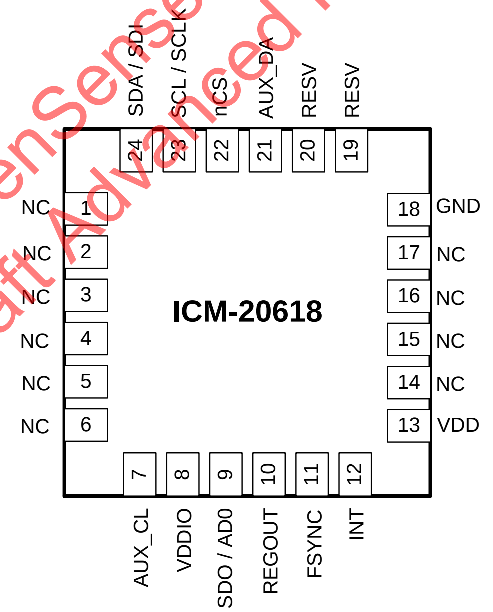


Figure 3 Pin out Diagram for ICM-20618 3x3x0.75mm QFN

4.2 Typical Operating Circuit

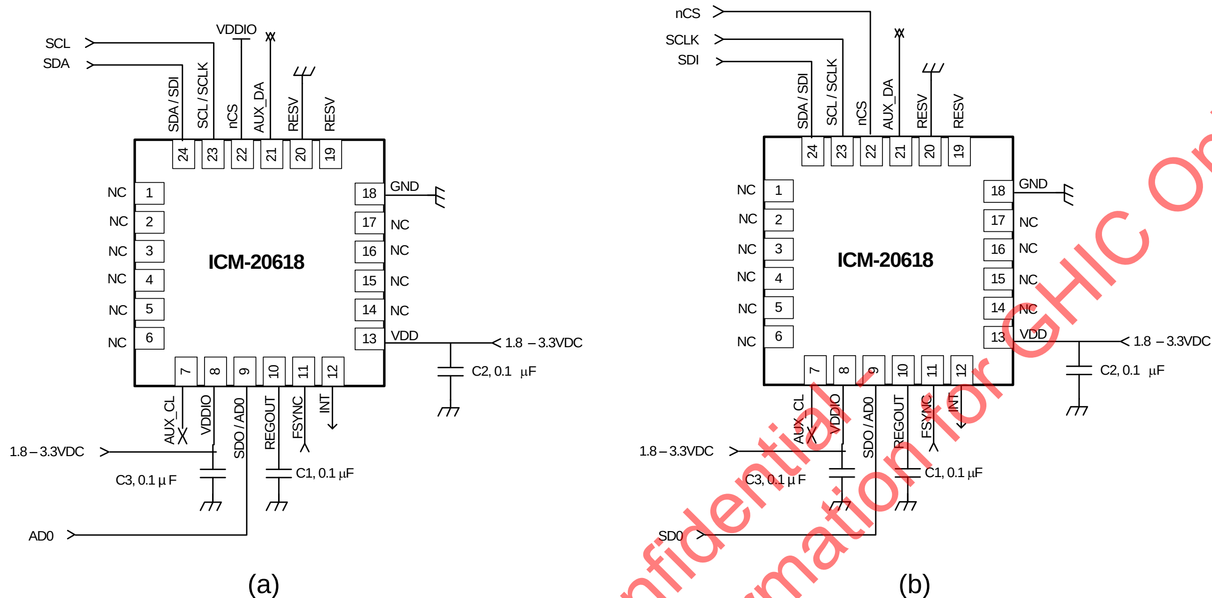


Figure 4 ICM-20618 Application Schematic. (a) I2C operation, (b) SPI operation.

Note: I2C lines are open drain and pullup resistors (e.g. 10kΩ) are required.

4.3 Bill of Materials for External Components

Component	Label	Specification	Quantity
Regulator Filter Capacitor	C1	X7R, 0.1µF ±10%	1
VDD Bypass Capacitor	C2	X7R, 0.1µF ±10%	1
VDDIO Bypass Capacitor	C3	X7R, 0.1µF ±10%	1

Table 10 Bill of Materials

4.4 Exposed Die Pad Precautions

InvenSense products have very low active and standby current consumption. The exposed die pad is not required for heat sinking, and should not be soldered to the PCB. Failure to adhere to this rule can induce performance changes due to package thermo-mechanical stress. There is no electrical connection between the pad and the CMOS.

4.5 Block Diagram

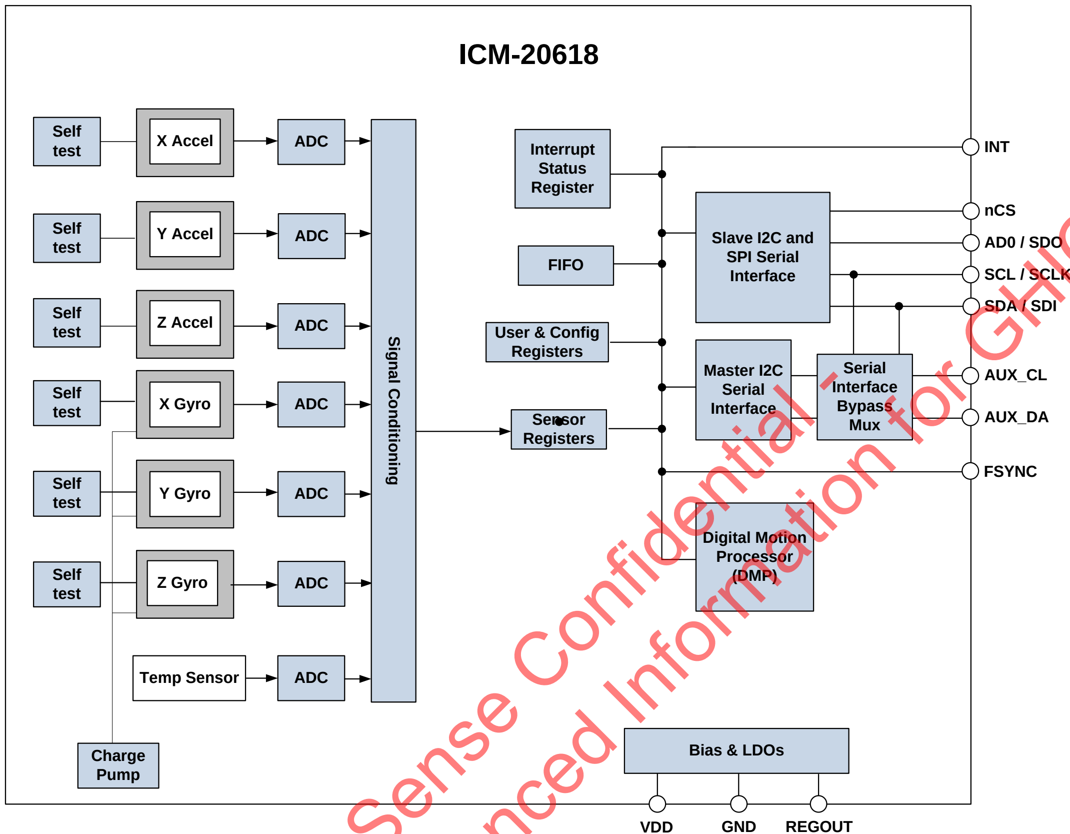


Figure 5 ICM-20618 Block Diagram

4.6 Overview

The ICM-20618 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- Digital Motion Processor (DMP) engine
- Primary I^{2}C and SPI serial communications interfaces
- Auxiliary I^{2}C serial interface
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.7 Three-Axis MEMS Gyroscope with 16-bit ADCs and Signal Conditioning

The ICM-20618 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±250, ±500, ±1000, or ±2000 degrees per second (dps).

4.8 Three-Axis MEMS Accelerometer with 16-bit ADCs and Signal Conditioning

The ICM-20618's 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The ICM-20618's architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g*, or ±16*g*.

4.9 Digital Motion Processor

The embedded Digital Motion Processor (DMP) within the ICM-20618 offloads computation of motion processing algorithms from the host processor. The DMP acquires data from accelerometers, gyroscopes, and additional 3rd party sensors such as magnetometers, and processes the data. The resulting data can be read from the FIFO. The DMP has access to one of the MPU's external pins, which can be used for generating interrupts.

The purpose of the DMP is to offload both timing requirements and processing power from the host processor. Typically, motion processing algorithms should be run at a high rate, often around 200Hz, in order to provide accurate results with low latency. This is required even if the application updates at a much lower rate; for example, a low power user interface may update as slowly as 5Hz, but the motion processing should still run at 200Hz. The DMP can be used to minimize power, simplify timing, simplify the software architecture, and save valuable MIPS on the host processor for use in applications.

4.10 Primary I2C and SPI Serial Communications Interfaces

The ICM-20618 communicates to a system processor using either a SPI or an I^2C serial interface. The ICM-20618 always acts as a slave when communicating to the system processor. The LSB of the of the I^2C slave address is set by pin 9 (AD0).

4.4 ICM-20618 Solution Using I2C Interface

In the figure below, the system processor is an I^2C master to the ICM-20618. In addition, the ICM-20618 is an I^2C master to the optional external compass sensor. The ICM-20618 has limited capabilities as an I^2C Master, and depends on the system processor to manage the initial configuration of any auxiliary sensors. The ICM-20618 has an interface bypass multiplexer, which connects the system processor I^2C bus pins 23 and 24 (SDA and SCL) directly to the auxiliary sensor I^2C bus pins 6 and 7 (AUX_DA and AUX_CL).

Once the auxiliary sensors have been configured by the system processor, the interface bypass multiplexer should be disabled so that the ICM-20618 auxiliary I²C master can take control of the sensor I²C bus and gather data from the auxiliary sensors.

For further information regarding I²C master control, please refer to section 6.

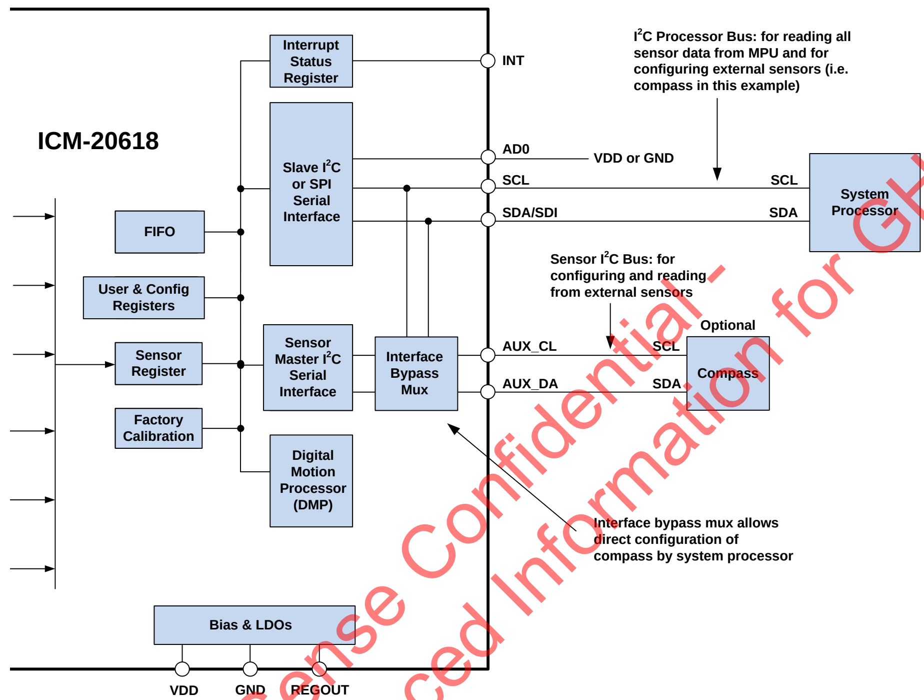


Figure 6 ICM-20618 Solution Using I²C Interface

4.5 ICM-20618 Solution Using SPI Interface

In the figure below, the system processor is an SPI master to the ICM-20618. Pins 8, 9, 23, and 24 are used to support the CS, SDO, SCLK, and SDI signals for SPI communications. Because these SPI pins are shared with the I²C slave pins (9, 23 and 24), the system processor cannot access the auxiliary I²C bus through the interface bypass multiplexer, which connects the processor I²C interface pins to the sensor I²C interface pins. Since the ICM-20618 has limited capabilities as an I²C Master, and depends on the system processor to manage the initial configuration of any auxiliary sensors, another method must be used for programming the sensors on the auxiliary sensor I²C bus pins 6 and 7 (AUX_DA and AUX_CL).

When using SPI communications between the ICM-20618 and the system processor, configuration of devices on the auxiliary I²C sensor bus can be achieved by using I²C Slaves 0-4 to perform read and write transactions on any device and register on the auxiliary I²C bus. The I²C Slave 4 interface can be used to perform only single byte read and write transactions. Once the external sensors have been configured, the ICM-20618 can perform single or multi-byte reads using the sensor I²C bus. The read results from the Slave 0-3 controllers can be written to the FIFO buffer as well as to the external sensor registers.

For further information regarding the control of the ICM-20618's auxiliary I²C interface, please refer to the ICM-20618 Register Map and Register Descriptions document.

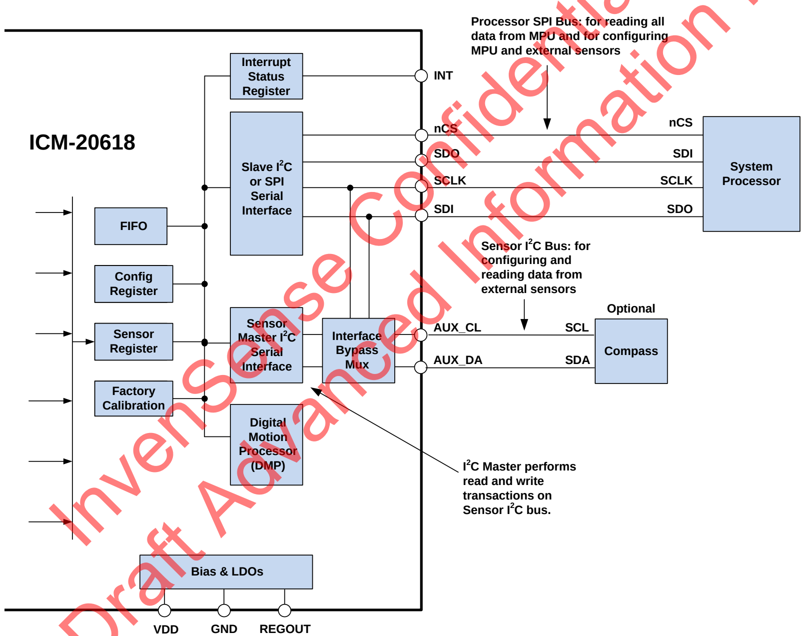


Figure 7 ICM-20618 Solution Using SPI Interface

4.11 Auxiliary I2C Serial Interface

The ICM-20618 has an auxiliary I²C bus for communicating to an off-chip 3-Axis digital output magnetometer or other sensors. This bus has two operating modes:

- I²C Master Mode: The ICM-20618 acts as a master to any external sensors connected to the auxiliary I²C bus
- Pass-Through Mode: The ICM-20618 directly connects the primary and auxiliary I²C buses together, allowing the system processor to directly communicate with any external sensors.

Auxiliary I²C Bus Modes of Operation:

- I²C Master Mode: Allows the ICM-20618 to directly access the data registers of external digital sensors, such as a magnetometer. In this mode, the ICM-20618 directly obtains data from auxiliary sensors without intervention from the system applications processor.

  For example, in I²C Master mode, the ICM-20618 can be configured to perform burst reads, returning the following data from a magnetometer:

  - X magnetometer data (2 bytes)
  - Y magnetometer data (2 bytes)
  - Z magnetometer data (2 bytes)

  The I²C Master can be configured to read up to 24 bytes from up to 4 auxiliary sensors. A fifth sensor can be configured to work single byte read/write mode.

- Pass-Through Mode: Allows an external system processor to act as master and directly communicate to the external sensors connected to the auxiliary I²C bus pins (AUX_DA and AUX_CL). In this mode, the auxiliary I²C bus control logic (3rd party sensor interface block) of the ICM-20618 is disabled, and the auxiliary I²C pins AUX_DA and AUX_CL (Pins 6 and 7) are connected to the main I²C bus (Pins 23 and 24) through analog switches internally.
  Pass-Through mode is useful for configuring the external sensors.

4.12 Self-Test

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers (registers 13 to 16).

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

Self-test response = Sensor output with self-test enabled – Sensor output without self-test enabled

The self-test response for each gyroscope axis is defined in the gyroscope specification table, while that for each accelerometer axis is defined in the accelerometer specification table.

When the value of the self-test response is within the specified min/max limits, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test. It is recommended to use InvenSense MotionApps software for executing self-test.

4.13 Clocking

The internal system clock sources include: (1) an internal relaxation oscillator, and (2) a PLL with MEMS gyroscope oscillator as the reference clock. With the recommended clock selection setting (CLKSEL = 1), the best clock source for optimum sensor performance and power consumption will be automatically selected based on the power mode. Specifically, the internal relaxation oscillator will be selected when operating in accelerometer only mode, while the PLL will be selected whenever gyroscope is on, which includes gyroscope and 6-axis modes.

As clock accuracy is critical to the preciseness of distance and angle calculations performed by DMP, it should be noted that the internal relaxation oscillator and PLL show different performances in some aspects. The internal relaxation oscillator is trimmed to have a consistent operating frequency at room temperature, while the PLL clock frequency varies from part to part. The PLL frequency deviation from the nominal value in percentage is captured in register TIMEBASE_CORRECTION_PLL (detailed in section 12.5), and users can factor it in during distance and angle calculations to not sacrifice accuracy. Other than that, PLL has better frequency stability and lower frequency variation over temperature than the internal relaxation oscillator.

4.14 Sensor Data Registers

The sensor data registers contain the latest gyro, accelerometer, auxiliary sensor, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.15 FIFO

The ICM-20618 contains a FIFO of size 512 bytes that is accessible via the Serial Interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyro data, accelerometer data, temperature readings, auxiliary sensor readings, and FSYNC input.

A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

For further information regarding the FIFO, please refer to the ICM-20618 Register Map and Register Descriptions document.

4.16 Interrupts

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) accelerometer event interrupts; and (4) the ICM-20618 did not receive an acknowledge from an auxiliary sensor on the secondary I^2C bus. The interrupt status can be read from the Interrupt Status register.

For further information regarding interrupts, please refer to the ICM-20618 Register Map and Register Descriptions document.

4.17 Digital-Output Temperature Sensor

An on-chip temperature sensor and ADC are used to measure the ICM-20618 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

4.18 Bias and LDOs

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICM-20618. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at REGOUT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

4.19 Charge Pump

An on-chip charge pump generates the high voltage required for the MEMS oscillators.

4.20 Standard Power Modes

The following table lists the user-accessible power modes for ICM-20618.

Mode	Name	Gyro	Accel	DMP
1	Sleep Mode	Off	Off	Off
2	Accelerometer Mode	Off	Low-Noise or Duty-Cycled	Duty-Cycled or Off
3	Gyroscope Mode	Low-Noise or Duty-Cycled	Off	Duty-Cycled or Off
4	6-Axis Mode	Low-Noise or Duty-Cycled	Low-Noise or Duty-Cycled	Duty-Cycled or Off
5	DMP only mode	Off	Off	Duty-Cycled

Table 11 Standard Power Modes for ICM-20618

Notes:

1. Power consumption for individual modes can be found in section 4.1.

5 Programmable Interrupts

The ICM-20618 has a programmable interrupt system which can generate an interrupt signal on the INT pin. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually.

Interrupt Name	Module
Motion Detection	Motion
FIFO Overflow	FIFO
FIFO Watermark	FIFO
Data Ready	Sensor Registers
I^2C Master errors: Lost Arbitration, NACKs	I^2C Master
I^2C Slave 4	I^2C Master
DMP	DMP

Table 12 Table of Interrupt Sources

For information regarding the interrupt enable/disable registers and flag registers, please refer to the ICM-20618 Register Map and Register Descriptions document.

6 Digital Interface

6.1 I2C and SPI Serial Interfaces

The internal registers and memory of the ICM-20618 can be accessed using either I^2C at 400 kHz or SPI at 2MHz. SPI operates in four-wire mode.

Pin Number	Pin Name	Pin Description
9	AD0 / SDO	I^2C Slave Address LSB (AD0); SPI serial data output (SDO)
22	nCS	Chip select (SPI mode only)
23	SCL / SCLK	I^2C serial clock (SCL); SPI serial clock (SCLK)
24	SDA / SDI	I^2C serial data (SDA); SPI serial data input (SDI)

Table 13 Serial Interface

Note:

To prevent switching into I^2C mode when using SPI, the I^2C interface should be disabled by setting the *I2C_IF_DIS* configuration bit. Setting this bit should be performed immediately after waiting for the time specified by the “Start-Up Time for Register Read/Write” in Section 6.3.

For further information regarding the *I2C_IF_DIS* bit, please refer to the ICM-20618 Register Map and Register Descriptions document.

6.2 I2C Interface

I^2C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I^2C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-20618 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the ICM-20618 is b110100X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin AD0. This allows two ICM-20618s to be connected to the same I^2C bus. When used in this configuration, the address of the one of the devices should be b1101000 (pin AD0 is logic low) and the address of the other should be b1101001 (pin AD0 is logic high).

6.3 I2C Communications Protocol

START (S) and STOP (P) Conditions

Communication on the I^2C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

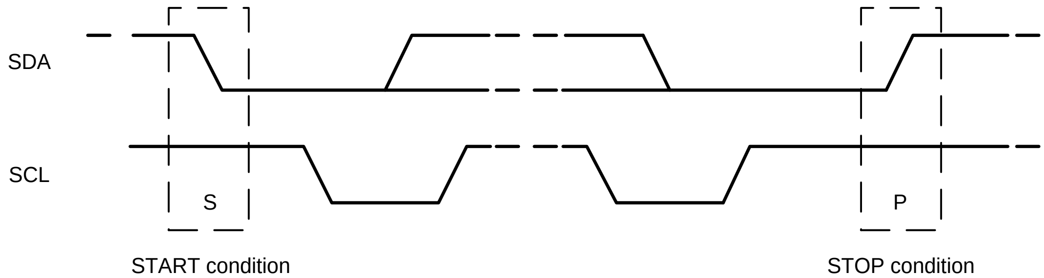


Figure 8 START and STOP Conditions

Data Format / Acknowledge

I^2C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

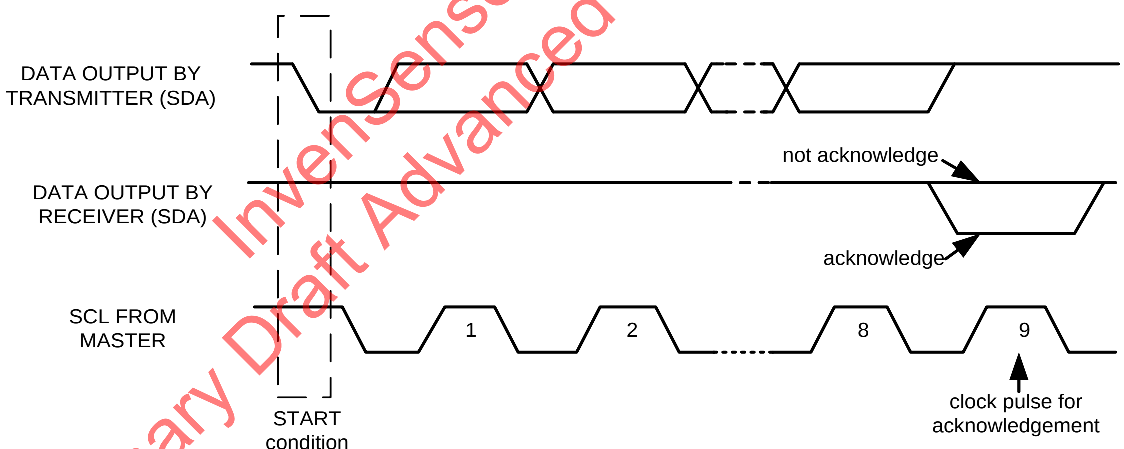


Figure 9 Acknowledge on the I^2C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

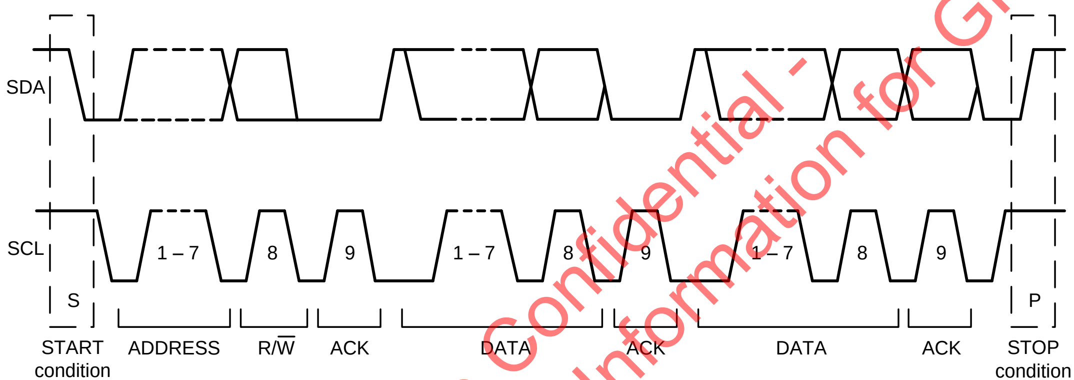


Figure 10 Complete I²C Data Transfer

To write the internal ICM-20618 registers, the master transmits the start condition (S), followed by the I²C address and the write bit (0). At the 9th clock cycle (when the clock is high), the ICM-20618 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the ICM-20618 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the ICM-20618 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal ICM-20618 registers, the master sends a start condition, followed by the I²C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the ICM-20618, the master transmits a start signal followed by the slave address and read bit. As a result, the ICM-20618 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9^{th} clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

6.4 I²C Terms

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9^{th} clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9^{th} clock cycle
RA	ICM-20618 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

Table 14 I²C Terms

6.5 SPI Interface

SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines. The ICM-20618 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO) and the Serial Data Input (SDI) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 2MHz
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

SPI Address format

MSB							LSB
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

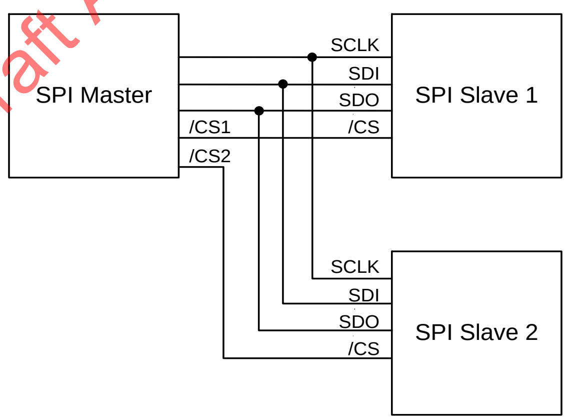


Figure 11 Typical SPI Master / Slave Configuration

7 Serial Interface Considerations

7.1 ICM-20618 Supported Interfaces

The ICM-20618 supports I²C communications on both its primary (microprocessor) serial interface and its auxiliary interface..

The ICM-20618's I/O logic levels are set to be VDDIO.

The figure below depicts a sample circuit of ICM-20618 with a third party magnetometer attached to the auxiliary I²C bus. It shows the relevant logic levels and voltage connections.

Note: Actual configuration will depend on the auxiliary sensors used.

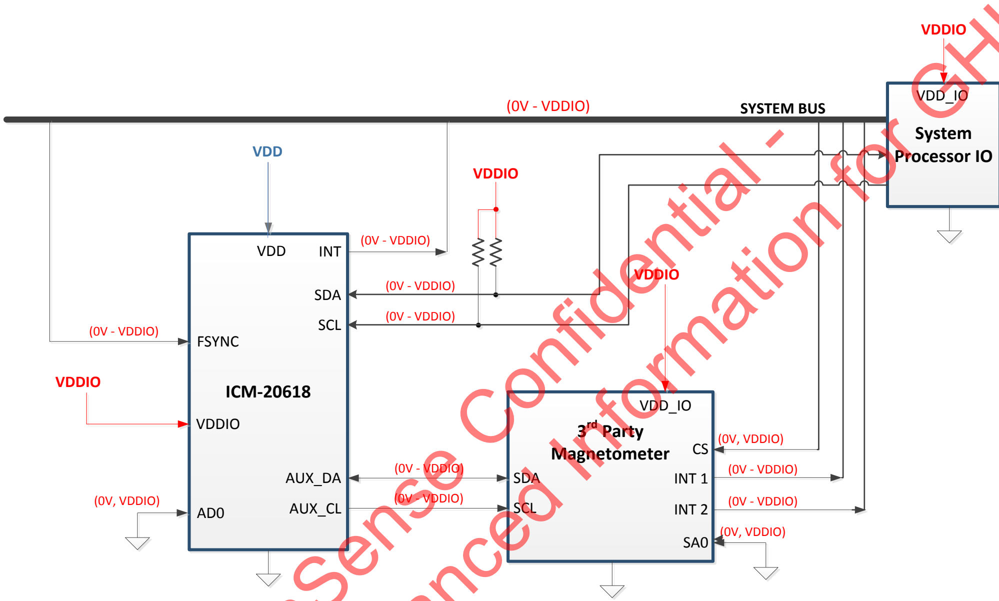


Figure 12 I/O Levels and Connections

8 Orientation of Axes

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

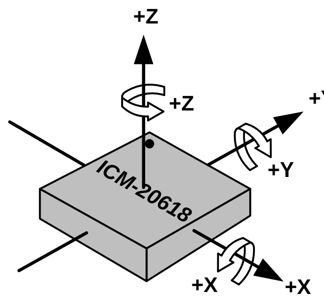
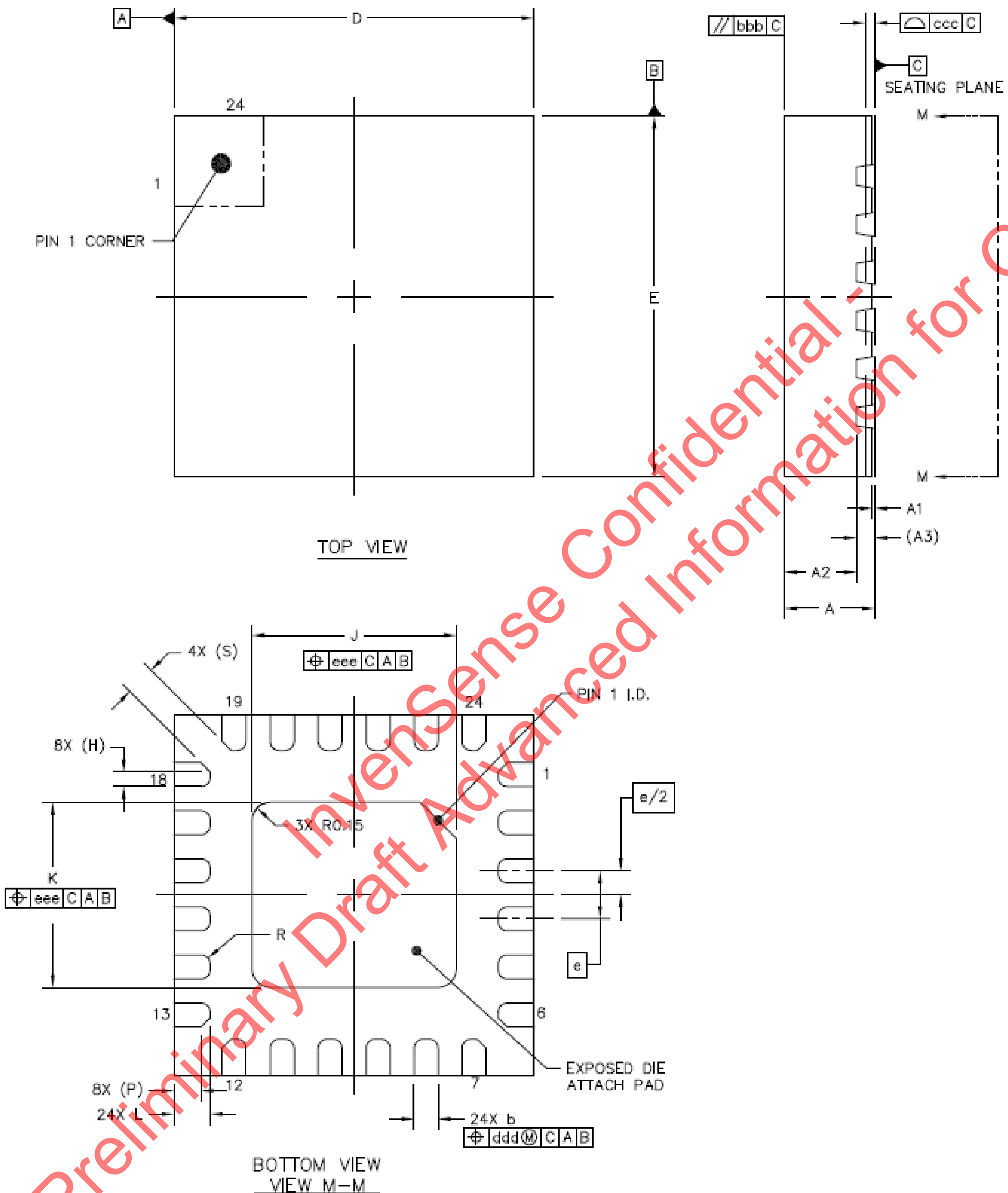


Figure 13 Orientation of Axes of Sensitivity and Polarity of Rotation

9 Package Dimensions

This section provides package dimensions for the device. Information for the 24 Lead QFN 3x3x0.75 package is below.

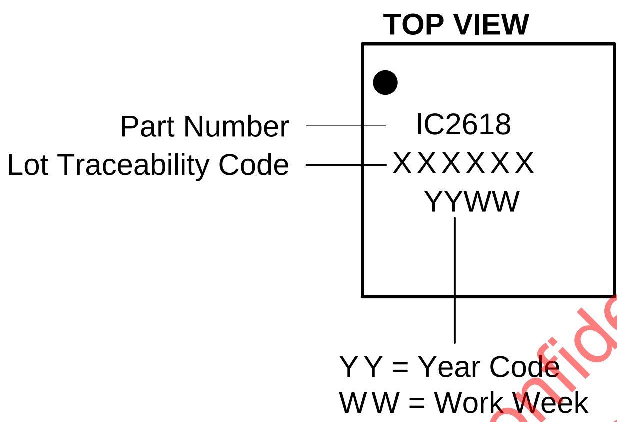


		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Total Thickness		A	0.7	0.75	0.8
Stand Off		A1	0	0.02	0.05
Mold Thickness		A2	---	0.6	---
L/F Thickness		A3	0.152 REF		
Lead Width		b	0.15	0.2	0.25
Body Size	X	D	2.9	3	3.1
	Y	E	2.9	3	3.1
Lead Pitch		e	0.4 BSC		
EP Size	X	J	1.65	1.7	1.75
	Y	K	1.49	1.54	1.59
Lead Length		L	0.25	0.3	0.35
		S	0.25 REF		
		R	0.075	---	---
		H	0.12 REF		
		P	0.22 REF		
Mold Flatness		bbb	0.1		
Coplanarity		ccc	0.075		
Lead Offset		ddd	0.1		
Exposed Pad Offset		eee	0.1		

10 Part Number Part Markings

The part number part markings for ICM-20618 devices are summarized below:

Part Number	Part Number Part Marking
ICM-20618	IC2618



11 Use Notes

11.1 Gyroscope Mode Transition

When gyroscope is transitioning from standard to low-noise mode, several unsettled output samples will be observed at the gyroscope output due to filter switching and settling. The number of unsettled gyroscope output samples depends on the filter and ODR settings.

11.2 LP_EN Bit-Field in Register PWR_MGMT_1

When accelerometer alone is operating in standard mode, LP_EN bit in register PWR_MGMT_1 should be set to 1 to achieve minimum power consumption. When both gyroscope and accelerometer are operating in standard mode the LP_EN bit should be set to 0. LP_EN should also be set to 0 when the gyroscope is operating in standard mode and the accelerometer is off.

11.3 Power Management 1 Register Setting

CLKSEL[2:0] has to be set to 001 to achieve the datasheet performance.

11.4 DMP Memory Access

Reading/writing DMP memory and FIFO through I2C in a multithreaded environment can cause wrong data being read. To avoid the issue, one may use SPI instead of I2C, or use I2C with mutexes.

11.5 Time Base Correction

The system clock frequency at room temperature in gyroscope mode and 6-Axis mode varies from part to part, and the clock rates specified in datasheet are the nominal values. The percentage of frequency deviation from the nominal values for each part is logged in register TIMEBASE_CORRECTION_PLL, and the range of the code is +/- 10% with each LSB representing a step of 0.079%. For example, if on one part TIMEBASE_CORRECTION_PLL = 0x0C = d'12, it means the clock frequency in gyroscope mode and 6-Axis mode is ~0.94% faster than the nominal value.

When operating in accelerometer-only mode, the system clock frequency at room temperature is the nominal frequency over parts, and it is independent of the value stored in TIMEBASE_CORRECTION_PLL register.

11.6 I^2C Master Clock Frequency

I^2C master clock frequency can be set by register I2C_MST_CLK as shown in the table below. Due to temperature variation and part to part variation of system clock frequency in different power modes, I2C_MST_CLK should be set such that in all conditions the clock frequency will not exceed what a slave device can support. To achieve a targeted clock frequency of 400 kHz, MAX, it is recommended to set I2C_MST_CLK = 7 (345.6 kHz / 46.67% duty cycle).

I2C_MST_CLK	Nominal CLK Frequency [kHz]	Duty Cycle
0	370.29	50.00%
1	-	-

2	370.29	50.00%
3	432.00	50.00%
4	370.29	42.86%
5	370.29	50.00%
6	345.60	40.00%
7	345.60	46.67%
8	304.94	47.06%
9	432.00	50.00%
10	432.00	41.67%
11	432.00	41.67%
12	471.27	45.45%
13	432.00	50.00%
14	345.60	46.67%
15	345.60	46.67%

12 Register Map

The following table lists the register map for the ICM-20618, for user banks 0, 1, 2, 3.

User Bank 0 Register Map:

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	0	WHO_AM_I	R	WHO_AM_I[7:0]							
03	3	USER_CTRL	R/W	DMP_EN	FIFO_EN	I2C_MST_EN	I2C_IF_DIS	DMP_RST	SRAM_RST	I2C_MST_RST	-
05	5	LP_CONFIG	R/W	-	I2C_MST_CYCLE	ACCEL_CYCLE	GYRO_CYCLE	-			
06	6	PWR_MGMT_1	R/W	DEVICE_RESET	SLEEP	LP_EN	-	TEMP_DIS	CLKSEL[2:0]		
07	7	PWR_MGMT_2	R/W	-		DISABLE_ACCEL			DISABLE_GYRO		
0F	15	INT_PIN_CFG	R/W	ACTL	OPEN	LATCH_INT_EN	INT_ANYRD_2CLEAR	ACTL_FSYNC	FSYNC_INT_MODE_EN	BYPASS_EN	-
10	16	INT_ENABLE	R/W	REG_WOF_EN	-			WOM_INT_EN	PLL_RDY_EN	DMP_INT_EN	I2C_MST_INT_EN
11	17	INT_ENABLE_1	R/W	-							RAW_DATA_0_RDY_EN
12	18	INT_ENABLE_2	R/W	-			FIFO_OVERFLOW_EN[4:0]				
13	19	INT_ENABLE_3	R/W	-			FIFO_WM_EN[4:0]				
17	23	I2C_MST_STATUS	R/C	PASS_THROUGH	I2C_SLV4_DONE	I2C_LOST_ARB	I2C_SLV4_NACK	I2C_SLV3_NACK	I2C_SLV2_NACK	I2C_SLV1_NACK	I2C_SLV0_NACK
19	25	INT_STATUS	R/C	-				WOM_INT	PLL_RDY_INT	DMP_INT	I2C_MST_INT
1A	26	INT_STATUS_1	R/C	-							RAW_DATA_0_RDY_INT
1B	27	INT_STATUS_2	R/C	-			FIFO_OVERFLOW_INT[4:0]				
1C	28	INT_STATUS_3	R/C	-			FIFO_WM_INT[4:0]				
2D	45	ACCEL_XOUT_H	R	ACCEL_XOUT_H[7:0]							
2E	46	ACCEL_XOUT_L	R	ACCEL_XOUT_L[7:0]							
2F	47	ACCEL_YOUT_H	R	ACCEL_YOUT_H[7:0]							
30	48	ACCEL_YOUT_L	R	ACCEL_YOUT_L[7:0]							
31	49	ACCEL_ZOUT_H	R	ACCEL_ZOUT_H[7:0]							
32	50	ACCEL_ZOUT_L	R	ACCEL_ZOUT_L[7:0]							
33	51	GYRO_XOUT_H	R	GYRO_XOUT_H[7:0]							
34	52	GYRO_XOUT_L	R	GYRO_XOUT_L[7:0]							
35	53	GYRO_YOUT_H	R	GYRO_YOUT_H[7:0]							
36	54	GYRO_YOUT_L	R	GYRO_YOUT_L[7:0]							
37	55	GYRO_ZOUT_H	R	GYRO_ZOUT_H[7:0]							
38	56	GYRO_ZOUT_L	R	GYRO_ZOUT_L[7:0]							
39	57	TEMP_OUT_H	R	TEMP_OUT_H[7:0]							
3A	58	TEMP_OUT_L	R	TEMP_OUT_L[7:0]							
3B	59	EXT_SLV_SENS_DATA_00	R	EXT_SLV_SENS_DATA_00[7:0]							
3C	60	EXT_SLV_SENS_DATA_01	R	EXT_SLV_SENS_DATA_01[7:0]							
3D	61	EXT_SLV_SENS_DATA_02	R	EXT_SLV_SENS_DATA_02[7:0]							
3E	62	EXT_SLV_SENS_DATA_03	R	EXT_SLV_SENS_DATA_03[7:0]							
3F	63	EXT_SLV_SENS_DATA_04	R	EXT_SLV_SENS_DATA_04[7:0]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
40	64	EXT_SLV_SENS_DATA_05	R	EXT_SLV_SENS_DATA_05[7:0]							
41	65	EXT_SLV_SENS_DATA_06	R	EXT_SLV_SENS_DATA_06[7:0]							
42	66	EXT_SLV_SENS_DATA_07	R	EXT_SLV_SENS_DATA_07[7:0]							
43	67	EXT_SLV_SENS_DATA_08	R	EXT_SLV_SENS_DATA_08[7:0]							
44	68	EXT_SLV_SENS_DATA_09	R	EXT_SLV_SENS_DATA_09[7:0]							
45	69	EXT_SLV_SENS_DATA_10	R	EXT_SLV_SENS_DATA_10[7:0]							
46	70	EXT_SLV_SENS_DATA_11	R	EXT_SLV_SENS_DATA_11[7:0]							
47	71	EXT_SLV_SENS_DATA_12	R	EXT_SLV_SENS_DATA_12[7:0]							
48	72	EXT_SLV_SENS_DATA_13	R	EXT_SLV_SENS_DATA_13[7:0]							
49	73	EXT_SLV_SENS_DATA_14	R	EXT_SLV_SENS_DATA_14[7:0]							
4A	74	EXT_SLV_SENS_DATA_15	R	EXT_SLV_SENS_DATA_15[7:0]							
4B	75	EXT_SLV_SENS_DATA_16	R	EXT_SLV_SENS_DATA_16[7:0]							
4C	76	EXT_SLV_SENS_DATA_17	R	EXT_SLV_SENS_DATA_17[7:0]							
4D	77	EXT_SLV_SENS_DATA_18	R	EXT_SLV_SENS_DATA_18[7:0]							
4E	78	EXT_SLV_SENS_DATA_19	R	EXT_SLV_SENS_DATA_19[7:0]							
4F	79	EXT_SLV_SENS_DATA_20	R	EXT_SLV_SENS_DATA_20[7:0]							
50	80	EXT_SLV_SENS_DATA_21	R	EXT_SLV_SENS_DATA_21[7:0]							
51	81	EXT_SLV_SENS_DATA_22	R	EXT_SLV_SENS_DATA_22[7:0]							
52	82	EXT_SLV_SENS_DATA_23	R	EXT_SLV_SENS_DATA_23[7:0]							
66	102	FIFO_EN_1	R/W	-				SLV_3_FIFO_EN	SLV_2_FIFO_EN	SLV_1_FIFO_EN	SLV_0_FIFO_EN
67	103	FIFO_EN_2	R/W	-			ACCEL_FIFO_EN	GYRO_Z_FIFO_EN	GYRO_Y_FIFO_EN	GYRO_X_FIFO_EN	TEMP_FIFO_EN
68	104	FIFO_RST	R/W	-			FIFO_RESET[4:0]				
69	105	FIFO_MODE	R/W	-			FIFO_MODE[4:0]				
70	112	FIFO_COUNTH	R	-			FIFO_CNT[12:8]				
71	113	FIFO_COUNTL	R	FIFO_CNT[7:0]							
72	114	FIFO_R_W	R/W	FIFO_R_W[7:0]							
74	116	DATA_RDY_STATUS	R/C	WOF_STATUS	WOM_STATUS	-		RAW_DATA_RDY[3:0]			
76	118	FIFO_CFG	R/W	-							FIFO_CFG
7F	127	REG_BANK_SEL	R/W	-		USER_BANK[1:0]		-			

User Bank 1 Register Map:

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02	2	SELF_TEST_X_GYRO	R/W	XG_ST_DATA[7:0]							
03	3	SELF_TEST_Y_GYRO	R/W	YG_ST_DATA[7:0]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04	4	SELF_TEST_Z_GYRO	R/W	ZG_ST_DATA[7:0]							
0E	14	SELF_TEST_X_ACCEL	R/W	XA_ST_DATA[7:0]							
0F	15	SELF_TEST_Y_ACCEL	R/W	YA_ST_DATA[7:0]							
10	16	SELF_TEST_Z_ACCEL	R/W	ZA_ST_DATA[7:0]							
14	20	XA_OFFS_H	R/W	XA_OFFS[14:7]							
15	21	XA_OFFS_L	R/W	XA_OFFS[6:0]							-
17	23	YA_OFFS_H	R/W	YA_OFFS[14:7]							
18	24	YA_OFFS_L	R/W	YA_OFFS[6:0]							-
1A	26	ZA_OFFS_H	R/W	ZA_OFFS[14:7]							
1B	27	ZA_OFFS_L	R/W	ZA_OFFS[6:0]							-
28	40	TIMEBASE_CORRECTION_PLL	R/W	TBC_PLL[7:0]							
7F	127	REG_BANK_SEL	R/W	-		USER_BANK[1:0]		-			

User Bank 2 Register Map:

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	0	GYRO_SMPLRT_DIV	R/W	GYRO_SMPLRT_DIV[7:0]							
01	1	GYRO_CONFIG_1	R/W	-		GYRO_DLPFCFG[2:0]			GYRO_FS_SEL[1:0]		GYRO_FCHOICE
02	2	GYRO_CONFIG_2	R/W	-		XGYRO_CTEN	YGYRO_CTEN	ZGYRO_CTEN	GYRO_AVGCFG[2:0]		
03	3	XG_OFFS_USRH	R/W	X_OFFS_USER[15:8]							
04	4	XG_OFFS_USRL	R/W	X_OFFS_USER[7:0]							
05	5	YG_OFFS_USRH	R/W	Y_OFFS_USER[15:8]							
06	6	YG_OFFS_USRL	R/W	Y_OFFS_USER[7:0]							
07	7	ZG_OFFS_USRH	R/W	Z_OFFS_USER[15:8]							
08	8	ZG_OFFS_USRL	R/W	Z_OFFS_USER[7:0]							
10	16	ACCEL_SMPLRT_DIV_1	R/W	-				ACCEL_SMPLRT_DIV[11:8]			
11	17	ACCEL_SMPLRT_DIV_2	R/W	ACCEL_SMPLRT_DIV[7:0]							
12	18	ACCEL_INTEL_CTRL	R/W	-						ACCEL_INTEL_EN	ACCEL_INTEL_MODE_INT
13	19	ACCEL_WOM_THR	R/W	WOM_THRESHOLD[7:0]							
14	20	ACCEL_CONFIG	R/W	-		ACCEL_DLPFCFG[2:0]			ACCEL_FS_SEL[1:0]		ACCEL_FCHOICE
15	21	ACCEL_CONFIG_2	R/W	-			AX_ST_EN_REG	AY_ST_EN_REG	AZ_ST_EN_REG	DEC3_CFG[1:0]	
52	82	FSYNC_CONFIG	R/W	-		WOF_DEGLITCH_EN	WOF_EDGE_INT	EXT_SYNC_SET[3:0]			
53	83	TEMP_CONFIG	R/W	-					TEMP_DLPFCFG[2:0]		
54	84	MOD_CTRL_USR	R/W	-							REG_LP_DMP_EN
7F	127	REG_BANK_SEL	R/W	-		USER_BANK[1:0]		-			

User Bank 3 Register Map:

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	0	I2C_MST_ODR_CONFIG	R/W	-				I2C_MST_ODR_CONFIG[3:0]			
01	1	I2C_MST_CTRL	R/W	MULT_MST_EN	-		I2C_MST_P_NSR	I2C_MST_CLK[3:0]			

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02	2	I2C_MST_DELAY_CTRL	R/W	DELAY_ES_SHADOW	-		I2C_SLV4_DELAY_EN	I2C_SLV3_DELAY_EN	I2C_SLV2_DELAY_EN	I2C_SLV1_DELAY_EN	I2C_SLV0_DELAY_EN
03	3	I2C_SLV0_ADDR	R/W	I2C_SLV0_RNW	I2C_ID_0[6:0]						
04	4	I2C_SLV0_REG	R/W	I2C_SLV0_REG[7:0]							
05	5	I2C_SLV0_CTRL	R/W	I2C_SLV0_EN	I2C_SLV0_BYTE_SW	I2C_SLV0_REG_DIS	I2C_SLV0_GRP	I2C_SLV0_LENG[3:0]			
06	6	I2C_SLV0_DO	R/W	I2C_SLV0_DO[7:0]							
07	7	I2C_SLV1_ADDR	R/W	I2C_SLV1_RNW	I2C_ID_1[6:0]						
08	8	I2C_SLV1_REG	R/W	I2C_SLV1_REG[7:0]							
09	9	I2C_SLV1_CTRL	R/W	I2C_SLV1_EN	I2C_SLV1_BYTE_SW	I2C_SLV1_REG_DIS	I2C_SLV1_GRP	I2C_SLV1_LENG[3:0]			
0A	10	I2C_SLV1_DO	R/W	I2C_SLV1_DO[7:0]							
0B	11	I2C_SLV2_ADDR	R/W	I2C_SLV2_RNW	I2C_ID_2[6:0]						
0C	12	I2C_SLV2_REG	R/W	I2C_SLV2_REG[7:0]							
0D	13	I2C_SLV2_CTRL	R/W	I2C_SLV2_EN	I2C_SLV2_BYTE_SW	I2C_SLV2_REG_DIS	I2C_SLV2_GRP	I2C_SLV2_LENG[3:0]			
0E	14	I2C_SLV2_DO	R/W	I2C_SLV2_DO[7:0]							
0F	15	I2C_SLV3_ADDR	R/W	I2C_SLV3_RNW	I2C_ID_3[6:0]						
10	16	I2C_SLV3_REG	R/W	I2C_SLV3_REG[7:0]							
11	17	I2C_SLV3_CTRL	R/W	I2C_SLV3_EN	I2C_SLV3_BYTE_SW	I2C_SLV3_REG_DIS	I2C_SLV3_GRP	I2C_SLV3_LENG[3:0]			
12	18	I2C_SLV3_DO	R/W	I2C_SLV3_DO[7:0]							
13	19	I2C_SLV4_ADDR	R/W	I2C_SLV4_RNW	I2C_ID_4[6:0]						
14	20	I2C_SLV4_REG	R/W	I2C_SLV4_REG[7:0]							
15	21	I2C_SLV4_CTRL	R/W	I2C_SLV4_EN	I2C_SLV4_BYTE_SW	I2C_SLV4_REG_DIS	I2C_SLV4_DLY[4:0]				
16	22	I2C_SLV4_DO	R/W	I2C_SLV4_DO[7:0]							
17	23	I2C_SLV4_DI	R	I2C_SLV4_DI[7:0]							
7F	127	REG_BANK_SEL	R/W	-		USER_BANK[1:0]		-			

13 Register Descriptions

This section describes the function and contents of each register within the ICM-20618.

Note: The device will come up in sleep mode upon power-up.

13.1 USR Bank 0 Register Map

13.1.1 WHO_AM_I

Name: WHO_AM_I
Address: 0 (00h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0xA0

BIT	NAME	FUNCTION
7:0	WHO_AM_I[7:0]	Register to indicate to user which device is being accessed. The value for ICM-20618 is 0xA0

13.1.2 USER_CTRL

Name: USER_CTRL
Address: 3 (03h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7	DMP_EN	1 – Enables DMP features. 0 – DMP features are disabled after the current processing round has completed.
6	FIFO_EN	1 – Enable FIFO operation mode. 0 – Disable FIFO access from serial interface. To disable FIFO writes by DMA, use FIFO_EN register. To disable possible FIFO writes from DMP, disable the DMP.
5	I2C_MST_EN	1 – Enable the I2C Master I/F module; pins ES_DA and ES_SCL are isolated from pins SDA/SDI and SCL/ SCLK. 0 – Disable I2C Master I/F module; pins ES_DA and ES_SCL are logically driven by pins SDA/SDI and SCL/ SCLK.
4	I2C_IF_DIS	1 – Reset I2C Slave module and put the serial interface in SPI mode only.
3	DMP_RST	1 – Reset DMP module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20MHz clock.
2	SRAM_RST	1 – Reset SRAM module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20MHz clock.
1	I2C_MST_RST	1 – Reset I2C Master module. Reset is asynchronous. This bit auto clears after one clock cycle of the internal 20MHz clock. NOTE: This bit should only be set when the I2C master has hung. If

		this bit is set during an active I2C master transaction, the I2C slave will hang, which will require the host to reset the slave.
0	-	Reserved

13.1.3 LP_CONFIG

Name: LP_CONFIG
Address: 5 (05h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 1000000

BIT	NAME	FUNCTION
7	-	Reserved
6	I2C_MST_CYCLE	1 - Operate I2C master in duty cycled mode. ODR is determined by I2C_MST_ODR_CONFIG register. 0 – Disable I2C master duty cycled mode.
5	ACCEL_CYCLE	1 – Operate ACCEL in duty cycled mode. ODR is determined by ACCEL_SMPLRT_DIV register. 0 – Disable ACCEL duty cycled mode.
4	GYRO_CYCLE	1 – Operate GYRO in duty cycled mode. ODR is determined by GYRO_SMPLRT_DIV register. 0 – Disable GYRO duty cycled mode.
3:0	-	Reserved

13.1.4 PWR_MGMT_1

Name: PWR_MGMT_1
Address: 6 (06h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0x41

BIT	NAME	FUNCTION
7	DEVICE_RESET	1 – Reset the internal registers and restores the default settings. Write a 1 to set the reset, the bit will auto clear.
6	SLEEP	When set, the chip is set to sleep mode (in sleep mode all analog is powered off). Clearing the bit wakes the chip from sleep mode.
5	LP_EN	When accelerometer alone is operating in low-power mode, LP_EN bit should be set to 1 to achieve minimum power consumption. When both gyroscope and accelerometer are operating in low-power mode the LP_EN bit should be set to 0. LP_EN should also be set to 0 when the gyroscope is operating in low-power mode and the accelerometer is off.
4	-	Reserved

3	TEMP_DIS	When set to 1, this bit disables the temperature sensor.
2:0	CLKSEL[2:0]	**Code: Clock Source** 0: Internal 20MHz oscillator 1-5: Auto selects the best available clock source – PLL if ready, else use the Internal oscillator 6: Internal 20MHz oscillator 7: Stops the clock and keeps timing generator in reset NOTE: CLKSEL[2:0] should be set to 1~5 to achieve full gyroscope performance.

13.1.5 PWR_MGMT_2

Name: PWR_MGMT_2
Address: 7 (07h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:6	-	Reserved
5:3	DISABLE_ACCEL	Only the following values are applicable: 111 – Accelerometer (all axes) disabled 000 – Accelerometer (all axes) on
2:0	DISABLE_GYRO	Only the following values are applicable: 111 – Gyroscope (all axes) disabled 000 – Gyroscope (all axes) on

13.1.6 INT_PIN_CFG

Name: INT_PIN_CFG
Address: 15 (0Fh)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7	ACTL	1 – The logic level for INT pin is active low. 0 – The logic level for INT pin is active high.
6	OPEN	1 – INT pin is configured as open drain. 0 – INT pin is configured as push-pull.
5	LATCH_INT_EN	1 – INT pin level held until interrupt status is cleared. 0 – INT pin indicates interrupt pulse is width 50us.
4	INT_ANYRD_2CLEAR	1 – Interrupt status in INT_STATUS is cleared (set to 0) if any read operation is performed. 0 – Interrupt status in INT_STATUS is cleared (set to 0) only by reading INT_STATUS register. This bit only affects the interrupt status bits that are contained in the register INT_STATUS, and the corresponding hardware interrupt.

		This bit does not affect the interrupt status bits that are contained in registers INT_STATUS_1, INT_STATUS_2, INT_STATUS_3, and the corresponding hardware interrupt.
3	ACTL_FSYNC	1 – The logic level for the FSYNC pin as an interrupt to the ICM-20618 is active low. 0 – The logic level for the FSYNC pin as an interrupt to the ICM-20618 is active high.
2	FSYNC_INT_MODE_EN	1 – This enables the FSYNC pin to be used as an interrupt. A transition to the active level described by the ACTL_FSYNC bit will cause an interrupt. The status of the interrupt is read in the I2C Master Status register PASS_THROUGH bit. 0 – This disables the FSYNC pin from causing an interrupt.
1	BYPASS_EN	When asserted, the I2C_MASTER interface pins (ES_CL and ES_DA) will go into 'bypass mode' when the I2C master interface is disabled.
0	-	Reserved

13.1.7 INT_ENABLE

Name: INT_ENABLE
Address: 16 (10h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7	REG_WOF_EN	1 – Enable wake on FSYNC interrupt 0 – Function is disabled.
6:4	-	Reserved
3	WOM_INT_EN	1 – Enable interrupt for wake on motion to propagate to interrupt pin. 0 – Function is disabled.
2	PLL_RDY_EN	1 – Enable PLL RDY interrupt (PLL RDY means PLL is running and in use as the clock source for the system) to propagate to interrupt pin. 0 – Function is disabled.
1	DMP_INT_EN	1 – Enable DMP interrupt to propagate to interrupt pin. 0 – Function is disabled.
0	I2C_MST_INT_EN	1 – Enable I2C master interrupt to propagate to interrupt pin. 0 – Function is disabled.

13.1.8 INT_ENABLE_1

Name: INT_ENABLE_1
Address: 17 (11h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:1	-	Reserved

0	RAW_DATA_0_RDY_EN	1 – Enable raw data ready interrupt from any sensor. 0 – Function is disabled.

13.1.9 INT_ENABLE_2

Name: INT_ENABLE_2 **Address: 18 (12h)** **Type: USR0** **Bank: 0** **Serial IF: R/W** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:5	-	Reserved
4:0	FIFO_OVERFLOW_EN[4:0]	1 – Enable interrupt for FIFO overflow to propagate to interrupt pin. 0 – Function is disabled.

13.1.10 INT_ENABLE_3

Name: INT_ENABLE_3 **Address: 19 (13h)** **Type: USR0** **Bank: 0** **Serial IF: R/W** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:5	-	Reserved
4:0	FIFO_WM_EN[4:0]	1 – Enable interrupt for FIFO watermark to propagate to interrupt pin. 0 – function is disabled

13.1.11 I2C_MST_STATUS

Name: I2C_MST_STATUS **Address: 23 (17h)** **Type: USR0** **Bank: 0** **Serial IF: R/C** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7	PASS_THROUGH	Status of FSYNC interrupt – used as a way to pass an external interrupt through this chip to the host. If enabled in the INT_PIN_CFG register by asserting bit FSYNC_INT_MODE_EN, this will cause an interrupt. A read of this register clears all status bits in this register.
6	I2C_SLV4_DONE	Asserted when I2C slave 4's transfer is complete, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted, and if the SLV4_DONE_INT_EN bit is asserted in the I2C_SLV4_CTRL register.

5	I2C_LOST_ARB	Asserted when I2C slave loses arbitration of the I2C bus, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted.
4	I2C_SLV4_NACK	Asserted when slave 4 receives a NACK, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted.
3	I2C_SLV3_NACK	Asserted when slave 3 receives a NACK, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted.
2	I2C_SLV2_NACK	Asserted when slave 2 receives a NACK, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted.
1	I2C_SLV1_NACK	Asserted when slave 1 receives a NACK, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted.
0	I2C_SLV0_NACK	Asserted when slave 0 receives a NACK, will cause an interrupt if bit I2C_MST_INT_EN in the INT_ENABLE register is asserted.

13.1.12 INT_STATUS

Name: INT_STATUS
Address: 25 (19h)
Type: USR0
Bank: 0
Serial IF: R/C
Reset Value: 0

BIT	NAME	FUNCTION
7:4	-	Reserved
3	WOM_INT	1 – Wake on motion interrupt occurred.
2	PLL_RDY_INT	1 – Indicates that the PLL has been enabled and is ready (delay of 4ms ensures lock).
1	DMP_INT	1 – Indicates the DMP has generated an interrupt
0	I2C_MST_INT	1 - Indicates I2C master has generated an interrupt

13.1.13 INT_STATUS_1

Name: INT_STATUS_1
Address: 26 (1Ah)
Type: USR0
Bank: 0
Serial IF: R/C
Reset Value: 0

BIT	NAME	FUNCTION
7:1	-	Reserved
0	RAW_DATA_0_RDY_INT	1 – Sensor Register Raw Data, from all sensors, is updated and ready to be read.

13.1.14 INT_STATUS_2

Name: INT_STATUS_2
Address: 27 (1Bh)
Type: USR0

Bank: 0 **Serial IF: R/C** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:5	-	Reserved
4:0	FIFO_OVERFLOW_INT[4:0]	1 – FIFO Overflow interrupt occurred.

13.1.15 INT_STATUS_3

Name: INT_STATUS_3 **Address: 28 (1Ch)** **Type: USR0** **Bank: 0** **Serial IF: R/C** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:5	-	Reserved
4:0	FIFO_WM_INT[4:0]	1 – Watermark interrupt for FIFO occurred

13.1.16 ACCEL_XOUT_H

Name: ACCEL_XOUT_H **Address: 45 (2Dh)** **Type: USR0** **Bank: 0** **Serial IF: R** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:0	ACCEL_XOUT_H[7:0]	High Byte of Accelerometer X-axis data

13.1.17 ACCEL_XOUT_L

Name: ACCEL_XOUT_L **Address: 46 (2Eh)** **Type: USR0** **Bank: 0** **Serial IF: R** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:0	ACCEL_XOUT_L[7:0]	Low Byte of Accelerometer X-axis data To convert the output of the accelerometer to acceleration measurement use the formula below:

		X_acceleration = ACCEL_XOUT/Accel_Sensitivity

13.1.18 ACCEL_YOUT_H

Name: ACCEL_YOUT_H
Address: 47 (2Fh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	ACCEL_YOUT_H[7:0]	High Byte of Accelerometer Y-axis data

13.1.19 ACCEL_YOUT_L

Name: ACCEL_YOUT_L
Address: 48 (30h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	ACCEL_YOUT_L[7:0]	Low Byte of Accelerometer Y-axis data To convert the output of the accelerometer to acceleration measurement use the formula below: Y_acceleration = ACCEL_YOUT/Accel_Sensitivity

13.1.20 ACCEL_ZOUT_H

Name: ACCEL_ZOUT_H
Address: 49 (31h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	ACCEL_ZOUT_H[7:0]	High Byte of Accelerometer Z-axis data

13.1.21 ACCEL_ZOUT_L

Name: ACCEL_ZOUT_L
Address: 50 (32h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	ACCEL_ZOUT_L[7:0]	Low Byte of Accelerometer Z-axis data To convert the output of the accelerometer to acceleration measurement use the formula below: Z_acceleration = ACCEL_ZOUT/Accel_Sensitivity

13.1.22 GYRO_XOUT_H

Name: GYRO_XOUT_H
Address: 51 (33h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	GYRO_XOUT_H[7:0]	High Byte of Gyroscope X-axis data

13.1.23 GYRO_XOUT_L

Name: GYRO_XOUT_L
Address: 52 (34h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	GYRO_XOUT_L[7:0]	Low Byte of Gyroscope X-axis data To convert the output of the gyroscope to angular rate measurement use the formula below: X_angular_rate = GYRO_XOUT/Gyro_Sensitivity

13.1.24 GYRO_YOUT_H

Name: GYRO_YOUT_H
Address: 53 (35h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	GYRO_YOUT_H[7:0]	High Byte of Gyroscope Y-axis data

13.1.25 GYRO_YOUT_L

Name: GYRO_YOUT_L
Address: 54 (36h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	GYRO_YOUT_L[7:0]	Low Byte of Gyroscope Y-axis data To convert the output of the gyroscope to angular rate measurement use the formula below: Y_angular_rate = GYRO_YOUT/Gyro_Sensitivity

13.1.26 GYRO_ZOUT_H

Name: GYRO_ZOUT_H
Address: 55 (37h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	GYRO_ZOUT_H[7:0]	High Byte of Gyroscope Z-axis data

13.1.27 GYRO_ZOUT_L

Name: GYRO_ZOUT_L
Address: 56 (38h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	GYRO_ZOUT_L[7:0]	Low Byte of Gyroscope Z-axis data To convert the output of the gyroscope to angular rate measurement use the formula below: Z_angular_rate = GYRO_ZOUT/Gyro_Sensitivity

13.1.28 TEMP_OUT_H

Name: TEMP_OUT_H
Address: 57 (39h)
Type: USR0
Bank: 0
Serial IF: R

Reset Value: 0		
BIT	**NAME**	**FUNCTION**
7:0	TEMP_OUT_H[7:0]	High Byte of Temp sensor data

13.1.29 TEMP_OUT_L

Name: TEMP_OUT_L **Address: 58 (3Ah)** **Type: USR0** **Bank: 0** **Serial IF: R** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:0	TEMP_OUT_L[7:0]	Low Byte of Temp sensor data To convert the output of the temperature sensor to degrees C use the following formula: TEMP_degC = ((TEMP_OUT – RoomTemp_Offset)/Temp_Sensitivity) + 21degC

13.1.30 EXT_SLV_SENS_DATA_00

Name: EXT_SLV_SENS_DATA_00 **Address: 59 (3Bh)** **Type: USR0** **Bank: 0** **Serial IF: R** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:0	EXT_SLV_SENS_DATA_00[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.31 EXT_SLV_SENS_DATA_01

Name: EXT_SLV_SENS_DATA_01 **Address: 60 (3Ch)** **Type: USR0** **Bank: 0** **Serial IF: R** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:0	EXT_SLV_SENS_DATA_01[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.32 EXT_SLV_SENS_DATA_02

Name: EXT_SLV_SENS_DATA_02
Address: 61 (3Dh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_02[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.33 EXT_SLV_SENS_DATA_03

Name: EXT_SLV_SENS_DATA_03
Address: 62 (3Eh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_03[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.34 EXT_SLV_SENS_DATA_04

Name: EXT_SLV_SENS_DATA_04
Address: 63 (3Fh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_04[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.35 EXT_SLV_SENS_DATA_05

Name: EXT_SLV_SENS_DATA_05
Address: 64 (40h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA	Sensor data read from external I2C devices via the I2C master

	_05[7:0]	interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.36 EXT_SLV_SENS_DATA_06

Name: EXT_SLV_SENS_DATA_06
Address: 65 (41h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_06[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.37 EXT_SLV_SENS_DATA_07

Name: EXT_SLV_SENS_DATA_07
Address: 66 (42h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_07[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.38 EXT_SLV_SENS_DATA_08

Name: EXT_SLV_SENS_DATA_08
Address: 67 (43h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_08[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.39 EXT_SLV_SENS_DATA_09

Name: EXT_SLV_SENS_DATA_09
Address: 68 (44h)
Type: USR0
Bank: 0
Serial IF: R

Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_09[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.40 EXT_SLV_SENS_DATA_10

Name: EXT_SLV_SENS_DATA_10
Address: 69 (45h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_10[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.41 EXT_SLV_SENS_DATA_11

Name: EXT_SLV_SENS_DATA_11
Address: 70 (46h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_11[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.42 EXT_SLV_SENS_DATA_12

Name: EXT_SLV_SENS_DATA_12
Address: 71 (47h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_12[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.43 EXT_SLV_SENS_DATA_13

Name: EXT_SLV_SENS_DATA_13
Address: 72 (48h)

Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_13[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.44 EXT_SLV_SENS_DATA_14

Name: EXT_SLV_SENS_DATA_14
Address: 73 (49h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_14[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.45 EXT_SLV_SENS_DATA_15

Name: EXT_SLV_SENS_DATA_15
Address: 74 (4Ah)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_15[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.46 EXT_SLV_SENS_DATA_16

Name: EXT_SLV_SENS_DATA_16
Address: 75 (4Bh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_16[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.47 EXT_SLV_SENS_DATA_17

Name: EXT_SLV_SENS_DATA_17
Address: 76 (4Ch)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_17[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.48 EXT_SLV_SENS_DATA_18

Name: EXT_SLV_SENS_DATA_18
Address: 77 (4Dh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_18[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.49 EXT_SLV_SENS_DATA_19

Name: EXT_SLV_SENS_DATA_19
Address: 78 (4Eh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_19[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.50 EXT_SLV_SENS_DATA_20

Name: EXT_SLV_SENS_DATA_20
Address: 79 (4Fh)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA	Sensor data read from external I2C devices via the I2C master

	_20[7:0]	interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.51 EXT_SLV_SENS_DATA_21

Name: EXT_SLV_SENS_DATA_21
Address: 80 (50h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_21[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.52 EXT_SLV_SENS_DATA_22

Name: EXT_SLV_SENS_DATA_22
Address: 81 (51h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_22[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.53 EXT_SLV_SENS_DATA_23

Name: EXT_SLV_SENS_DATA_23
Address: 82 (52h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:0	EXT_SLV_SENS_DATA_23[7:0]	Sensor data read from external I2C devices via the I2C master interface. The data stored is controlled by the I2C_SLV(0-4)_ADDR, I2C_SLV(0-4)_REG, and I2C_SLV(0-4)_CTRL registers

13.1.54 FIFO_EN_1

Name: FIFO_EN_1
Address: 102 (66h)
Type: USR0
Bank: 0
Serial IF: R/W

Reset Value: 0		
BIT	**NAME**	**FUNCTION**
7:4	-	Reserved
3	SLV_3_FIFO_EN	1 – write EXT_SENS_DATA registers associated to SLV_3 (as determined by I2C_SLV2_CTRL, I2C_SLV1_CTRL, and I2C_SL20_CTRL) to the FIFO at the sample rate; 0 – function is disabled
2	SLV_2_FIFO_EN	1 – write EXT_SENS_DATA registers associated to SLV_2 (as determined by I2C_SLV0_CTRL, I2C_SLV1_CTRL, and I2C_SL20_CTRL) to the FIFO at the sample rate; 0 – function is disabled
1	SLV_1_FIFO_EN	1 – write EXT_SENS_DATA registers associated to SLV_1 (as determined by I2C_SLV0_CTRL and I2C_SLV1_CTRL) to the FIFO at the sample rate; 0 – function is disabled
0	SLV_0_FIFO_EN	1 – write EXT_SENS_DATA registers associated to SLV_0 (as determined by I2C_SLV0_CTRL) to the FIFO at the sample rate; 0 – function is disabled

13.1.55 FIFO_EN_2

Name: FIFO_EN_2 Address: 103 (67h) Type: USR0 Bank: 0 Serial IF: R/W Reset Value: 0		
BIT	**NAME**	**FUNCTION**
7:5	-	Reserved
4	ACCEL_FIFO_EN	1 – write ACCEL_XOUT_H, ACCEL_XOUT_L, ACCEL_YOUT_H, ACCEL_YOUT_L, ACCEL_ZOUT_H, and ACCEL_ZOUT_L to the FIFO at the sample rate; 0 – function is disabled
3	GYRO_Z_FIFO_EN	1 – Write GYRO_ZOUT_H and GYRO_ZOUT_L to the FIFO at the sample rate 0 – function is disabled
2	GYRO_Y_FIFO_EN	1 – Write GYRO_YOUT_H and GYRO_YOUT_L to the FIFO at the sample rate 0 – function is disabled
1	GYRO_X_FIFO_EN	1 – Write GYRO_XOUT_H and GYRO_XOUT_L to the FIFO at the sample rate 0 – function is disabled
0	TEMP_FIFO_EN	1 – Write TEMP_OUT_H and TEMP_OUT_L to the FIFO at the sample rate 0 – function is disabled

13.1.56 FIFO_RST

Name: FIFO_RST

Address: 104 (68h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:5	-	Reserved
4:0	FIFO_RESET[4:0]	S/W FIFO reset.

13.1.57 FIFO_MODE

Name: FIFO_MODE
Address: 105 (69h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:5	-	Reserved
4:0	FIFO_MODE[4:0]	0 - Stream 1 - Snapshot When set to '1', when the FIFO is full, additional writes will not be written to FIFO. When set to '0', when the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data.

13.1.58 FIFO_COUNTH

Name: FIFO_COUNTH
Address: 112 (70h)
Type: USR0
Bank: 0
Serial IF: R
Reset Value: 0

BIT	NAME	FUNCTION
7:5	-	Reserved
4:0	FIFO_CNT[12:8]	High Bits, count indicates the number of written bytes in the FIFO. Reading this byte latches the data for both FIFO_COUNTH, and FIFO_COUNTL.

13.1.59 FIFO_COUNTL

Name: FIFO_COUNTL
Address: 113 (71h)
Type: USR0
Bank: 0
Serial IF: R

Reset Value: 0		
BIT	**NAME**	**FUNCTION**
7:0	FIFO_CNT[7:0]	Low bits, count indicates the number of written bytes in the FIFO.

13.1.60 FIFO_R_W

Name: FIFO_R_W
Address: 114 (72h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	FIFO_R_W[7:0]	Reading from or writing to this register actually reads/writes the FIFO. For example, to write a byte to the FIFO, write the desired byte value to FIFO_R_W[7:0]. To read a byte from the FIFO, perform a register read operation and access the result in FIFO_R_W[7:0].

13.1.61 DATA_RDY_STATUS

Name: DATA_RDY_STATUS
Address: 116 (74h)
Type: USR0
Bank: 0
Serial IF: R/C
Reset Value: 0

BIT	NAME	FUNCTION
7	WOF_STATUS	Wake on FSYNC interrupt status. Cleared on read.
6	WOM_STATUS	Wake on motion interrupt status. Cleared on read.
5:4	-	Reserved
3:0	RAW_DATA_RDY[3:0]	Data from sensors is copied to FIFO or SRAM. Set when sequence controller kicks off on a sensor data load. Only bit 0 is relevant in a single FIFO configuration. Cleared on read.

13.1.62 FIFO_CFG

Name: FIFO_CFG
Address: 118 (76h)
Type: USR0
Bank: 0
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:1	-	Reserved
0	FIFO_CFG	This bit should be set to 1 if interrupt status for each sensor is

		required.

13.1.63 REG_BANK_SEL

Name: REG_BANK_SEL
Address: 127 (7Fh)
Type: ALL
Bank: 0
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:6	-	Reserved
5:4	USER_BANK[1:0]	Use the following values in this bit-field to select a USER BANK 0: Select USER BANK 0 1: Select USER BANK 1 2: Select USER BANK 2 3: Select USER BANK 3
3:0	-	Reserved

13.2 USR Bank 1 Register Map

13.2.1 SELF_TEST_X_GYRO

Name: SELF_TEST_X_GYRO
Address: 2 (02h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	XG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

13.2.2 SELF_TEST_Y_GYRO

Name: SELF_TEST_Y_GYRO
Address: 3 (03h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	YG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

13.2.3 SELF_TEST_Z_GYRO

Name: SELF_TEST_Z_GYRO
Address: 4 (04h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	ZG_ST_DATA[7:0]	The value in this register indicates the self-test output generated during manufacturing tests. This value is to be used to check against subsequent self-test outputs performed by the end user.

13.2.4 SELF_TEST_X_ACCEL

Name: SELF_TEST_X_ACCEL
Address: 14 (0Eh)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	XA_ST_DATA[7:0]	Contains self-test data for the X Accelerometer.

13.2.5 SELF_TEST_Y_ACCEL

Name: SELF_TEST_Y_ACCEL
Address: 15 (0Fh)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	YA_ST_DATA[7:0]	Contains self-test data for the Y Accelerometer.

13.2.6 SELF_TEST_Z_ACCEL

Name: SELF_TEST_Z_ACCEL
Address: 16 (10h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	ZA_ST_DATA[7:0]	Contains self-test data for the Z Accelerometer.

13.2.7 XA_OFFS_H

Name: XA_OFFS_H

Address: 20 (14h) Type: USR1 Bank: 1 Serial IF: R/W Reset Value: Trimmed on a per-part basis for optimal performance		
BIT	**NAME**	**FUNCTION**
7:0	XA_OFFS[14:7]	Upper bits of the X accelerometer offset cancellation.

13.2.8 XA_OFFS_L

Name: XA_OFFS_L Address: 21 (15h) Type: USR1 Bank: 1 Serial IF: R/W Reset Value: Trimmed on a per-part basis for optimal performance		
BIT	**NAME**	**FUNCTION**
7:1	XA_OFFS[6:0]	Lower bits of the X accelerometer offset cancellation.
0	-	Reserved

13.2.9 YA_OFFS_H

Name: YA_OFFS_H Address: 23 (17h) Type: USR1 Bank: 1 Serial IF: R/W Reset Value: Trimmed on a per-part basis for optimal performance		
BIT	**NAME**	**FUNCTION**
7:0	YA_OFFS[14:7]	Upper bits of the Y accelerometer offset cancellation.

13.2.10 YA_OFFS_L

Name: YA_OFFS_L Address: 24 (18h) Type: USR1 Bank: 1 Serial IF: R/W Reset Value: Trimmed on a per-part basis for optimal performance		
BIT	**NAME**	**FUNCTION**
7:1	YA_OFFS[6:0]	Lower bits of the Y accelerometer offset cancellation.
0	-	Reserved

13.2.11 ZA_OFFS_H

Name: ZA_OFFS_H
Address: 26 (1Ah)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: Trimmed on a per-part basis for optimal performance

BIT	NAME	FUNCTION
7:0	ZA_OFFS[14:7]	Upper bits of the Z accelerometer offset cancellation.

13.2.12 ZA_OFFS_L

Name: ZA_OFFS_L
Address: 27 (1Bh)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: Trimmed on a per-part basis for optimal performance

BIT	NAME	FUNCTION
7:1	ZA_OFFS[6:0]	Lower bits of the Z accelerometer offset cancellation.
0	-	Reserved

13.2.13 TIMEBASE_CORRECTION_PLL

Name: TIMEBASE_CORRECTION_PLL
Address: 40 (28h)
Type: USR1
Bank: 1
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	TBC_PLL[7:0]	System PLL clock period error (signed, [-10%, +10%])

13.2.14 REG_BANK_SEL

Name: REG_BANK_SEL
Address: 127 (7Fh)
Type:
Bank: 1
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:6	-	Reserved
5:4	USER_BANK[1:0]	Use the following values in this bit-field to select a USER BANK

		0: Select USER BANK 0 1: Select USER BANK 1 2: Select USER BANK 2 3: Select USER BANK 3
3:0	-	Reserved

13.3 USR Bank 2 Register Map

13.3.1 GYRO_SMPLRT_DIV

Name: GYRO_SMPLRT_DIV
Address: 0 (00h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	GYRO_SMPLRT_DIV[7:0]	Gyro sample rate divider. Divides the internal sample rate to generate the sample rate that controls sensor data output rate, FIFO sample rate, and DMP sequence rate. NOTE: This register is only effective when FCHOICE = 1'b1 (FCHOICE_B register bit is 1'b0), and (0 < DLPF_CFG < 7). ODR is computed as follows: 1.1kHz/(1+GYRO_SMPLRT_DIV[7:0])

13.3.2 GYRO_CONFIG_1

Name: GYRO_CONFIG_1
Address: 1 (01h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 1

BIT	NAME	FUNCTION
7:6	-	Reserved
5:3	GYRO_DLPFCFG[2:0]	Gyro low pass filter configuration as shown in the table below
2:1	GYRO_FS_SEL[1:0]	Gyro Full Scale Select: 00 = ±250 dps 01= ±500 dps 10 = ±1000 dps 11 = ±2000 dps
0	GYRO_FCHOICE	0 – bypass gyro DLPF 1 – enable gyro DLPF

The gyroscope DLPF is configured by GYRO_DLPFCFG, when GYRO_FCHOICE = 1. The gyroscope data is filtered according to the value of GYRO_DLPFCFG and GYRO_FCHOICE as shown in the table below.

GYRO_FCHOICE	GYRO_DLPFCFG	Output		
		3dB BW [Hz]	NBW [Hz]	Rate [Hz]
0	x	12106	12316	9000
1	0	196.6	229.8	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	1	151.8	187.6	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	2	119.5	154.3	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	3	51.2	73.3	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	4	23.9	35.9	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	5	11.6	17.8	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	6	5.7	8.9	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255
1	7	361.4	376.5	1125/(1+GYRO_SMPLRT_DIV)Hz where GYRO_SMPLRT_DIV is 0, 1, 2,…255

13.3.3 GYRO_CONFIG_2

Name: GYRO_CONFIG_2
Address: 2 (02h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:6	-	Reserved
5	XGYRO_CTEN	X Gyro self-test enable
4	YGYRO_CTEN	Y Gyro self-test enable
3	ZGYRO_CTEN	Z Gyro self-test enable
2:0	GYRO_AVGCFG[2:0]	Averaging filter configuration settings for low-power mode 0: 1x averaging 1: 2x averaging 2: 4x averaging 3: 8x averaging 4: 16x averaging 5: 32x averaging 6: 64x averaging

		7: 128x averaging

The following table lists the gyroscope filter bandwidths available in the low-power mode of operation. In the low-power mode of operation, the gyroscope is duty-cycled.

	Averages	**1x**	**2x**	**4x**	**8x**	**16x**	**32x**	**64x**	**128x**
	GYRO_FCHOICE	1	1	1	1	1	1	1	1
	GYRO_AVGCFG	0	1	2	3	4	5	6	7
	Ton (ms)	1.15	1.59	2.48	4.26	7.82	14.93	29.15	57.59
	NBW (Hz)	773.5	469.8	257.8	134.8	68.9	34.8	17.5	8.8
GYRO_SMPLRT_DIV	**ODR (Hz)**	**Current Consumption [mA]**							
255	4.4	1.15	1.16	1.17	1.18	1.20	1.25	1.35	1.54
64	17.3	1.18	1.19	1.21	1.26	1.35	1.54	1.91	N/A
63	17.6	1.18	1.19	1.21	1.26	1.35	1.54	1.91	
32	34.1	1.21	1.23	1.27	1.36	1.55	1.91	N/A	
31	35.2	1.21	1.24	1.28	1.37	1.55	1.93		
16	66.2	1.26	1.30	1.39	1.57	1.92	N/A		
15	70.3	1.26	1.32	1.41	1.59	1.97			
10	102.3	1.29	1.41	1.58	1.80	2.50			
8	125.0	1.36	1.44	1.61	1.94	N/A			
7	140.6	1.39	1.49	1.66	2.04				
5	187.5	1.47	1.59	1.84	2.54				
4	225.0	1.58	1.69	2.12	N/A				
3	281.3	1.72	1.94	2.39					
2	375.0	1.94	2.24	N/A					
1	562.5	2.39	N/A						

Note 1: The current values shown above are TYP values.

Note 2: Ton is the ON time for motion measurement when the gyroscope is in duty cycle mode.

Note 3: The gyroscope current values shown above correspond to the default device configuration with LP_EN (bit 5 of register 0x06, USR bank 0) set to 0.

13.3.4 XG_OFFS_USRH

Name: XG_OFFS_USRH
Address: 3 (03h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	X_OFFS_USER[15:8]	Upper byte of X gyro offset cancellation

13.3.5 XG_OFFS_USRL

Name: XG_OFFS_USRL
Address: 4 (04h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	X_OFFS_USER[7:0]	Lower byte of X gyro offset cancellation

13.3.6 YG_OFFS_USRH

Name: YG_OFFS_USRH
Address: 5 (05h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	Y_OFFS_USER[15:8]	Upper byte of Y gyro offset cancellation

13.3.7 YG_OFFS_USRL

Name: YG_OFFS_USRL
Address: 6 (06h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	Y_OFFS_USER[7:0]	Lower byte of Y gyro offset cancellation

13.3.8 ZG_OFFS_USRH

Name: ZG_OFFS_USRH

Address: 7 (07h) Type: USR2 Bank: 2 Serial IF: R/W Reset Value: 0		
BIT	**NAME**	**FUNCTION**
7:0	Z_OFFS_USER[15:8]	Upper byte of Z gyro offset cancellation

13.3.9 ZG_OFFS_USRL

Name: ZG_OFFS_USRL Address: 8 (08h) Type: USR2 Bank: 2 Serial IF: R/W Reset Value: 0		
BIT	**NAME**	**FUNCTION**
7:0	Z_OFFS_USER[7:0]	Lower byte of Z gyro offset cancellation

13.3.10 ACCEL_SMPLRT_DIV_1

Name: ACCEL_SMPLRT_DIV_1 Address: 16 (10h) Type: USR2 Bank: 2 Serial IF: R/W Reset Value: 0		
BIT	**NAME**	**FUNCTION**
7:4	-	Reserved
3:0	ACCEL_SMPLRT_DIV[11:8]	MSB for ACCEL sample rate div

13.3.11 ACCEL_SMPLRT_DIV_2

Name: ACCEL_SMPLRT_DIV_2 Address: 17 (11h) Type: USR2 Bank: 2 Serial IF: R/W Reset Value: 0		
BIT	**NAME**	**FUNCTION**
7:0	ACCEL_SMPLRT_DIV[7:0]	LSB for ACCEL sample rate div ODR is computed as follows: 1.125kHz/(1+ACCEL_SMPLRT_DIV[11:0])

13.3.12 ACCEL_INTEL_CTRL

Name: ACCEL_INTEL_CTRL
Address: 18 (12h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:2	-	Reserved
1	ACCEL_INTEL_EN	Enable the WOM logic
0	ACCEL_INTEL_MODE_INT	Selects WOM algorithm 1 = Compare the current sample with the previous sample. 0 = Initial sample is stored, all future samples are compared to the initial sample

13.3.13 ACCEL_WOM_THR

Name: ACCEL_WOM_THR
Address: 19 (13h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	WOM_THRESHOLD[7:0]	This register holds the threshold value for the Wake on Motion Interrupt for ACCEL x/y/z axes. LSB = 4mg. Range is 0mg to 1020mg

13.3.14 ACCEL_CONFIG

Name: ACCEL_CONFIG
Address: 20 (14h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 1

BIT	NAME	FUNCTION
7:6	-	Reserved
5:3	ACCEL_DLPFCFG[2:0]	Accelerometer low pass filter configuration as shown in the table below
2:1	ACCEL_FS_SEL[1:0]	Accelerometer Full Scale Select: 00: ±2g 01: ±4g 10: ±8g 11: ±16g
0	ACCEL_FCHOICE	0: bypass accel DLPF 1: enable accel DLPF

ACCEL_FCHOICE	ACCEL_DLPFCFG	Output		
		3dB BW [Hz]	NBW [Hz]	Rate [Hz]
0	x	1209	1248	4500
1	0	246.0	265.0	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…255
1	1	246.0	265.0	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…255
1	2	111.4	136.0	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…255
1	3	50.4	68.8	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…255
1	4	23.9	34.4	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…255
1	5	11.5	17.0	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…255
1	6	5.7	8.3	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…255
1	7	473	499	1125/(1+ACCEL_SMPLRT_DIV)Hz where ACCEL_SMPLRT_DIV is 0, 1, 2,…255

The data rate out of the DLPF filter block can be further reduced by a factor of 1.125kHz/(1+ACCEL_SMPLRT_DIV[11:0]) where ACCEL_SMPLRT_DIV is a 12-bit integer.

13.3.15 ACCEL_CONFIG_2

Name: ACCEL_CONFIG_2
Address: 21 (15h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:5	-	Reserved
4	AX_ST_EN_REG	X Accel self-test enable
3	AY_ST_EN_REG	Y Accel self-test enable
2	AZ_ST_EN_REG	Z Accel self-test enable
1:0	DEC3_CFG[1:0]	Controls the number of samples averaged in the accelerometer decimator: 0: average 1 or 4 samples depending on ACCEL_FCHOICE (see table below)

		1: average 8 samples 2: average 16 samples 3: average 32 samples

The following table lists the accelerometer filter bandwidths available in the low-power mode of operation. In the low-power mode of operation, the accelerometer is duty-cycled.

	Averages	**1x**	**4x**	**8x**	**16x**	**32x**
	ACCEL_FCHOICE	0	1	1	1	1
	ACCEL_DLPFCFG	x	7	7	7	7
	DEC3_CFG	0	0	1	2	3
	Ton (ms)	0.821	1.488	2.377	4.154	7.71
	NBW (Hz)	1237.5	496.8	264.8	136.5	69.2
ACCEL_SMPLRT_DIV	**ODR [Hz]**	**Current Consumption [µA]**				
4095	0.27	222.9	223.1	223.3	223.9	224.9
2044	0.55	223.0	223.2	223.4	223.9	225.0
1022	1.1	223.2	223.6	224.1	225.0	227.1
513	2.19	223.6	224.3	225.3	227.3	231.5
255	4.4	224.2	225.6	227.7	231.7	240.2
127	8.79	225.8	228.5	232.4	240.2	255.5
63	17.6	229.0	234.7	242.0	258.7	288.3
31	35.2	235.1	246.5	261.6	291.6	351.9
15	70.3	247.8	270.1	299.9	360.4	480.4
10	102	252.0	291.3	335.3	433.0	612.0
7	141	272.6	317.5	377.5	497.4	N/A
3	281	322.4	412.2	N/A		
1	563	422.1	N/A			

Note 1: The current values shown above are TYP values.

Note 2: Ton is the ON time for motion measurement when the accelerometer is in duty cycle mode.

Note 3: The accelerometer current values shown above correspond to the default device configuration with LP_EN (bit 5 of register 0x06, USR bank 0) set to 0.

13.3.16 FSYNC_CONFIG

Name: FSYNC_CONFIG
Address: 82 (52h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0

BIT	**NAME**	**FUNCTION**

5	WOF_DEGLITCH_EN	Enable digital deglitching of FSYNC input for Wake on FSYNC.
4	WOF_EDGE_INT	0: FSYNC is a level interrupt for Wake on FSYNC 1: FSYNC is an edge interrupt for Wake on FSYNC actl_fsync is used to set the polarity of the interrupt
3:0	EXT_SYNC_SET[3:0]	Enables the FSYNC pin data to be sampled. EXT_SYNC_SET FSYNC bit location 0: Function disabled 1: TEMP_OUT_L[0] 2: GYRO_XOUT_L[0] 3: GYRO_YOUT_L[0] 4: GYRO_ZOUT_L[0] 5: ACCEL_XOUT_L[0] 6: ACCEL_YOUT_L[0] 7: ACCEL_ZOUT_L[0]

13.3.17 TEMP_CONFIG

Name: TEMP_CONFIG
Address: 83 (53h)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
2:0	TEMP_DLPFCFG[2:0]	Low pass filter configuration for temperature sensor as shown in the table below:

TEMP_DLPCFG<2:0>	Temp Sensor	
	NBW (Hz)	Rate (kHz)
0	7932.0	9
1	217.9	1.125
2	123.5	1.125
3	65.9	1.125
4	34.1	1.125
5	17.3	1.125
6	8.8	Rate (kHz)
7	7932.0	9

13.3.18 MOD_CTRL_USR

Name: MOD_CTRL_USR
Address: 84 (54h)
Type: USR2
Bank: 2
Serial IF: R/W

Reset Value: 11		
BIT	**NAME**	**FUNCTION**
7:1	-	Reserved
0	REG_LP_DMP_EN	Enable turning on DMP in Low Power Accelerometer mode. Note that DMP still needs to be globally enabled in MOD_CTRL and USER_CTRL registers.

13.3.19 REG_BANK_SEL

Name: REG_BANK_SEL
Address: 127 (7Fh)
Type: USR2
Bank: 2
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:6	-	Reserved
5:4	USER_BANK[1:0]	Use the following values in this bit-field to select a USER BANK 0: Select USER BANK 0 1: Select USER BANK 1 2: Select USER BANK 2 3: Select USER BANK 3
3:0	-	Reserved

13.4 USR Bank 3 Register Map

13.4.1 I2C_MST_ODR_CONFIG

Name: I2C_MST_ODR_CONFIG
Address: 0 (00h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	I2C_MST_ODR_CONFIG[3:0]	ODR configuration for external sensor when gyroscope and accelerometer are disabled. ODR is computed as follows: 1.1kHz/(2^((odr_config[3:0]))) When gyroscope is enabled, all sensors (including I2C_MASTER) use the gyroscope ODR. If gyroscope is disabled then all sensors (including I2C_MASTER) use the accelerometer ODR.

13.4.2 I2C_MST_CTRL

Name: I2C_MST_CTRL

Address: 1 (01h) **Type: USR3** **Bank: 3** **Serial IF: R/W** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7	MULT_MST_EN	Enables multi-master capability. When disabled, clocking to the I2C_MST_IF can be disabled when not in use and the logic to detect lost arbitration is disabled.
6:5	-	Reserved
4	I2C_MST_P_NSR	This bit controls the I2C Master's transition from one slave read to the next slave read. 0 - there is a restart between reads. 1 - there is a stop between reads.
3:0	I2C_MST_CLK[3:0]	Sets I2C master clock frequency as shown in the table below

I2C_MST_CLK	Nominal CLK Frequency [kHz]	Duty Cycle
0	370.29	50.00%
1	-	-
2	370.29	50.00%
3	432.00	50.00%
4	370.29	42.86%
5	370.29	50.00%
6	345.60	40.00%
7	345.60	46.67%
8	304.94	47.06%
9	432.00	50.00%
10	432.00	41.67%
11	432.00	41.67%
12	471.27	45.45%
13	432.00	50.00%
14	345.60	46.67%
15	345.60	46.67%

13.4.3 I2C_MST_DELAY_CTRL

Name: I2C_MST_DELAY_CTRL
Address: 2 (02h)
Type: USR3

Bank: 3 Serial IF: R/W Reset Value: 0		
BIT	**NAME**	**FUNCTION**
7	DELAY_ES_SHADOW	Delays shadowing of external sensor data until all data is received
6:5	-	Reserved
4	I2C_SLV4_DELAY_EN	When enabled, slave 4 will only be accessed 1/(1+I2C_SLC4_DLY) samples as determined by I2C_MST_ODR_CONFIG
3	I2C_SLV3_DELAY_EN	When enabled, slave 3 will only be accessed 1/(1+I2C_SLC4_DLY) samples as determined by I2C_MST_ODR_CONFIG
2	I2C_SLV2_DELAY_EN	When enabled, slave 2 will only be accessed 1/(1+I2C_SLC4_DLY) samples as determined by I2C_MST_ODR_CONFIG
1	I2C_SLV1_DELAY_EN	When enabled, slave 1 will only be accessed 1/(1+I2C_SLC4_DLY) samples as determined by I2C_MST_ODR_CONFIG
0	I2C_SLV0_DELAY_EN	When enabled, slave 0 will only be accessed 1/(1+I2C_SLC4_DLY) samples as determined by I2C_MST_ODR_CONFIG

13.4.4 I2C_SLV0_ADDR

Name: I2C_SLV0_ADDR Address: 3 (03h) Type: USR3 Bank: 3 Serial IF: R/W Reset Value: 0		
BIT	**NAME**	**FUNCTION**
7	I2C_SLV0_RNW	1 – Transfer is a read 0 – Transfer is a write
6:0	I2C_ID_0[6:0]	Physical address of I2C slave 0

13.4.5 I2C_SLV0_REG

Name: I2C_SLV0_REG Address: 4 (04h) Type: USR3 Bank: 3 Serial IF: R/W Reset Value: 0		
BIT	**NAME**	**FUNCTION**
7:0	I2C_SLV0_REG[7:0]	I2C slave 0 register address from where to begin data transfer

13.4.6 I2C_SLV0_CTRL

Name: I2C_SLV0_CTRL Address: 5 (05h)

Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7	I2C_SLV0_EN	1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register, which is always EXT_SENS_DATA_00 for I2C slave 0. 0 – function is disabled for this slave
6	I2C_SLV0_BYTE_SW	1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV0_REG[0] = 1, or if the last byte read has a register address lsb = 0. For example, if I2C_SLV0_REG = 0x1, and I2C_SLV0_LENG = 0x4: 1) The first byte read from address 0x1 will be stored at EXT_SENS_DATA_00, 2) the second and third bytes will be read and swapped, so the data read from address 0x2 will be stored at EXT_SENS_DATA_02, and the data read from address 0x3 will be stored at EXT_SENS_DATA_01, 3) The last byte read from address 0x4 will be stored at EXT_SENS_DATA_03 0 – no swapping occurs, bytes are written in order read.
5	I2C_SLV0_REG_DIS	When set, the transaction does not write a register value, it will only read data, or write data
4	I2C_SLV0_GRP	External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc.., or if the groups are address 1 and 2, 3 and 4, etc.. 0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address.
3:0	I2C_SLV0_LENG[3:0]	Number of bytes to be read from I2C slave 0

13.4.7 I2C_SLV0_DO

Name: I2C_SLV0_DO
Address: 6 (06h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	I2C_SLV0_DO[7:0]	Data out when slave 0 is set to write

13.4.8 I2C_SLV1_ADDR

Name: I2C_SLV1_ADDR
Address: 7 (07h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7	I2C_SLV1_RNW	1 – Transfer is a read 0 – Transfer is a write
6:0	I2C_ID_1[6:0]	Physical address of I2C slave 1

13.4.9 I2C_SLV1_REG

Name: I2C_SLV1_REG
Address: 8 (08h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	I2C_SLV1_REG[7:0]	I2C slave 1 register address from where to begin data transfer

13.4.10 I2C_SLV1_CTRL

Name: I2C_SLV1_CTRL
Address: 9 (09h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7	I2C_SLV1_EN	1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register as determined by I2C_SLV0_EN and I2C_SLV0_LENG. 0 – function is disabled for this slave
6	I2C_SLV1_BYTE_SW	1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV1_REG[0] = 1, or if the last byte read has a register address lsb = 0. For example, if I2C_SLV0_EN = 0x1, and I2C_SLV0_LENG = 0x3 (to show swap has to do with I2C slave address not EXT_SENS_DATA address), and if I2C_SLV1_REG = 0x1, and I2C_SLV1_LENG = 0x4: 1) The first byte read from address 0x1 will be stored at EXT_SENS_DATA_03 (slave 0's data will be in EXT_SENS_DATA_00, EXT_SENS_DATA_01, and

		EXT_SENS_DATA_02), 2) the second and third bytes will be read and swapped, so the data read from address 0x2 will be stored at EXT_SENS_DATA_04, and the data read from address 0x3 will be stored at EXT_SENS_DATA_05, 3) The last byte read from address 0x4 will be stored at EXT_SENS_DATA_06 0 – no swapping occurs, bytes are written in order read.
5	I2C_SLV1_REG_DIS	When set, the transaction does not write a register value, it will only read data, or write data
4	I2C_SLV1_GRP	External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc.., or if the groups are address 1 and 2, 3 and 4, etc.. 0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address.
3:0	I2C_SLV1_LENG[3:0]	Number of bytes to be read from I2C slave 1

13.4.11 I2C_SLV1_DO

Name: I2C_SLV1_DO
Address: 10 (0Ah)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	I2C_SLV1_DO[7:0]	Data out when slave 1 is set to write

13.4.12 I2C_SLV2_ADDR

Name: I2C_SLV2_ADDR
Address: 11 (0Bh)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7	I2C_SLV2_RNW	1 – Transfer is a read 0 – Transfer is a write
6:0	I2C_ID_2[6:0]	Physical address of I2C slave 2

13.4.13 I2C_SLV2_REG

Name: I2C_SLV2_REG

Address: 12 (0Ch) **Type: USR3** **Bank: 3** **Serial IF: R/W** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:0	I2C_SLV2_REG[7:0]	I2C slave 2 register address from where to begin data transfer

13.4.14 I2C_SLV2_CTRL

Name: I2C_SLV2_CTRL **Address: 13 (0Dh)** **Type: USR3** **Bank: 3** **Serial IF: R/W** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7	I2C_SLV2_EN	1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register as determined by I2C_SLV0_EN, I2C_SLV0_LENG, I2C_SLV1_EN and I2C_SLV1_LENG. 0 – function is disabled for this slave
6	I2C_SLV2_BYTE_SW	1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV2_REG[0] = 1, or if the last byte read has a register address lsb = 0. See I2C_SLV1_CTRL for an example. 0 – no swapping occurs, bytes are written in order read.
5	I2C_SLV2_REG_DIS	When set, the transaction does not write a register value, it will only read data, or write data
4	I2C_SLV2_GRP	External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc.., or if the groups are address 1 and 2, 3 and 4, etc.. 0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address.
3:0	I2C_SLV2_LENG[3:0]	Number of bytes to be read from I2C slave 2

13.4.15 I2C_SLV2_DO

Name: I2C_SLV2_DO **Address: 14 (0Eh)** **Type: USR3** **Bank: 3**

Serial IF: R/W **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:0	I2C_SLV2_DO[7:0]	Data out when slave 2 is set to write

13.4.16 I2C_SLV3_ADDR

Name: I2C_SLV3_ADDR **Address: 15 (0Fh)** **Type: USR3** **Bank: 3** **Serial IF: R/W** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7	I2C_SLV3_RNW	1 – Transfer is a read 0 – Transfer is a write
6:0	I2C_ID_3[6:0]	Physical address of I2C slave 3

13.4.17 I2C_SLV3_REG

Name: I2C_SLV3_REG **Address: 16 (10h)** **Type: USR3** **Bank: 3** **Serial IF: R/W** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:0	I2C_SLV3_REG[7:0]	I2C slave 3 register address from where to begin data transfer

13.4.18 I2C_SLV3_CTRL

Name: I2C_SLV3_CTRL **Address: 17 (11h)** **Type: USR3** **Bank: 3** **Serial IF: R/W** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7	I2C_SLV3_EN	1 – Enable reading data from this slave at the sample rate and storing data at the first available EXT_SENS_DATA register as determined by I2C_SLV0_EN, I2C_SLV0_LENG, I2C_SLV1_EN, I2C_SLV1_LENG, I2C_SLV2_EN and I2C_SLV2_LENG. 0 – function is disabled for this slave
6	I2C_SLV3_BYTE_SW	1 – Swap bytes when reading both the low and high byte of a word. Note there is nothing to swap after reading the first byte if I2C_SLV3_REG[0] = 1, or if the last byte read has a register address lsb = 0.

		See I2C_SLV1_CTRL for an example. 0 – no swapping occurs, bytes are written in order read.
5	I2C_SLV3_REG_DIS	When set, the transaction does not write a register value, it will only read data, or write data
4	I2C_SLV3_GRP	External sensor data typically comes in as groups of two bytes. This bit is used to determine if the groups are from the slave's register address 0 and 1, 2 and 3, etc.., or if the groups are address 1 and 2, 3 and 4, etc.. 0 indicates slave register addresses 0 and 1 are grouped together (odd numbered register ends the group). 1 indicates slave register addresses 1 and 2 are grouped together (even numbered register ends the group). This allows byte swapping of registers that are grouped starting at any address.
3:0	I2C_SLV3_LENG[3:0]	Number of bytes to be read from I2C slave 3

13.4.19 I2C_SLV3_DO

Name: I2C_SLV3_DO
Address: 18 (12h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:0	I2C_SLV3_DO[7:0]	Data out when slave 3 is set to write

13.4.20 I2C_SLV4_ADDR

Name: I2C_SLV4_ADDR
Address: 19 (13h)
Type: USR3
Bank: 3
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7	I2C_SLV4_RNW	1 – Transfer is a read 0 – Transfer is a write
6:0	I2C_ID_4[6:0]	Physical address of I2C slave 4

Note: The I^2C Slave 4 interface can be used to perform only single byte read and write transactions.

13.4.21 I2C_SLV4_REG

Name: I2C_SLV4_REG
Address: 20 (14h)
Type: USR3
Bank: 3

Serial IF: R/W **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:0	I2C_SLV4_REG[7:0]	I2C slave 4 register address from where to begin data transfer

13.4.22 I2C_SLV4_CTRL

Name: I2C_SLV4_CTRL **Address: 21 (15h)** **Type: USR3** **Bank: 3** **Serial IF: R/W** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7	I2C_SLV4_EN	1 – Enable data transfer with this slave at the sample rate. If read command, store data in I2C_SLV4_DI register, if write command, write data stored in I2C_SLV4_DO register. Bit is cleared when a single transfer is complete. Be sure to write I2C_SLV4_DO first 0 – function is disabled for this slave
6	I2C_SLV4_INT_EN	1 – Enables the completion of the I2C slave 4 data transfer to cause an interrupt. 0 – Completion of the I2C slave 4 data transfer will not cause an interrupt.
5	I2C_SLV4_REG_DIS	When set, the transaction does not write a register value, it will only read data, or write data
4:0	I2C_SLV4_DLY[4:0]	When enabled via the I2C_MST_DELAY_CTRL, those slaves will only be enabled every1/(1+I2C_SLV4_DLY) samples as determined by I2C_MST_ODR_CONFIG

13.4.23 I2C_SLV4_DO

Name: I2C_SLV4_DO **Address: 22 (16h)** **Type: USR3** **Bank: 3** **Serial IF: R/W** **Reset Value: 0**		
BIT	**NAME**	**FUNCTION**
7:0	I2C_SLV4_DO[7:0]	Data out when slave 4 is set to write

13.4.24 I2C_SLV4_DI

Name: I2C_SLV4_DI **Address: 23 (17h)** **Type: USR3** **Bank: 3** **Serial IF: R** **Reset Value: 0**

BIT	NAME	FUNCTION
7:0	I2C_SLV4_DI[7:0]	Data read from I2C Slave 4.

13.4.25 REG_BANK_SEL

Name: REG_BANK_SEL
Address: 127 (7Fh)
Type:
Bank: 3
Serial IF: R/W
Reset Value: 0

BIT	NAME	FUNCTION
7:6	-	Reserved
5:4	USER_BANK[1:0]	Use the following values in this bit-field to select a USER BANK 0: Select USER BANK 0 1: Select USER BANK 1 2: Select USER BANK 2 3: Select USER BANK 3
3:0	-	Reserved

14 References

Please refer to “InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)” for the following information:

- Manufacturing Recommendations
    - Assembly Guidelines and Recommendations
    - PCB Design Guidelines and Recommendations
    - MEMS Handling Instructions
    - ESD Considerations
    - Reflow Specification
    - Storage Specifications
    - Package Marking Specification
    - Tape & Reel Specification
    - Reel & Pizza Box Label
    - Packaging
    - Representative Shipping Carton Label
- Compliance
    - Environmental Compliance
    - DRC Compliance
    - Compliance Declaration Disclaimer