CE/CZ3001: Advanced Computer Architecture:

Tutorial-6

1. A processor has a 32 byte memory and an 8 byte direct-mapped cache. Size of each block in cache and main memory is 1 byte. Table 1 shows the current state of the cache and Table II shows a sequence of memory references. Write hit or miss under the each address in the memory reference sequence below.

Table 1: current stage of cache

Index	V	Tag	Data
000	N		
001	Y	00	Mem(00001)
010	N		
011	Y	11	Mem(11011)
100	Y	10	Mem(10100)
101	Y	01	Mem(01101)
110	Y	00	Mem(00110)
111	N		

Table 2: Memory reference sequence

Addr	10011	00001	00110	01010	01110	11001	00001	11100	10100
H/M									

(Answer: M, H, H, M, M, M, M, M, M)

2. Assume the following sequence of 8-bit addresses generated by the microprocessor as given in Table 1. The cache size is 16 bytes and block size is 4 bytes. Assume a 2-way set associative cache design that uses the LRU algorithm. Assume that the cache is initially empty. First determine the TAG, INDEX, OFFSET fields and fill in the table above. In the figure below, clearly mark for each access the TAG, Least Recently Used (LRU), and HIT/MISS information for each access.

Time	0	1	2	3	4	5	6	7
Access	10001101	10110010	10111111	10001100	10011100	11101001	11111110	11101001
TAG								
OFFSET								
INDEX								

(Answer: hit rate 25%)