CE/CZ3001: Advanced Computer Architecture:

Tutorial-7

1. Let the CPI required by a processor for a given program is 1.25 for memory system having 100% hit-rate in L1 data cache. Assume that the program has 20% of load/store instructions and the access to the instruction cache is ideal (100% hit rate).

   a) Estimate the CPI required by the same processor with a different memory system for the same program having the following memory access specifications:
      a. For L1 data cache
         1) 20% miss rate
         2) 8 cycle miss penalty
      b. For L2 data cache
         1) 10% miss rate
         2) 30 cycle miss penalty
   b) Compare this to the CPI of the same processor with another memory system, without an L2 data cache (every miss from L1 data cache goes to main memory) and miss penalty=30 cycles.

   (Answer: a) CPI=1.69, b) CPI =2.45)

2. Suppose a machine adopts always-untaken as branch prediction technique, and the branch frequencies (as percentages of all instructions) are as follows:
   - Conditional branches 15%
   - Jumps and Calls 1%

   Among all conditional branches, 60% are taken, 40% not taken.
   We are examining a 4-stage pipeline where the branch is resolved at the end of the 2nd stage for Jumps and Calls and at the end of the 3rd stage for conditional branches. Ignoring other pipeline stalls, what is the CPI of this machine?

   (Answer: CPI=1.19)