CE/CZ3001: Advanced Computer Architecture:

Tutorial-4

1. In this exercise, we examine how pipelining affects the clock cycle time of the processor. Assume that individual stages of the data path have the following latencies:

IF	ID	EX	MEM	WB
300ps	400ps	350ps	500ps	100ps

   a) What is the minimum possible period of clock signal in a pipelined and a nonpipelined processor?
   b) What is the total latency (in picoseconds) of LDUR instruction in a pipelined and nonpipelined processor?
   c) If we split one stage of the pipelined datapath into two stages, each with nearly half the latency of the original stage, which stage would you like to split and what is the minimum clock period of the new pipelined processor?
   d) Assume the following distribution of instructions executed by the processor:

ALU	CBZ	LDUR	STUR
50%	25%	15%	10%

      1) If there are no stalls, what is the utilization (in terms of % of clock cycles used) of the data memory?
      2) What is the percentage of utilization of the write-register port of the Register file of the processor?

   (Answer: a) 500ps for pipelined, 1650ps for nonpipelined, b) 2500ps for pipelined, 1650ps for nonpipelined, c) longest delay 500ps (MEM) should be split, the new cycle time is 400ps, d) 1) 25%, 2) 65%

2. Spot all data dependencies (including the ones that do not lead to stalls). Draw arrows from the stages where data is made available, directed to where it is needed. Circle the associated registers in the instructions.
   a) Assume no forwarding. Note that write-back operations and the decode operations of different instructions can happen in the same clock cycle. One dependency is shown below. You need to show the remaining dependencies. How many stalls are required to resolve the hazards?
   b) If data forwarding is allowed, how many stalls are required to resolve the hazards?
   c) Find the steady state CPI for the designs of no forwarding and with forwarding assuming the given instructions sequence is repeated very large number of times?

ADDI X0, X1, #100	F	D	E	M	WB					
LDUR X2, [X0, #8]		F	D	E	M	WB				
ADD X3, X1, X2			F	D	E	M	WB			
STUR X3, [X0, #8]				F	D	E	M	WB		
LDUR X5, [X6, #0]					F	D	E	M	WB	
ORR X5, X0, X3						F	D	E	M	WB

(Answer: a) 6, b) 1 cycle, c) 2 in “no forwarding” case and 1.16 in “full forwarding” case)

3. Consider an instruction sequence: A, B, C, D, E, F, G, H. Figure 1 shows the dependencies in this instruction sequence, where each arrow represents true data dependence. There are two 2-way superscalar machines, P1 and P2. (i.e. at most 2 instructions can be issued at the same time). P1 is an in-order machine (no instruction can start before a preceding instruction starts), and P2 is an out-of-order machine (instructions can execute in any order as long as data dependencies are honored.

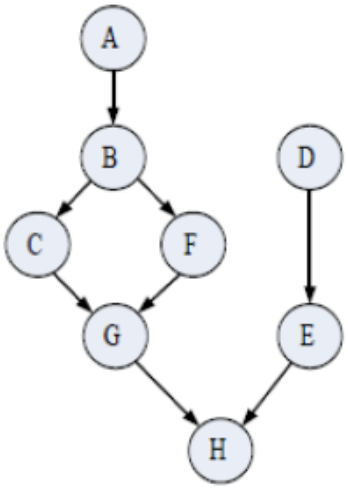

Figure 1: dependence diagram

a) Show the instruction schedules for both computers in the given table. The time in the table is represented by the number of cycles that have passed; lane 1 and lane 2 represent the two-lanes for the superscalar data path, where only lane 1 is used if only 1 of two possible instructions is issued.
b) What is the speedup of P2 over P1 for this instruction sequence?

(Answer: a) , b) 1.2)