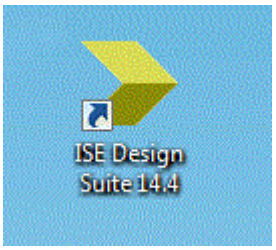
I. Starting ISE Software

To start ISE, **double-click the desktop icon**



Or go to, **Start --- All Programs --- Xilinx Design Tools --- ISE Design Suite 14.4 --- ISE Design Tools --- 64-bit Project Navigator**

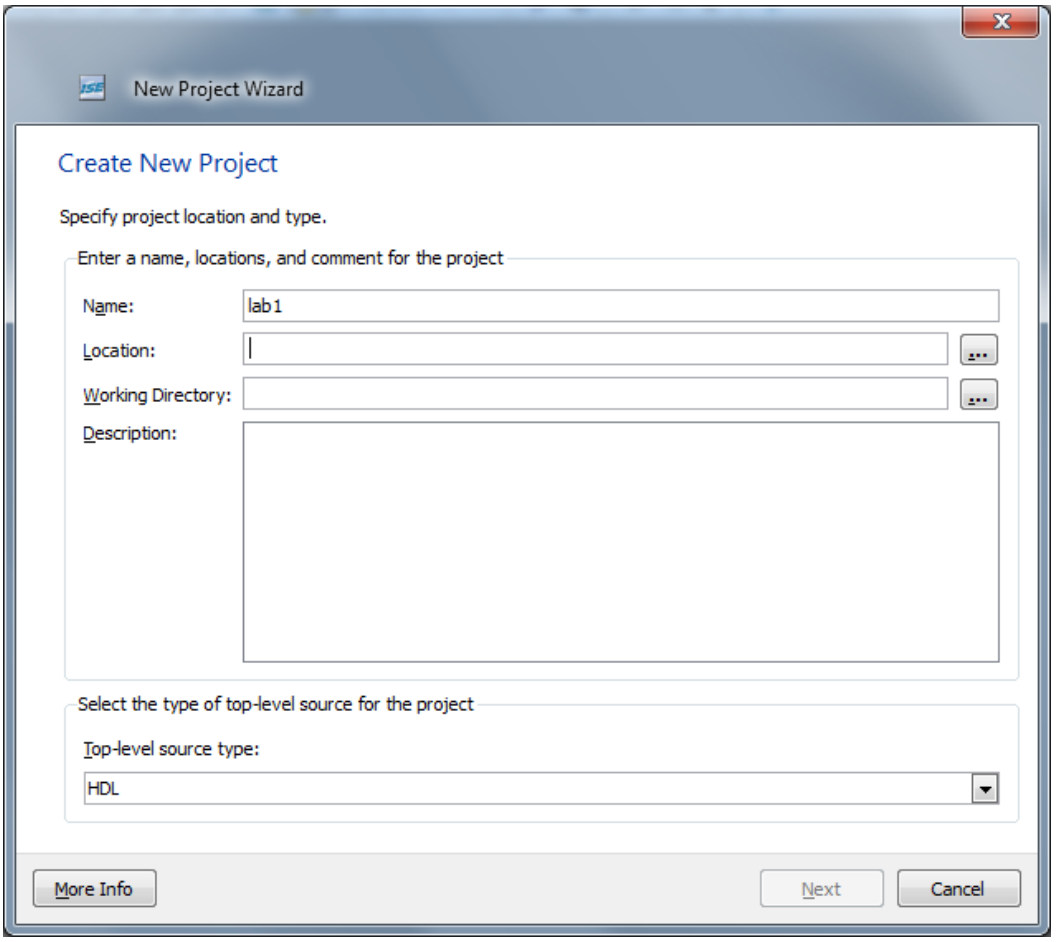
II. Create ı New Project

To create a new ISE project **Select File > New Project.** The page *Create New*

Project appears

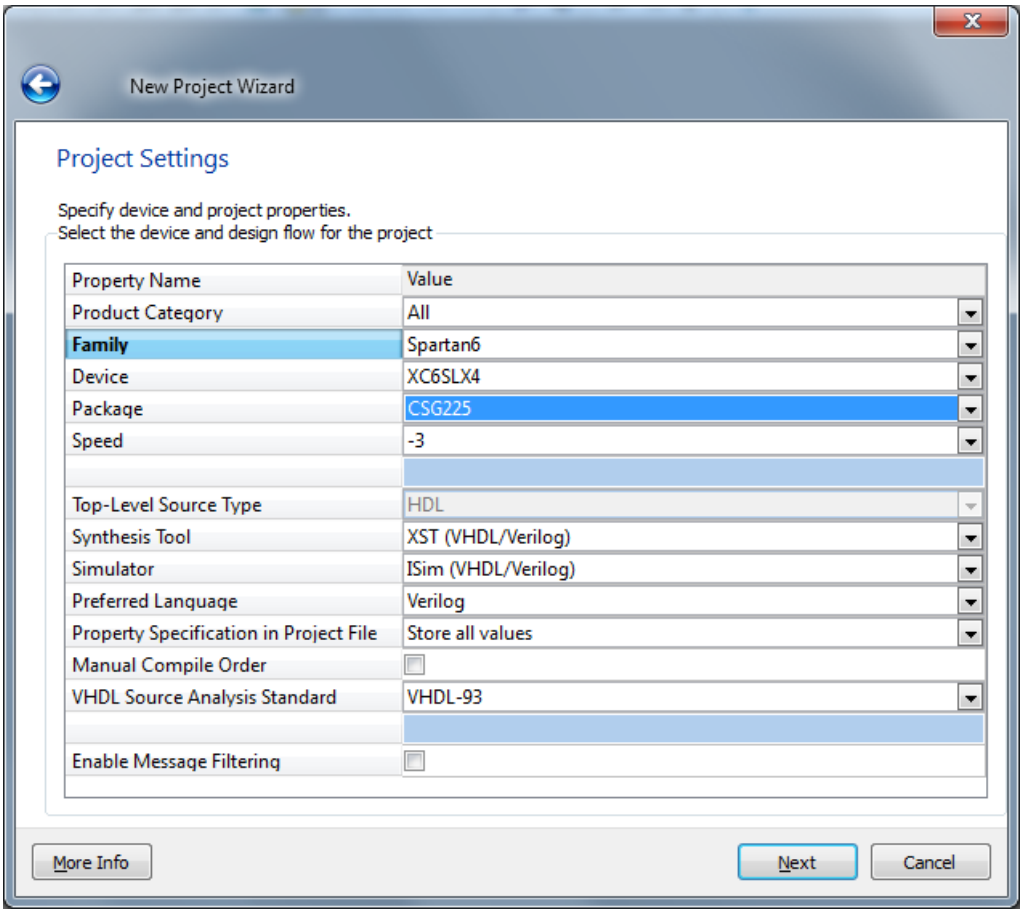
A Create New Project page

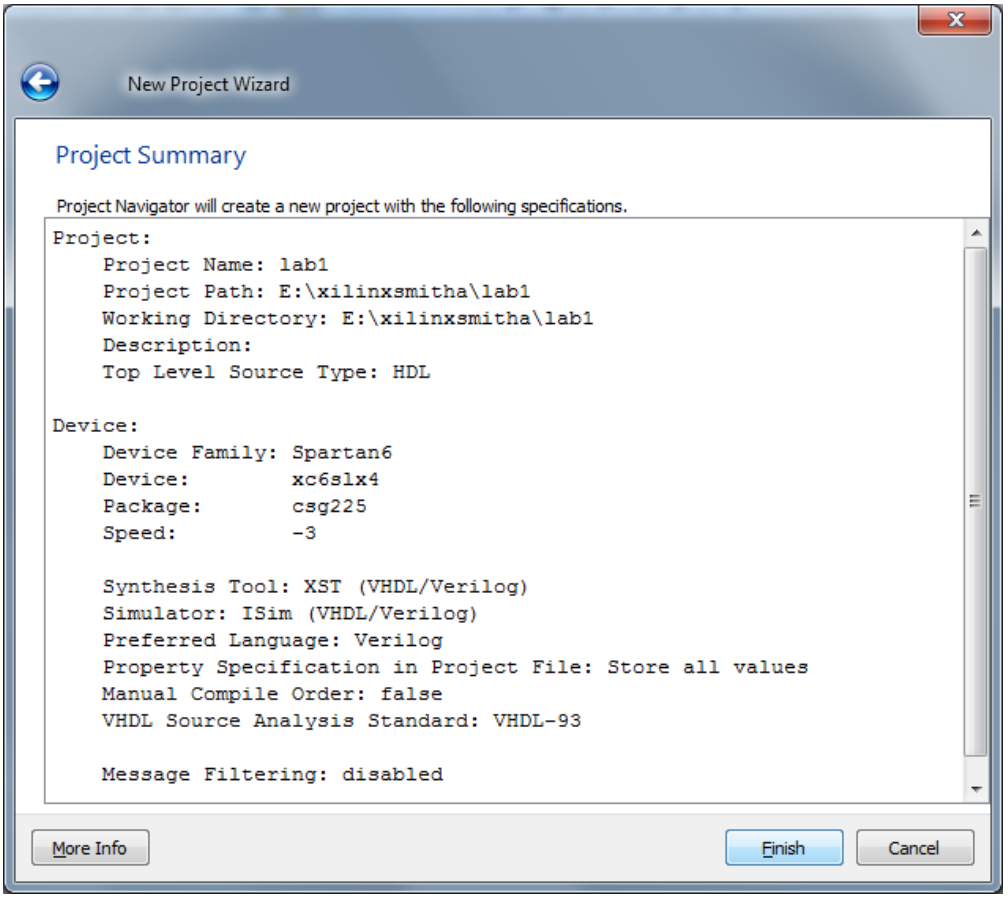
1. In the field Project ***Name***, type **lab1**
   - You can choose another name that does not contain any white spaces
2. In the field Project ***Location***, browse to a location (directory path) for the new project
   - If you use **Window**, browse to a directory under your **Nest drive**
3. In the field ***Top-level source type*****, select > *HDL***
4. **Click > *Next*** to move to the page ***Project Settings***



B Project Settings page

1. In the field **family, select >Spartan6**
2. In the field ***device,* Select > *XC6SLX4***
3. In the field ***package,* Select > *CSG225***
4. In the field ***speed,* Select > *-3***
5. In the field ***Simulator*, Select > *ISim(VHDL/Verilog)***
6. In the field ***Preferred Language*, Select > *Verilog***
7. **Click > *Next*** to move to the page ***Project Summary***
5. **Click > *Finish*** in the page ***Project Summary***





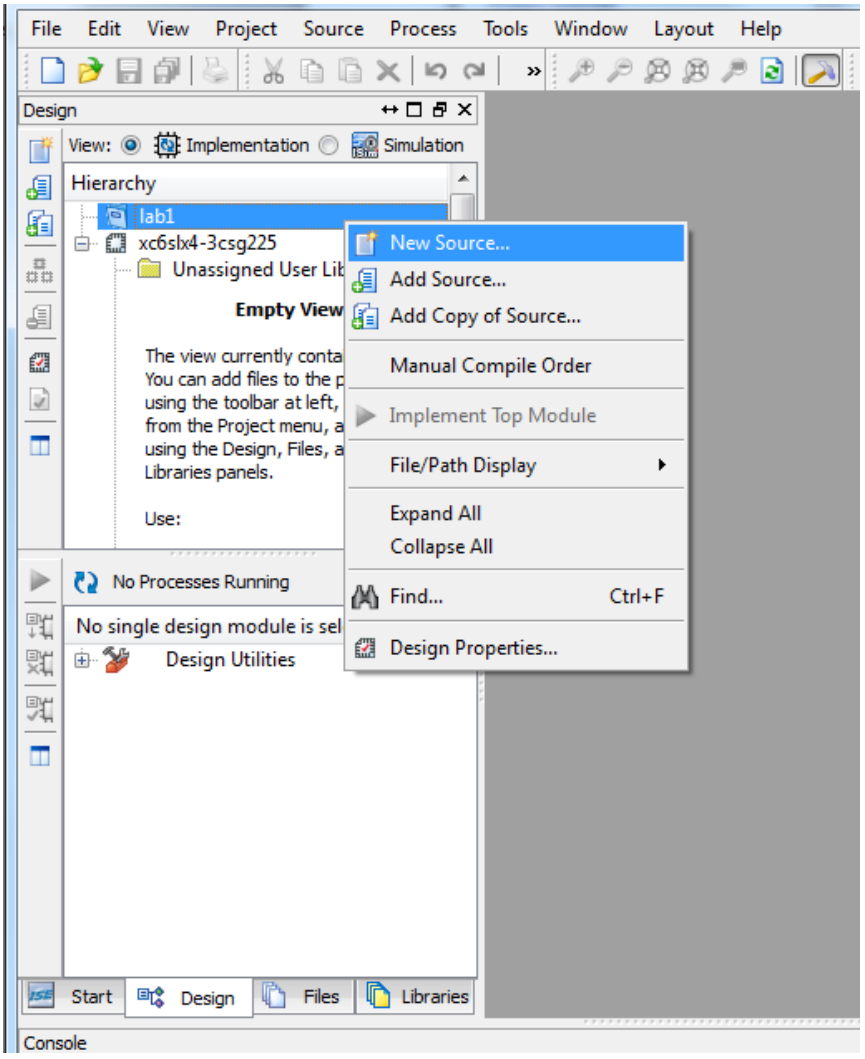
III. Create a New Design

To study how to create a new design, we will design in this section a 2- Input X-OR Gate. The X-OR Function is defined as:

Y = A1 xor B1 = A1'B1+ A1B1'

A Create a HDL Source

1. In ***ISE Design Suite*** that appears on the left side of ISE, click on the***Design*** Tab to go to the ***Design Panel***
2. In the ***Design Panel***, **right-click** on the icon ***lab1*** and **select >*New Source*** to move to the page ***Select Source Type***



The page ***Select Source Type***

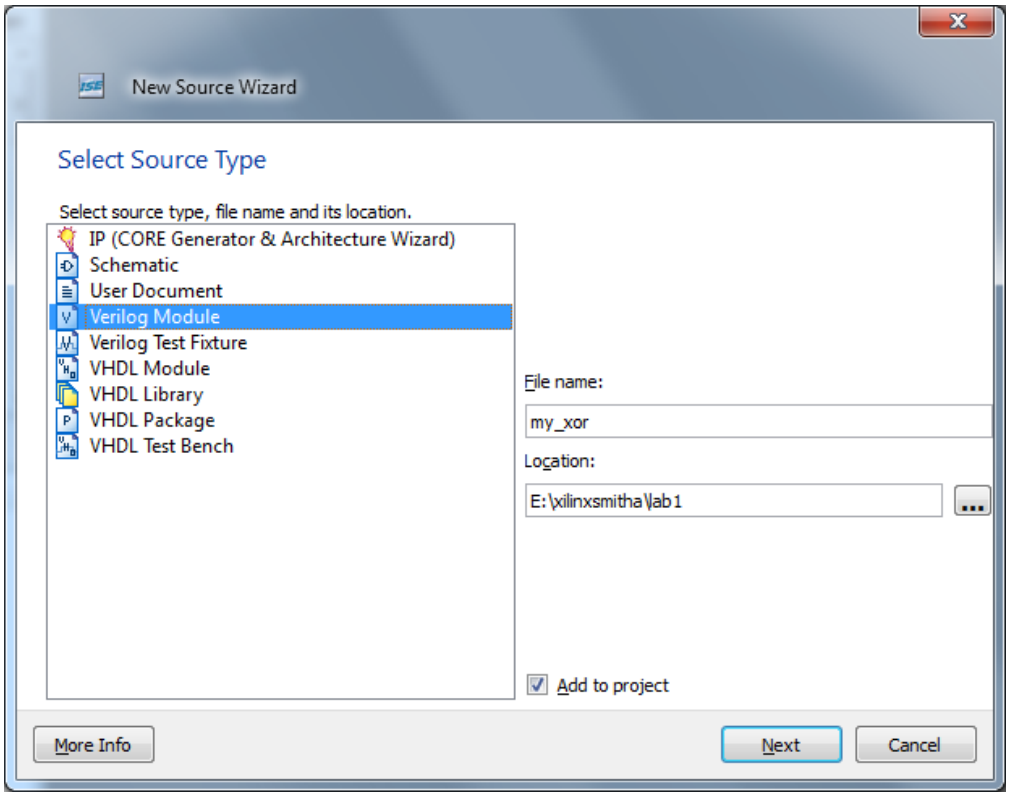
i) In the field ***File Name***, type **my_xor**

- You can choose another name that does not contain any white spaces

ii) From the Column at the left-side, select ***Verilog Module*** as a Source Type

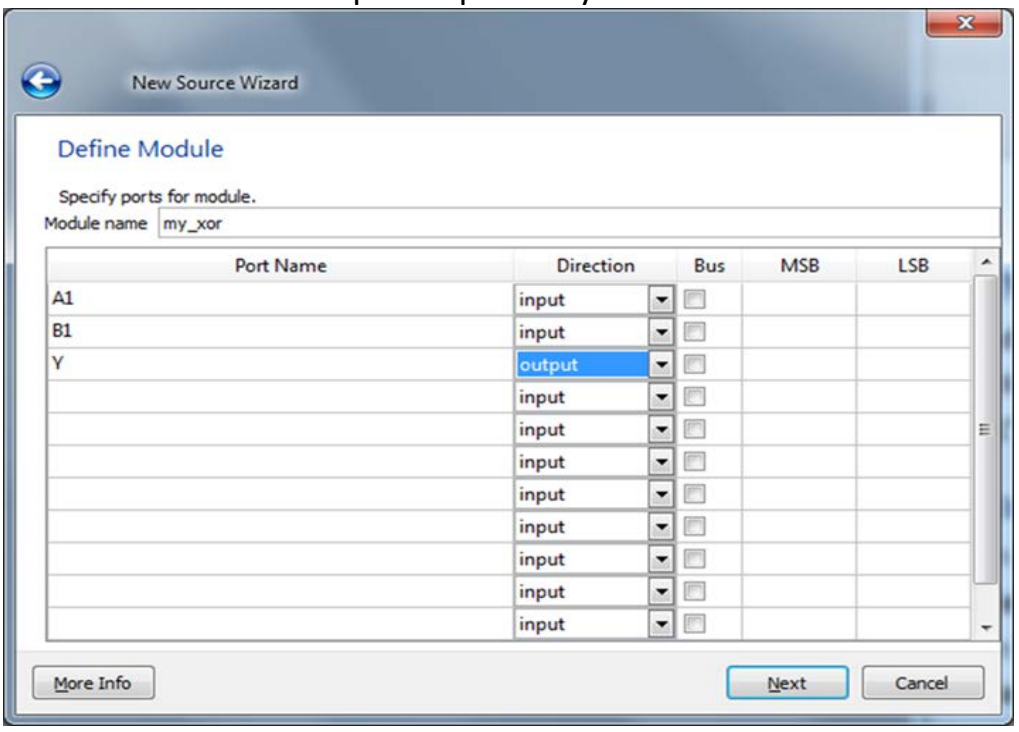
iii) **Tick** the option > ***Add To Project***.

iv) **Click > *Next*** to move to the page ***define the module***

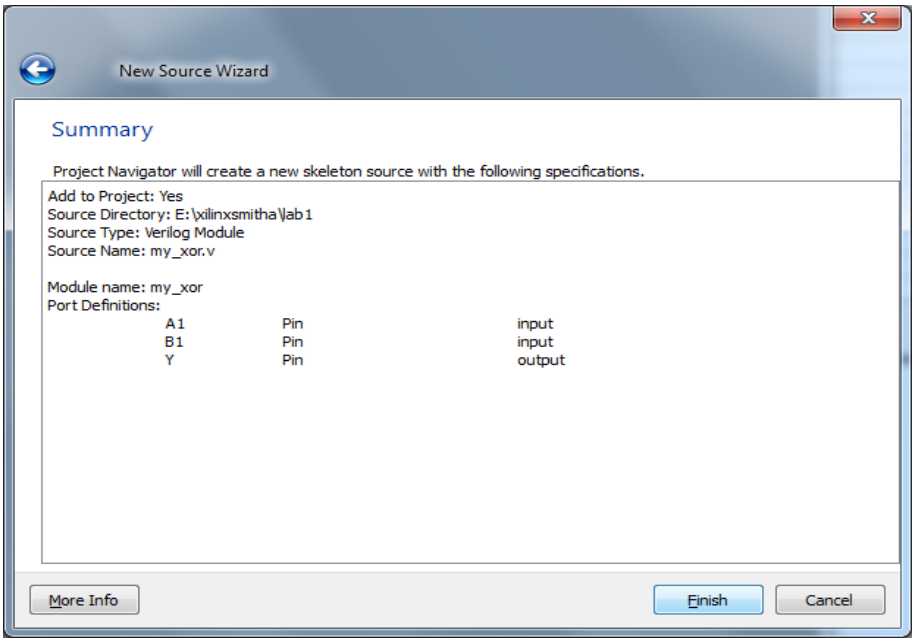


The page ***Define module***

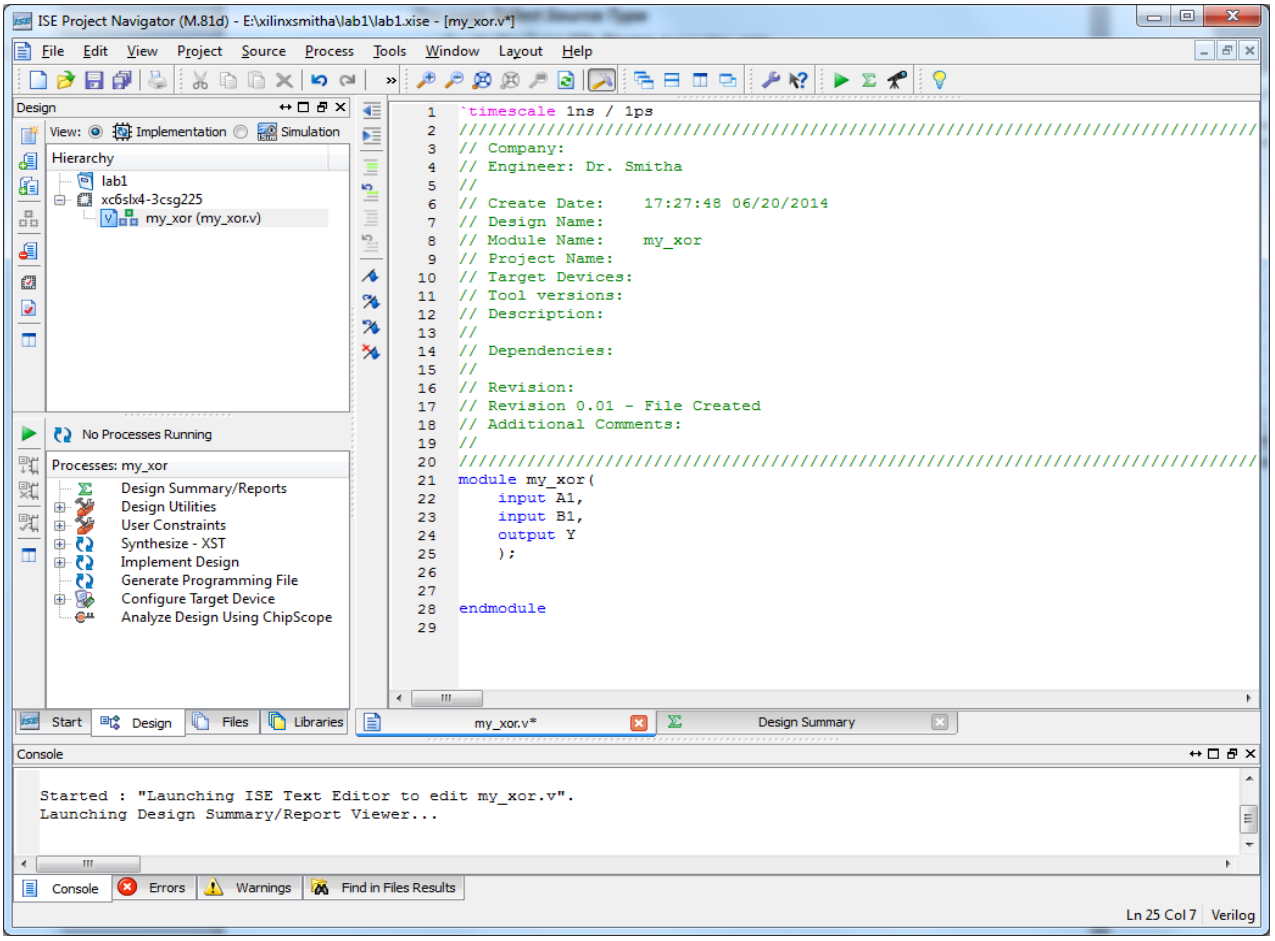
i) In the field **Port name** add A1, B1 and Y as input, input and output respectively.



ii) Click next to go to **project summary**

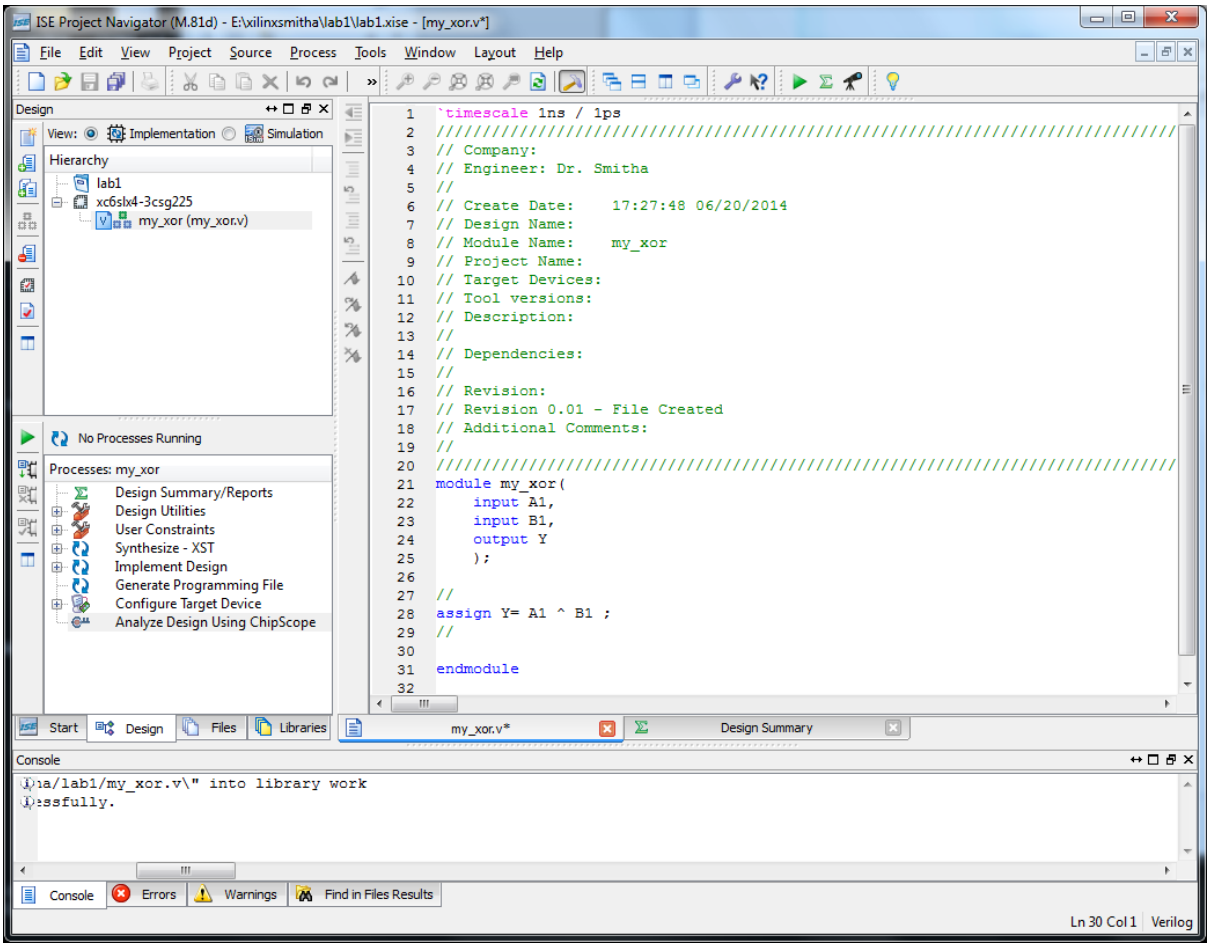


iii) Click finish and we can see the Verilog file my_xor.v in the **ISE project navigator**



Now we can add the main program for xor gate. The main code is written after the input definition and before the endmodule. Hence we create xor gate as

assign Y = A1 ^ B1;



IV. Create a New Test Bench

To verify the correctness behavior of our design, we need to simulate it. However, before the simulation, we have to create a test bench that stimulates the input ports of our design with different input values. We provide the set of stimuli to our design using a Verilog source file.

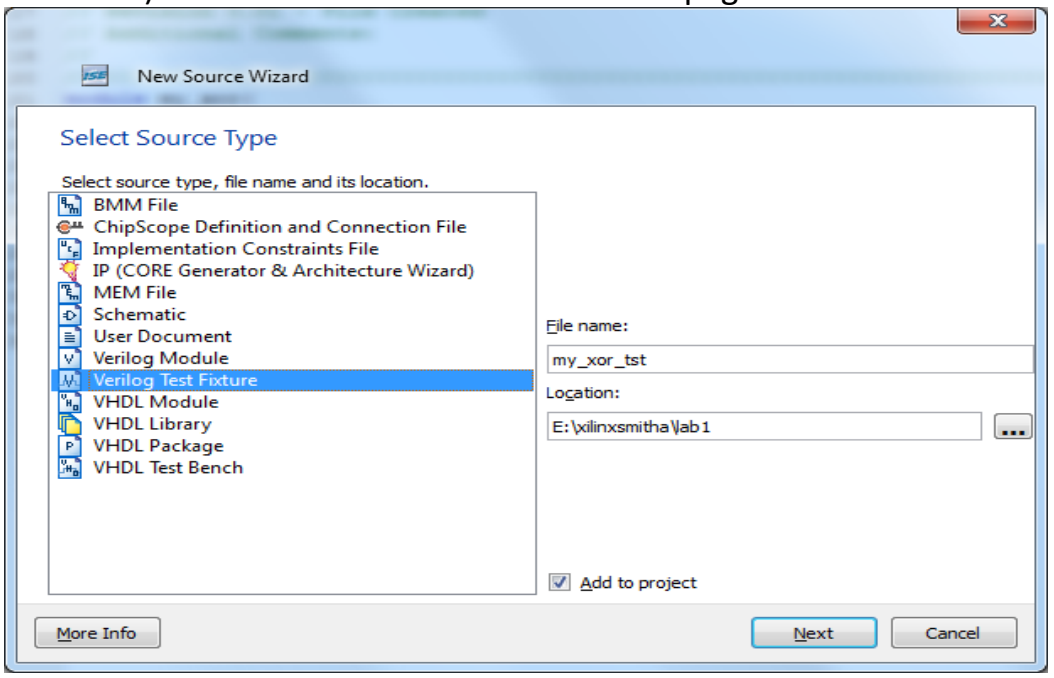
A Create a Verilog Source

1. In ***ISE Design Suite***, appears on the left side, go to the ***Design Panel***
2. In the ***Design Panel***, **right-click** on the icon ***lab1*** and **select > *New Source*** to move to the page ***Select Source Type***
3. The page ***Select Source Type Page***
   i) In the field ***File Name***, type **my_xor_tst**
   - You can choose another name that does not contain any white spaces

ii) From the Column at the left-side, select ***Verilog Test Fixture*** as a Source Type

iii) **Tick** the option **> *Add To Project***

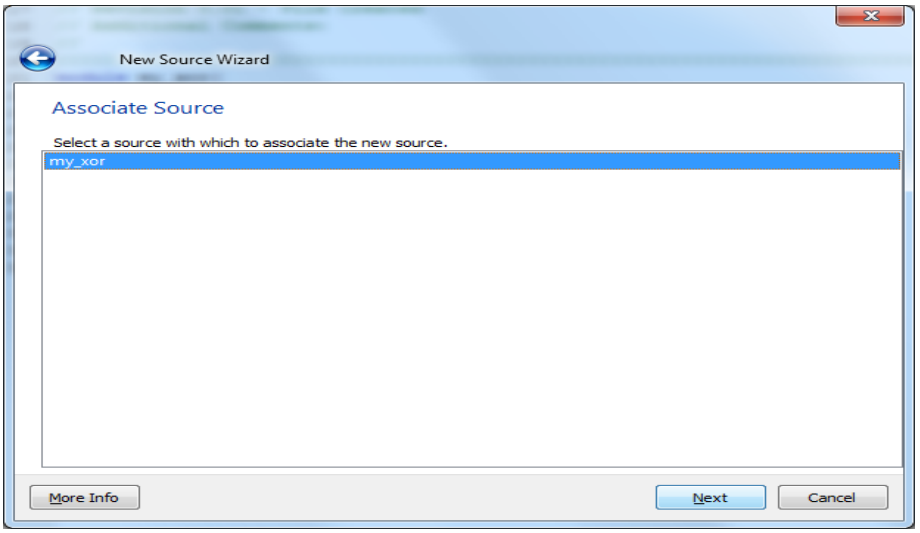
iv) **Click > *Next*** to move to the page ***Associate Source***



4. The page ***Associate Source***

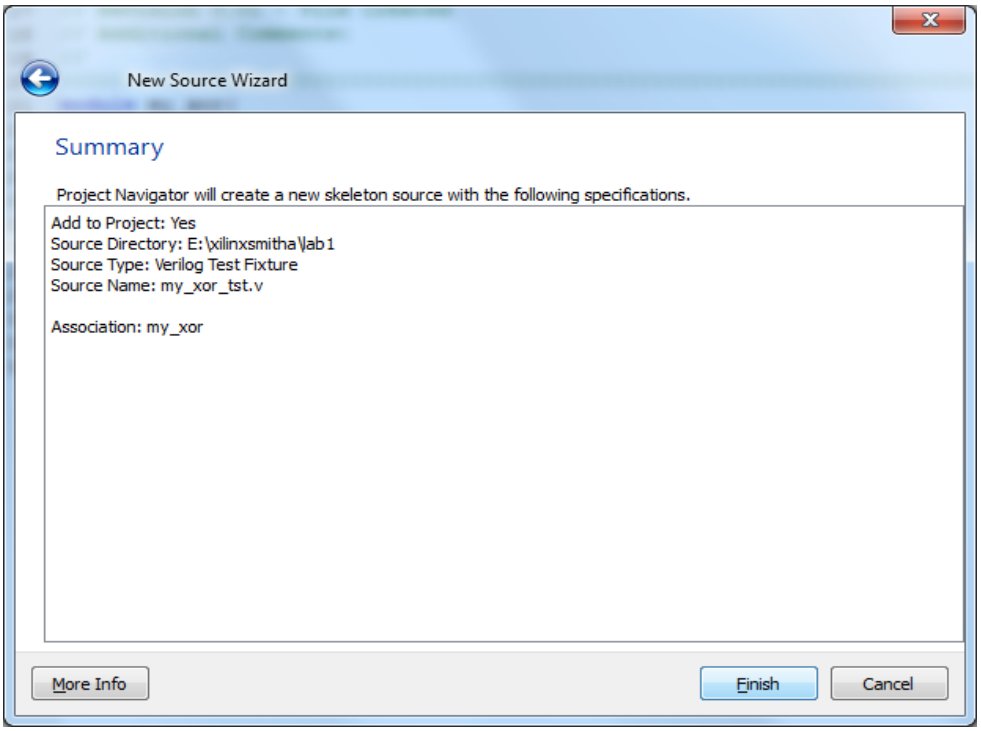
i) **Select > *my_xor*** as the source with which we want to associate our test bench.

ii) **Click > *Next*** to move to the page ***Project Summary***

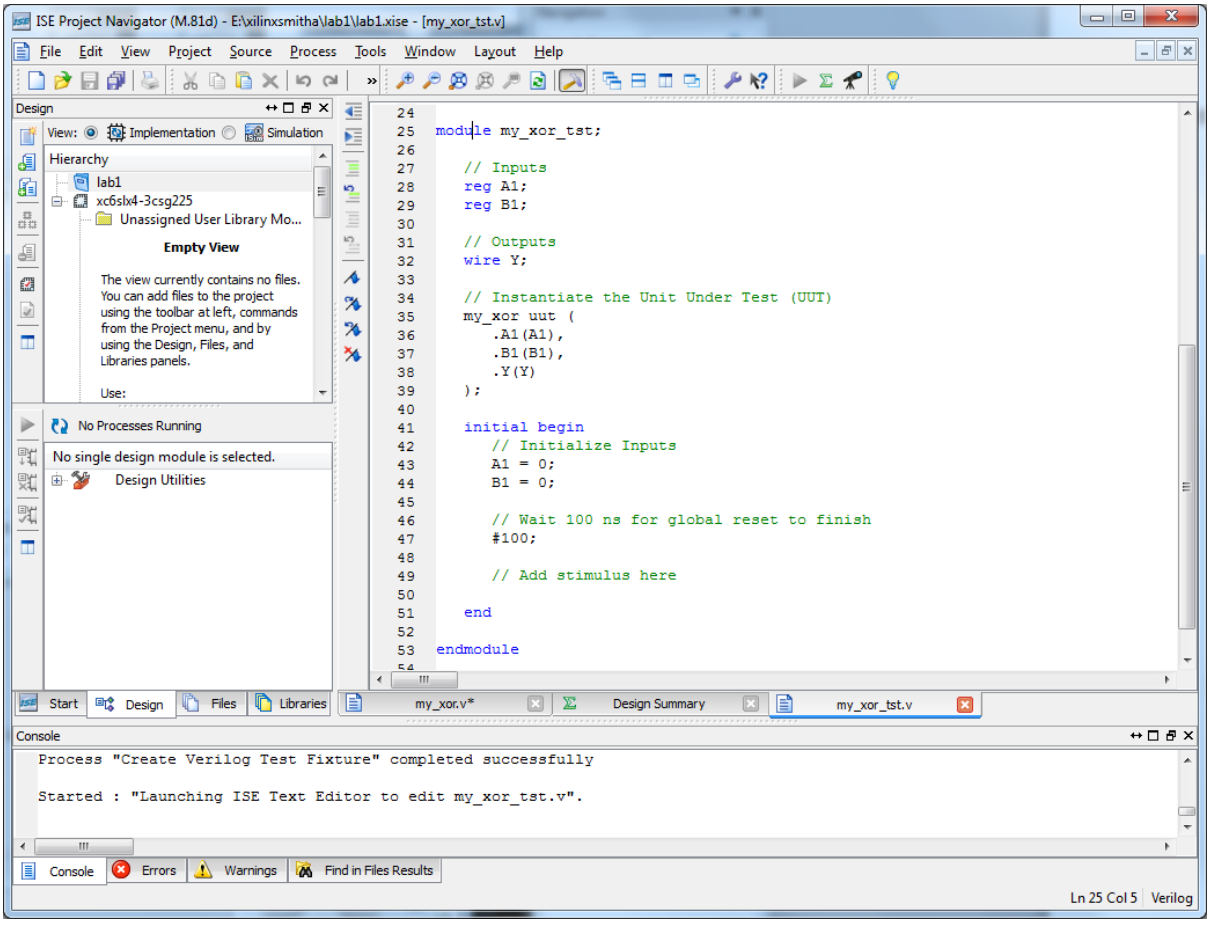


5. In the page ***Project Summary*** **, click > *Finish***

➢ A verilogsource file ***my_xor_tst*** is added to the project



my_xor_tst.v is generated



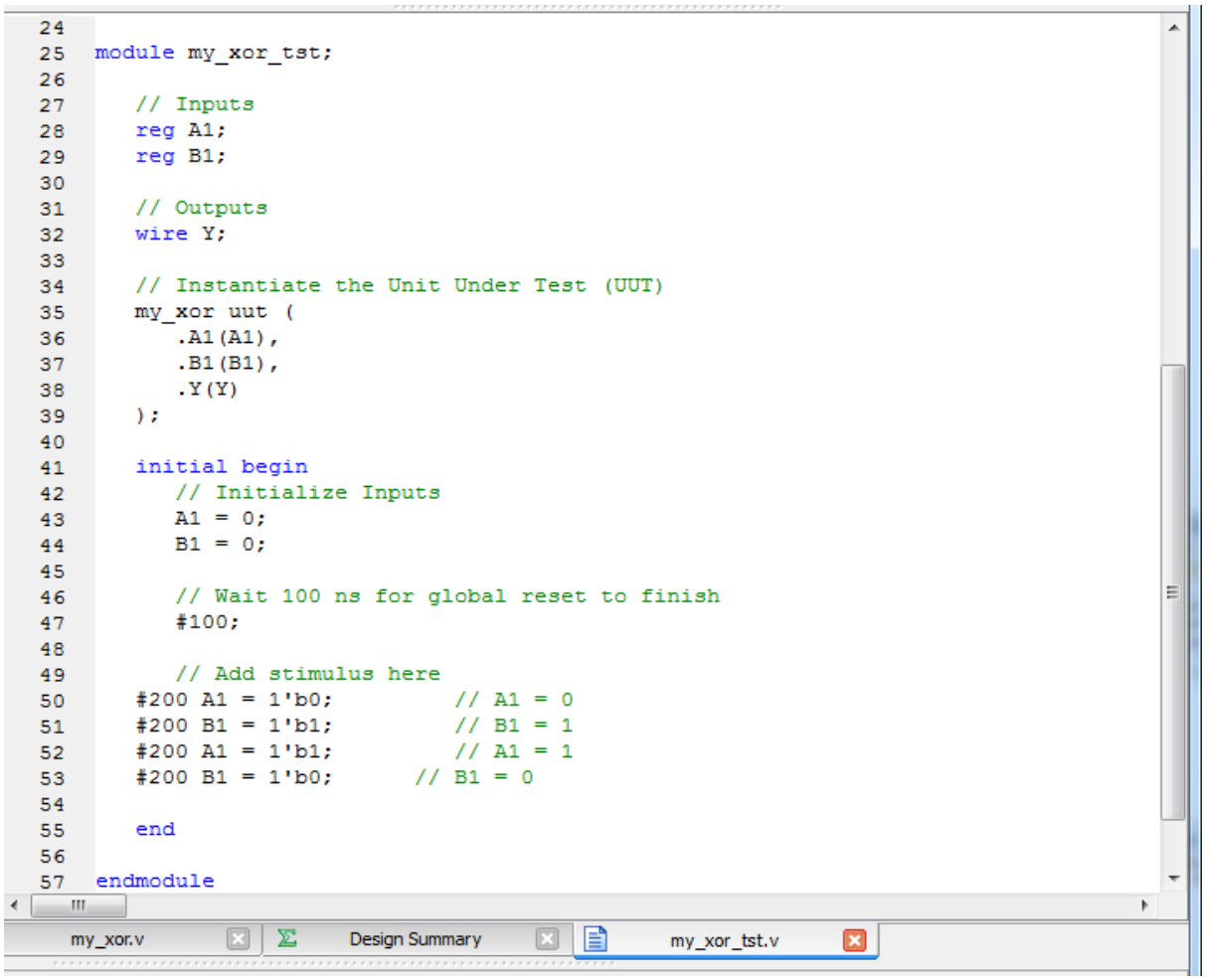
B Edit the Verilog File

1. Open the file ***my_xor_tst.v*** and move to the following section at the end of the file

```
initial begin
// Initialize Inputs
A1 = 0;
B1 = 0;
// Wait 100 ns for global reset to finish
#100;
// Add stimulus here
```

We can add the stimulus here by assigning the value '1' and '0' for A1 and B1 inorder to obtain the values for Y.

```
#200 A1 = 1'b0;          // A1 = 0
#200 B1 = 1'b1;          // B1 = 1
#200 A1 = 1'b1;          // A1 = 1
#200 B1 = 1'b0;          // B1 = 0
```

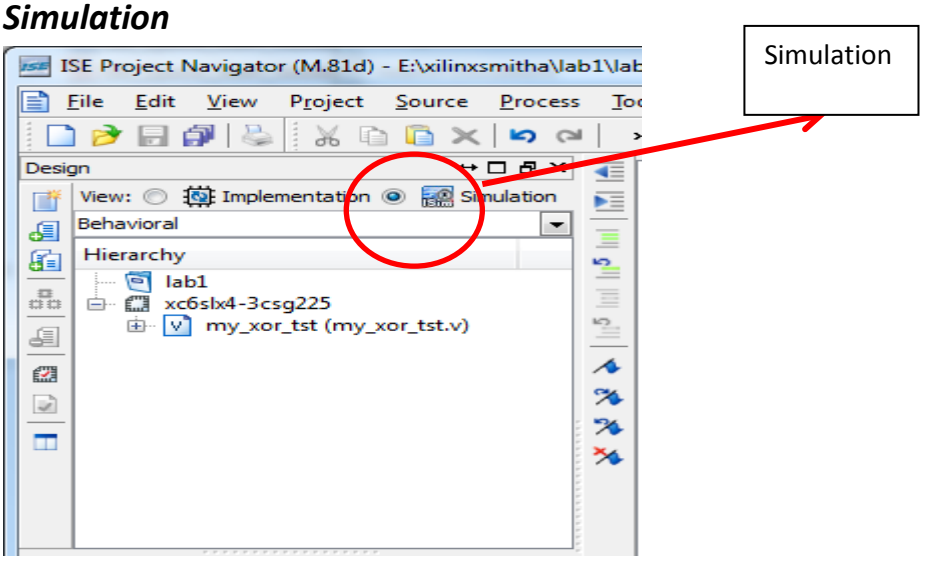


V. Simulate our Design

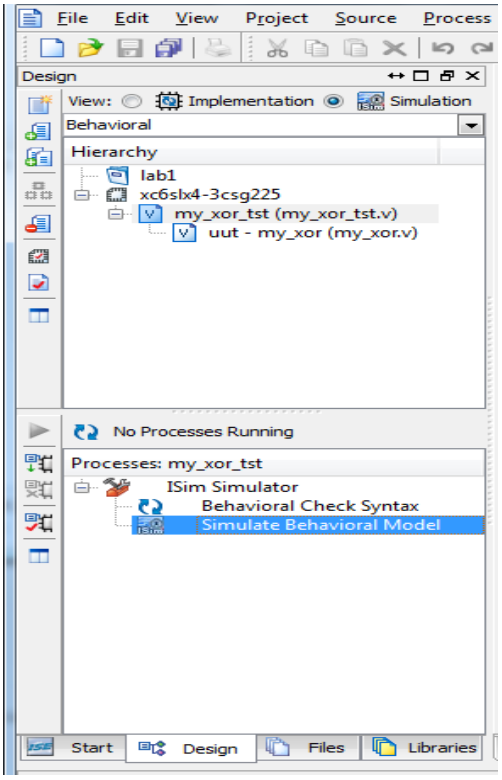
In this section, we will simulate our design to verify that it behaves as we expect. We will use the Integrated Simulator (ISim)

A ISIM

1. Open ***Design Panel***. In ***Design Panel View***, **select > *Simulation***



2. In ***Design Panel > Hierarchy***, **select > *my_xor_tst.v***
3. In ***Design Panel > Processes > ISim Simulator***, **Double Click > *Simulate Behavioral Model*** to open the Integrated Simulator (**ISim**)



4. ISIM Window

   i) **Zoom-Out** to view the whole simulation time, the Default ***simulation time*** is **1000 ns**,

   ii) The Simulator shows the three ports **A1, B1 and Y1**

   iii) Compare the value of Y1 with A1 and B1. **Y1** Should always equal to **A1 X-OR B1**