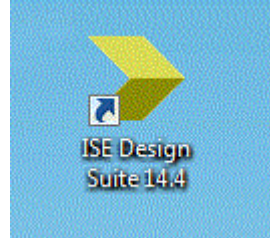


## I. Starting ISE Software

To start ISE, **double-click the desktop icon**



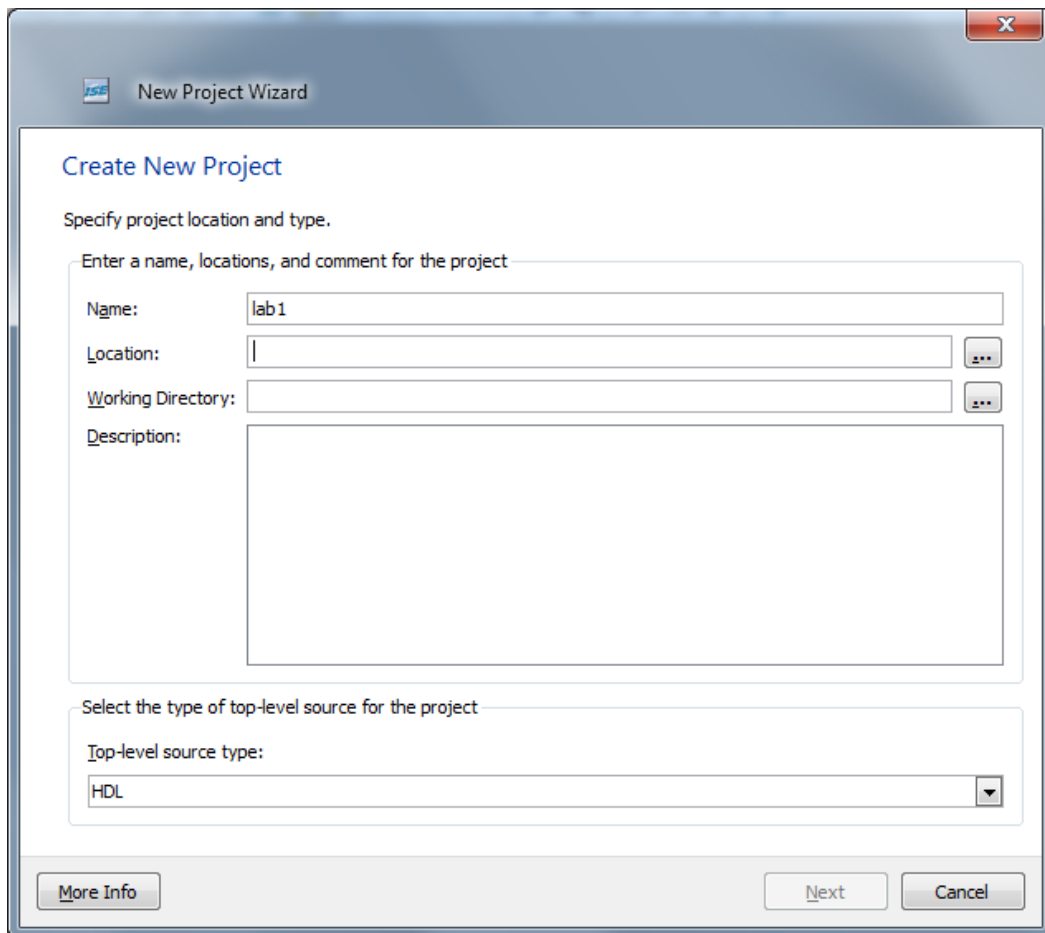
Or go to, **Start --- All Programs --- Xilinx Design Tools --- ISE Design Suite 14.4 --- ISE Design Tools --- 64-bit Project Navigator**

## II. Create a New Project

To create a new ISE project **Select File > New Project**. The page *Create New Project* appears

### A Create New Project page

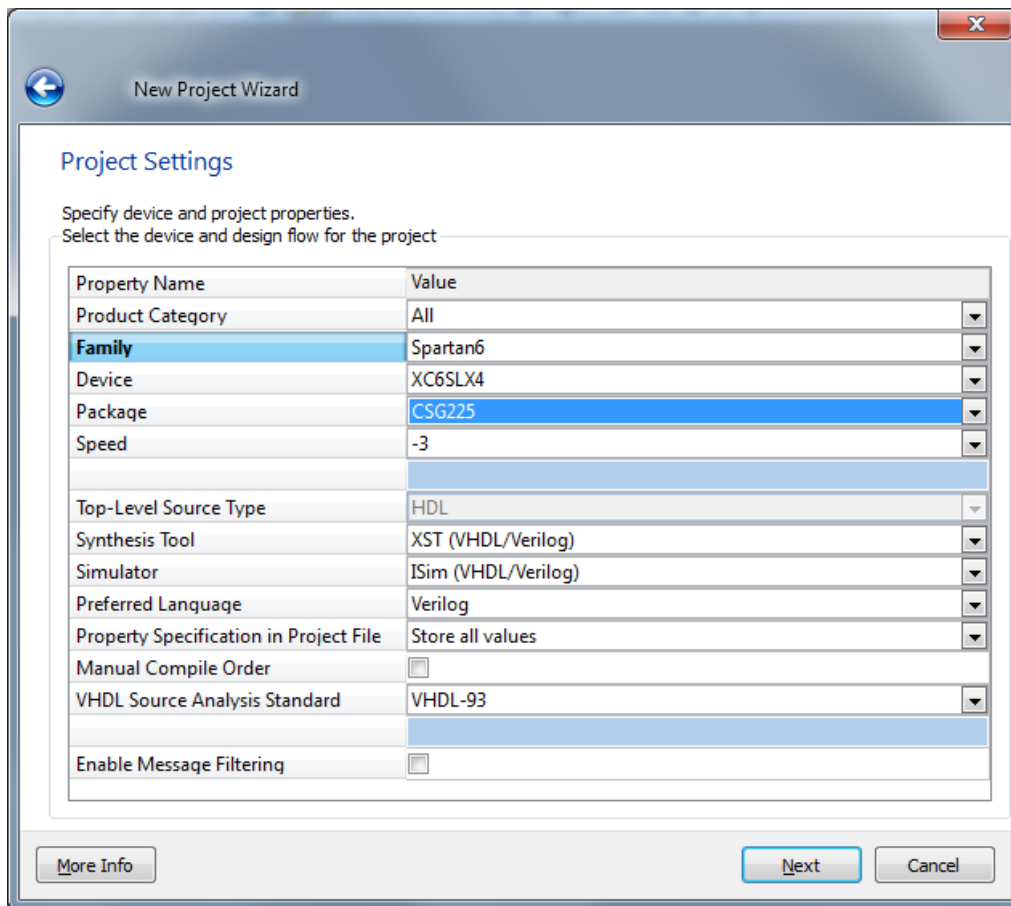
1. In the field Project **Name**, type **lab1**
  - You can choose another name that does not contain any white spaces
2. In the field Project **Location**, browse to a location (directory path) for the new project
  - If you use **Window**, browse to a directory under your **Nest drive**
3. In the field **Top-level source type**, select > **HDL**
4. Click > **Next** to move to the page **Project Settings**



The image shows a 'New Project Wizard' dialog box with a title bar containing the Xilinx logo and the text 'New Project Wizard'. The main content area is titled 'Create New Project' and includes the instruction 'Specify project location and type.' Below this, there is a section titled 'Enter a name, locations, and comment for the project' which contains four input fields: 'Name:' with the value 'lab1', 'Location:' with an empty field and a browse button (...), 'Working Directory:' with an empty field and a browse button (...), and 'Description:' with a large text area. Below this section is another titled 'Select the type of top-level source for the project' which contains a 'Top-level source type:' dropdown menu currently set to 'HDL'. At the bottom of the dialog are three buttons: 'More Info', 'Next', and 'Cancel'.

## B Project Settings page

1. In the field **family**, select >Spartan6
2. In the field **device**, Select > XC6SLX4
3. In the field **package**, Select > CSG225
4. In the field **speed**, Select > -3
5. In the field **Simulator**, Select > ISim(VHDL/Verilog)
6. In the field **Preferred Language**, Select > Verilog
7. Click > **Next** to move to the page **Project Summary**
5. Click > **Finish** in the page **Project Summary**



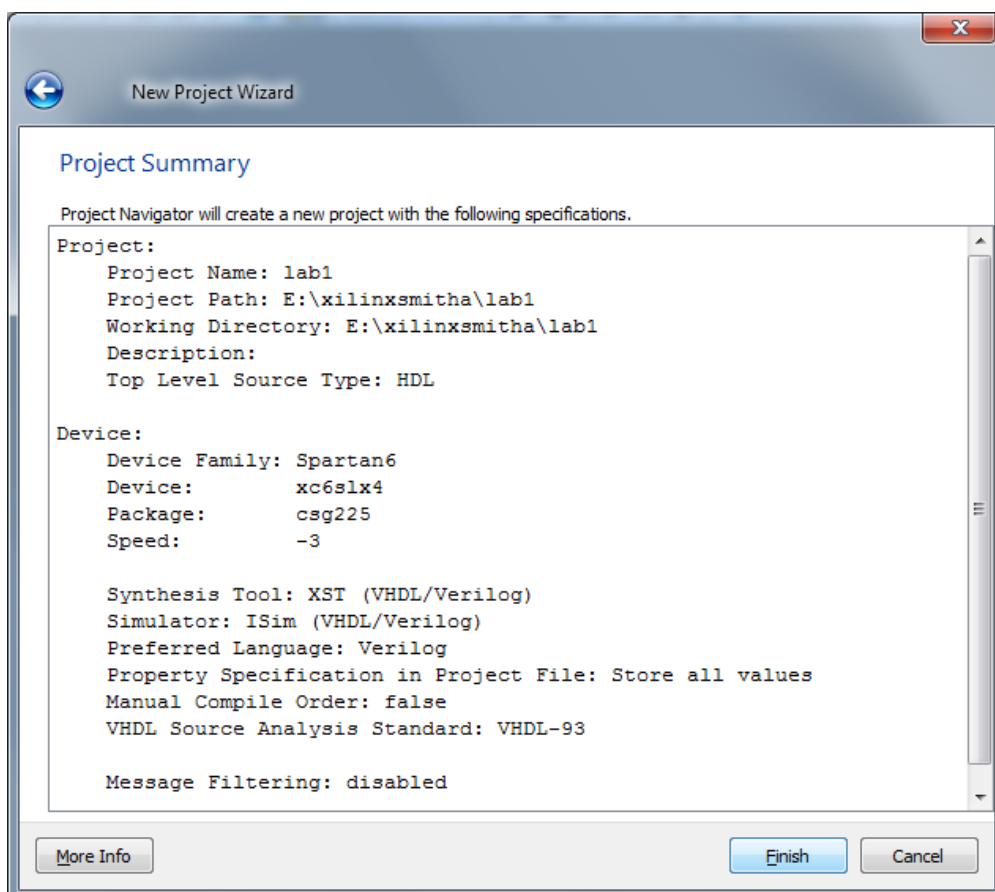
**New Project Wizard**

**Project Settings**

Specify device and project properties.  
Select the device and design flow for the project

Property Name	Value
Product Category	All
<b>Family</b>	Spartan6
Device	XC6SLX4
Package	CSG225
Speed	-3
Top-Level Source Type	HDL
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISim (VHDL/Verilog)
Preferred Language	Verilog
Property Specification in Project File	Store all values
Manual Compile Order	<input type="checkbox"/>
VHDL Source Analysis Standard	VHDL-93
Enable Message Filtering	<input type="checkbox"/>

More Info Next Cancel



**New Project Wizard**

**Project Summary**

Project Navigator will create a new project with the following specifications.

```

Project:
  Project Name: lab1
  Project Path: E:\xilinxsmitha\lab1
  Working Directory: E:\xilinxsmitha\lab1
  Description:
  Top Level Source Type: HDL

Device:
  Device Family: Spartan6
  Device: xc6slx4
  Package: csg225
  Speed: -3

  Synthesis Tool: XST (VHDL/Verilog)
  Simulator: ISim (VHDL/Verilog)
  Preferred Language: Verilog
  Property Specification in Project File: Store all values
  Manual Compile Order: false
  VHDL Source Analysis Standard: VHDL-93

  Message Filtering: disabled
  
```

More Info Finish Cancel

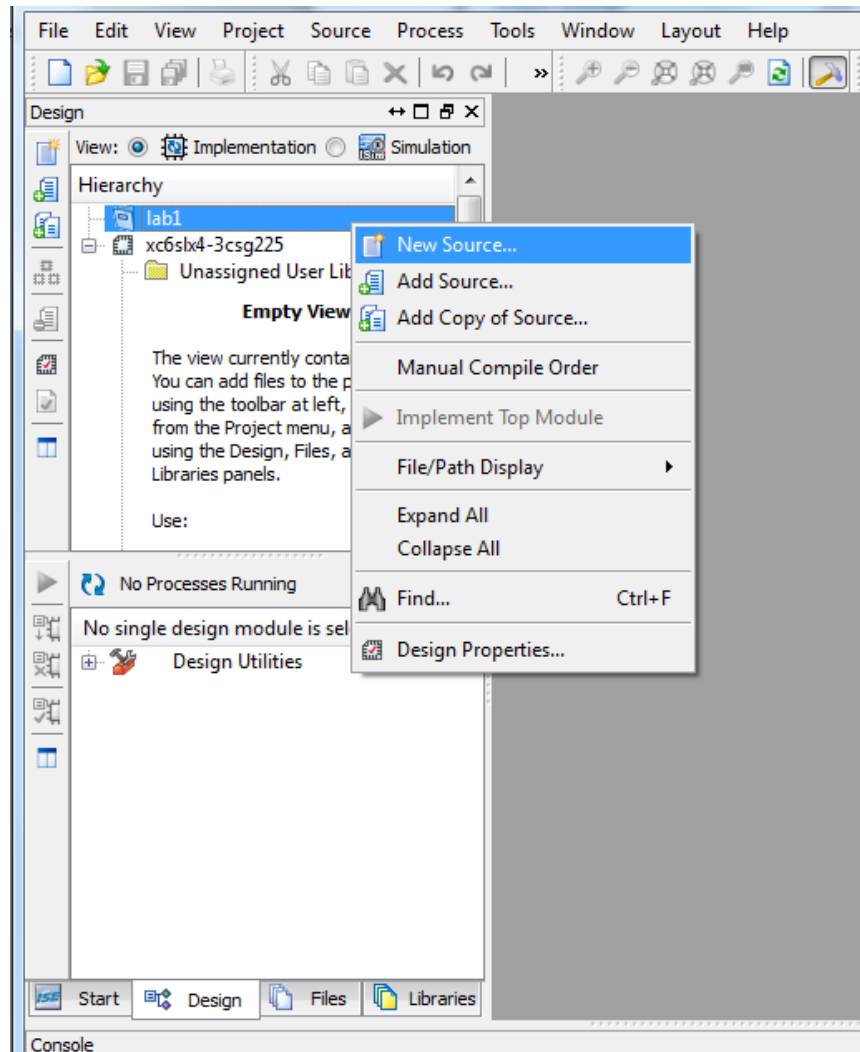
### III. Create a New Design

To study how to create a new design, we will design in this section a 2- Input X-OR Gate. The X-OR Function is defined as:

$$Y = A1 \text{ xor } B1 = A1'B1 + A1B1'$$

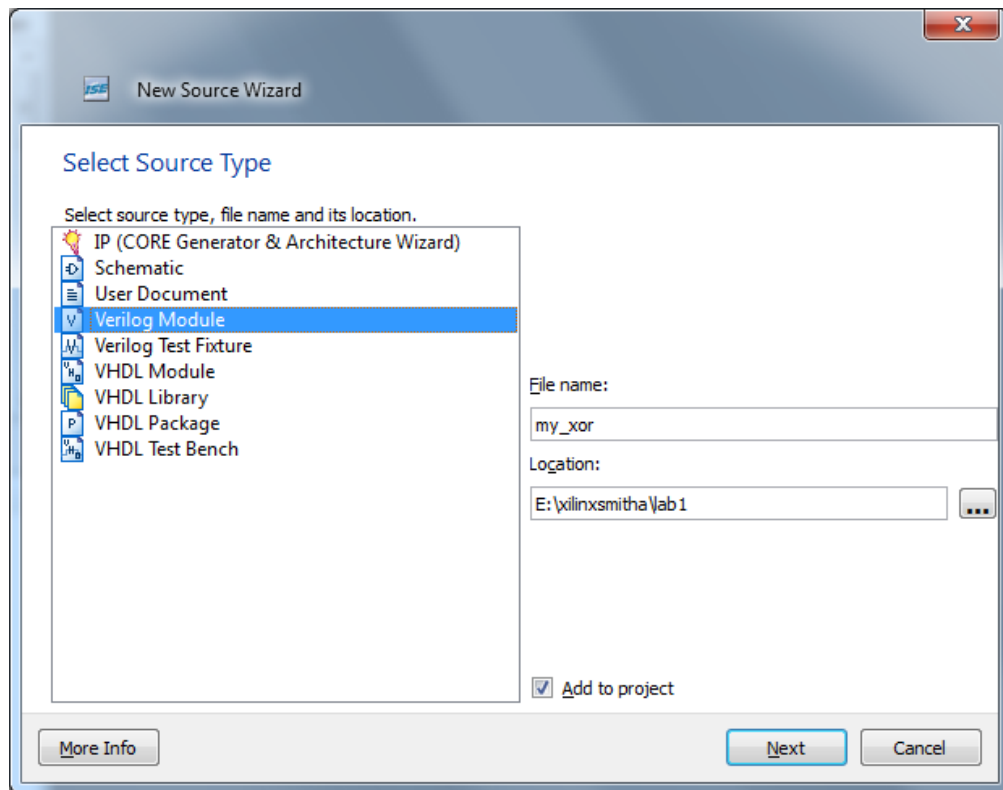
## A Create a HDL Source

1. In **ISE Design Suite** that appears on the left side of ISE, click on the **Design** Tab to go to the **Design Panel**
2. In the **Design Panel**, right-click on the icon **lab1** and select **>New Source** to move to the page **Select Source Type**



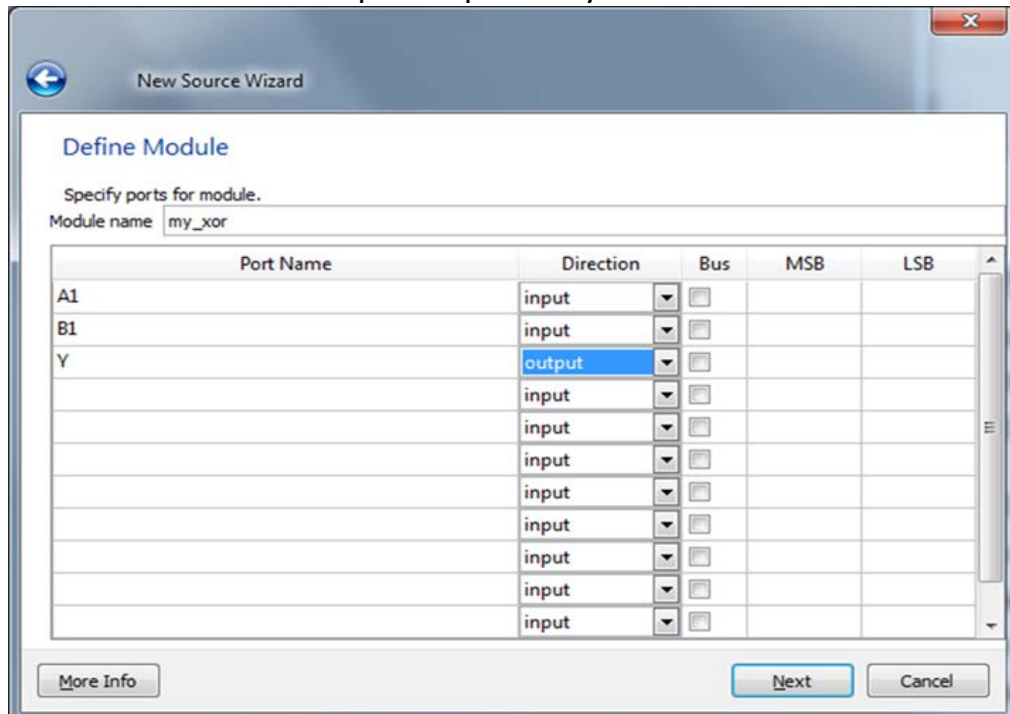
The page **Select Source Type**

- i) In the field **File Name**, type **my\_xor**
  - You can choose another name that does not contain any white spaces
- ii) From the Column at the left-side, select **Verilog Module** as a Source Type
- iii) Tick the option **> Add To Project**.
- iv) Click **> Next** to move to the page **define the module**

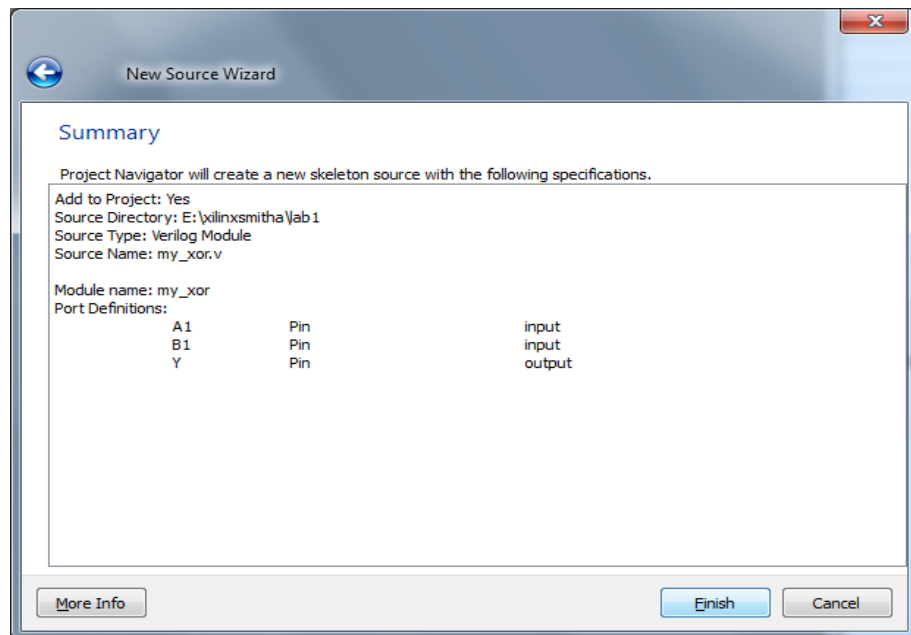


The page **Define module**

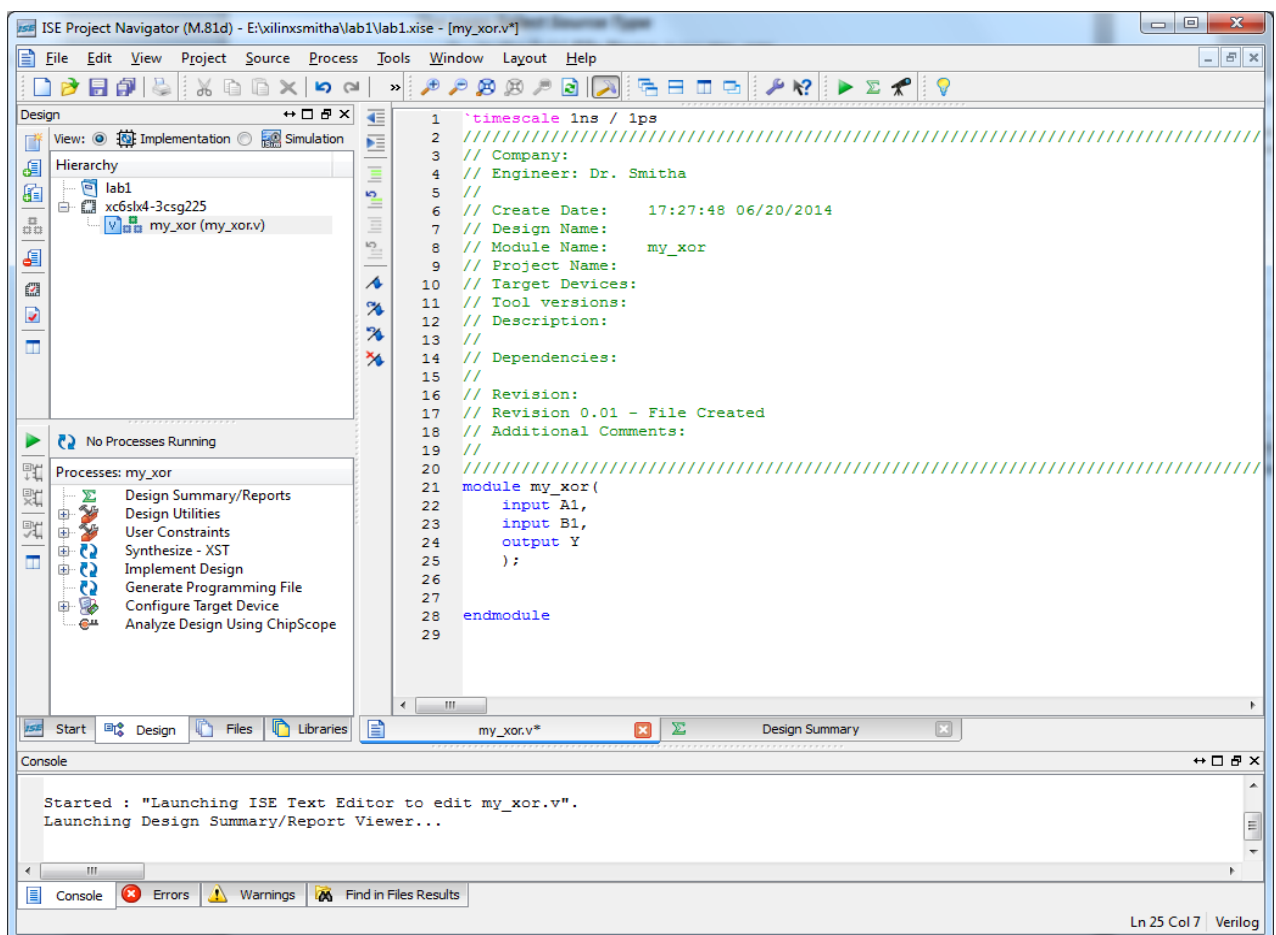
- i) In the field **Port name** add A1, B1 and Y as input, input and output respectively.



- ii) Click next to go to **project summary**

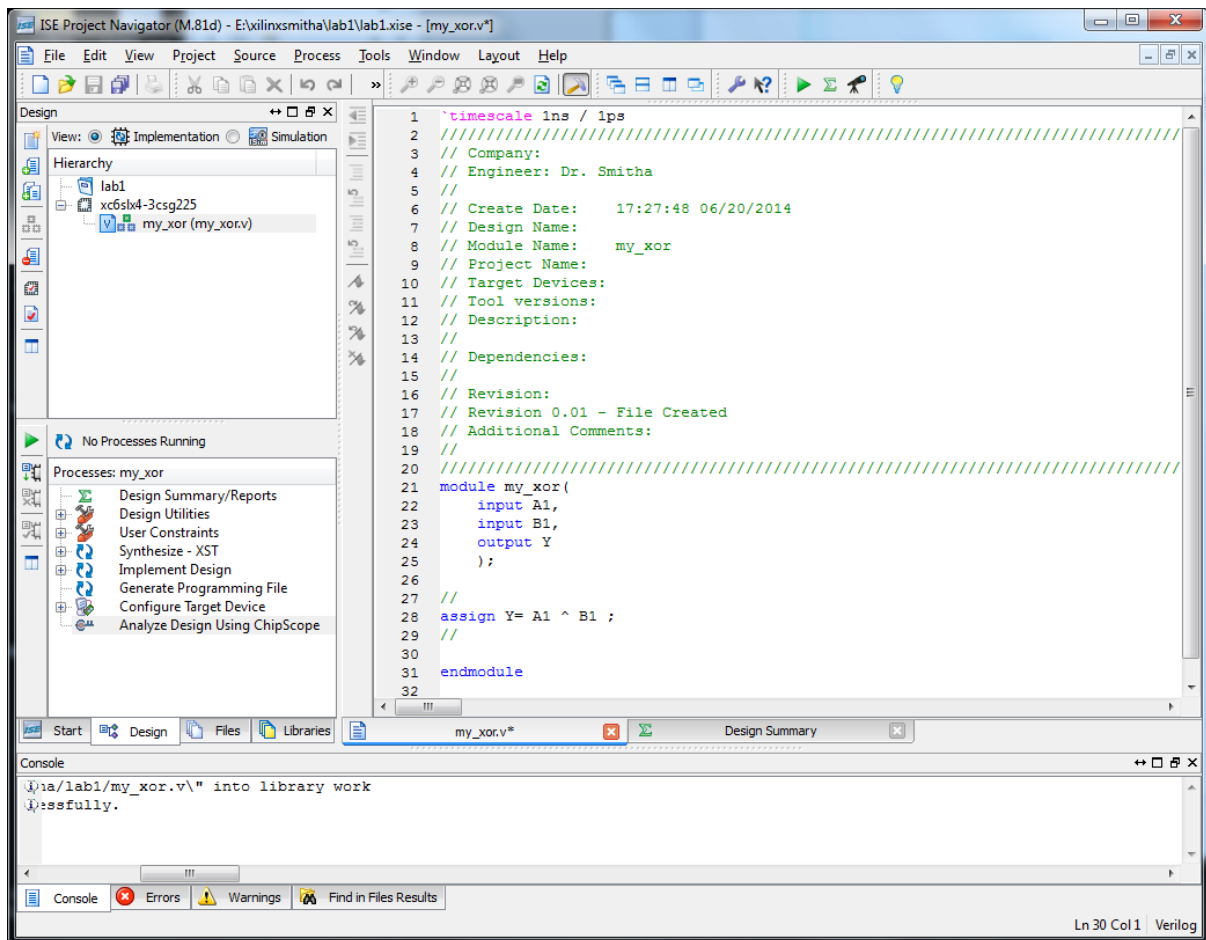


- iii) Click finish and we can see the Verilog file my\_xor.v in the ISE project navigator



Now we can add the main program for xor gate. The main code is written after the input definition and before the endmodule. Hence we create xor gate as

**assign Y = A1 ^ B1;**



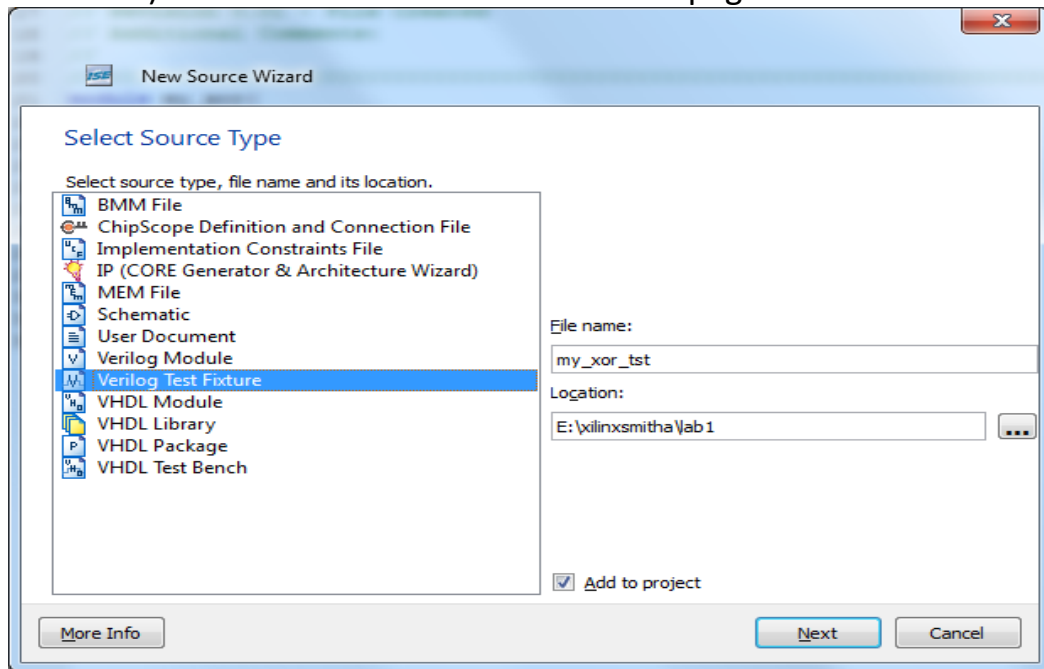
## IV. Create a New Test Bench

To verify the correctness behavior of our design, we need to simulate it. However, before the simulation, we have to create a test bench that stimulates the input ports of our design with different input values. We provide the set of stimuli to our design using a Verilog source file.

### A Create a Verilog Source

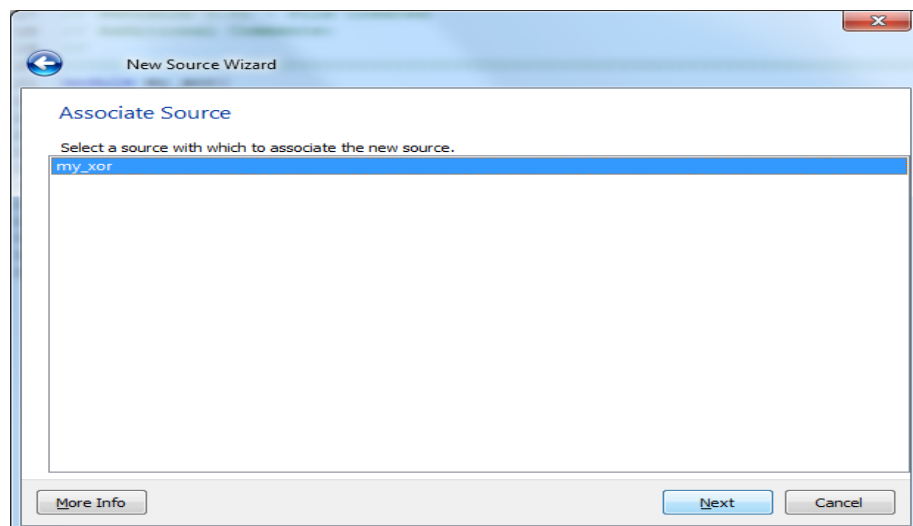
1. In **ISE Design Suite**, appears on the left side, go to the **Design Panel**
2. In the **Design Panel**, right-click on the icon **lab1** and select > **New Source** to move to the page **Select Source Type**
3. The page **Select Source Type Page**
  - i) In the field **File Name**, type **my\_xor\_tst**
    - You can choose another name that does not contain any white spaces

- ii) From the Column at the left-side, select **Verilog Test Fixture** as a Source Type
- iii) **Tick** the option > **Add To Project**
- iv) **Click > Next** to move to the page **Associate Source**



4. The page **Associate Source**

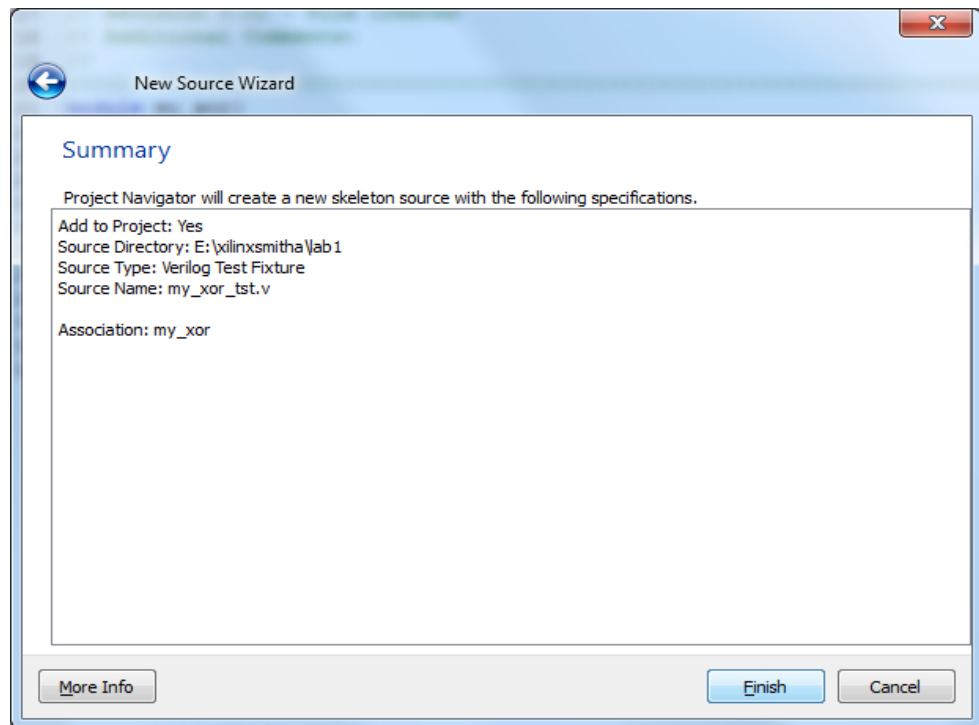
- i) **Select > my\_xor** as the source with which we want to associate our test bench.
- ii) **Click > Next** to move to the page **Project Summary**



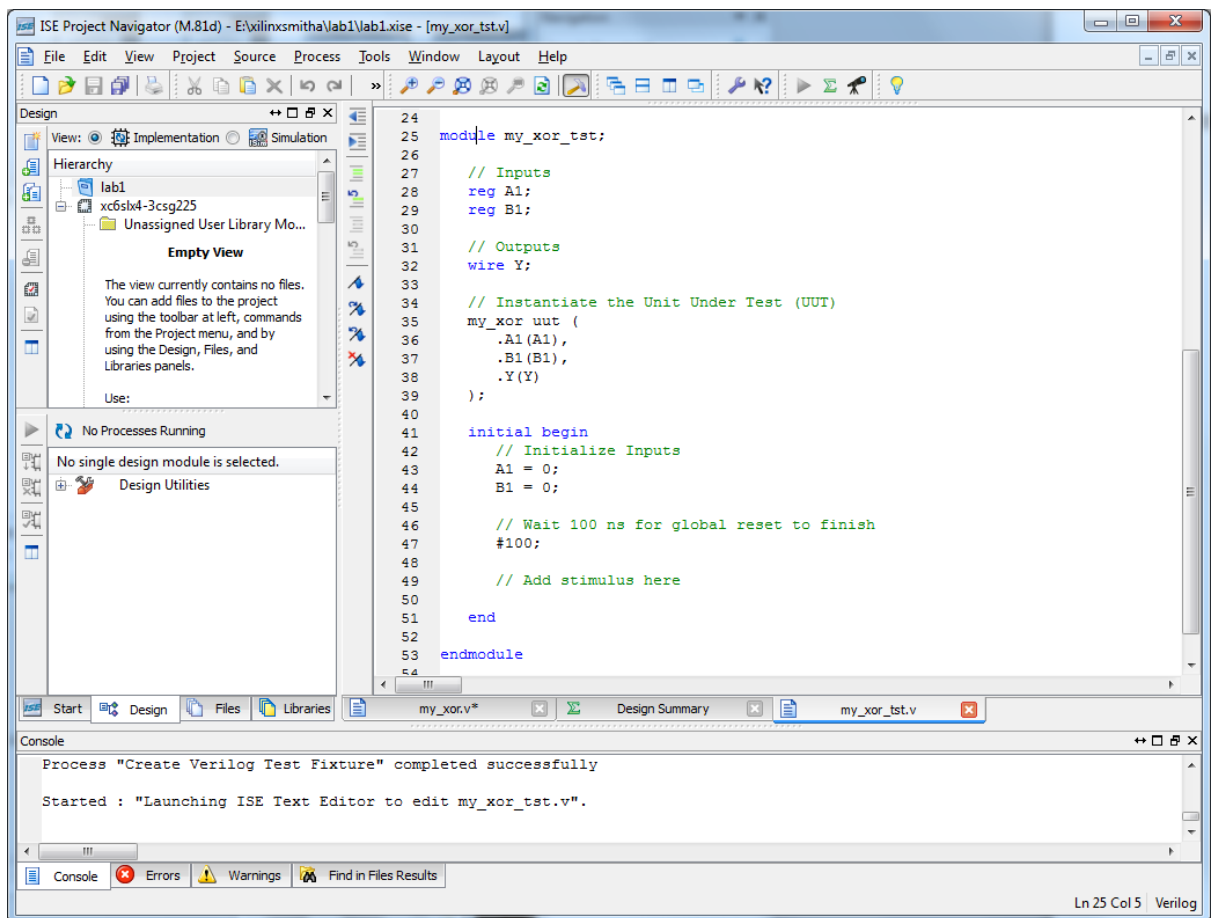
5. In the page **Project Summary** , click > **Finish**

- A verilogsource file **my\_xor\_tst** is added to the project





*my\_xor\_tst.v* is generated



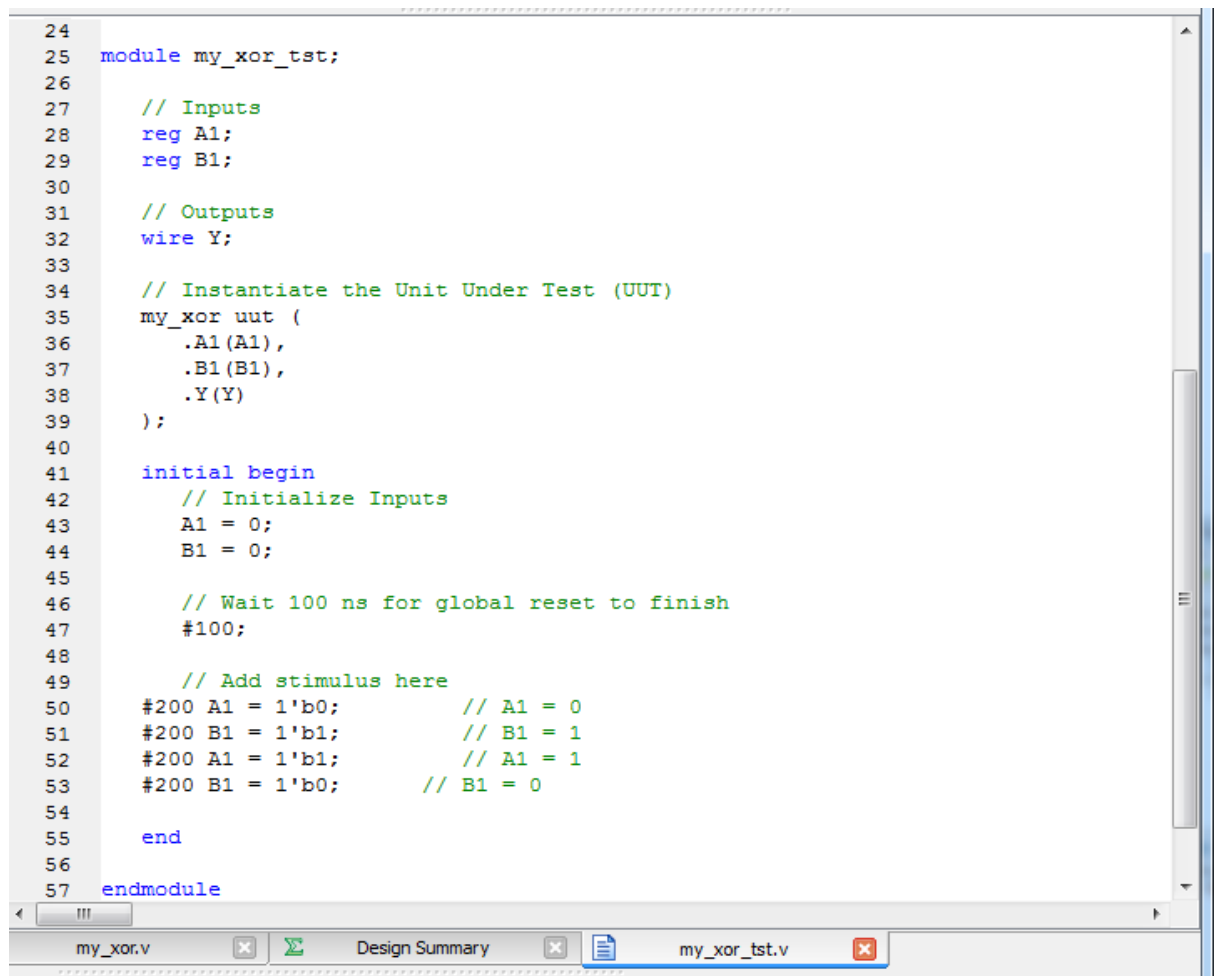
## B Edit the Verilog File

1. Open the file **my\_xor\_tst.v** and move to the following section at the end of the file

```
initial begin
// Initialize Inputs
A1 = 0;
B1 = 0;
// Wait 100 ns for global reset to finish
#100;
// Add stimulus here
```

We can add the stimulus here by assigning the value '1' and '0' for A1 and B1 inorder to obtain the values for Y.

```
#200 A1 = 1'b0;           // A1 = 0
#200 B1 = 1'b1;           // B1 = 1
#200 A1 = 1'b1;           // A1 = 1
#200 B1 = 1'b0;           // B1 = 0
```



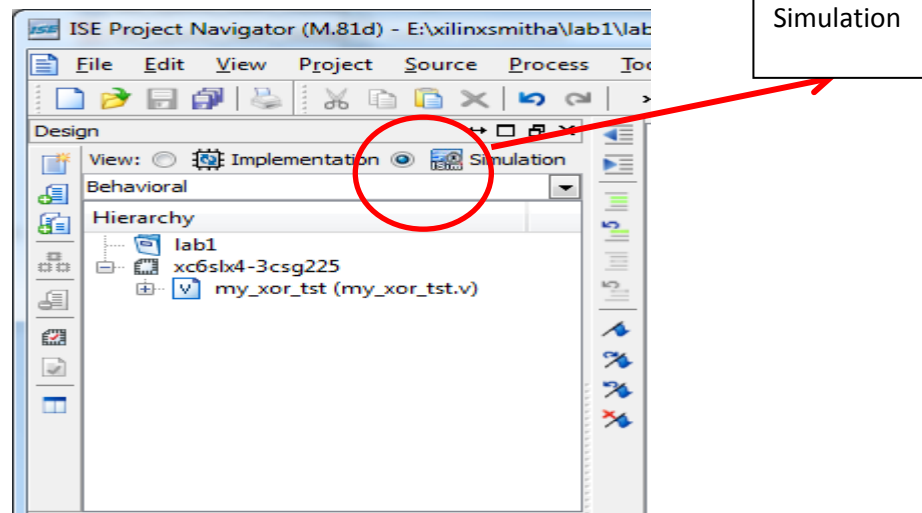
```
24
25 module my_xor_tst;
26
27     // Inputs
28     reg A1;
29     reg B1;
30
31     // Outputs
32     wire Y;
33
34     // Instantiate the Unit Under Test (UUT)
35     my_xor uut (
36         .A1(A1),
37         .B1(B1),
38         .Y(Y)
39     );
40
41     initial begin
42         // Initialize Inputs
43         A1 = 0;
44         B1 = 0;
45
46         // Wait 100 ns for global reset to finish
47         #100;
48
49         // Add stimulus here
50         #200 A1 = 1'b0;           // A1 = 0
51         #200 B1 = 1'b1;           // B1 = 1
52         #200 A1 = 1'b1;           // A1 = 1
53         #200 B1 = 1'b0;           // B1 = 0
54
55     end
56
57 endmodule
```

## V. Simulate our Design

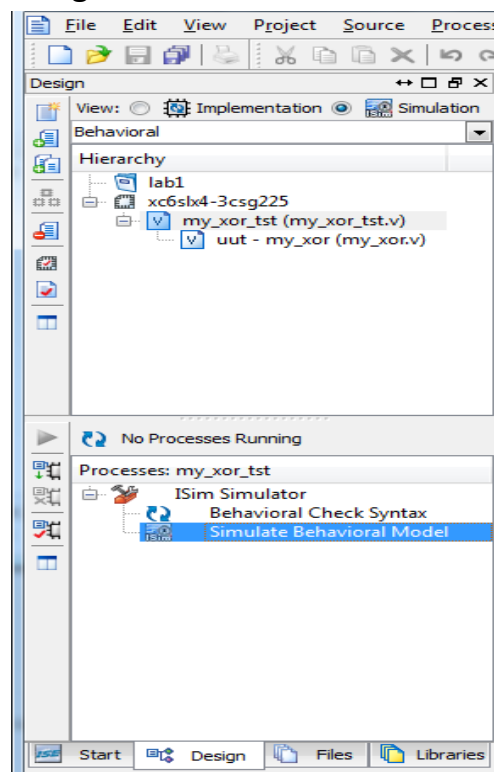
In this section, we will simulate our design to verify that it behaves as we expect. We will use the Integrated Simulator (ISim)

### A ISIM

1. Open **Design Panel**. In **Design Panel View**, select > **Simulation**



2. In **Design Panel > Hierarchy**, select > **my\_xor\_tst.v**
3. In **Design Panel > Processes > ISim Simulator**, Double Click > **Simulate Behavioral Model** to open the Integrated Simulator (ISim)



#### 4. ISIM Window

- i) **Zoom-Out** to view the whole simulation time, the Default **simulation time** is **1000 ns**,
- ii) The Simulator shows the three ports **A1, B1 and Y1**
- iii) Compare the value of Y1 with A1 and B1. **Y1** Should always equal to **A1 X-OR B1**

