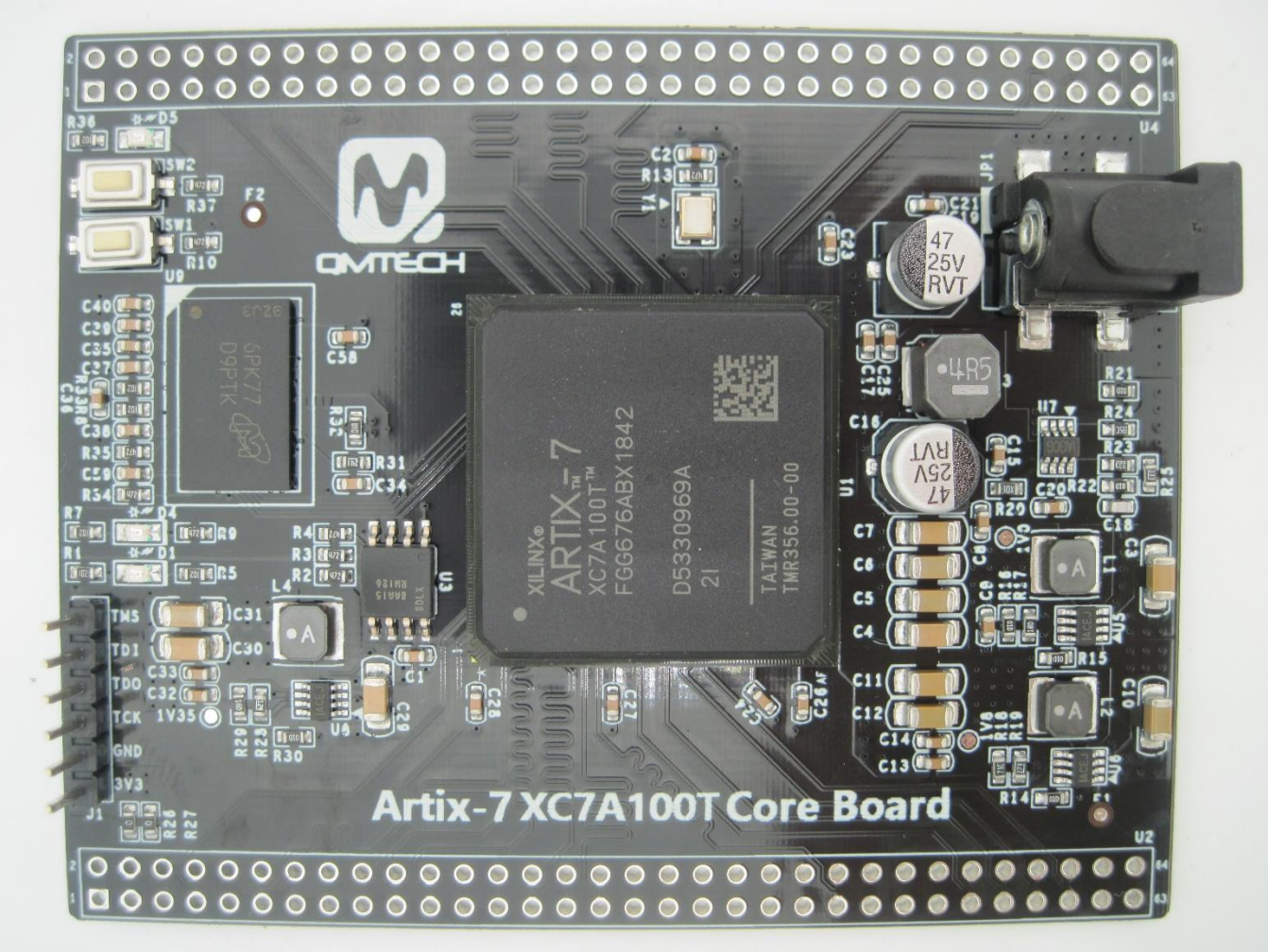
QMTECH XC7A100T STARTER KIT

USER MANUAL(CORE BOARD)



Preface

The QMTech® XC7A100T core board uses Xilinx Artix®-7 devices to demonstrate the highest performance-per-watt fabric, transceiver line rates, DSP processing, and AMS integration in a cost-optimized FPGA. Featuring the MicroBlaze™ soft processor and 1,066Mb/s DDR3 support, the family is the best value for a variety of cost and power-sensitive applications including software-defined radio, machine vision cameras, and low-end wireless backhaul.

For more information, updates and useful links, please visit QMTECH Official Website:

http://www.chinaqmtech.com

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1. Introduction

1.1 Document Scope

This demo user manual introduces the QMTECH XC7A100T core board and describes how to setup the core board running with application software Xilinx Vivado 2018.3. Users may employee the on board rich logic resource FPGA XC7A100T-2FGG676I and large DDR3 memory MT41K128M16 to implement various applications. The core board also has 108 non-multiplexed FPGA IOs for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module etc.

1.2 Kit Overview

Below section lists the parameters of the QMTECH XC7A100T core board:

- On-Board FPGA: XC7A100T-2FGG676I;
- On-Board FPGA external crystal frequency: 50MHz;
- XC7A100T-2FGG676I has rich block RAM resource up to 4,860Kb;
- XC7A100T-2FGG676I has 101,440 logic cells;
- On-Board MT25QL128 SPI Flash, 16M bytes for user configuration code;
- On-Board 256MB Micron DDR3, MT41K128M16JT-125:K;
- On-Board 3.3V power supply for FPGA by using MP2315 wide input range DC/DC;
- XC7A100T core board has two 64p, 2.54mm pitch headers for extending user IOs. All IOs are precisely designed with length matching;
- XC7A100T core board has 2 user switches;
- XC7A100T core board has 3 user LEDs;
- XC7A100T core board has JTAG interface, by using 6p, 2.54mm pitch header;
- XC7A100T core board PCB size is: 6.7cm x 8.4cm;
- Default power source for board is: 2A@5V DC, the DC header type: DC-050, 5.5mmx2.1mm;

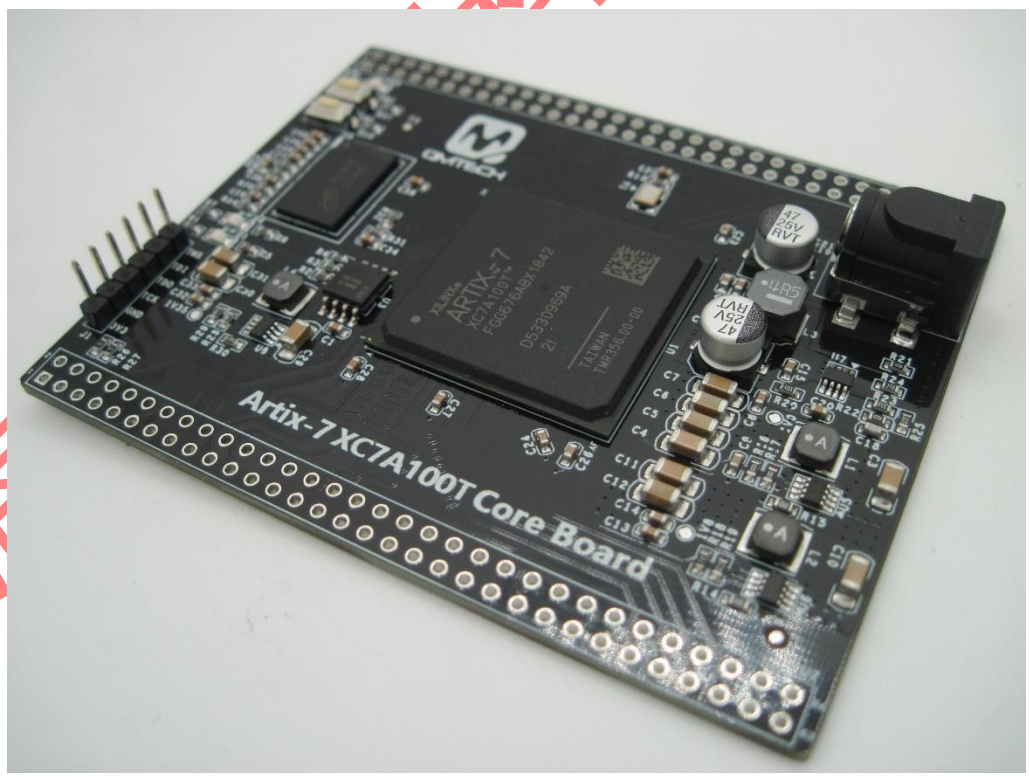


Figure 1-1. QMTECH XC7A100T Core Board Overview

2. Getting Started

The QMTECH XCA100T core board includes below item:

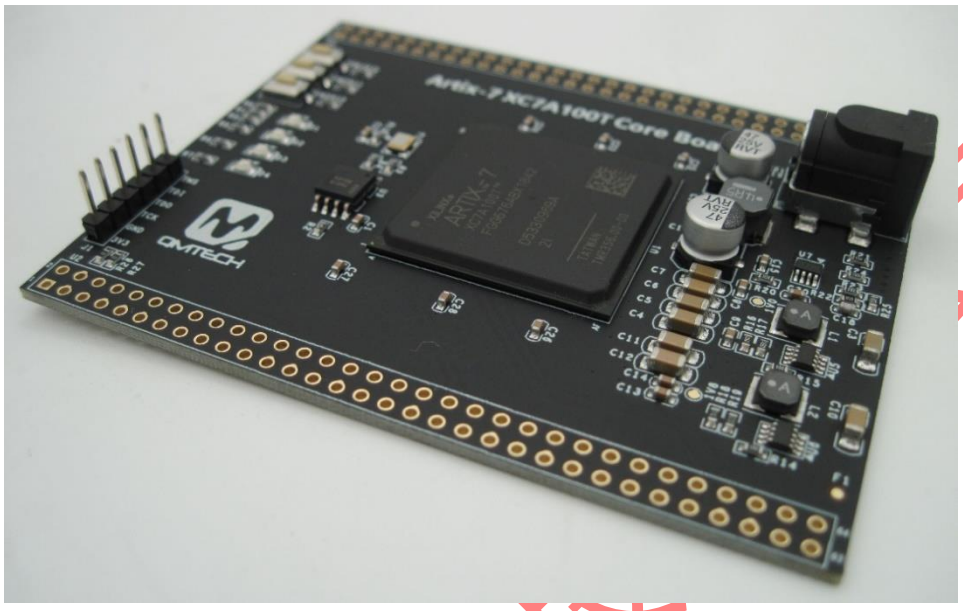


Figure 2-1. QMTECH XC7A100T Top View

Below image shows the dimension of the QMTECH XC7A100T core board: 6.71cm x 8.41cm. The unit in below image is millimeter(mm).

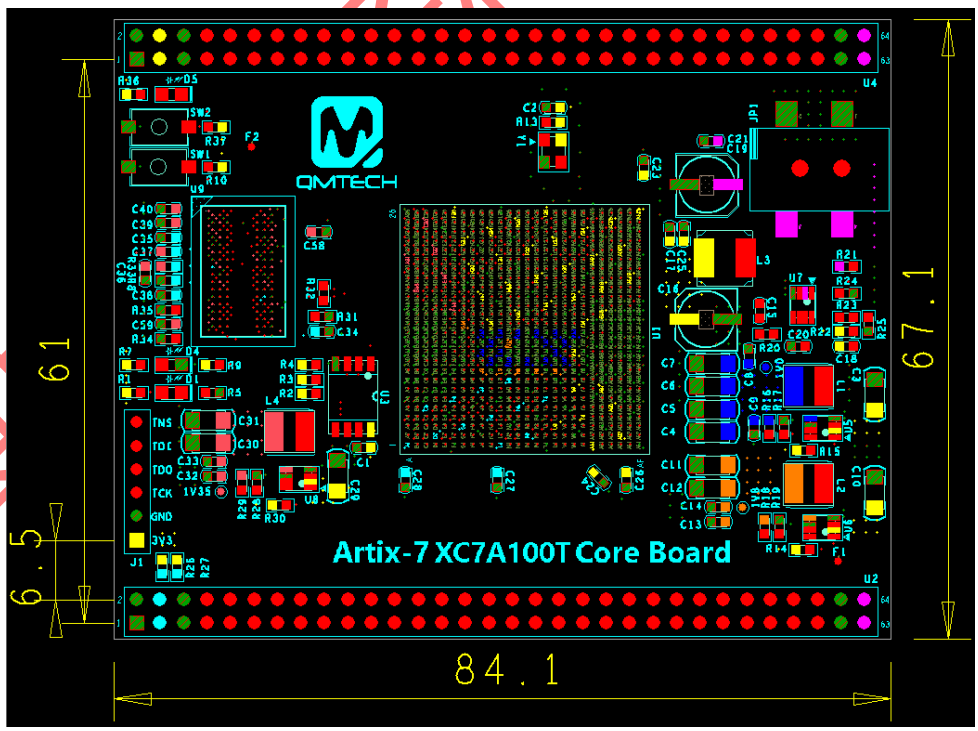


Figure 2-2. QMTECH XC7A100T Core Board Dimension

2.1 Install Development Tools

The QMTECH XC7A100T core board tool chain consists of Xilinx Vivado 2018.3, Xilinx USB platform cable, XC7A100T core board and 5V DC power supply. Below image shows the Xilinx Vivado 2018.3 development environment which could be downloaded from Xilinx office website:

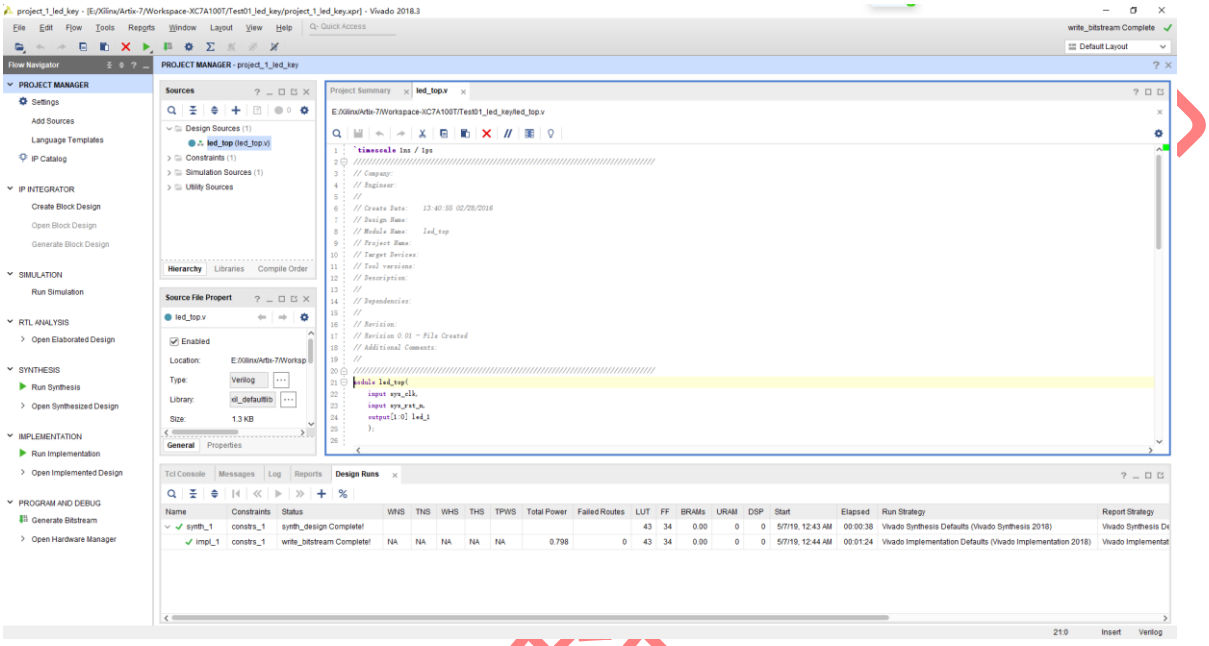


Figure 2-3. Vivado 2018.3

Below image shows the JTAG connection between Xilinx USB platform cable and XC7A100T core board:

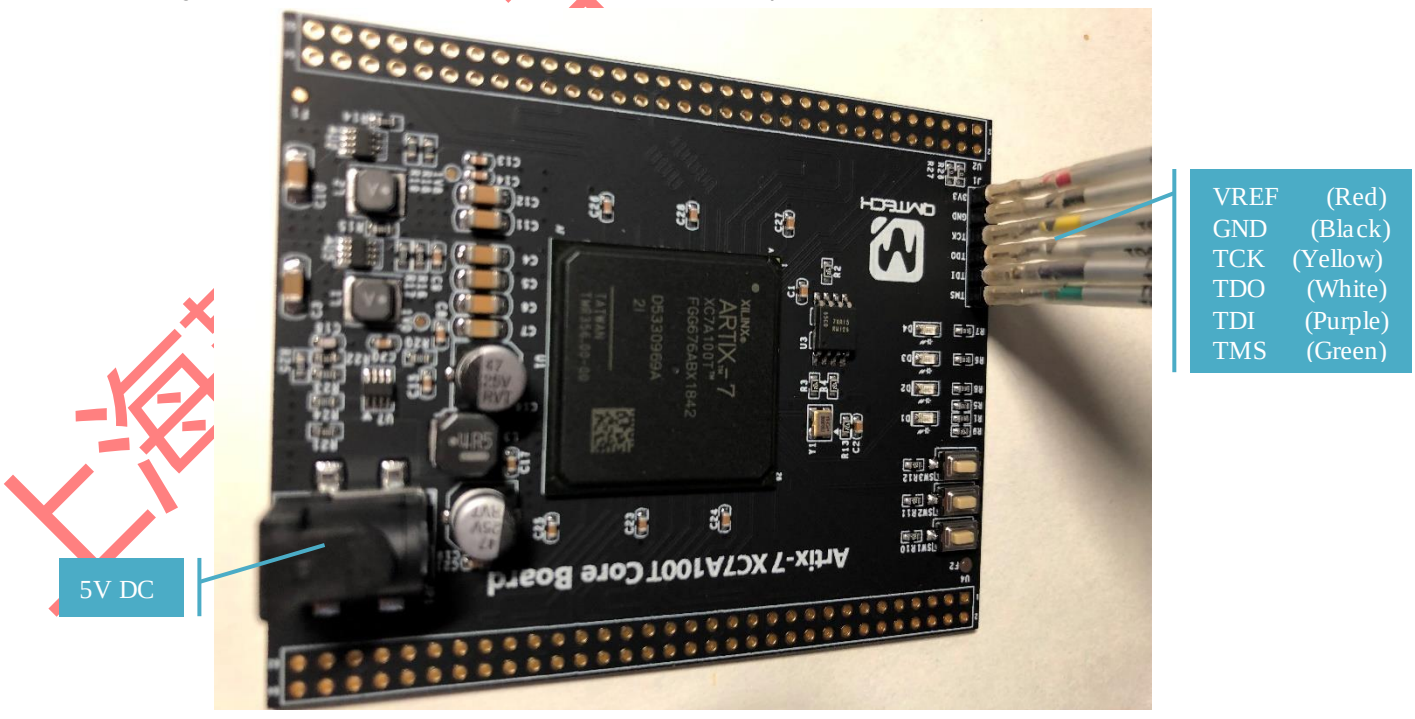


Figure 2-4. JTAG Connection and Power Supply

2.2 QMTECH XC7A100T Starter Kit Hardware Design

2.2.1 FPGA Power Supply

The core board needs 5V DC input as power supply which could be directly injected from power header or the 64P female header U2/U4. Users may refer to the hardware schematic for the detailed design. The on board LED D4 indicates the 3.3V supply, it will be turned on when the 5V power supply is active. In default status, all the FPGA banks IO power level is 3.3V because bank power supply is 3.3V. However, BANK34 and BANK35 IO's power level could be changed according to detailed custom requirement. There're two 0 ohm resisters could be removed: R26/R27, and instead the BANK34 and BANK35's power supply could be injected from 64P female header U8. Detailed design refers to hardware schematic.

Note: FPGA core supply 1.0V is regulated by Monolithic Power Systems, Inc. (MPS) DC/DC chip MP2143 which could output maximum 3A current.

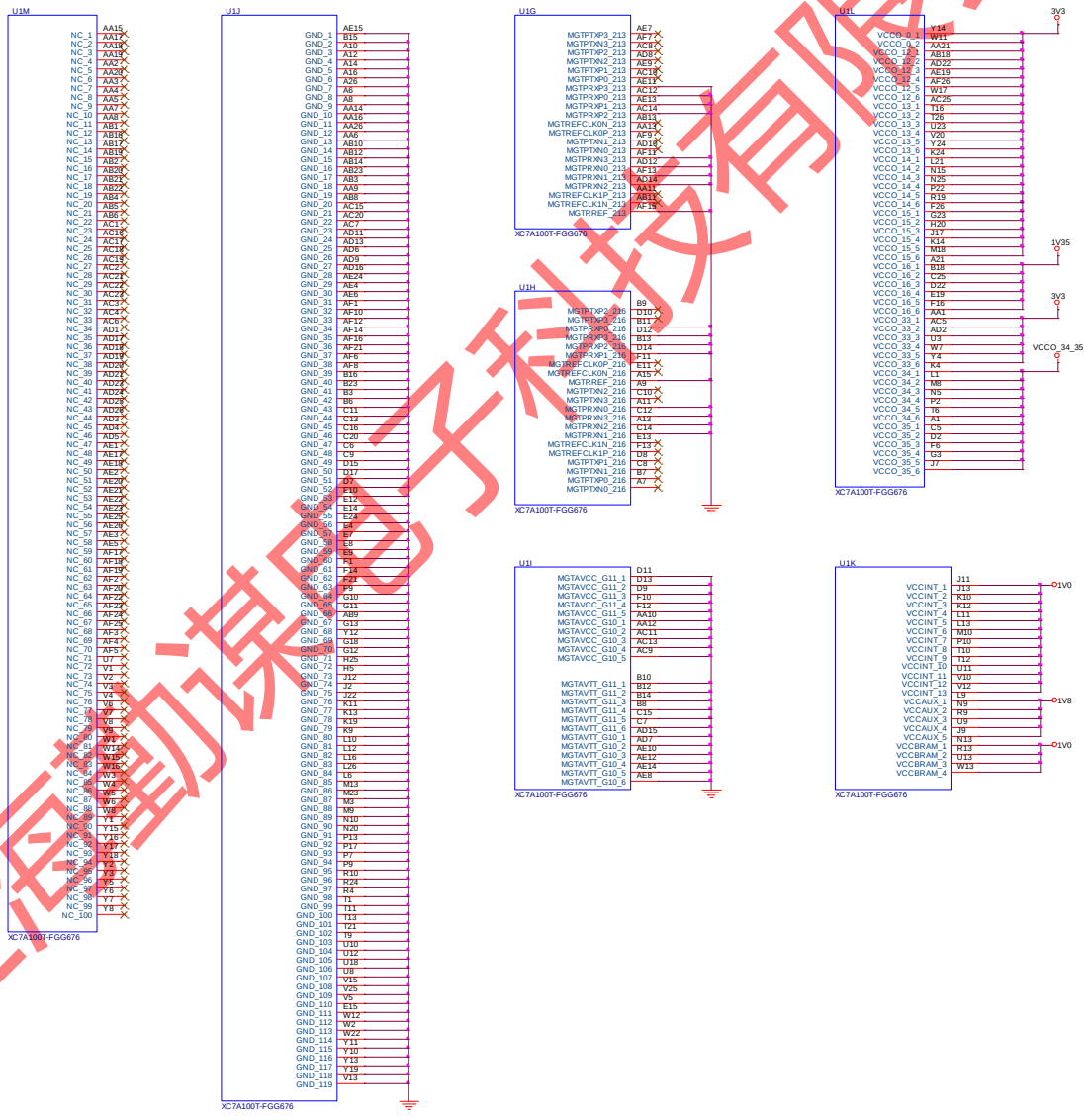


Figure 2-5. Power Supply for the FPGA

2.2.2 SPI Flash Boot

In default, the FPGA XC7A100T boots from external SPI Flash, detailed hardware design is shown in below figure. The SPI flash is using MT25QL128 manufactured by Micron, with 128Mbit memory storage.

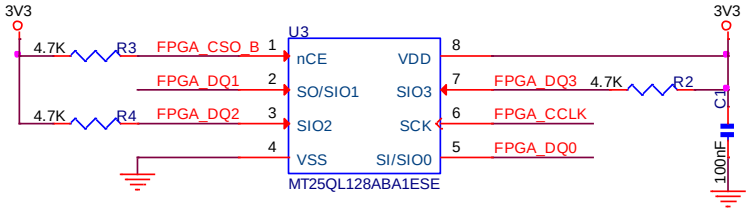


Figure 2-6. SPI Flash

The FPGA boot sequence setting M0:M1:M2 is configured as 1:0:0 which indicates FPGA will boot from SPI Flash after power on.

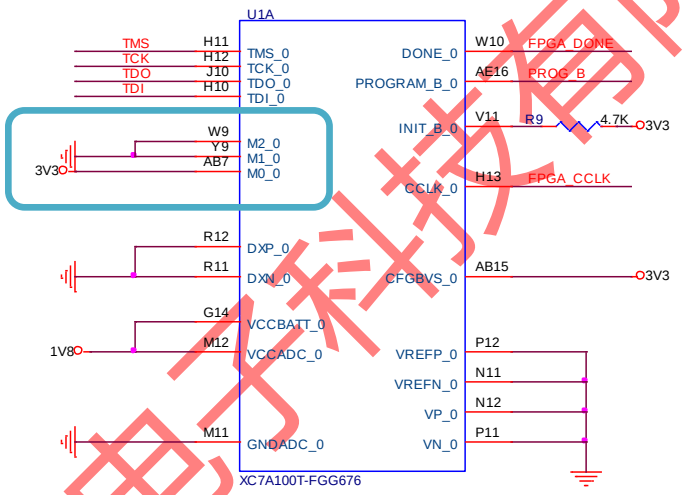


Figure 2-7. M0:M1:M2 Hardware Settings

The LED D1 will be turned on after the FPGA successfully loading configuration file from SPI Flash during power on stage. In this case, LED D1 could be used as FPGA loading status indicator.

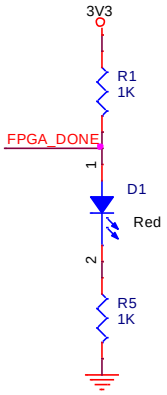


Figure 2-8. FPGA_DONE Status Indicator

2.2.3 System Clock

FPGA chip XC7A100T-2FTG676I has system clock frequency 50MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/° c. Below image shows the detailed hardware design:

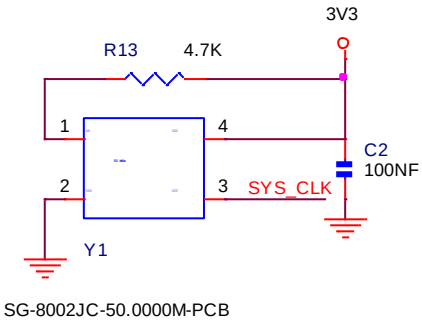
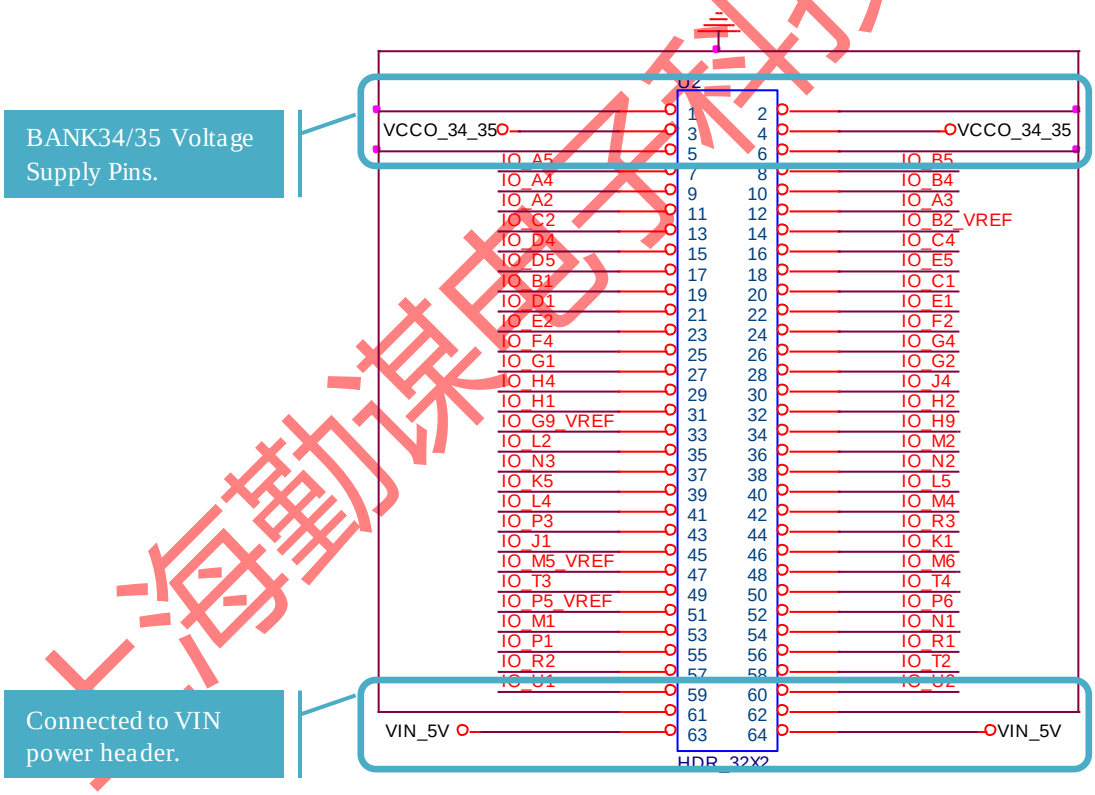


Figure 2-9. 50MHz System Clock

2.2.4 User Extension IOs

The core board has two 64P 2.54mm pitch female headers which are used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc.



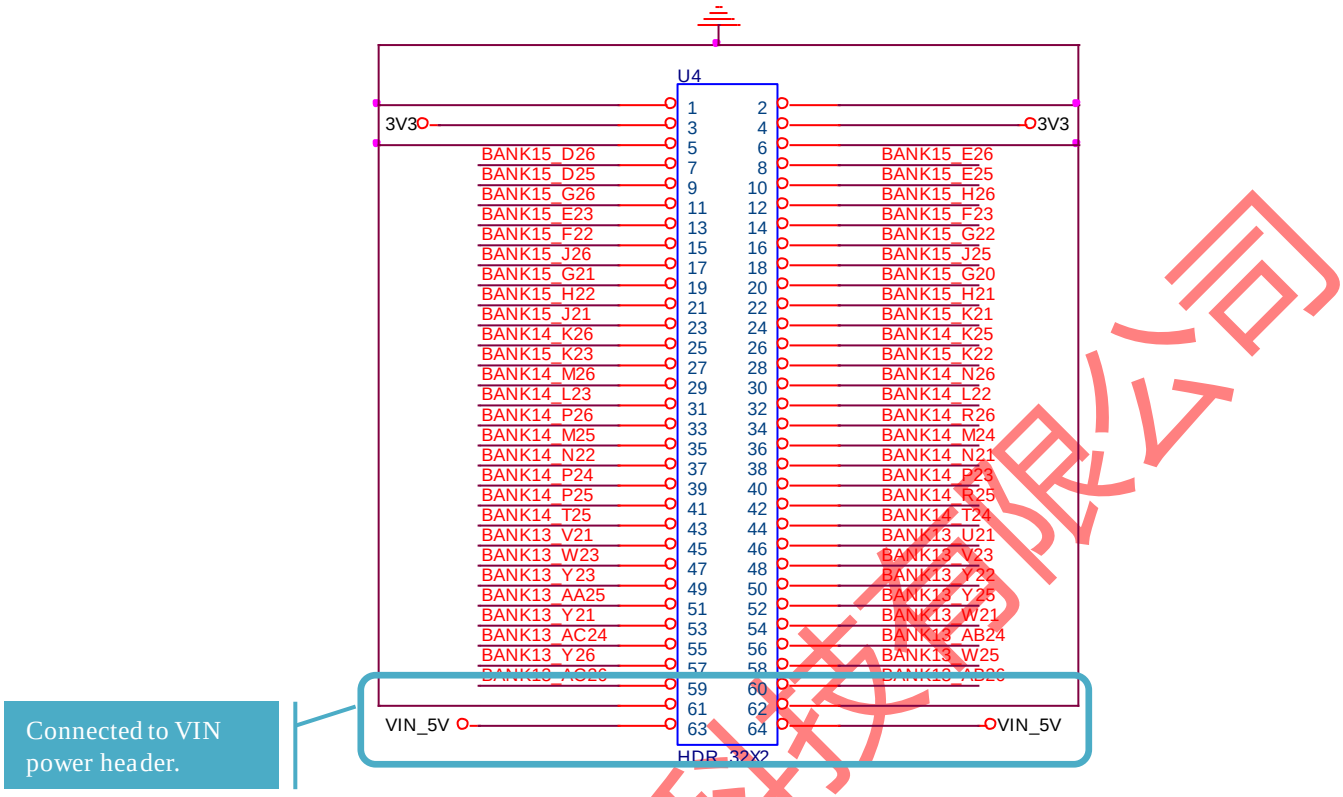


Figure 2-10. Extension IO

2.2.1 3.3V Power Supply

The core board's 3.3V power supply is using high efficiency DC/DC chip MP2315 provided by MPS Inc. The MP2315 supports wide voltage input range from 4.5V to 24V. In normal use case, 5V DC power supply is suggested to be applied on the board. Below image shows the MP2315 hardware design:

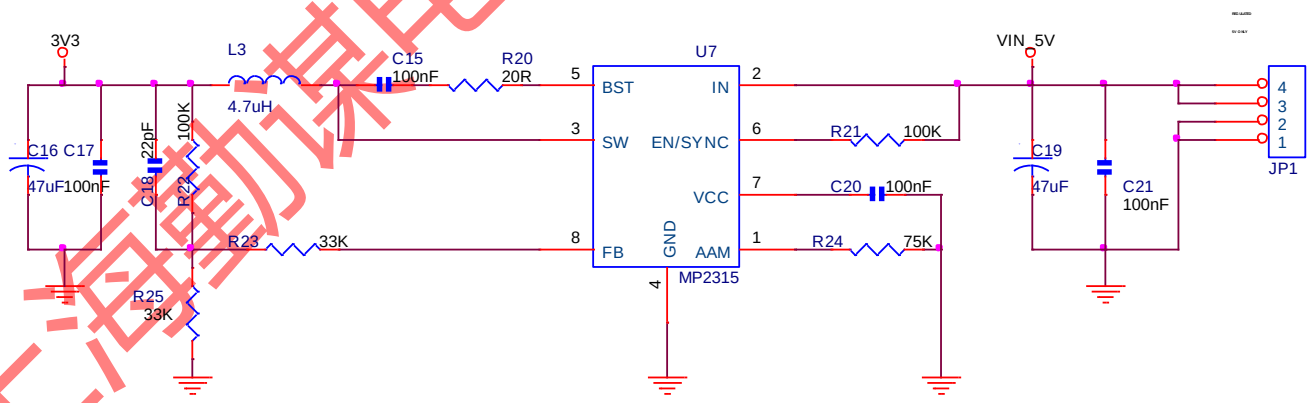


Figure 2-11. MP2315 Hardware Design

2.2.2 JTAG Port

The on board JTAG port uses 6P 2.54mm pitch header which could be easily connected to Xilinx USB platform cable. Below image shows the hardware design of the JTAG port:

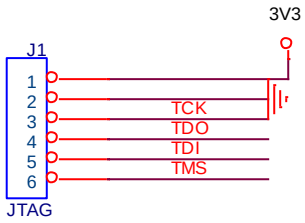


Figure 2-12. JTAG Port

2.2.3 User LEDs

Below image shows two user LEDs and 3.3V power supply indicator:

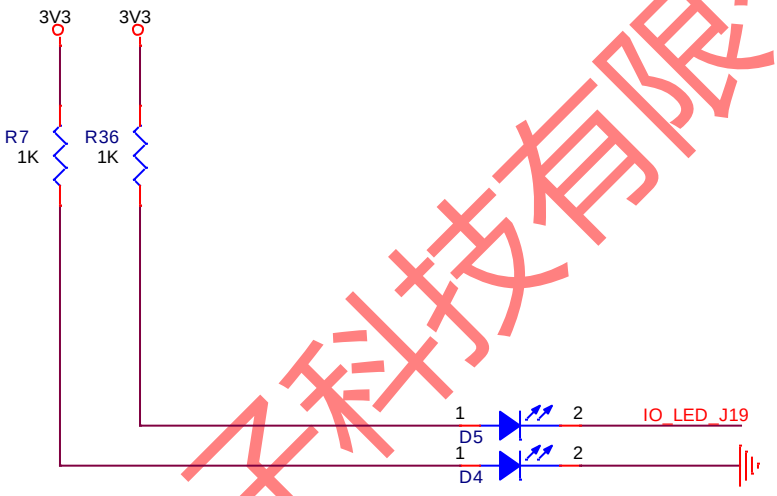


Figure 2-13. LEDs

2.2.4 User Keys

Below image shows the PROGRAM_B key and two user keys:

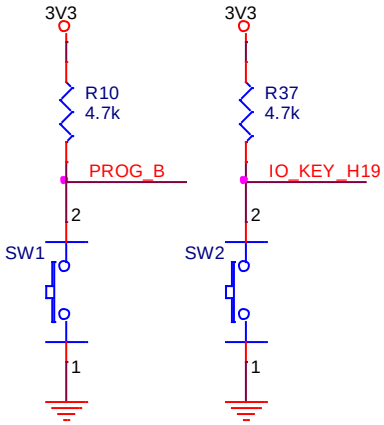


Figure 2-14. Keys

2.2.5 DDR3 Memory

The core board has on board 16bit width data bus, 256MB memory size DDR3 MT41K128M16JT-125:K provided by Micron. Below image shows the detailed hardware design:

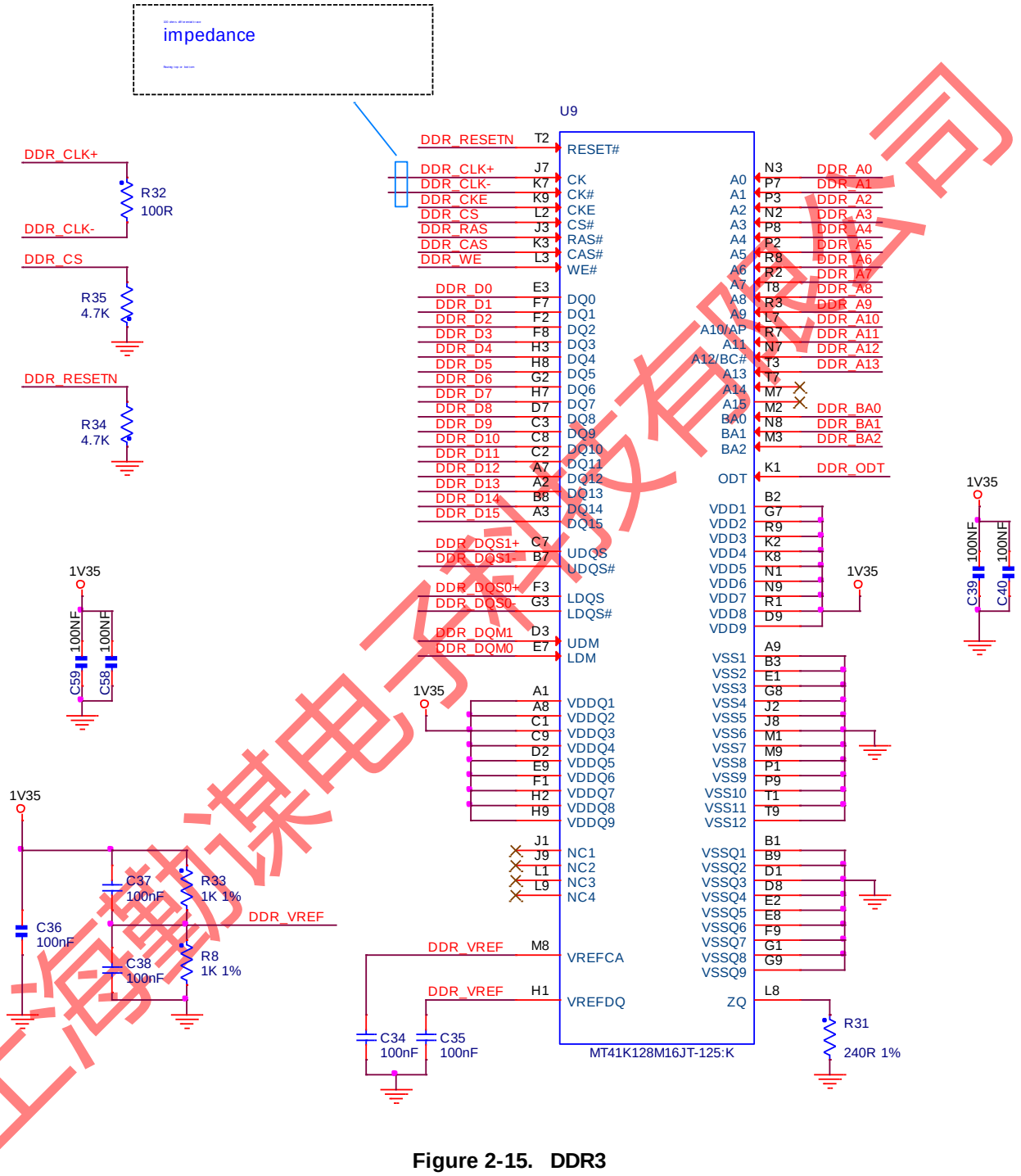


Figure 2-15. DDR3

3. Reference

[1] ug470_7Series_Config.pdf
[2] ds181_Artix_7_Data_Sheet.pdf
[3] ug475_7Series_Pkg_Pinout.pdf
[4] MT25Q_QLHS_L_128_ABA_0.pdf
[5] MT41J128M16JT-125K.pdf
[6] MP2315.pdf
[7] MP2143.PDF

4. Revision

Doc. Rev.	Date	Comments
0.1	01/09/2019	Initial Version.
1.0	03/09/2019	V1.0 Formal Release.