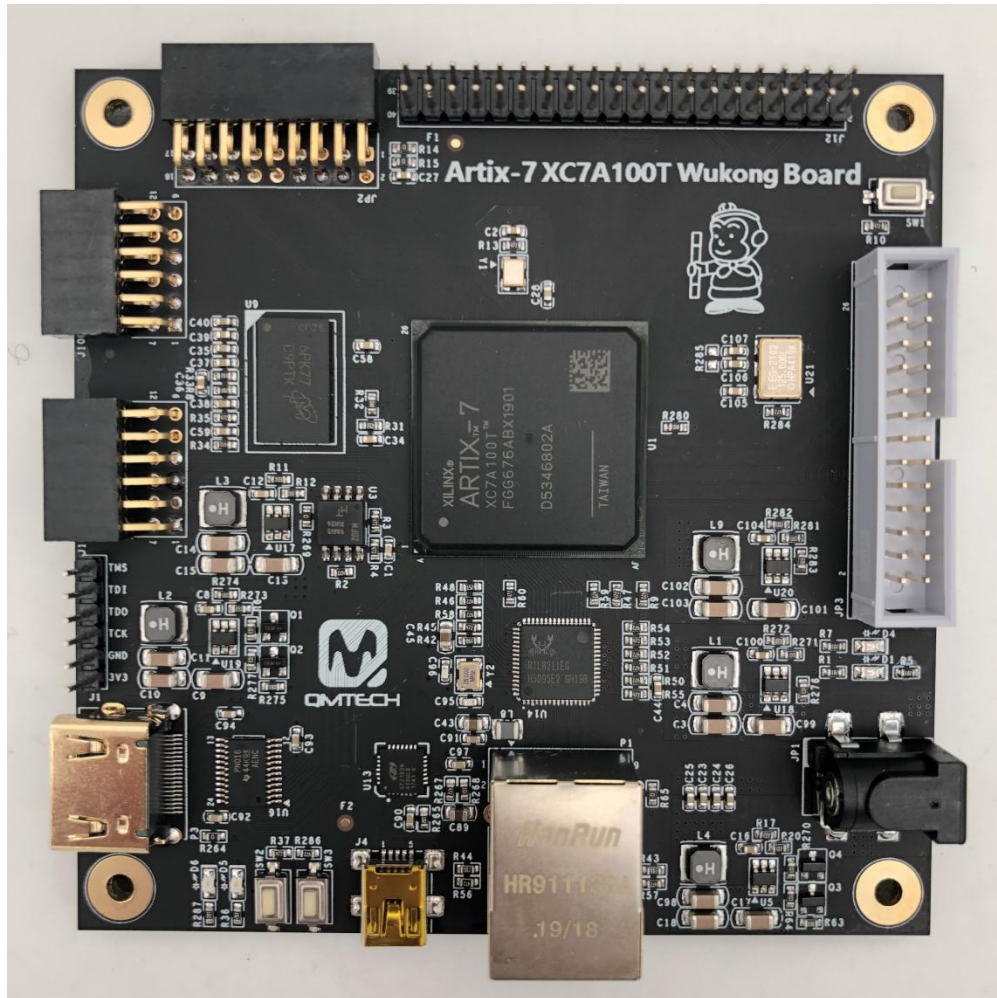# QMTECH XC7A100T WUKONG BOARD

USER MANUAL(EXPERIMENTS)

Preface

The QMTech® XC7A100T Wukong Board uses Xilinx Artix®-7 devices to demonstrate the highest performance-per-watt fabric, transceiver line rates, DSP processing, and AMS integration in a cost-optimized FPGA. Featuring the MicroBlaze™ soft processor and 1,066Mb/s DDR3 support, the family is the best value for a variety of cost and power-sensitive applications including software-defined radio, machine vision cameras, and low-end wireless backhaul.

For more information, updates and useful links, please visit QMTECH Official Website:

http://www.chinaqmtech.com

Table of Contents

1. QMTECH XC7A100T Wukong Board Introduction

1.1 Wukong Board Overview

QMTECH XC7A100T Wukong board provides several user interfaces to meet different customer needs. Below section lists the detailed info of these user interfaces:

➢ USB to UART Serial Port, by using Silicon Labs' CP2102N chip.

➢ HDMI display interface, by using TI's chip TPD12S016;

➢ GMII ethernet interface, by using Realtek's RTL8211EG chip;

➢ CMOS/CCD camera interface, by using 18pin female header;

➢ Two Digilent PMOD standard compatible female headers;

1.2 Wukong Board Top View

Below figure shows the top view of QMTECH XC7A100T Wukong Board. The board's dimension is 9.96mm x 9.96mm. All these functional chips' power supply is injected from the power header, detailed connection refer to the hardware schematic.
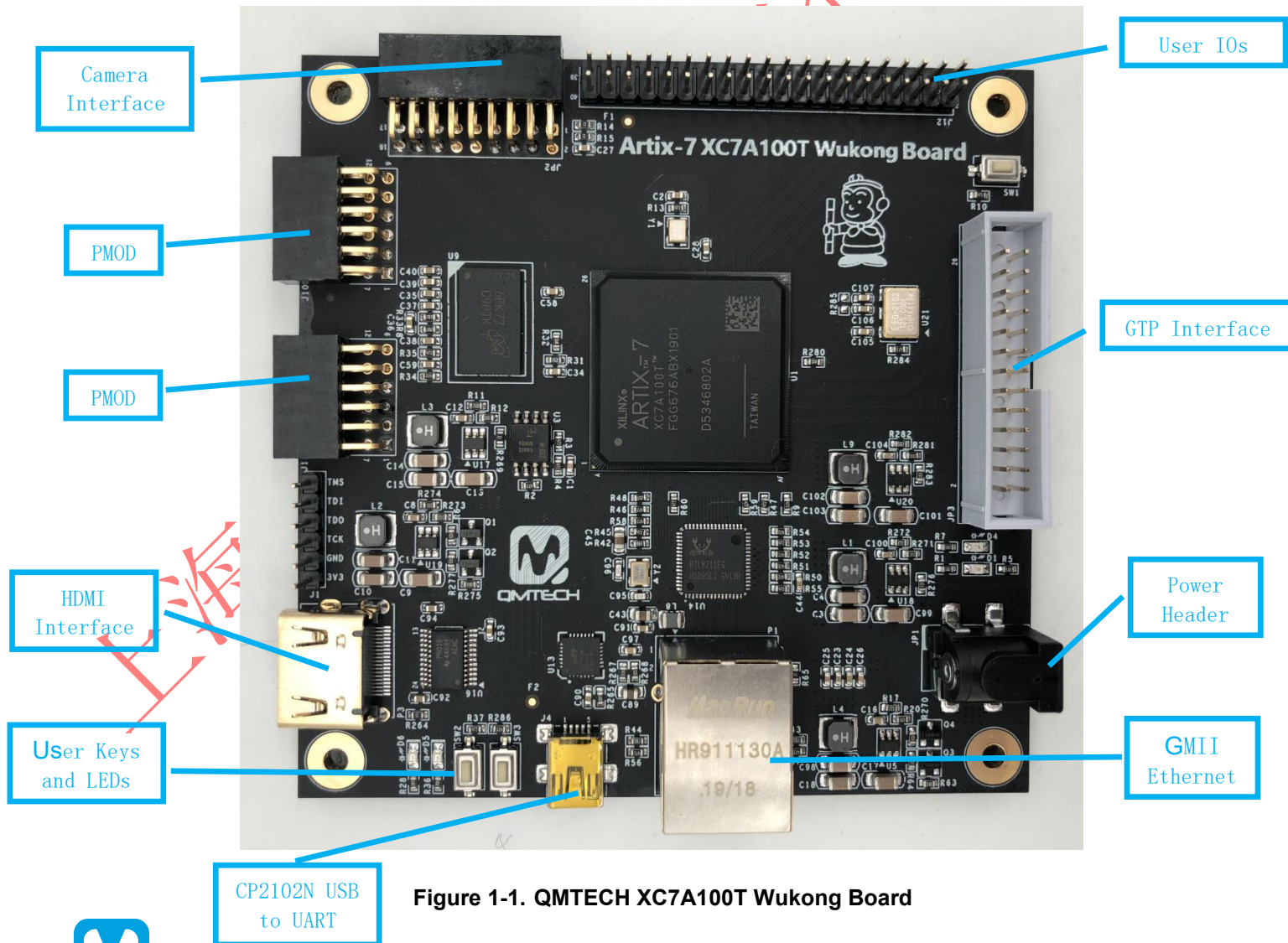

Figure 1-1. QMTECH XC7A100T Wukong Board

2.   Experiment (1): USB to Serial Port

The CP2102N is a USB 2.0 to serial port bridge chip designed by Silicon Labs. The CP2102N includes a USB 2.0 full-speed function controller, USB transceiver, oscillator, UART and eliminates the need for other external USB components are required for development. Below figure shows the hardware design of CP2102N on the QMTECH XC7A100T Wukong board.
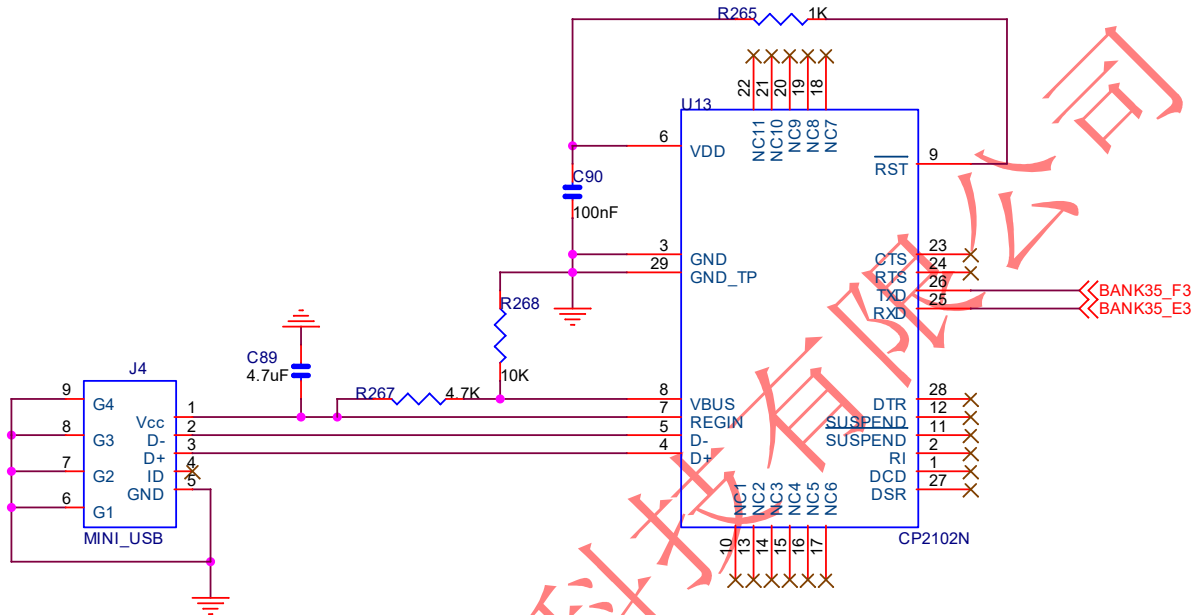

Figure 2-1. CP2102 Hardware Design

Before start to test the CP2102N's USB to UART serial communication function, make sure all the hardware connections of the development kit are correctly connected. Xilinx USB platform cable's VREF, GND, TDI, TMS, TCK, TDO pins shall be connected to XC7A100T board's JTAG interface. Then power on the development kit with 5V DC power source. Xilinx USB platform cable's indicator LED's color will turn from brown into green. At the same time, the Mini-USB cable shall also be plugged in the board, below figure shows an example hardware setup:

All the test examples are developed in the Vivado2018.3 environment. Open the CP2102 test project located in this release folder: /Software/Test05_usb_uart_cp2102. Below figure shows the project of **uart_top**:
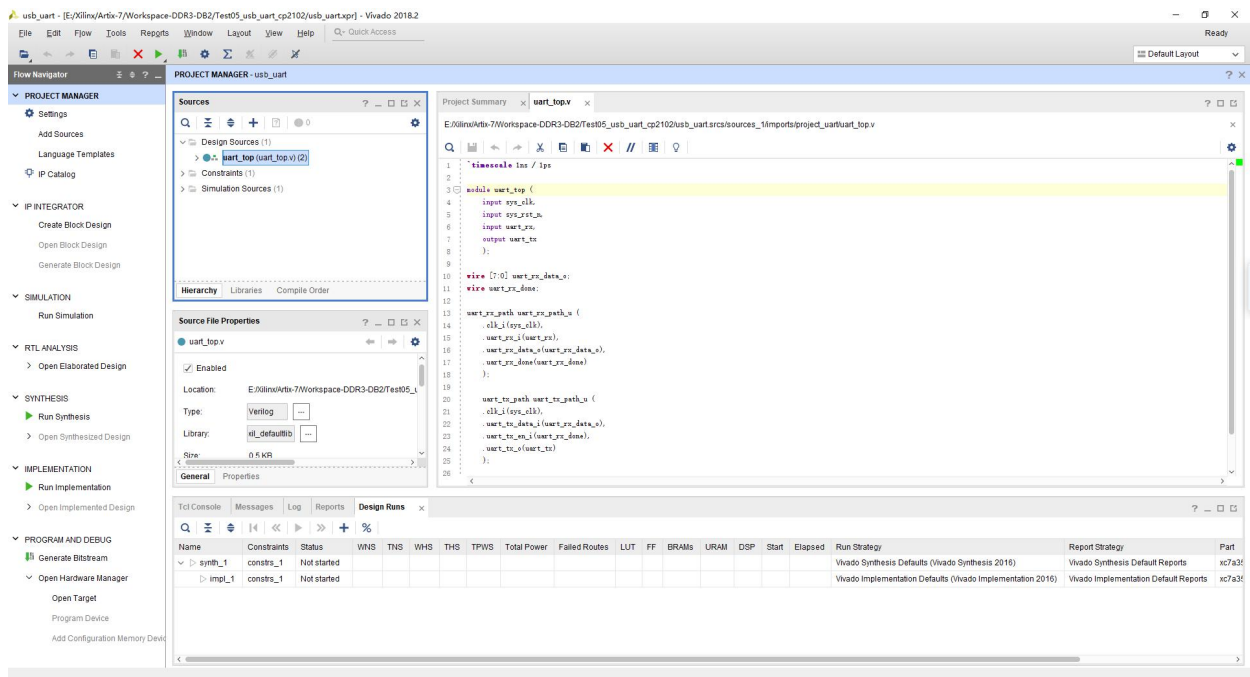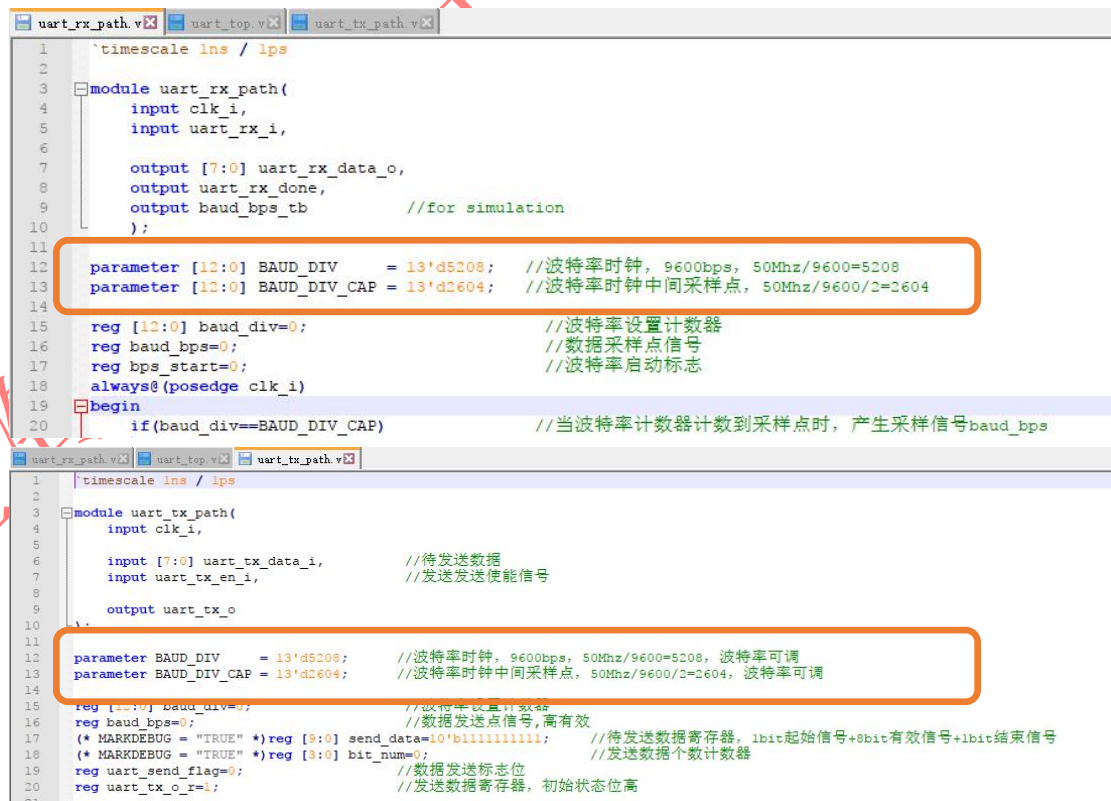

Figure 2-2. CP2102 UART Communication Test Example

In this example project, the default communication parameters are: 9600bps, 8 data bit, No Parity Check, 1 stop bit. If users want to test other communication parameters, change the source code accordingly.

After the CP2102 communication test project correctly synthesized, implemented and generated *.bit file, users could use Vivado 2018.3 program tool to program the generated *.bit file into FPGA. Below image shows the FPGA program status with program tool.
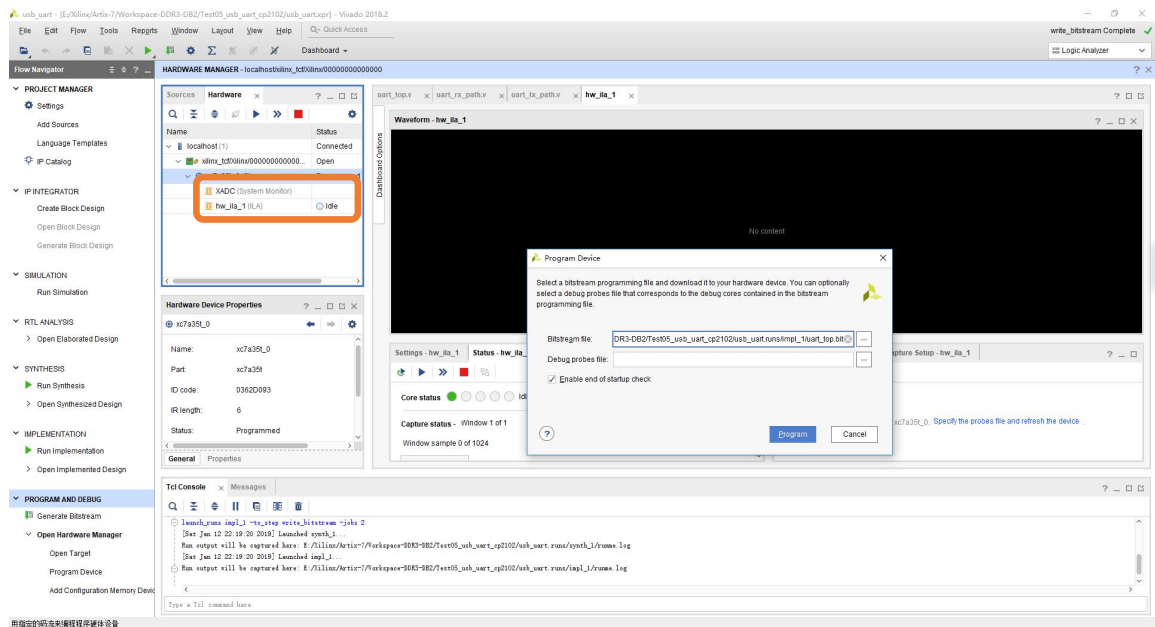

Figure 2-3. Program *.bit File

The CP2102 example test project's main functionality is performing an UART loopback communication. The FPGA program will send the received UART data back to the PC. Below figure shows user employees some PC based UART test tool to send data to FPGA: *http://www.cmsoft.cn QQ:10865600*. After a short while the PC UART test tool will receive the same data stream from FPGA, which means the CP2102 loopback test program is running correctly.

Figure 2-4. UART Loopback Test

3. Experiment (2): HDMI Displays

Transition Minimized Differential Signaling (TMDS) is used for transmitting video data over the High-Definition Multimedia Interface (HDMI). The XC7A100T Wukong Board uses TI's TPD12S016 chip, which is a single-chip High Definition Multimedia Interface (HDMI) device with auto-direction sensing I2C voltage level shift buffers, a load switch, and integrated low capacitance high-speed electrostatic discharge (ESD) transient voltage suppression (TVS) protection diodes. Below image shows the hardware design.
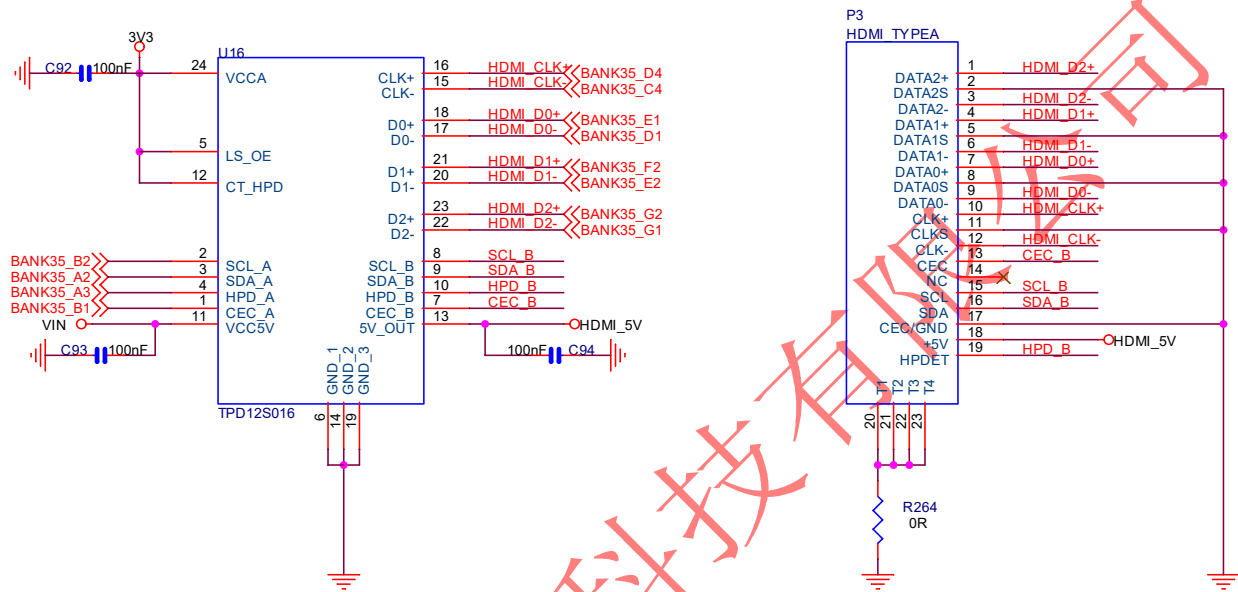

Figure 3-1. HDMI Display Hardware Designs

Before start to test the HDMI display function, make sure all the hardware connections of the development kit are correctly connected. Xilinx USB platform cable's VREF, GND, TDI, TMS, TCK, TDO pins shall be connected to XC7A100T board's JTAG interface. Then power on the development kit with 5V DC power source. Xilinx USB platform cable's indicator LED's color will turn from brown into green. At the same time, the HDMI cable shall also be plugged in the board, below figure shows an example hardware setup:
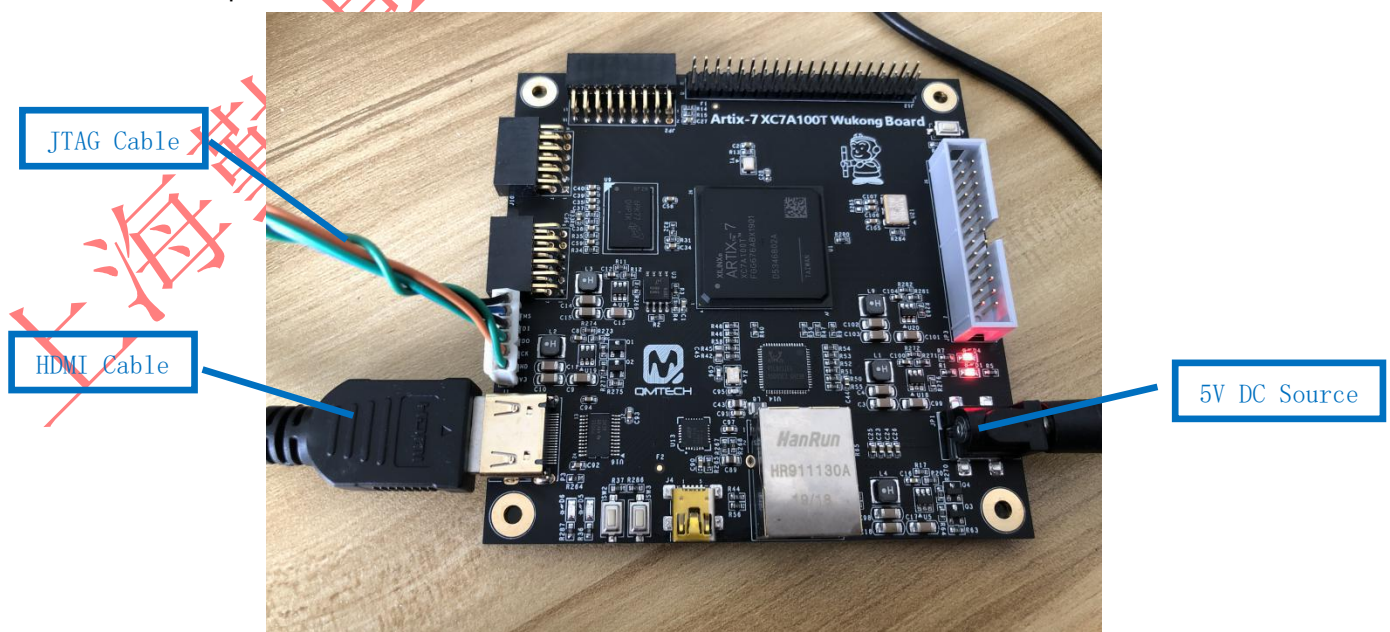
Open the HDMI test project located in this release folder: /Software/Test06_HDMI_OUT. Below figure shows the example project of Test06_HDMI_OUT:
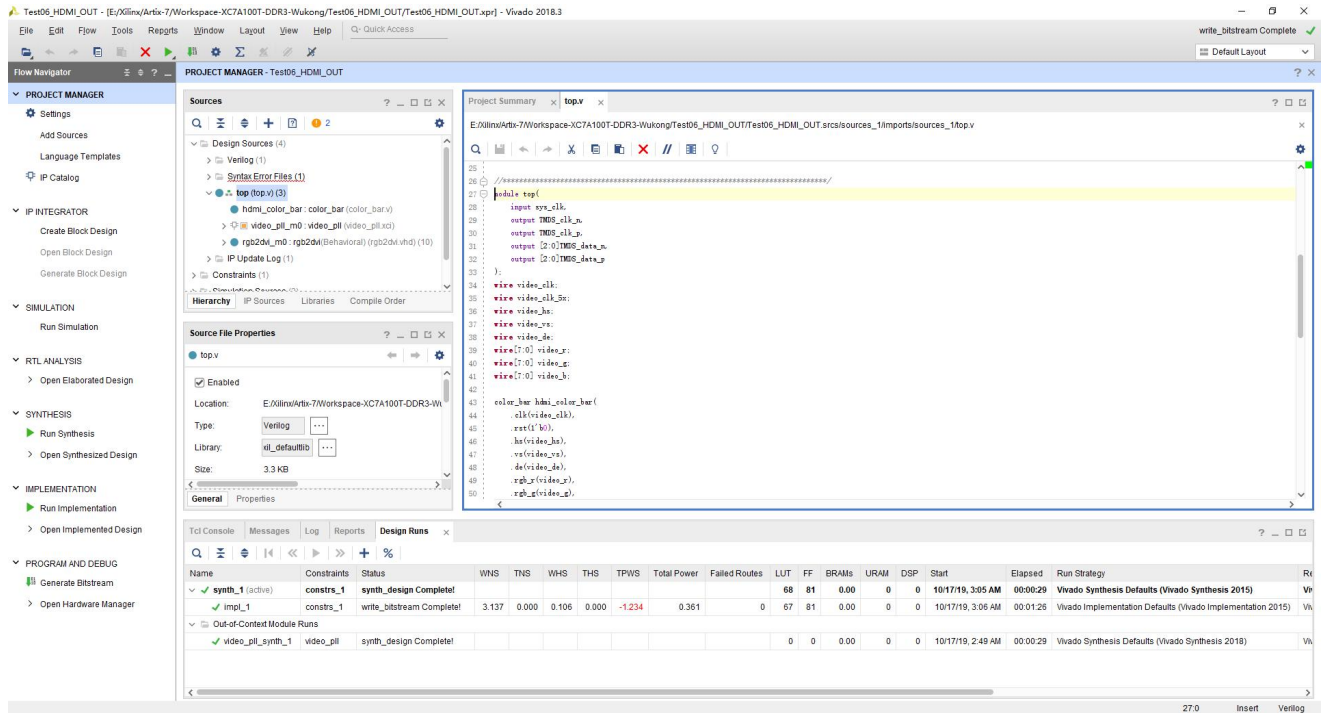

Figure 3-2. HDMI Display Function Test

After the HDMI display test project correctly synthesized, implemented and generated *.bit file, users could use Xilinx Vivado 2018.3 program tool to program the generated *.bit file into FPGA. Below image shows the FPGA program status with program tool.
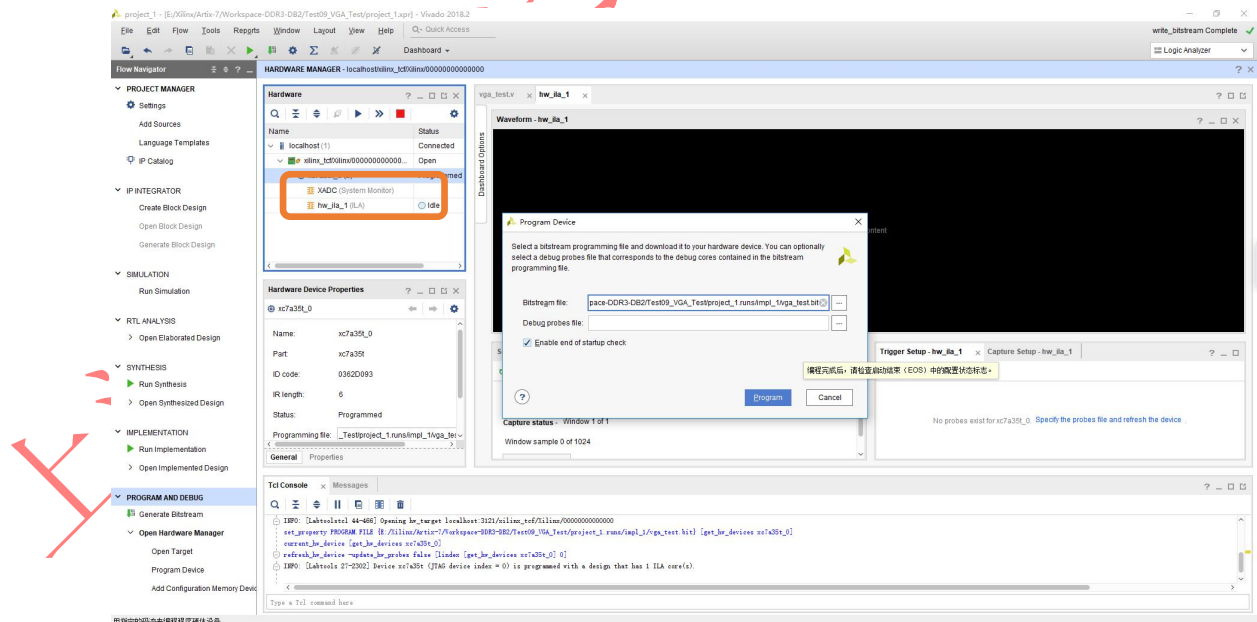

Figure 3-3. Program FPGA

After the FPGA correctly loaded the top.bit file, the HDMI monitor will display color bar pattern. Below image shows the example color bar pattern.
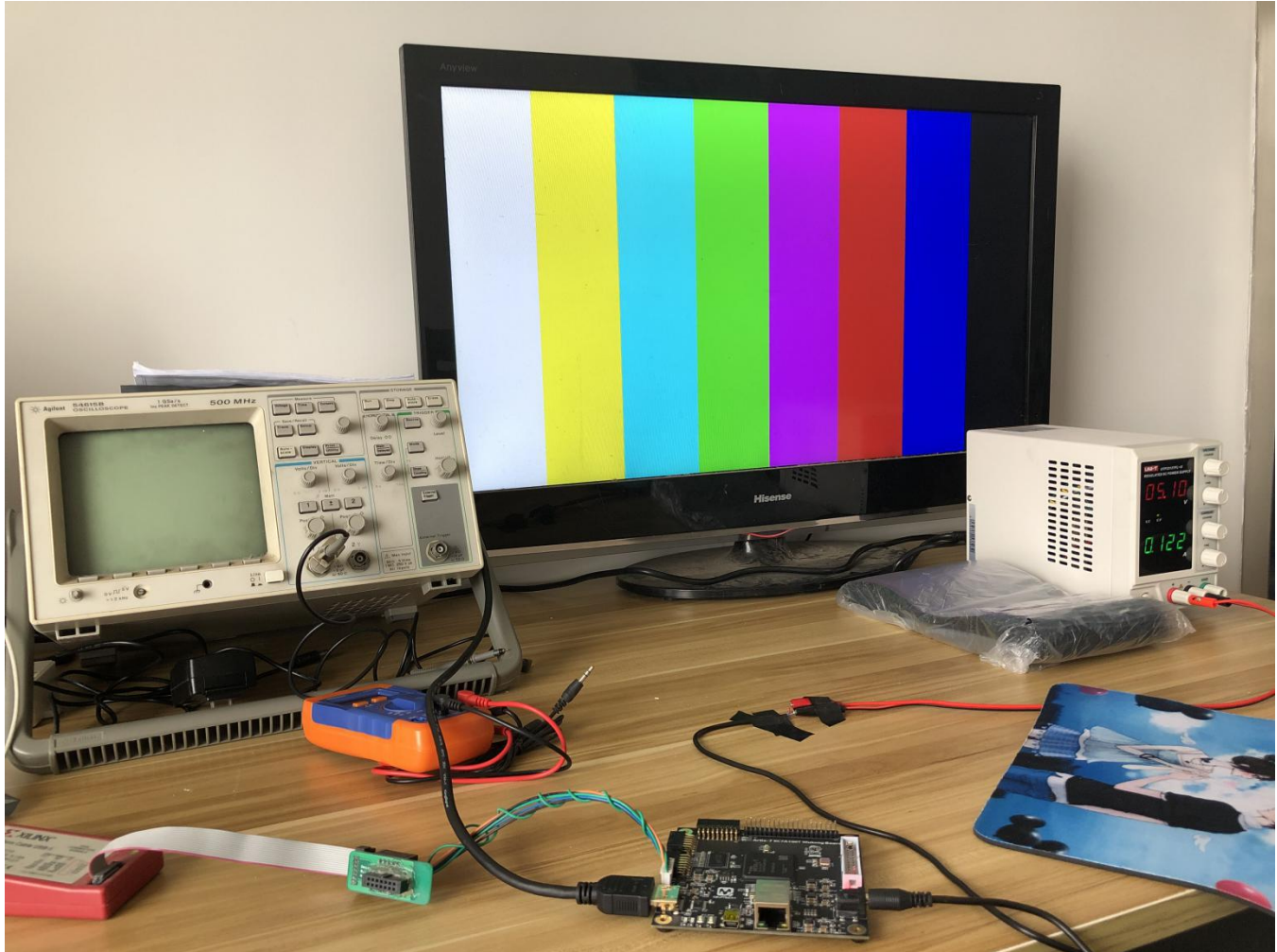

Figure 3-4. HDMI Display Test

4. Experiment (3): GMII Ethernet Test

The XC7A100T board uses RTL8211EG to implement the 10M/100M/1000M triple speed ethernet interface. It provides all the necessary physical layer functions to transmit and receive ethernet packets over the CAT.5 UTP cable. The data transfer between PHY and FPGA is via the Gigabit Media Independent Interface(GMII) for 1000Base-T. The RTL8211EG-VB chip supports 3.3V signaling for GMII interface. Below image shows the hardware design of RTL8211EG:
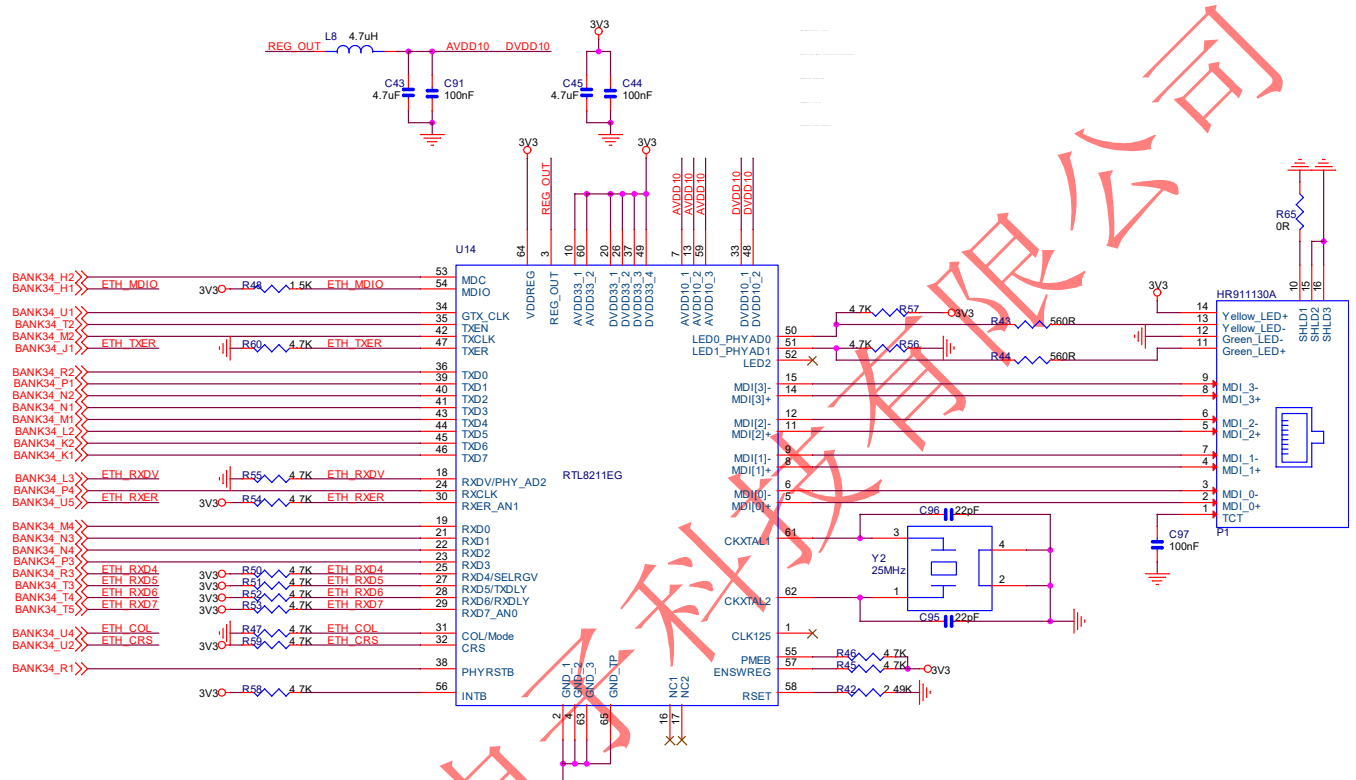

Figure 4-1. RTL8211 Hardware Design

Before start to test the GMII ethernet communication function, make sure all the hardware connections of the development kit are correctly connected. Xilinx USB Platform cable shall be connected to XC7A100T board's JTAG interface. The ethernet cable shall be plugged in the board and the test computer simultaneously. Then power on the development kit with 5V DC power source. Below figure shows an example hardware setup:
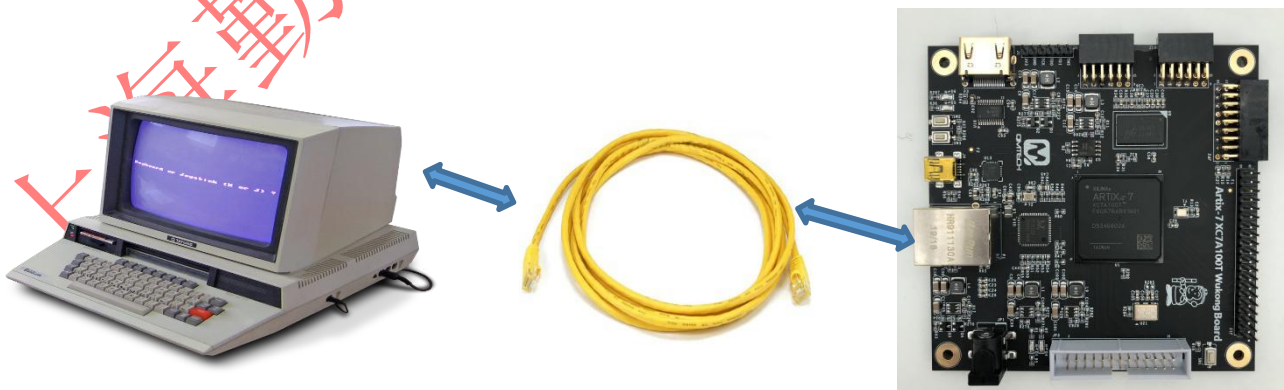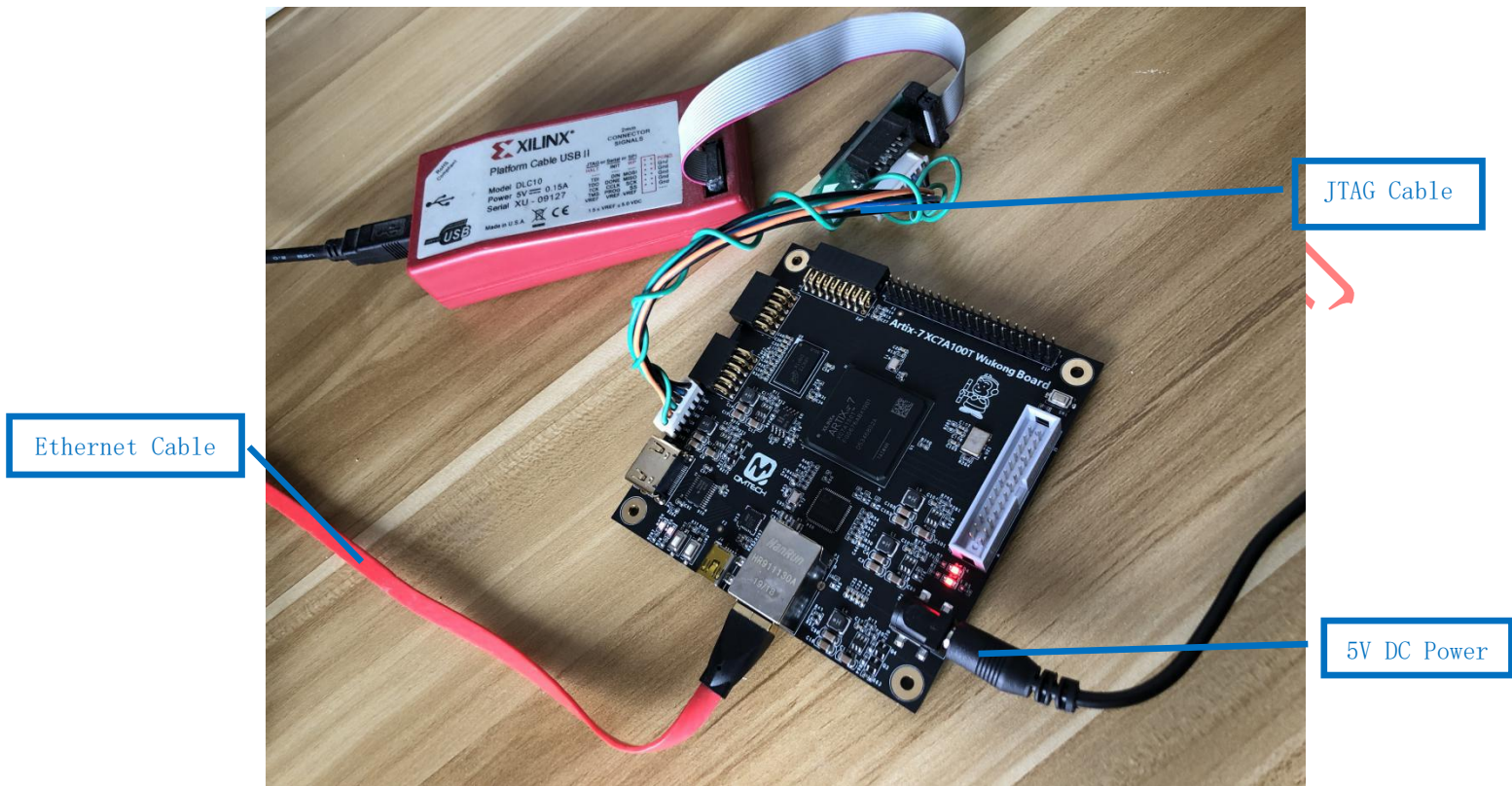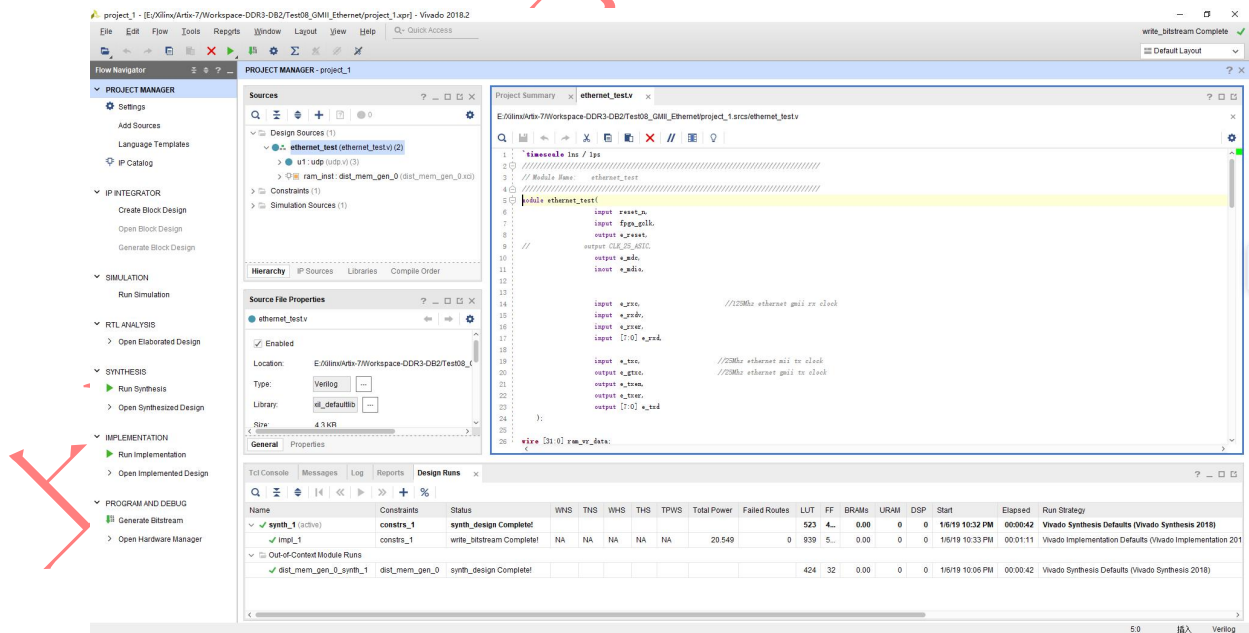
Figure 4-2. Test Setup

Use Vivado2018.3 to open the GMII ethernet test project located in this release folder: /Software/ Test08_GMII_Ethernet. Below figure shows the example project of ethernet_test:

After the ethernet test project correctly synthesized, implemented and generated *.bit file, users could use Vivado 2018.3 program tool to program the generated *.bit file into FPGA. Below image shows the FPGA program status with program tool.
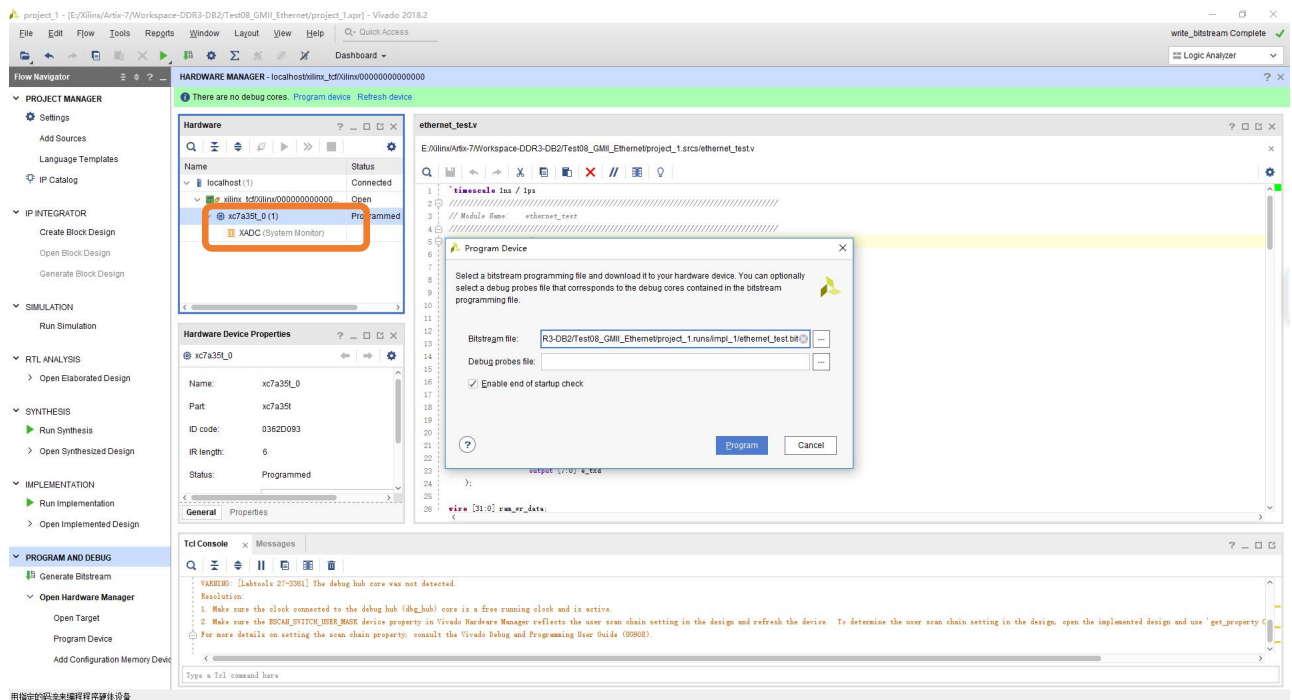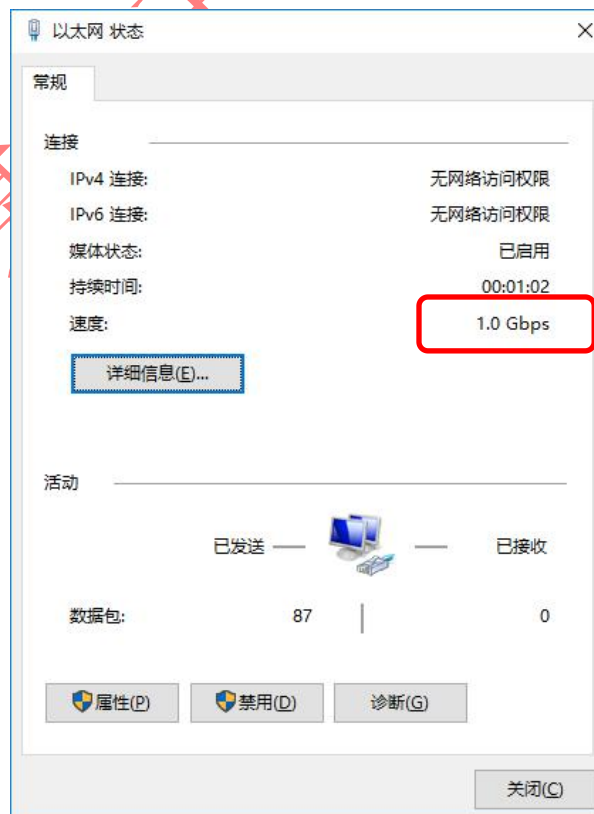

Figure 4-3. FPGA Program

Users could check the ethernet connection status in the Windows OS. Below images shows the ethernet communication speed between the FPGA development board and the test computer is 1Gbps based.

In order to finish this ethernet test, users need to set the Windows's Static IP into 192.168.0.3:
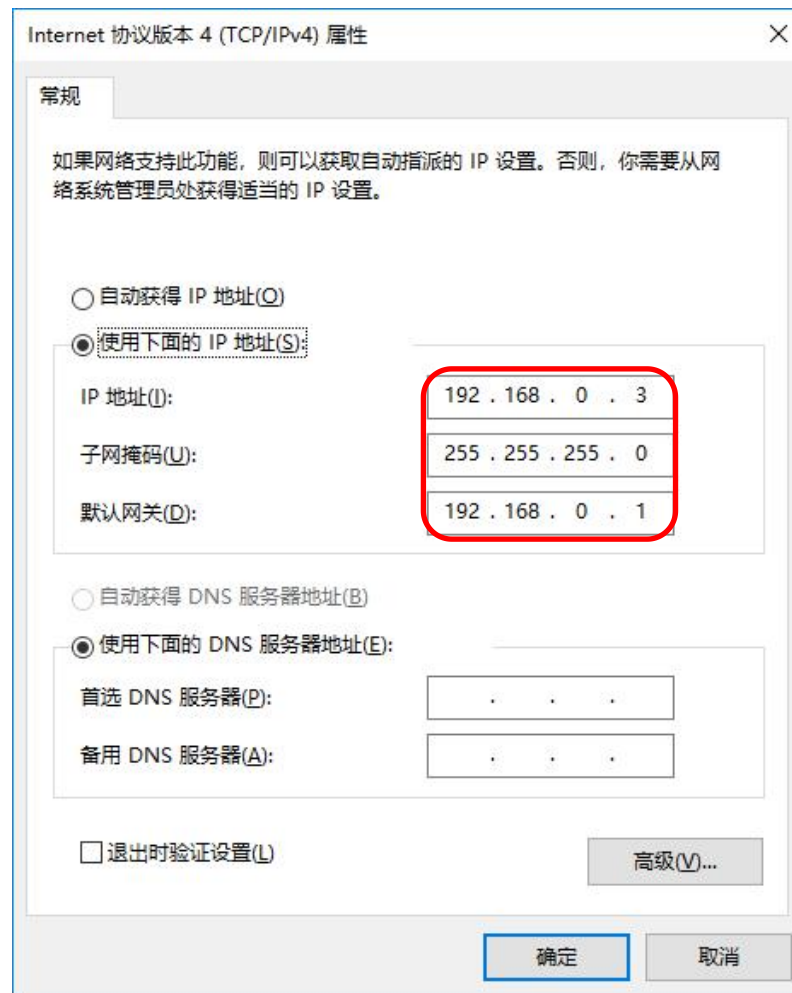

Figure 4-4. Configure Test PC's IP

Run Windows Command Console as administrator. In that DOS type command window bind the development board's IP address(192.168.0.2) and MAC address (00-0a-35-01-fe-c0) by typing command: ARP -s 192.168.0.2 00-0a-35-01-fe-c0:

Figure 4-5. Binding IP and MAC

Open the NetAssist ethernet debug tool and set the communication parameters as shown in below figure. The NetAssist tool will receive the test data "HELLO QMTECH BOARD" sent from development board. Then press the【Send】button to send the test data *http://www.cmsoft.cn QQ:10865600* to the FPGA development board. In response, the FPGA will send back test data to the test PC.
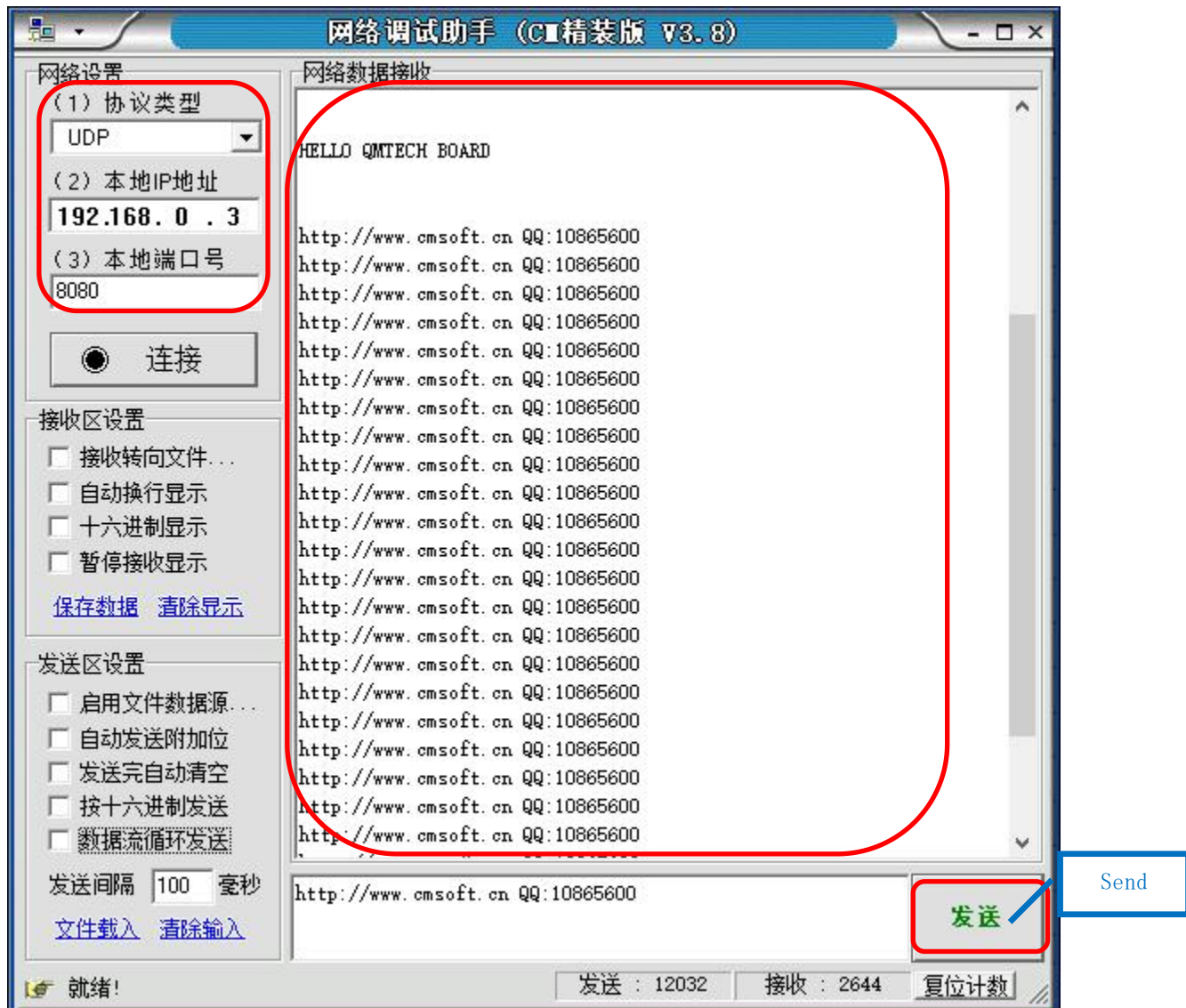

Figure 4-6. GMII Ethernet Test Result

5.   Reference

[1] ug470_7Series_Config.pdf
[2] ds181_Artix_7_Data_Sheet.pdf
[3] ug475_7Series_Pkg_Pinout.pdf
[4] n25q_64a_3v_65nm.pdf
[5] MT41J128M16JT-125K.pdf

6. Revision

Doc. Rev.	Date	Comments
0.1	21/11/2019	Initial Version.
1.0	25/11/2019	V1.0 Formal Release.