

# OTA Design Using $g_m/i_d$ Method in Open-Source GF180MCU Process

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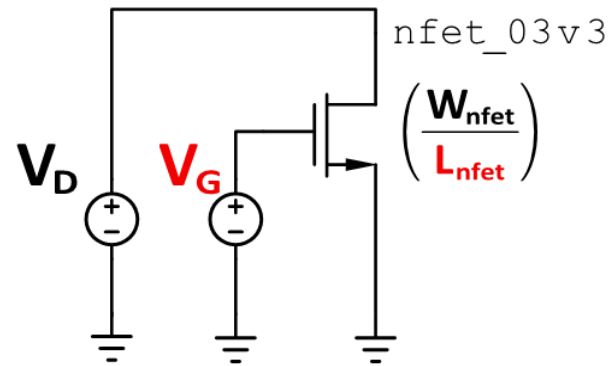
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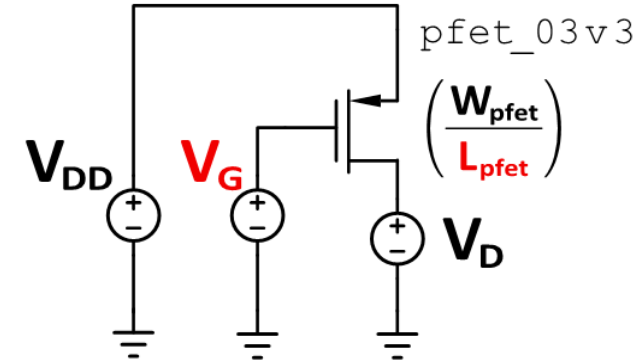
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# Creating LUT

## NMOS Testbench



## PMOS Testbench

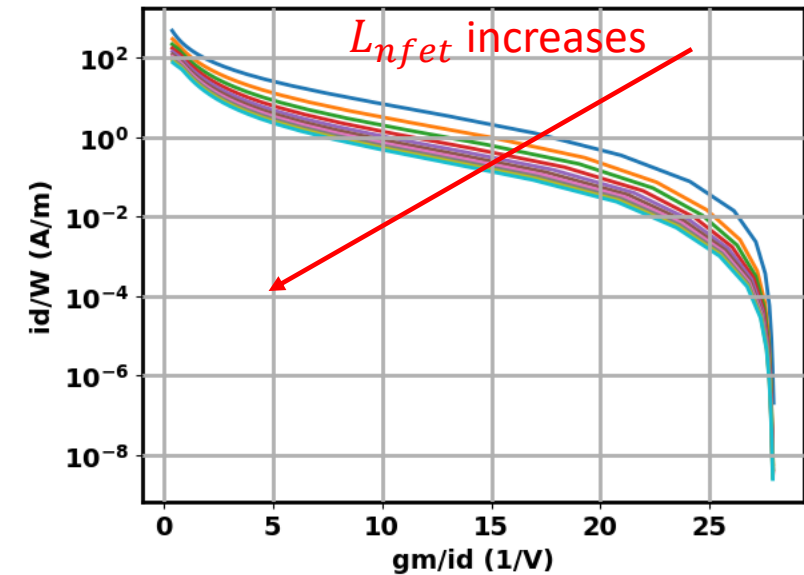
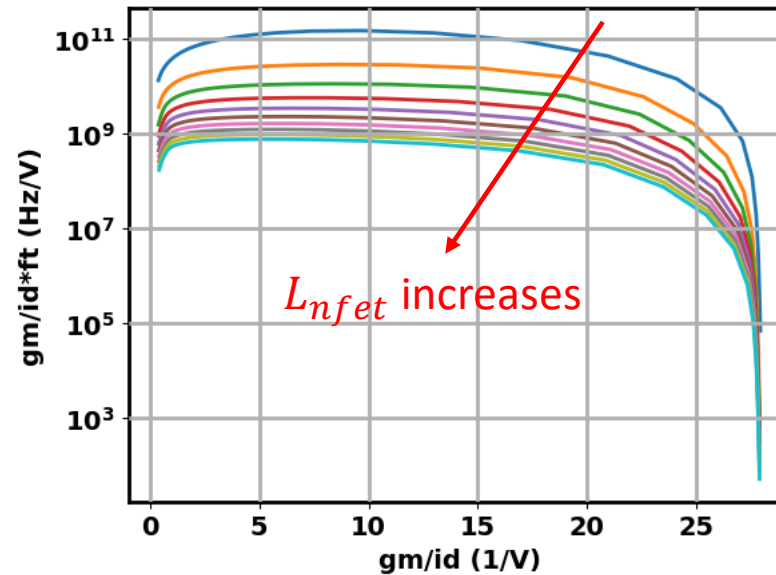
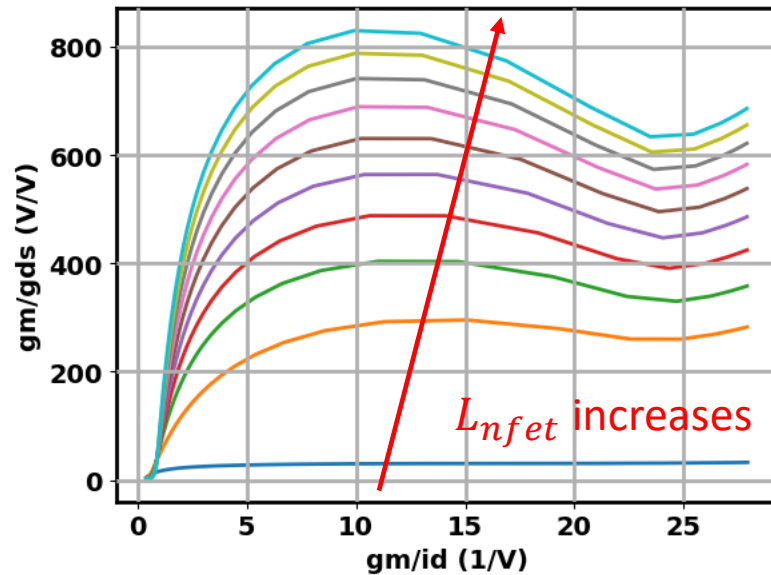


- In GF180MCU,  $V_{DD} = 3.3\text{ V}$
- In both testbenches:
  - Set  $V_D = \frac{V_{DD}}{2} = 1.65\text{ V}$ ,  $W_{nfet} = 4\text{ }\mu\text{m}$  (which does not matter here, can be any other reasonable value)
  - Sweep  $V_G$  from 0 to 3.3 V (step size up to you)
  - Sweep  $L_{nfet}$  from 0.28  $\mu\text{m}$  to 0.4  $\mu\text{m}$  (step size up to you)

# Creating LUT

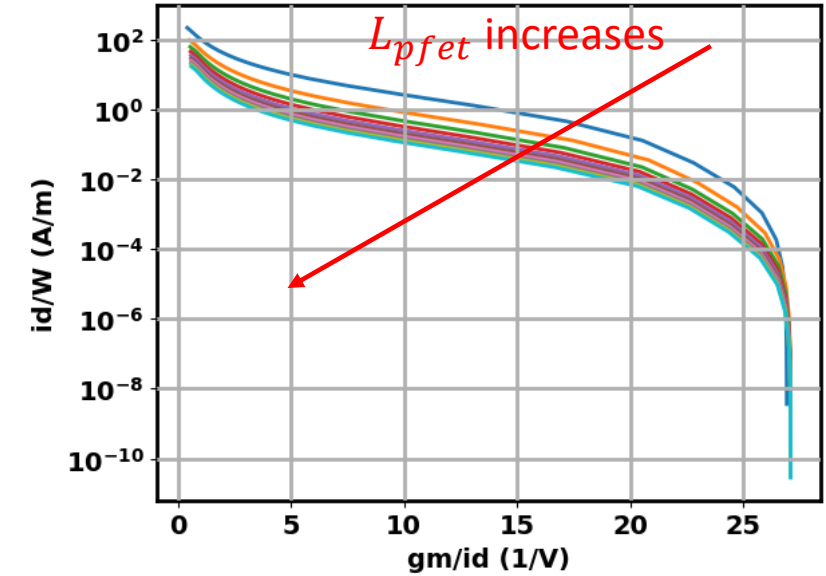
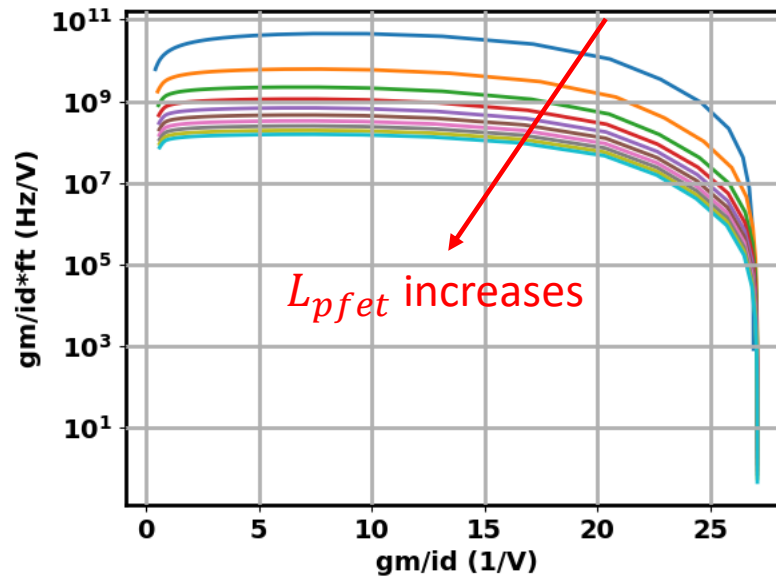
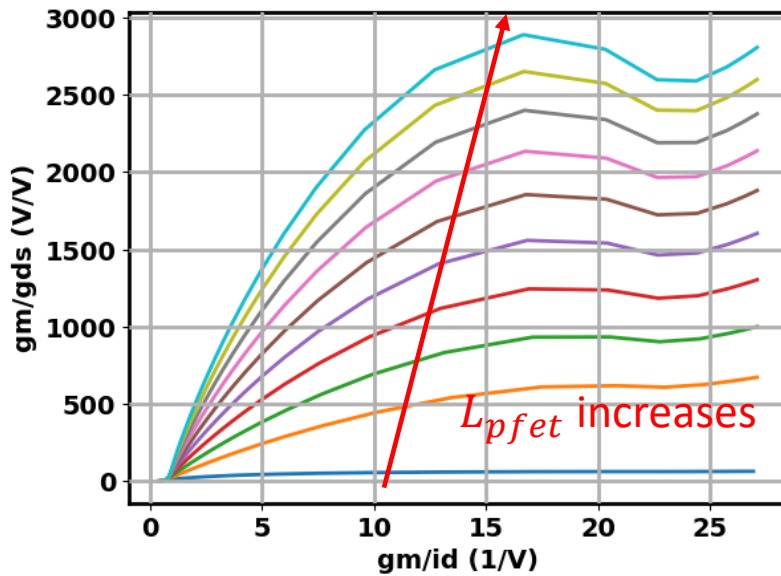
- Generating three key plots:
  - $i_d/W$  vs  $g_m/i_d$  (current density, tells you the efficiency of how much current you pay for the transconductance; used for sizing purpose)
  - $g_m/g_{ds}$  vs  $g_m/i_d$  (for gain requirement)
  - $f_t * g_m/i_D$  vs  $g_m/i_d$  (for best GBW requirement, usually it tells the optimal  $g_m/i_D$  range)

# Creating LUT - NMOS



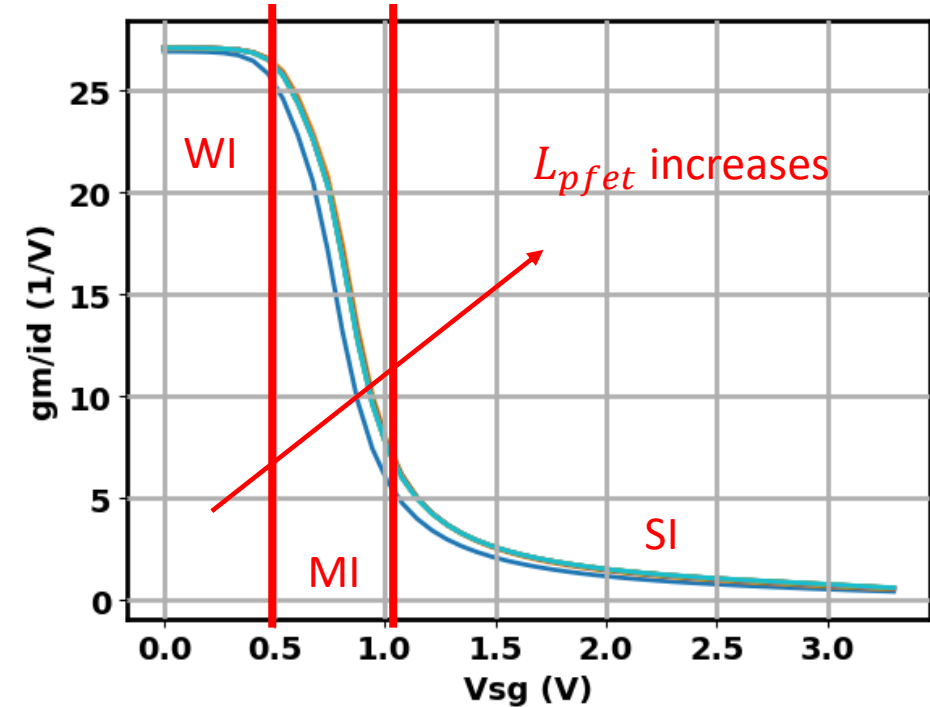
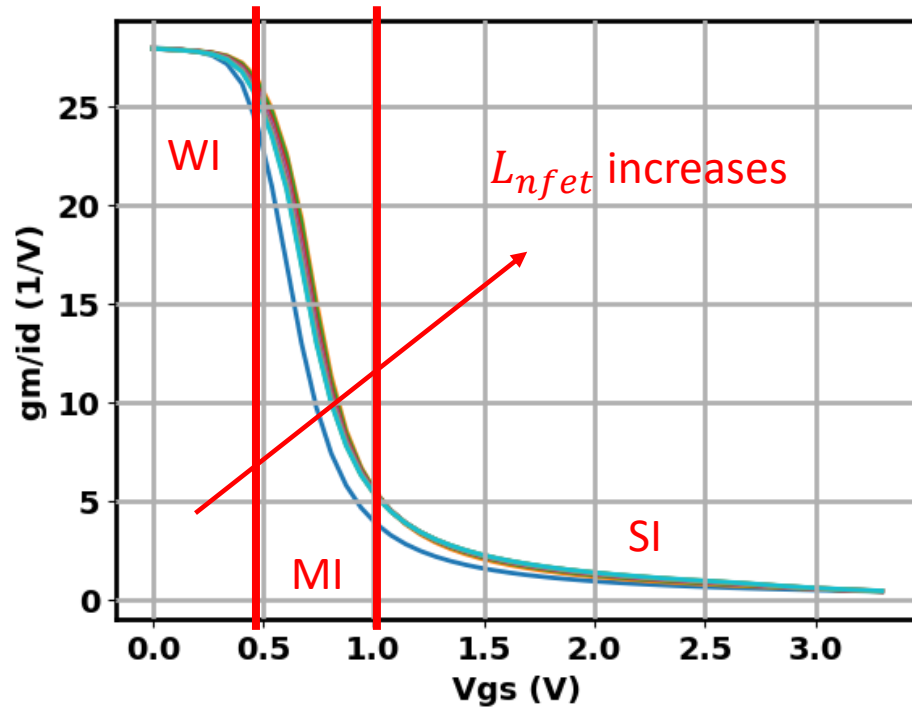
- Increasing  $L$  will increase the gain
- Increasing  $L$  will decrease  $f_t$
- Increasing  $L$  will decrease current density

# Creating LUT - PMOS



- With same  $g_m/i_d$ , PMOS has higher intrinsic gain than NMOS
- With same  $g_m/i_d$ , PMOS is slower than NMOS
- With same  $g_m/i_d$ , PMOS has lower current density

# $g_m/i_d$ vs. $V_{gs}$ (NMOS, $V_{sg}$ for PMOS)



- By choosing different  $g_m/i_d$ , transistors are biased in different region
  - Weak-inversion (WI): low-power
  - Strong-inversion (SI): high-speed
  - Moderate-inversion (MI): a good compromise between WI and SI

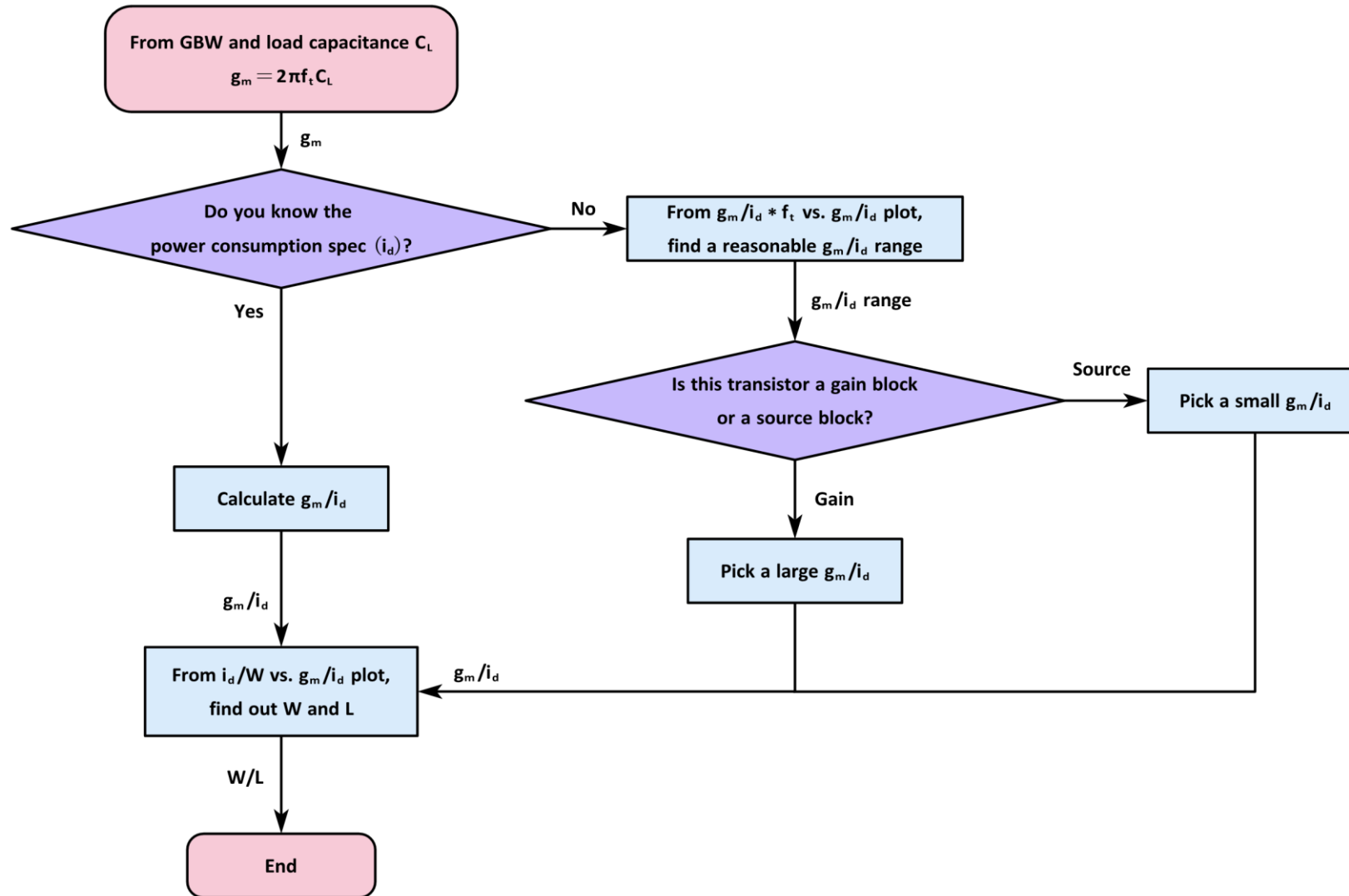
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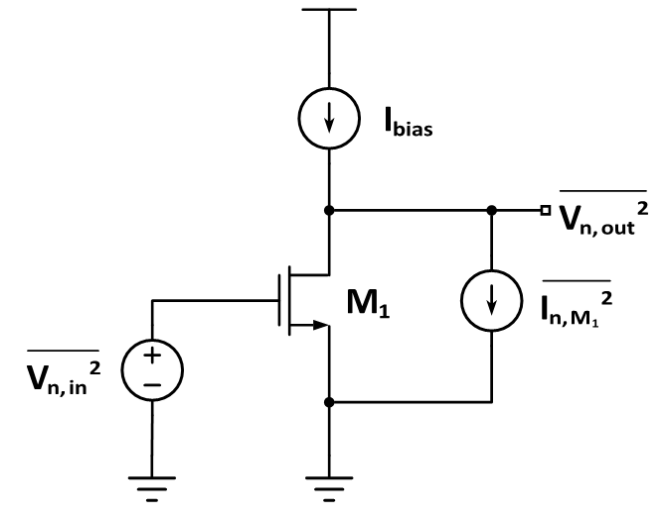


# Simplified Design Algorithm Using $g_m/i_d$ Method



# Choice of large and small $g_m/i_d$

- Why you want large  $g_m/i_d$  for gain stage, but small  $g_m/i_d$  for biasing/source?
- Transistor current noise:  $\overline{I_{n,M_1}^2} = 4kT\gamma g_{m,M_1} \approx \frac{8}{3}kT g_{m,M_1}$ 
  - The larger  $g_m$ , transistor itself is noisier. When it is used as a current source, we want the noise smaller, therefore smaller  $\frac{g_m}{i_d}$ .
- When this noise is input-referred:
  - $\overline{V_{n,out}^2} = \overline{I_{n,M_1}^2} r_{o,M_1}^2 \approx \frac{8}{3}kT g_m r_{o,M_1}^2$
  - $\overline{V_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{g_{m,M_1}^2 r_{o,M_1}^2} \approx \frac{8}{3} \frac{kT}{g_{m,M_1}}$
  - Therefore, when it is used as a gain stage, by increasing  $g_m$ , the input-referred noise is decreasing.

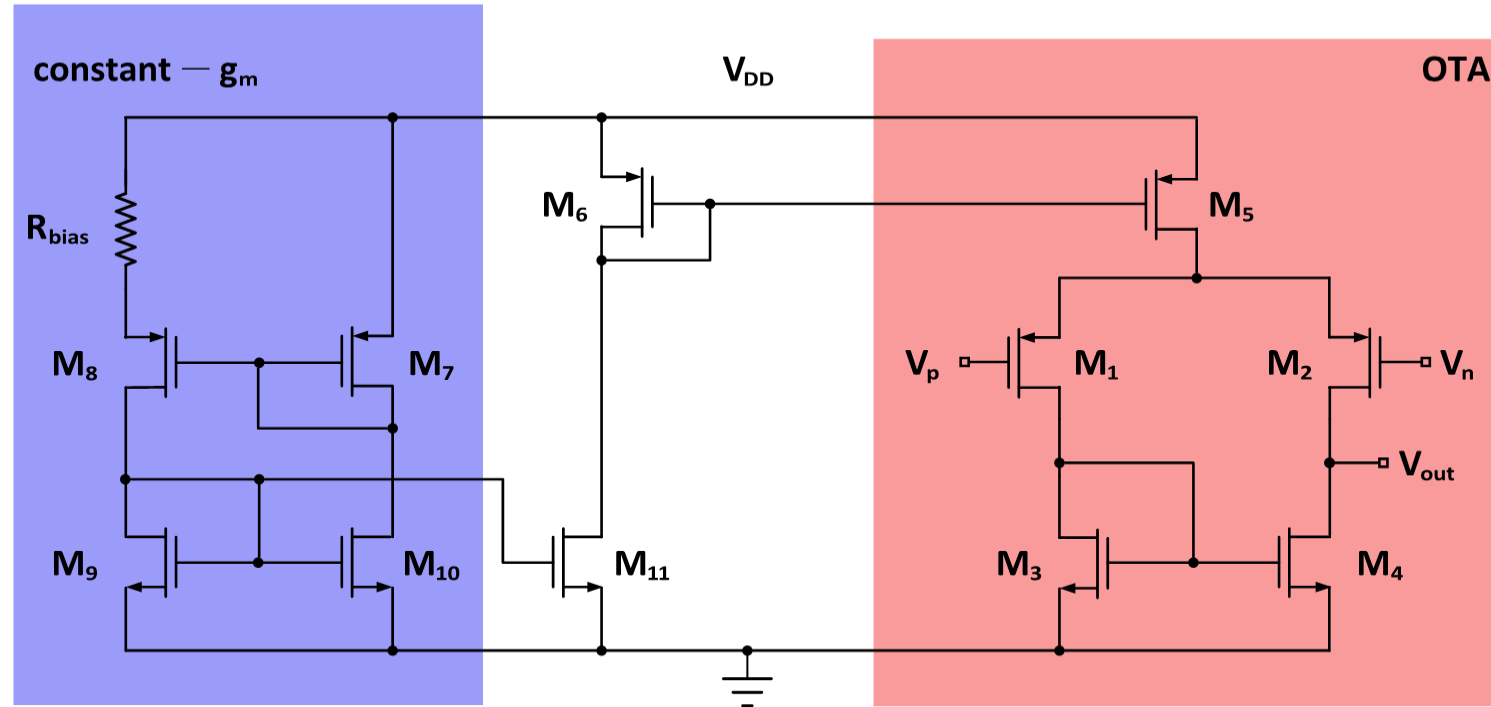


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# Design Example: Diff-pair with Constant- $g_m$ Biasing



- Specifications:
  - $GBW = 20 \text{ MHz}$
  - $C_L = 10 \text{ pF}$

# Design Example: Diff-pair with Constant- $g_m$ Biasing

- Start with  $M_1$  (and  $M_2$ )
  - From  $C_L$  and  $GBW$ :  $g_{m,M_1} = 2\pi f_t(1 + 0.2)C_L \approx 1.5 \text{ mS}$ 
    - The factor 0.2 is to capture some parasitic capacitance
  - Since we don't have a specific power consumption spec here, we pick  $g_m/i_d = 15$  for  $M_1$  since it is a gain stage.
  - Calculate  $i_d$ :  $i_d = \frac{g_{m,M_1}}{g_m/i_d} = \frac{1.5 \text{ mS}}{15} = 100 \text{ }\mu\text{A}$
  - From  $i_d/W$  vs.  $g_m/i_d$  plot (LUT) of PMOS, we determine (there could be some other different candidates)  $W_{M_1} = 80 \text{ }\mu\text{m}$ ,  $L_{M_1} = 280 \text{ nm}$ 
    - If you have any DC gain requirement, you can increase  $L_{M_1}$  by looking at  $g_m/g_{ds}$  vs.  $g_m/i_d$  plot, which will give you a new  $W_{M_1}$ .

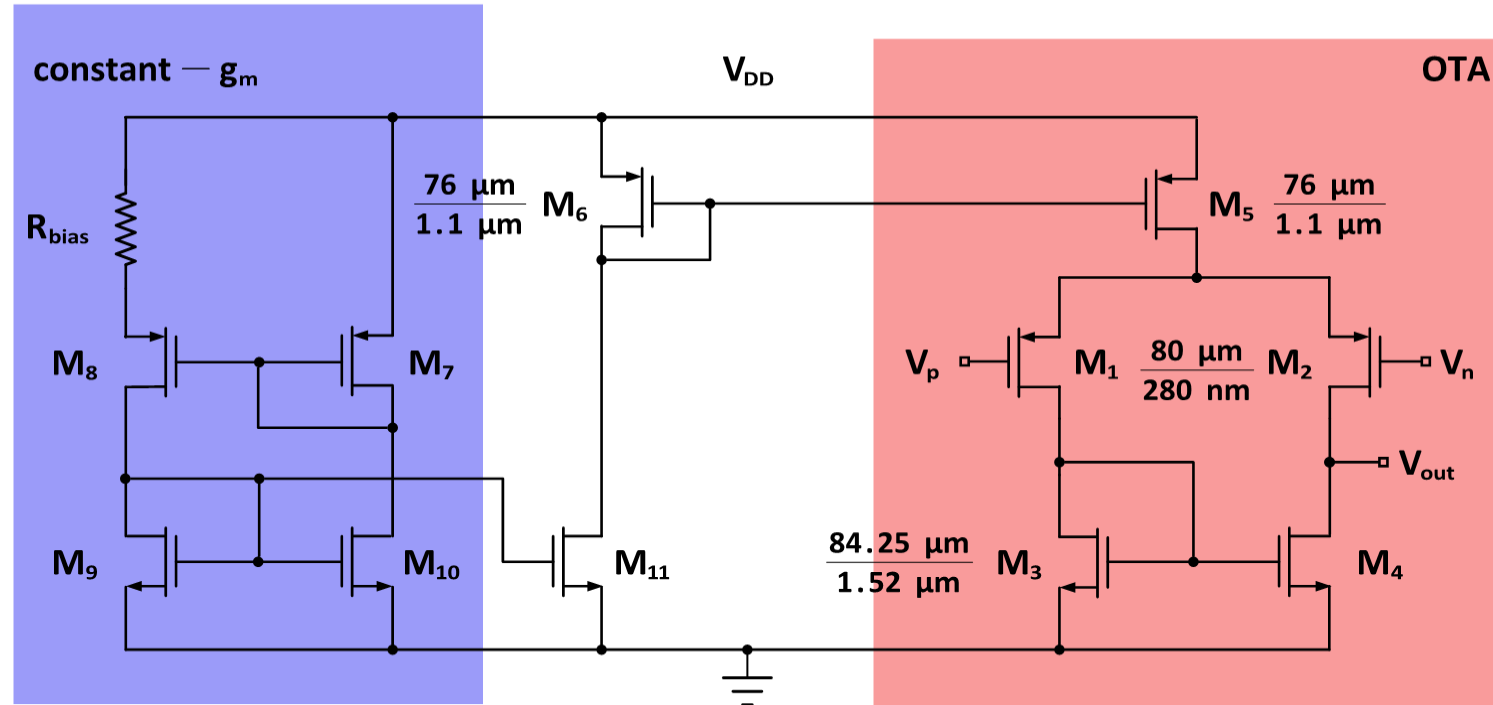
# Design Example: Diff-pair with Constant- $g_m$ Biasing

- Second, we design  $M_3$  (and  $M_4$ )
  - Since we don't have a specific power consumption spec here, we pick  $g_m/i_d = 10$  for  $M_3$  since it is active load (source), so it should be smaller.
  - Since we know  $i_{d,M_3} = i_{d,M_1} = 100 \mu A$  already from the calculation of  $M_1$ , from  $i_d/W$  vs.  $g_m/i_d$  plot (LUT) of NMOS, we determine (there could be some other different candidates)  $W_{M_3} = 84.25 \mu m$ ,  $L_{M_1} = 1.52 \mu m$ 
    - The active load and current source shall have larger output impedance, therefore  $L$  is intentionally picked larger value.

# Design Example: Diff-pair with Constant- $g_m$ Biasing

- Third, we design current mirror  $M_5$  (and  $M_6$ )
  - For simplicity here, we assume  $M_5$  and  $M_6$  have the same dimension (can be scaled down later for reducing power consumption).
  - Since we don't have a specific power consumption spec here, we pick  $g_m/i_d = 4$  for  $M_5$  since it is active load (source), so it should be smaller.
    - The  $g_m/i_d$  is even smaller than  $M_3$ 's since here,  $i_{d,M_5} = 2i_{d,M_3}$ , smaller  $g_m/i_d$  can give larger  $L$  values, which is desirable for current mirror design.
    - Since we don't have a specific power consumption spec here, we pick  $g_m/i_d = 4$  for  $M_5$  since it is active load (source), so it should be smaller.
  - Since we know  $i_{d,M_5} = 2i_{d,M_1} = 200 \mu A$  already from the calculation of  $M_1$ , from  $i_d/W$  vs.  $g_m/i_d$  plot (LUT) of PMOS, we determine (there could be some other different candidates)  $W_{M_5} = 76 \mu m$ ,  $L_{M_5} = 1.1 \mu m$

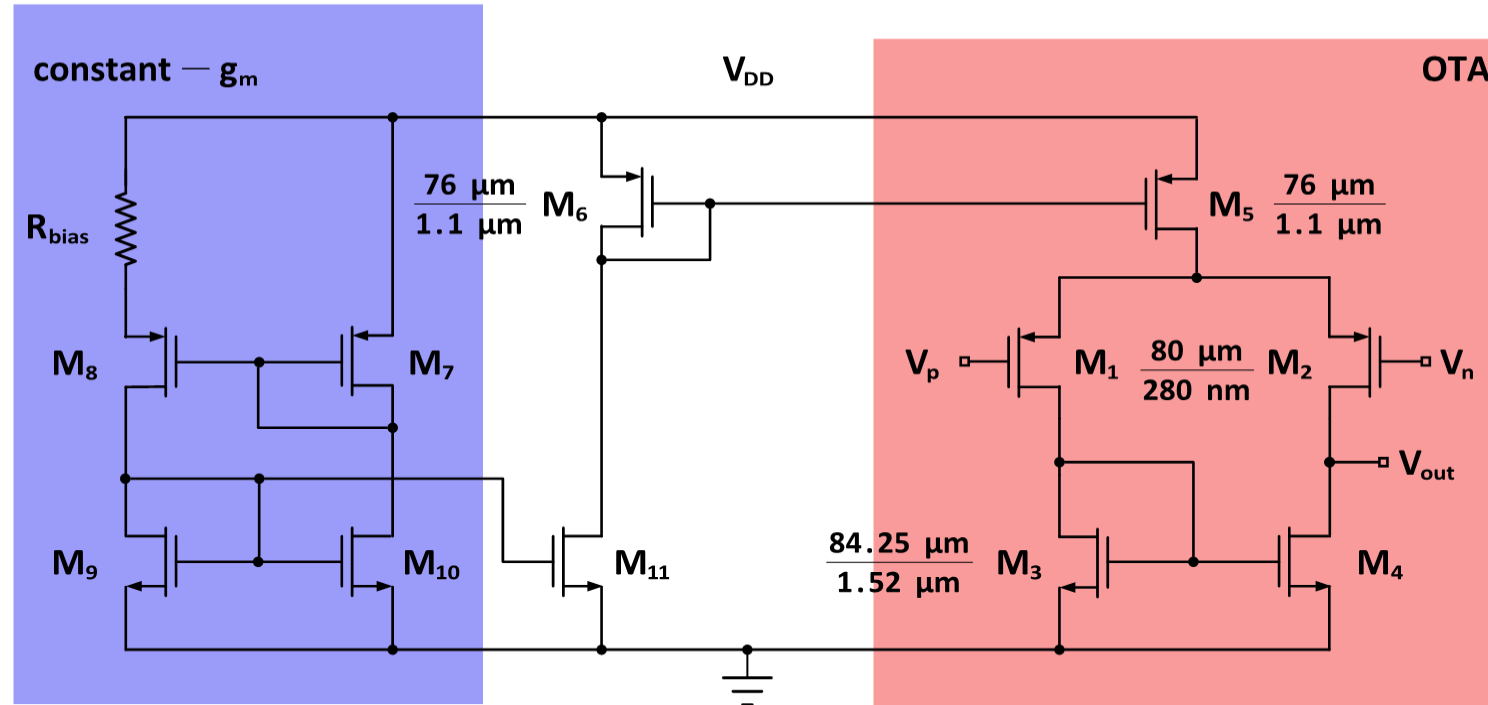
# Design Example: Diff-pair with Constant- $g_m$ Biasing



- Now, we start designing constant- $g_m$  block



# Design Example: Diff-pair with Constant- $g_m$ Biasing



- Ideally,  $g_{m,M_7} = \frac{1}{R_{bias}}$  if  $W_{M_8} = 4W_{M_7}$
- If we let  $M_1$  and  $M_7$  have the same size, and if we can somehow let  $M_1$  and  $M_7$  have the same  $g_m$ , then their  $i_d$  will also be the same.

# Design Example: Diff-pair with Constant- $g_m$ Biasing

- Design  $R_{bias}$ :

- Letting  $g_{M_1} = g_{M_7}$ :  $g_{M_1} = \frac{g_m}{i_d} \times i_{d,M_1} = 1.5 \text{ mS} = g_{M_7}$

- $R_{bias} = \frac{1}{g_{M_7}} = 667 \text{ } \Omega$

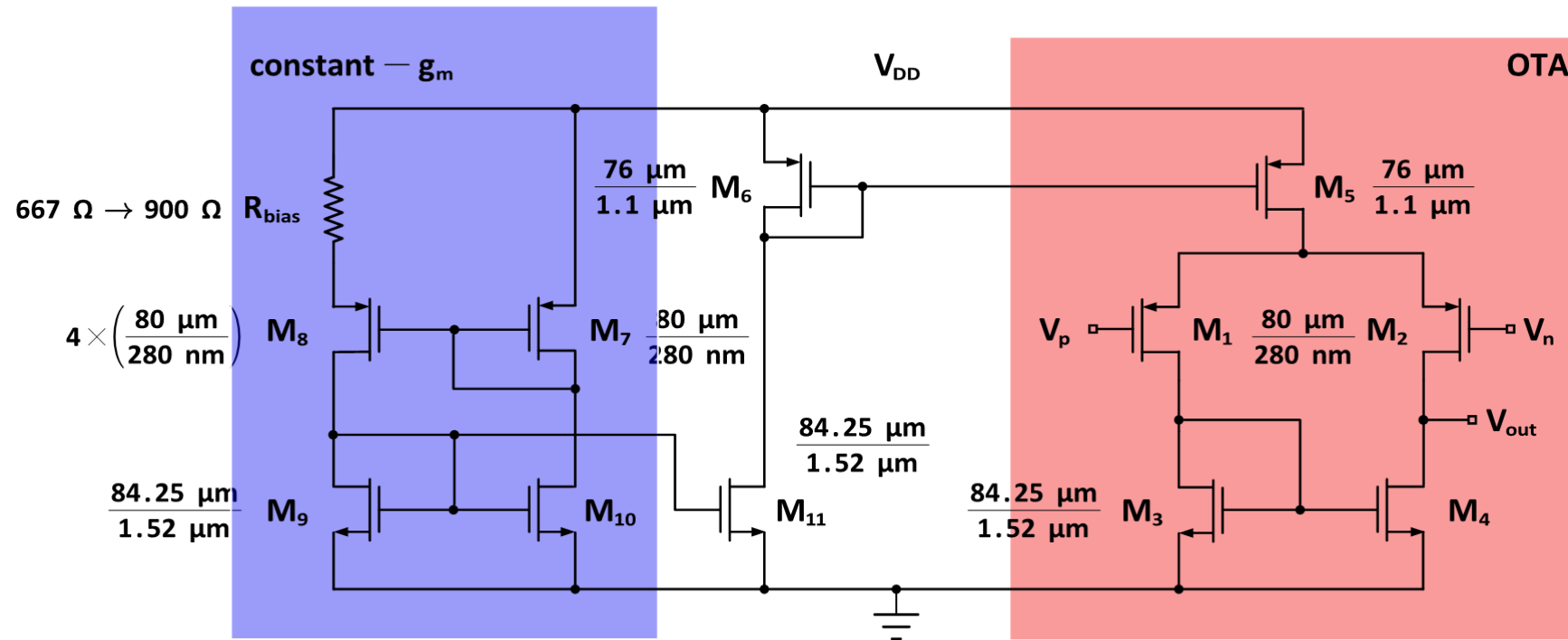
# Design Example: Diff-pair with Constant- $g_m$ Biasing

- Design  $M_7$  (and  $M_8$ ):
  - Simply copying  $M_1$  to  $M_7$ :  $W_{M_1} = W_{M_7} = 80 \mu m$ ;  $L_{M_1} = L_{M_7} = 280 nm$
  - Rather than making  $W_{M_8} = 4W_{M_7}$ , we can let  $W_{M_8} = W_{M_7}$  and use multiplier:  $M_{M_8} = 4M_{M_7}$

# Design Example: Diff-pair with Constant- $g_m$ Biasing

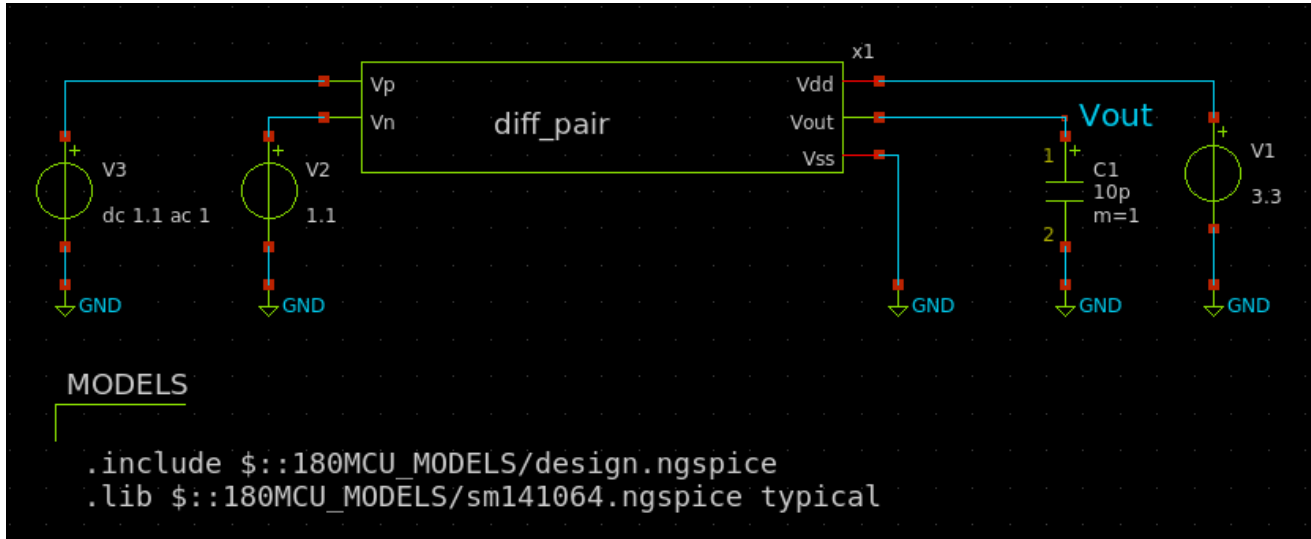
- Design  $M_9$  ( $M_{10}$  and  $M_{11}$ ):
  - Simply copying  $M_3$  to  $M_9$ ,  $M_{10}$  and  $M_{11}$
  - If necessary, you can increase  $L$  of  $M_9$ ,  $M_{10}$  and  $M_{11}$  to increase the output resistance of current mirror
    - Ensure you are always operating them in saturation region!

# Design Example: Diff-pair with Constant- $g_m$ Biasing

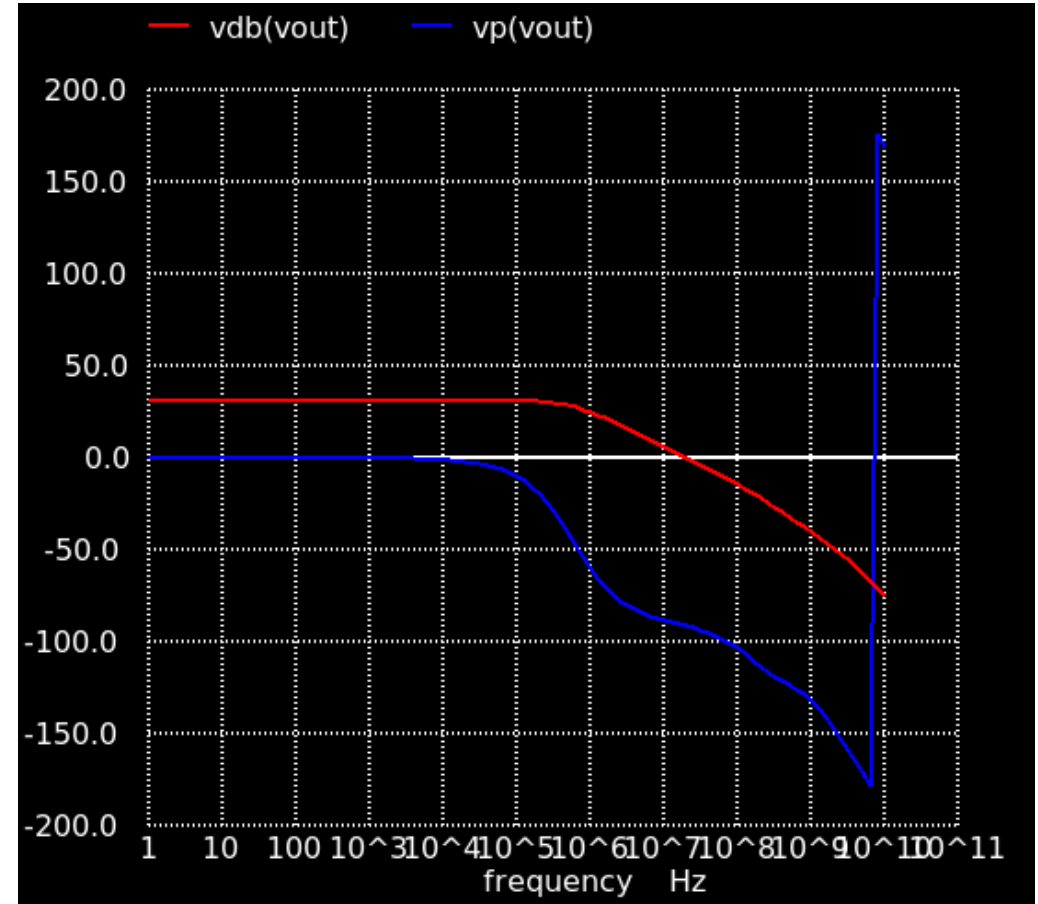


- Small fine tune is needed on  $R_{bias}$  (from  $667 \Omega$  to  $900 \Omega$ ) to achieve more accurate results

# Results



params	gm/id method	SPICE simulation
Id_M1 (uA)	100.53	102.69
Id_M3 (uA)	100.53	102.69
Id_M5 (uA)	201.06	205.38
gm/id_M1 (1/V)	15.00	12.86
gm/id_M3 (1/V)	10.00	10.66
gm/id_M5 (1/V)	4.00	4.23
gain (dB)	34.62	35.69
GBW (MHz)	20.00	19.95

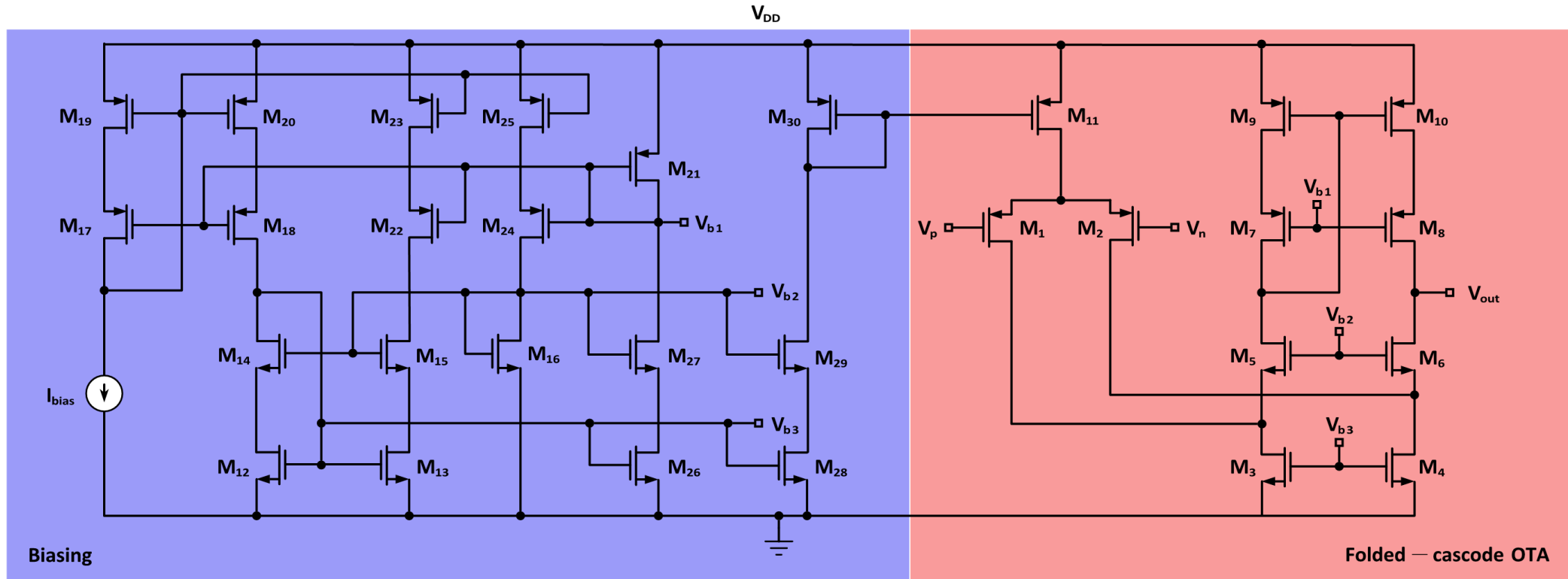


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# Folded-cascode OTA with high-swing current mirror biasing



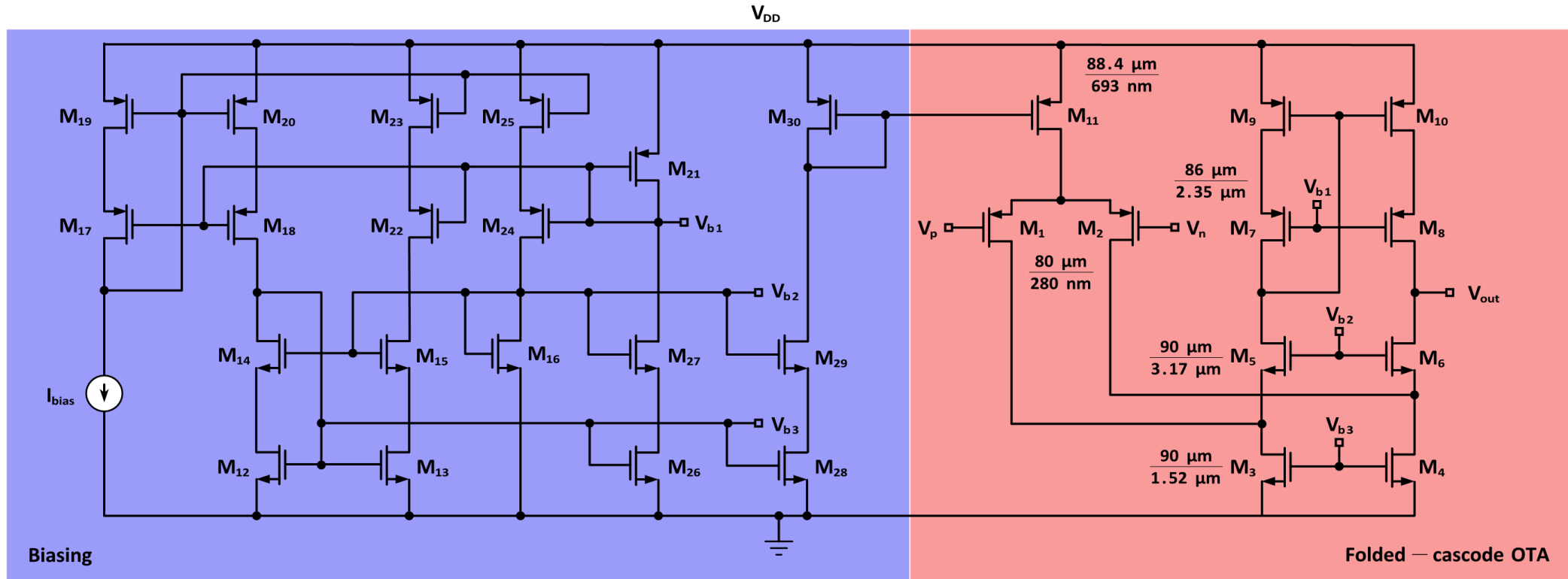
- Specifications:
  - $GBW = 20 \text{ MHz}$
  - $C_L = 10 \text{ pF}$
- Could be more challenging due to the voltage headroom and more biasing points.



# Folded-cascode OTA with high-swing current mirror biasing

- First, start from the folded-cascode OTA design
- Like the design of diff-pair OTA,  $g_m/i_d$  method is applied here, so the detailed calculations are omitted here (see previous example).
  - $g_{m,M_1} = 2\pi f_t(1 + 0.2)C_L = 1.5 \text{ mS}$
  - For  $M_1 - M_2$ , pick  $\frac{g_m}{i_d} = 15$ ,  $i_{d,M_1} = \frac{g_{m,M_1}}{\frac{g_m}{i_d}} = 100 \text{ }\mu\text{A}$ :  $W_{M_1} = 80 \text{ }\mu\text{m}$ ,  $L_{M_1} = 280 \text{ nm}$ . Again, if you have gain requirement, you can consider increase  $L_{M_1}$ .
  - For  $M_7 - M_{10}$ , pick  $\frac{g_m}{i_d} = 4$ , by assuming  $i_{d,M_7} = i_{d,M_1} = 100 \text{ }\mu\text{A}$ :  $W_{M_1} = 86 \text{ }\mu\text{m}$ ,  $L_{M_1} = 2.35 \text{ }\mu\text{m}$ .
  - For  $M_3 - M_4$ , pick  $\frac{g_m}{i_d} = 8$ , noted that  $i_{d,M_3} = i_{d,M_1} + i_{d,M_7} = 200 \text{ }\mu\text{A}$ :  $W_{M_3} = 90 \text{ }\mu\text{m}$ ,  $L_{M_3} = 1.52 \text{ }\mu\text{m}$ .
  - For  $M_5 - M_6$ , pick  $\frac{g_m}{i_d} = 8$ , noted that  $i_{d,M_5} = i_{d,M_7} = 100 \text{ }\mu\text{A}$ :  $W_{M_5} = 90 \text{ }\mu\text{m}$ ,  $L_{M_3} = 3.17 \text{ }\mu\text{m}$ .
  - For  $M_{11}$ , pick  $\frac{g_m}{i_d} = 4$ , noted that  $i_{d,M_{11}} = 2i_{d,M_1} = 200 \text{ }\mu\text{A}$ :  $W_{M_5} = 88.4 \text{ }\mu\text{m}$ ,  $L_{M_3} = 693 \text{ nm}$ .

# Folded-cascode OTA with high-swing current mirror biasing

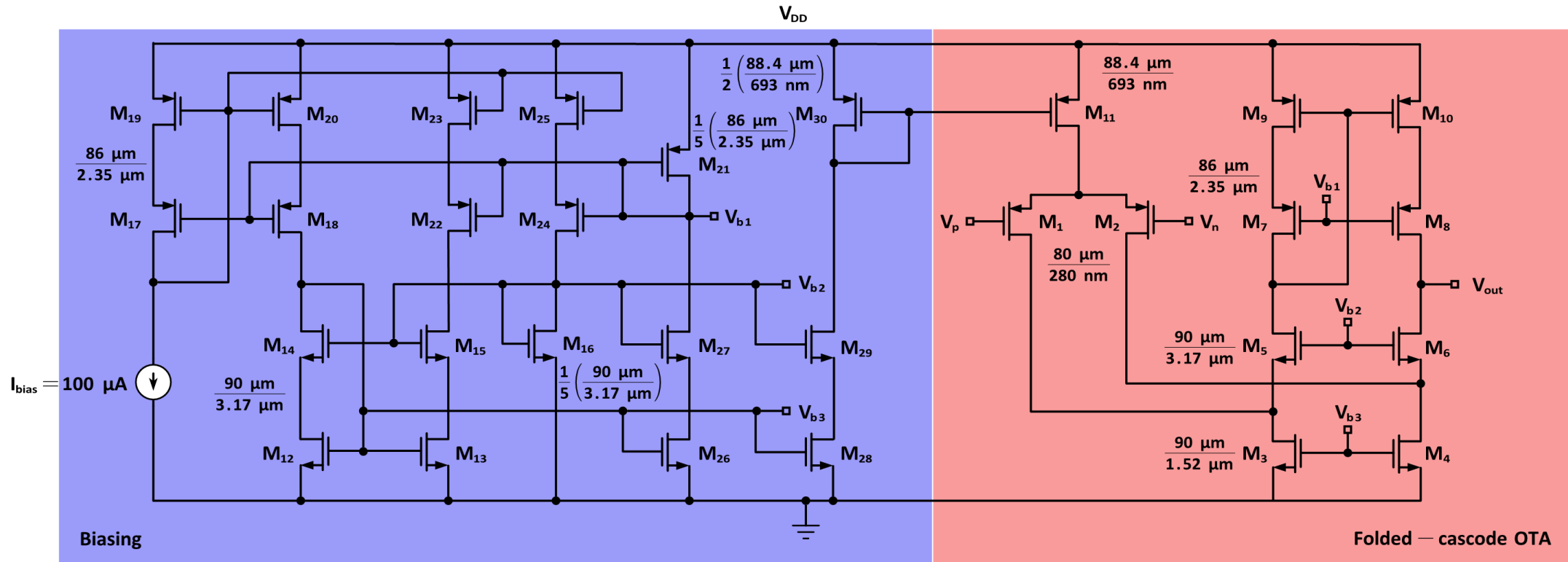


- We next start with designing high-swing current mirror.
  - PMOS high-swing current mirror:  $M_{17} - M_{21}$
  - NMOS high-swing current mirror:  $M_{12} - M_{16}$

# Folded-cascode OTA with high-swing current mirror biasing

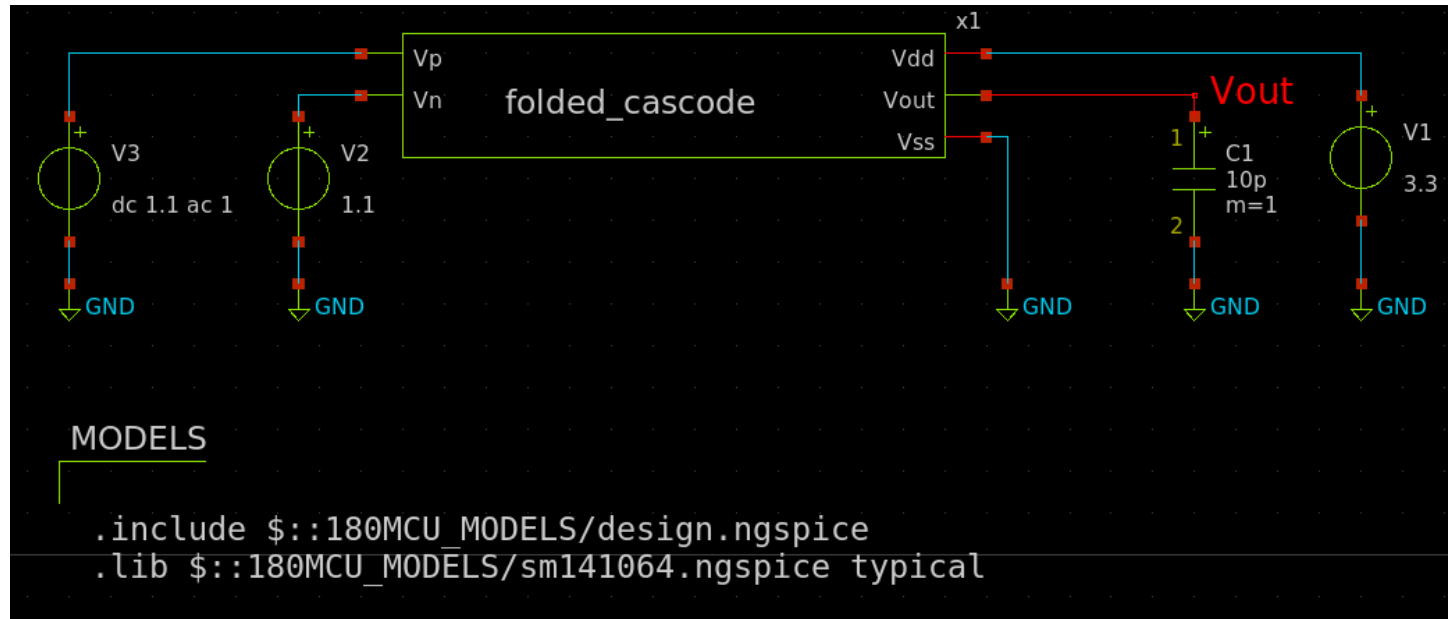
- Similar concept is applied here: passing the same current will ensure the same transconductance, so the biasing point ( $g_m/i_d$ ) will be the same.
- For PMOS high swing current mirror ( $M_{17} - M_{21}$ ),  $M_{17} - M_{20}$  have the same size as  $M_7$ ,  $M_{21}$  has its length  $L_{M_{21}} = 4L_{M_7}$  (or 5 times).
  - $I_{bias} = i_{d,M_7} = 100 \mu A$
- For NMOS high swing current mirror ( $M_{12} - M_{16}$ ),  $M_{12} - M_{15}$  have the same size as  $M_5$ ,  $M_{16}$  has its length  $L_{M_{16}} = 4L_{M_5}$  (or 5 times).
- For  $M_{22} - M_{25}$ , their size can be the same as  $M_7$ .
- For  $M_{26} - M_{29}$ , their size can be the same as  $M_5$ .
- For  $M_{29}$ ,  $W_{M_{29}} = W_{M_{11}}$ ,  $L_{M_{29}} = 2L_{M_{11}}$ .
  - As the current flows through  $M_{11}$  is twice of the current through  $M_3$  here.

# Folded-cascode OTA with high-swing current mirror biasing



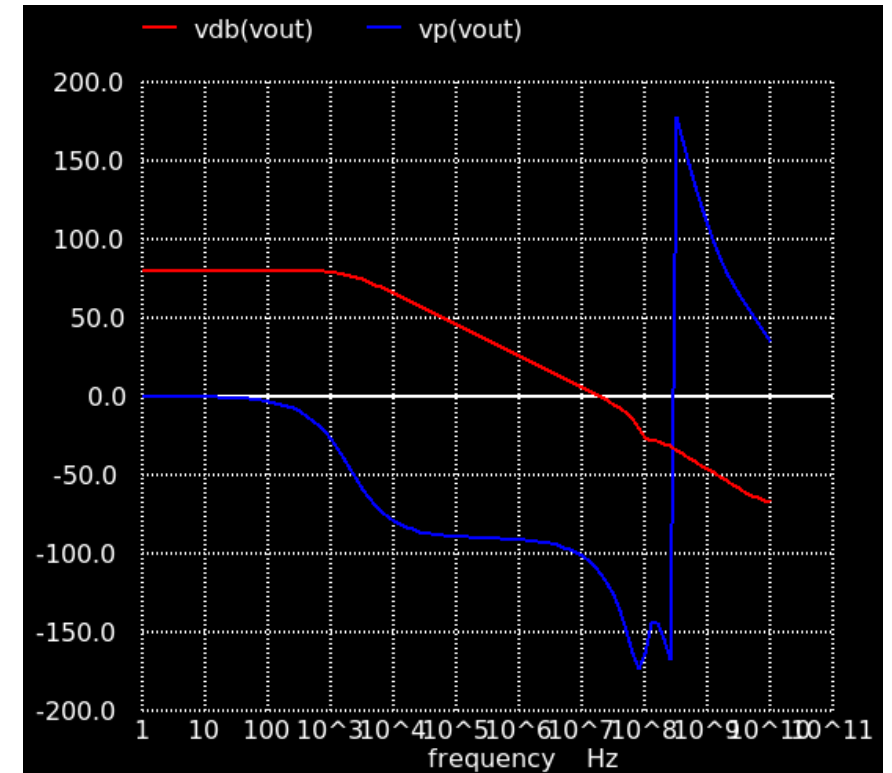
- $V_{b1} = 1.465 \text{ V}, V_{b2} = 1.17 \text{ V}, V_{b3} = 0.876 \text{ V}$
- If you want to replace  $I_{bias}$ , you can use constant- $g_m$  method introduced previously (or a BGR).
- Similarly, you can scale down the dimensions of current mirror to reduce their power consumption.

# Results



\*\*\* SPICE simulations finished! \*\*\*

params	gm/id method	SPICE simulation
Id_M1 (uA)	100.53	109.12
Id_M3 (uA)	201.06	198.36
Id_M5 (uA)	100.53	89.24
Id_M7 (uA)	100.53	89.25
Id_M11 (uA)	201.06	218.23
gm/id_M1 (1/V)	15.00	12.71
gm/id_M3 (1/V)	8.00	8.05
gm/id_M5 (1/V)	8.00	8.44
gm/id_M7 (1/V)	4.00	4.54
gm/id_M11 (1/V)	4.00	5.91
gain (dB)	108.61	80.24
GBW (MHz)	20.00	19.95

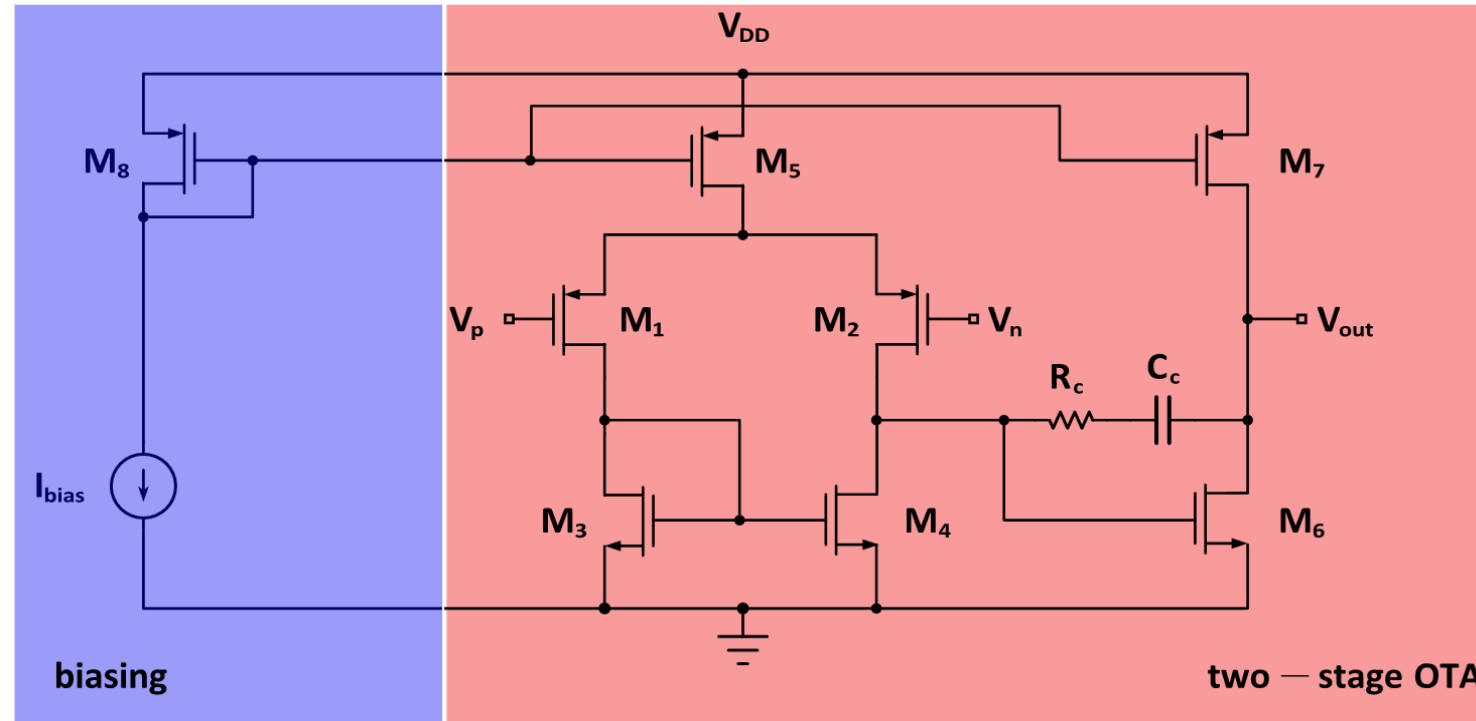


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# Two-stage OTA with Miller lead compensation



- Specifications:
  - $GBW = 20\text{ MHz}$
  - $C_L = 10\text{ pF}$

# Two-stage OTA with Miller lead compensation

- A few equations are needed here to guide the design here:

- $f_t = \frac{g_m}{2\pi C_c}$

- $C_c \geq 0.22 C_L$  to guarantee at least around 60° PM

- $R_c \approx \frac{1}{1.7 f_t C_c}$  to give you around extra 30° PM

- For removing input-offset voltage:  $\frac{\left(\frac{W}{L}\right)_{M_6}}{\left(\frac{W}{L}\right)_{M_4}} = 2 \frac{\left(\frac{W}{L}\right)_{M_7}}{\left(\frac{W}{L}\right)_{M_5}}$

- In case if you have SR requirement:  $SR = \frac{I_{M_5}}{C_c}$



# Two-stage OTA with Miller lead compensation

- Start with  $M_1 - M_2$ :
  - For extra margin, we take  $C_c = 0.3C_L = 3 \text{ pF}$ . This also gives  $R_c = 9.8 \text{ k}\Omega$ .
  - For extra margin,  $g_{m,M_1} = 2\pi f_t(1 + 0.5)C_c = 0.565 \text{ mS}$
  - Pick its  $\frac{g_m}{i_d} = 15$ , a relatively large value:  $i_{d,M_1} = \frac{g_{m,M_1}}{\frac{g_m}{i_d}} = 37.7 \text{ }\mu\text{A}$
  - Pick  $W_{M_1} = 30 \text{ }\mu\text{m}$ ,  $L_{M_1} = 280 \text{ nm}$ . For two stage OTA, input stage does not need high gain, which is what the second stage is for.

# Two-stage OTA with Miller lead compensation

- Second, design active load  $M_3 - M_4$ 
  - Very similar to the design of active load in the diff-pair OTA example, detailed analysis is omitted here.
  - Pick  $\frac{g_m}{i_d} = 10$ ,  $W_{M_3} = 31.6 \mu m$ ,  $L_{M_3} = 1.52 \mu m$
- Third, design current source  $M_5$ 
  - Very similar to the design of current source in the diff-pair OTA example, detailed analysis is omitted here. Just remember  $i_{d,M_5} = 2i_{d,M_1}$ .
  - Pick  $\frac{g_m}{i_d} = 4$ ,  $W_{M_5} = 28.4 \mu m$ ,  $L_{M_5} = 1.1 \mu m$

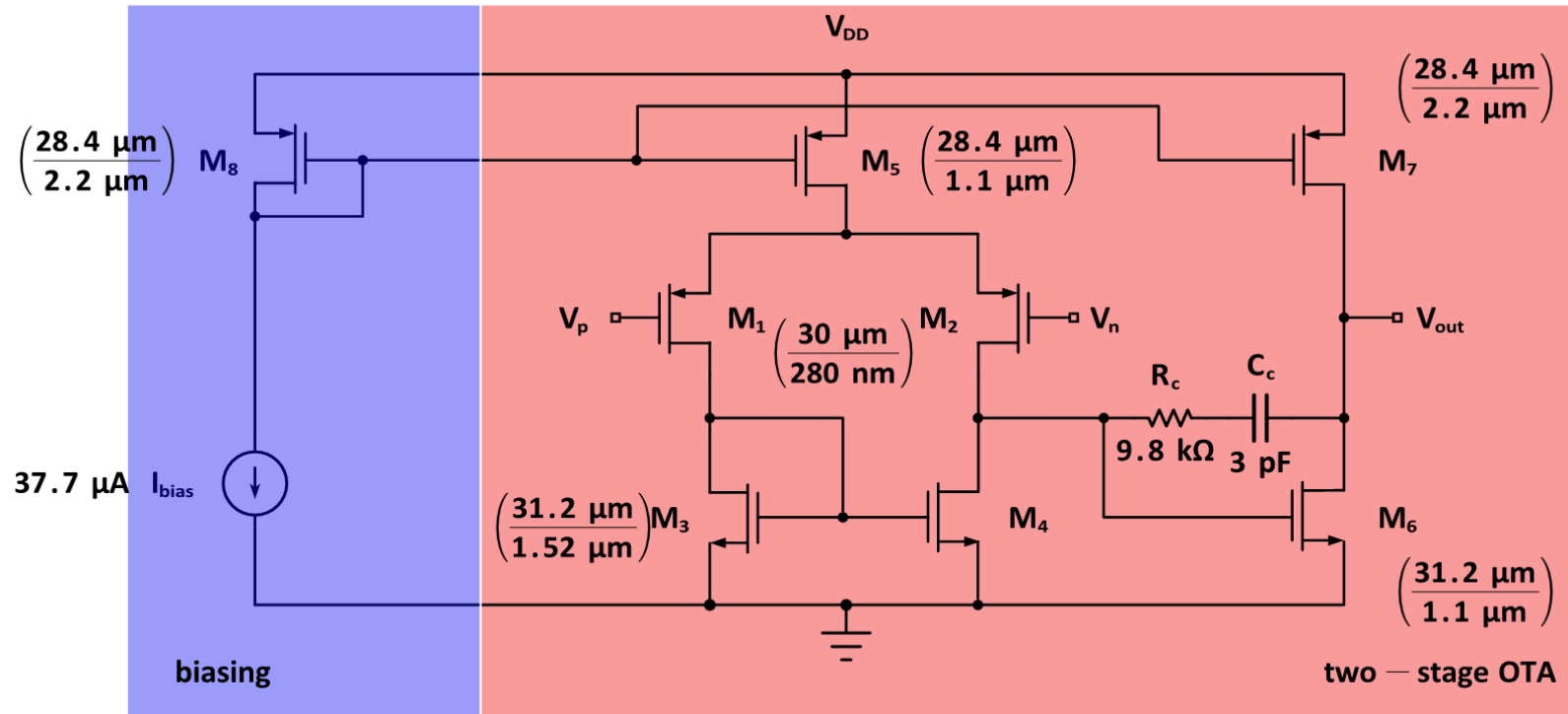
# Two-stage OTA with Miller lead compensation

- We now design the second stage. We first start with designing the current source  $M_7$ , as it makes the later current mirror design simpler.
  - We do not have an explicit power budget here, so we assume  $i_{d,M_7} = \frac{1}{2} i_{d,M_5} = 37.7 \mu A$ .
  - We do not apply normal  $g_m/i_d$  method here, since we do not want to violate the input-offset voltage rule. Therefore, we simply do the following sizing for  $M_7$ :  $W_{M_7} = W_{M_5} = 28.4 \mu m$ ,  $L_{M_7} = 2L_{M_5} = 2.2 \mu m$ .
  - We can reversely check its  $g_m/i_d$  now (from  $\frac{i_d}{W}$  vs.  $\frac{g_m}{i_d}$  plot), which is 6.1, and this is a relatively small number.

# Two-stage OTA with Miller lead compensation

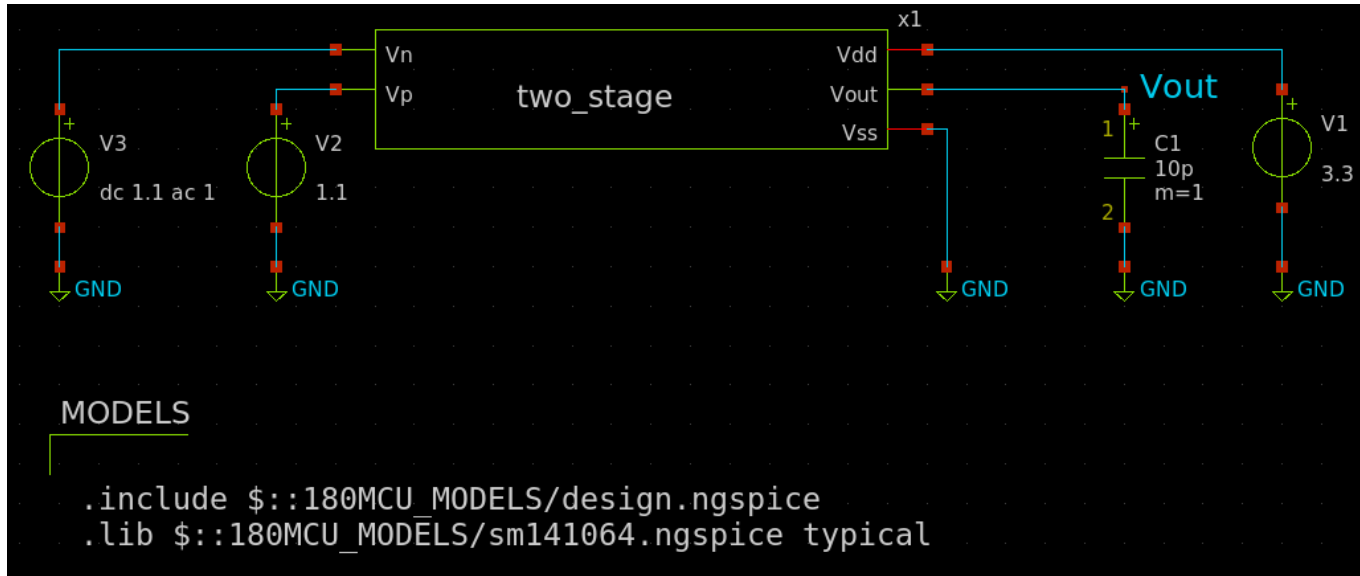
- We then design the gain transistor  $M_6$  of the second stage:
  - Through input-offset sizing relationship:  $\left(\frac{W}{L}\right)_{M_6} = 2 \frac{\left(\frac{W}{L}\right)_{M_7}}{\left(\frac{W}{L}\right)_{M_5}} \times \left(\frac{W}{L}\right)_{M_4} = 20.79$
  - We pick  $L_{M_6} = 1.1 \mu m$  for some high gain, which leads to  $W_{M_6} = 23 \mu m$ .
  - We can reversely check its  $g_m/i_d$  now (from  $\frac{i_d}{W}$  vs.  $\frac{g_m}{i_d}$  plot), which is 11, and this is a relatively large number.
- Current mirror transistor  $M_8$  can be the same as  $M_7$  for now.
  - $I_{bias} = 37.7 \mu A$

# Two-stage OTA with Miller lead compensation



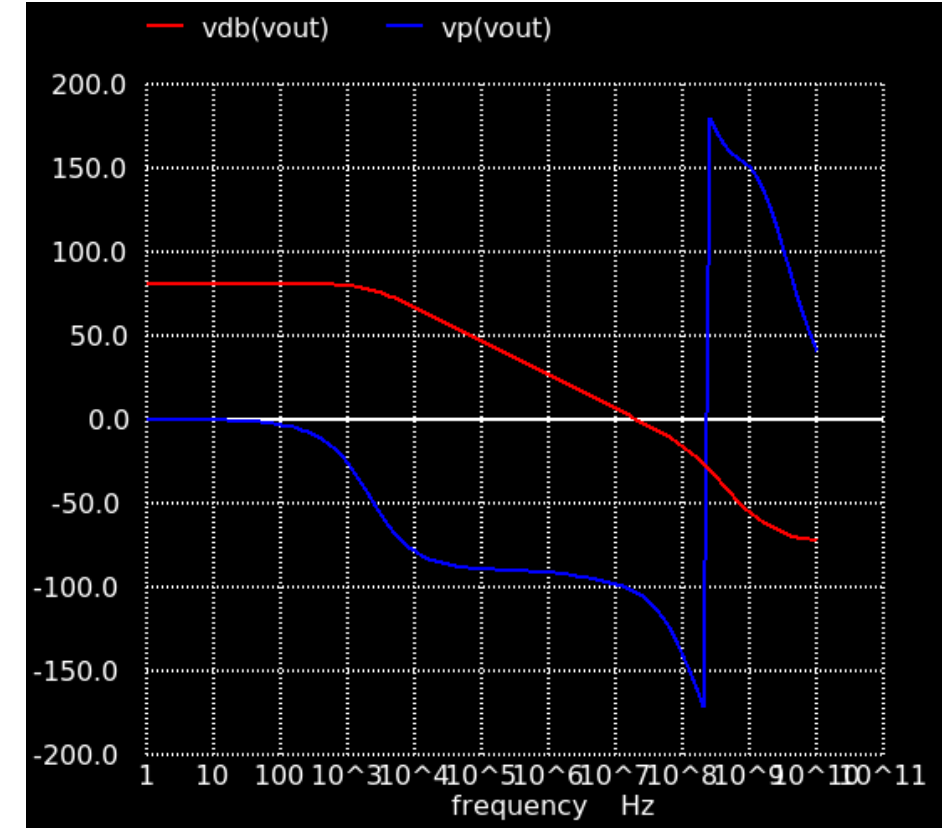
- If you want to replace  $I_{bias}$ , you can use constant- $g_m$  method introduced previously (or a BGR).
- Similarly, you can scale down the dimensions of current mirror to reduce their power consumption.

# Results



\*\*\* SPICE simulations finished! \*\*\*

params	gm/id method	SPICE simulation
Id_M1 (uA)	37.69911184307752	39.95
Id_M3 (uA)	37.69911184307752	39.95
Id_M5 (uA)	75.39822368615503	79.90
Id_M6 (uA)	37.69911184307752	37.96
Id_M7 (uA)	37.69911184307752	37.96
gm/id_M1 (1/V)	15	12.70
gm/id_M3 (1/V)	10	10.51
gm/id_M5 (1/V)	4	4.15
gm/id_M6 (1/V)	10.996805517419196	10.88
gm/id_M7 (1/V)	6.094891296677578	4.12
gain (dB)	83.29207884089496	80.99
GBW (MHz)	20.0	19.95
PM (degree)	-	77.38



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- Creating LUT for  $g_m/i_d$
- $g_m/i_d$  design flow
- Design Example in GF180MCU
  - Diff-pair OTA with constant- $g_m$  biasing
  - Folded-cascode OTA with high-swing current mirror biasing
  - Two-stage OTA with Miller lead compensation
- Conclusion

# Conclusion

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- A brief introduction of  $g_m/i_d$  method is presented.
- Three common OTA circuits are designed using  $g_m/i_d$  method in open-source GF180MCU CMOS process.
- Simulation results are very close to the first-order calculations using  $g_m/i_d$  method.



# References

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- Analog Integrated Circuit Design, 2<sup>nd</sup> Edition
- Paul Allen's lecture notes on two-stage op-amp:  
[https://pallen.ece.gatech.edu/Academic/ECE\\_6412/Spring\\_2004/L130-OpAmpCompII\(2UP\).pdf](https://pallen.ece.gatech.edu/Academic/ECE_6412/Spring_2004/L130-OpAmpCompII(2UP).pdf)
- Eric Yeh's YouTube video on  $g_m/i_d$  method:  
<https://www.youtube.com/@ericyeh3787>
- Dr. Hesham Omran's YouTube video on  $g_m/i_d$  method:  
<https://www.youtube.com/watch?v=dzz4z3ijVts>