REV	Description 4		BY
D	1. Improved layout for the USB PHY. 2. Removed unused parts from the design. 3. Added current measurement function to the TWL4030. 4. Added filter caps to the VBUS rail input and output. 5. Changed U9 & U11 package to the QFN	8/14/08	GC
C1	Added J12 and J13 to provide access to the RGB TTL signals on the LCD. Added 5 filter caps. Moved the USB Host port from Port1 to Port2. Deleted R1. Added 10K pulldown to USB reset signal. Added 10K pulldown resistors as ID function to determine board type by reading these pins. Added series resistor, R53, in the CLK line of the HSUSB clock line. May be removed after testing.	10/1/08	GC
C2	Moved the McBSP3_DX signal to pin AB26. Moved the McBSP3_DR signal to pin AB25. Moved the McBSP3_CLKX signal to pin AD25. Changes were to allow access to three PWM signals from OMAP3530.	1/1/09	GC
C _{C2A}	Changed R70 and R72 from 12K to 1.2K to lower the impedance due to noise issues. Changed R71 and R73 from 12K to 1.2K to lower the impedance due to noise issues.	3/11/09	GC

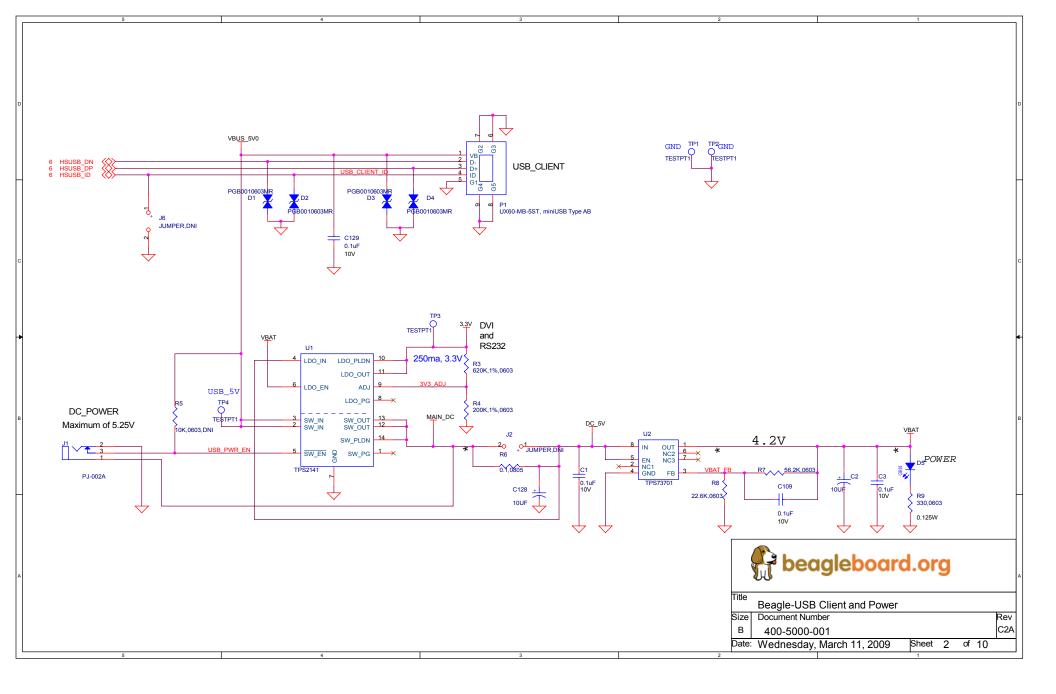
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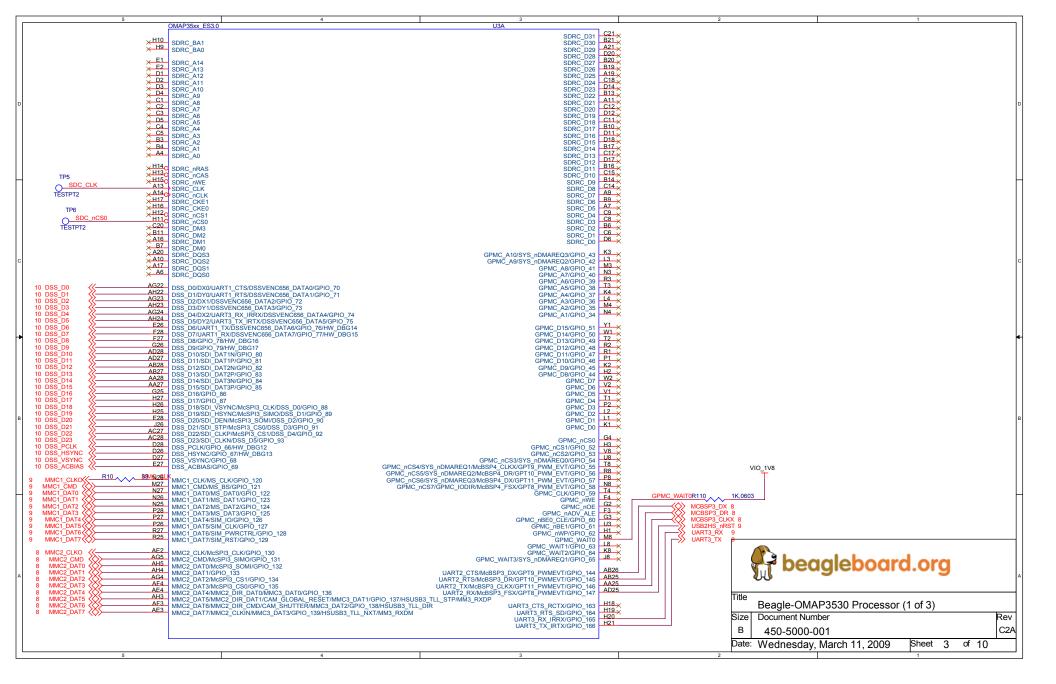
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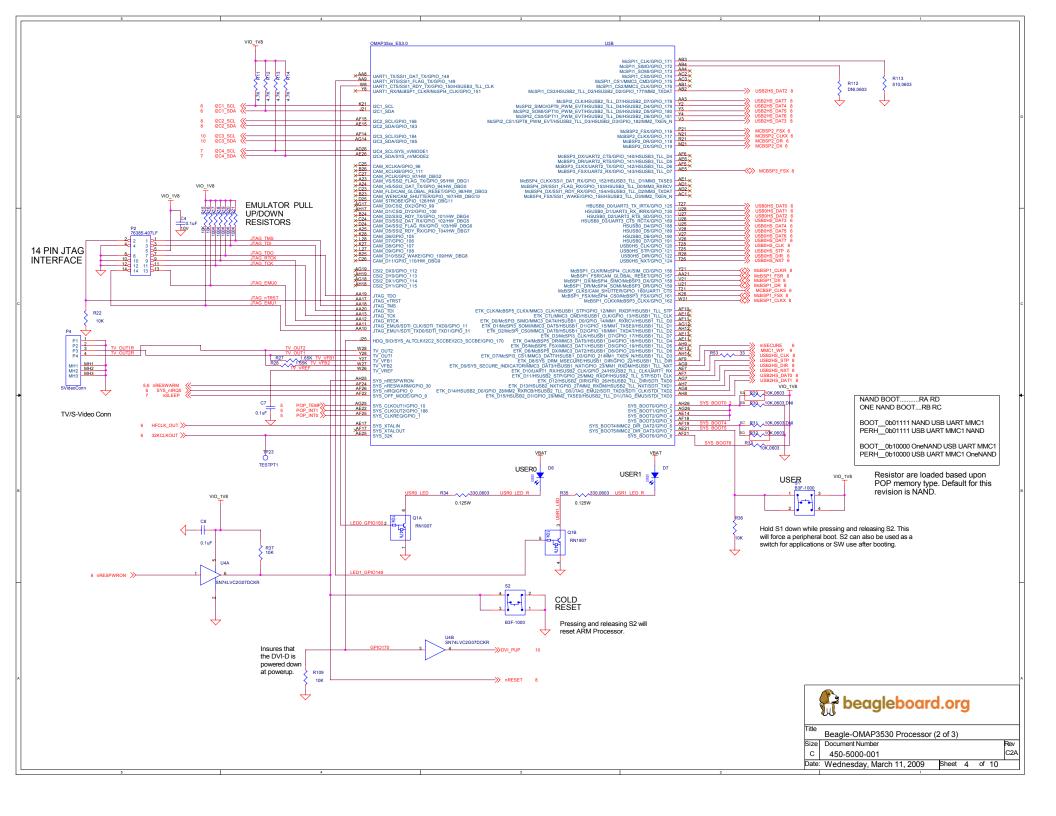
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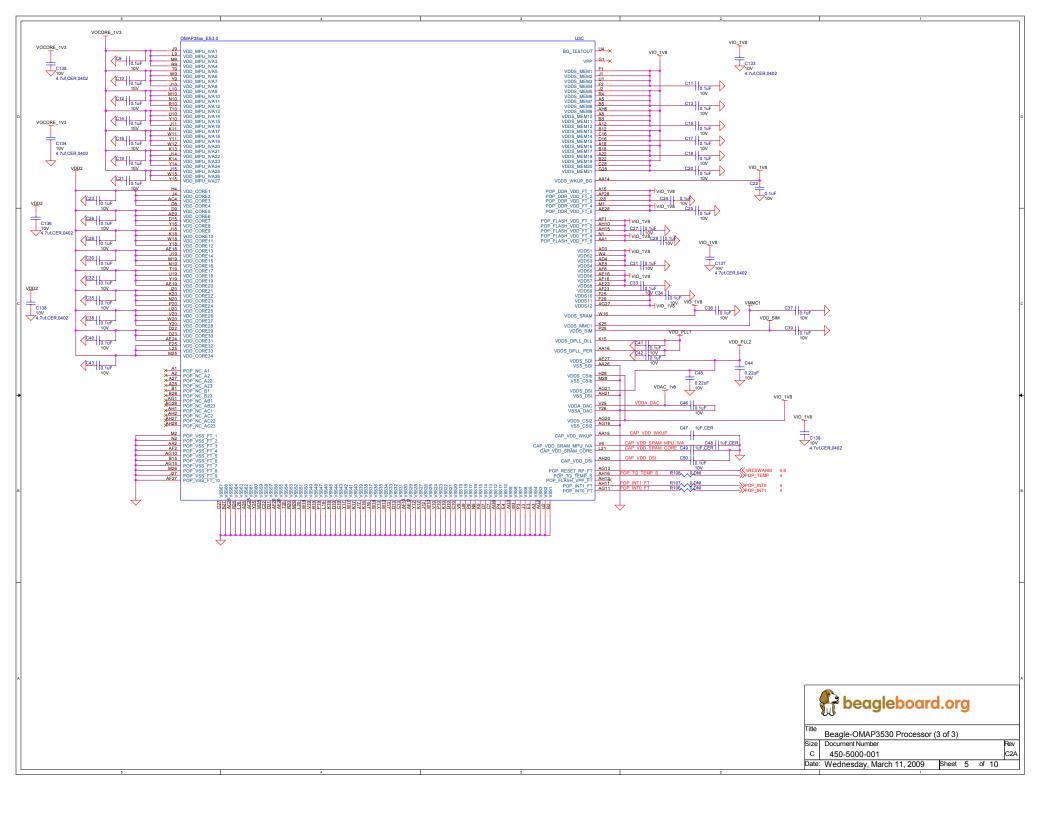


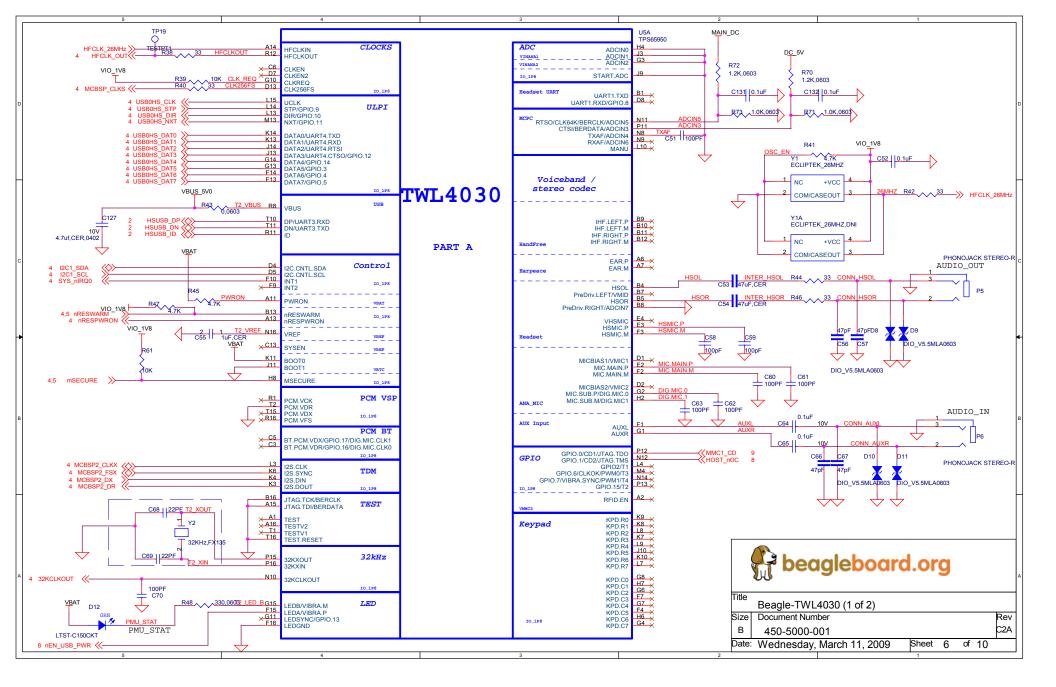
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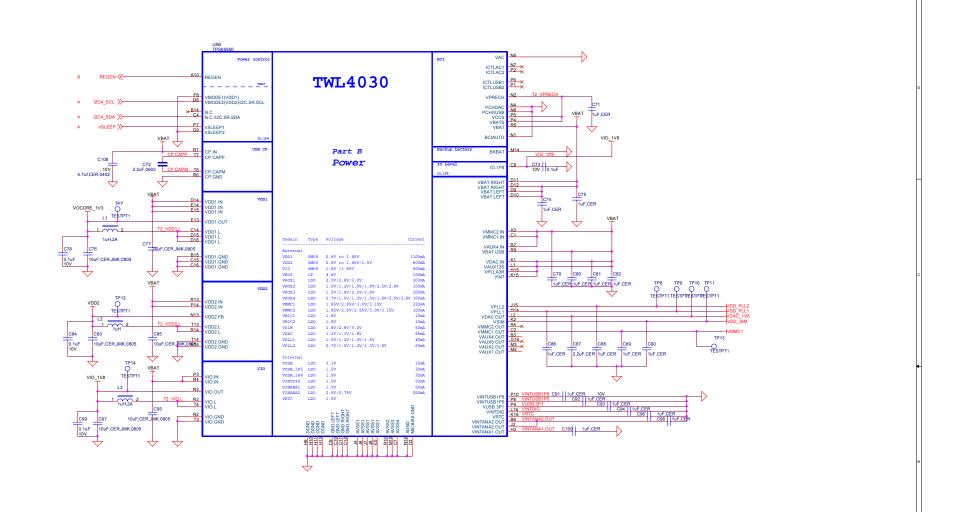














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