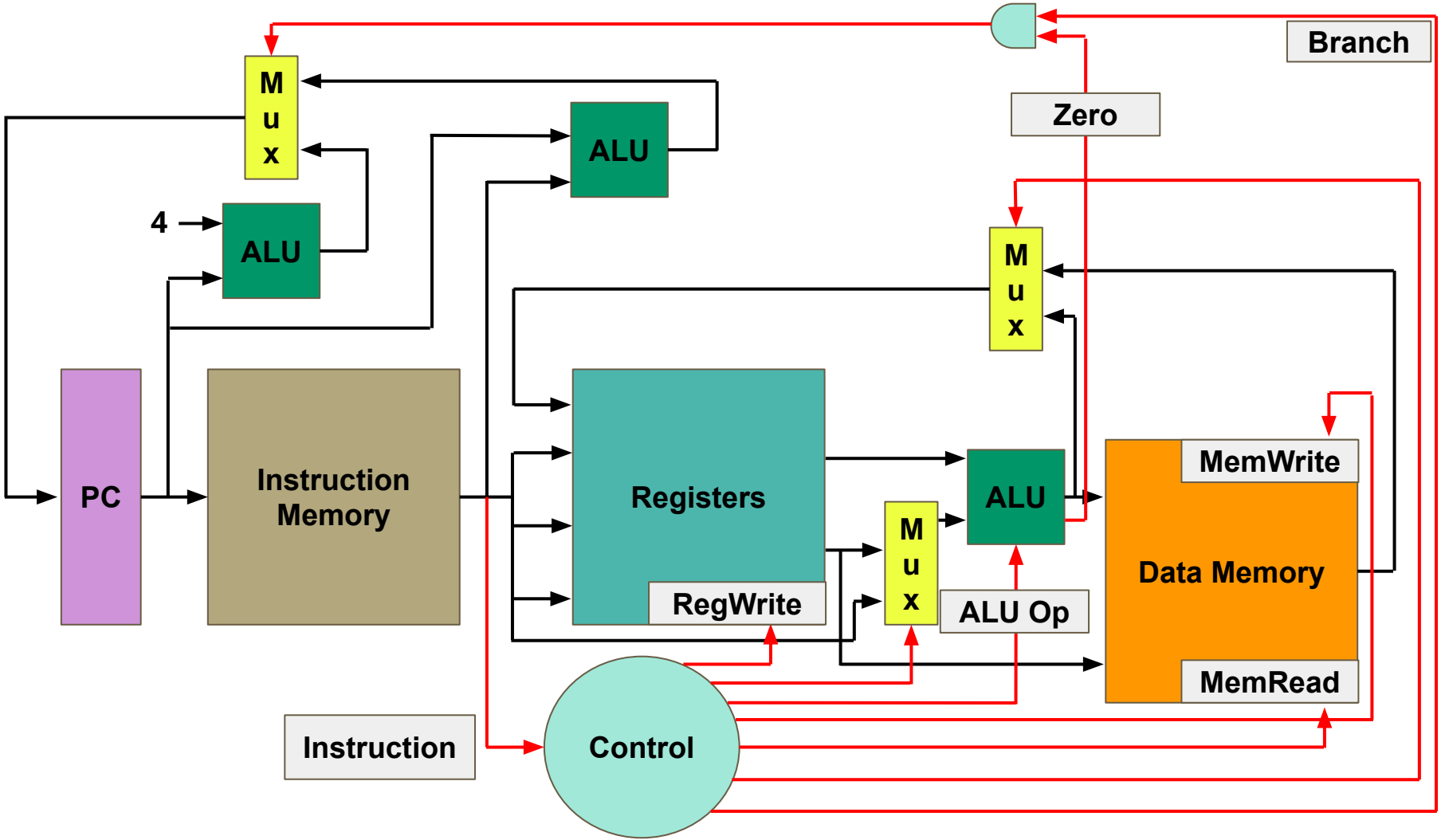
Bits of Architecture

Tracing RISC-V Instructions

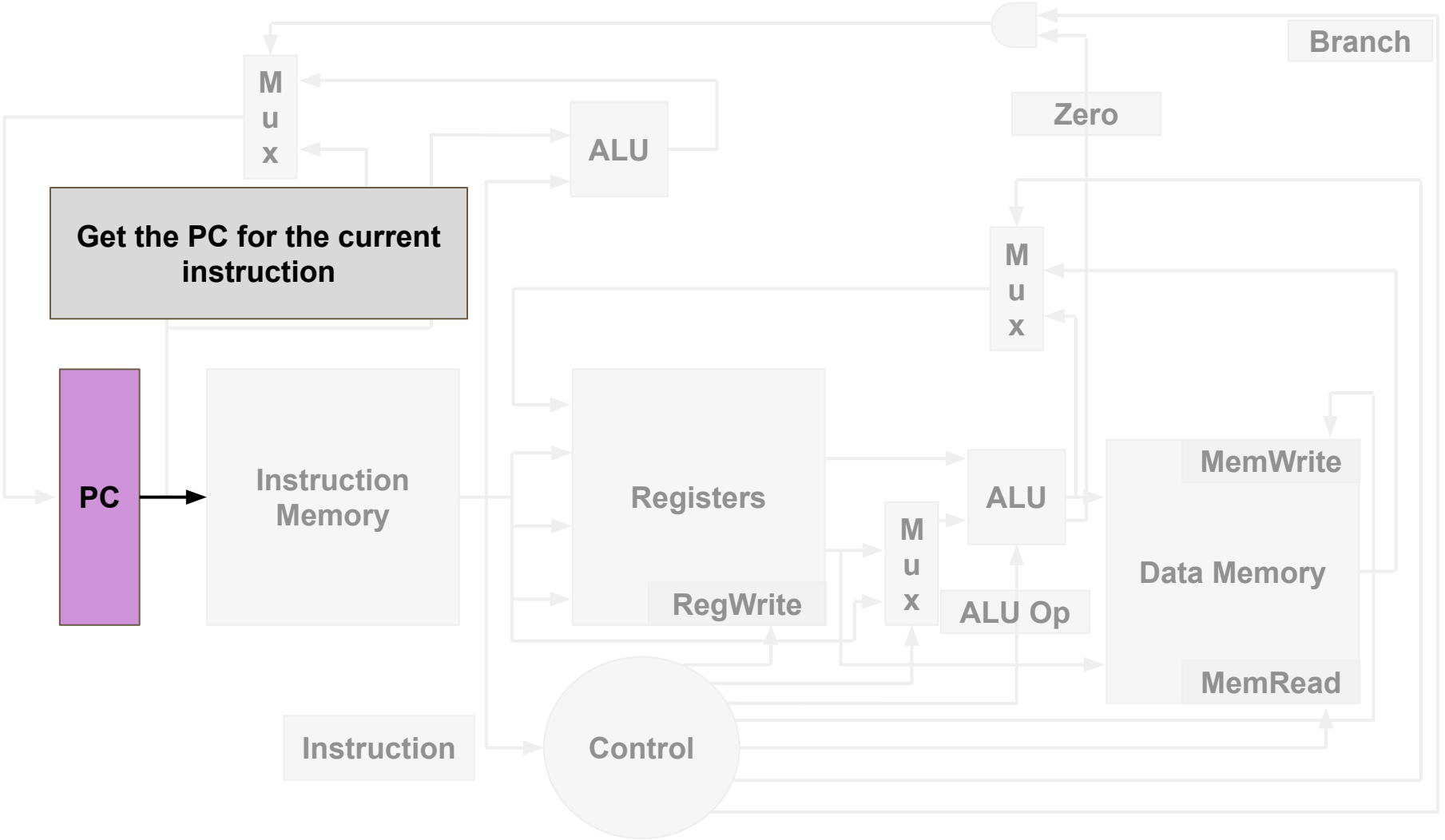
Our Processor

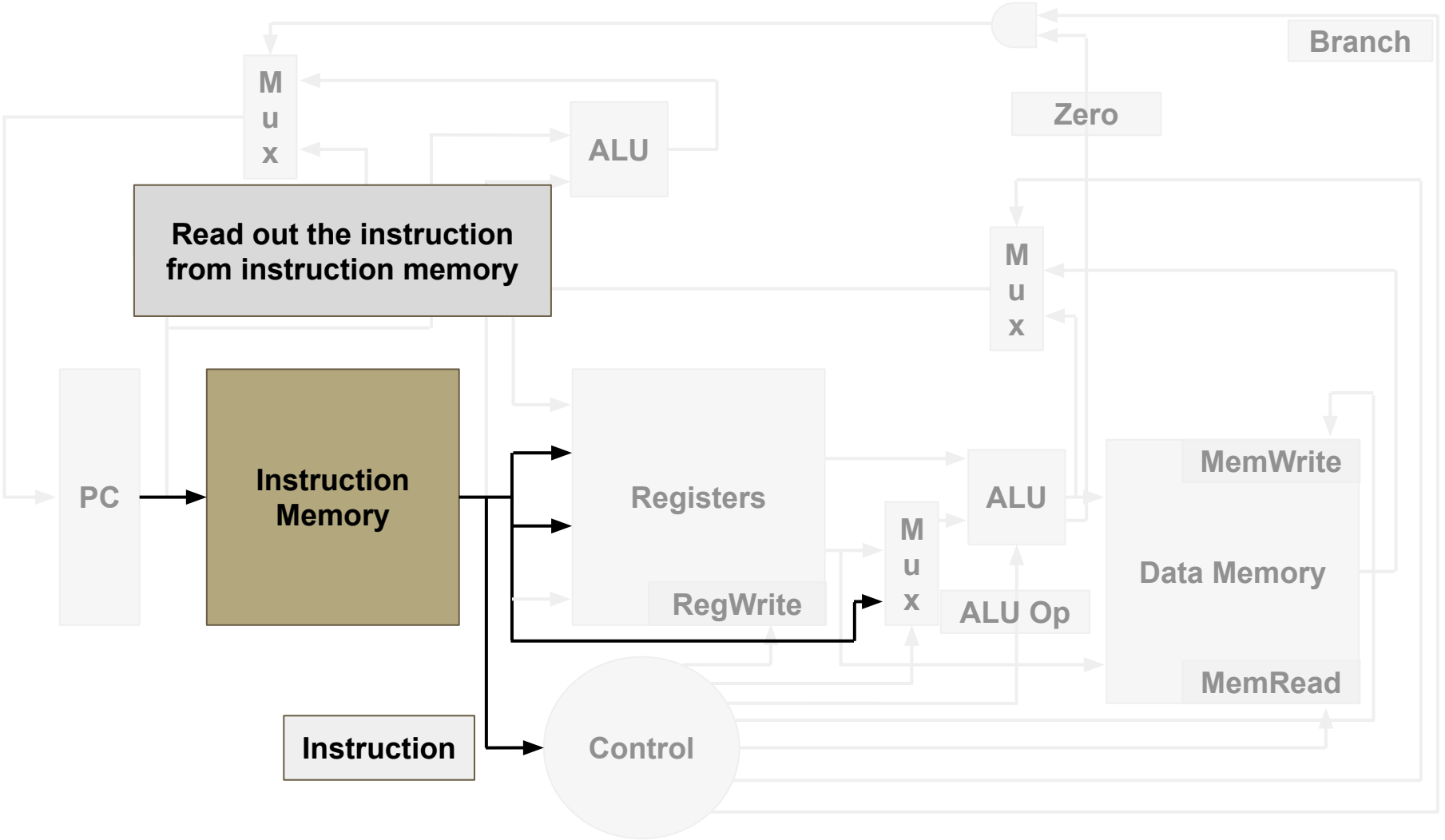

Branch
M
u
x
Zero
ALU
4
ALU
M
u
x
PC
Instruction
Memory
Registers
RegWrite
M
u
x
ALU
MemWrite
Data Memory
MemRead
ALU Op
Instruction
Control

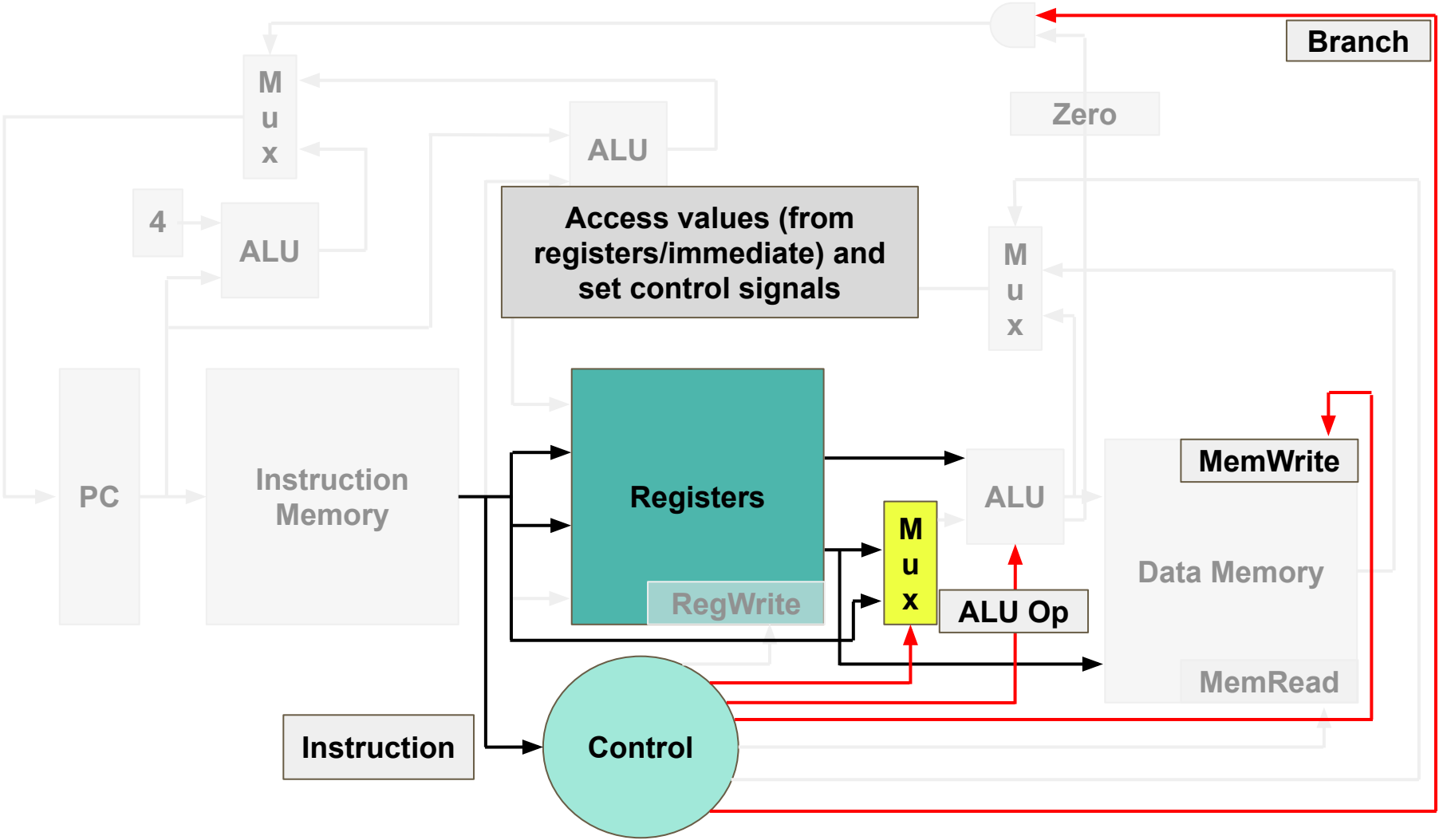
Which Instructions Do We Support?

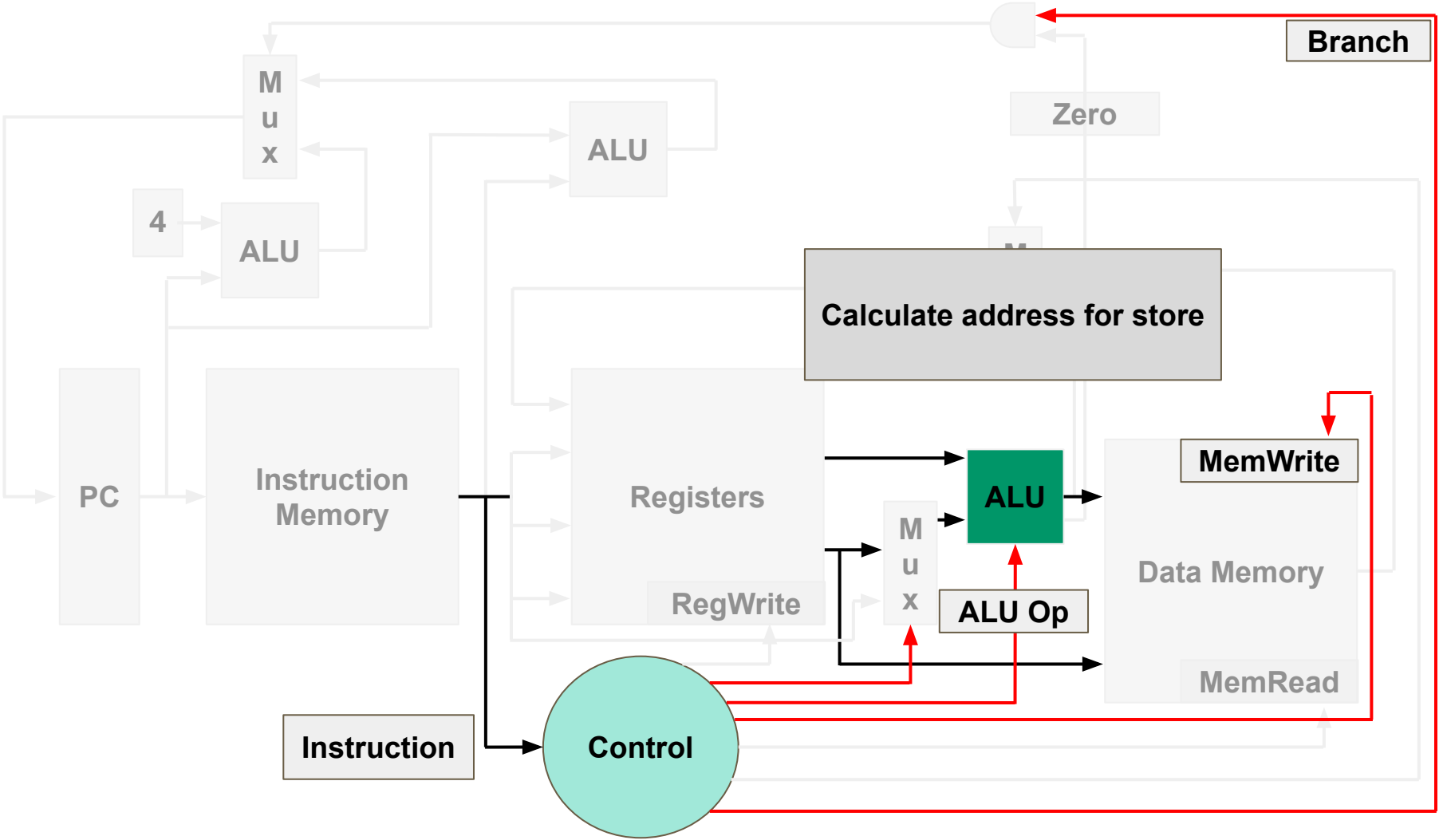
- Memory Instructions
  - Store Word (**sw**)
  - Load Word (**lw**)
- Some arithmetic/logical operations
  - **add**, **sub**, **and**, and **or**
- Conditional Branch
  - **beq**

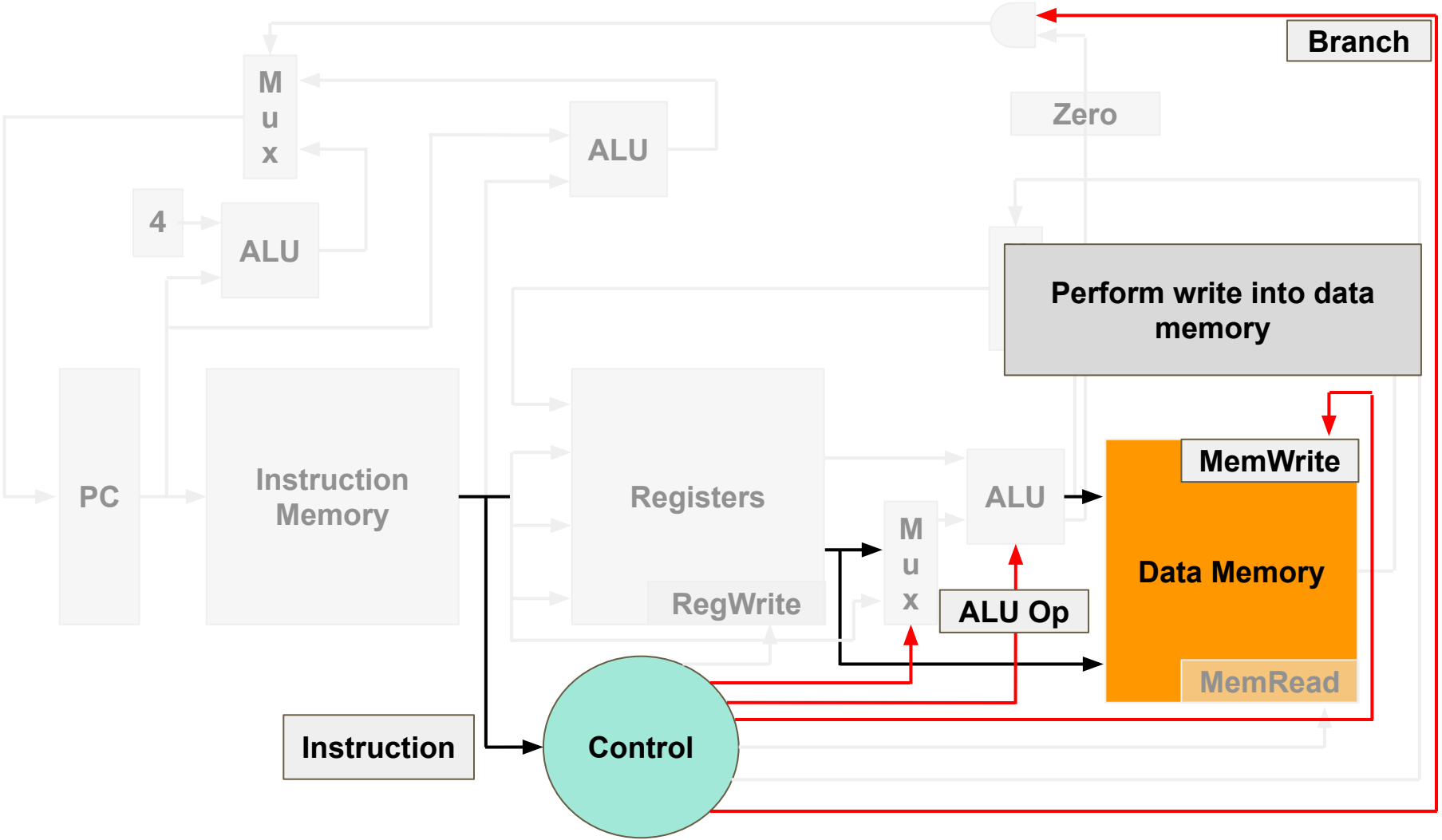
Store Word (sw)

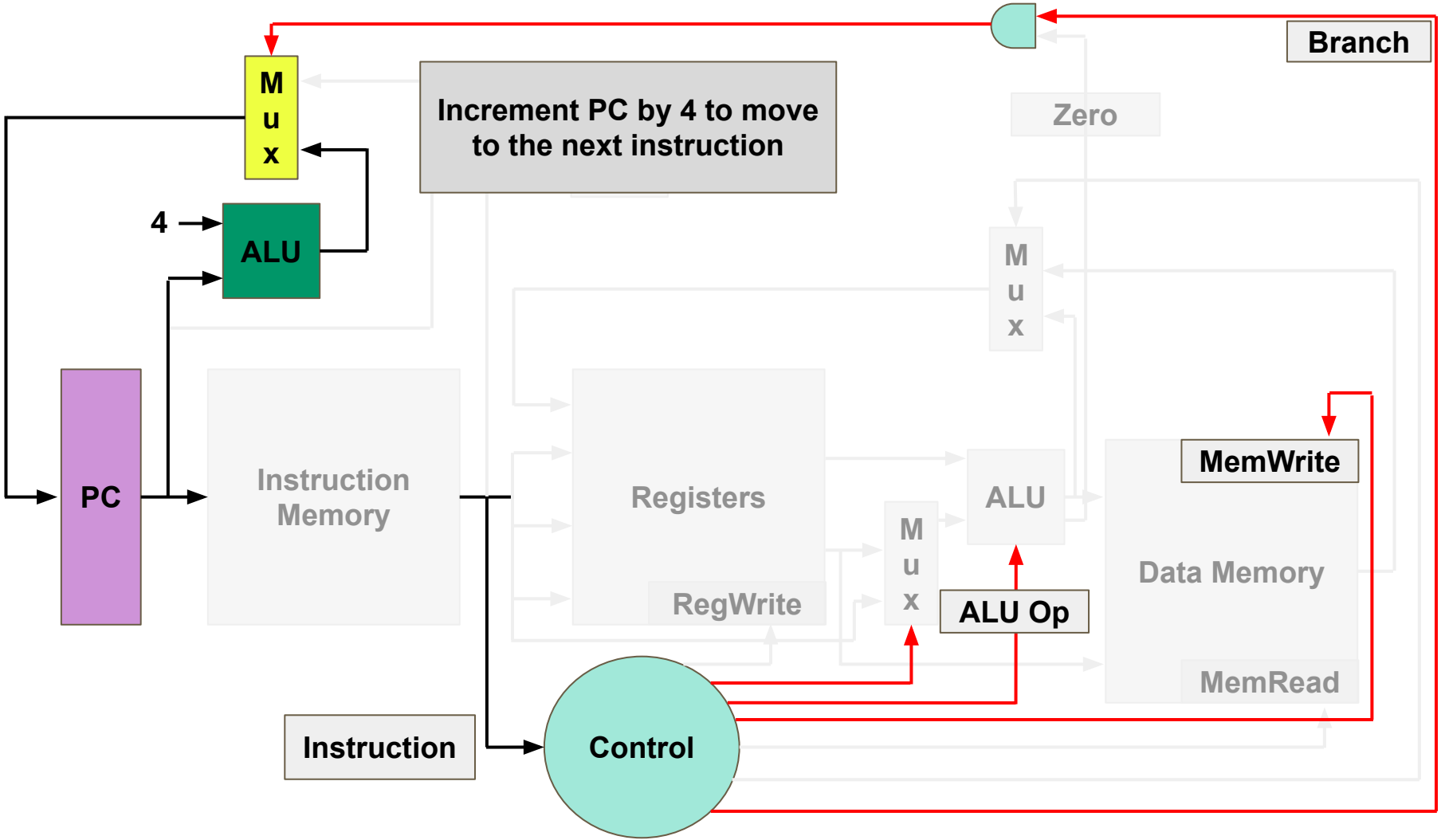

Branch
M
u
x
Zero
ALU
Get the PC for the current instruction
M
u
x
PC
Instruction Memory
Registers
RegWrite
M
u
x
ALU
ALU Op
MemWrite
Data Memory
MemRead
Instruction
Control


Branch
M
u
x
Zero
ALU
Read out the instruction
from instruction memory
M
u
x
PC
Instruction
Memory
Registers
RegWrite
M
u
x
ALU
ALU Op
MemWrite
Data Memory
MemRead
Instruction
Control

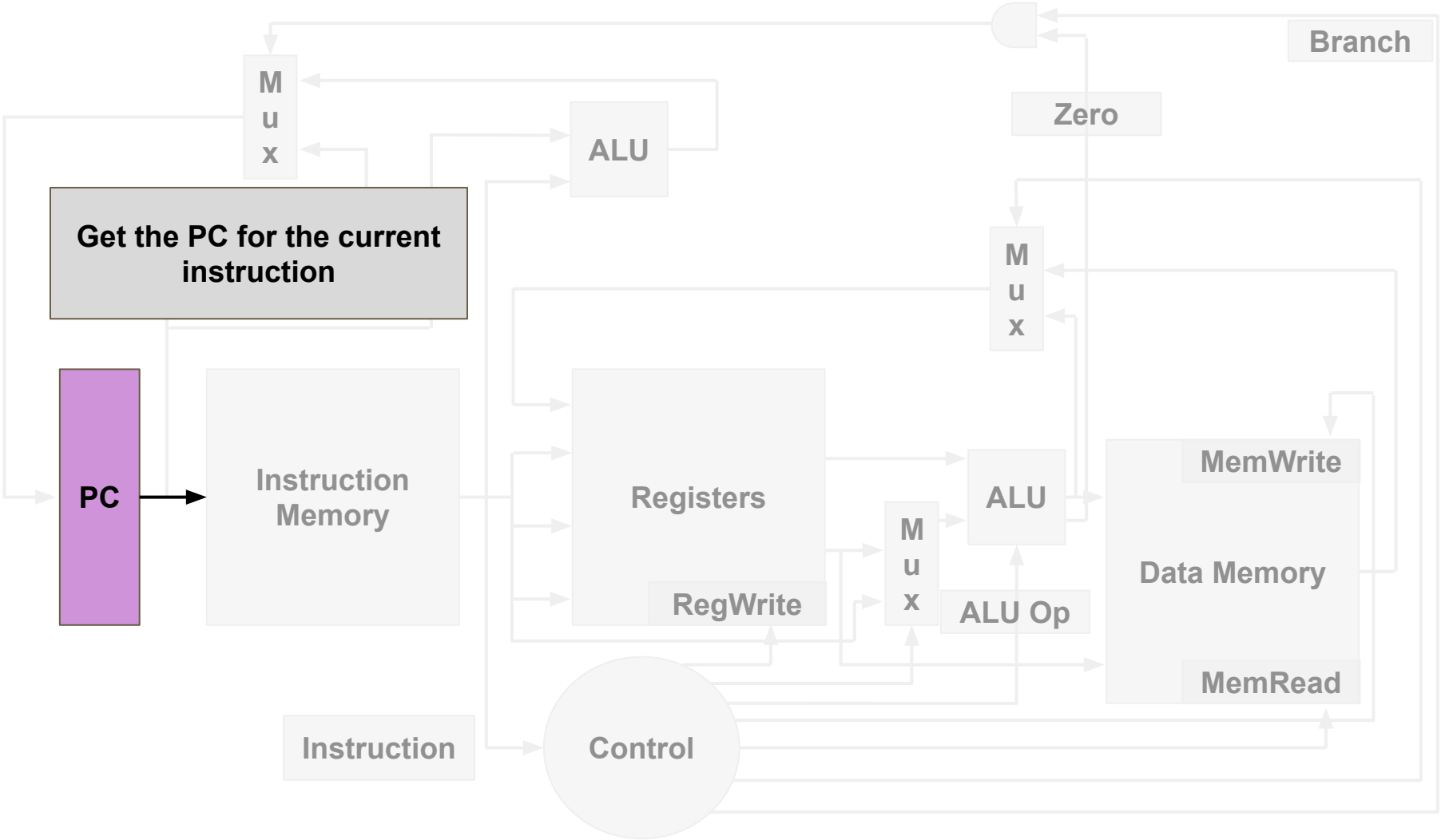

Branch
M
u
x
ALU
Zero
4
ALU
Access values (from registers/immediate) and set control signals
M
u
x
PC
Instruction Memory
Registers
RegWrite
M
u
x
ALU
MemWrite
Data Memory
ALU Op
MemRead
Instruction
Control

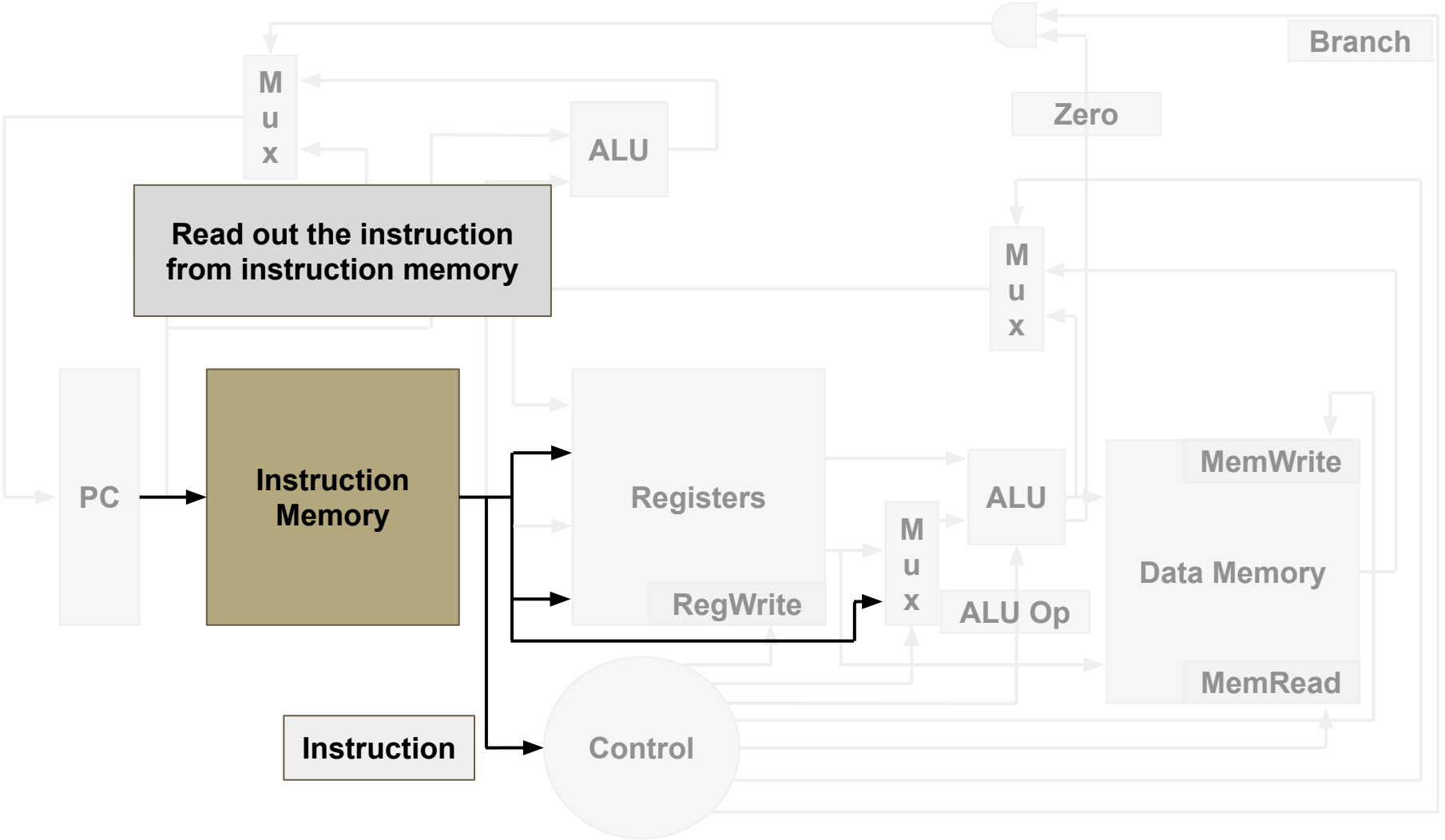

Branch
M
u
x
ALU
Zero
4
ALU
Calculate address for store
PC
Instruction
Memory
Registers
RegWrite
ALU
M
u
x
ALU Op
MemWrite
Data Memory
MemRead
Instruction
Control

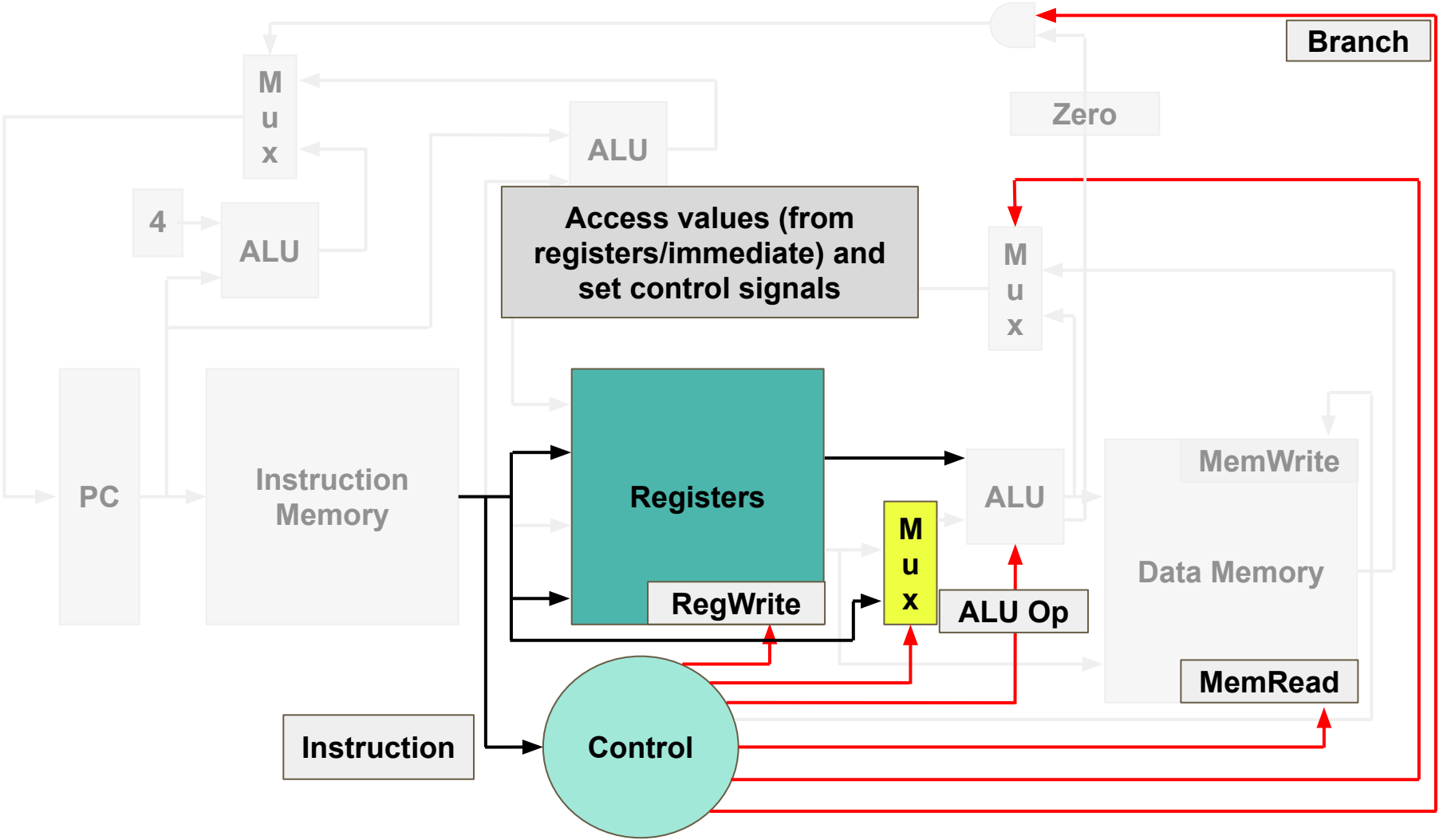

Branch
M
u
x
ALU
Zero
4
ALU
Perform write into data memory
PC
Instruction Memory
Registers
RegWrite
M
u
x
ALU
MemWrite
Data Memory
MemRead
ALU Op
Instruction
Control

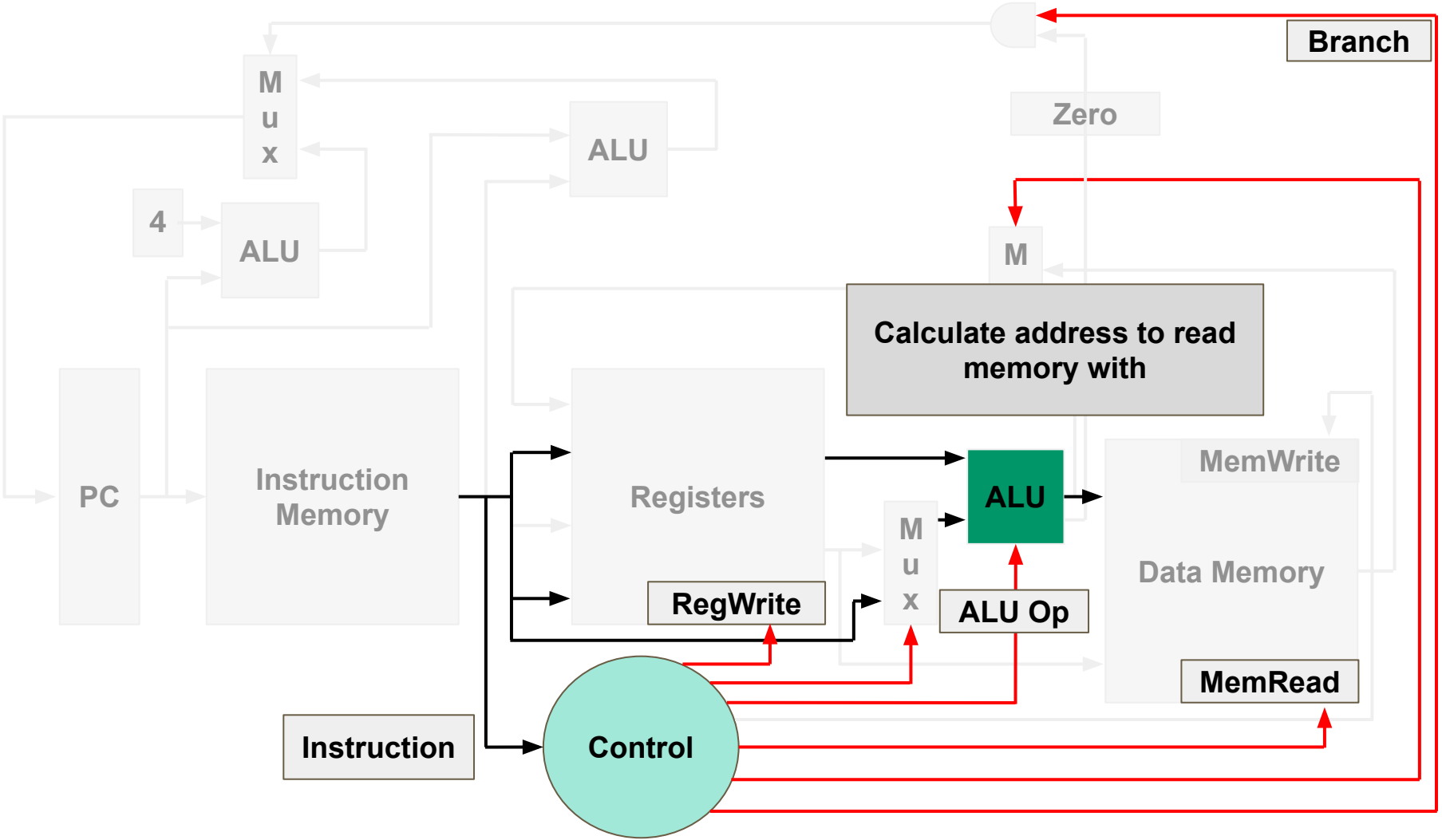

Branch
M
u
x
Increment PC by 4 to move to the next instruction
Zero
4
ALU
M
u
x
PC
Instruction Memory
Registers
RegWrite
M
u
x
ALU
MemWrite
Data Memory
MemRead
ALU Op
Instruction
Control

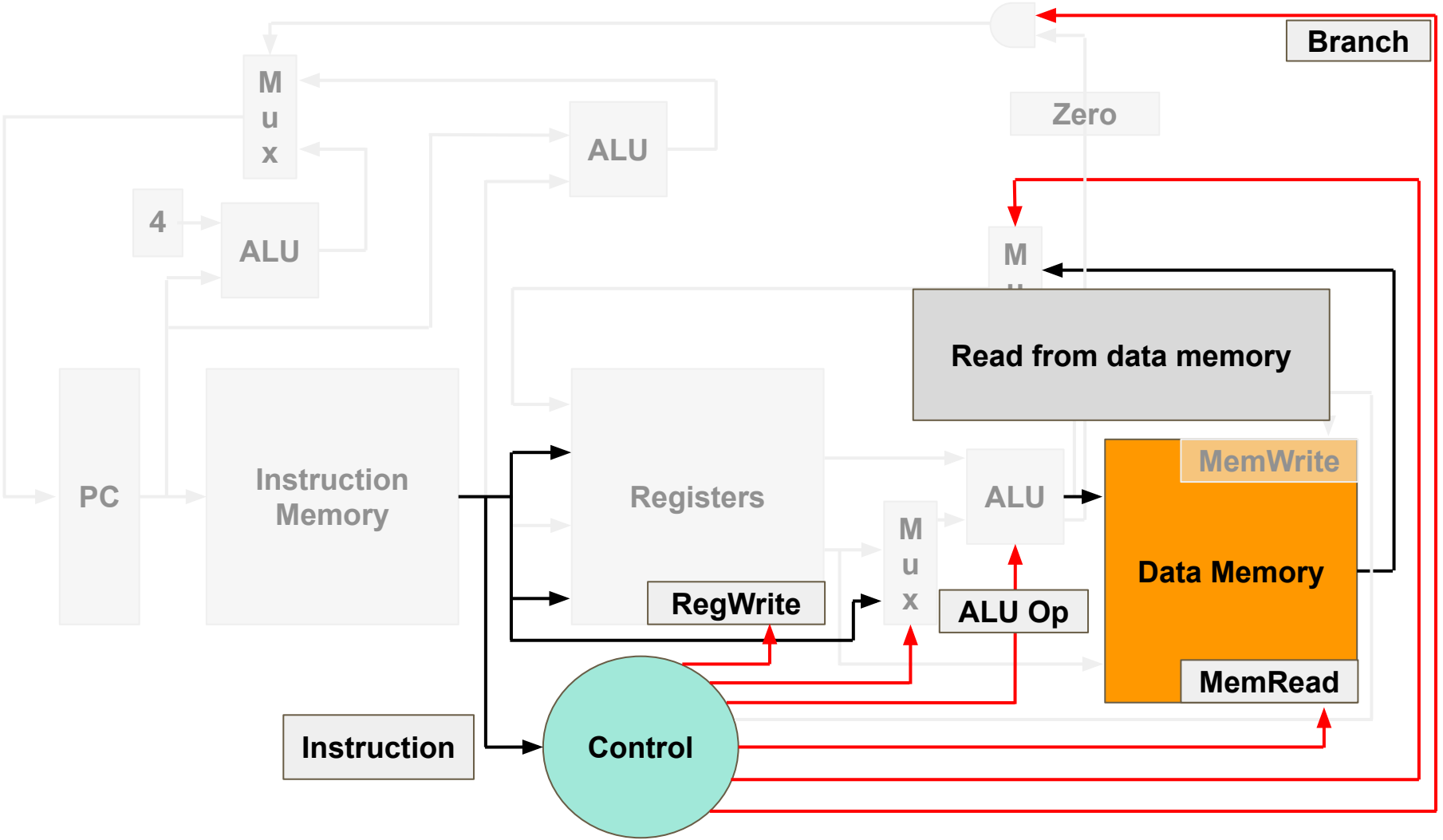
Load Word (lw)

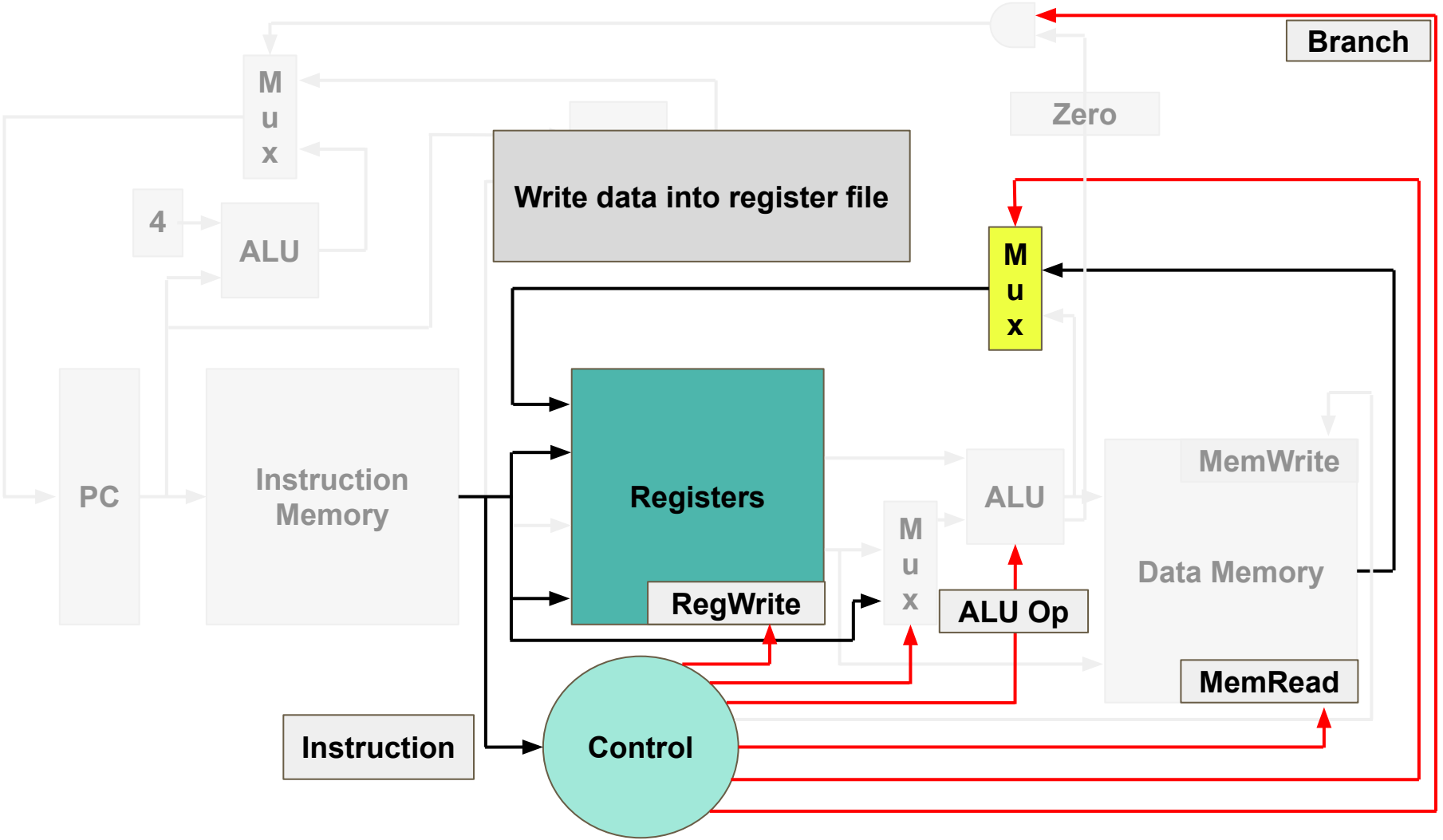

Branch
M
u
x
Zero
ALU
Get the PC for the current instruction
M
u
x
PC
Instruction Memory
Registers
RegWrite
M
u
x
ALU
ALU Op
MemWrite
Data Memory
MemRead
Instruction
Control

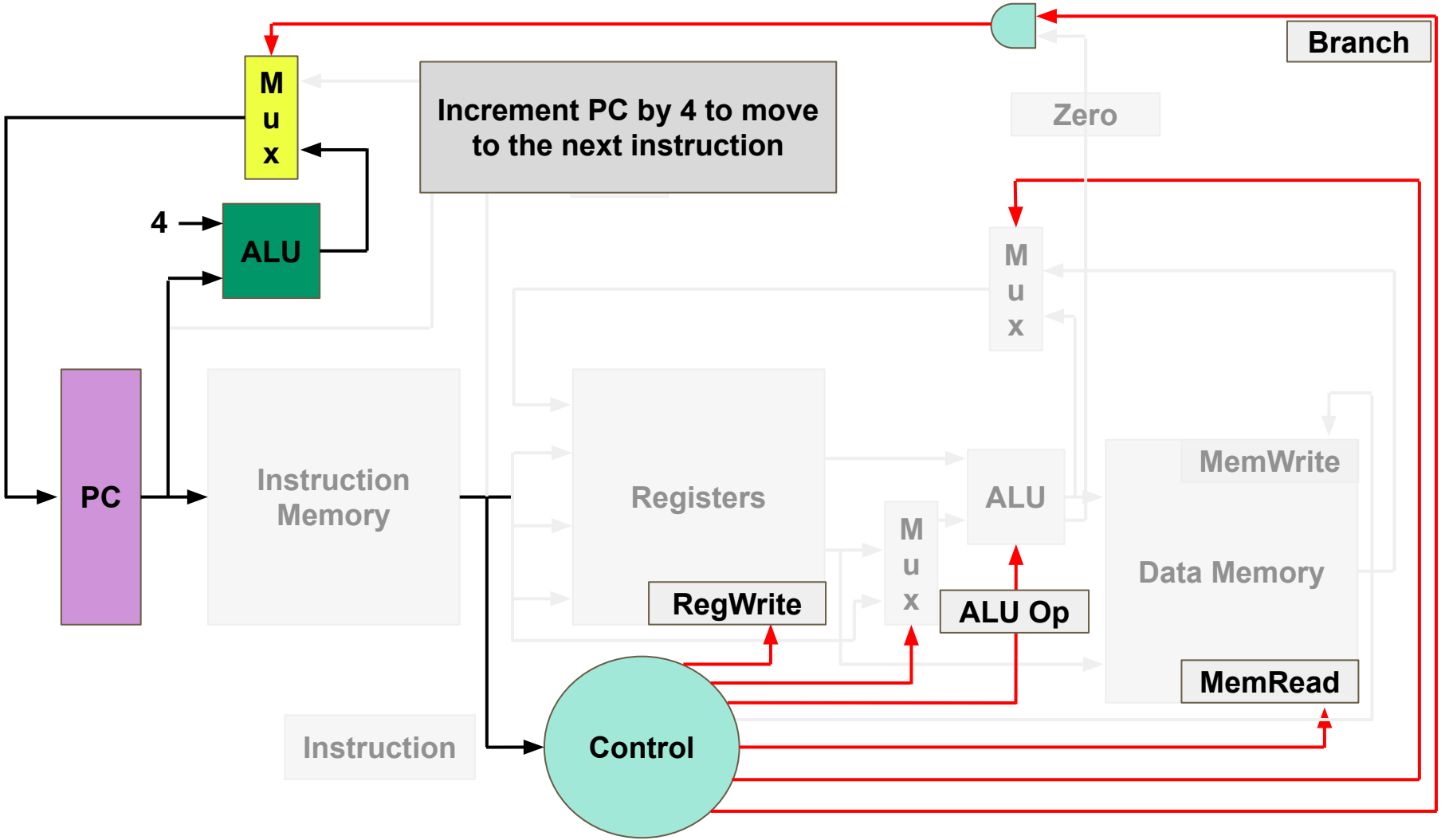

Branch
M
u
x
Zero
ALU
Read out the instruction
from instruction memory
M
u
x
PC
Instruction
Memory
Registers
RegWrite
M
u
x
ALU
ALU Op
MemWrite
Data Memory
MemRead
Instruction
Control


Branch
M
u
x
Zero
ALU
4
ALU
Access values (from registers/immediate) and set control signals
M
u
x
PC
Instruction Memory
Registers
RegWrite
M
u
x
ALU
MemWrite
Data Memory
ALU Op
MemRead
Instruction
Control

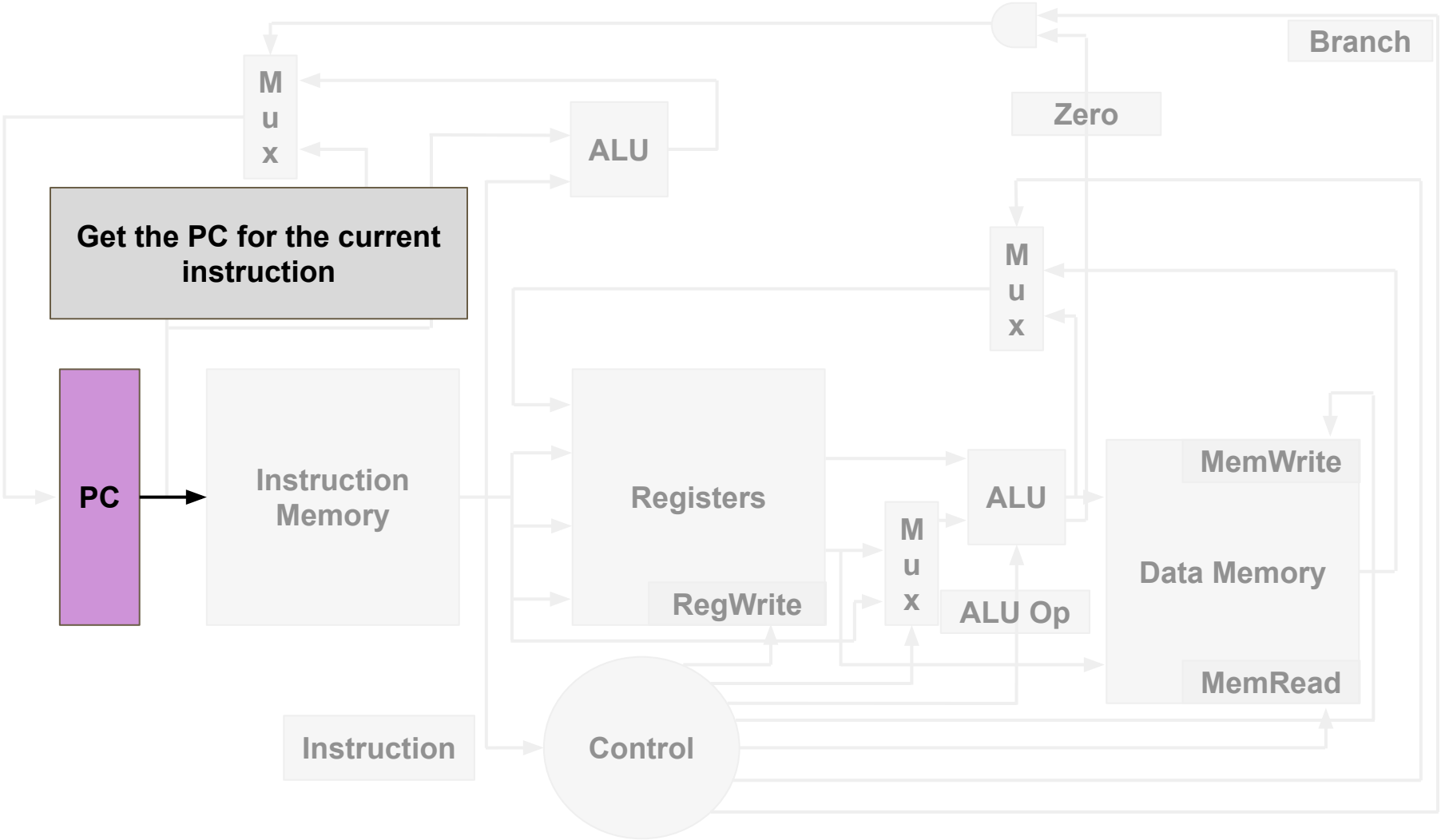

Branch
M
u
x
Zero
ALU
4
ALU
M
Calculate address to read memory with
PC
Instruction Memory
Registers
ALU
MemWrite
M
u
x
Data Memory
RegWrite
ALU Op
MemRead
Instruction
Control

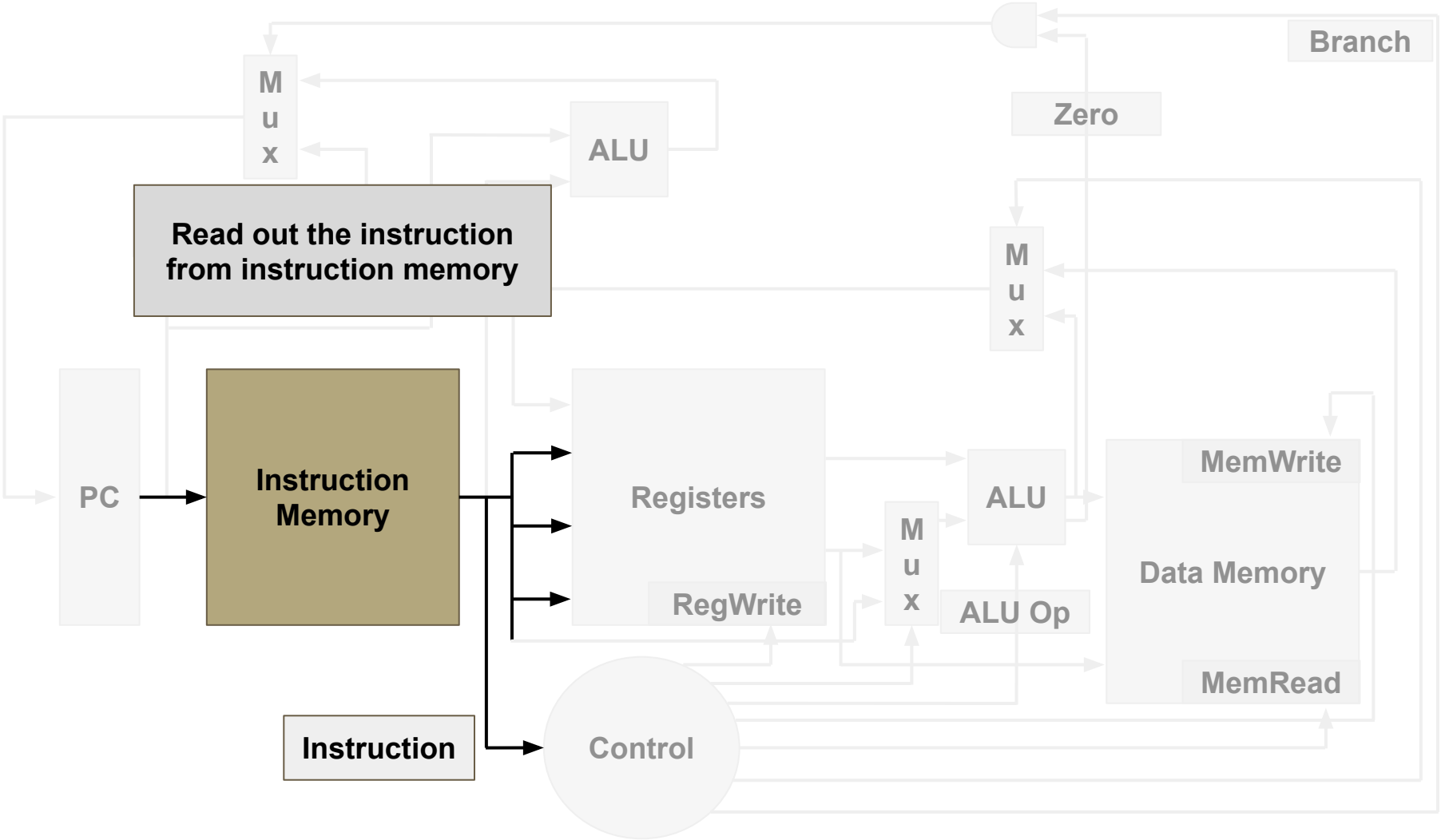

Branch
M
u
x
Zero
ALU
4
ALU
M
u
Read from data memory
PC
Instruction
Memory
Registers
ALU
MemWrite
M
u
x
Data Memory
RegWrite
ALU Op
Instruction
Control
MemRead

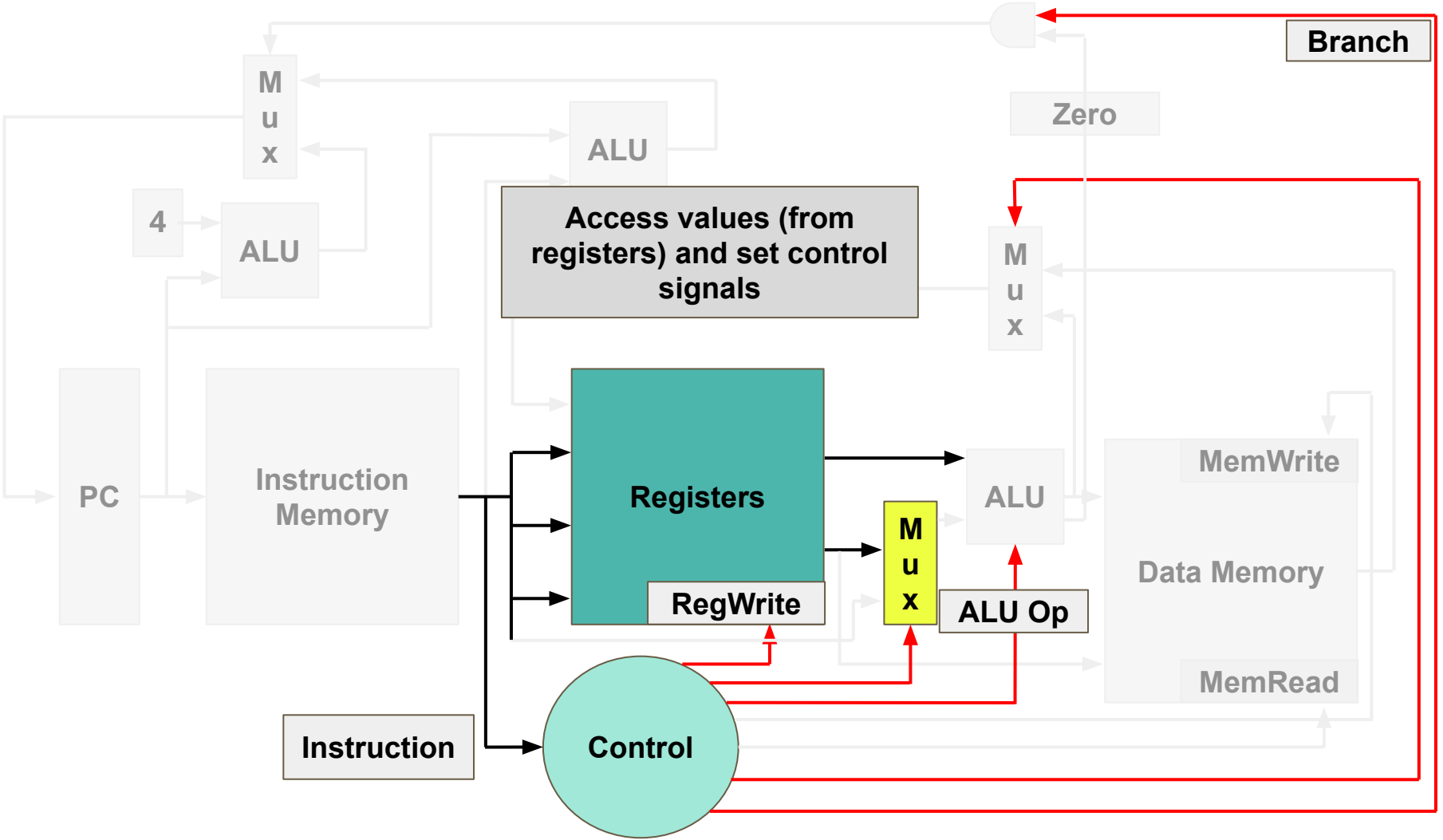

Branch
M
u
x
Zero
Write data into register file
4
ALU
M
u
x
PC
Instruction
Memory
Registers
RegWrite
M
u
x
ALU
MemWrite
Data Memory
ALU Op
MemRead
Instruction
Control

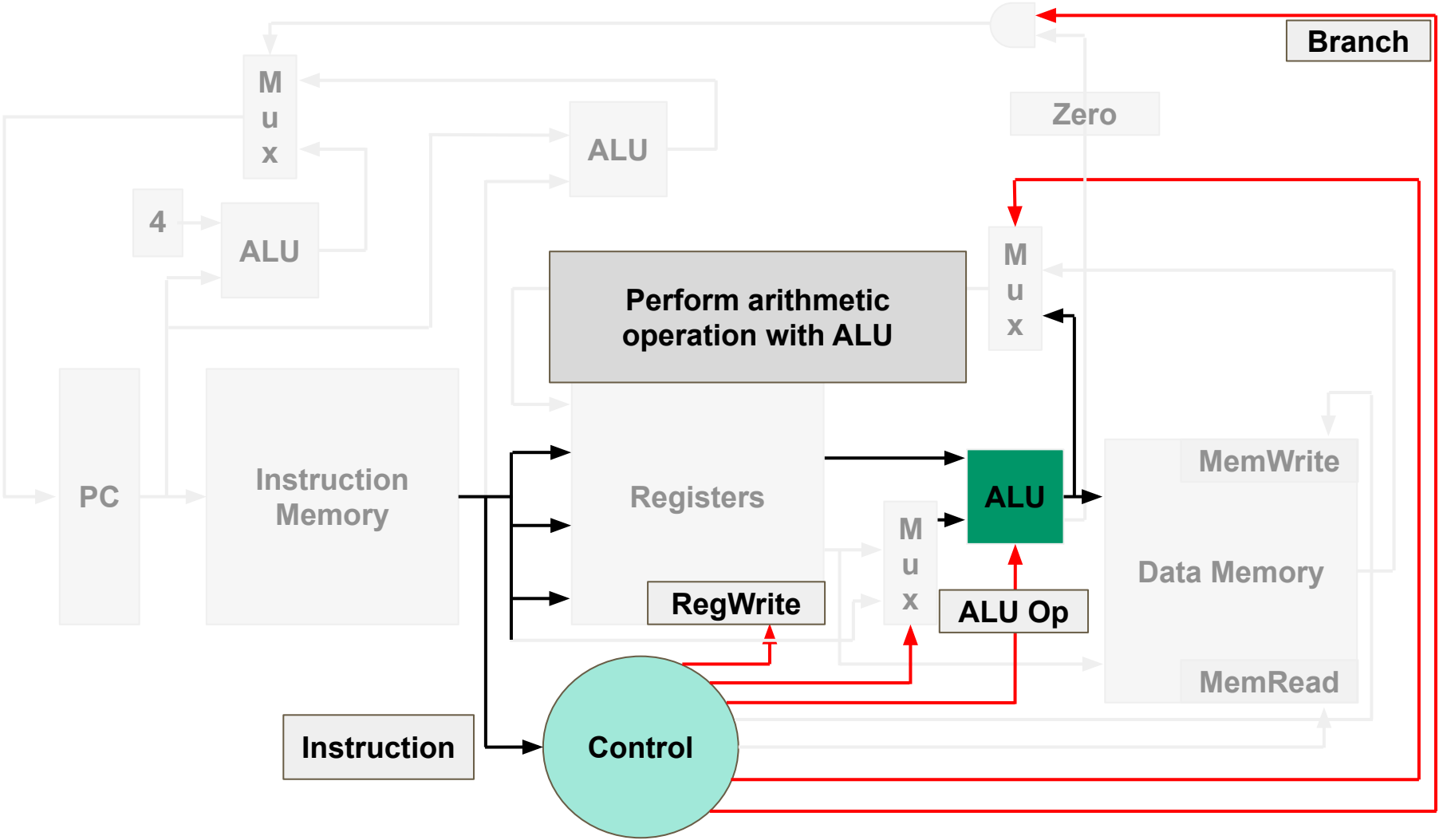

Branch
M
u
x
Increment PC by 4 to move to the next instruction
Zero
4
ALU
M
u
x
PC
Instruction Memory
Registers
ALU
MemWrite
M
u
x
Data Memory
RegWrite
ALU Op
MemRead
Instruction
Control

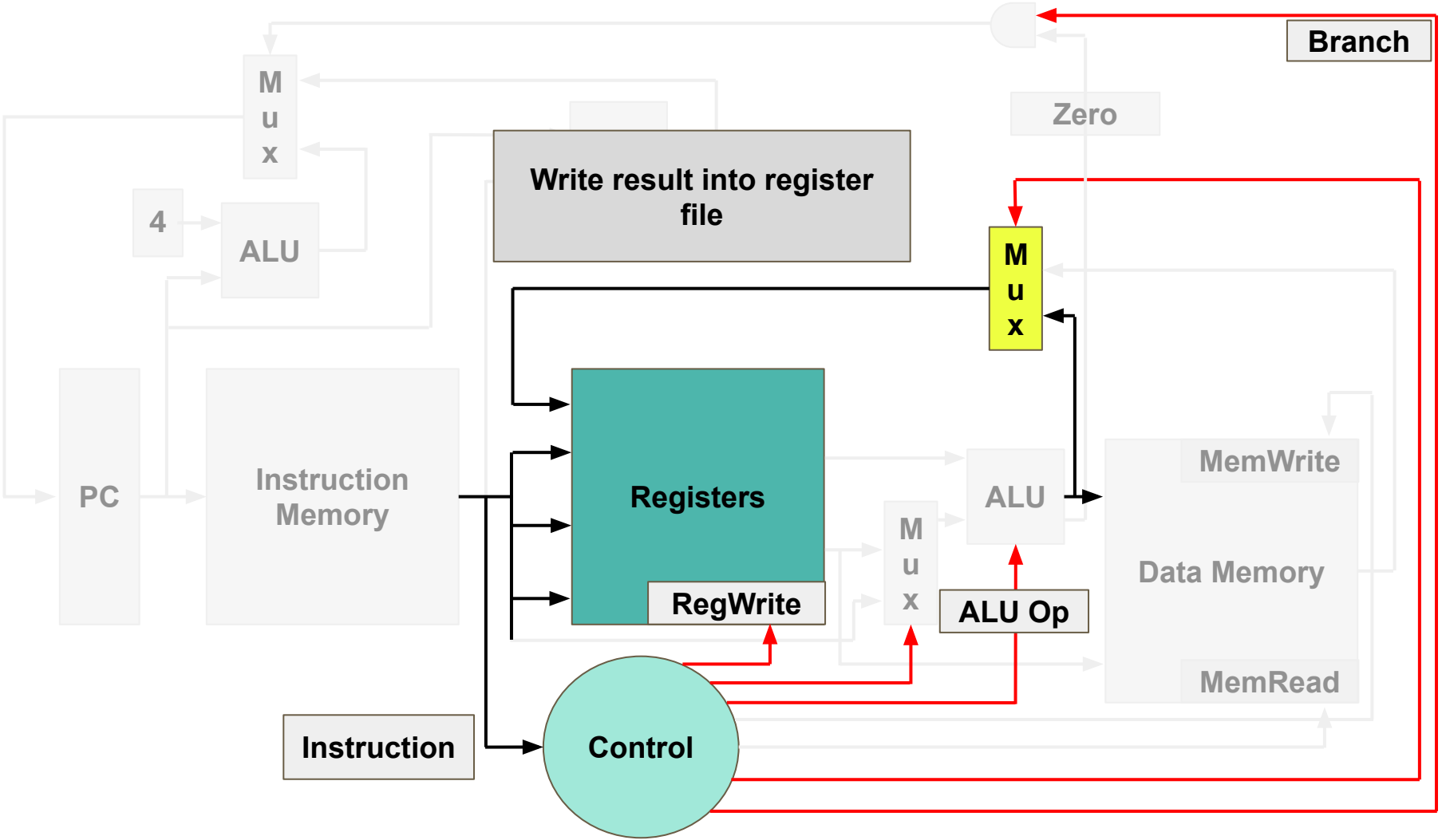
Arithmetic Operations

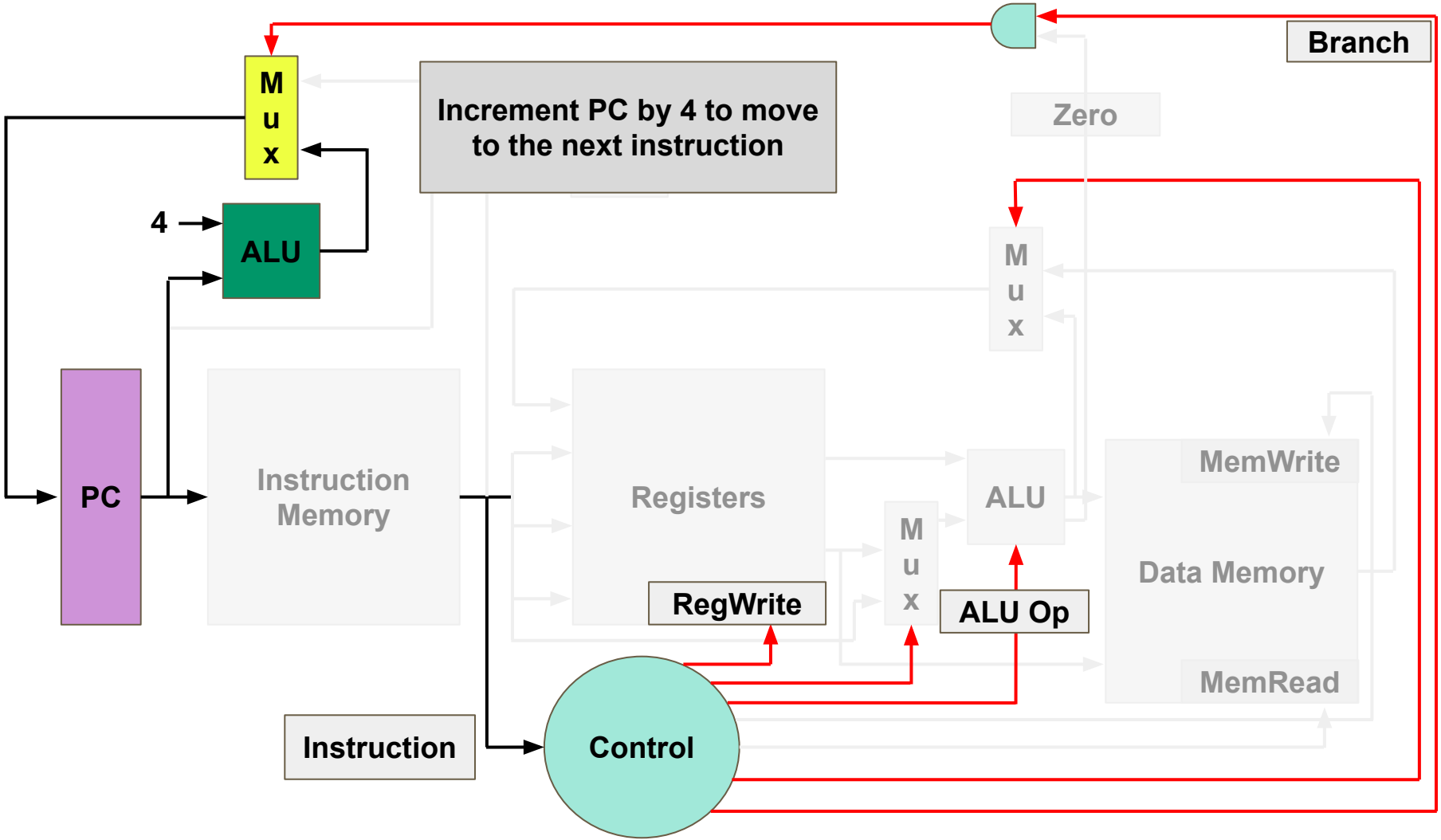

Branch
M
u
x
Zero
ALU
Get the PC for the current instruction
M
u
x
PC
Instruction Memory
Registers
RegWrite
M
u
x
ALU
ALU Op
MemWrite
Data Memory
MemRead
Instruction
Control


Branch
M
u
x
Zero
ALU
Read out the instruction
from instruction memory
M
u
x
PC
Instruction
Memory
Registers
RegWrite
M
u
x
ALU
ALU Op
MemWrite
Data Memory
MemRead
Instruction
Control

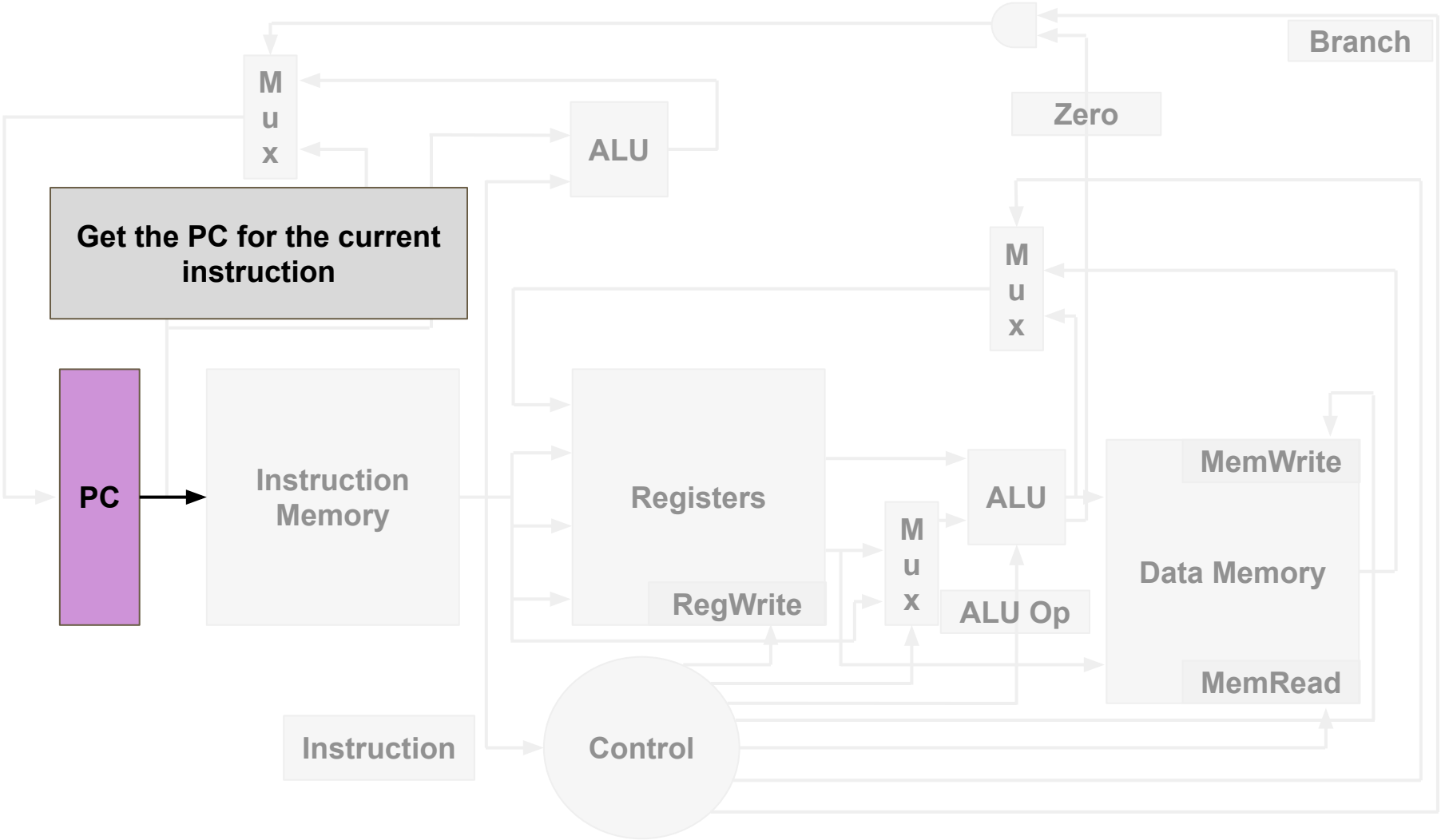

Branch
M
u
x
Zero
ALU
4
ALU
Access values (from registers) and set control signals
M
u
x
PC
Instruction Memory
Registers
RegWrite
M
u
x
ALU
ALU Op
MemWrite
Data Memory
MemRead
Instruction
Control

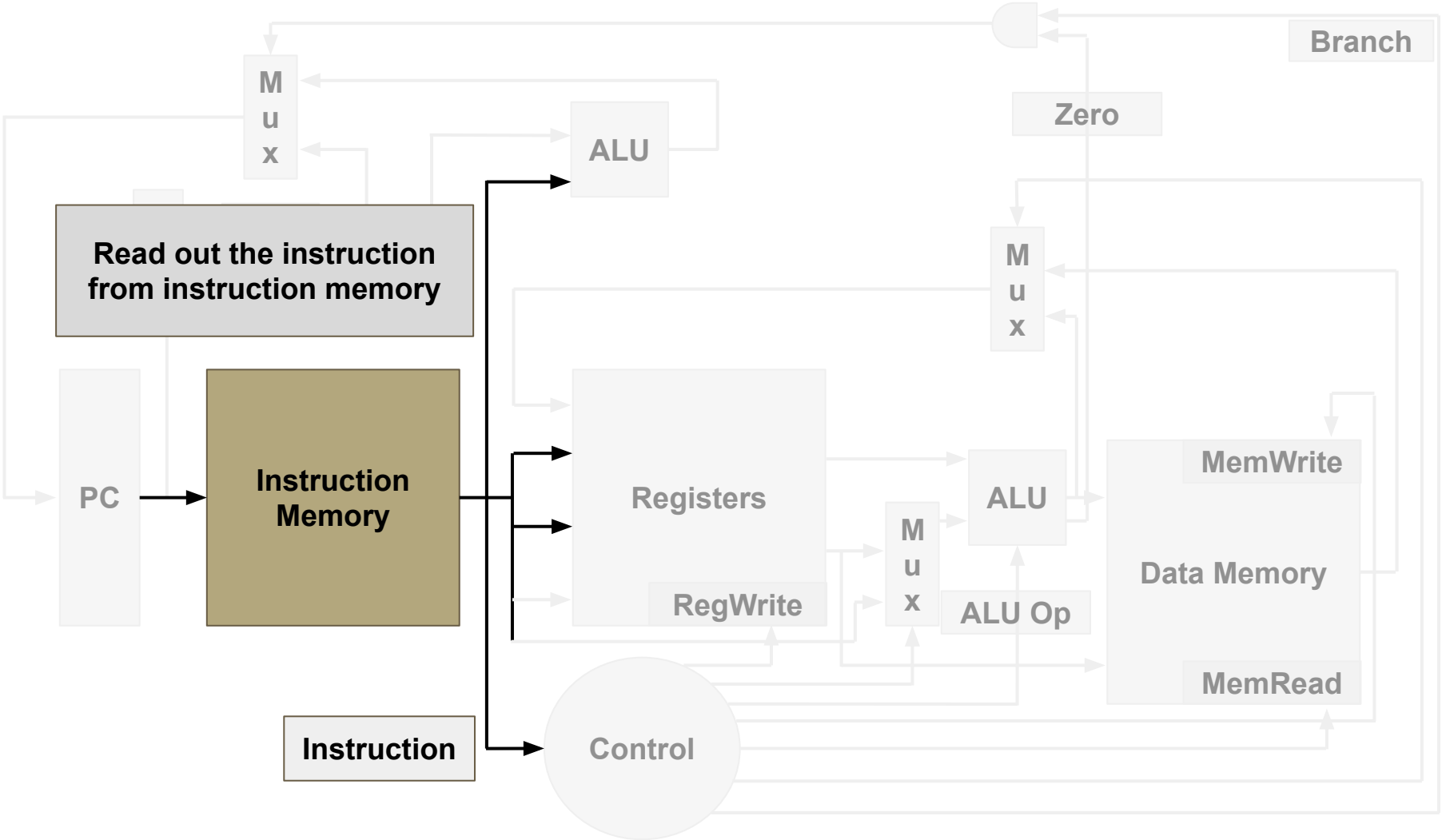

Branch
M
u
x
Zero
ALU
4
ALU
M
u
x
Perform arithmetic operation with ALU
PC
Instruction Memory
Registers
ALU
MemWrite
M
u
x
Data Memory
RegWrite
ALU Op
MemRead
Instruction
Control

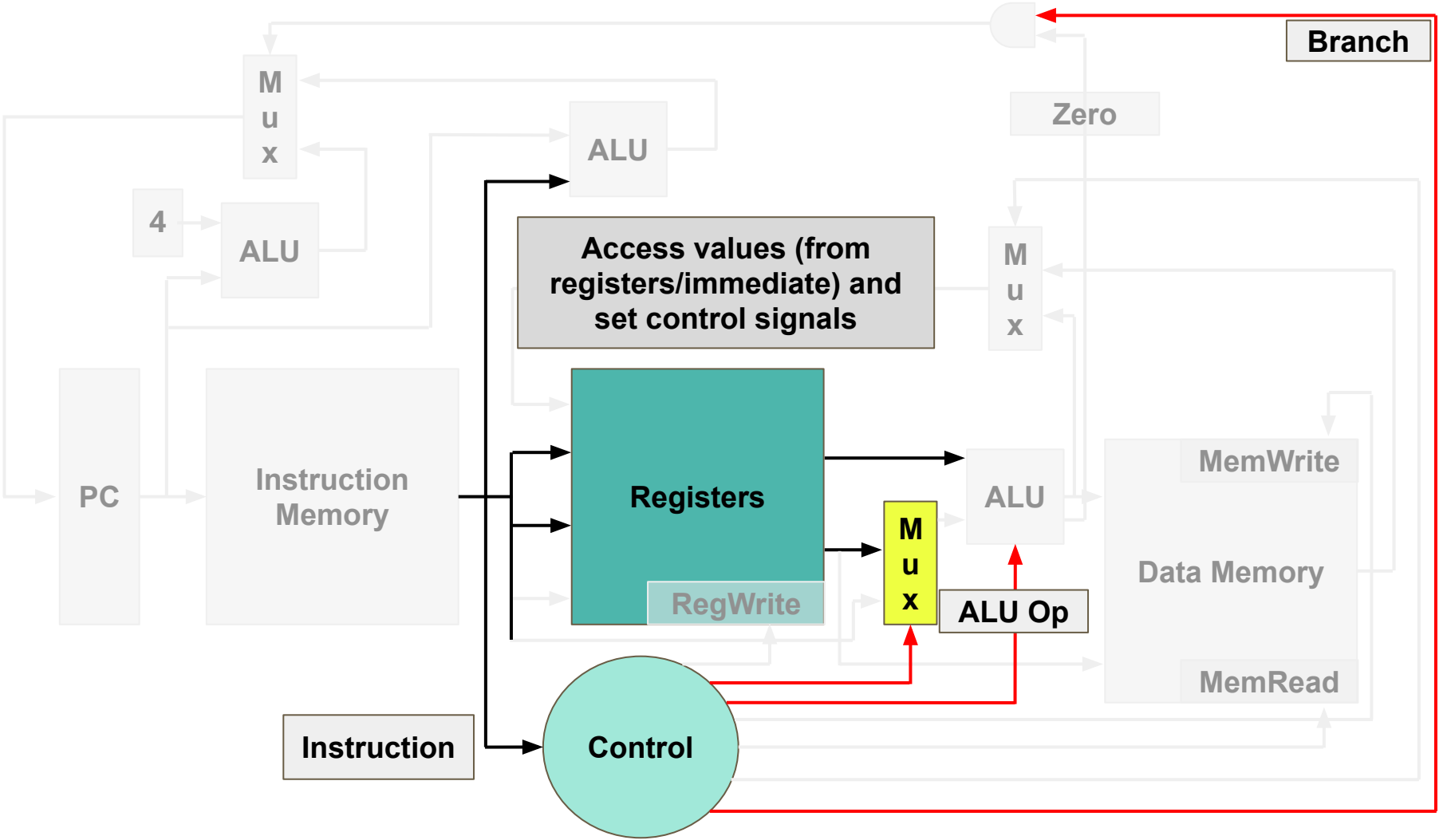

Branch
M
u
x
Zero
4
ALU
Write result into register file
M
u
x
PC
Instruction Memory
Registers
RegWrite
M
u
x
ALU
MemWrite
Data Memory
MemRead
ALU Op
Instruction
Control

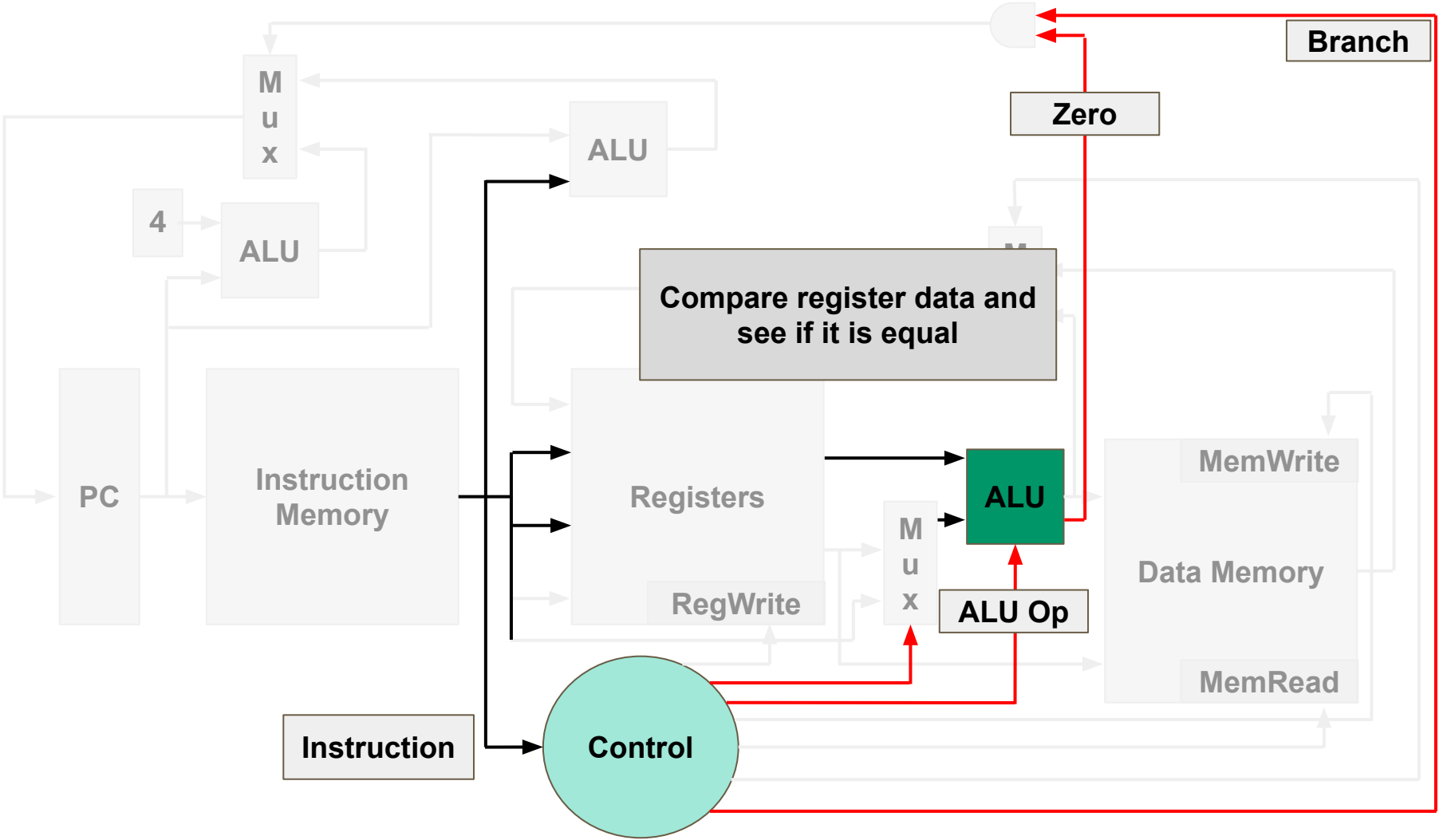

Branch
M
u
x
Increment PC by 4 to move to the next instruction
Zero
4
ALU
M
u
x
PC
Instruction Memory
Registers
ALU
MemWrite
M
u
x
Data Memory
RegWrite
ALU Op
MemRead
Instruction
Control

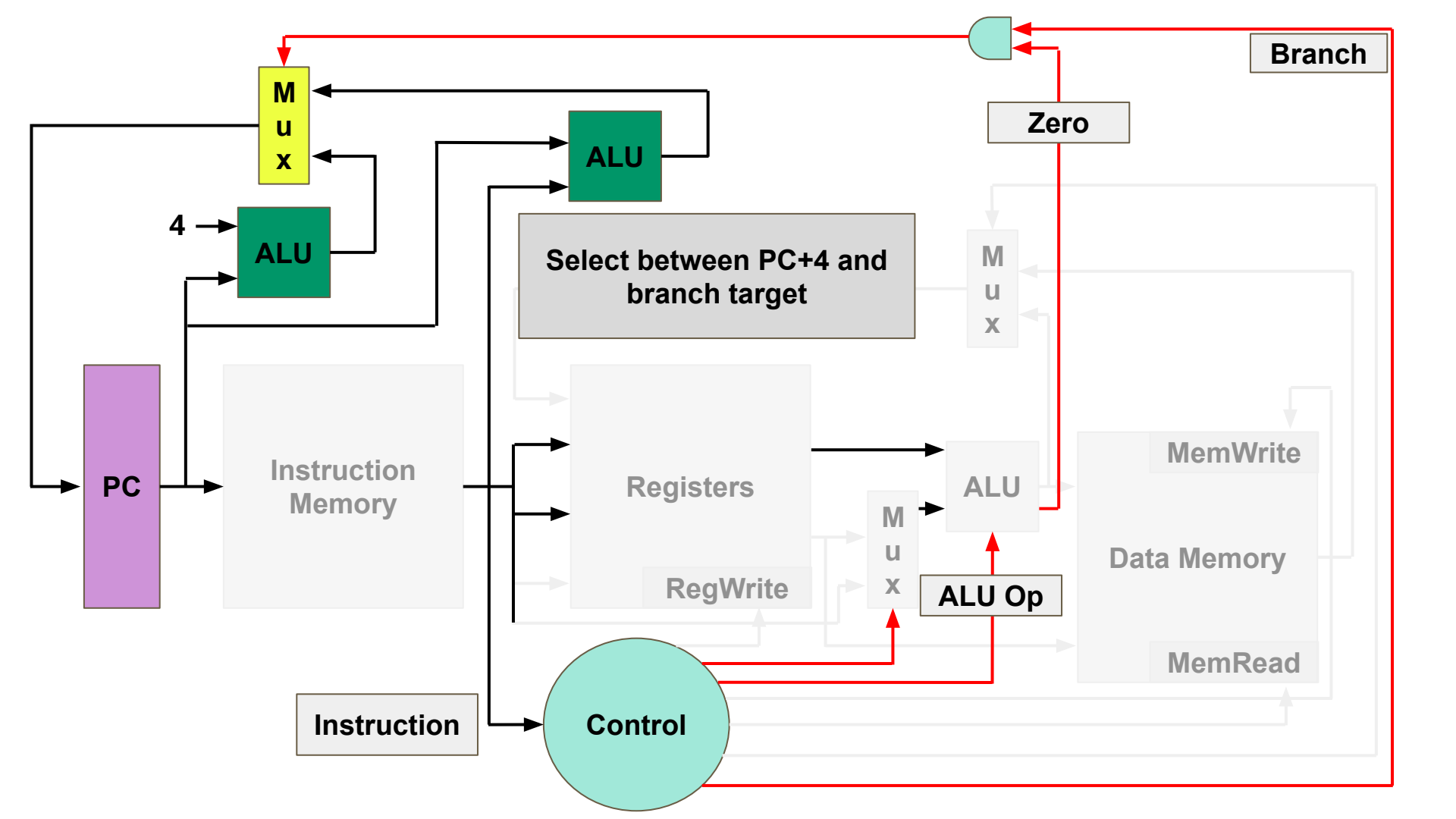
Conditional Branch (beq)


Branch
M
u
x
Zero
ALU
Get the PC for the current instruction
M
u
x
PC
Instruction Memory
Registers
RegWrite
M
u
x
ALU
ALU Op
MemWrite
Data Memory
MemRead
Instruction
Control


Branch
M
u
x
Zero
ALU
Read out the instruction
from instruction memory
M
u
x
PC
Instruction
Memory
Registers
ALU
MemWrite
M
u
x
Data Memory
RegWrite
ALU Op
MemRead
Instruction
Control


Branch
M
u
x
ALU
Zero
4
ALU
Access values (from registers/immediate) and set control signals
M
u
x
PC
Instruction Memory
Registers
RegWrite
M
u
x
ALU
MemWrite
Data Memory
MemRead
ALU Op
Instruction
Control


Branch
Zero
M
u
x
ALU
4
ALU
Compare register data and see if it is equal
PC
Instruction Memory
Registers
RegWrite
ALU
M
u
x
ALU Op
MemWrite
Data Memory
MemRead
Instruction
Control


Branch
M
u
x
Zero
ALU
4
ALU
Select between PC+4 and branch target
M
u
x
PC
Instruction Memory
Registers
RegWrite
M
u
x
ALU
MemWrite
Data Memory
MemRead
ALU Op
Instruction
Control