Processor Definition:

Single-Cycle CPU that implements basic MIPS Instructions

Total Estimated Time : 20 Hrs.

~~**High-Level Design: 20 Min.**~~

Submodules : .75 Hrs.[1]

SignExtend : 20 Min.
Instruction Decoder : 20 Min.
LeftShift : 5 Min.

Instructions : 9.5 Hrs

Midpoint Check-in (by 11/11): 5 Hrs.

LW(Load Word) : 2 Hrs.[2]

SW(Store Word) : 1 Hr.

ALU Controls: 2 Hrs

XORI(Xor with Immediate) : 30 mins
ADD(add) : 30 mins.
SUB(sub) : 30 mins.
SLT(Set on Less than) : 30 mins

After Midpoint Check-in: 4.5 Hrs

J(Jump) : 1.5 Hrs.

JR(Jump Register) : 1 Hr.

JAL(Jump and Link) : 1 Hr.

BNE(Branch Not Equal) : 1 Hr.

Test/Debug : 5.5 Hrs

Test Program (by 11/14) : 2.5 Hrs
Debugging Submodules : 2.5 Hrs
Synthesis on Vivado : .5 Hrs.

Report : 4 Hrs

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[1] Only the ones that haven't been introduced yet in past labs

[2] Time including testing. This is our first module, and we'll build upon it, so Load Word would take the longest.