Two stage Boost system capable of 5V to 192V-440V DC-DC conversion

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ABSTRACT: Numerous electronic and MEMS devices based on functional materials require an ultra-high electrical field and thus a high electrical voltage for their operation, while only a negligible current is needed whereas ubiquitous and mobile computing applications of these devices only support a low voltage source for energy supply. Which often come in the form of a small form factor battery with a typical voltage of 3.7V - 5V. In such scenarios DC-DC conversion becomes essential. In this work a two stage boost system is presented which can provide 192V to 440V at its output while using a 5V input supply. Output can be adjusted by changing the values of inductors from 10µH to 120µH. Converter has been designed and fabricated in 1um SOI process. In the results it is also demonstrated that the two stage boost circuit requires 45.8% less combined inductance as compared to the single stage design.

1 INTRODUCTION

Devices based on functional material require high voltage for their regular operation e.g. electrostatically actuated MEMS devices, tunable ferroelectric materials [Ning et al. (2014)] etc. all operate on more than 100V. Availability of higher voltage also allows the MEMS chip designers to save the silicon area. For example in MEMS devices comb drives are used for electrostatic actuation. Force generated by the comb drive is directly proportional to the square of applied voltage. This effect enables the designer to reduce the comb size if higher input voltage is available [Khan at al. (2010)]. Analytically saying if a comb drive is designed to generate a certain amount of force at 100V, the same amount of force can be generated by a 16 times smaller comb drive if 400V are applied at its input. This shows that the availability of high voltage can tremendously reduce the size of electrostatic actuators and can help in packing more functionality in the same silicon area.

Supply voltage of digital ICs is continuously reducing. In most of the applications high voltage devices have to be controlled by digital ICs which are mostly operating on either 5V of power supply or 3.3V of battery. To avoid the use of two different voltage sources in a system (one for the digital part and one for the high voltage I/O part) DC-DC converters are required. A number of DC-DC boost converter ICs are available in the market which can provide tens of volts at their output.

LT3494 (2006) is an IC developed by Linear Technology which can perform "3V - 40V" conversion. LT3460 (2007) is another IC developed by the same company and is capable of "2.5V – 36V" conversion and provides better output current as compared to LT3494. Texas Instruments has also developed an IC [TPS61045 (2009)] for DC-DC conversion. Their IC is capable of "1.8V – 28V" conversion and has the maximum efficiency of 85%. All previously mentioned ICs require off-chip components and their output voltage is less than 50V.

Past research was mainly focused on increasing the efficiency of low voltage DC-DC converters. For example Kong et al. (2012) have improved the efficiency of a 3.7V-8V boost converter. Nakase et al. (2013) have presented a boost system which is capable of 1.03V-5V conversion. Wang et al. (2013) have also represented a 5V-12V boost converter with improved efficiency.

In the last couple of years, research attention has been diverted towards the development of high voltage converters. Jeon et al. (2013) have developed a single stage boost converter which is capable of 3.3V-80V conversion. Shen et al. (2012) have presented a charge pump design which can generate 120V at its output. Test results of this chip are later published by Hofmann et al. (2012). Output of this circuit is not adjustable and the output current is also limited due to the use of charge pump circuit topology.

In none of the previous approaches ultra-high voltage (400V+) conversions were attempted. The highest achieved output voltage is 120V [Shen et al. (2012)]. In this work a two stage boost circuit is represented which is capable of performing ultra-high voltage conversions. By using the 5V input supply the designed converter can generate 192-440V at the output. Output voltage is adjusted by the varying the value of external inductors from 10µH to 120µH.

The remainder of the paper is organized as follows. In the next section proposed converter topology is discussed. Section 3 elaborates the modified boost circuit architecture. Chip fabrication is presented in Section 4 and results are discussed in Section 5. At the end paper is concluded in Section 6.

2 PROPOSED CONVERTER TOPOLOGY

In this section the design goals and the proposed design is discussed. Design goals can be summarized in following three points

1) System should be capable of doing 5V - 400+ V conversions.
2) Output of the system should be adjustable to widen the application domain.
3) If external components have to be used, their size should be minimal, so that in future they can be monolithically integrated or packaged together with the chip

For high voltage conversion charge pump circuit topology or the boost circuit topology can be used. Charge pumps have the advantage of no off-chip component but their efficiency is compromised due to high number of required stages and in comparison to boost circuits, charge pumps provide less output current. Due to the before mentioned reasons most of the commercially available ICs like LT3494 (2006), TPS61045 (2009), LT3460 (2007) uses the boost circuit.

The output of the charge pump is fixed and to make it adjustable DAC array has to be used as shown by Ning et al. (2014). In contrast to charge pump the output of the boost circuit can be varied by changing the external inductor. This adjustability is the second design goal of this work.

Owing to above mentioned reasons, boost circuit topology was selected. Boost circuits definitely have the disadvantage of external inductors but its output current and efficiency at high voltage conversions make it a better candidate. In order to fulfill the third design goal, 5V- 400+ V conversions should be done by using minimum external inductance. In the next section an endeavor has been made to minimize the required inductance.

3 BOOST CIRCUIT ARCHITECTURE

In this section initially basic operation of the single stage boost circuit is discussed. Later it is improved by using the discontinuous conduction mode (DCM) and two stage architecture.

Schematic of the boost circuit is shown in Figure 1. Its working can be divided into two phases. In charging phase switching stage is closed and the diode is reversed biased. In this circuit configuration inductor charges until a steady state is achieved. The second spike generation phase starts by the opening of switching stage. Opening of switching stage interrupts the inductor current $i_L(t)$ which results in the generation of a voltage spike whose magnitude can be found by using equation 1.

$$v_L(t) = -\left(L\frac{d\, i_L(t)}{dt} \right) \quad (1)$$

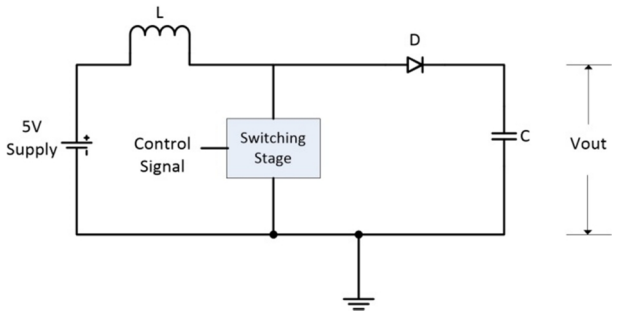

Figure 1. Single stage Boost circuit

Polarities of the generated voltage spike and the input voltage source add up and momentarily make the diode forward biased which allows the transfer of generated voltage to the capacitor.

From equation (1) it is clear that to increase the generated voltage, either inductance or the rate of change of current has to be changed. Rate of change of inductor's current is dependent upon the time required to turn off the high voltage transistors used in the switching stage. Transistor's turn off time is the sum of turn off delay, fall time and the reverse recovery time. For the selected technology (xdh10) and transistors the minimum turn-off time is 3.415µs [7].

By using the information of duty cycle and the minimum turn-off time, maximum clock frequency of the boost circuit in continuous conduction mode (CCM) can be determined. In CCM, the duty cycle of the boost circuit can be found by equation (2)

$$D = \frac{V_o - V_s}{V_o} \quad (2)$$

For 5V-400V conversion, V_o = 400V and V_s = 5V. By substituting these values in equation (2), the value of required duty cycle is obtained and i.e. D =

98.75%. This implies that turn-off duration for the transistors of switching stage would be only 1.25% time of the clock period. If it is assumed that 1.25% time of the clock period is 3.415 µs (i.e. the minimum turn-off time) then 100% time of the clock period would be

$$T = \frac{3.415\ us}{0.0125} = 273.2\ \mu s$$

Maximum operating frequency can be found by taking the inverse of above found time period i.e.

$$f_{max} = \frac{1}{273.2\ us} = 3.66\ kHz$$

For a boost circuit the above stated frequency is quite low and if it is used it would result in a very large inductor. Exact value of inductor can be found by using equation (3)

$$L = \frac{D(1-D)^2 R}{2f} \qquad (3)$$

As stated in the introduction the targeted load for this work is the devices which require high voltage but low current. For the sake of calculation, here a load current of 10µA is assumed. At 400V, load current of 10uA results in a load resistance ® of 40 MΩ.

By substituting the values of D, R and f in equation (3) we get the value of minimum required inductor and that is

$$L \approx 843\ mH$$

In currently available IC technology, fabrication of such a big inductor is not possible. This value should be reduced so that in future at least 3D packaging can be tried. To reduce the inductor size, the boost circuit has to be operated in discontinuous conduction mode (DCM). In DCM the inductor current becomes zero before the start of the next clock cycle. This rapid change in inductor current results in a higher di/dt term. From equation (1) it can be seen that for a fix v_L, increase in the rate of change of current results in a reduced value of L.

Boost circuit shown in Figure 1 was implemented in cadence ® by using a 1um SOI process (xdh10) from xfab. In post layout simulations it is found that 5V-400V conversion in DCM can be achieved by using a 350µH inductor.

To further reduce the inductor size, a multistage approach was analyzed because more inductors connected in series can generate a higher resultant voltage spike. A two stage boost circuit is shown in Figure 2. This concept is also simulated in Cadence ® by using xdh10 technology. The resultant waveform is shown in Figure 4. It can be seen from Figure 4 that with the help of two 120µH external inductor the proposed circuit while operating under discontinuous conduction mode can attain a stable voltage of 435V in just 2ms.

Equivalent circuits of two stage boost when the switches are open and closed are shown in Figure 3. The operation of the circuit can be divided into following two phases.

3.1 *Phase 1 (Charging Phase)*

When switches are closed, both inductors are in charging mode. Current $i_{L1}(t) + i_{L2}(t)$ passes through the inductor L_1 and current $i_{L2}(t)$ passes through the inductor L_2. Maximum value of the charging current is dependent upon the R_{on} of the switching stages, inductance of the inductor and internal resistance of the inductors.

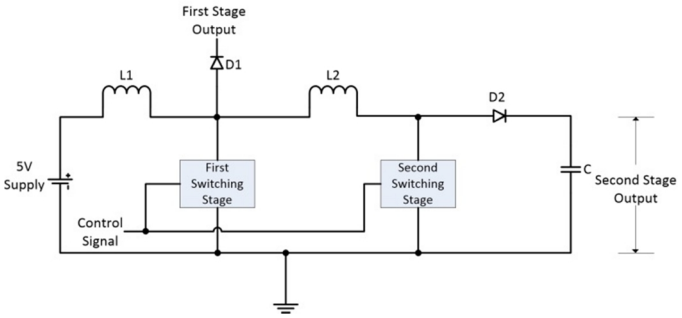

Figure 2. Two stage Boost Circuit

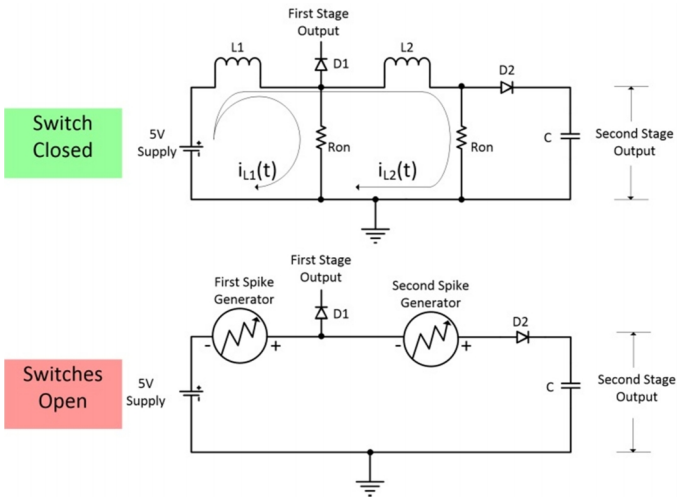

Figure 3. Equivalent Circuit Topology when switches are close and open

3.2 *Phase 2 (Spike Generation)*

After the elapse of time DT (D is the duty cycle and T is the time period), switches become open and the normal current flow is interrupted. This interruption in the current flow generates a high voltage spike in both of the inductors and series connection between the inductors adds the generated voltage spikes.

Magnitude of the generated voltage spike can be calculated by using equation (1).

As shown earlier more current passes through L_1 in phase 1, which results in a higher voltage spike generated by L_1 as compared to L_2. Voltage spikes generated by L_1 and L_2 can be equalized by increasing the inductance of L_2.

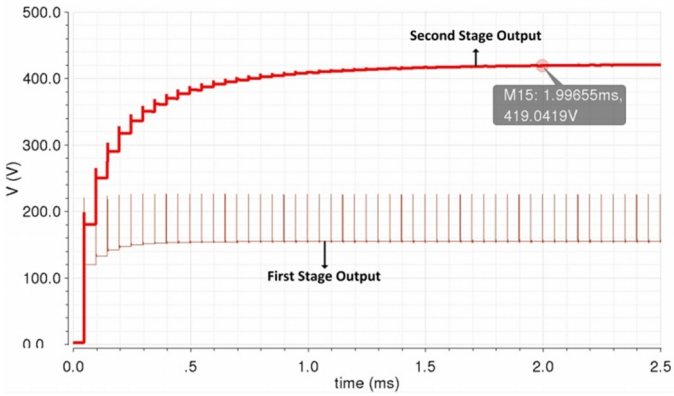

Figure 4. Transient response of two stage boost converter by using two 120uH inductors

To equalize the voltage spikes $L_2 \neq L_1$ and the required value of L_2 can be determined by equation (4).

$$v_{L1}(t) = v_{L2}(t)$$

$$L_1 \frac{d}{dt}[i_{L1}(t) + i_{L2}(t)] = L_2 \frac{d}{dt} i_{L2}(t)$$

$$L_2 = \frac{L_1 \frac{d}{dt}[i_{L1}(t) + i_{L2}(t)]}{\frac{d}{dt} i_{L2}(t)}$$

$$L_2 = L_1 \left| \frac{\frac{d\, i_{L1}(t)}{dt}}{\frac{d\, i_{L2}(t)}{dt}} + 1 \right| \qquad (4)$$

Inductors of equal inductance can also be used, if the condition formulated in equation (4) is hard to satisfy. In this case the voltages generated by two stages would not be equal.

In the next step designed two stage boost system was simulated in cadence ® with a number of different inductors to ensure the adaptability and stability of the system. It is observed that a number of output voltages can be generated by using different set of inductors.

4 CHIP FABRICATION

To verify the effectiveness of multistage boost architecture a chip has to be designed and fabricated. As an initial step all the available high voltage IC technologies were analyzed for this specific design and it is found that xdh10 [7] best suits the requirements. Xdh10 is a 1µm SOI process from xfab.

Designed chip includes switching stages, diodes for both stages, and a 265pF capacitor at the output of stage 2. All these components are optimized, to handle the voltage up to 650V. Trenches are placed around the capacitor, diodes and switching stages so that leakage current can be reduced and a problem in one part does not affect the others. Size of the chip is 35 mm^2 and its picture is shown in Figure 5.

Schematic of the chip is shown in Figure 2. Due to the on-chip capacitor for stage 2 its output is automatically low pass filtered. At the output of first stage, voltage spikes are produced (one spike/clock cycle). These spikes can also be converted into a stable voltage by using an external capacitor. Attachment of an external capacitor gives the chip ability to produce two stable output voltages at the same time. Chip output with two 120uH inductor is shown in Figure 6. At the input 5V and the clock signal are supplied externally. Clock current is quite low because it has to only drive the gate terminal of transistors.

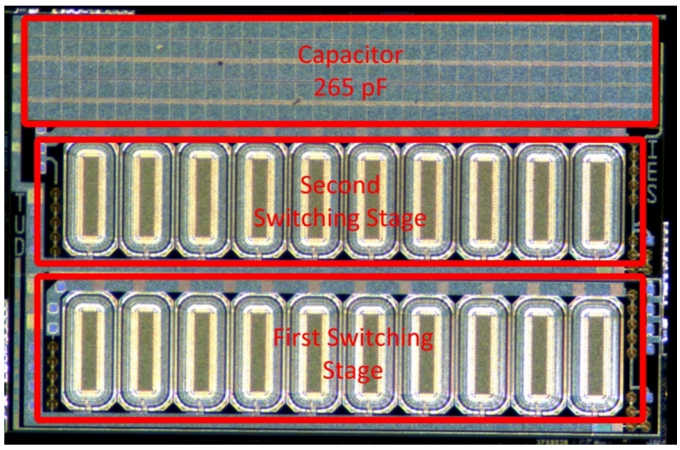

Figure 5. Picture of fabricated chip

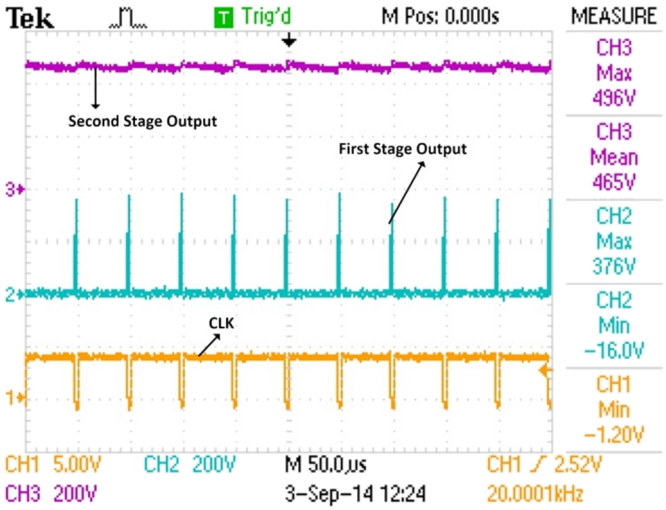

Figure 6. Chip output when two 120uH inductors are used

5 RESULTS

Figure 6 is showing the output of the designed system when two 120µH inductors are used. As designed, stage 1 is producing the voltage spikes and stage 2 is providing a stable output voltage due to the on-chip capacitor. To verify the adaptability of the output voltage, chip has been tested with a number of external inductors and the results are summarized in Table 1. The test setup is shown in Fig 10.

Figure 7 is showing the "V_{out} vs load current" graph. It can be seen that an increase in the load current reduces the output voltage. 100µH and 120µH inductors show better voltage stability whereas worst voltage stability is shown by 10µH inductor. System is designed to provide more than10µA at 400V. It can be seen from zoomed voltage curve of 120µH inductors that actual chip can maintain output voltage higher than 400V while supplying more than 70µA load current.

"Operating frequency vs load current" graph is shown in Figure 8 and it can be seen there that higher load currents require higher operating frequency. Figure 8 is also showing that larger inductors can operate on lower frequencies whereas smaller inductors require higher operating frequencies. Quantitatively speaking 100µH and 120µH inductors can be operated with less than 100 kHz operating frequency for most of the loading conditions whereas smaller inductors (10µH and 15µH) require higher operating frequency in range of 125 kHz to 200 kHz. Higher frequency increases the losses and reduces the efficiency.

Figure 9 is showing the "efficiency vs load current" graph. Efficiency increases by increasing the load current but at the cost of output voltage. More than 20% efficiency is shown by 47µH, 100µH and 120µH inductors. Best efficiency (i.e. 34.12%) is shown by 100µH inductor at 2.2mA load current. To compare the efficiency with other high voltage converters, charge pump represented by Shen et al. (2012) is considered here. Their charge pump can provide output voltage of 120V, can supply load current up to 100µA and shows 12% efficiency. The boost system presented in this work when operated with 100µH inductors gives 120V output, while supplying a load current of 1mA-2mA and the efficiency of the system varies from 20-34% (higher load current results in better efficiency). When compared at the output voltage of 120V the boost system presented here surely shows better attributes. At higher voltages (400+V) the efficiency is less due to discontinue conduction mode.

The chip is specifically designed to generate 400+V. Such high voltage can be achieved by using either 100µH or 120µH inductors. Due to this design objective chip shows better stability, better efficiency and better load current when operated with 100µH or 120µH inductors.

Smaller inductors (22µH, 15µH and 10µH) can be used if a voltage less than 260V along with lower output current is required. If output voltage is required in the range of 100-250V with a load current of 1-2mA, then the use of 100µH and 120µH inductors is recommended.

From Figure 9 it can be seen that these lower inductors require higher operating frequencies which results in more switching loses and reduced system efficiency.

Table 1: Output voltage at different inductor values

Sr. No.	Inductor	V_{out} (V)
1	2 x 10µH	192
2	2 x 15µH	260
3	2 x 22µH	250
4	2 x 47µH	350
5	2 x 100µH	408
6	2 x 120µH	440

Chip temperature has also been analyzed during the working of chip. It is found that normally temperature stays between 40°-50°C and under any loading condition temperature never exceeds 60°C.

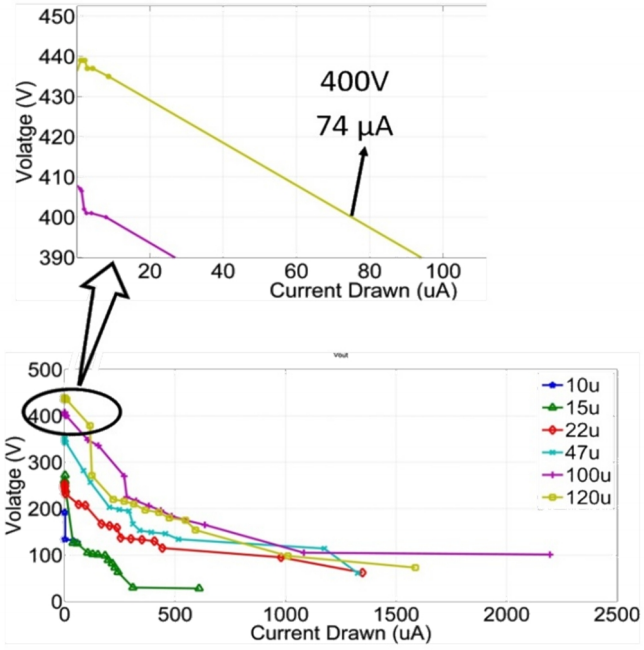

Figure 7. Output voltage Vs Load current

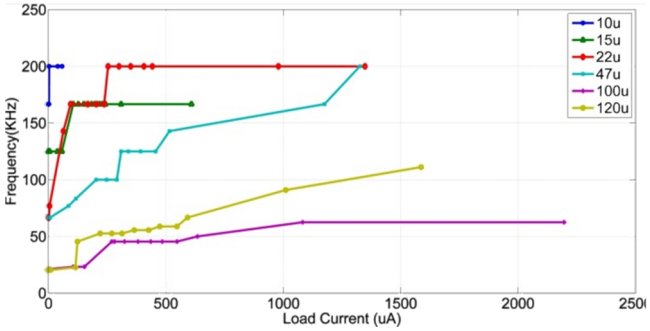

Figure 8. Frequency vs load current

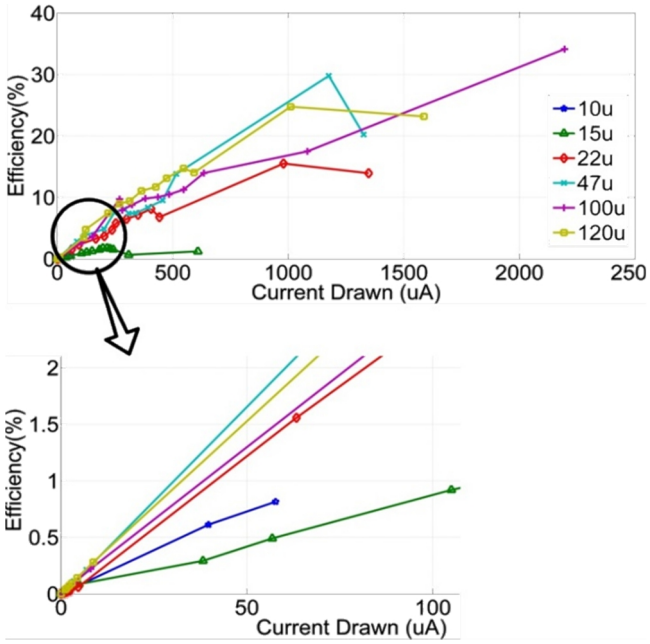

Figure 9. Efficiency Vs Load current

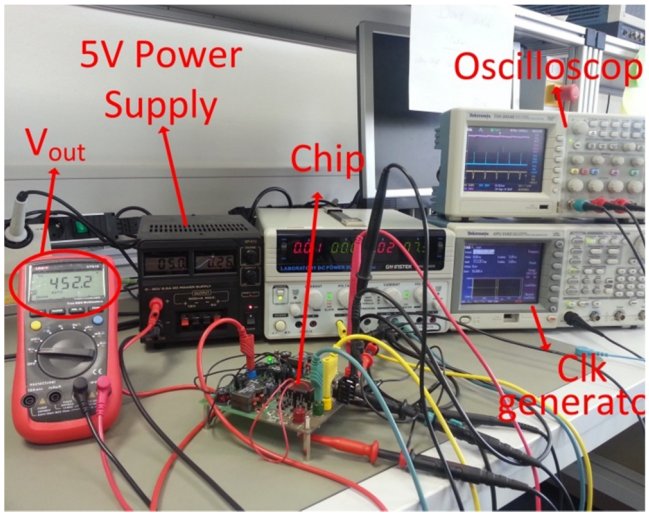

Figure 10. Test Setup

6 CONCLUSION AND FUTURE WORK

A DC-DC boost converter is presented with a novel two stage architecture. As compared to single stage design, combined inductance (L1 + L2) required by two stage boost converter is 45.8% less. In a single stage design, a single inductor has to bear the full strength of generated voltage spike whereas in two stage architecture the generated voltage spike is divided among the two inductors. This phenomenon reduces the voltage stress on inductors and improves their reliability. If an external capacitor is used with stage 1, two stable output voltages can be attained simultaneously. The presented system can operate with a number of inductors and can produce the output voltages varying from 192V-440V. Inductors can be selected according to the loading conditions.

Output characteristics of the chip are better if larger inductors are used. These inductors also allow the converter to operate on lower frequency, which in turn reduces the switching loses and improves the efficiency.

In future, authors want to further improve the efficiency.

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