Bharat Acharya Education

COA

GATE CS

2022 | Solutions

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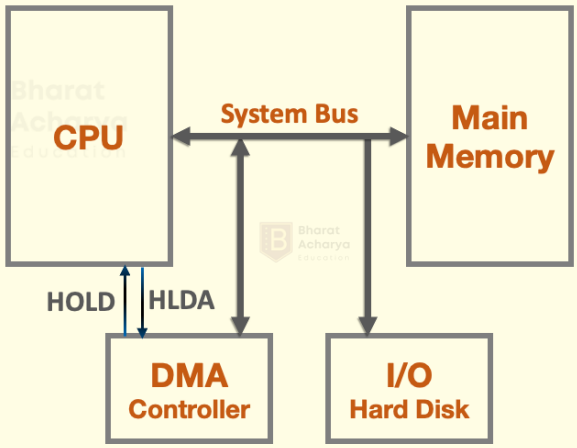
Q1 | Which one of the following facilitates transfer of bulk data from hard disk to main memory with the highest throughput?

Q17, 1m

(A) DMA based I/O transfer
(B) Interrupt driven I/O transfer
(C) Polling based I/O transfer
(D) Programmed I/O transfer

Solution

(A) DMA based I/O transfer



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Q2 | Let R1 and R2 be two 4-bit registers that store numbers in 2's complement form. For the operation R1+R2, which one of the following values of R1 and R2 gives an arithmetic overflow?

Q18, 1m

(A) R1 = 1011 and R2 = 1110
(B) R1 = 1100 and R2 = 1010
(C) R1 = 0011 and R2 = 0100
(D) R1 = 1001 and R2 = 1111

Solution

(B) R1 = 1100 and R2 = 1010

Option B

```
          0
   R1   = 1100
 + R2   = 1010
---------------
        = 0110
---------------
          1
Second Last carry = 0
       Last carry = 1

Overflow: 0 XOR 1 = 1
```


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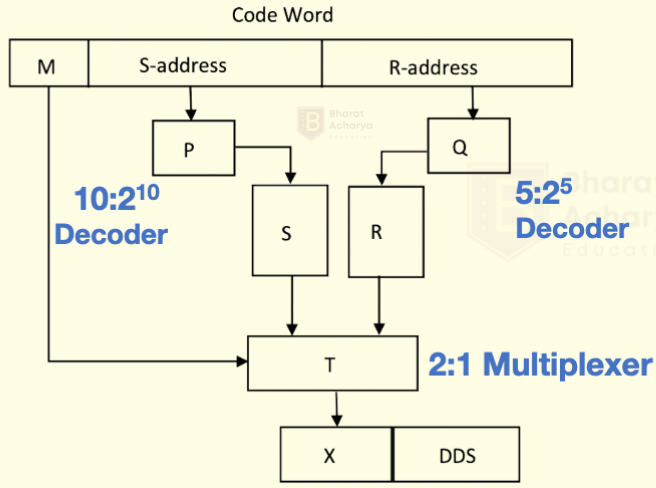
Q3 | Consider a digital display system (DDS) shown in the figure that displays the contents of register X. A 16-bit code word is used to load a word in X, either from S or from R. S is a 1024-word memory segment and R is a 32-word register file. Based on the value of mode bit M, T selects an input word to load in X. P and Q interface with the corresponding bits in the code word to choose the addressed word. Which one of the following represents the functionality of P, Q, and T?

Q40, 2m



(A) P is 10:1 multiplexer; Q is 5:1 multiplexer; T is 2:1 multiplexer

(B) P is $10:2^{10}$ decoder; Q is $5:2^5$ decoder; T is 2:1 encoder

(C) P is $10:2^{10}$ decoder; Q is $5:2^5$ decoder; T is 2:1 multiplexer

(D) P is 1:10 de-multiplexer; Q is 1:5 de-multiplexer; T is 2:1 multiplexer

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Q4 | Consider a demand paging system with four, page frames (initially empty) and LRU page replacement policy. For the following page reference string

7, 2, 7, 3, 2, 5, 3, 4, 6, 7, 7, 1, 5, 6, 1

the page fault rate, defined as the ratio of number of page faults to the number of memory accesses (rounded off to one decimal place) is = _____

Q64, 2m

Frame	7	2	7	3	2	5	3	4	6	7	7	1	5	6	1
0	7	7	7	7	7	7	7	4	4	4	4	4	5	5	5
1		2	2	2	2	2	2	2	6	6	6	6	6	6	6
2				3	3	3	3	3	3	3	3	1	1	1	1
3						5	5	5	5	7	7	7	7	7	7
			H		H		H				H			H	H

Hits = **6**

Page Faults = **9**

Total attempts = **15**

Page Fault Ratio = 9 ÷ 15 = **0.6**

Final Answer = 0.6

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Q5 | Consider three floating point numbers A, B and C stored in registers RA, RB and RC, respectively as per IEEE-754 single precision floating point format. The 32-bit content stored in these registers (in hexadecimal form) are as follows.

RA = 0xC1400000	RB = 0x42100000	RC = 0x41400000

Which one of the following is FALSE?

Q41, 2m

	S (1)	Exponent (8)	Mantissa (23)	Actual Number
A	1	100 0001 0	100 0000 ...	- 12
B	0	100 0010 0	001 0000 ...	+ 36
C	0	100 0001 0	100 0000 ...	+ 12

(A) A + C = 0 ... TRUE
(B) C = A + B ... FALSE
(C) B = 3C ... TRUE
(D) (B-C) > 0 ... TRUE

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Q6 | Let WB and WT be two set associative cache organizations that use LRU algorithm for cache block replacement. WB is a write back cache and WT is a write through cache. Which of the following statements is/are FALSE?

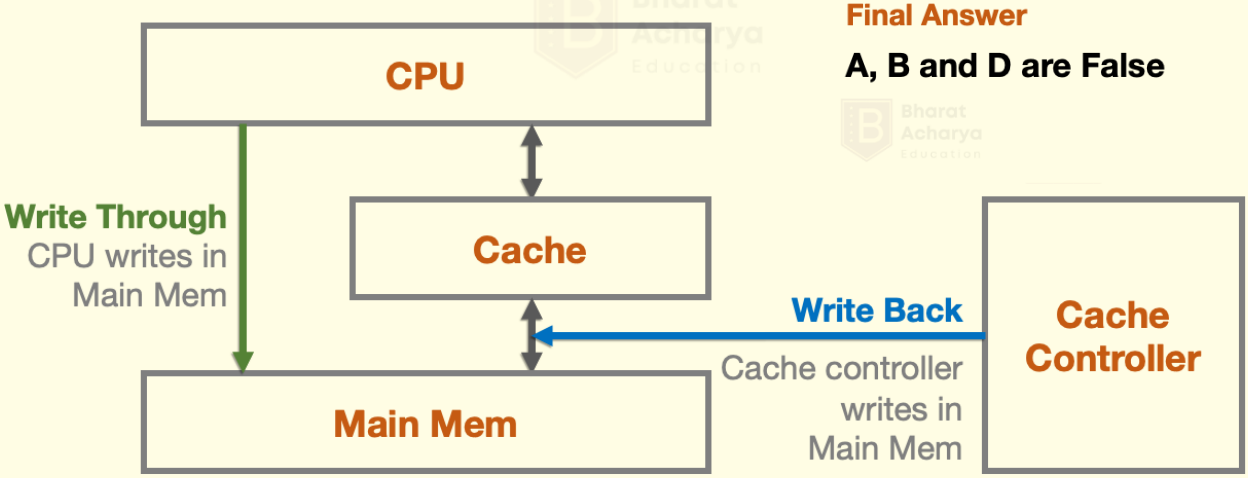
Q24, 1m

(A) Each cache block in WB and WT has a dirty bit.

(B) Every write hit in WB leads to a data transfer from cache to main mem.

(C) Eviction of a block from WT will not lead to data transfer from cache to main mem.

(D) A read miss in WB will never lead to eviction of a dirty block from WB.



Final Answer

A, B and D are False

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Q7 | Consider a system with 2 KB direct mapped data cache with a block size of 64 bytes. The system has a physical address space of 64 KB and a word length of 16 bits. During the execution of a program, four data words P, Q, R, and S are accessed in that order 10 times (i.e., PQRSPQRS....). Hence, there are 40 accesses to data cache altogether. Assume that the data cache is initially empty and no other data words are accessed by the program. The addresses of the first bytes of P, Q, R, and S are 0xA248, 0xC28A, 0xCA8A, and 0xA262, respectively. For the execution of the above program, which of the following statements is/are TRUE with respect to the data cache?

Q54, 2m

```
P  Tag:20, Block:09, Loc:08
Q  Tag:24, Block:10, Loc:04
R  Tag:25, Block:10, Loc:10
S  Tag:20, Block:09, Loc:34
```

Final Answer

A, B and D are True

(A) Every access to S is a hit

(B) Once P is brought to the cache it is never evicted

(C) At the end of the execution only R and S reside in the cache

(D) Every access to R evicts Q from the cache

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