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# | CISC vs RISC

| | RISC | CISC |
|---|---|---|
| 1 | **Instructions of a fixed size** | Instructions of **variable size** |
| 2 | Most instructions take **same time to fetch**. | Instructions have **different fetching times**. |
| 3 | Instruction set **simple and small**. | Instruction set **large and complex**. |
| 4 | **Less addressing modes** as most operations are register based. | **Complex addressing modes** as most operations are memory based. |
| 5 | **Compiler design is simple** | **Compiler design is complex** |
| 6 | **Total size of program is large** as many instructions are required to perform a task as instructions are simple. | **Total size of program is small** as few instructions are required to perform a task as instructions are complex & more powerful. |
| 7 | Instructions use a **fixed number of operands.** | Instructions have **variable** number of operands. |
| 8 | Ideal for processors performing a **dedicated operation**. | Ideal for processors performing a **verity of operations**. |
| 9 | Since instructions are simple, they can be decoded by a **hardwired control unit**. | Since instructions are complex, they require a **Micro-programmed Control Unit**. |
| 10 | Execution speed is **faster** as most operations are register based. | Execution speed is **slower** as most operations are memory based. |
| 11 | As No. of cycles per instruction is fixed, it gives a **better degree of pipelining** | Since number of cycles per instruction varies, **pipelining has more bubbles** or stalls. |
| 12 | E.g.:: **ARM7**, **PIC 18** Microcontrollers. | E.g.: Intel **8085, 8086** Microprocessors. |

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**Special Note:**

If you are learning this by piracy, then you are not my student.
You are simply a thief! #PoorUpbringing

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