COA

MCQ - 2021

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Section 1

Introduction to Computer Organization & Number Systems

Q1) PC contains _____

(a) The next instruction

(b) Opcode of the next instruction

(c) Operand of the next instruction

(d) Address of the next instruction

Answer…

(a) The next instruction

(b) Opcode of the next instruction

(c) Operand of the next instruction

(d) Address of the next instruction

Video Reference: COA | **Introduction**

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Q2) Primary Memory consists of ____

(a) Only RAM

(b) RAM and ROM

(c) Hard Disc, CD/ DVD

(d) All of the above

Answer…

(a) Only RAM

(b) RAM and ROM

(c) Hard Disc, CD/ DVD

(d) All of the above

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Q3) SP contains ____

(a) The Stack

(b) The Top of Stack

(c) Address of the Top of Stack

(d) Address of next instruction

Answer…

(a) The Stack

(b) The Top of Stack

(c) Address of the Top of Stack

(d) Address of next instruction

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Q4) ROM is used to store ____

(a) The BIOS

(b) The Operating System

(c) Antivirus Software

(d) All passwords

Answer…

(a) The BIOS

(b) The Operating System

(c) Antivirus Software

(d) All passwords

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Q5) Instructions are decoded by the ____

(a) ALU

(b) Control Unit

(c) RAM

(d) Status Register

Answer…

(a) ALU

(b) Control Unit

(c) RAM

(d) Status Register

Video Reference: COA | **Introduction**

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Q6) +25d in binary is

(a) 11001

(b) 011001

(c) 0010 0101

(d) 010001

Answer...

(a) 11001

(b) 011001

(c) 0010 0101

(d) 010001

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Q7) What is the range of an 8-bit signed number?

(a) 0…255

(b) -127…+128

(c) -128….+128

(d) -128…+127

Answer…

(a) 0…255

(b) -127…+128

(c) -128….+128

(d) -128…+127

Video Reference: COA | **Number Representation**

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Q8) -25d in binary is

(a) 100111

(b) 111001

(c) 1010 0101

(d) 110001

Answer…

(a) 100111

(b) 111001

(c) 1010 0101

(d) 110001

Important Type

Video Reference: COA | **Number Representation**

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Q9) Negative numbers are stored in ____

(a) Sign Magnitude form

(b) 1's Complement form

(c) 2's Complement form

(d) ASCII form

Answer…

(a) Sign Magnitude form

(b) 1's Complement form

(c) 2's Complement form

(d) ASCII form

Video Reference: COA | **Number Representation**

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Q10) 2's Complement is preferred because ___

(a) It is fast

(b) It is cheap

(c) It is simple

(d) It doesn't give -0

Answer…

(a) It is fast

(b) It is cheap

(c) It is simple

(d) It doesn't give -0

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Video Reference: COA | **Number Representation**

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Q) Should you learn by cheating / piracy?

(a) Yes, I am raised like this!
(b) Who cares about the teacher's effort? I am cheap!
(c) Education by cheating will still help me!
(d) NO. We should support good teachers who work so hard yet charge very less!

Answer…

I leave this answer to YOU!

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Section 2

The ALU

Q11) Full Adder is better than Half adder as ____

(a) It adds twice

(b) It includes carry input

(c) It uses less gates

(d) It is cheaper

Answer…

(a) It adds twice

(b) It includes carry input

(c) It uses less gates

(d) It is cheaper

Video Reference: COA | **Adder Circuits**

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Q12) In a full adder, the inputs are xi, yi, cin. The output SUM (zi) is ____

(a) xi.yi

(b) xi.yi.cin

(c) $xi.\overline{Yi}.\overline{Cin} + .\overline{Xi}.yi.\overline{Cin} + \overline{Xi}.\overline{Yi}.cin$

(d) $xi.yi.cin + xi.\overline{Yi}.\overline{Cin} + .\overline{Xi}.yi.\overline{Cin} + \overline{Xi}.\overline{Yi}.cin$

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Answer…

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(a) xi.yi

(b) xi.yi.cin

(c) $xi.\overline{Yi}.\overline{Cin} + .\overline{Xi}.yi.\overline{Cin} + \overline{Xi}.\overline{Yi}.cin$

(d) $xi.yi.cin + xi.\overline{Yi}.\overline{Cin} + .\overline{Xi}.yi.\overline{Cin} + \overline{Xi}.\overline{Yi}.cin$

Video Reference: COA | **Adder Circuits**

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Q13) In a full adder, the inputs are xi, yi, cin. The output Carry (Cout) is ____

(a) xi.yi + xi.cin + yi.cin

(b) xi.cin + yi.cin

(c) xi.yi + yi.cin

(d) cin + xi.cin + yi.cin

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Answer...

(a) xi.yi + xi.cin + yi.cin

Important Type

(b) xi.cin + yi.cin

(c) xi.yi + yi.cin

(d) cin + xi.cin + yi.cin

Video Reference: COA | **Adder Circuits**

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Q14) Subtraction is done by ____

(a) Adding 1's complement

(b) Adding 2's complement

(c) Subtracting 1's complement

(d) Subtracting 2's complement

Answer…

(a) Adding 1's complement

(b) Adding 2's complement

(c) Subtracting 1's complement

(d) Subtracting 2's complement

Video Reference: COA | **Adder Circuits**

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Q15) Carry look ahead adder is _____ and _____ compared to Ripple Carry adder

(a) Simple and Slow

(b) Simple and Fast

(c) Complex and Slow

(d) Complex and Fast

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Important Type

Answer…

(a) Simple and Slow

(b) Simple and Fast

(c) Complex and Slow

(d) Complex and Fast

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Q16) In Booth's Algorithm, for 0 to 0 or 1 to 1 we simply ____

(a) Right Shift

(b) Add and Left shift

(c) Do nothing

(d) Left shift

Answer…

(a) Right Shift

(b) Add and Left shift

(c) Do nothing

(d) Left shift

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Video Reference: COA | **Adder Circuits**

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Q17) Multiplication of 4-bit numbers yields maximum ____ bit result

(a) 4

(b) 5

(c) 8

(d) 9

Answer…

(a) 4

(b) 5

(c) 8

(d) 9

Video Reference: COA | **Booth's Algorithm**

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Q18) IEEE 754 32-bit Single precision format has the following bit distribution…

(a) S (1), E (7), M (24)

(b) S (1), E (9), M (22)

(c) S (1), M (31)

(d) S (1), E (8), M (23)

Answer…

(a) S (1), E (7), M (24)

(b) S (1), E (9), M (22)

(c) S (1), M (31)

(d) S (1), E (8), M (23)

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Important Type

Video Reference: COA | **FP Number Representation**

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Q19) IEEE 754 64-bit Double precision format has the following bit distribution…

(a) S (1), E (10), M (53)

(b) S (1), E (11), M (52)

(c) S (1), E (12), M (51)

(d) S (1), E (15), M (48)

Answer…

(a) S (1), E (10), M (53)

(b) S (1), E (11), M (52)

(c) S (1), E (12), M (51)

(d) S (1), E (15), M (48)

Video Reference: COA | **FP Number Representation**

www.BharatAcharyaEducation.com

Q20) IEEE 754 32-bit Single precision bias value?

(a) There is no biassing

(b) 129

(c) 128

(d) 127

Answer…

(a) There is no biassing

(b) 129

(c) 128

(d) 127

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Important Type

Video Reference: COA | **FP Number Representation**

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Q21) IEEE 754 64-bit Double precision bias value?

(a) 1023

(b) 1024

(c) 1025

(d) There is no biassing

Answer…

(a) 1023

(b) 1024

(c) 1025

(d) There is no biassing

Video Reference: COA | **FP Number Representation**

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Q22) What is overflow condition in floating point numbers?

(a) Exponent is too large to be stored

(b) Mantissa is too large to be stored

(c) Mantissa is too small to be stored

(d) When there is a carry

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Important Type

Answer…

(a) Exponent is too large to be stored

(b) Mantissa is too large to be stored

(c) Mantissa is too small to be stored

(d) When there is a carry

Video Reference: COA | **FP Number Representation**

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Q23) Infinity is indicated in FP system as ____ ?

(a) Exponent all 0s, Mantissa all 0s

(b) Exponent all 0s, Mantissa all 1s

(c) Exponent all 1s, Mantissa all 0s

(d) Exponent all 1s, Mantissa all 1s

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Answer…

(a) Exponent all 0s, Mantissa all 0s

(b) Exponent all 0s, Mantissa all 1s

(c) Exponent all 1s, Mantissa all 0s

(d) Exponent all 1s, Mantissa all 1s

Video Reference: COA | **FP Number Representation**

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Q24) Zero is indicated in FP system as ____ ?

(a) Exponent all 0s, Mantissa all 0s

(b) Exponent all 0s, Mantissa all 1s

(c) Exponent all 1s, Mantissa all 0s

(d) Exponent all 1s, Mantissa all 1s

Answer…

(a) Exponent all 0s, Mantissa all 0s

(b) Exponent all 0s, Mantissa all 1s

(c) Exponent all 1s, Mantissa all 0s

(d) Exponent all 1s, Mantissa all 1s

Video Reference: COA | **FP Number Representation**

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Q25) Which of the following is normalized number?

(a) 00.0101

(b) 0.0101

(c) 10.0101

(d) 1.01001

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Answer…

(a) 00.0101

(b) 0.0101

(c) 10.0101

(d) 1.01001

Video Reference: COA | **FP Number Representation**

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Q) We cheat and learn by piracy because…

(a) We are cheap

(b) We are educated thieves

(c) We were raised with low morals

(d) We love to backstab our teacher!

Answer…

All of the above

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Section 3

Instructions and Control Unit

Q26) Which is not a pipelining hazard?

(a) Branching

(b) Data Dependency

(c) Structural Hazard

(d) Overheating

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Important Type

Answer…

(a) Branching

(b) Data Dependency

(c) Structural Hazard

(d) Overheating

Video Reference: COA | **Pipelining**

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Q27) Pipelining increases _____?

(a) Accuracy

(b) Durability

(c) Performance

(d) Reliability

Answer…

(a) Accuracy

(b) Durability

(c) Performance

(d) Reliability

Video Reference: COA | **Pipelining**

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Q28) Immediate addressing mode means

(a) Data is given in the instruction

(b) Address is given in the instruction

(c) Data is given in registers

(d) Address is given using a register

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Important Type

Answer…

(a) Data is given in the instruction

(b) Address is given in the instruction

(c) Data is given in registers

(d) Address is given using a register

Video Reference: COA | **Addressing Modes**

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Q29) ADD BL, CL is an example of

(a) Immediate Addressing mode

(b) Register Addressing mode

(c) Direct Addressing mode

(d) Indirect Addressing mode

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Important Type

Answer…

(a) Immediate Addressing mode

(b) Register Addressing mode

(c) Direct Addressing mode

(d) Indirect Addressing mode

Video Reference: COA | **Addressing Modes**

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Q30) In which addressing mode we give the address of the operand?

(a) Immediate Addressing mode

(b) Register Addressing mode

(c) Direct Addressing mode

(d) Indirect Addressing mode

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Important Type

Answer…

(a) Immediate Addressing mode

(b) Register Addressing mode

(c) Direct Addressing mode

(d) Indirect Addressing mode

Video Reference: COA | **Addressing Modes**

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Q31) Indirect addressing mode is used when we want to…

(a) Not disclose the address

(b) Access a series of locations

(c) Access the odd bank

(d) Indirectly end the program

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Important Type

Answer…

(a) Not disclose the address

(b) Access a series of locations

(c) Access the odd bank

(d) Indirectly end the program

Video Reference: COA | **Addressing Modes**

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Q32) Consider the following 8085 instruction… LDA 200H. Here A gets data from location 2000H. This is ____ addressing mode?

(a) Immediate

(b) Register

(c) Direct

(d) Indirect

Answer…

(a) Immediate

(b) Register

(c) Direct

(d) Indirect

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Important Type

Video Reference: COA | **Addressing Modes**

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Q33) Consider the following 8086 instruction… MOV CL, [BX]. Here CL gets data from a memory location pointed by BX register. This is ____ addressing mode?

(a) Immediate

(b) Register

(c) Direct

(d) Indirect

Answer…

(a) Immediate

(b) Register

(c) Direct

(d) Indirect

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Important Type

Video Reference: COA | **Addressing Modes**

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Q34) Branch Prediction avoids _____

(a) Flushing of pipelines
(b) Overheating of CPU
(c) Data Dependency
(d) Shared data problems

Answer…

(a) Flushing of pipelines
(b) Overheating of CPU
(c) Data Dependency
(d) Shared data problems

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Video Reference: COA | **Pipelining**

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Q35) Micro-operations for fetching are…

(a) PC←PC+1, MAR←PC, MBR←Mem, IR←MBR

(b) MAR←PC, MBR←Mem, IR←MBR, PC←PC+1

(c) MBR←Mem, MAR←PC, IR←MBR, PC←PC+1

(d) MAR←PC, IR←MBR, MBR←Mem, PC←PC+1

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Answer…

(a) PC←PC+1, MAR←PC, MBR←Mem, IR←MBR

(b) MAR←PC, MBR←Mem, IR←MBR, PC←PC+1

(c) MBR←Mem, MAR←PC, IR←MBR, PC←PC+1

(d) MAR←PC, IR←MBR, MBR←Mem, PC←PC+1

Video Reference: COA | **Micro-operations**

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Q36) 1 T-state is _____

(a) 1 clock cycle

(b) 1 machine cycle

(c) 1 instruction cycle

(d) 1 bus cycle

Answer…

(a) 1 clock cycle

(b) 1 machine cycle

(c) 1 instruction cycle

(d) 1 bus cycle

Video Reference: COA | **Micro-operations**

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Q37) 1 Micro-operation requires ____

(a) 1 machine cycle

(b) 2 machine cycles

(c) 1 Clock cycle

(d) 2 Clock cycles

Answer…

(a) 1 machine cycle

(b) 2 machine cycles

(c) 1 Clock cycle

(d) 2 Clock cycles

Video Reference: COA | **Micro-operations**

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Q38) Hardwired control units are ____ and ____ compared to microprogrammed control units?

(a) Flexible and Faster

(b) Flexible and Slower

(c) Rigid and Slower

(d) Rigid and Faster

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Important Type

Answer…

(a) Flexible and Faster

(b) Flexible and Slower

(c) Rigid and Slower

(d) Rigid and Faster

Video Reference: COA | **Hardwired Control Units**

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Q39) Which of the following is NOT a Hardwired CU method?

(a) State Table Method

(b) Delay Element Method

(c) Sequence Counter Method

(d) Wilke's Design

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Important Type

Answer…

(a) State Table Method

(b) Delay Element Method

(c) Sequence Counter Method

(d) Wilke's Design

Video Reference: COA | **Hardwired Control Units**

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Q40) Microinstructions are stored in ____?

(a) Main Memory
(b) Cache Memory
(c) Control Memory
(d) Secondary Memory

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Important Type

Answer…

(a) Main Memory
(b) Cache Memory
(c) Control Memory
(d) Secondary Memory

Video Reference: COA | **Microprogrammed Control Units**

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Q41) In Wilke's Design, Microinstructions had a ____ filed and a ____ field?

(a) Address and Data

(b) Control and Address

(c) Data and Control

(d) Horizontal and Vertical

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Important Type

Answer…

(a) Address and Data

(b) Control and Address

(c) Data and Control

(d) Horizontal and Vertical

Video Reference: COA | **Microprogrammed Control Units**

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Q42) Horizontal Microinstructions are ____ and _____ compared to Vertical?

(a) Wider and Faster
(b) Narrow and Faster
(c) Wider and Slower
(d) Narrow and Slower

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Important Type

Answer…

(a) Wider and Faster
(b) Narrow and Faster
(c) Wider and Slower
(d) Narrow and Slower

Video Reference: COA | **Microprogrammed Control Units**
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Q43) Emulation is a strong advantage of _____?

(a) Hardwired Control Units

(b) Microprogrammed Control Units

(c) Pipelined control units

(d) Non-Pipelined control units

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Important Type

Answer…

(a) Hardwired Control Units

(b) Microprogrammed Control Units

(c) Pipelined control units

(d) Non-Pipelined control units

Video Reference: COA | **Microprogrammed Control Units**

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Q44) Multiple control signals can be simultaneously generated in ____?

(a) Horizontal Microinstructions

(b) Vertical Microinstructions

(c) Both of them

(d) None of them

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Important Type

Answer…

(a) Horizontal Microinstructions

(b) Vertical Microinstructions

(c) Both of them

(d) None of them

Video Reference: COA | **Microprogrammed Control Units**

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Q45) RISC processors have

(a) Better pipelining

(b) More registers

(c) Fewer addressing modes

(d) All of the above

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Important Type

Answer…

(a) Better pipelining

(b) More registers

(c) Fewer addressing modes

(d) All of the above

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Section 4

Memory Section

Q46) _____ is the fastest memory

(a) Dynamic RAM

(b) Static RAM

(c) Hard Disc

(d) DVD

Answer…

(a) Dynamic RAM

(b) Static RAM

(c) Hard Disc

(d) DVD

Video Reference: COA | **Memory Hierarchy**

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Q47) RAM and ROM are _____ type of memory

(a) Optical

(b) Magnetic

(c) Semiconductor

(d) Quantum

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Important Type

Answer…

(a) Optical

(b) Magnetic

(c) Semiconductor

(d) Quantum

Video Reference: COA | **Memory Hierarchy**

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Q48) Hard disk is _____ type of memory

(a) Optical

(b) Magnetic

(c) Semiconductor

(d) Quantum

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Answer…

(a) Optical

(b) Magnetic

(c) Semiconductor

(d) Quantum

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Q49) Floppy disk is _____ type of memory

(a) Optical

(b) Magnetic

(c) Semiconductor

(d) Quantum

Answer…

(a) Optical

(b) Magnetic

(c) Semiconductor

(d) Quantum

Video Reference: COA | **Memory Hierarchy**

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Q50) CD/DVD are _____ type of memory

(a) Optical

(b) Magnetic

(c) Semiconductor

(d) Quantum

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Answer…

(a) Optical

(b) Magnetic

(c) Semiconductor

(d) Quantum

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Q51) Blu Ray discs are _____ type of memory

(a) Optical
(b) Magnetic
(c) Semiconductor
(d) Quantum

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Important Type

Answer…

(a) Optical
(b) Magnetic
(c) Semiconductor
(d) Quantum

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Q52) Pen drives are _____ type of memory

(a) RAM

(b) ROM

(c) FLASH RAM

(d) FLASH ROM

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Important Type

Answer…

(a) RAM

(b) ROM

(c) FLASH RAM

(d) FLASH ROM

Video Reference: COA | **Memory Hierarchy**

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Q53) The operating system in your computer is stored in _____

(a) RAM
(b) ROM
(c) BIOS
(d) Hard Disc

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Important Type

Answer…

(a) RAM
(b) ROM
(c) BIOS
(d) Hard Disc

Video Reference: COA | **Memory Hierarchy**

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Q54) Split cache means the cache is divided to contain _____ and _____

(a) Address and Data

(b) Code and Data

(c) Codes and Addresses

(d) Data and Register files

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Important Type

Answer…

(a) Address and Data

(b) Code and Data

(c) Codes and Addresses

(d) Data and Register files

Video Reference: COA | **Memory Hierarchy**

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Q55) SRAM is faster than DRAM because ____

(a) Capacitors take time to charge

(b) Capacitors are faster than flipflops

(c) Flipflops have race around

(d) Registers are smaller

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Important Type

Answer…

(a) Capacitors take time to charge

(b) Capacitors are faster than flipflops

(c) Flipflops have race around

(d) Registers are smaller

Video Reference: COA | **Memory Hierarchy**

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Q56) Which is an invalid type of ROM

(a) PROM

(b) EPROM

(c) FLASH ROM

(d) DDR4

Answer…

(a) PROM

(b) EPROM

(c) FLASH ROM

(d) DDR4

Video Reference: COA | **Memory Hierarchy**

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Q57) Dirty page means ____

(a) Contains illicit data

(b) It is modified in Main Memory

(c) It is modified in Secondary Memory

(d) It always gives Page Fault

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Important Type

Answer…

(a) Contains illicit data

(b) It is modified in Main Memory

(c) It is modified in Secondary Memory

(d) It always gives Page Fault

Video Reference: COA | **Paging**

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Q58) Page Table is present in _____

(a) CPU

(b) Main Memory

(c) Secondary Memory

(d) Page Directory

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Important Type

Answer…

(a) CPU

(b) Main Memory

(c) Secondary Memory

(d) Page Directory

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Q59) TLB is present in _____

(a) CPU

(b) Main Memory

(c) Secondary Memory

(d) Page Directory

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Important Type

Answer…

(a) CPU

(b) Main Memory

(c) Secondary Memory

(d) Page Directory

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Q60) Page Fault means ___

(a) Required page absent in Virtual Mem

(b) Required page absent in Physical Mem

(c) Required page absent in Cache Mem

(d) Required page absent in Entire computer

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Important Type

Answer…

(a) Required page absent in Virtual Mem

(b) Required page absent in Physical Mem

(c) Required page absent in Cache Mem

(d) Required page absent in Entire computer

Video Reference: COA | **Paging**

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Q61) ___ is not a Page Replacement policy

(a) FIFO

(b) LRU

(c) LFU

(d) Best Fit

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Important Type

Answer…

(a) FIFO

(b) LRU

(c) LFU

(d) Best Fit

Video Reference: COA | **Paging**

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Q62) Hit Ratio = _____

(a) Number of hits / number of misses

(b) Number of hits / number of hits + misses

(c) Number of misses / number of hits

(d) Number of hits / no of pages

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Important Type

Answer…

(a) Number of hits / number of misses

(b) Number of hits / number of hits + misses

(c) Number of misses / number of hits

(d) Number of hits / no of pages

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Q63) Segments are of _____ size and pages are of _____ size

(a) Variable, Variable

(b) Variable, Fixed

(c) Fixed, Variable

(d) Fixed, Fixed

Answer…

(a) Variable, Variable

(b) Variable, Fixed

(c) Fixed, Variable

(d) Fixed, Fixed

Video Reference: COA | **Paging**

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Q64) Thrashing means ____

(a) Few page-faults

(b) Too many page-faults

(c) Too many dirty pages

(d) TLB is corrupt

Answer…

(a) Few page-faults

(b) Too many page-faults

(c) Too many dirty pages

(d) TLB is corrupt

Video Reference: COA | **Paging**

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Q65) Cache memory is made up of ____

(a) SRAM

(b) DRAM

(c) SD RAM

(d) SSDRAM

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Important Type

Answer…

(a) SRAM

(b) DRAM

(c) SD RAM

(d) SSDRAM

Video Reference: COA | **Cache Memory**

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Q66) L1 Cache is present ____

(a) Inside the processor

(b) Inside the L2 cache

(c) Inside the Main Memory

(d) Inside the BIOS ROM

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Important Type

Answer…

(a) Inside the processor

(b) Inside the L2 cache

(c) Inside the Main Memory

(d) Inside the BIOS ROM

Video Reference: COA | **Cache Memory**

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Q67) MESI stands for

(a) Memory Exclusive System Information

(b) Memory Exclusive System Installation

(c) Modified Exclusive Shared Invalid

(d) GOAT

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Answer…

(a) Memory Exclusive System Information

(b) Memory Exclusive System Installation

(c) Modified Exclusive Shared Invalid

(d) GOAT

Video Reference: COA | **Cache Memory**

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Q68) Which is not a cache mapping technique?

(a) Associative

(b) Direct

(c) Set Associative

(d) Interleaving

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Important Type

Answer…

(a) Associative

(b) Direct

(c) Set Associative

(d) Interleaving

Video Reference: COA | **Cache Mapping**

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Q69) Which technique has consecutive locations in different chips?

(a) Higher order interleaving

(b) Lower order interleaving

(c) Both of them

(d) None of them

Answer…

(a) Higher order interleaving

(b) Lower order interleaving

(c) Both of them

(d) None of them

Video Reference: COA | **Memory Interleaving**

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Q70) In Set associative mapping, the main memory address is divided into?

(a) Block No | Set No | Location

(b) Location | Set No | Block No

(c) Set No | Block No | Location

(d) Set No | Block No | Page No

Answer…

(a) Block No | Set No | Location

(b) Location | Set No | Block No

(c) Set No | Block No | Location

(d) Set No | Block No | Page No

Video Reference: COA | **Cache Mapping**

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Q71) Lower order interleaving is done to ____?

(a) Increase size of memory

(b) Increase speed by accessing more data/cycle

(c) Increase reliability of memory

(d) Increase Hit Ratio

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Important Type

Answer…

(a) Increase size of memory

(b) Increase speed by accessing more data/cycle

(c) Increase reliability of memory

(d) Increase Hit Ratio

Video Reference: COA | **Cache Mapping**

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Q72) (4K x 8) means…

(a) 8 chips of 4B
(b) 4KB
(c) 32KB
(d) Wrong notation

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Important Type

Answer…

(a) 8 chips of 4B
(b) 4KB
(c) 32KB
(d) Wrong notation

Video Reference: COA | **Memory Hierarchy**

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Section 5

Input / Output Section

Q73) Compared to serial communication, parallel communication is _____ and _____

(a) Slower and Cheaper
(b) Faster and Cheaper
(c) Slower and Costlier
(d) Faster and Costlier

Answer…

(a) Slower and Cheaper
(b) Faster and Cheaper
(c) Slower and Costlier
(d) Faster and Costlier

Video Reference: COA | **Introduction**
www.BharatAcharyaEducation.com

Q74) Which is not an I/O data transfer scheme?

(a) Programmed I/O
(b) Interrupt driven I/O
(c) Daisy Chaining
(d) DMA

Answer…

(a) Programmed I/O
(b) Interrupt driven I/O
(c) Daisy Chaining
(d) DMA

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Important Type

Video Reference: COA | **Introduction**

www.BharatAcharyaEducation.com

Q75) Which is not a Bus Arbitration scheme?

(a) Daisy Chaining
(b) Polling
(c) Independent Request
(d) Interleaving

Answer…

(a) Daisy Chaining
(b) Polling
(c) Independent Request
(d) Interleaving

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Important Type

Video Reference: COA | **Bus Contention**

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Q76) Vectored Interrupt means?

(a) ISR address is variable
(b) ISR address is fixed
(c) Interrupt cannot be disabled
(d) Interrupt can be disabled

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Important Type

Answer...

(a) ISR address is variable
(b) ISR address is fixed
(c) Interrupt cannot be disabled
(d) Interrupt can be disabled

Video Reference: COA | **Interrupts**

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Q77) DMA means transferring data directly between ____ and _____?

(a) Memory and I/O
(b) Memory and CPU
(c) Memory and Cache
(d) Memory and I/O Processor

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Important Type

Answer…

(a) Memory and I/O
(b) Memory and CPU
(c) Memory and Cache
(d) Memory and I/O Processor

Video Reference: COA | **Interrupts**

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Useful Links...

My Recommended
Reference books
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8085 Microprocessor | Ramesh Gaonkar
Link: https://amzn.to/2VtJTOz

8086 Microprocessor | Douglas Hall
Link: https://amzn.to/3lyFOTC

8086 Microprocessor | Liu Gibson
Link: https://amzn.to/36yFCzG

8086 Microprocessor | Barry Brey
Link: https://amzn.to/37czFc3

8086 Microprocessor | Kenneth Ayala
Link: https://amzn.to/33DJAFn

8051 Microcontroller | Bharat Acharya
Link: https://amzn.to/3obYQRs

8051 Microcontroller | Mazidi
Link: https://amzn.to/3lyKxVA

COA | William Stallings
Link: https://amzn.to/33CuQXb

COA | John Hayes
Link: https://amzn.to/2VujTlV

COA | Tanenbaum
Link: https://amzn.to/3mM8MRe

Raspberry Pi Book | Raspberry Pi Made Easy
Link: https://amzn.to/3acdDIl

Raspberry Pi Board | Pi3-MODB-1GB Motherboard
Link: https://amzn.to/3m9xzO5

Arduino Book | 26 Basic Arduino Projects
Link: https://amzn.to/3mgep9r

Arduino Board | T9-NHXR-186H Uno R3
Link: https://amzn.to/344cnCU

English Speaking Book | Effortless English
Link: https://amzn.to/3gFCVzH

English Speaking Book | How to Talk to Anyone
Link: https://amzn.to/349cugB

Personality Development | The Art of Public Speaking
Link: https://amzn.to/3aj0xsT

Aptitude Test | RS Aggarwal
Link: https://amzn.to/2Waq4vO

Motivational book | The 7 Habits of Highly Effective People
Link: https://amzn.to/3ngomou

Motivational book | Think and Grow Rich
Link: https://amzn.to/3a9jNbY

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