CORE-V MCU Verification Plan

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Test Bench Architecture

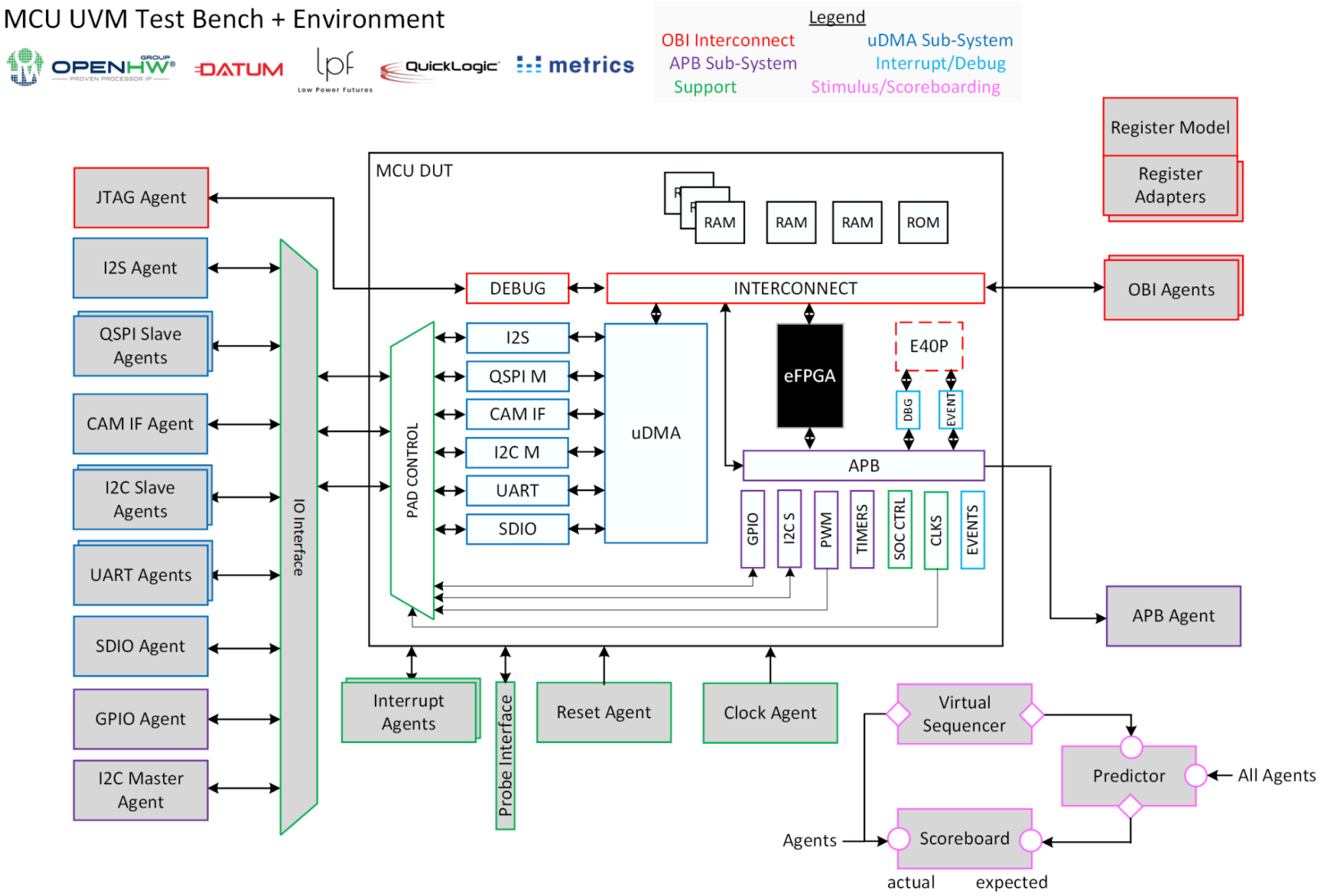
Top-Level - uvmt_cvmcu + uvme_cvmcu

Salient Points

- Some required UVM Agents and Libraries are property of Datum Technology Corporation and a license for each is required to simulate.
- All UVM Environments, Agents and Tests extend Datum UVMx classes, not UVM directly. As such, a license for UVMx from Datum is required to simulate.
- RISC-V Core RTL is not used in most tests. Wherever ‘core’ is mentioned in Verification Points, it is implied to mean a pair of OBI Agents acting as a mock RISC-V core:
    - OBI Instructions
    - OBI Data

Block Diagram

MCU UVM Test Bench + Environment



Verification Points

Memories

#	Test	Description
1	mem_walk	Ensure all ROM locations are readable from the core.
2	mem_walk	Ensure all Non-Interleaved SRAM locations are readable/writeable from the core.
3	mem_walk	Ensure all Interleaved SRAM locations are readable/writeable from the core.

uDMA

#	Test	Description
1	reg_hw_reset, reg_bit_bash	Ensure all top-level uDMA Registers are accessible from the core.

uDMA Peripherals

UARTs

#	Test	Description
1	reg_hw_reset, reg_bit_bash	Ensure all 2x UARTs Registers are accessible from the core.
2	udma_uart_eg	Ensure that both UARTs operate as defined in standard for data transfers from the core to agents in the test bench.
3	udma_uart_ig	Ensure that both UARTs operate as defined in standard for data transfers from the agents in the test bench to the core.

APB Peripherals

Event Timers

#	Test	Description
1	reg_hw_reset, reg_bit_bash	Ensure all Event Timers Registers are accessible from the core.

Advanced Timers (PWM)

#	Test	Description
1	reg_hw_reset, reg_bit_bash	Ensure all Advance Timers Registers are accessible from the core.

FLL (Clock & Reset Control)

#	Test	Description
1	reg_hw_reset, reg_bit_bash	Ensure all FLL Registers are accessible from the core.

GPIO

#	Test	Description
1	reg_hw_reset, reg_bit_bash	Ensure all GPIO Registers are accessible from the core.

SoC Control

#	Test	Description
1	reg_hw_reset, reg_bit_bash	Ensure all SoC Control Registers are accessible from the core.