

# Computer Architecture (ECS 154A) Study Guide

Davis Computer Science Club — Tutoring Committee

Winter Quarter 2015

- 1 Logical Expressions
  - 1.1 Operations
  - 1.2 Truth Table
  - 1.3 Boolean Algebra
  - 1.4 Equivalence Laws
  - 1.5 Karnaugh Maps
- 2 Combinational Logic Circuits
  - 2.1 Gates
  - 2.2 Timing Diagrams
  - 2.3 Multiplexers, Decoders, Shifters
  - 2.4 Adders and Subtractors
  - 2.5 Designing Combinational Logic Circuits
- 3 Finite State Automata
  - 3.1 Moore Model
  - 3.2 Mealy Model
- 4 Sequential Logic Circuit
  - 4.1 Latches
  - 4.2 Flip Flops
  - 4.3 Registers and Counters
  - 4.4 Designing Sequential Logic Circuits
- 5 Single Cycle CPU Design
- 6 Cache
- 7 Virtual Memory
- 8 Multi-Cycle CPU Design
- 9 Pipeline CPU Design