

#W8.2 Schematic

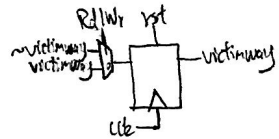
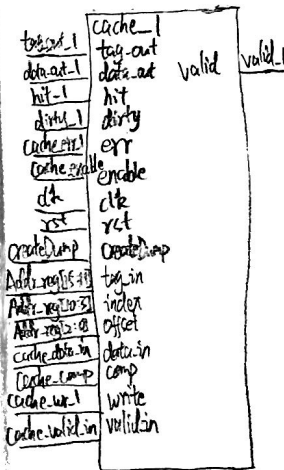
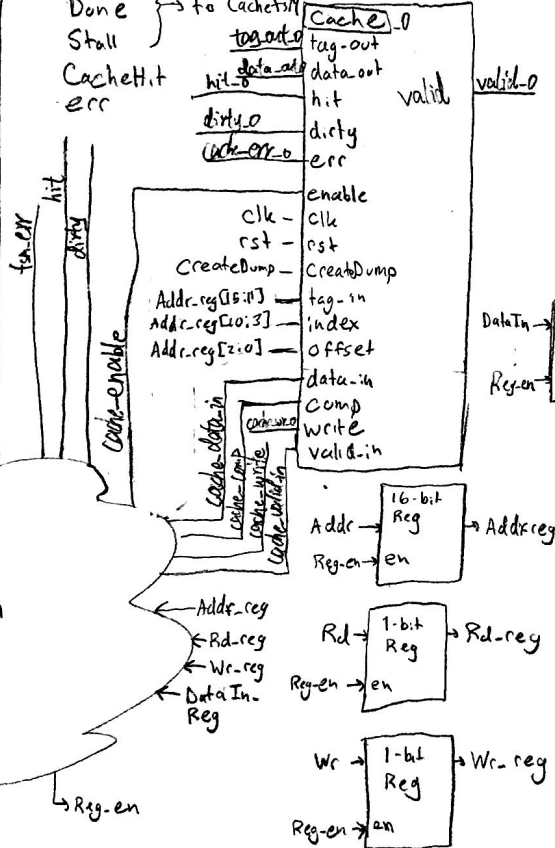
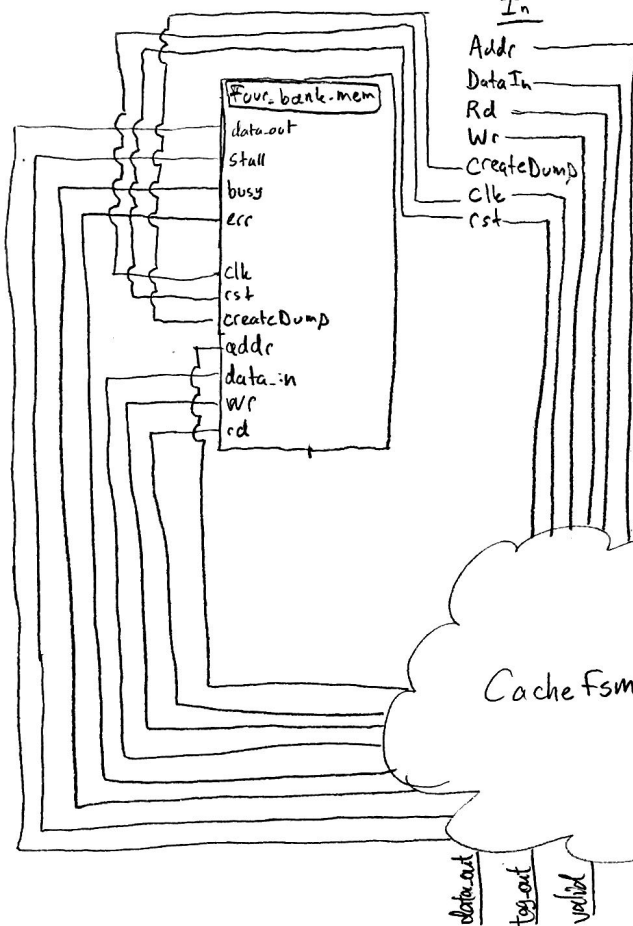
Mem-system Module

assign err = (Addr.reg[5] == 1) | fsm_err | cache_err_0 | cache_err_1

assign hit = (tag.in == tag.out_0) ? hit_0 : hit_1;
assign valid = (state == check_hit) ?

((tag.in == tag.out_0) ? valid_0 : valid_1);
(evict_sel ? valid_1 : valid_0);

assign dirty = evict_sel ? dirty_1 : dirty_0;



assign evict_sel = (~valid_0) ? 1'b0 : (~valid_1) ? 1'b1 : victimary;

assign cache_data_out = hit_0 ? data.out_0 : data.out_1;

assign DataOut = cache_data_out;

assign cache_wr_0 = cache_write ? (hit_0 | (~evict_sel)) : 1'b0;

assign cache_wr_1 = cache_write ? (hit_1 | evict_sel) : 1'b0;