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A CMOS Fish Freshness to Continuous-Time Incremental Sigma-Delta Modulator for Monitoring Fish Freshness in Fish Markets

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***Abstract* - In this paper, a CMOS fish freshness to continuous-time incremental sigma-delta modulator for monitoring fish freshness in fish market is proposed for Internet of Things (IoT) techniques. The chip is fabricated in the TSMC 0.35 µm 2P4M CMOS technology with 3.0 V power supply. Furthermore, by using MATLAB and SPICE programs, all the performance and functions of the proposed fish freshness to continuous-time incremental sigma-delta modulator have been correctly verified and proven in simulations. The chip size is 1.26 × 2.69 mm². The proposed chip is aimed to be applied in detecting fish freshness in fish markets.**

Index Terms – Fish freshness, Internet of Things (IoT), Continuous-Time Incremental Sigma-Delta Modulator (CT-ISDM).

I. INTRODUCTION

As we know, many people eat fish every day. Therefore, fish freshness becomes especially important to human health. Till now, several studies [1] - [16] have been proposed for detecting food spoilage. Among them, [1] had also been developed for the same purpose. However, when [1] is followed, whole system resolution is always limited by its periodical output signal. Thus, to increase whole system resolution, it is the aim of this work. The whole block diagram of the proposed chip is shown in the Figure 1. By utilizing the proposed chip, whole system resolution can not only be increased, but also can immune the environmental noise in fish markets.

A CMOS fish freshness to continuous-time incremental sigma-delta modulator for monitoring fish freshness in fish markets is proposed. The chip is fabricated in the TSMC 0.35 µm 2P4M CMOS technology with 3.0 V power supply. Furthermore, by using MATLAB and SPICE programs, all the performance and functions of the proposed fish freshness to continuous-time incremental sigma-delta modulator have been correctly verified and proven in simulations.

Section II provides all the structures design of block schematics and simulation results of the proposed fish resistance transducer. Section III reports the final conclusion and the expectation for further works.

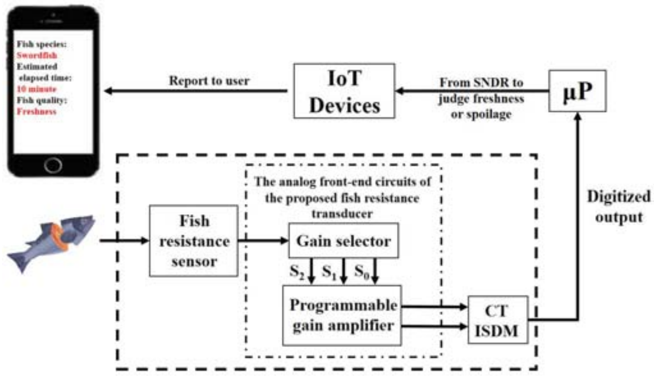

Fig. 1. The whole block diagram of the proposed chip for monitoring fish freshness in fish markets.

II. THE STRUCTURES DESIGN AND SIMULATION RESULTS OF THE PROPOSED FISH RESISTANCE TRANSDUCER

A. *Fish resistance sensor*

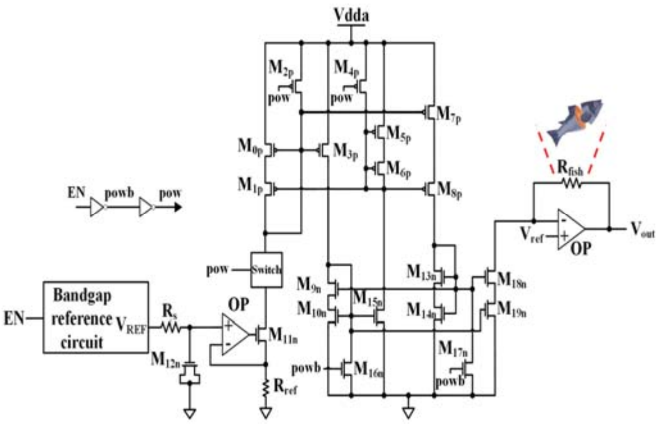

Fig. 2. The proposed circuit schematic of the fish resistance sensor.

In the Figure 2, the bandgap reference circuit gives a stable voltage V_{REF}, then V_{REF} through the resistance R_{ref} is transformed into a current. After processing by the current mirror, the voltage V_{out} is obtained when the current flows through the fish resistance R_{fish}.

B. *Analog front-end circuits of the proposed fish resistance transducer*

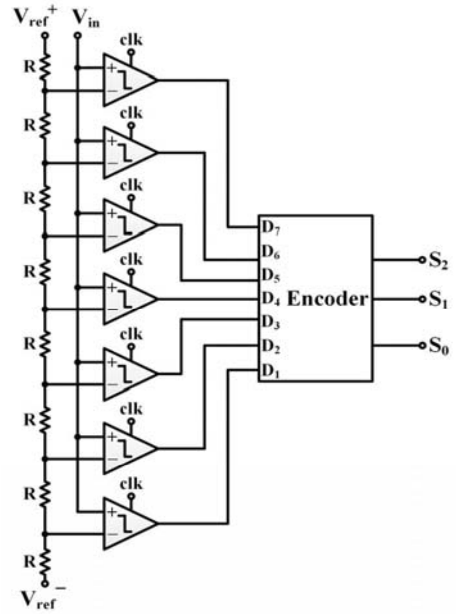

Fig. 3. The proposed circuit schematic of gain selector.

The voltage V_{in} in the Figure 3 is equal to the output voltage of the fish resistance sensor V_{out}. The proposed gain selector can uniformly quantize the V_{in} into digital codes S_2 to S_0. The proposed programmable gain amplifier is shown in the Figure 4. The gain which is shown in the Figure 5 is distributed from 16.09 dB to 23.9 dB and corresponds to codes 000 to 111. The differential inputs V_{in}^{+} and V_{in}^{-} are externally generated by a differential oscillator and the frequency is 5 kHz. Afterward, the differential outputs are connected to the inputs of the proposed CT-ISDM.

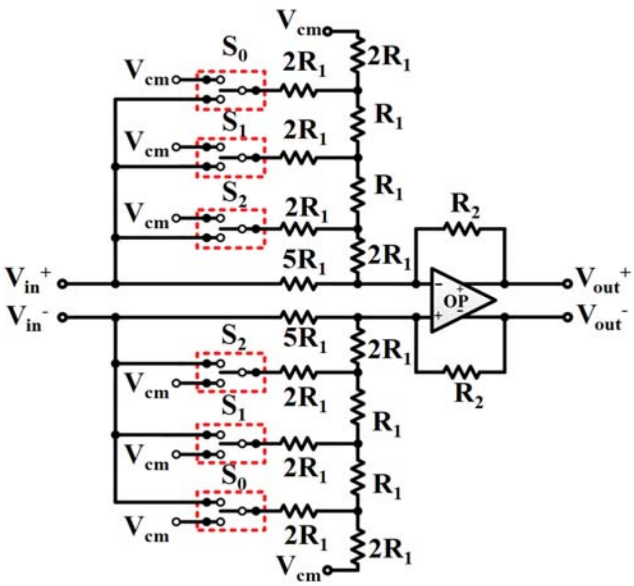

Fig. 4. The proposed circuit schematic of the programmable gain amplifier.

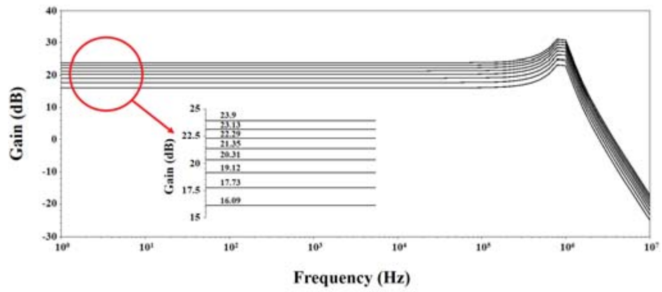

Fig. 5. The frequency response simulation of the programmable gain amplifier.

C. The proposed CT-ISDM

The topology of the proposed CT-ISDM is shown in the Figure 6. It includes a single bit DAC, a single bit quantizer, an excess loop delay (ELD), three integrators, and the gain circuits including feedforward a_1 to a_3, b_1 to b_3 and feedback c_1 to c_2, and g. The noise transfer function is derived by

$$\mathrm{NTF}(s) = \frac{S^3 + (a_3 g)S}{S^3 + (b_1 c_1 + b_3 c_2)S^2 + (a_3 g + b_2 b_3 c_1)S + (a_2 a_3 b_3 c_1 + a_3 b_1 c_1 g)} \quad (1)$$

where a_1 to a_3, b_1 to b_3, c_1 to c_2, and g represent the coefficients of the proposed CT-ISDM. Calculating the $\mathrm{NTF}_{\mathrm{filter}}$ carefully, it could be resulted as

$$\mathrm{NTF}_{\mathrm{filter}}(s) = \frac{S^3 + (0.002313)S}{S^3 + (0.333694)S^2 + (0.07807)S + 0.013728} \quad (2)$$

Figure 7 and 8 which are the pole-zero graph and s-plane graph respectively show the simulations of the $\mathrm{NTF}_{\mathrm{filter}}$ for stability by applying MATLAB programs. In the Figure 7, it shows all the roots of the $\mathrm{NTF}_{\mathrm{filter}}(z)$ are located in the unit circle. In the Figure 8, it shows all the roots of the $\mathrm{NTF}_{\mathrm{filter}}(s)$ are located on the left of the jw axis. Hence, it shows that $\mathrm{NTF}_{\mathrm{filter}}$ can work stably.

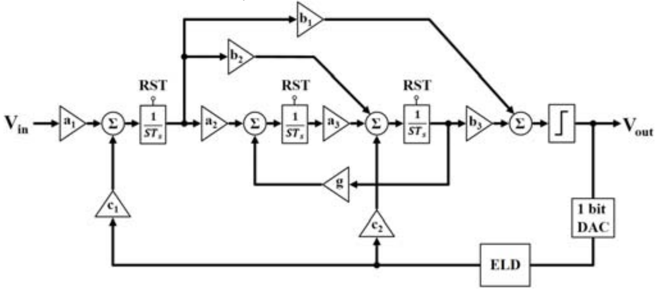

Fig. 6. The topology of the proposed CT-ISDM for monitoring fish freshness in fish markets.

SPICE simulation programs are used to obtain the output codes of the CT-ISDM after establishing the whole circuits. Afterwards, these digital codes are calculated to obtain the SNDR through dedicated MATLAB programs.

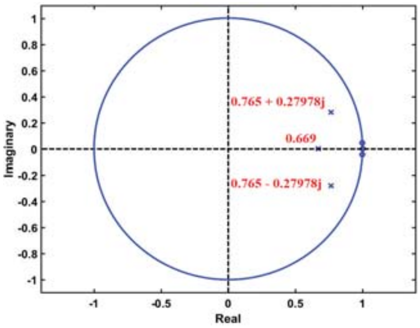

Fig. 7. The pole-zero graph of the $NTF_{filiter}(z)$.

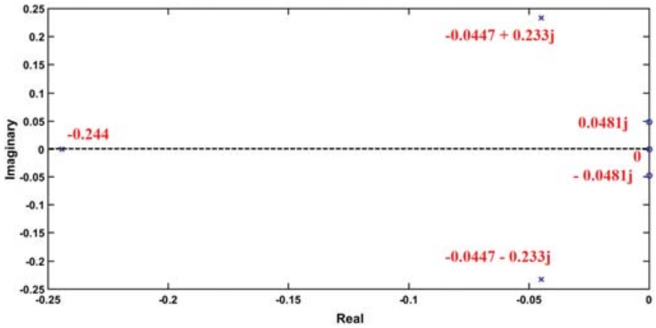

Fig. 8. The s-plane graph of the $NTF_{filiter}(s)$.

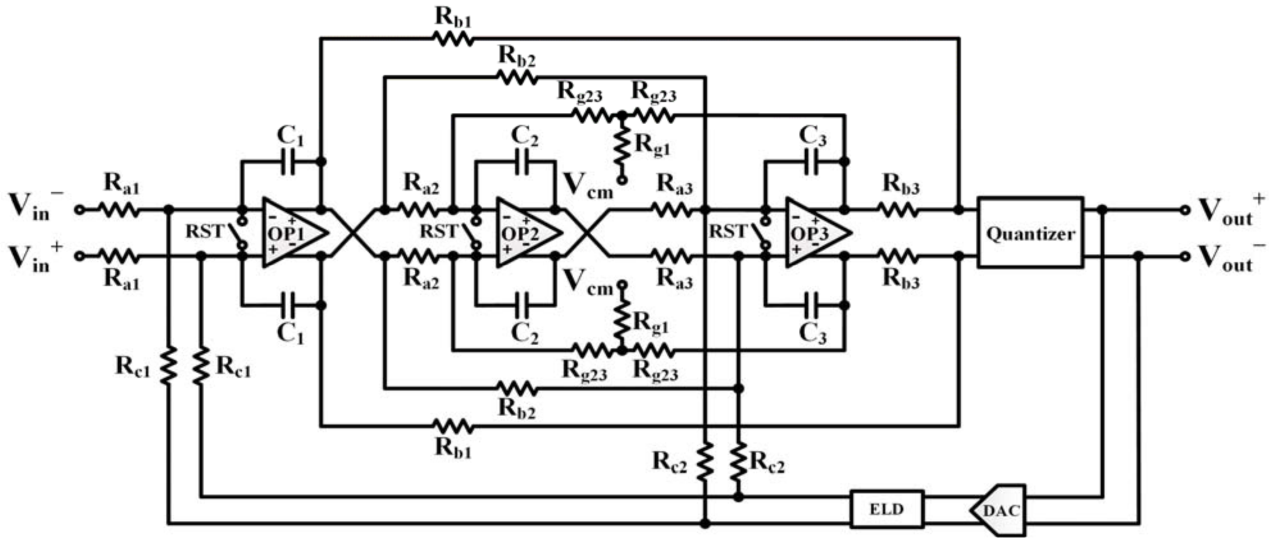

Fig. 9. The circuit schematic of the proposed CT-ISDM.

Figure 9 shows the circuit schematic of the proposed CT-ISDM. It adopts 2 MHz as the sampling frequency and 50 as the oversampling ratio (OSR), respectively. The RST signal is designed to reset the integrators after each 50 clock cycles. The peak SNDR of the proposed CT-ISDM is achieved 82.9 dB as the input amplitude at 850 mV as shown in the Figure 10. The result shows the proposed CT-ISDM has successfully reached 13-bit resolution. Figure 11 displays simulation results for SNDR versus input level. The dynamic range is 84.61 dB.

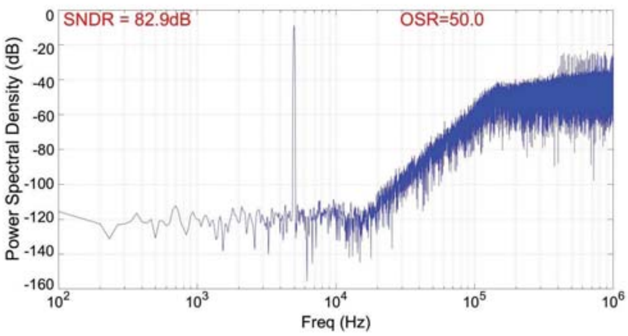

Fig. 10. The output spectrum of the proposed CT-ISDM at the maximum signal amplitude 850 mV. The $SNDR_{peak}$ can be achieved 82.9 dB.

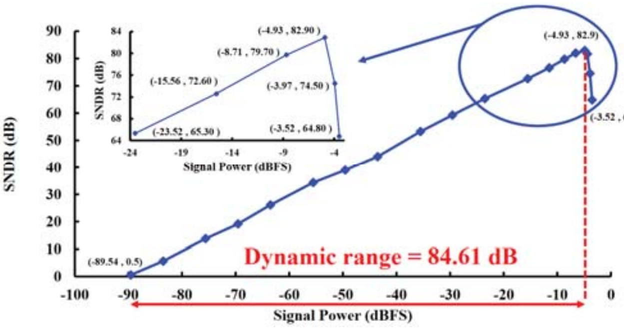

Fig. 11. The SNDR of the proposed CT-ISDM versus input signal level.

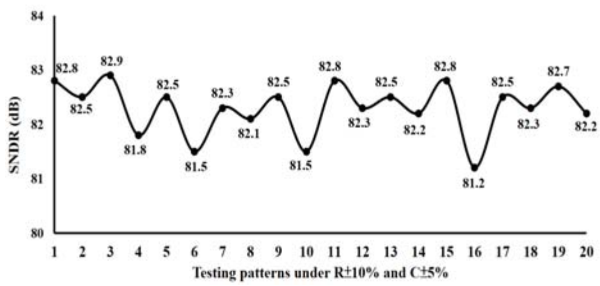

Fig. 12. The SNDR of testing patterns under R±10% and C±5%.

Figure 12 reveals the results of SNDR by adjusting resistance value and capacitor value under ±10% and ±5% respectively. From simulations, this result explains 13-bit resolution is also ensured.

Finally, the relationship of fish resistance with time is shown in the Figure 13. Then, utilizing the information and cooperating with the fish resistance sensor, the proposed fish resistance transducer and the proposed CT-ISDM. The simulation results are shown in the Figure 14 and 15. The time shown in the Figure 13 and the Figure 15 represents that the fish has been placed in normal temperature during the time.

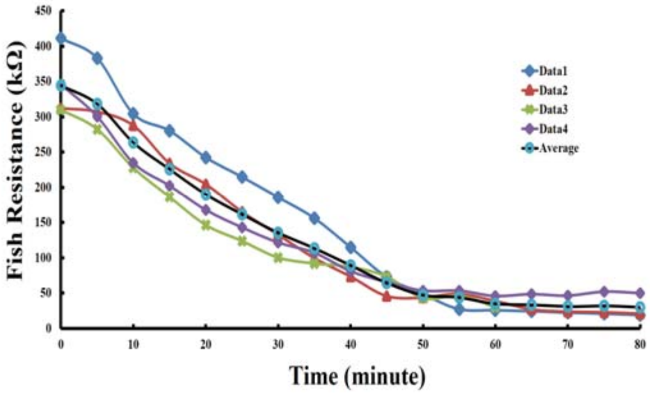

Fig. 13. Time to Fish resistance.

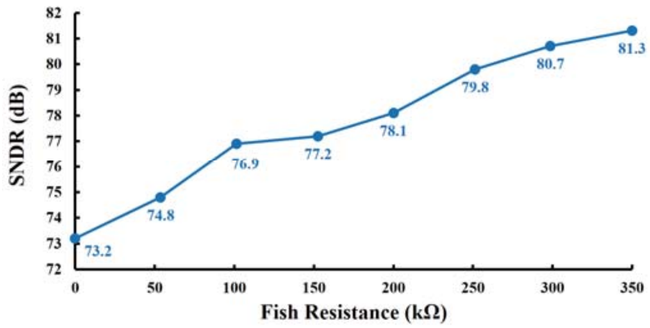

Fig. 14. Fish resistance to SNDR.

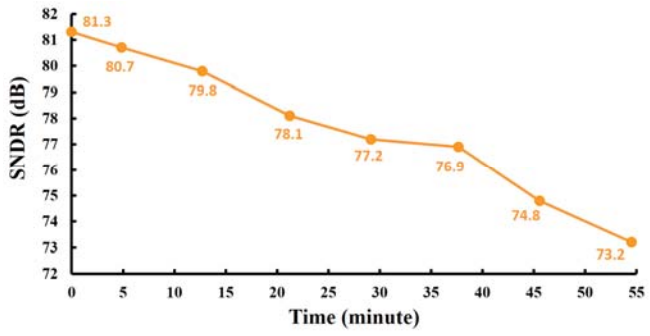

Fig. 15. The SNDR versus the time.

Figure 16 displays the layout diagram of the proposed chip. The layout area is 1.26×2.69 mm^2. The performance of the proposed fish freshness to continuous-time incremental sigma-delta modulator for monitoring fish freshness in fish markets are stated in Table I.

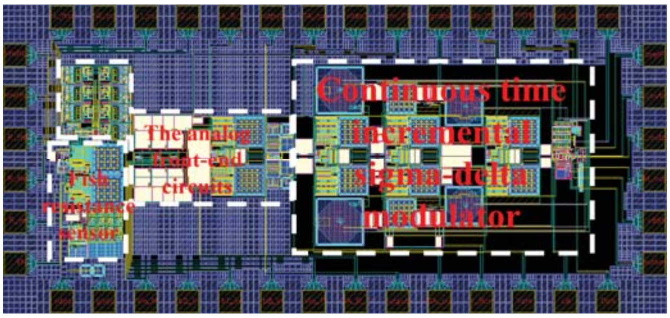

Fig. 16. The layout diagram of the whole chip.

TABLE I
SUMMARY OF THE PERFORMANCE OF THE PROPOSED FISH FRESHNESS TO CONTINUOUS-TIME INCREMENTAL SIGMA-DELTA MODULATOR FOR MONITORING FISH FRESHNESS IN FISH MARKET.

Technology	0.35μm 2P4M CMOS
Supply voltage	3 V
Oversampling ratio	50
Clock frequency	2 MHz
Chip area	1.26×2.69 mm^2
Dynamic range	84.61 dB
SNDRpeak	82.9 dB
PGA gain range	16.09 to 23.9 dB
SNDR versus fish resistance from 0 Ω to 350 kΩ	73.2 to 81.3 dB
Application field	Fish resistance transducer

III. CONCLUSION

The size of chip is 1.26×2.69 mm^2 and the chip is implemented by TSMC 0.35 μm 2P4M CMOS technology with 3.0 V power supply. Furthermore, all the performance and functions of the proposed fish freshness to continuous-time incremental sigma-delta modulator have been correctly verified and proven in simulations by MATLAB and SPICE programs. It will be tested to monitor fish freshness in fish markets in the future.

ACKNOWLEDGMENT

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